Very Low V_t [Ir-Hf]/HfLaO CMOS Using Novel Self-Aligned Low Temperature Shallow Junctions

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Abstract

We report very low V_t [Ir-Hf]/HfLaO CMOS using novel self-aligned low-temperature ultra shallow junctions with gate-first process compatible with current VLSI. At 1.2 nm EOT, good $\phi_{m\text{-}eff}$ of 5.3 and 4.1 eV, low V_t of +0.05 and 0.03 V, high mobility of 90 and 243 cm^2/Vs, and small 85°C BTI <32 mV (10 MV/cm, 1 hr) are measured for *p*- and *n*-MOS.

Undesired high V_t & EOT scaling challenges

The major challenge for metal-gate/high-κ CMOSFET is to lower the undesired high V_t, while the detailed mechanisms are still not clear yet [1]-[6]. One method to address this issue is to compensate the high V_t by using proper dual metal-gates, which have an effective work-function ($\phi_{m\text{-}eff}$) lower than the target 4.1 eV for *n*-MOS, and higher than the needed 5.2 eV for *p*-MOS. Although Lanthanide-silicide FUSI (Yb_xSi) [2] and TaC gates work well for *n*-MOS, the choice of an appropriate metal gate for *p*-MOS is especially difficult. This is because only Pt and Ir in the Periodic Table have a required work-function greater than the target 5.2 eV [2], but Pt is also difficult to be etched by RIE. Previously, we showed that Ir_3Si/HfLaON *p*-MOS [1] has the needed high $\phi_{m\text{-}eff}$ of 5.08 eV and low V_t of -0.1 V at 1.6 nm equivalent-oxide-thickness (EOT), even after ion implant activation of a 1000°C RTA. Unfortunately, further scaling EOT to 1.2 nm, reduces flat-band voltage (V_{fb}) of these devices to produce an undesirable high V_t. Since this approach was not successful, a fundamental understanding of the high V_t and V_{fb} roll-off is necessary, when EOT is scaled.

In this paper, we report a new method to address these basic challenges. At 1.2 nm EOT, the self-aligned and gate-first [Ir-Hf]/HfLaO *p*- and *n*-MOS showed proper $\phi_{m\text{-}eff}$ of 5.3 and 4.1 eV, low V_t of +0.05 and 0.03 V, together with high mobility of 90 and 243 cm^2/Vs and good 85°C BTI reliability. This good device performance was achieved by using a novel low-temperature (<900°C) ultra-shallow junction (*USJ*) process, which lowers the interface reaction exponentially compared with a conventional 1000°C RTA needed for dopant activation. Besides, the measured *USJ* depth (X_j) was only 9.5~20 nm for p^+/n case. The X_j for n^+/p was 23~35 nm, better than that for a 1 keV As^+ implant [7] at the same sheet resistance (R_s). This is due to a reduction of defect-assisted diffusion arising from ion implant damage. These results compare well with previous work [1]-[6], and display a lower V_t and smaller EOT, with a self-aligned *USJ* and gate-first process that is compatible with VLSI.

Experimental Details

The Metal-gate/HfLaO *C*MOSFET process included depositing HfLaO using PVD [1], a post-deposition anneal, and TaN/Ir and Ir/TaN/Hf deposition. After gate patterning, self-aligned 5 nm Ga or 10-nm-Ni/5-nm-Ga (with top 100 nm SiO_2 capping layer) was deposited for *p*-MOS, followed by 550~900°C RTA solid-phase diffusion (SPD). For *n*-MOS, NiAl-silicide Schottky contact for sub-45-nm node was made [8], or self-aligned H_3PO_4 was spun deposited, transformed to P_2O_5 at 200°C and SPD at 850~900°C RTA. Such wet H_3PO_4 spray and doping processes are used for commercial Si solar cell manufacture. Finally, source-drain metal contacts were added. For comparison, [Ir_3Si-Hf_xSi]/HfLaON CMOS using B^+ and As^+ implant and 1000°C RTA were also fabricated [1].

Results and Discussion

A. V_{fb} roll-off at scaled EOT:

Fig. 1 shows the *C-V* characteristics of HfLaON *C*MOS after a 1000°C RTA, where EOT of 1.6 and 1.2 nm are determined using a quantum-mechanical *C-V* simulation. A low V_{fb} is obtained for *n*-MOS using an Hf_xSi gate at 1.2nm EOT; however, the V_{fb} is reduced for the Ir_3Si/HfLaON *p*-MOS. Since the same Ir_3Si metal-gate was used for the HfLaON, the unwanted lower V_{fb} at thinner EOT may be attributed to the higher oxide charge density as described by the V_{fb} equation in Fig. 2. These charges arise from inevitable charged vacancy and dangling bonds in non-stoichiometric oxides (x<2) from interface reaction and inter-diffusion:

$$Si + HfO_2 \xrightarrow{\Delta} SiO_x + HfO_{2-x} \qquad (x < 2) \qquad (1)$$

Such reactions are possible at high temperature owing to the similar bond enthalpies of 800 and 802 kJ/mol for respective SiO_2 and HfO_2 [2]. Also at thinner EOT, only thin interfacial SiO_2 is permissible to meet the required high κ value for low leakage current. Since the interfacial chemical reactions follow Arrhenius temperature dependence, we aimed to develop a low temperature process to reduce such effects.

B. Low temperature shallow junctions:

Figs. 3-6 show the R_s, *J-V* and SIMS of p^+/n junctions for different cases. Adding Ni to Ga SPD improves the R_s through Ni-Ga co-diffusion and silicide formation while maintaining good p^+/n characteristics with an ideality factor (n) of 1.36. A *USJ* X_j of 9.5 and 20 nm was measured by SIMS for the Ga and Ni/Ga cases. Figs. 7-10 show the R_s, *J-V* and SIMS of n^+/p junctions. Although the NiAl-silicide Schottky contact has an n of 1.9, the self-aligned H_3PO_4 spin

process improves n to 1.4, gives a 10X smaller leakage and a low R_s. A *USJ* X_j of 23 or 35 nm was measured by SIMS after 850 or 875°C RTA – this is better than that for a 1 keV As^+ implant and spike RTA at the same R_s [7]. This is due to the free from defect-assisted diffusion caused by As^+ implant damage. This ≤900°C process temperature is important for HfLaO in preserving its amorphous structure at 900°C (as shown in Fig. 11) without using the nitrided HfLaON, which reduces the possible pinning at metal-gate/high-κ interface. The amorphous structure of HfLaO at 900°C is better than crystallized HfO_2 for achieving good BTI, by avoiding charge trapping at poly-HfO_2 grain boundaries [1]-[3].

C. Device characteristics:

Figs. 12-15 are the *C-V* and *J-V* characteristics of TaN/Ir and Ir/TaN/Hf on HfLaO devices. At 1.2 nm EOT, the gate leakage current was only 2.4×10^{-4} and 1.8×10^{-4} A/cm^2 at ±1 V. Fig. 16 shows the *J-EOT* plot, where much better leakage current than SiO_2 is obtained at 1.2 nm EOT. Reducing the RTA temperature to <900°C is vital for choosing proper $\phi_{m\text{-}eff}$ pure metal gate electrode, since Ir/HfLaO failed after 1000°C RTA due to Ir diffusion through the high-κ dielectric [2].

Note that the V_{fb} of TaN/Ir/HfLaO at 850°C is 0.7 V larger than TaN/Ir_3Si/HfLaON at 1000°C in Fig. 1. To understand this large improvement, we have plotted the V_{fb}-EOT in Fig. 17 and proper $\phi_{m\text{-}eff}$ of 5.3 and 4.1 eV are obtained for p- and n-MOS. The $\phi_{m\text{-}eff}$ at top Ir interface is only 0.3 eV higher than Ir_3Si (5.0 eV) and insufficient to explain the large 0.7 V V_{fb} roll-off. Since similar high-κ was used, the undesired V_{fb} lowering is attributed to the charges in non-stoichiometric oxides in *eq.* (1) – these being created during the higher 1000°C RTA for the Ir_3Si/HfLaON case. Such oxide vacancies can be predicted theoretically, and can create lower energy traps within the HfO_2 [9]. This may be one of the reasons for pinning the $\phi_{m\text{-}eff}$ to Si midgap via lower energy barrier trap-assisted conduction. This interface reaction reduces exponentially when reducing the process temperature to <900°C for the Ir/HfLaO devices.

The I_d-V_d, I_d-V_g and μ_{eff}-E characteristics of [Ir-Hf]/HfLaO p- and n- MOSFETs are shown in Figs. 18-20, respectively. Good transistor characteristics, low V_t of +0.05 and 0.03 V and high mobility of 90 and 243 cm^2/Vs are measured. The improved mobility, compared with 1000°C RTA HfLaON CMOS, is consistent with lower charged vacancies associated with interfacial reactions in *eq.* (1). The gate reliability is shown in the BTI data of Fig. 21, where a small ΔV_t<32 mV occurs for CMOS stressed at 10 MV/cm and 85°C for 1 hr. Such good BTI reliability is due to the amorphous structure of HfLaO under ≤900°C process temperature, which prevents BTI degradation by carrier-trapping in poly grain boundaries of HfO_2 case. Table 1 compares various metal-gate/high-κ CMOS data [1]-[6]. The merits of self-aligned [Ir-Hf]/HfLaO p-and n-MOS with SPD *USJ* are proper $\phi_{m\text{-}eff}$ of 5.3 and 4.1 eV, low V_t of +0.05 and 0.03 V, high mobility of 90 and 243 cm^2/Vs, and small BTI <32 mV (85°C, 10 MV/cm & 1 hr). Our results are comparable with or better than the best reported data for metal-gate/high-κ CMOS [1]-[6], with a small 1.2 nm EOT, and using a self-aligned and gate-first process compatible with VLSI line.

Conclusions

We have shown that the interfacial reactions are key factors for V_{fb} roll-off that then yields an undesired high V_t for highly-scaled EOT. Our ultra-shallow junction process, performed at ≤900°C, produced appropriate $\phi_{m,eff}$ values, small leakage and low threshold voltages for [Ir-Hf]/HfLaO CMOS devices.

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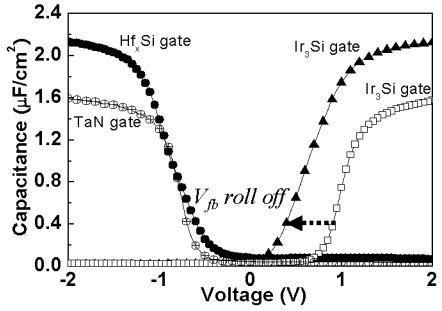

Fig. 1. *C-V* of metal-gate/HfLaON CMOS after 1000°C RTA. The $|V_{fb}|$ roll-off with EOT scaling indicates the importance of the interface.

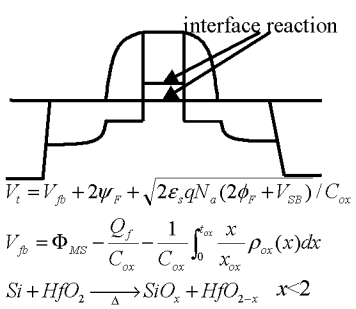

Fig. 2. The $|V_t|$ increase can arise from top and bottom interface. The charged oxide vacancies in non-stoichiometric SiO_x and HfO_{2-x} can modify V_{fb} and increase $|V_t|$.

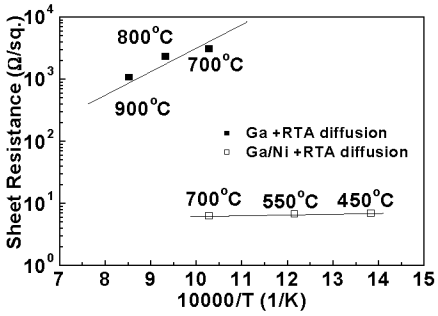

Fig. 3. R_s of Ga and Ni/Ga, formed by Solid Phase Diffusion (SPD), as a function of RTA temperature.

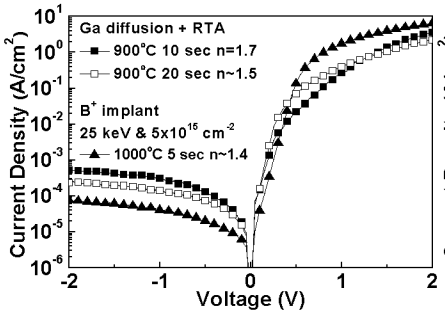

Fig. 4. *J-V* of p^+/n junction formed by SiO_2/Ga SPD at 900°C RTA, and a control B^+ implantation at a 1000°C RTA.

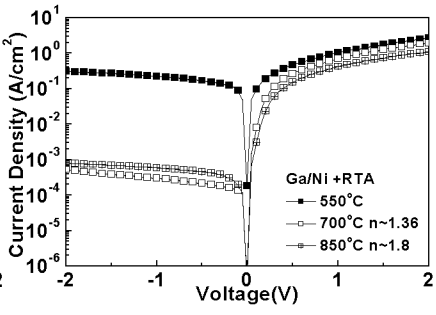

Fig. 5. *J-V* of p^+/n junction for SiO_2/Ni/Ga SPD at 550~850°C RTA. Leakage and *n* factors were comparable with the Ga 900°C SPD but formed at a lower temperature.

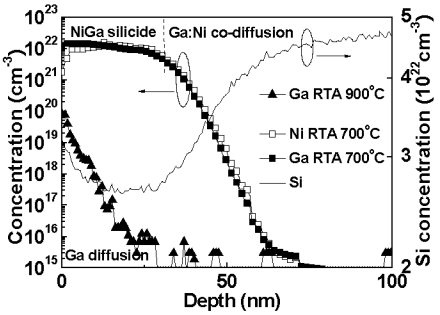

Fig. 6. SIMS profile of Ga and Ni/Ga-silicide, with ultra shallow junctions of 9.5 or 20 nm at SPD of 900°C or 700°C RTA. The X_j *is* defined at 10^{18} cm^{-3} in [7].

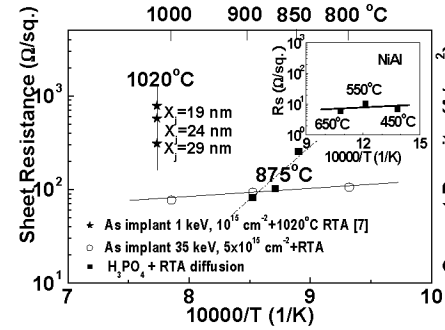

Fig. 7. Variation R_s of NiAl (insert), H_3PO_4 spin SPD and As^+ implant with RTA condition. Data for the 1 keV As^+ implant and 1020°C RTA are from [7].

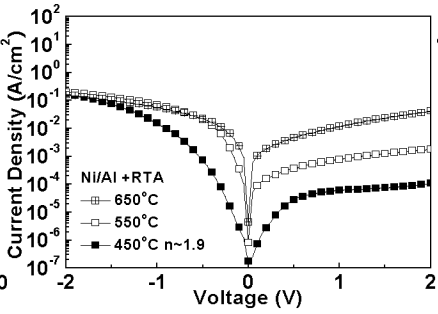

Fig. 8. *J-V* of n^+/p junction with NiAl Schottky contact. Although R_s<10 Ω/sq, the leakage and *n* are poor.

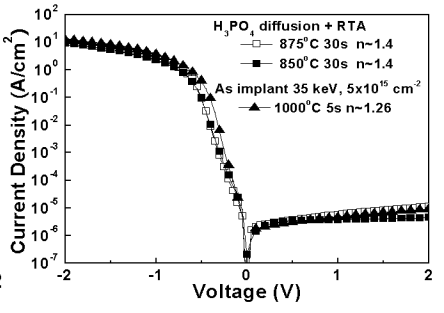

Fig. 9. *J-V* of n^+/p junctions made by H_3PO_4 spin SPD at 850 and 875°C RTA. The leakage and *n* are similar to those for the As^+ implant and 1000°C RTA case.

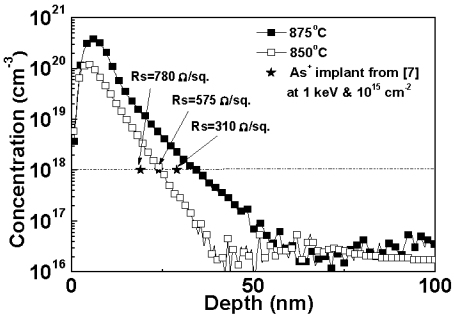

Fig. 10. Phosphorus SIMS profile for H_3PO_4 spin SPD, with X_j of 23 and 35 nm, for 850 and 875°C RTAs. The X_j data from [7] are included for comparison.

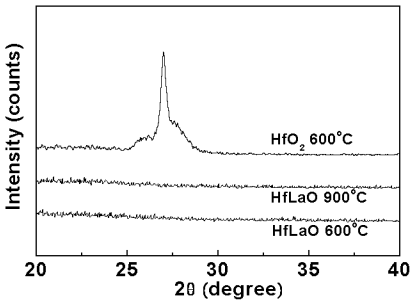

Fig. 11. Grazing incident XRD spectra of HfLaO after 600°C and 900°C 30 sec RTA. Amorphous structure w/o crystallization is still preserved and is important for BTI.

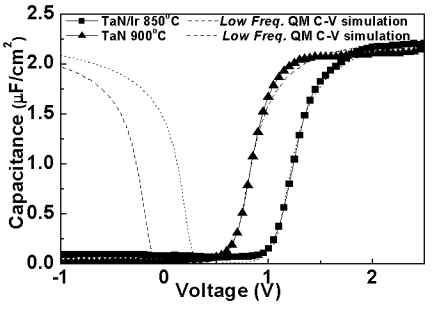

Fig. 12. *C-V* of HfLaO *p*-MOS with TaN/Ir and TaN gates, after 850 and 900°C RTAs. V_{fb} is 0.7 V higher than for Ir_3Si/HfLaON after a 1000°C RTA (Fig. 1).

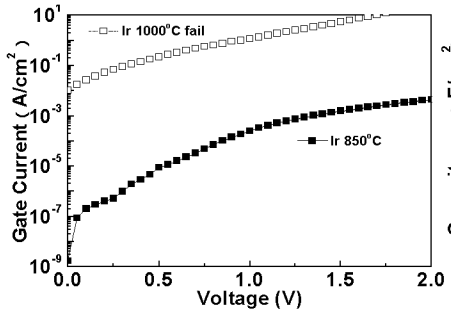

Fig. 13. *J-V* of HfLaO *p*-MOS with TaN/Ir gate after 850°C or 1000°C RTA. Low leakage current occurs for a 850°C RTA but fails at 1000°C because of metal diffusion.

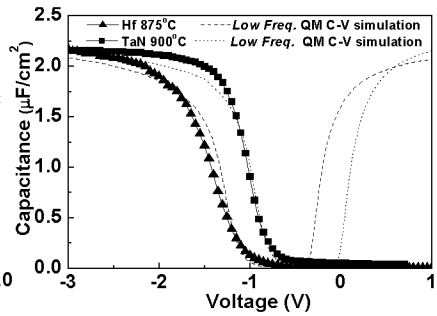

Fig. 14. *C-V* of HfLaO *n*-MOS with Ir/TaN/Hf and TaN gates after 875 and 900 °C RTAs. Data from a quantum-mechanical C-V simulation are included.

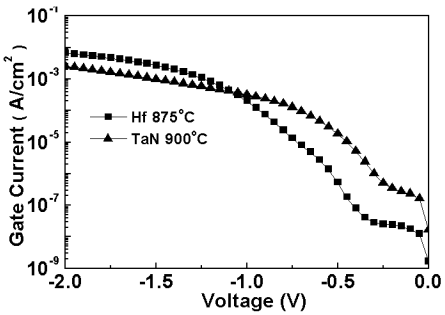

Fig. 15. *J-V* of HfLaO *n*-MOS with Ir/TaN/Hf and TaN gates, after 875 and 900°C RTAs.

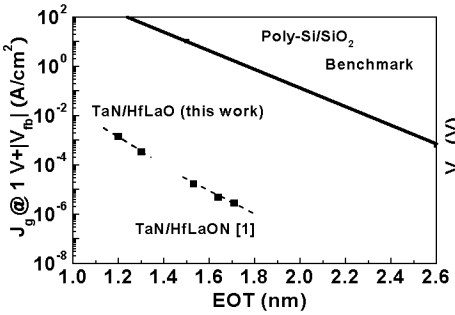

Fig. 16. Gate leakage current density for HfLaO at 1.2 nm EOT, compared with SiO_2 and HfLaON [1].

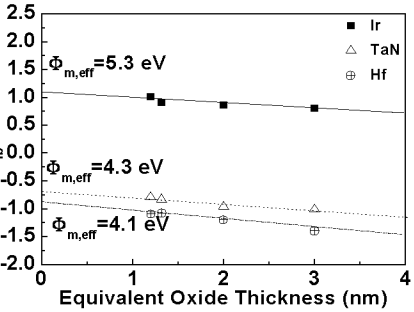

Fig. 17. V_{fb}-*EOT* for Ir, TaN and Hf gates. Effective work-functions are 5.3, 4.3 and 4.1 eV.

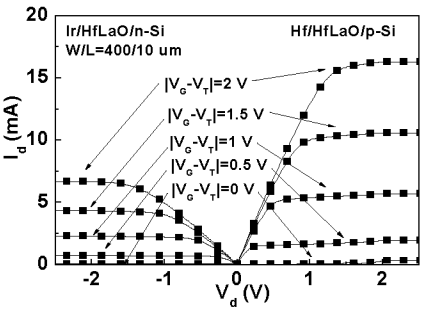

Fig. 18. I_d-V_d of self-aligned and gate-first *p*- and *n*-MOSFETs.

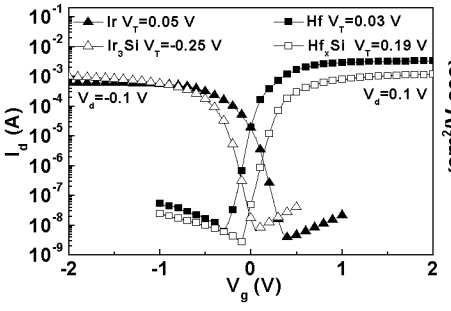

Fig. 19. I_d-V_g of self-aligned & gate-first *p*- and *n*-MOSFETs, compared with dual gated [Ir_3Si-Hf_xSi]/HfLaON CMOS (1000°C RTA).

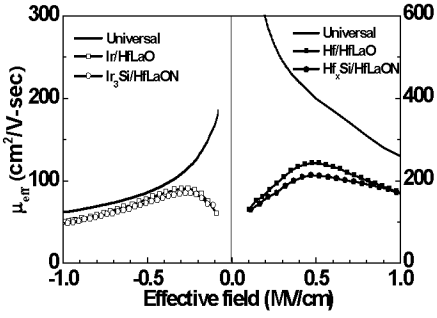

Fig. 20. Hole and electron mobility of self-aligned gate-first CMOSFETs compared with [Ir_3Si-Hf_xSi]/HfLaON CMOS (1000°C RTA).

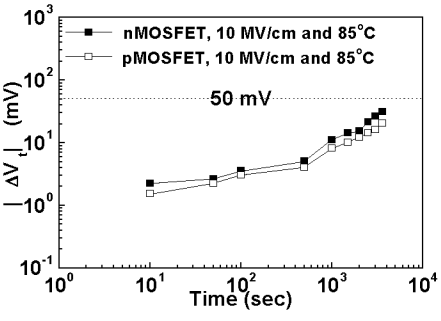

Fig. 21. The ΔV_t shift for dual-gated HfLaO CMOSFETs stressed at 85°C and 10 MV/cm for 1 hour.

High-κ	Metal-Gate, *p/n*	EOT (nm)	$\phi_{m\text{-}eff}$ (eV), *p/n*	V_t (V), *p/n*	Process Temp.	Mobility (cm^2/Vs), *p/n*
This work HfLaO	**Ir / Hf**	**1.2**	**5.3 / 4.1**	**+0.05 / 0.03**	**<900°C SPD**	**90 / 243**
This work HfLaON	**Ir_3Si / Hf_xSi**	**1.2**	**5.0 / 4.3**	**-0.25 / 0.19**	**1000°C**	**86 / 214**
HfLaON [1]	Ir_3Si / TaN	1.6	5.08 / 4.28	-0.1 / 0.18	1000°C	84 / 217
HfAlON [2]	Ir_xSi / Yb_xSi	1.7	4.9 / 4.15	-0.29 / 0.1	950°C/Low T. FUSI	80 / 180
HfTaO [3]	- / TaN	1.6	-/ 4.6	- / -	1000°C	- / 354
HfSiON [4]	$Ni_{31}Si_{12}$ / NiSi	1.5	~4.8 / ~4.5	-0.4 / 0.5	Low Temp. FUSI	~70 / ~240
HfSiON [5]	NiSiGe / -	1.3	- / -	-0.5 / -	Low Temp. FUSI	70 / -
HfSiON [6]	Ni_3Si / $NiSi_2$	1.7	4.8 / 4.4	-0.69 / 0.47	Low Temp. FUSI	65 / 230

Table 1. Comparison of device integrity data for various metal-gate/high-κ *n*- and *p*-MOSFETs.