國 立 交 通 大 學

光電工程學系碩士班

碩士論文

應用於主動畫素感測器之元件的雜訊分析與補償方法

Noise Analysis and Compensation Method for the Device in the Application of Active Pixel Sensor

研 究 生：楊詠暄　　Student : Yung-Hsuan Yang

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中華民國 一百零二 年 六 月

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A Thesis
Submitted to Institute of Electro-Optical Engineering
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of Master
in
Institute of Electro-Optical Engineering

June 2013

Hsinchu, Taiwan, Republic of China

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摘 要

主動畫素感測器因可將感測電壓加以放大，故可提供較強的輸出訊號，但仍需符合高解析度及低雜訊的要求。由於輸出訊號受畫素感測電路中薄膜電晶體間的差異如截止電壓偏移或載子移動率不同等的影響，會造成感測誤差，需要加以補正。此外，目前有數種薄膜電晶體技術可供選擇，我們以雜訊的觀點來比較其特性。

本篇論文研究重點有兩個部分，第一部分對不同材質之電晶體雜訊加以量測及分析，之後利用其提出之雜訊公式計算各個受測元件的訊雜比值，並且說明何種材料的電晶體具有較好的特性，以利用於電路設計。第二部分則基於利用兩個薄膜電晶體、兩個儲存電容以及兩條控制掃描線的最簡設計下，提出輸入已知電流的校正方法，以達到補償截止電壓、載子移動率等元件變動的目的，並利用實際操作來驗證其功能。

經由此研究，我們可確認此高解析度、高敏感性與高精確度的主動式感測電路設計，並以所提出的元件雜訊分析的方法，判斷出最適合感測電路使用的薄膜電晶體技術。

Noise Analysis and Compensation Method for the Device in the Application of Active Pixel Sensor

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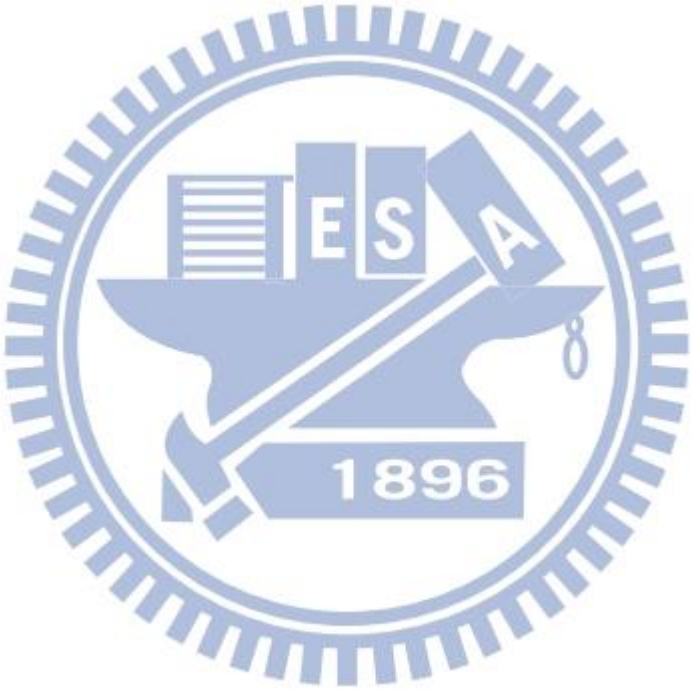
Abstract

The active pixel sensor can amplify sensing voltage, and it can provide a stronger output signal. However, it still needs to meet the requirements of high-resolution and low noise. Because the output signal can be affected by the variation of thin film transistor, such as the threshold voltage shift or the difference in mobility, the sensing error can be induced and needs to be corrected. In addition, currently, there are kinds of thin film transistor technologies. Their characteristics are studied in the view point of noise performance.

This thesis focuses on two parts. The first is the noise measurement and analysis for the transistors made of different materials. A noise formula is newly proposed to calculate the signal-to-noise ratios for the devices under test. Based on that analysis, we explain how the transistor technology suitable for the application in active pixel sensing circuit can be properly determined. The second part is based on the simplest sensing circuit containing only two thin film transistors, two storage capacitors and

two scan lines. The calibration method of applying bias currents is proposed to compensate the variations in threshold voltage, mobility, etc. The method is verified in its function experimentally.

In this study, we confirm the active X-ray sensing array can be high resolution, high sensitivity and high accuracy. In addition, the analysis of noise helps to determine the appropriate thin-film transistor technology for the sensing circuit.



Acknowledgements

在這兩年碩士生涯，首先要感謝我的指導教授戴亞翔博士，老師給予我專業上的知識，使我能夠在這研究領域裡成長與進步。除此之外，老師還時常教導我分析數據的技巧以及處事態度，都讓我受益無窮。並且，老師對於論文內容的嚴謹要求以及不辭辛勞地修訂，更是令我感激不已。我很榮幸能夠當老師的碩士研究生，因為您讓我在最後的求學階段能夠有個美好句點。在此，對老師致上最深的敬意。

另外還必須感謝這兩年陪伴我的人。感謝博班的祿盛學長以及碩班的柏成、政達和承旻學長，願意在我困難的時候伸手幫助我解決問題，也會分享專業上的知識。感謝同一屆實驗室的同學君毅和嘉鴻，我們一起修課一起度過許多的難關，也一起完成了學位。也要感謝學弟俊佑、忠倫和亞瑋的熱情幫忙，讓我的實驗能夠順利完成。因為有你們的加入，才讓我的碩士班兩年生活充實且精采。最後要感謝的是家人以及淑玉的支持以及鼓勵，有了你們的陪伴，我才能順利取得碩士學位，最後在此向你們獻上最誠摯的感謝。

詠暄　2013.6.27

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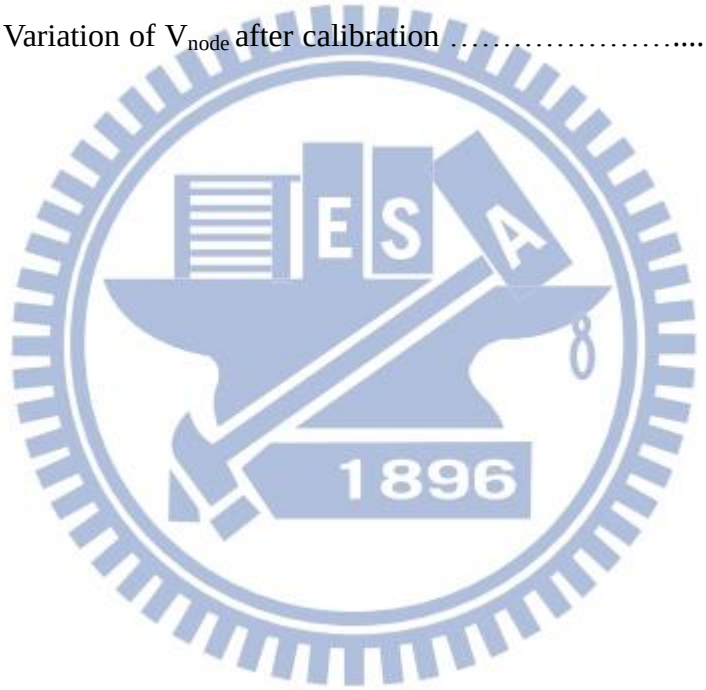


Chapter 1

Introduction

1.1 Background

X-ray is a form of electromagnetic radiation, and its range of frequencies from $3x10^{16}$ Hz to $3x10^{19}$ Hz. X-ray has a number of advantages such as through soft substances easily and be partially blocked by dense substances, and it can form a high-contrast image on the imaging device. As a result, X-ray is often used in medical application because it provides a painless procedure to take images which inside of the body. Although X-ray is very useful and powerful, its non-portable equipment is inconvenient and expensive. And it is well known that exposure to radiation is very harmful. Therefore, it is necessary to reduce the risk of exposure to X-ray for patients' safety. For the above reasons, X-ray equipment is rapidly evolving. In order to improve the convenience and the safety, the next generation which is called digital flat panel detectors is a combination of the X-ray photography and the flat panel display technique.

Active matrix flat panel technology based on thin-film transistors (TFTs) has been recently extended to digital x-ray diagnostic medical imaging. Digital detectors provide immediate feedback to radiologists through computer displays, and enable electronic storage that is both convenient and economically attractive. The active matrix has lot of light sensing pixel circuits; each pixel circuits include a photodiode and one or several TFTs. The photodiode may produces leakage current when receiving light exposure, and the leakage current increases as exposing intensity increases. Fig.1.1 shows active matrix detector array with peripheral electronics [1].

Fig.1.2 shows the x-ray sensing system diagram which can be divided into three parts [2]. The first place is x-ray sensing component. Traditionally, component can be classified into direct and indirect; both of them depend on photosensitive material primarily. In general, indirect methods absorb x-rays and convert into a visible light by the photosensitive material. Then, through amorphous silicon photodiode, the visible light is further converted into electrical signal. Direct methods use sensing component which can put the x-ray into electron-hole pairs directly, afterward accumulated charge on the capacitor to produce a voltage difference as a sensing signal.

The second part is the signal readout circuit. The most widely used architecture in flat panel imagers is the passive pixel sensor (PPS) which connects the photodiode to one readout TFT, as shown in Fig.1.3 (a) [3-4]. The PPS has the advantages of being compact and amenable to high-resolution imaging because of its simplicity. However, reading the small output signal of the PPS in the large area applications requires high performance charge amplifiers. These charge amplifiers introduce noise that degrades the signal-to-noise ratio (SNR), especially at low signal levels. Therefore, active pixel sensor (APS) is proposed in recent years, as shown in Fig.1.3 (b). APS has several advantages such as high immunity to external noise, high SNR, fast operating speed and possibility of compensating function, so it is a good candidate for flat panel imagers [5-7]. The electrical signal caused by different intensity of X-ray irradiation is sent via the readout circuit to the back-end system for interpretation. In APS, the first two sections are built into a basic pixel circuit.

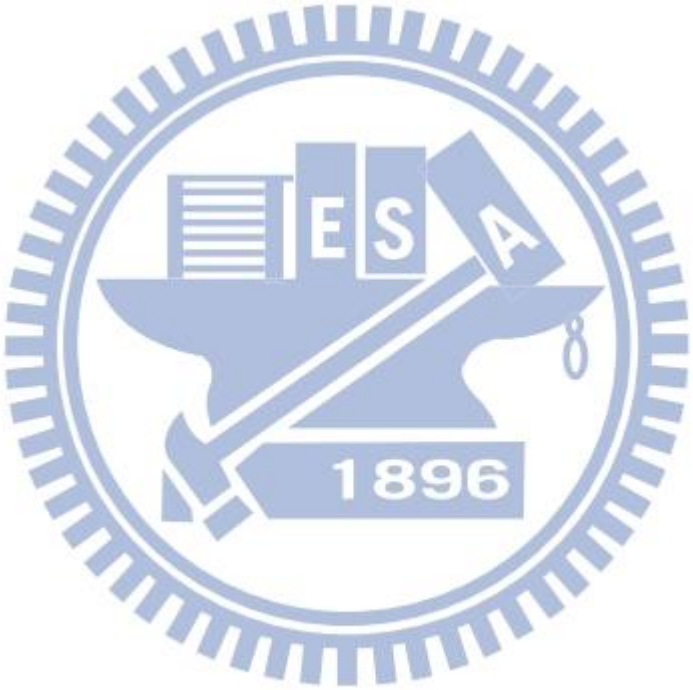
The last part is the back-end interpretation systems of the link with the pixel matrix circuit. In the entire system, since the performance of the sensing component is pretty much decided by what materials are used, the reading circuit has become the key design issue to the whole system.

1.2 Motivation

Previously, our group proposed the voltage- and current- programmed of two-TFT (2T) APS [8], as shown in Fig. 1-4 and 1-5, respectively. They can provide the function of the threshold voltage compensation in a simple configuration. [9-10] Nevertheless, the circuit has problem when the device mobility changes, an error is induced in the output signal. Therefore, we want develop a solution to compensate more kind of variations in devices. When it comes to the implementation of the APS circuit with TFTs, we wonder which kind of TFT technology is the most suitable to be adapted in the view point of SNR. Therefore, we study the noise behaviors for the most popular TFT technologies, namely, amorphous silicon, low-temperature polycrystalline silicon, and amorphous indium-gallium-zinc oxide TFTs.

1.3 Thesis Organization

After the introduction of chapter 1, this thesis investigates the three different kinds of material TFTs devices noise measurement and the analysis of 2T APS circuits. The device noise measurements and analysis are discussed in chapter 2. Then, we would tell how we utilize the calibration method to implement the current compensation circuit in chapter 3. Finally, conclusions of this research are given in chapter 4. The section organization of the thesis is listed below:



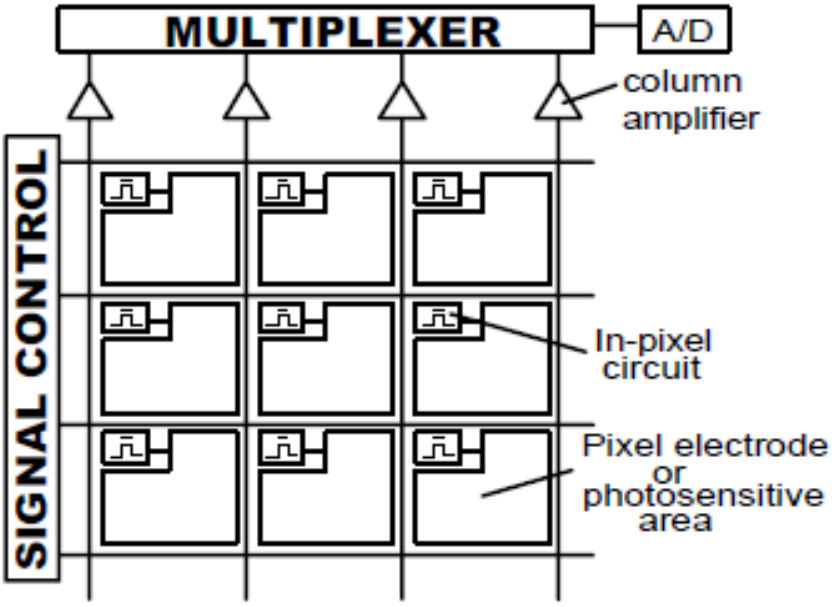


Fig 1.1 Active matrix detector array with peripheral electronics

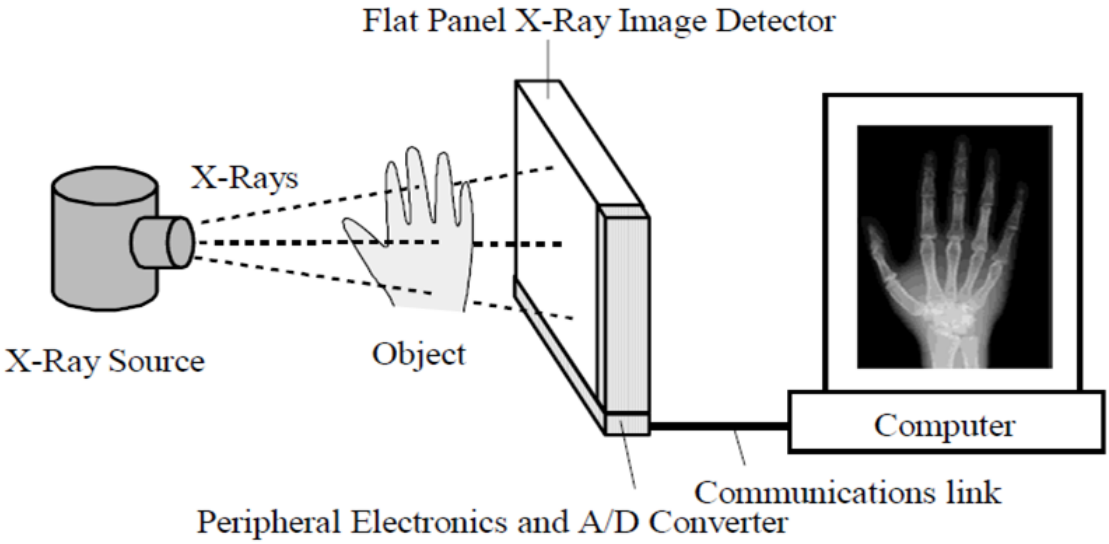


Fig.1.2 The x-ray sensing system diagram

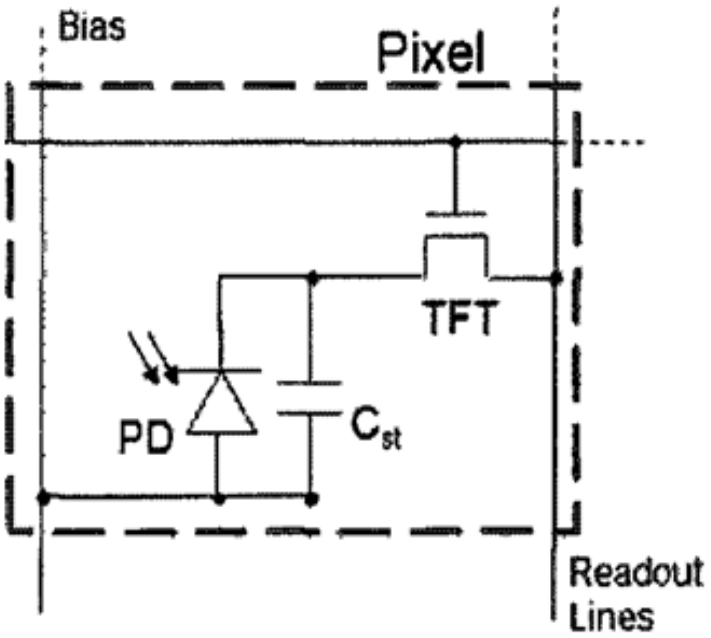


Fig. 1-3 (a) Passive pixel sensor (PPS)

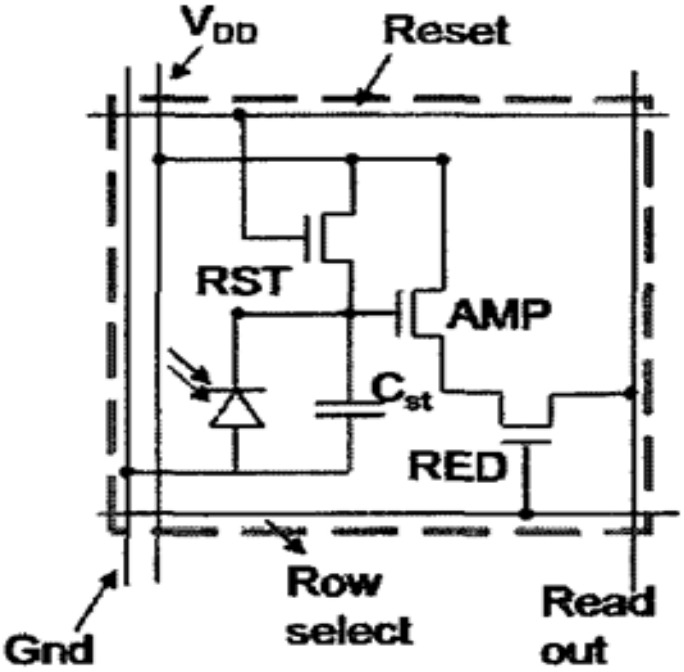


Fig. 1-3 (b) Active pixel sensor (APS)

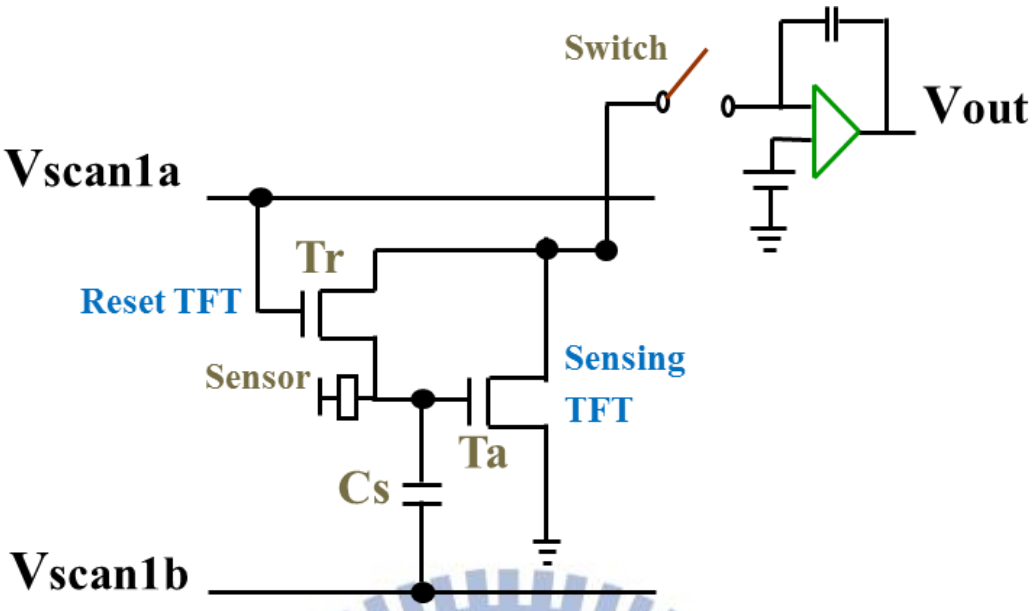


Fig. 1-4　2T1C APS circuit with voltage compensation

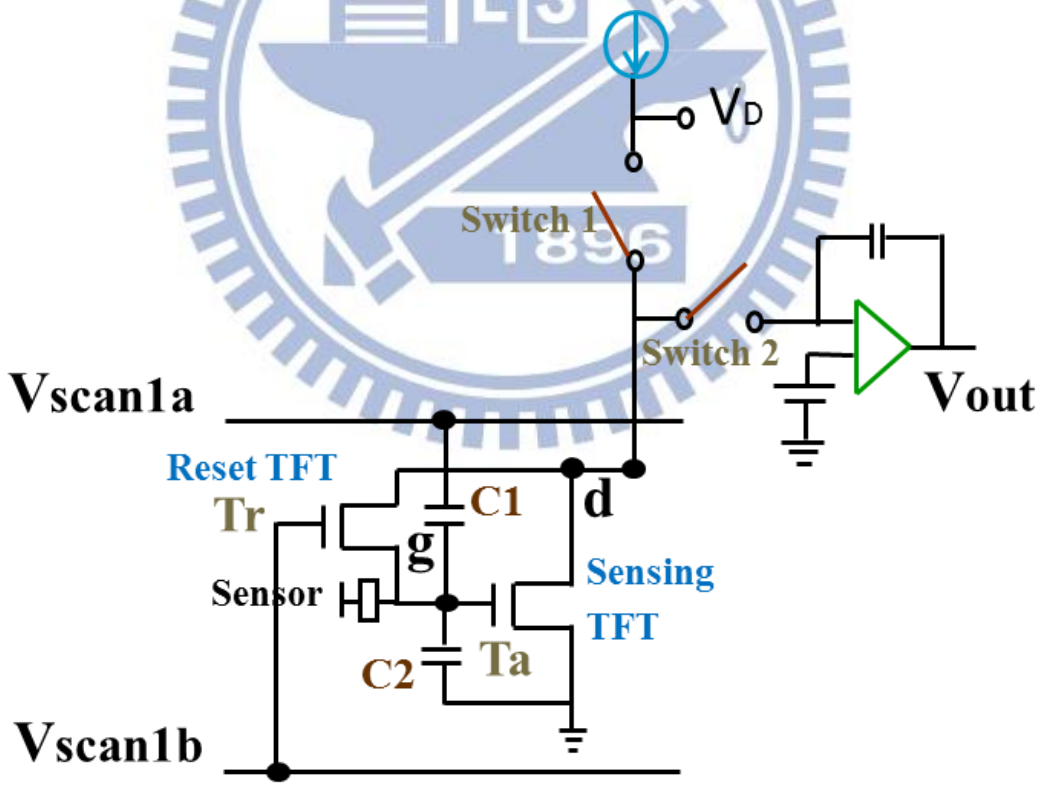


Fig. 1-5　2T2C APS circuit with current compensation

Chapter 2

Device Noise Measurement and Analysis

In this chapter, we compare the noise behavior for the TFTs of various materials. At the first, we would introduce the experimental instruments and assumption for the noise measurement, as well as the measurement procedures. Then, we will do the noise analysis and propose a new noise expression by formula derivation. Finally, the Signal-to-Noise Ratio (SNR), i.e. the ratio of signal power to noise power is calculated, so that it can be used as a figure of merit to compare the performance of TFTs in the different operating conditions. The SNR is also used to compare the devices of different materials.

2.1 Experimental Setup and Operation

2.1.1 Experimental Machine Introduction

In this section, we introduce the experimental setup shown in Fig. 2-1 and 2-2, and explain how we measure the device noise.

At the first, we put the packaged device on the breadboard with the power supplied from the lithium batteries, which can provide the designated voltage in a module. The advantage of the battery is that it can supply clean power with less noise.

The second, we connect the breadboard to the current preamplifier which

converts the low-level current into a measurable voltage signal. The power of the amplifier is also provided by a clean DC battery for low noise. The instrument has several options of gain, which has their own background noise levels, as show in Table 2-1. As a result, we choose the proper gain setting for the measurement of our devices.

The next step is that we put the packaged device and the battery module on breadboard, as well as the current preamplifier into a shielding box to shield out the devices under test (DUT) from the outside interference in atmosphere.

At the last, we link the shielding box and signal source analyzer (SSA) with transmission lines. The SSA we use is made by Agilent in the model number of E5052B, which can convert the voltage signal into spectrum. Fig 2-2 shows the block diagram and the connection of the noise measurement setup.

The measurement result is in the form of the baseband (non-modulated) spectrum (V/√Hz) versus frequency (Hertz). The measured baseband voltage noise spectrum in V/√Hz can be converted back to the current noise spectrum in A/√Hz with the chosen gain of the current preamplifier.

In the previous papers [11], the measurement results are usually represented in the curves of power spectrum *S* versus frequency *f*, where *S* is the square of current noise spectrum in the unit of A^2/Hz and it exhibits $\frac{1}{f}$ dependence. Therefore, in this thesis, we also plot our measurement result in the same way.

2.1.2 Background Noise

The noise measurement can be affected by some factors. We take the following factors into consideration to minimize the background noise of the experiments.

Firstly, all of the elements are bonded and accessed on the breadboard rather than using the point-to-point probes. The packaged component can avoid unsecured contacts and long cables between DUT and instrument. However, a certain extent leakage current of the level from 10pA to 100pA is introduced.

Secondly, even though the shielding box is not in vacuum extraction, the moisture, temperature, atmospheric pressure and other ambient factors are put aside because of their minor effects in general.

The last one is about the transmission line, which transmits the signal along with possible noise and distortion. As a result, we choose the hollow transmission line made of special material instead of the traditional copper wire to reduce the background noise.

Figure 2-3(a) show the background noise measurement results of the preamplifier, which is consistent with Table 2-1. The overall background noise with the peripherals including SSA, shielding box and breadboard are shown in Fig. 2-3(b). Only the noise level above the overall background noise will be taken as the real noise of the DUT.

2.1.3 DUTs and Measurement Conditions

For comparison, the DUTs in this thesis are TFTs made of a-Si, LTPS and IGZO as well as the devices with different widths and lengths, as summarized in Table 2-2. Before the noise measurement, we utilize Keithley 4200 to measure I_D-V_G curves of TFTs at several drain voltages.

These DUTs are then subject to the noise measurement with gate and drain voltages in DC. Many DC values of the gate voltage in the range from -5V to 15V and

those of the drain voltage are fixed at 5V and 10V. Each of the DC tests corresponds to the noise baseband spectrum and is displayed and stored in the SSA instrument.

In our noise analysis, the frequency band of noise measurement is from 10Hz to 1 KHz, since the general operation frequency of an APS panel is 60Hz.

2.2 Noise Measurement Results and Discussion

2.2.1 Noise Database

The database is built by measuring the DUTs under different bias voltages. The noise results of the DUTs measured at the drain voltage equal to 10V are shown in Fig. 2-4(a) to (i). From those figures, it is observed that all the power noise spectrums follow the $\frac{1}{f}$ dependence, which is consistent with the previous reports. In addition, we can find that, for those gate voltages in the off region, all DUTs have noise lower than the background in the spectrum. Even not shown in this thesis, the data for the drain voltage of 5V also show the same behaviors of low off region noise.

As for the higher gate voltages, the curves overlap substantially and make it difficult to do further analysis. In order to make the noise analysis simple, we need to develop a parameter to describe the noise level rather than comparing the entire curves.

2.2.2 Calculation of Noise in Ampere (NiA)

Firstly, we follow the conventional way of noise analysis. Since the baseband power spectrum S is in the form of $\frac{\gamma}{f}$ for every curve in the unit of A^2/Hz [12], it can be expressed in equation:

$$S = \frac{\gamma}{f} \tag{2-1}$$

where f is the frequency and γ is the indication for the noise level in the unit of A^2. Equation (2-1) can be rewritten as

$$\log(S) = \log(\gamma) - \log(f) \tag{2-2}$$

By drawing the curves of S versus f with both X and Y-axes in logarithm scale, Y-intercept gives log (γ).

Another method of extracting γ is to integrate the noise power spectrum S in a certain range of frequency f:

$$\int_{f_{Low}}^{f_{High}} Sdf = \int_{f_{Low}}^{f_{High}} \frac{\gamma}{f} df = \gamma\left[\ln(f_{High}) - \ln(f_{Low})\right], \tag{2-3}$$

and the result is proportional to γ. In this thesis, we use the second method to get the square of noise. In the measurement results, we often observed that the noise does not always follow the ideal (1/f) dependence. If it is the case, the Y-intercept extracted by the method of interception gets fussy, because the slope of the log (S)-log (f) curve is uncertain.

In this thesis, we define a new index NiA to represent the noise in ampere by integrating the noise power spectrum from 10Hz to 1 KHz and then taking the square root, as the following definition:

$$NiA^2 = \int_{10Hz}^{1KHz} Sdf \quad \text{Or} \quad NiA = \sqrt{\int_{10Hz}^{1KHz} Sdf} \tag{2-4}$$

2.2.3 Noise Discussion

Using the index NiA, we study the noise quality of the devices and the different material in various sizes. Fig. 2-5(a) and (b) show NiA versus gate voltage for the a-Si TFT with different sizes at V_D=5V and 10V, respectively. As can be seen, NiA increases with the gate voltage above some threshold as well as the drain voltage. In the further observation, we find that the larger W/L ratio leads to the higher NiA. The similar observations are also found for the TFTs made of the other two materials, as shown in Fig. 2-6 and 2-7. All the observations of NiA are very much like those of drain current, which also increases with drain voltage and size, not to mention the threshold of the gate voltage. Therefore, we try to correlate the NiA and drain current in the following section.

2.3 Noise Analysis

2.3.1 Noise versus Drain Current

Plotting the NiA-V_G and I_D-V_G curves of the same TFT together, as shown in Fig. 2-8(a), the resembling threshold voltage of NiA and I_D is clearly seen. We further change the Y-axis to logarithmic scale, putting aside the background noise and leakage current, the two curves overlap very well with appropriate adjustments on the offset and scale, as shown in Fig. 2-8(b). The adjustment can be described by the simple formula below

$$(\log NiA) * \alpha + \log A = \log I_D \qquad (2\text{-}5)$$

In the equation, α and log A correspond to the scale and offset, respectively. Take the power of 10 on both sides of equation (2-5) leads to equation (2-6).

$$I_D = A * NiA^{\alpha} \text{ or } \quad NiA = \left(\frac{1}{A} I_D \right)^{1/\alpha} \tag{2-6}$$

We call this equation (2-6) is the "noise formula", since it can simply express the relationship between the noise and drain current. Based on the noise formula, we extract the values of A and α by linear fitting the curves of NiA versus I_D for the nine devices of DUTs, which are shown in Fig. 2-9. The fitted parameters of these DUTs are listed in table 2-3. The graphs overlapping the NiA-V_G and I_D-V_G curves together for all the DUTs are shown in Fig. 2-10 (a) to (i). It proves that the noise formula is universal for various TFTs in the aspects of material, size, as well as the gate and drain voltages.

2.3.2 Discussion of the Noise Formula

Even the newly proposed noise formula describes the relation between NiA and I_D very well, no matter what size or material the TFT is, we wonder if there is a theoretical ground for it. In this section, we compare the conventional noise expression with our noise formula.

From the reference [13], we can see the conventional noise spectrum can be written as

$$S = \frac{\alpha_H q}{f * WLC_{OX} |V_G - V_T|} I_D^2 \tag{2-7}$$

Where α_H is Hooge's parameter, *C*ox is the gate dielectric capacitance per unit area, q is the elementary electron charge and V_T is the threshold voltage.

We put this *S* in equation (2-7) into the equation (2-4)

$$
\begin{aligned}
NiA^2 &= \int_{10Hz}^{1KHz} Sdf \\
&= \int_{10Hz}^{1KHz} \frac{\alpha_H q * I_D^2}{fWLC_{OX}\left|V_G - V_T\right|} df \\
&= \frac{\alpha_H q \ln(100)}{WLC_{OX}\left|V_G - V_T\right|} I_D^2 \qquad (2\text{-}8) \\
&= \left(\frac{\alpha_H q \ln(100)}{WLC_{OX}}\right)\left(\frac{{I_D}^2}{\left|V_G - V_T\right|}\right)
\end{aligned}
$$

Taking a close look at the equation (2-8), the items in the first bracket are constants. Thus, as long as the $\left|V_G - V_T\right|$ in the second bracket is in the relation of power-law to $I_{D,}$ it can be expressed by I_D and leave I_D the only variable on the right hand side of the equation (2-8). In this case, NiA can be in the form of our noise formula (2-6).

Now the question is coming to whether I_D versus $\left|V_G - V_T\right|$ is in the power law. As known well, the TFT of drain current formula is

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_G - V_T)^{\beta} \qquad (2\text{-}9)$$

Where μ is the field effect mobility and β is usually 2 in many literatures but subject to change with device. The power-law relation of the drain current can express as

$$V_G - V_T = \left(\frac{1}{2}\mu C_{OX}\frac{W}{L}\right)^{-1/\beta} I_D^{1/\beta} \qquad (2\text{-}10)$$

Substituting equation (2-10) into equation (2-8), we can obtain.

$$NiA^2 = \int_{10Hz}^{1KHz} Sdf$$

$$= \left(\frac{\alpha_H q \ln(100)}{WLC_{OX}} \right) \left(\frac{I_D{}^2}{\left(\frac{1}{2} \mu C_{OX} \frac{W}{L} \right)^{-1/\beta} I_D^{1/\beta}} \right) \tag{2-11}$$

$$= \left(\frac{\alpha_H q \ln(100)}{WLC_{OX}} \right) \left(\frac{1}{2} \mu C_{OX} \frac{W}{L} \right)^{1/\beta} \left(I_D^{\left(2-1/\beta\right)} \right)$$

The next step, we square the noise formula (2-4) to get

$$NiA^2 = \left(\frac{1}{A} I_D \right)^{2/\alpha} = \left(\frac{1}{A} \right)^{2/\alpha} I_D^{2/\alpha} \tag{2-12}$$

and compare the coefficients with equation (2-6). The exponential term gives

$$2 - 1/\beta = \frac{2}{\alpha} \text{ or } \alpha = \frac{2\beta}{2\beta - 1} \tag{2-13}$$

and the constant term gives

$$\left(\frac{1}{A} \right)^{2/\alpha} = \frac{\left(\frac{1}{2} \mu C_{OX} \frac{W}{L} \right)^{1/\beta} \alpha_H q \ln 100}{WLC_{OX}} \text{ or } A = \left(\frac{WLC_{OX}}{\left(\frac{1}{2} \mu C_{OX} \frac{W}{L} \right)^{1/\beta} \alpha_H q \ln 100} \right)^{\alpha/2} \tag{2-14}$$

The value of β plays an important role in the derivation above to get the A and α values of the equations (2-13) and (2-14), respectively. The extraction of the β parameter will be further discussed later in Chapter 3.

2.3.3 Comparison of TFTs in SNR

SNR is a popular measurement used in science and engineering that compares the level of a desired signal to the noise [14]. It is defined as the ratio of signal power

to the noise power:

$$SNR = \frac{{I_D}^2}{NiA^2} \tag{2-13}$$

Fig. 2-11(a) and (b) plots the SNR for all the DUTs with VD=10V versus V_G and I_D, respectively. From the graphs which seem complicated and hard to observe the tendency, as a result, we need another method to show the SNR diagram.

According to the noise formula (2-6), we can rewrite the SNR as equation (2-14)

$$\sqrt{SNR} = \frac{I_D}{NiA} = \frac{I_D}{\left(\frac{1}{A} I_D\right)^{1/\alpha}} = A^{1/\alpha} * I_D^{\left(1-1/\alpha\right)} \tag{2-14}$$

Then, we transform the SNR into SNR_{dB}

$$\begin{aligned} SNR_{dB} &= 10\log\left(SNR\right) \\ &= 20\log\left(\sqrt{SNR}\right) \\ &= 20\log\left(I_D / NiA\right) \\ &= 20\log\left(A^{1/\alpha} * I_D^{\left(1-1/\alpha\right)}\right) \\ &= \left(20/\alpha\right)\log\left(A\right) + 20\left(1-1/\alpha\right)\log\left(I_D\right) \end{aligned} \tag{2-15}$$

In equation (2-15), SNR_{dB} is derived to be a linear function of log (I_D). Therefore, we replot the curves of SNR in dB scale versus I_D in logarithm scale, as shown in Fig. 2-11 (c). It can be seen that all the curves are linear. This figure provides us a better way to describe and compare the noise performance of devices.

In the analog-to-digital converter (ADC) system, the SNR_{dB} of an ADC is equal to (6.02N+1.76) dB, where N equals the number of ADC bits. If we want that the DUTs can be as high as the 16-bit which is equal to 98.08dB, only the IGZO and a-Si TFTs can achieve in our study. The LTPS TFTs just has the capability of 15-bit or 92.06dB. Even though LTPS TFT has higher signal current, since it also has larger

noise, its SNR is the lowest among the three kinds of materials. It seems not a good candidate for the APS application.

Furthermore, with similar SNR, the IGZO TFTs can provide higher drain current than a-Si ones. As a result, the IGZO TFT is the best choice according to our SNR_{dB} analysis.

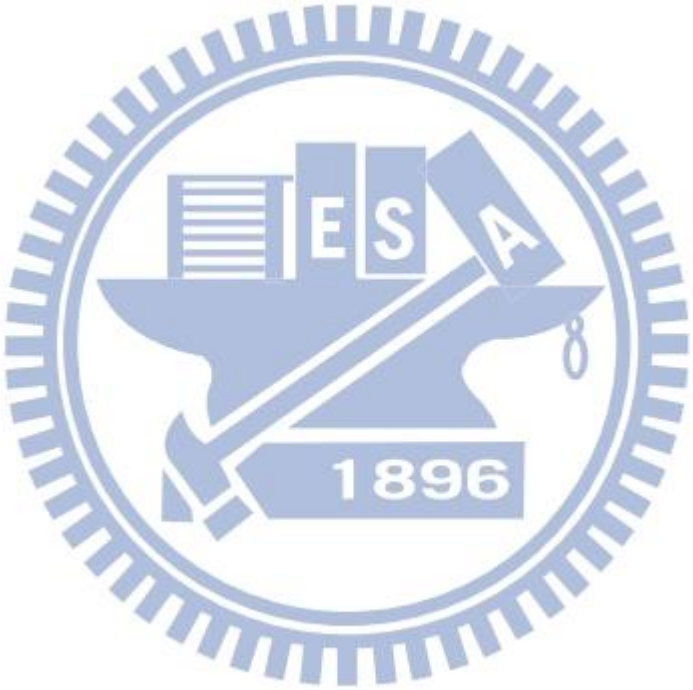


Table 2-1 Specifications of preamplifier (Model 5182) with different gains

Gain A/V	Max DC Input Current	Noise Current at 1 kHz
10^{-5}	9 mA	10 pA/root Hz
10^{-6}	900 µA	5 pA/root Hz
10^{-7}	9 µA	135 fA/root Hz
10^{-8}	900 nA	45 fA/root Hz
10^{-8}, low noise	90 nA	15 fA/root Hz

Table 2-2 Summary of DUTs in this thesis

Material	Width/Length		
a-Si	20µm/10µm	15µm/5µm	51µm/5µm
LTPS	20µm4µm	20µm/5µm	20µm/6µm
IGZO	20µm/5µm	20µm/10µm	20µm/15µm

Table 2-3 Extracted A and α parameters for the DUTs

Material	W/L	VD=5V			VD=10V		
		α	A	R (Square value)	α	A	R (Square value)
a-Si	20/10	3.248	1.61E+30	0.9925	3.028	1.77E+27	0.9993
	15/5	1.276	8.73E+07	0.9926	1.347	4.14E+08	0.9946
	51/5	1.006	1.78E+05	0.9936	1.147	3.45E+06	0.9959
LTPS	20/4	1.801	2.24E+11	0.9882	1.511	1.16E+09	0.9884
	20/5	1.645	7.59E+09	0.9876	1.392	3.26E+07	0.9947
	20/6	1.177	1.73E+06	0.9928	1.219	3.80E+06	0.9992
IGZO	20/5	1.631	2.61E+11	0.9825	1.476	7.89E+09	0.9866
	20/10	1.197	2.79E+07	0.9727	1.273	1.39E+08	0.9968
	20/15	2.383	6.07E+19	0.9569	1.837	6.62E+13	0.9836

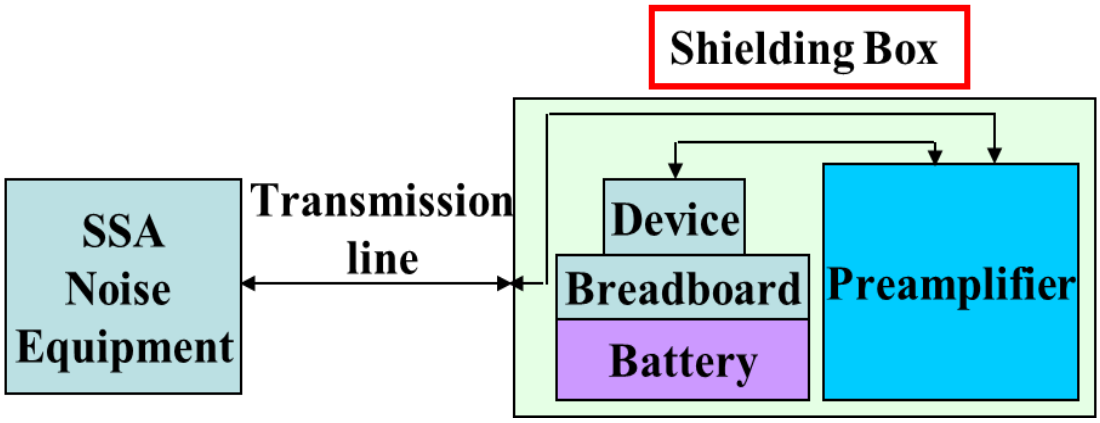


Fig. 2-1 The illustration of the instrument setup for the noise measurement

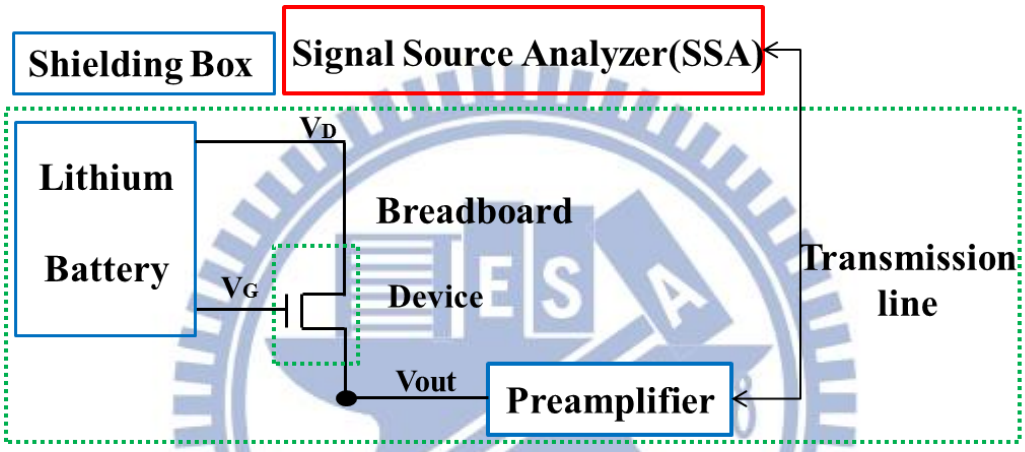


Fig. 2-2 The block diagram showing the connection of the noise measurement setup

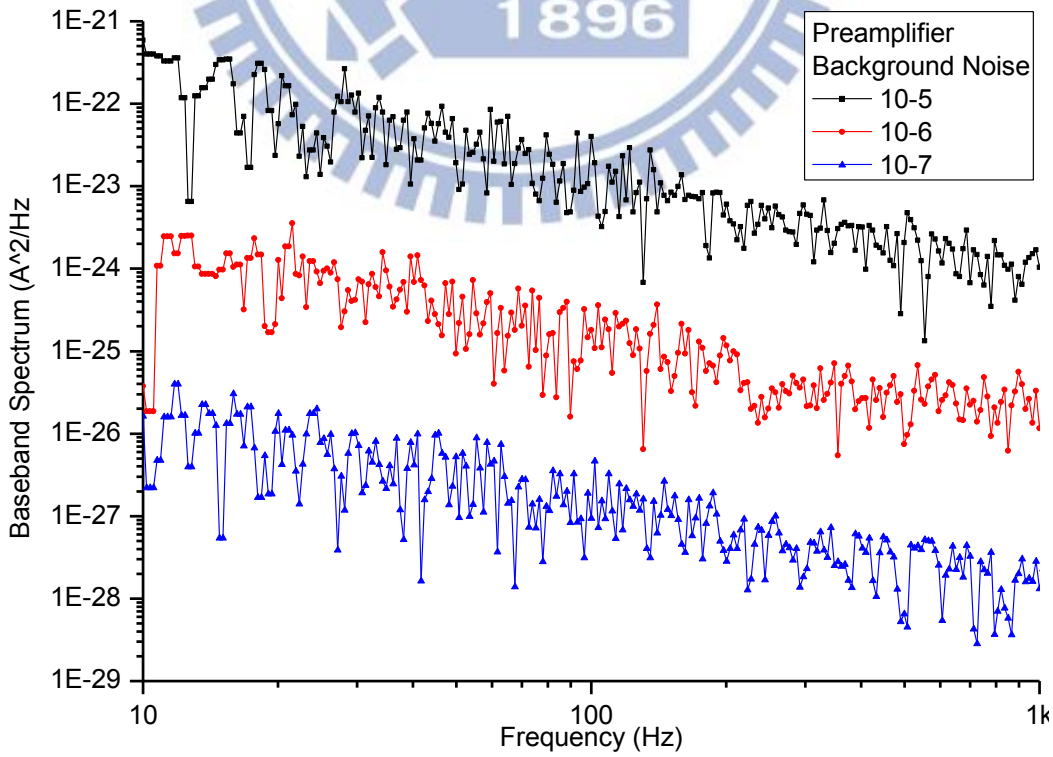


Fig. 2-3(a) Background noise measurement results of the preamplifier

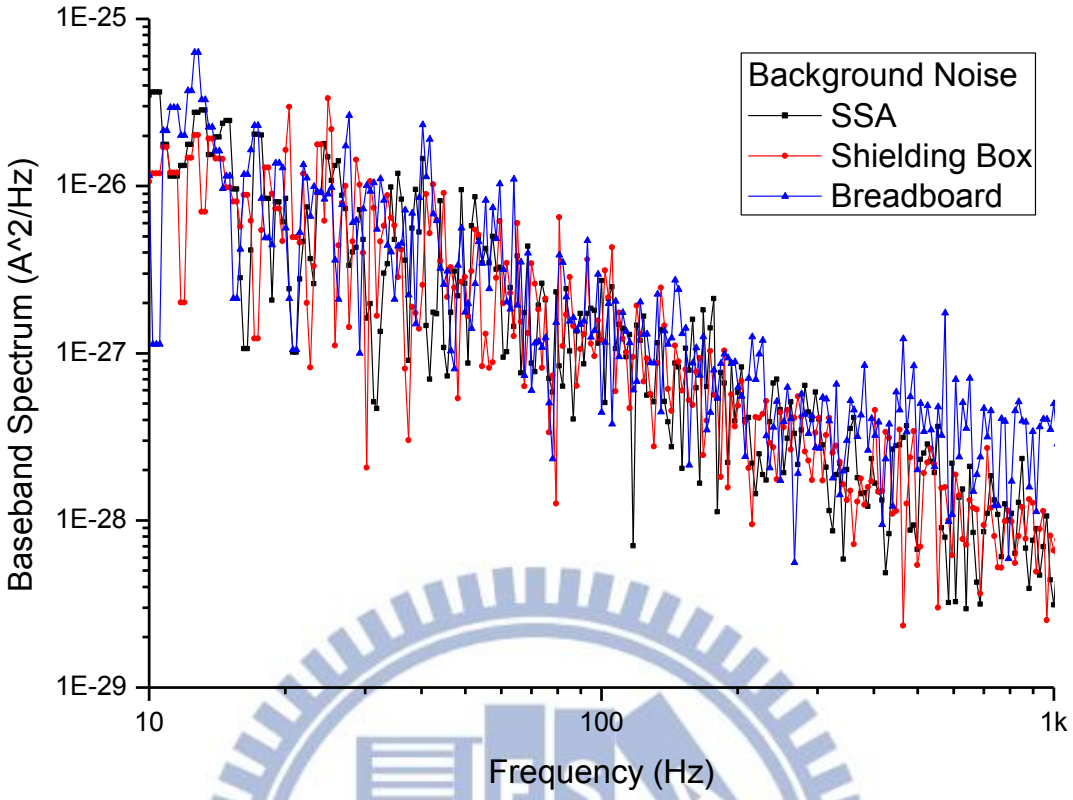


Fig. 2-3 (b) Background noise measurement results of the peripheral instrument

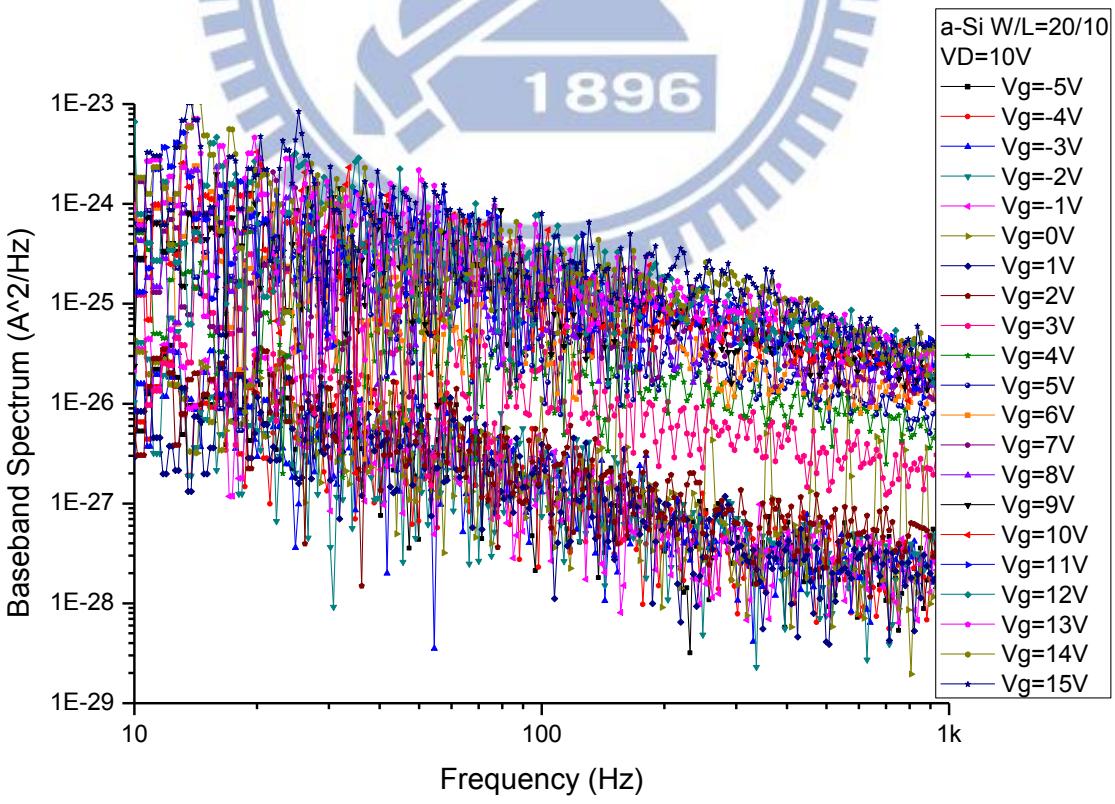


Fig. 2-4 (b) Noise measurement results of a-Si W/L=20/10

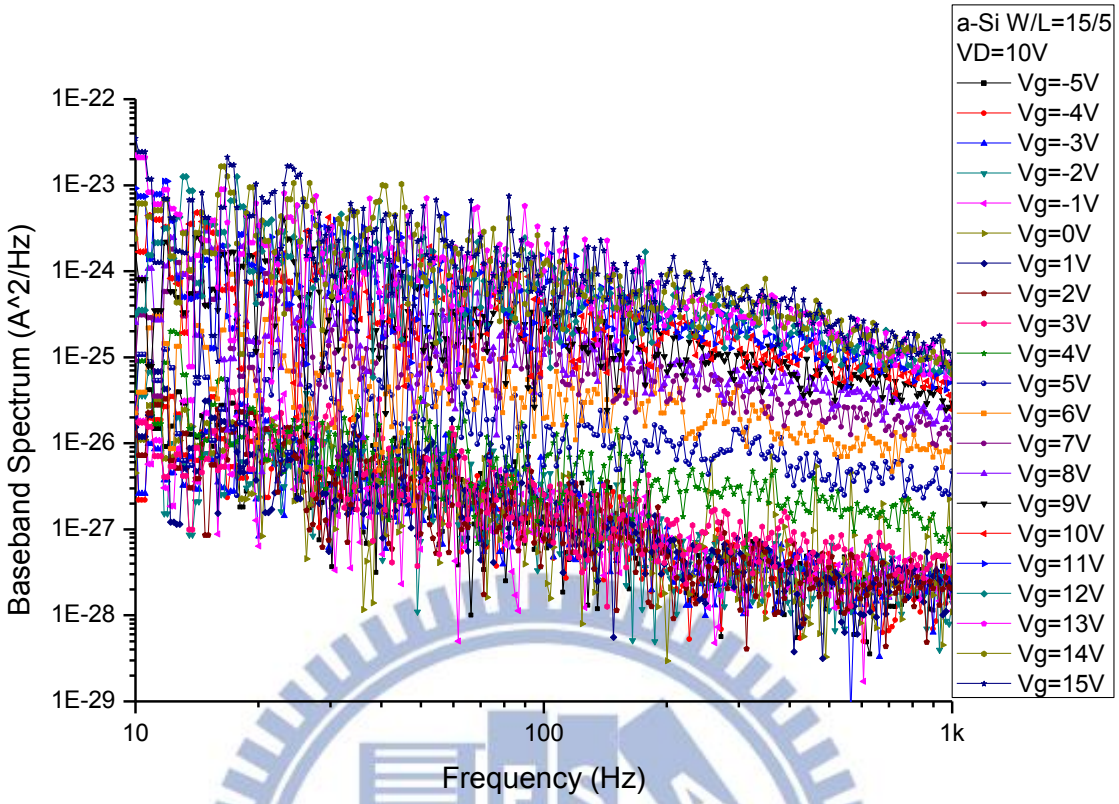


Fig. 2-4 (a) Noise measurement results of a-Si W/L=15/5

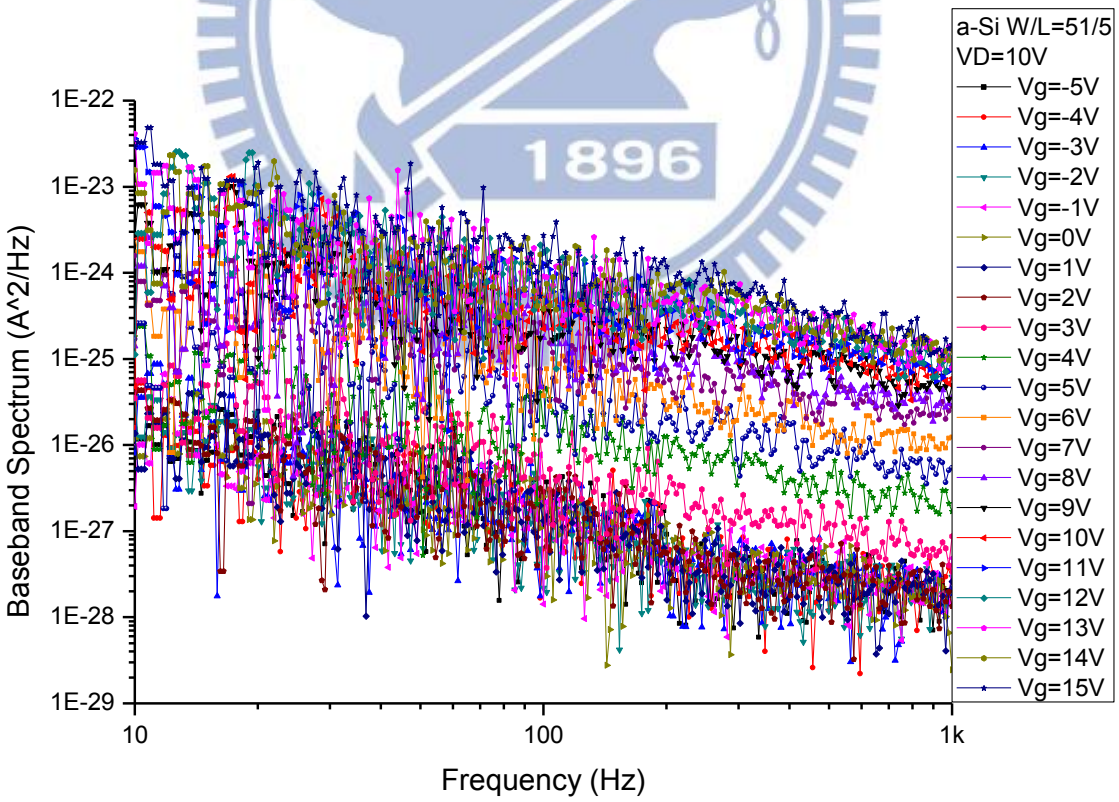


Fig. 2-4 (c) Noise measurement results of a-Si W/L=51/5

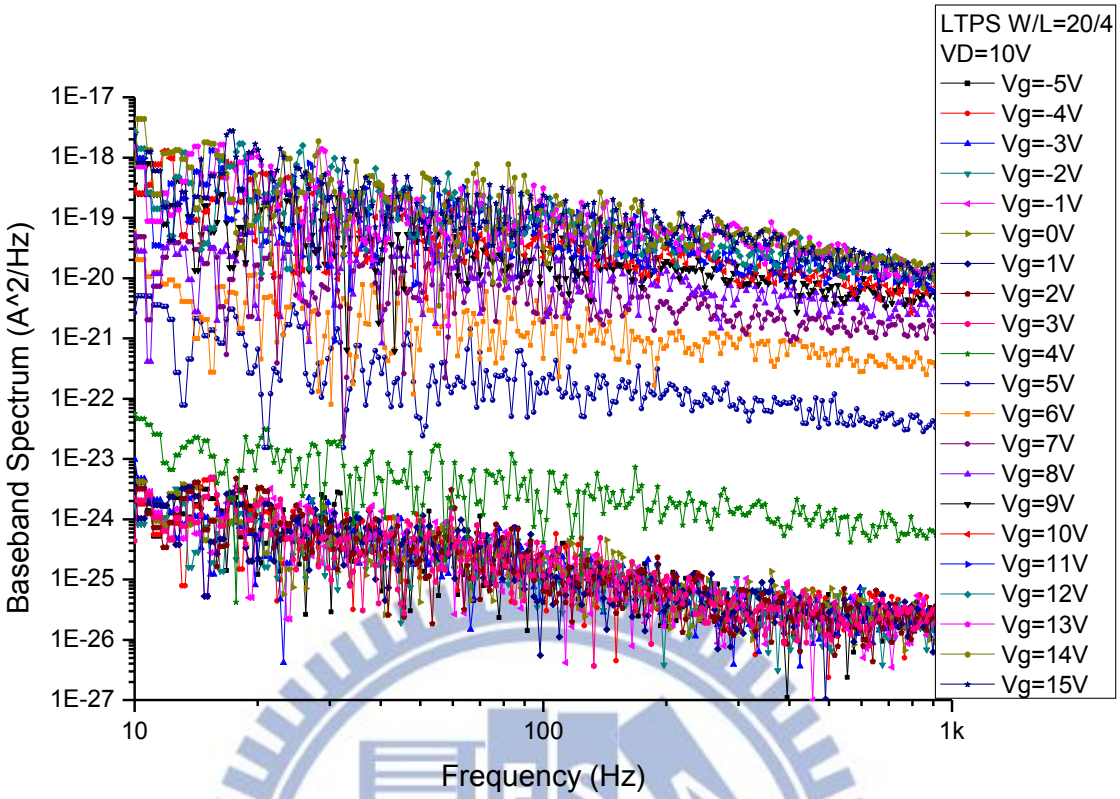


Fig. 2-4 (d) Noise measurement results of LTPS W/L=20/4

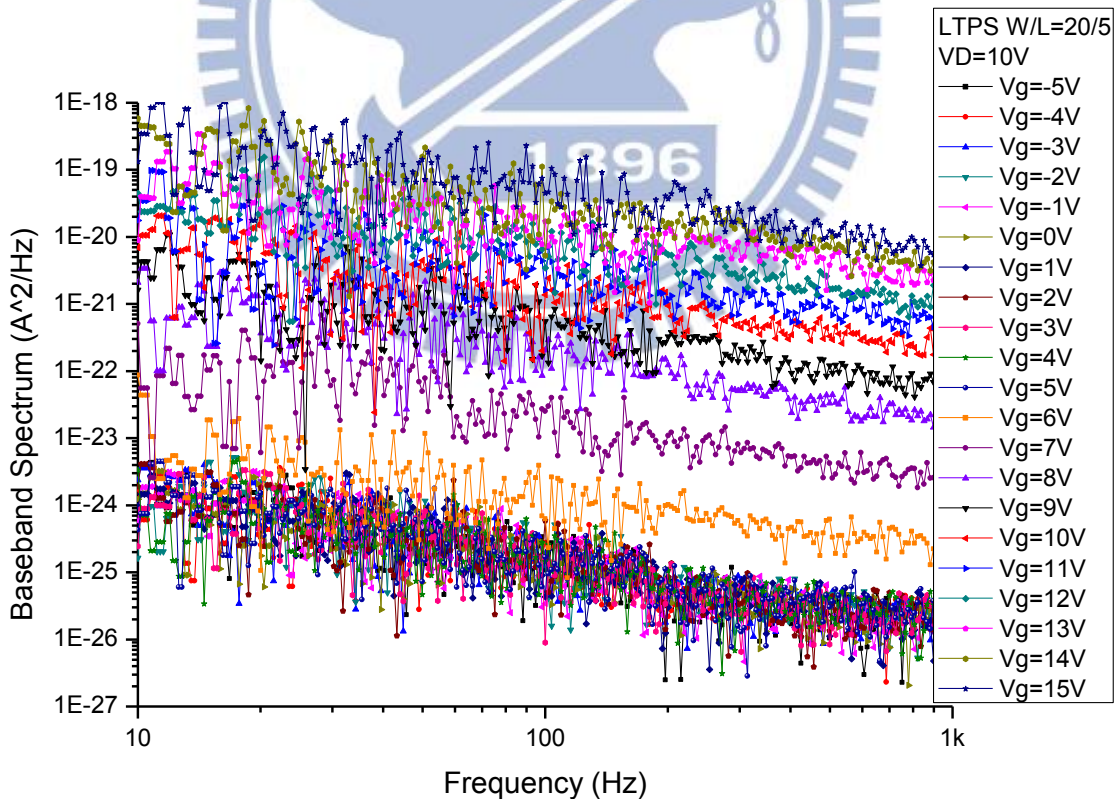


Fig. 2-4 (e) Noise measurement results of LTPS W/L=20/5

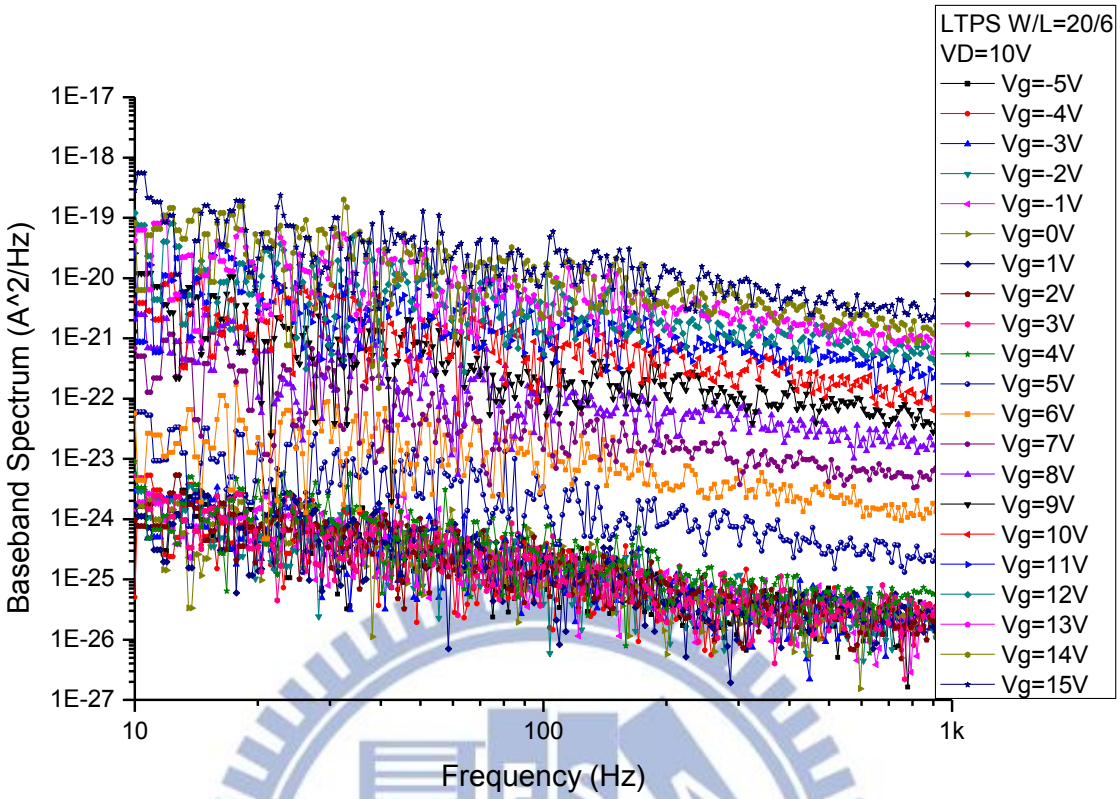


Fig. 2-4 (f) Noise measurement results of LTPS W/L=20/6

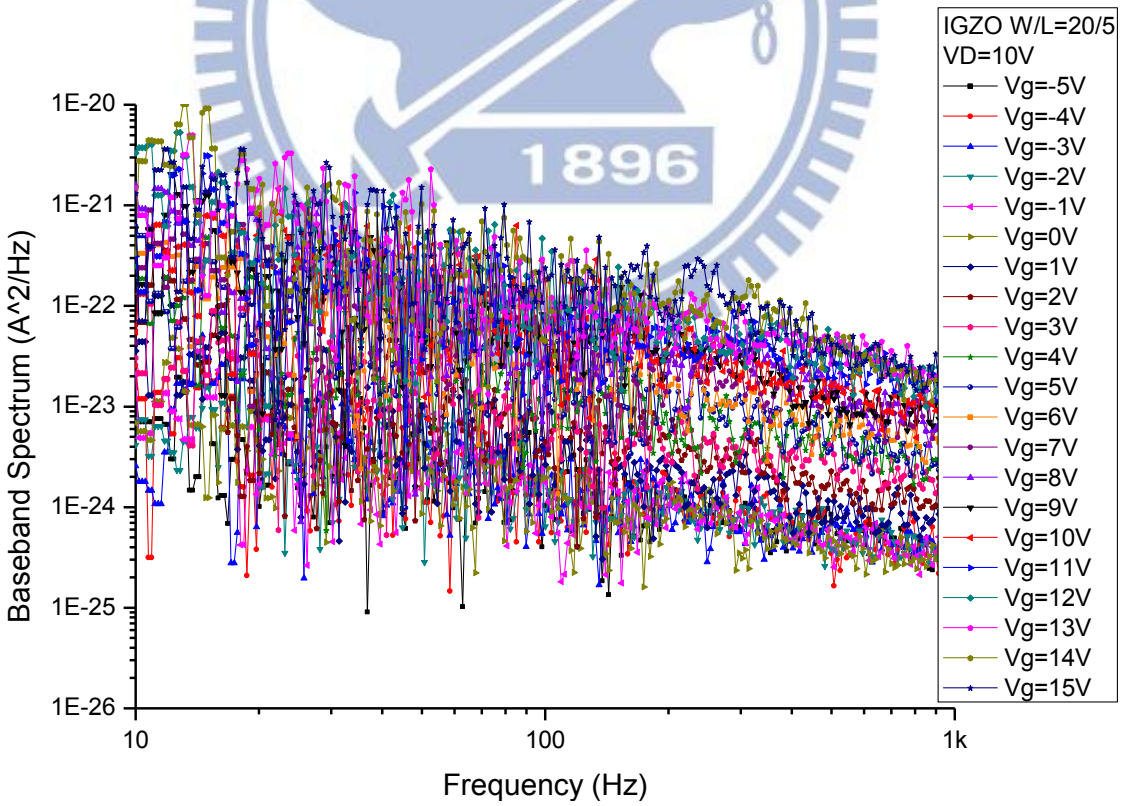


Fig. 2-4 (g) Noise measurement results of IGZO W/L=20/5

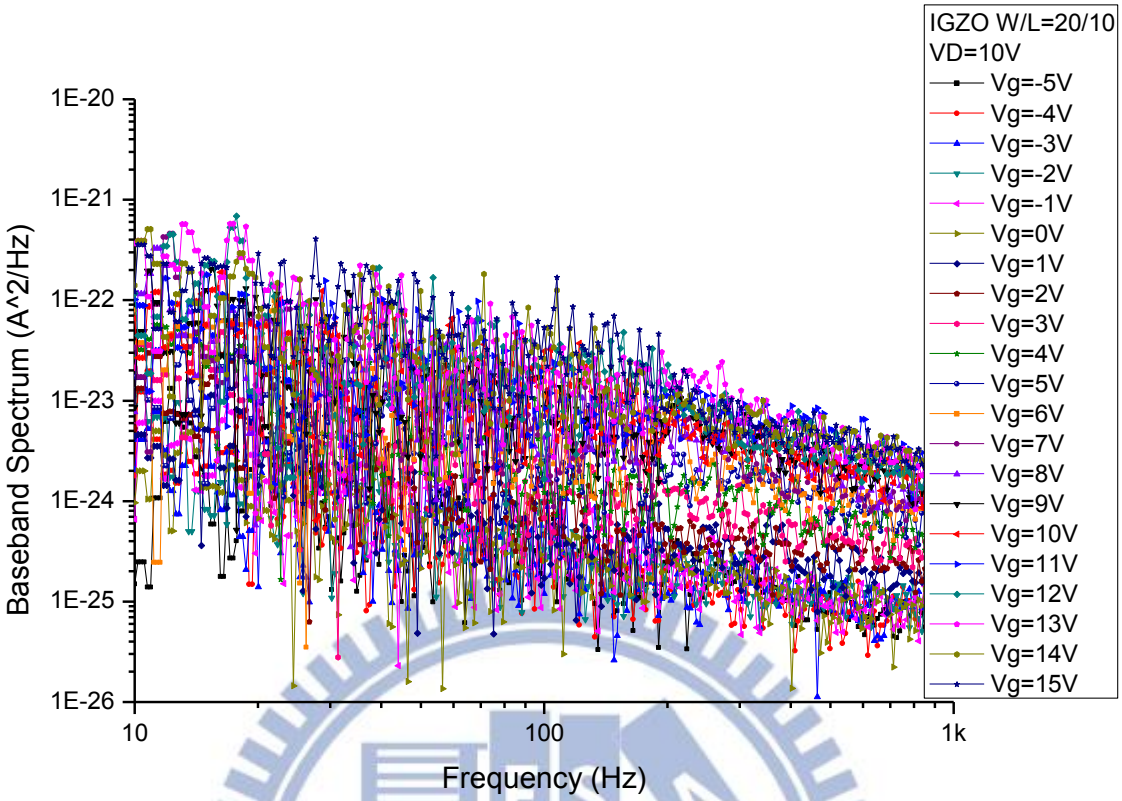


Fig. 2-4 (h) Noise measurement results of IGZO W/L=20/10

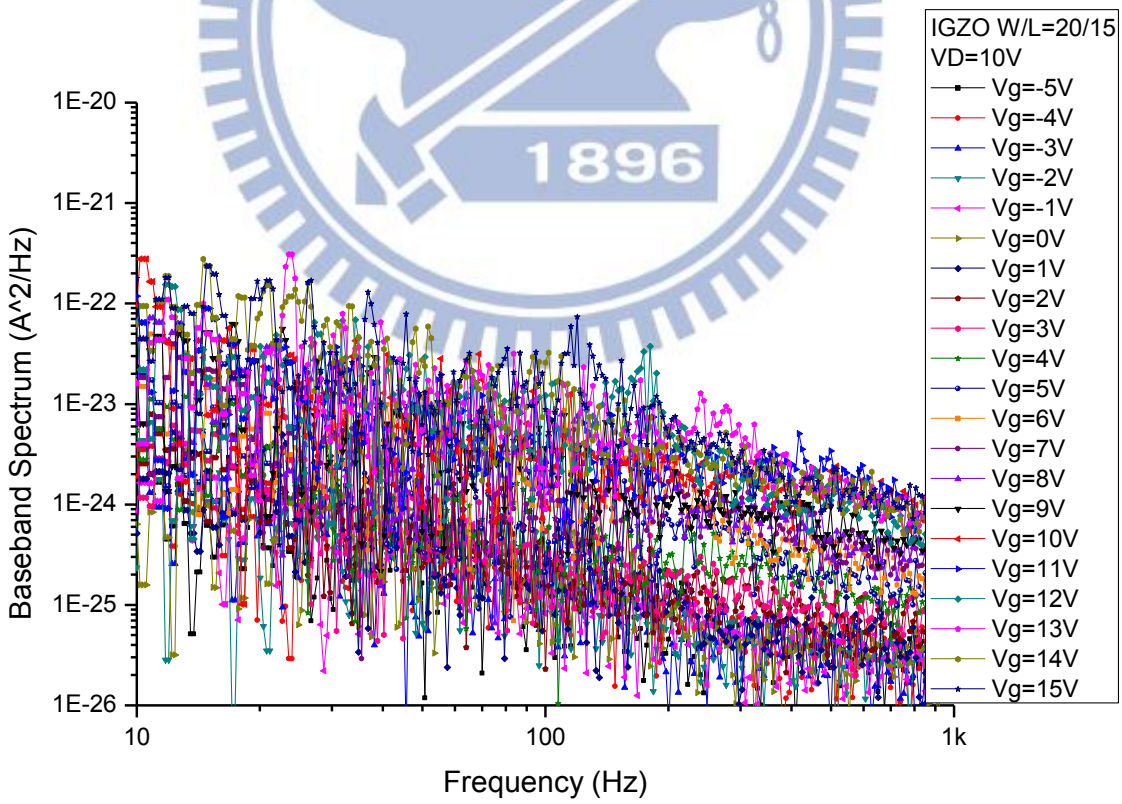
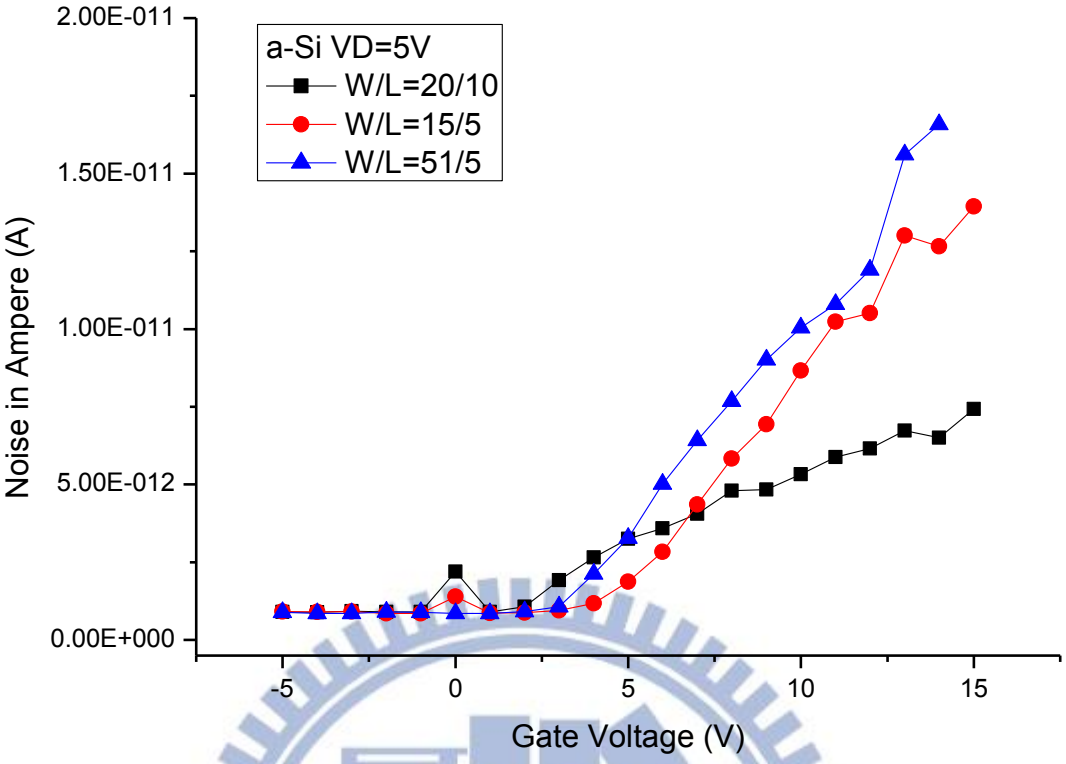
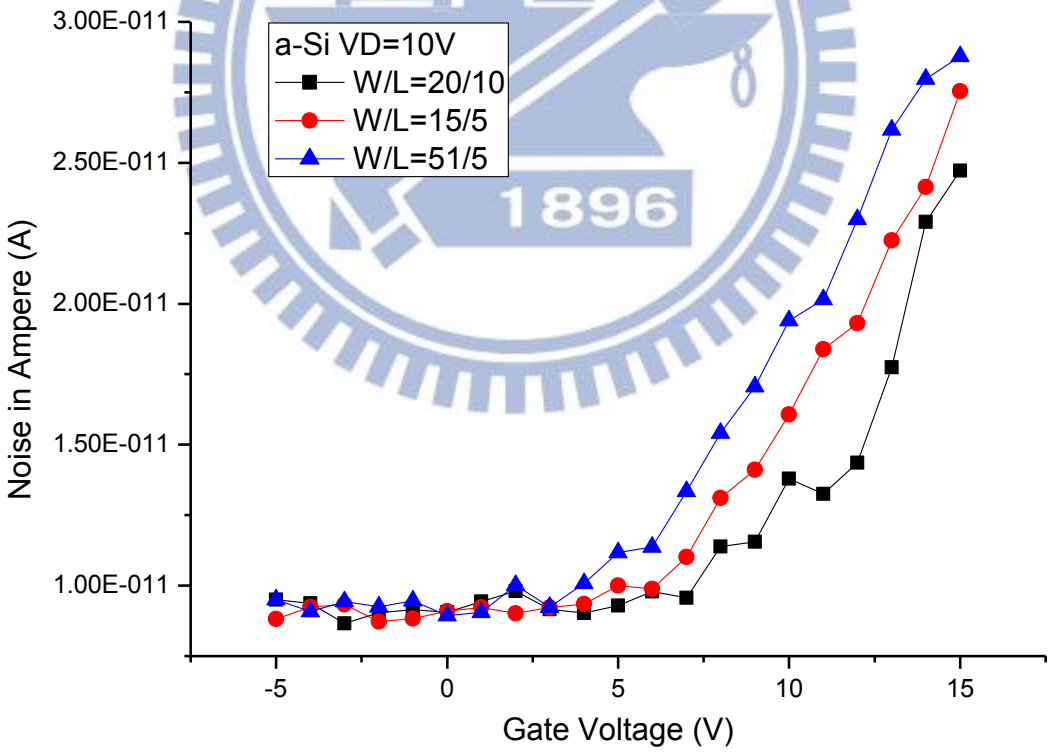


Fig. 2-4 (i) Noise measurement results of IGZO W/L=20/15

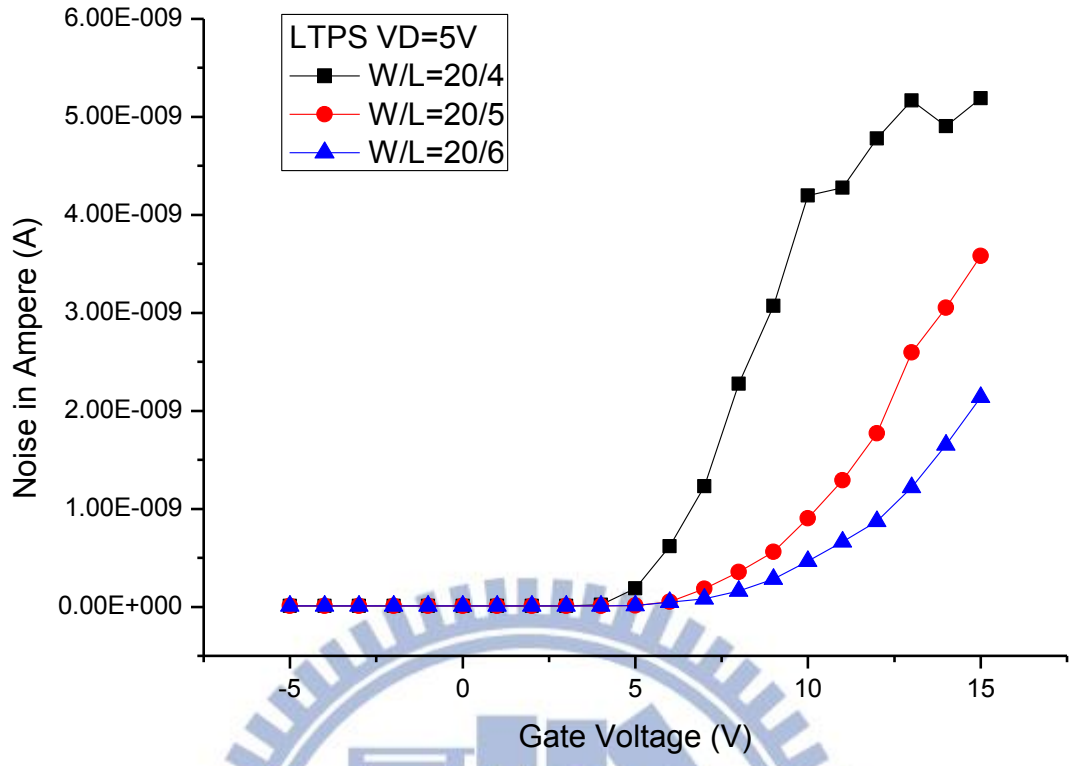


(a)

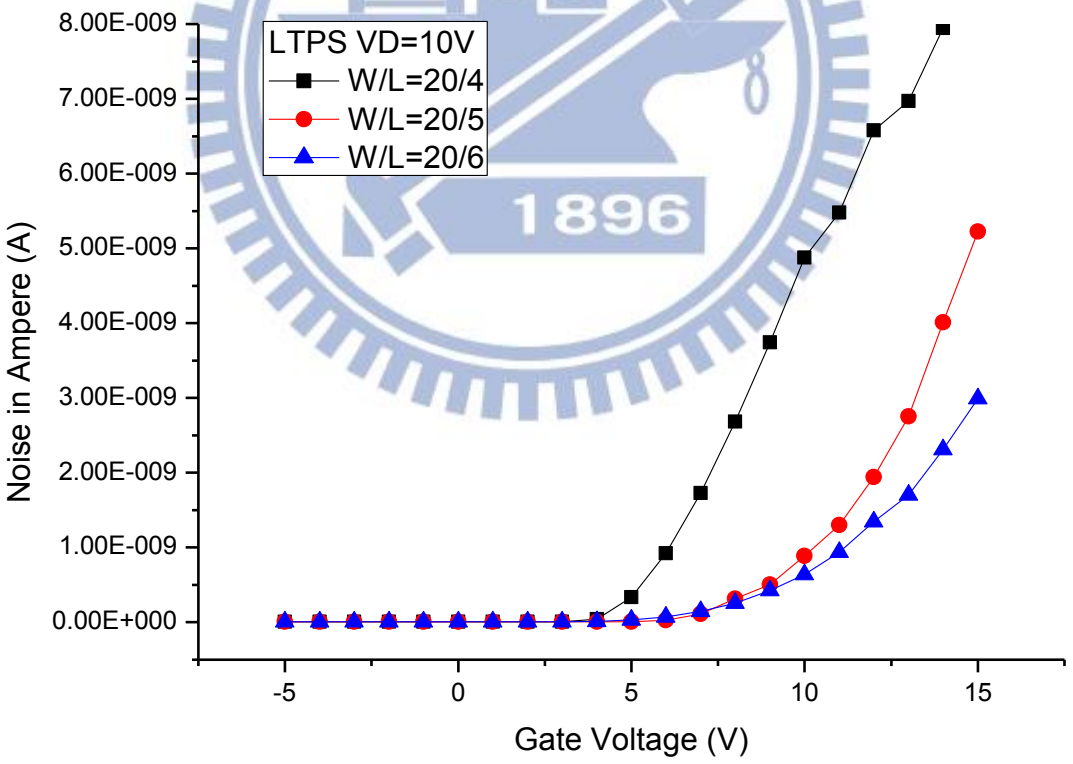


(b)

Fig. 2-5 NiA versus gate voltage for the a-Si TFTs with different sizes at drain voltage of (a) 5V and (b) 10V

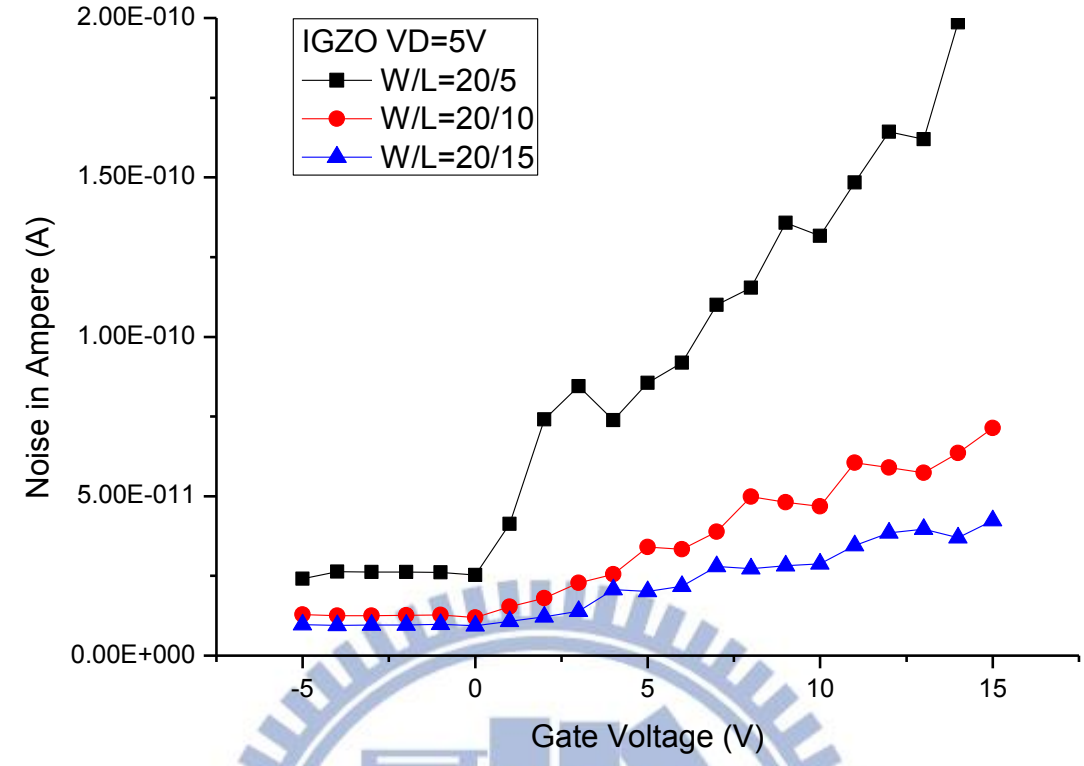


(a)

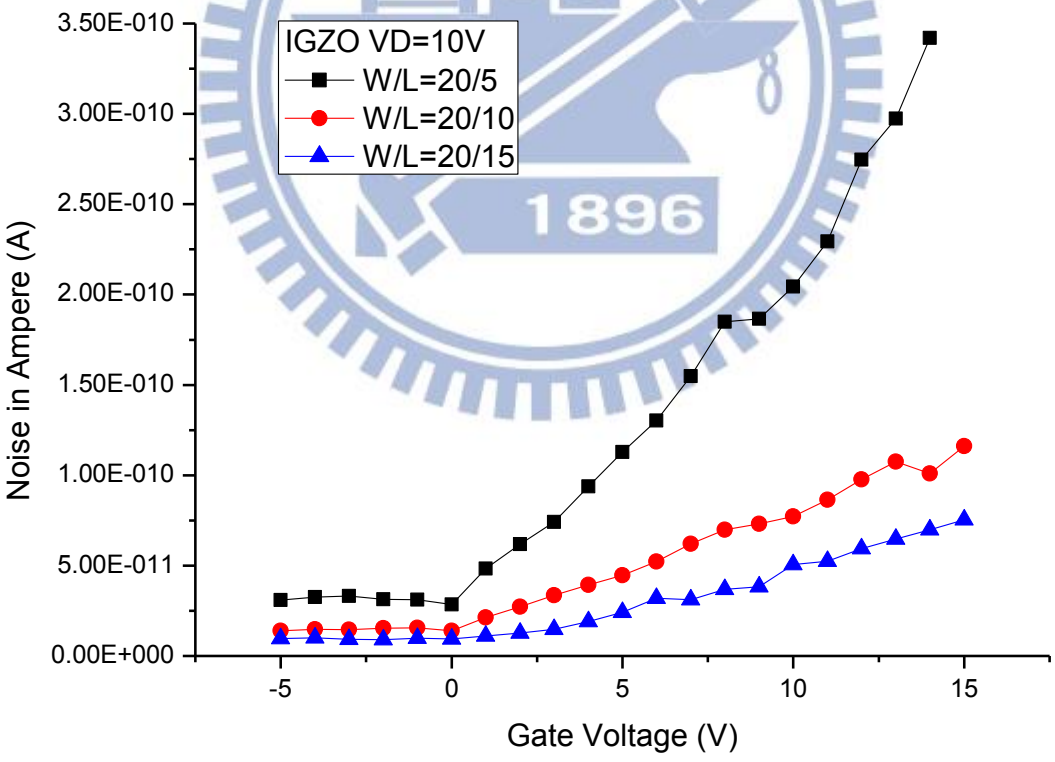


(b)

Fig. 2-6 NiA versus gate voltage for the LTPS TFTs with different sizes at drain voltage of (a) 5V and (b) 10V



(a)



(b)

Fig. 2-7 NiA versus gate voltage for the IGZO TFTs with different sizes at drain voltage of (a) 5V and (b) 10V

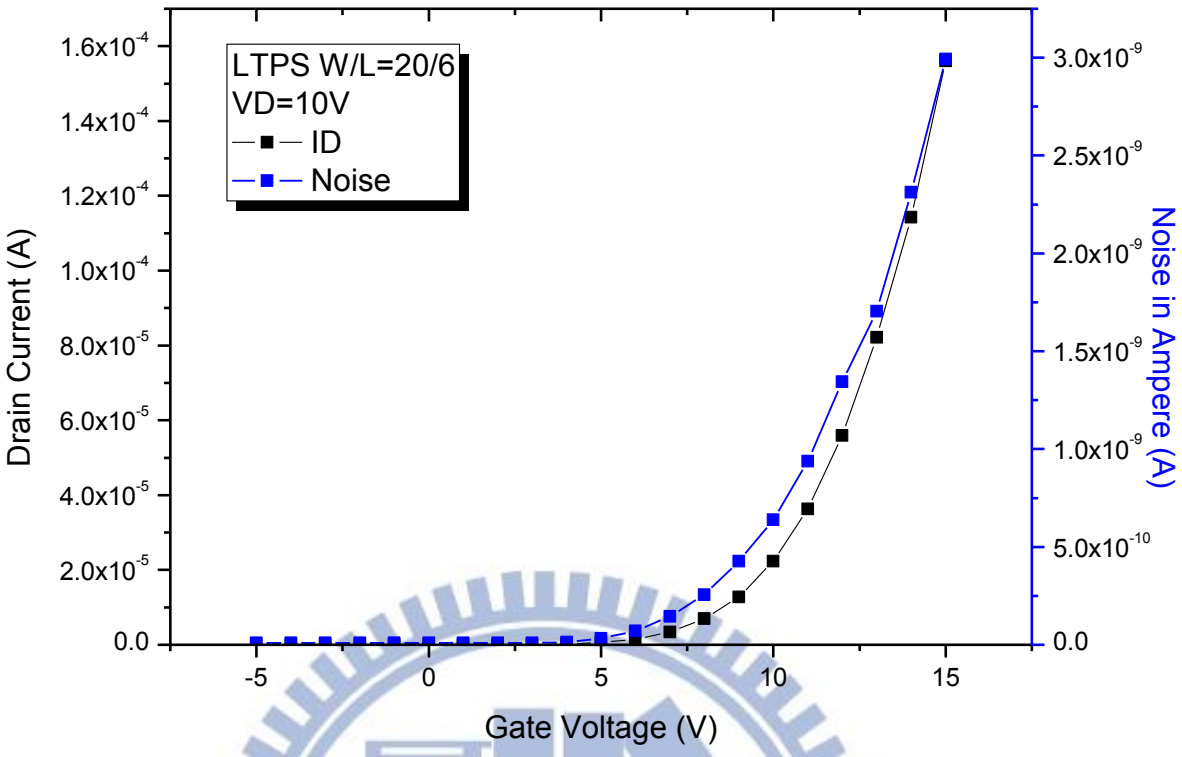


Fig. 2-8 (a) Drain current and NiA versus gate voltage with Y-axis in linear scale

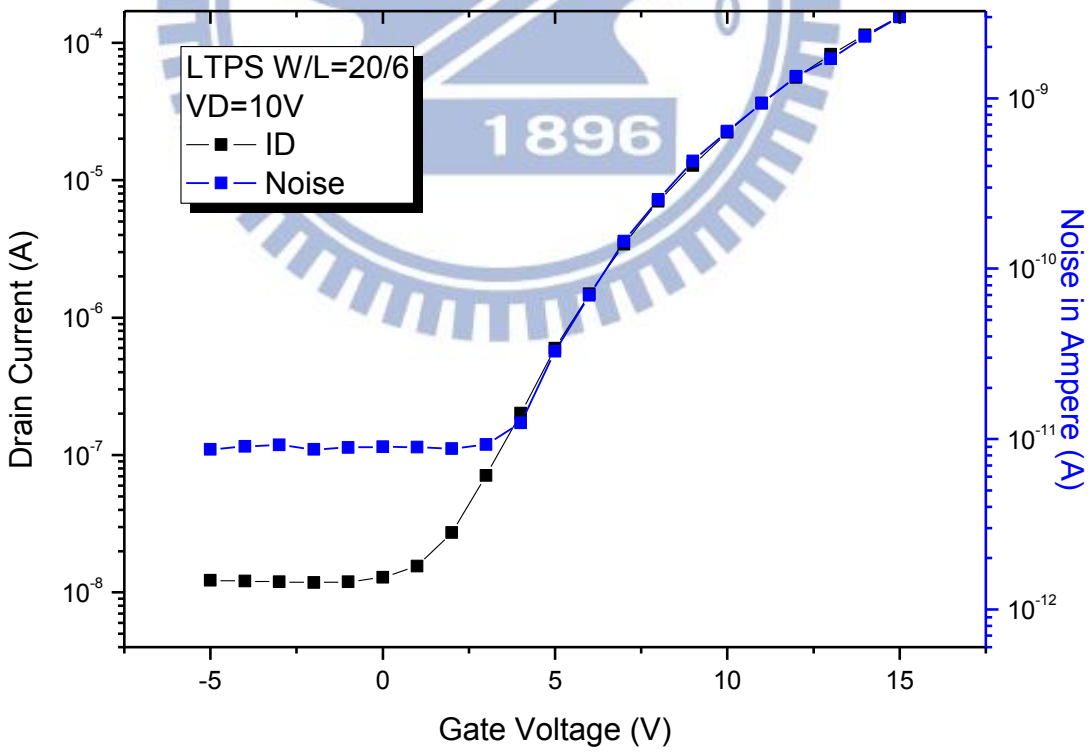


Fig. 2-8 (b) Drain current and NiA versus gate voltage with Y-axis in logarithm scale

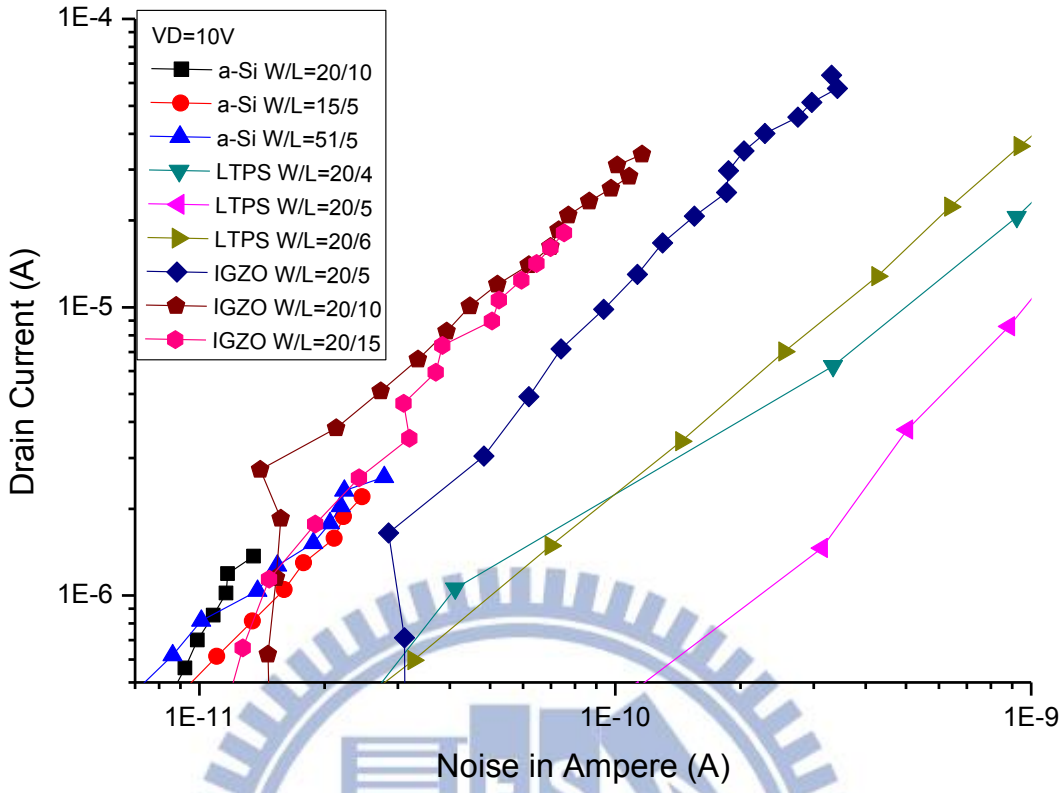


Fig. 2-9 Through the noise formula to get A and α in the nine element

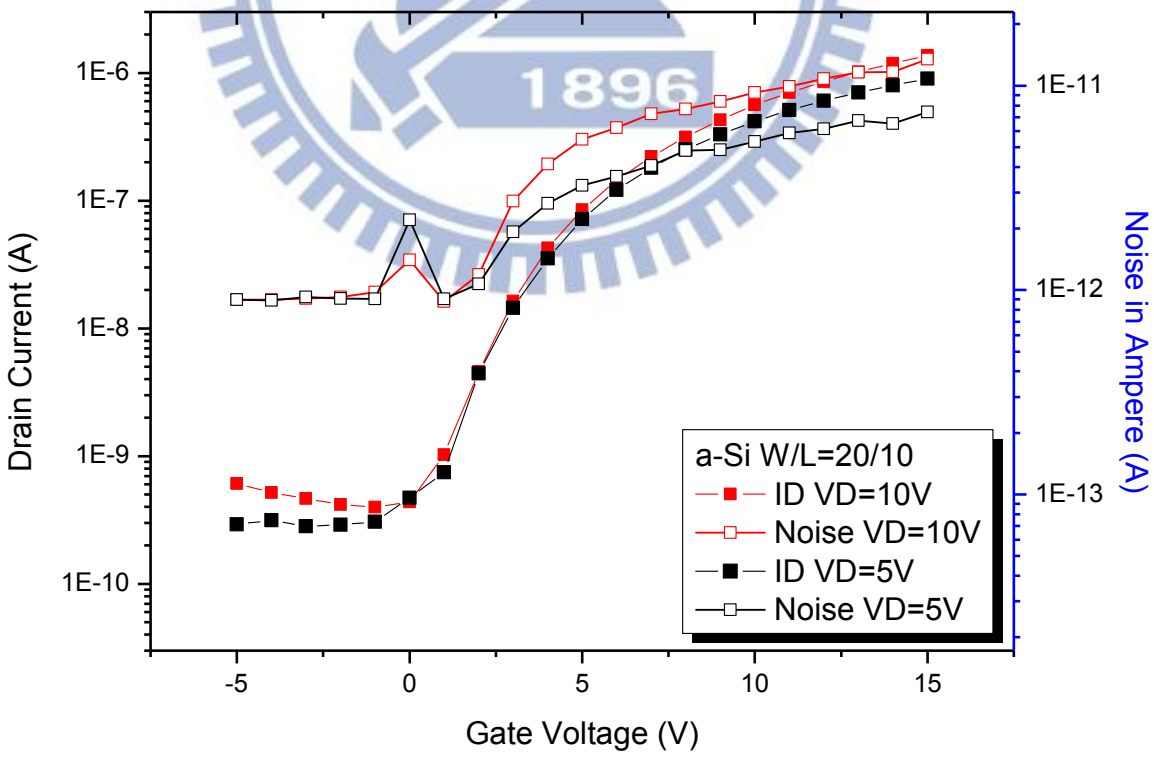


Fig. 2-10 (a) Adjustment of a-Si W/L=20/10 with A and α

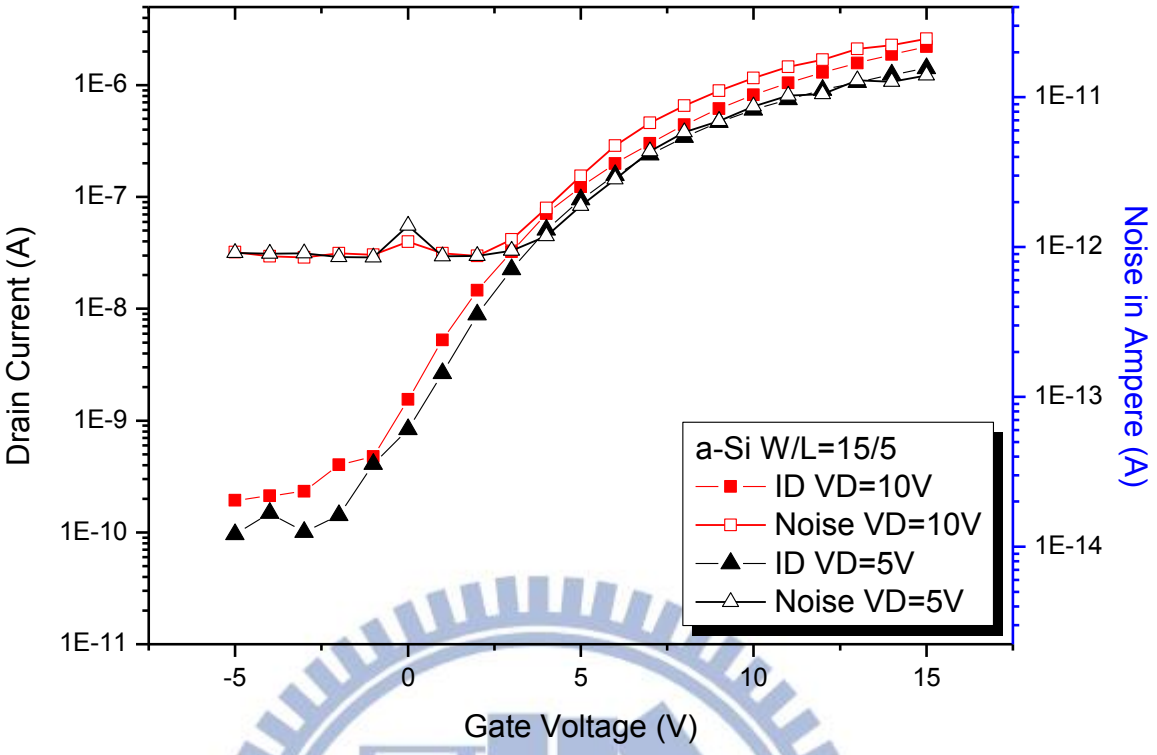


Fig. 2-10 (b) Adjustment of a-Si W/L=15/5 with A and α

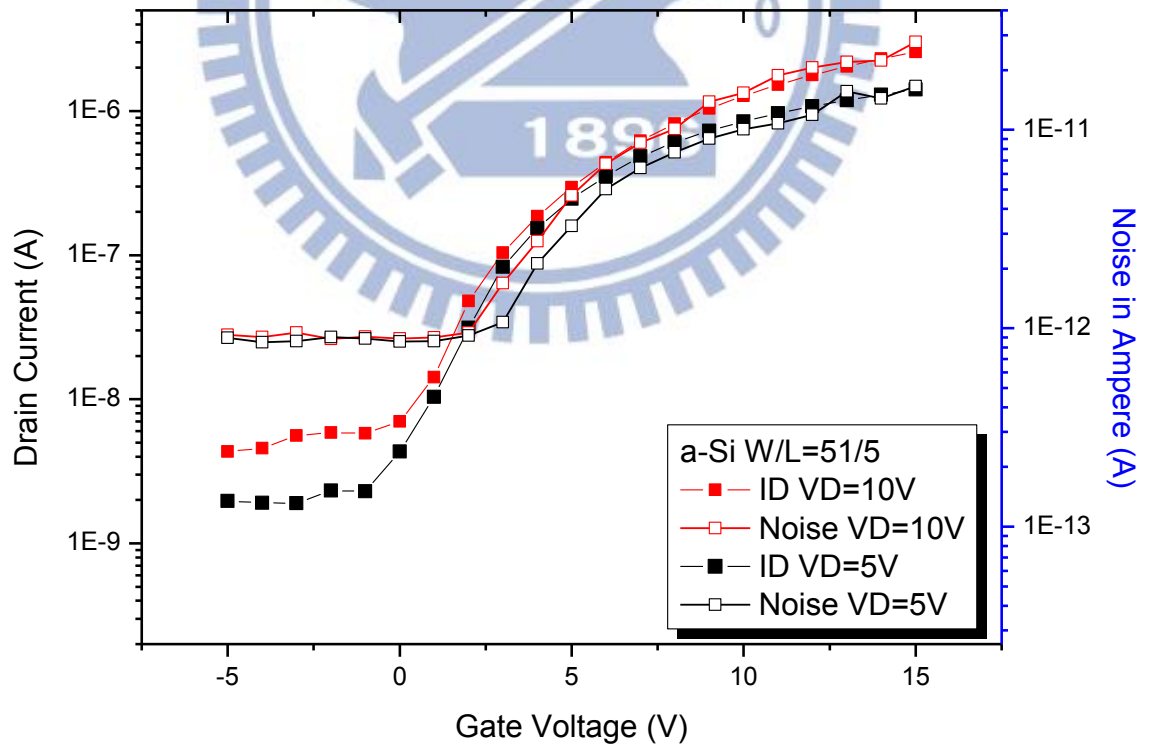


Fig. 2-10 (c) Adjustment of a-Si W/L=51/5 with A and α

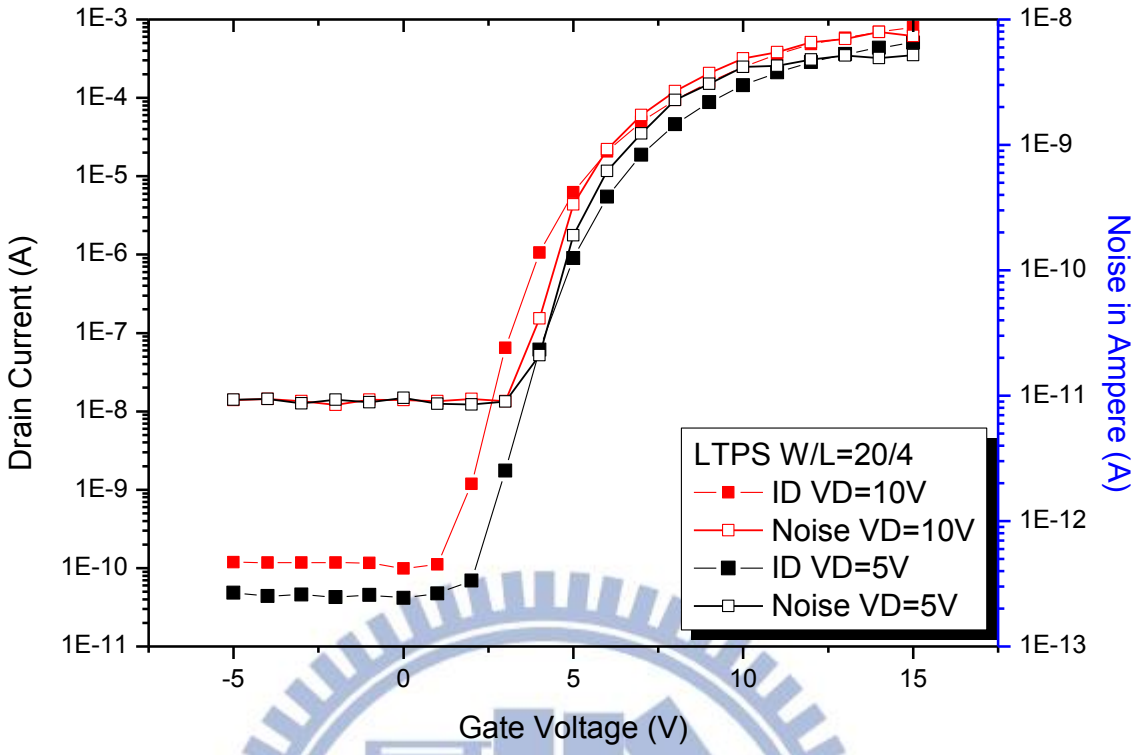


Fig. 2-10 (d) Adjustment of LTPS W/L=20/4 with A and α

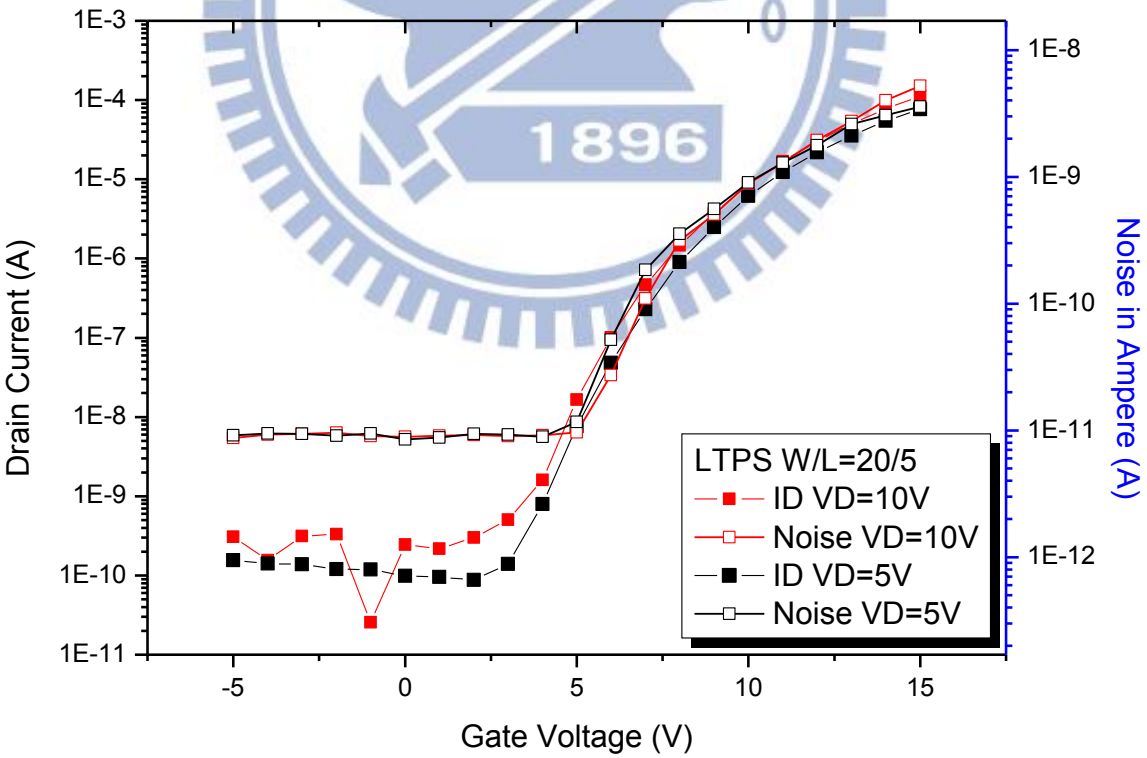


Fig. 2-10 (e) Adjustment of LTPS W/L=20/5 with A and α

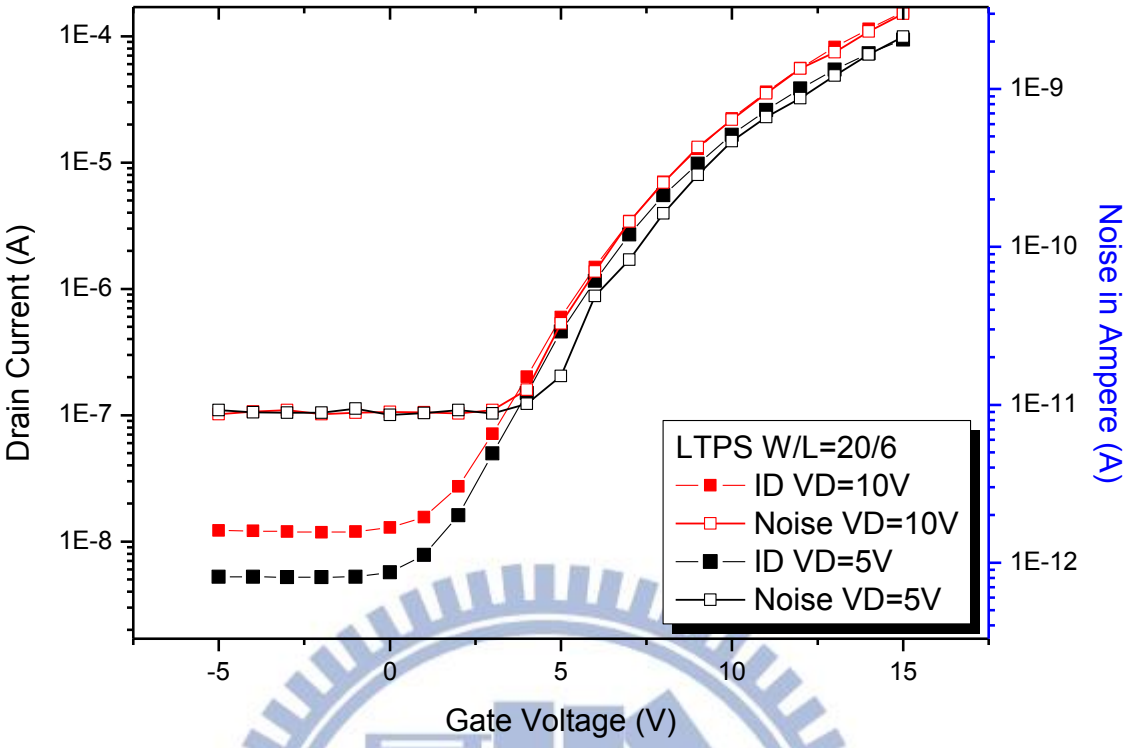


Fig. 2-10 (f) Adjustment of LTPS W/L=20/6 with A and α

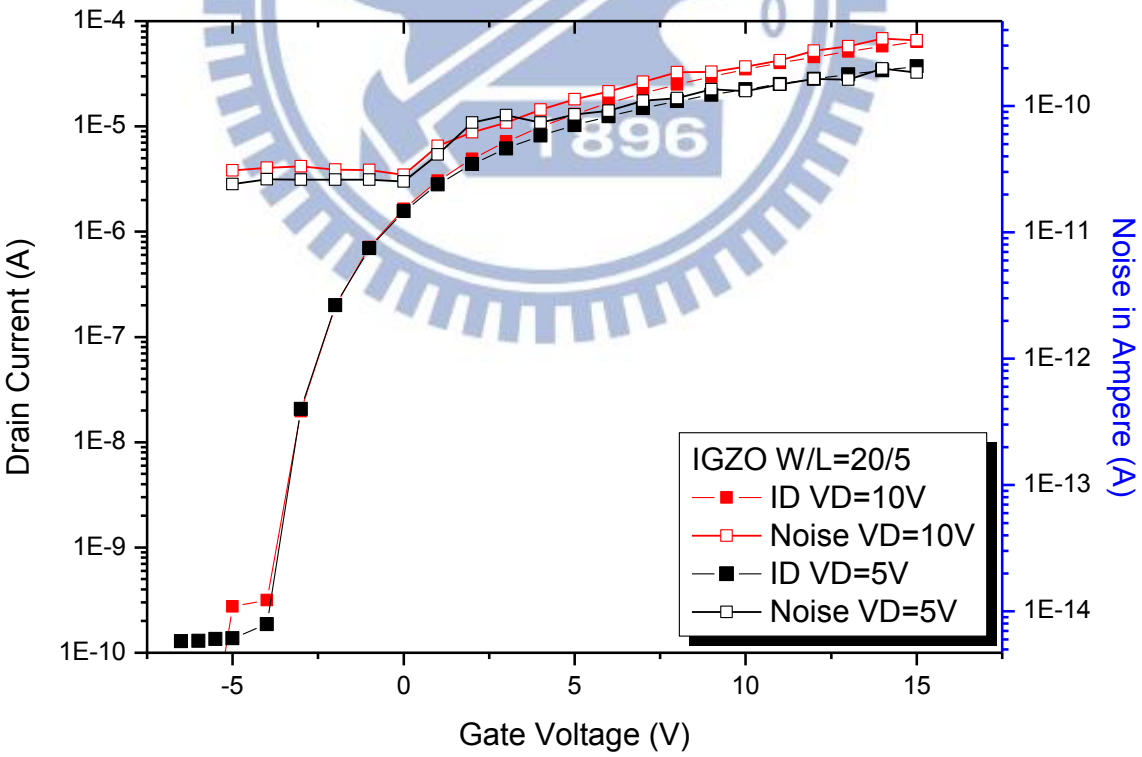


Fig. 2-10 (g) Adjustment of IGZO W/L=20/5 with A and α

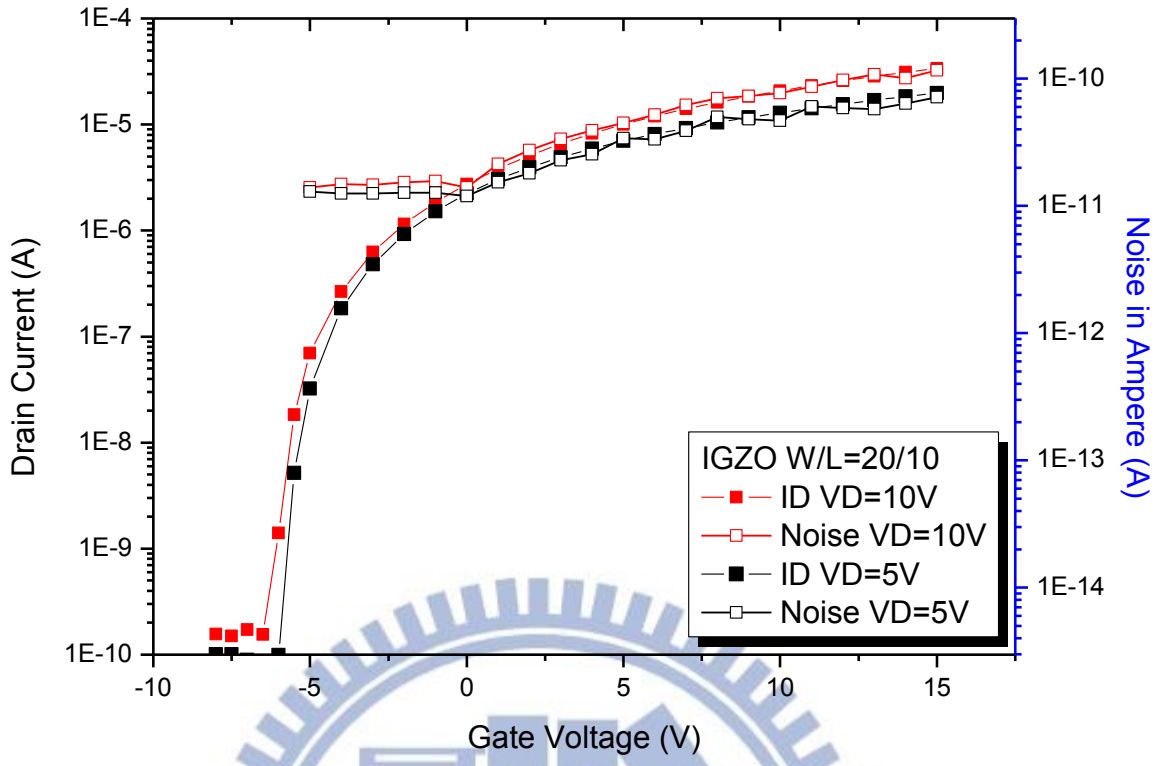


Fig. 2-10 (h) Adjustment of IGZO W/L=20/10 with A and α

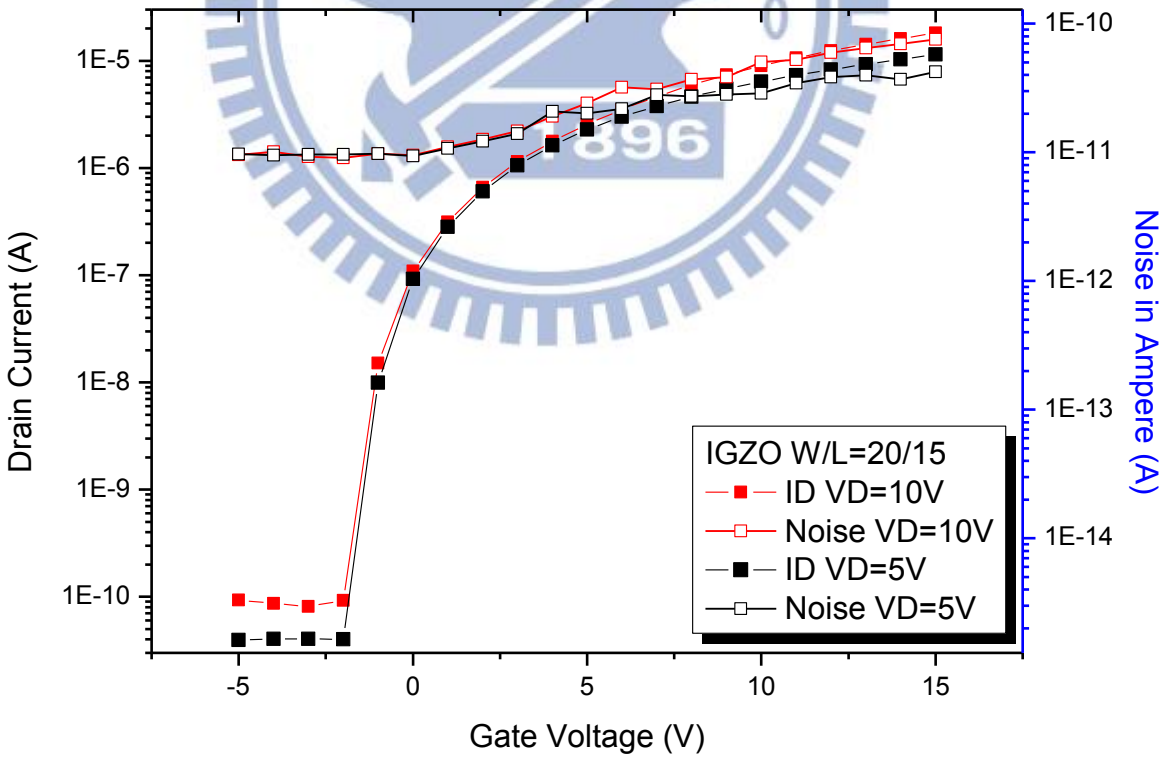


Fig. 2-10 (i) Adjustment of IGZO W/L=20/15 with A and α

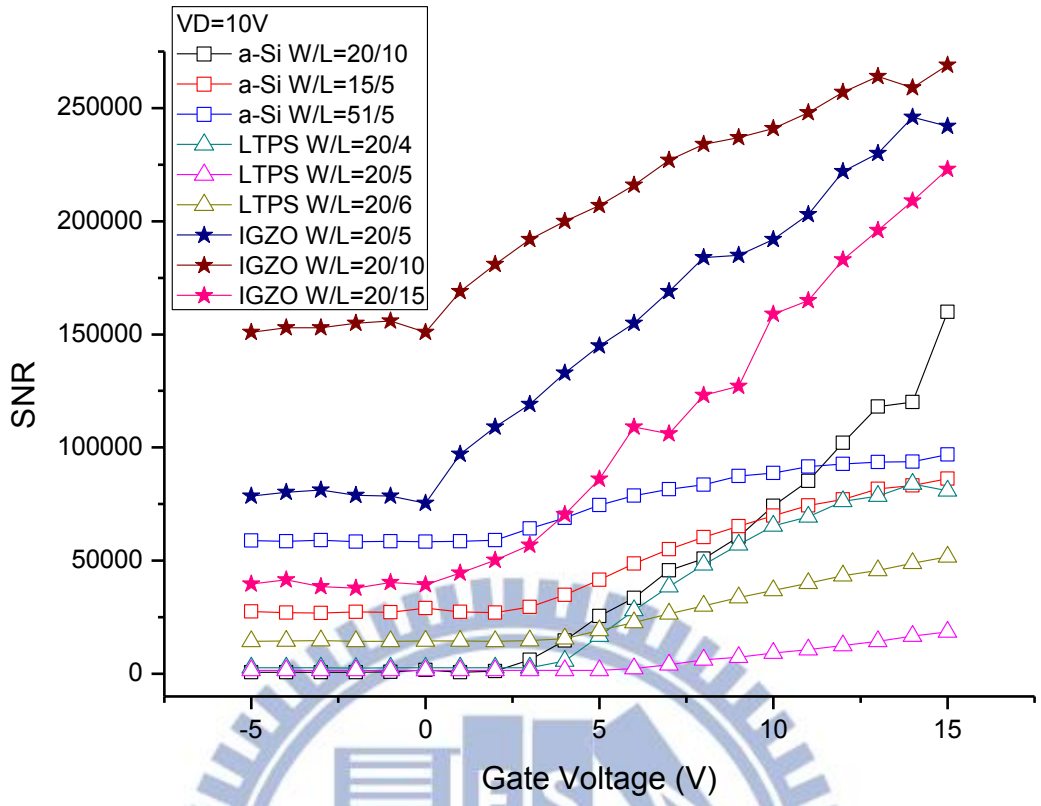


Fig. 2-11 (a) Plots the SNR for all the DUTs with VD=10V versus V_G

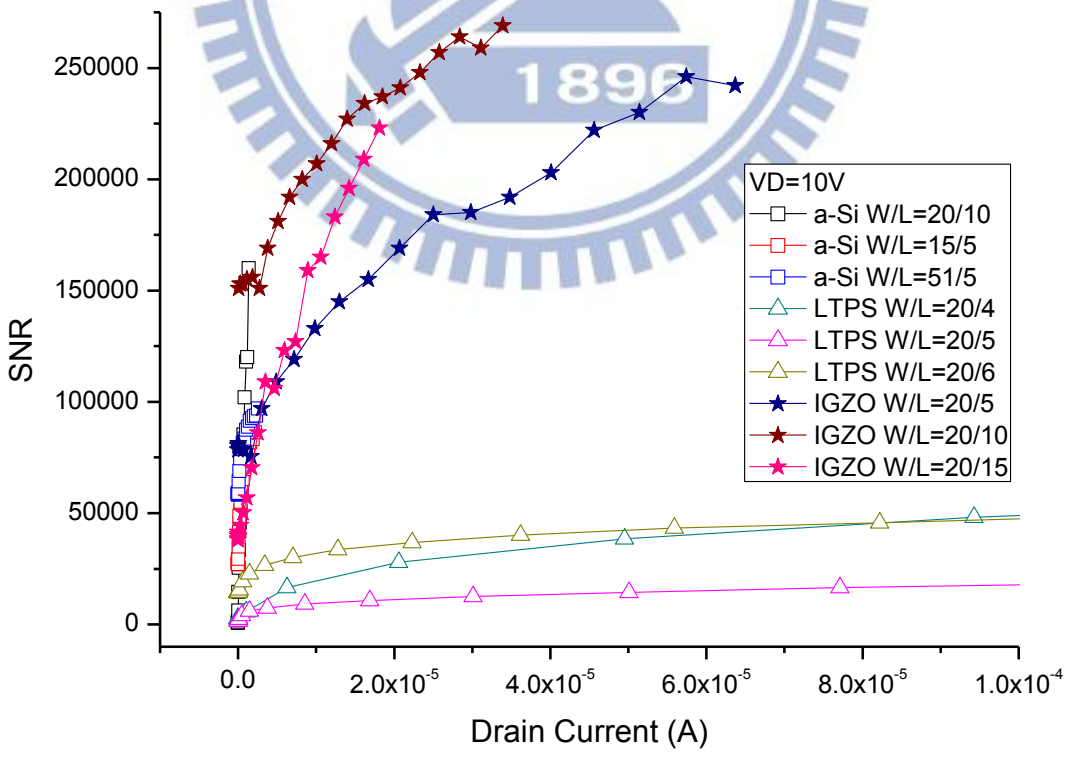


Fig. 2-11 (b) Plots the SNR for all the DUTs with VD=10V versus I_D

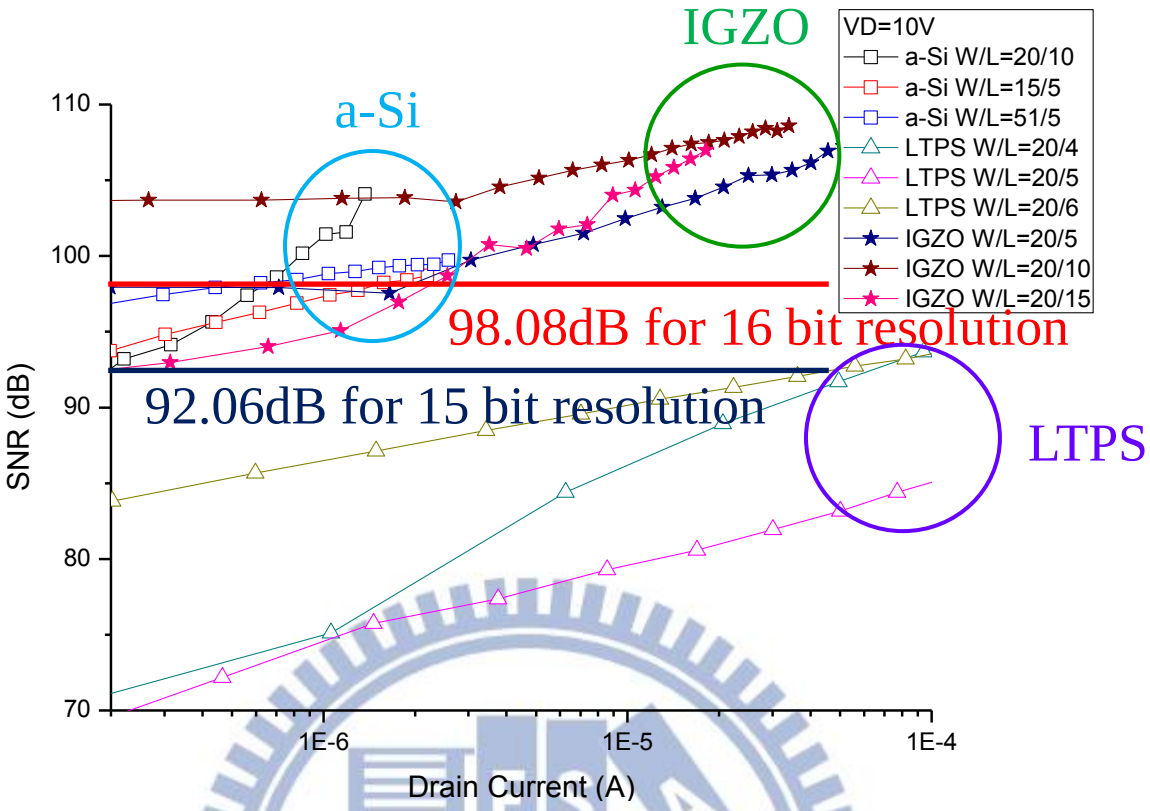


Fig. 2-11 (c) Replot the curves of SNR in dB scale versus I_D in logarithm scale

Chapter 3

Compensation Method

3.1 Two-TFT Pixel Circuit

In order to achieve simpler pixel structure and better resolution, minimal number of TFTs in the pixel circuit is preferred. Two-TFT (2T) pixel circuit design for APS was previously proposed to replace the 3T APS for high resolution [8]. Fig. 3-1 shows the proposed 2T1C APS architecture. The pixel circuit is composed of an amplifier TFT (T_a), a reset TFT (T_r), a storage capacitor (C_s), a photo detector, and the readout circuit is composed by integrator. Although the voltage-programmed circuit can cancel out the threshold voltage shift, it cannot compensate the mobility variation. Another proposed 2T2C current-programmed circuit which can compensate both the threshold voltage shift and mobility variation of amplify TFT, is shown in Fig. 3-2. However, both of these 2T pixel circuits can only compensate the status before exposure. Once the pixel is exposed and thus the voltage at the sensing node changes, the output current still varies with the mobility. Based on the same 2T2C current-programmed circuit shown in Fig. 3-2, we develop a new operation procedure. The newly proposed operation method can compensate not only the threshold voltage shift but also the mobility variations. Furthermore, it can calibrate the power factor in the equation of the output current depending on the gate voltage. It is to be explained in the following section.

3.2 Current-Programmed Circuit Operation

3.2.1 Calibration Procedure

The thin film transistor current formula of the saturated region is listed in the equation (3-1).

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_G - V_T)^{\beta} = K(V_G - V_T)^{\beta} \quad (3\text{-}1),$$

Where I_D is saturation current, Cox is oxide capacitance and the value of β is derived to be 2 with gradual channel approximation (GCA). However, in the study of calibration process on our device, it is found that the value of β is not necessarily equal to 2 and is subject to change with device. This power factor of β needs to be calibrated too. For the β value other than 2, the back-traced V_G at the sensing node according to I_D would be wrong. The full procedure of calibration is described below:

From equation (3-1), on both sides, taking the natural logarithm leads to equation (3-2):

$$\ln I_D = \beta\left[\ln K + \ln\left(V_G - V_T\right)\right] \quad (3\text{-}2)$$

When $V_G >> V_T$, the differentials of the both sides equation (3-2) can give the parameter value of β:

$$\beta = \frac{d\ln I_D}{d\ln V_G} \quad (3\text{-}3)$$

Then, by taking the power of $1/\beta$ on the both sides of equation (3-1), equation (3-4) provides linearity with the known β value:

$$I_D^{\frac{1}{\beta}} = K(V_G - V_T) \quad (3\text{-}4)$$

The slope and intercept of equation (3-4) correspond to K and V_T respectively, where $K = \frac{1}{2}\mu C_{OX}\frac{W}{L}$.

Using equations (3-1) to (3-4), as long as a number of known drain current I_D are given, the corresponding gate voltage V_G can be obtained accurately.

3.2.2 Circuit Operation

For the 2T2C current-programmed circuit shown in Fig. 3-2, Switch1 and Switch2 are shared in time by all the pixels in the same column outside the array. Switch1 is put between the drain of Ta and the current bias source, while Switch2 controls the path from the drain of Ta to the integrator. Since Ta is used as an amplifying TFT and T_r is used as a switch TFT, it is Ta to be calibrated. C1 and C2 are connected from the gate of Ta to the scan bus Vscan1a and ground, respectively. Fig. 3-3 shows the circuit driving scheme. From this timing diagram, the circuit operation can be divided into three stages that are compensation, exposure and sensing frame. The operation is described by following steps.

(1) Sequential Compensation

From Fig. 3.3, we repeat the same operation four times in compensation frame by adjusting the current bias differently instead of a fixed one. In the compensation period, for the first time, both of the scan lines in every pixel go high simultaneously to turn on Tr and couple a voltage on the gate of Ta via C1. As the Tr is on, the gate and drain (noted as g and d in Fig. 3-2, respectively) of the sensing TFT Ta are bound together to form a diode-connected TFT. At the same time, Switch1 is closed which

pouring the first bias current I_D into the diode-connected TFT. Thus, the gate is set to a corresponding voltage that stored in the capacitor C2. Furthermore, due to diode connection, we can force Ta to be in the saturation region with the drain and gate voltage of Ta equal, e.g. $V_G = V_D$. At this moment, we can measure this voltage out of the pixel at V_D, as shown in Fig. 3-2. After the first compensation, Vscan1a and Vscan1b go low. The voltage at g node will couple a negative voltage via C1 which cause Ta to turn off, which prevents the current from being poured into the pixel circuit. In such a way, we acquire the first point of equation (3-1) for the pixel compensation. Then, the Vscan2a and Vscan2b go high again for the acquisition of the second point for the pixel compensation by setting another value of the bias current. After repeating the same operation for totally four times by pouring into four different values of the bias current which make Ta in saturation, a set of four forced current versus measured V_D can be obtained. As a result, using these four groups of I_D and V_D=V_G data and then substituting them into equation (3-1), we can obtain the parameters of β, K, and V_T. These values are stored for the later calculation.

(2) Integration

Switch1 is opened and all scan signals goes low to inactivate all pixels for integration. The incident light generates sensing currents in the sensing pixels. The individual current induces the change in the gate voltage of the Ta for each pixel.

(3) Readout

In readout period, Vscan,a goes high sequentially to drag Vg to turn on Ta, while Switch2 is closed to feed the drain of Ta in every pixels with Vbias. Thus output current is produced sequentially and steered out to the input of charge amplifier to readout. The voltage change ΔV_G at the sensing node g can be calculated by the output current and the obtained β, K, and V_T for each respective pixel. Since C1 and C2 are known capacitance, the sensing charge ΔQ is given by ΔV_{G*}(C1+C2) and the

exposure light intensity is thus sensed.

3.3 Circuit Measurement and Results

After introducing the calibration procedure and circuit operation, in this section we test the circuit in actual operation. There are two purposes of the measurement. The first is to confirm that the parameters of β, K, and V_T can be extracted with different bias current values. The second is to verify that the current-programed circuit can really do the threshold voltage compensation.

3.3.1 Extraction of Parameters

Fig. 3-4 shows the measurement setup of the diode-connect with drain current biases simulate the configuration in the compensation period. The circuit includes two parts: the driving peripheral and the TFT circuit under test. For the driving part, Keithley 4200 is used to supply both sources of the accurate voltage and current bias. The values of V_{reset}, V_{node} and I_{bias} can be properly set to be from 5V to 25V, from 0V to 20V, and from 1μA to 6μA, respectively. For the circuit part, T_a and T_r are properly chosen to have the size of W/L=15μm/5μm and 20μm/10μm, accordingly. They are interconnected on the breadboard to form the circuit to be tested.

Fig. 3-5 shows the diode-connection current versus drain voltage of Ta. As can be seen, the diode characteristic only occurs when V_{reset} is larger than the drain voltage of T_a. As a result, the sink current with 1μA to 6μA are applied with V_{reset} =25V in the following experiment. Fig. 3-6 (a) shows how the node voltage corresponds to the bias current. The calibration parameters β、K and V_T extracted from Fig. 3-6 (a).The

value are 2.7118, 6E-4 and -5/600, correspondingly. These values are to be used later in the calculation of compensation.

Then, V_{reset} is set to -15V to turn off T_r, so that the circuit is in configuration for the sensing period. The gate voltage of T_a, which corresponding to the sensing node sweeps to measure the drain current as the sensed signal, as shown in the Fig. 3-6 (b).

The verify the validation of the proposed compensation method, we translate the measured drain current back to its corresponding node voltage at the gate of Ta using the flow chart shown in Fig 3-7. The traced-back node voltage is compared with the applied gate voltage in Fig. 3-8, as well as in table 3.1. From the table, we consider the minor variation error comes from the Early effect of TFT, which occurs when the drain voltage rises. This effect results in the reduced channel length and then cause slight increase drain current. Fig. 3-9 shows the I_D-V_D characteristic curves of Ta. As can be seen, the Early effect is quite small. Consequently, the error is less than 1.5% after utilizing the calibration method.

By the way, if we use different bias currents as the reference in the step of parameter extraction, the variation can have a little change accordingly. Therefore, the appropriate selection of the reference bias current can further reduce variation and improve the system performance.

3.3.2 Circuit Compensation Verification

3.3.2.1 Scheme and Operation

In this section, we verify the threshold voltage compensation mechanism with current-programmed circuit experimentally. Fig. 3-10 shows the test pixel circuits and

its driving scheme. In this experiment, we use the IGZO TFTs as the switch, amplifying and reset TFTs. The IGZO TFTs have higher drain current to provide more convenience in the measurement with oscilloscope.

The width the TFTs in the test circuit are all 20μmwhile the length of T_a, T_r, Switch 1, Switch 2 and Switch 3 are 20μm, 20μm, 20μm, 5μm, and 5μm, correspondingly. The capacitance of C1, C2 and C3 are 50pF, 5pF and 100pF, respectively. Vbias is fixed at 15V while Ibias is fixed at 5μA. Since it is hard to find many devices with different threshold voltages, , we instead change the value of Vref from -2V to 2V with 0.5V voltage step to simulate the threshold voltage shift in Ta. Connecting to the two inputs of the operational amplifier, the Vref and the source of Ta are virtually shorted to each other. As a result, we can rewrite the drain current in saturation region formula as

$$\begin{aligned} I_D &= \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS}-V_T)^2 \\ &= \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_G-V_{ref}-V_T)^2 \\ &= \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_G-(V_{ref}+\Delta V)-(V_T-\Delta V))^2 \end{aligned} \quad (3\text{-}5).$$

With the constant bias current of I_D, $V_G - V_{ref} - V_T$ needs to be constant, too. For the invariant V_T of Ta during the experiment, the change ΔV in Vref can simulate the shift of $-\Delta V$ in threshold voltage.

3.3.2.1 Compensation of Verification Results

Fig. 3-11 (a) shows the measured waveform of the gate voltage for the 2T2C current-programmed circuit with changing Vref. As can be seen, the gate voltage variation range is 4.03V, which can correspond to the changing range of 4V in V_{ref}.

Furthermore, Fig. 3-11 (b) shows the output voltage signal waveforms, which shift down with V_{ref} accordingly. The output current I_{out} can be calculated from the slope of the output voltage (V_{out} / Time) in the readout period by the formula below:

$$I_{out} = C_3(\Delta V_{out} / \Delta Time) \quad (3\text{-}6).$$

Fig. 3-12 shows the current variation versus threshold voltage shift and its corresponding error with and without compensation. It is observed that the Ivariation without compensation is as high as 131.12% owing to the +/- 2V V_T shift. With compensation, the Ivariation is reduced to 7.17%. As a result, it verifies V_T compensating function of the proposed circuit successfully.

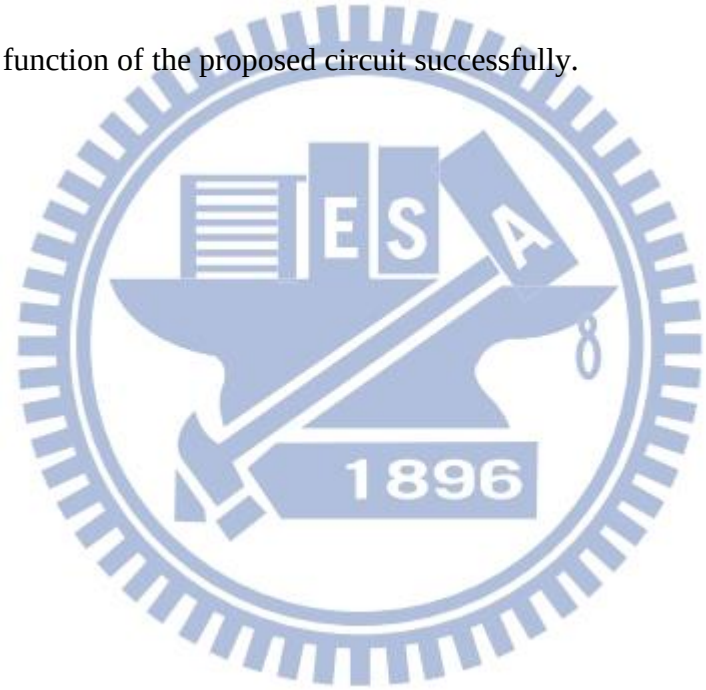


Table 3-1 Variation of V_{node} after calibration

I_D(A)	V_G(V)	V_{node}(V)	V_{node} Fitting(V)	Variation (%)	Variation Fitting (%)
3uA	15.1	15.4	15.32	1.98	1.47
4uA	16.8	17.11	17.00	1.84	1.22
5uA	18.3	18.58	18.45	1.53	0.81
6uA	19.7	19.88	19.74	0.94	0.20

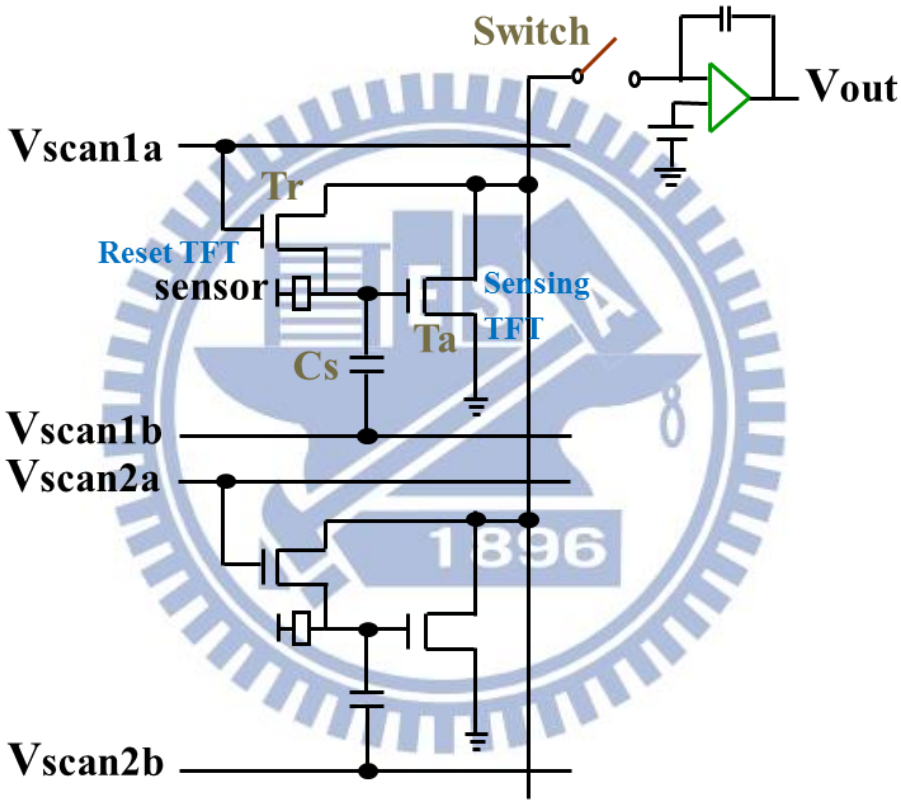


Fig. 3-1 2T1C voltage-programmed circuit with voltage source

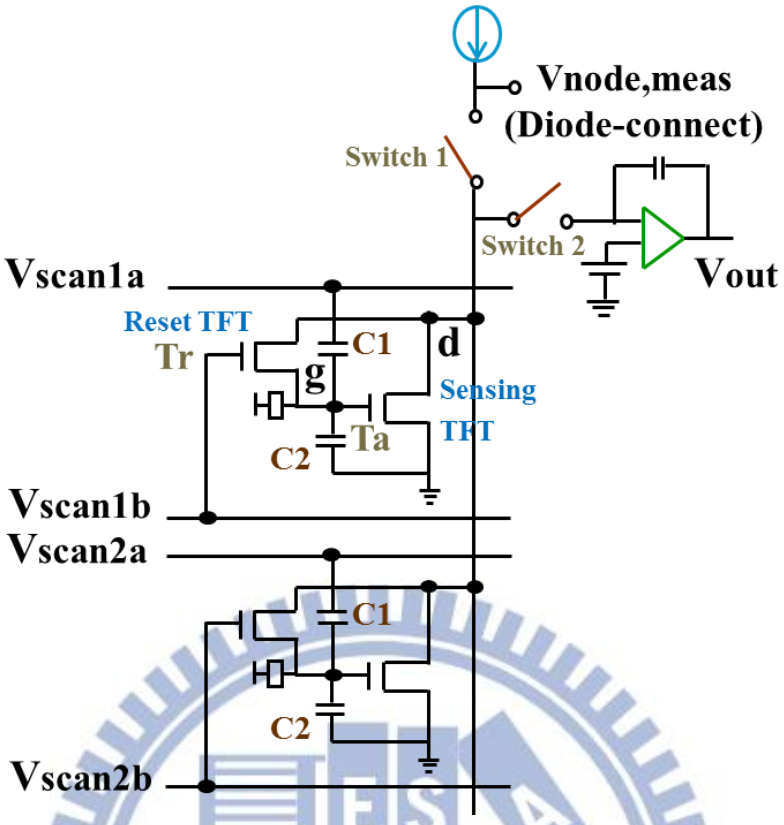


Fig. 3-2 2T2C Current-programmed circuit with Ibias flowing into pixel

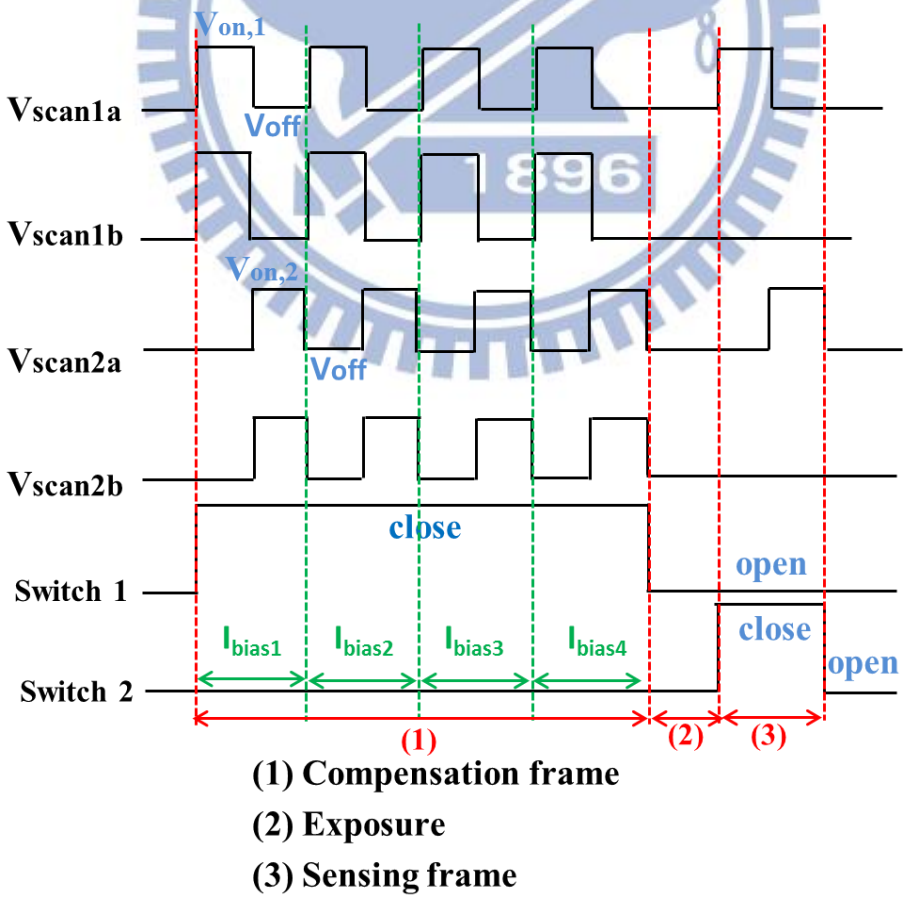


Fig. 3-3 Current-programmed circuit driving scheme

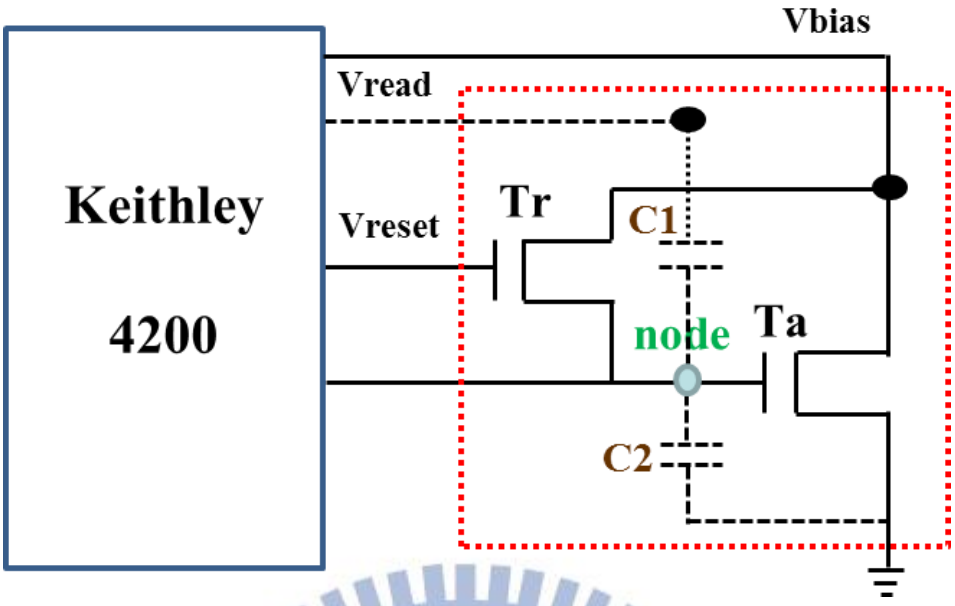


Fig. 3-4 The measurement setup of diode-connect with drain current bias

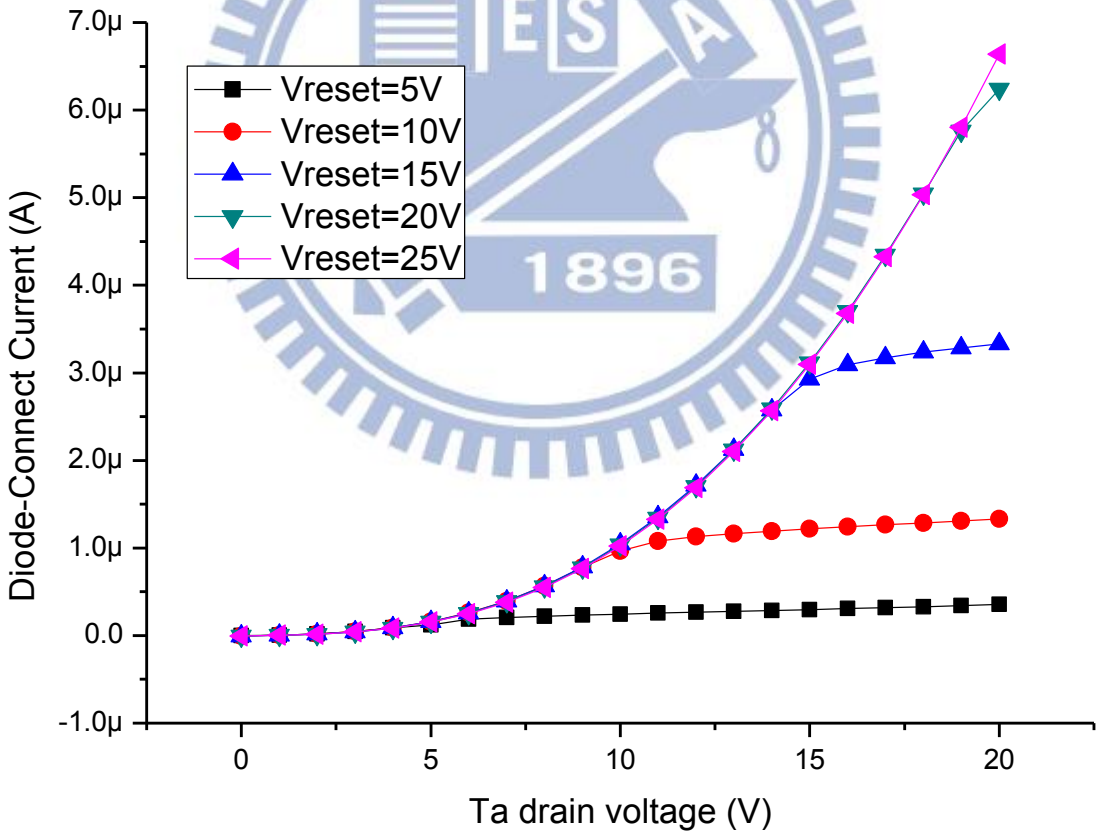


Fig. 3-5 Diode-connect current versus drain voltage of Ta

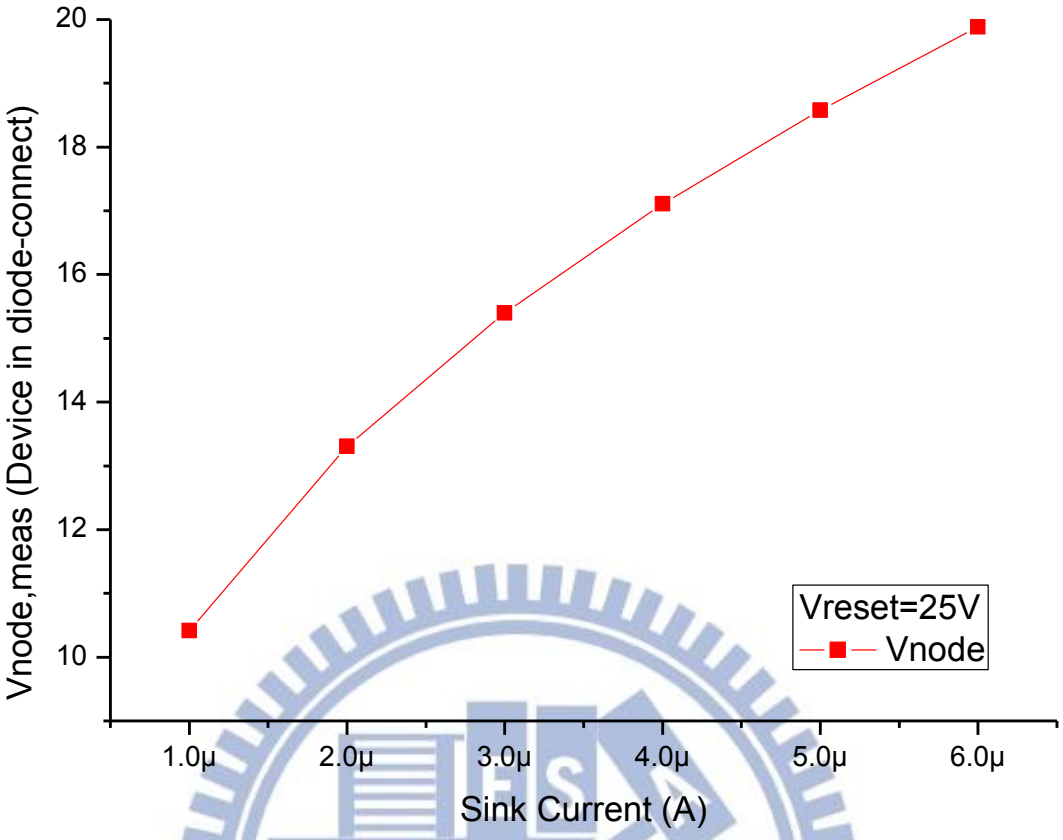


Fig. 3-6 (a) The node voltage corresponds to the bias current

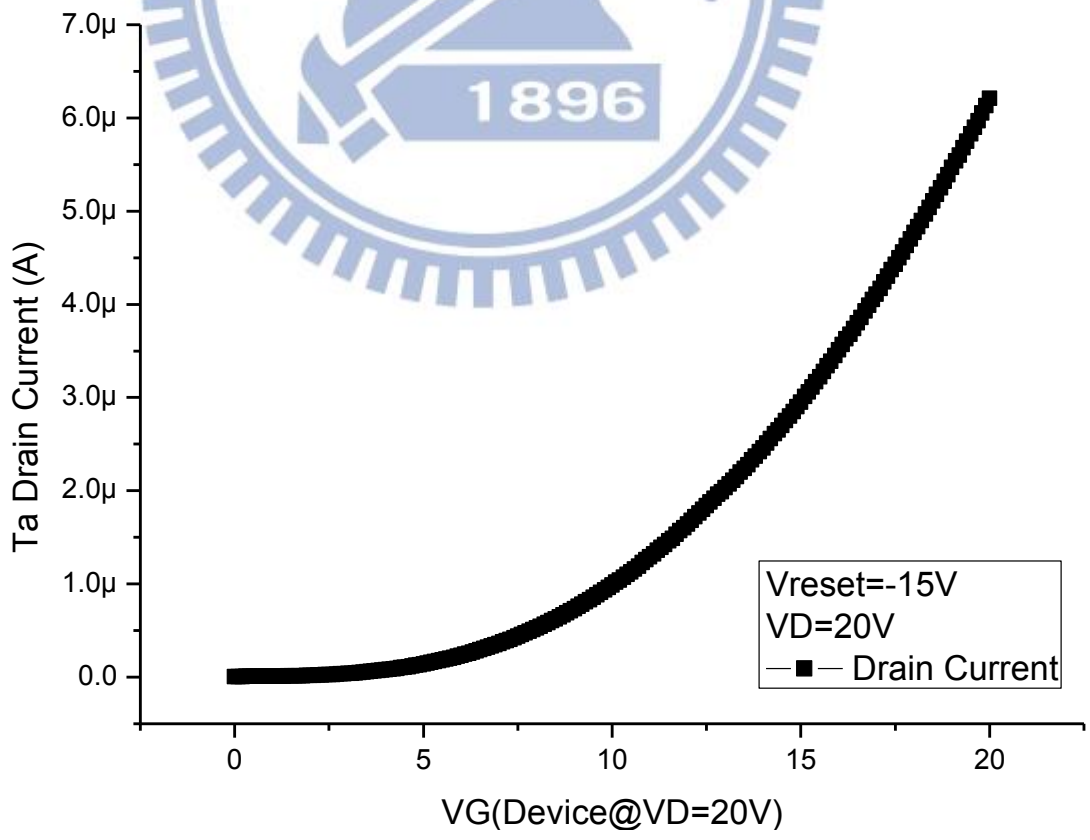


Fig. 3-6 (b) The sensing node sweeps to measure the drain current as the sensed signal

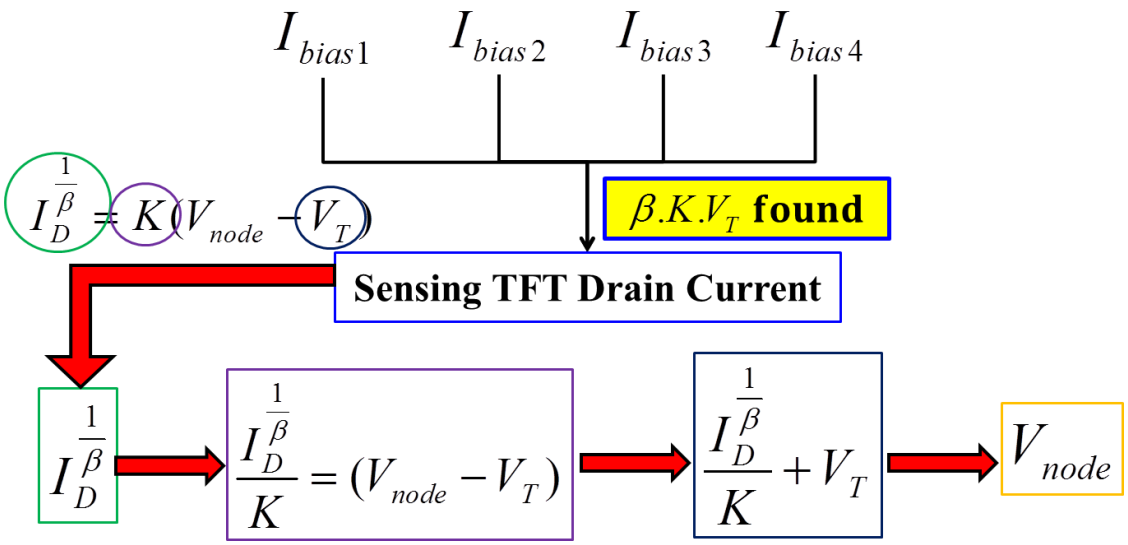


Fig. 3-7 The flowing chart with back stepping Ta gate voltage

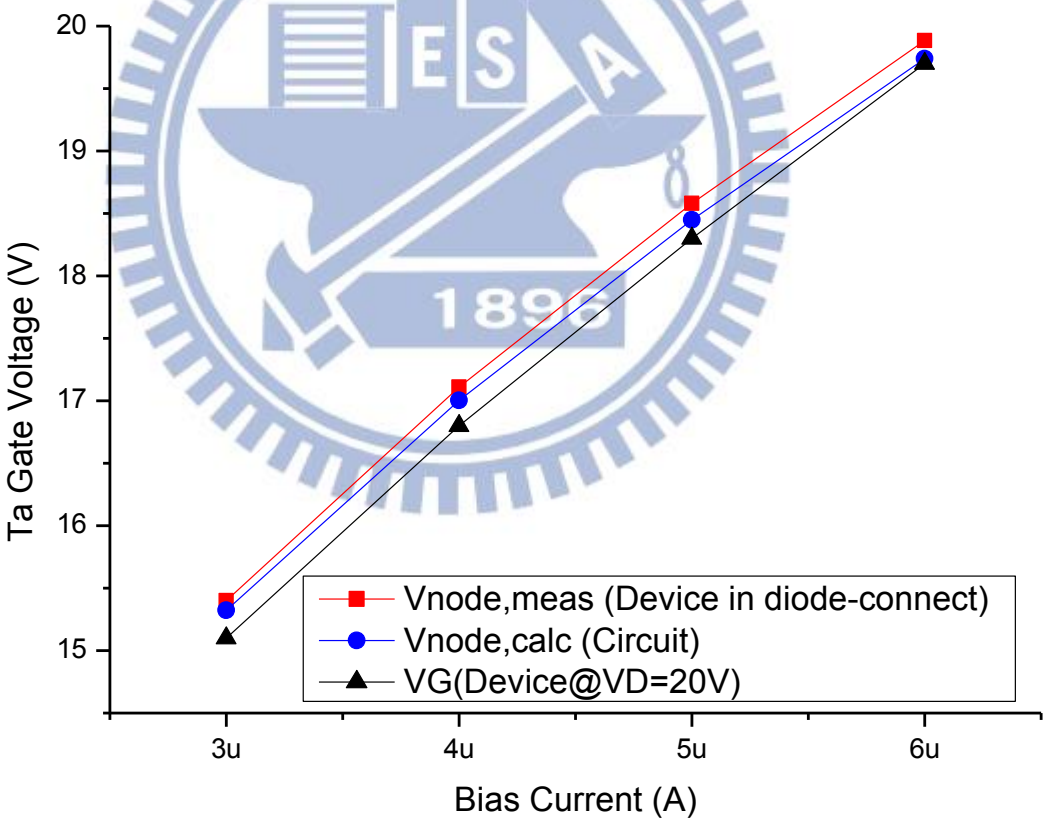


Fig. 3-8 The traced-back node voltage is compared with the applied gate voltage

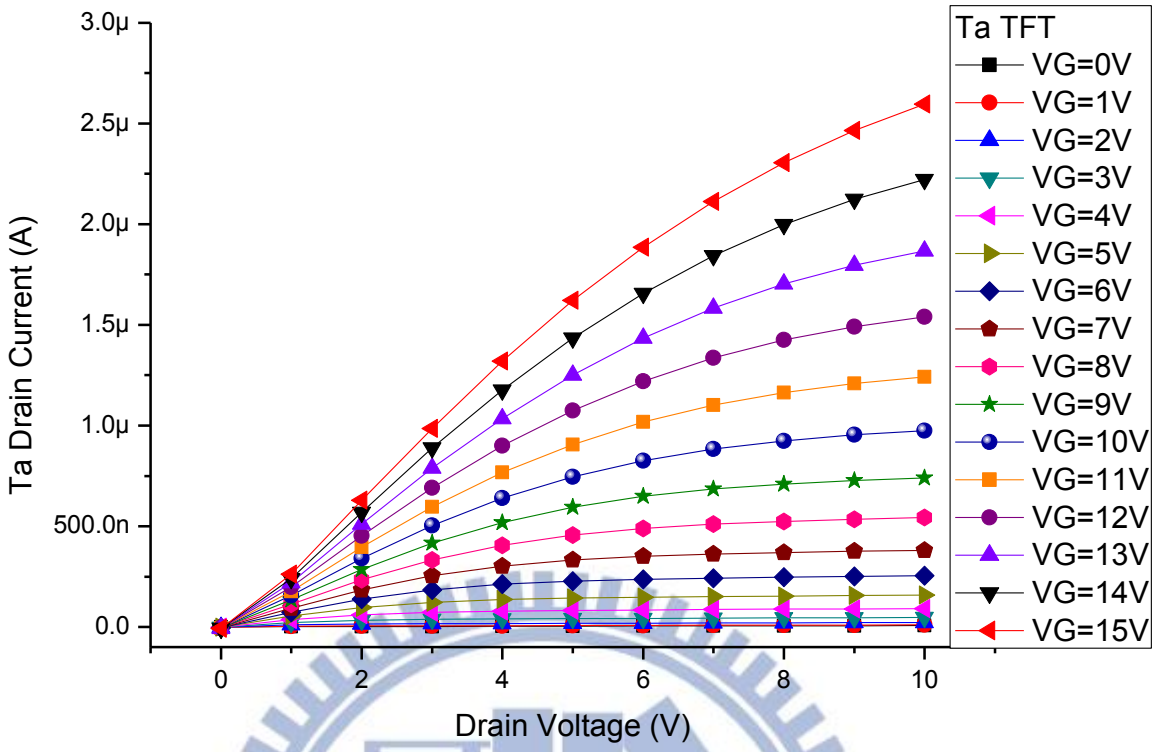


Fig. 3-9 The I_D-V_D characteristic curves of Ta

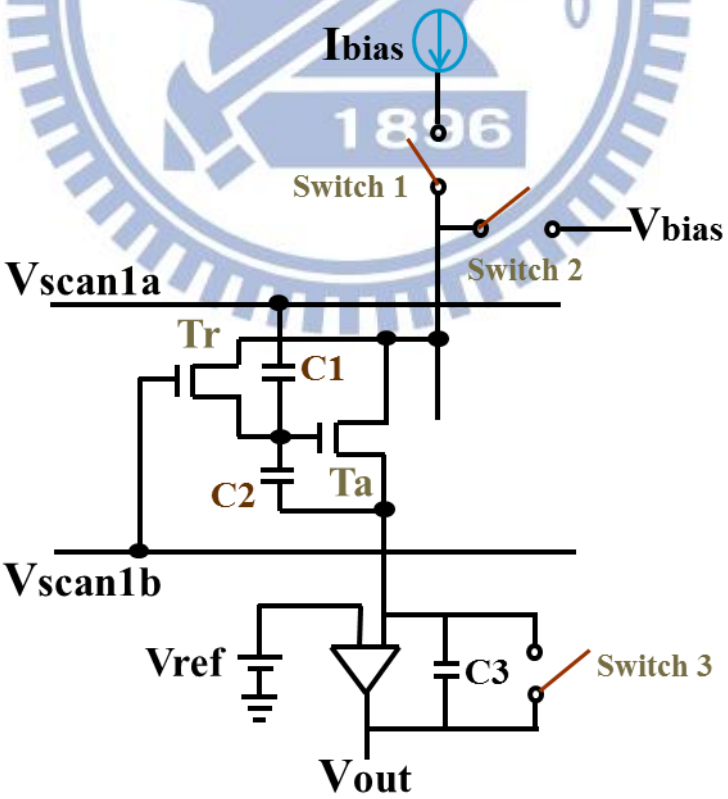


Fig. 3-10 (a) Current-programmed circuit with compensation function

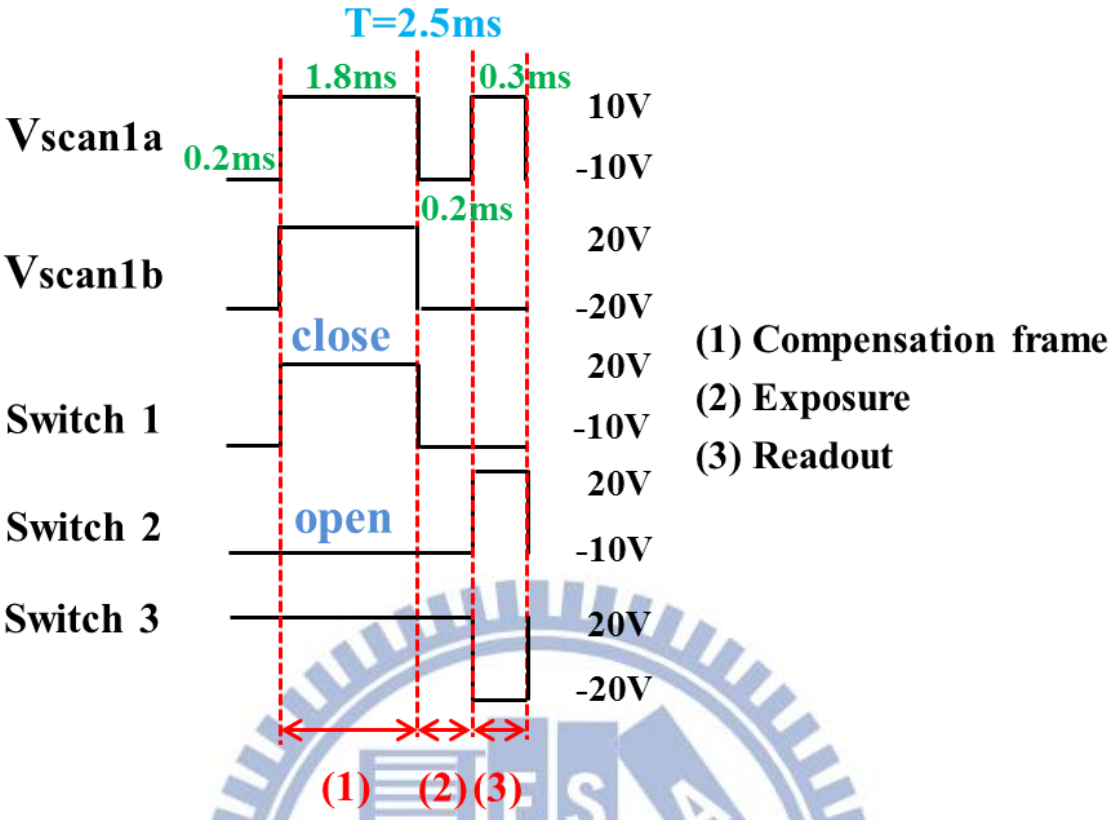


Fig. 3-10 (b) The driving scheme for the circuit of Fig. 3-9(a)

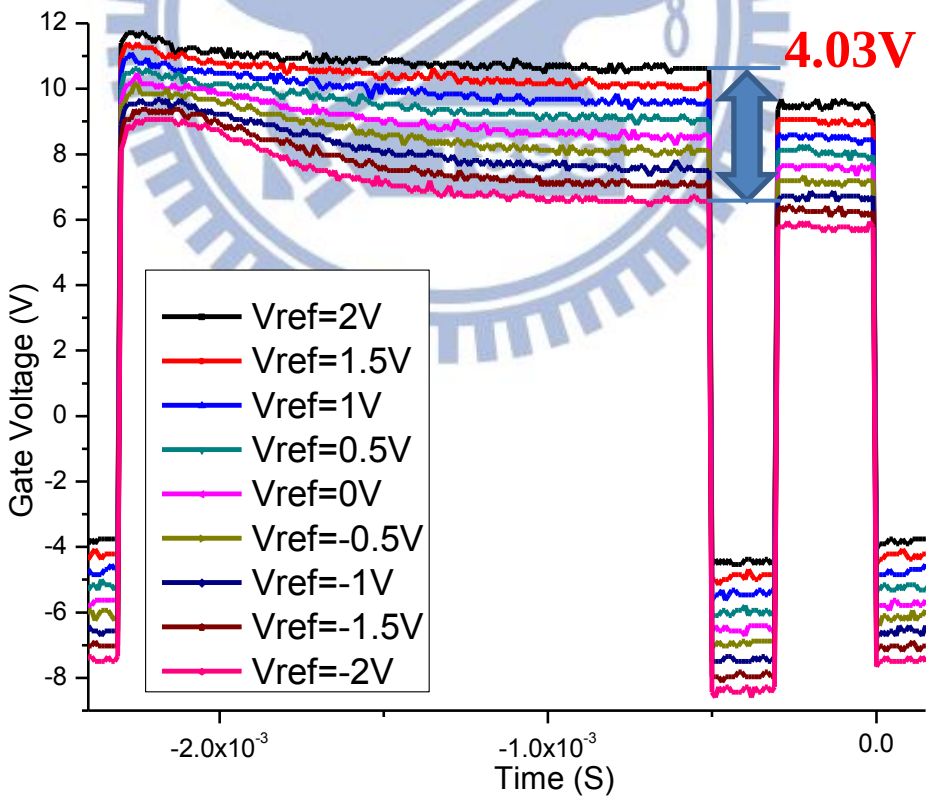


Fig. 3-11 (a) 2T2C current-programmed circuit of gate voltage waveform with changing Vref

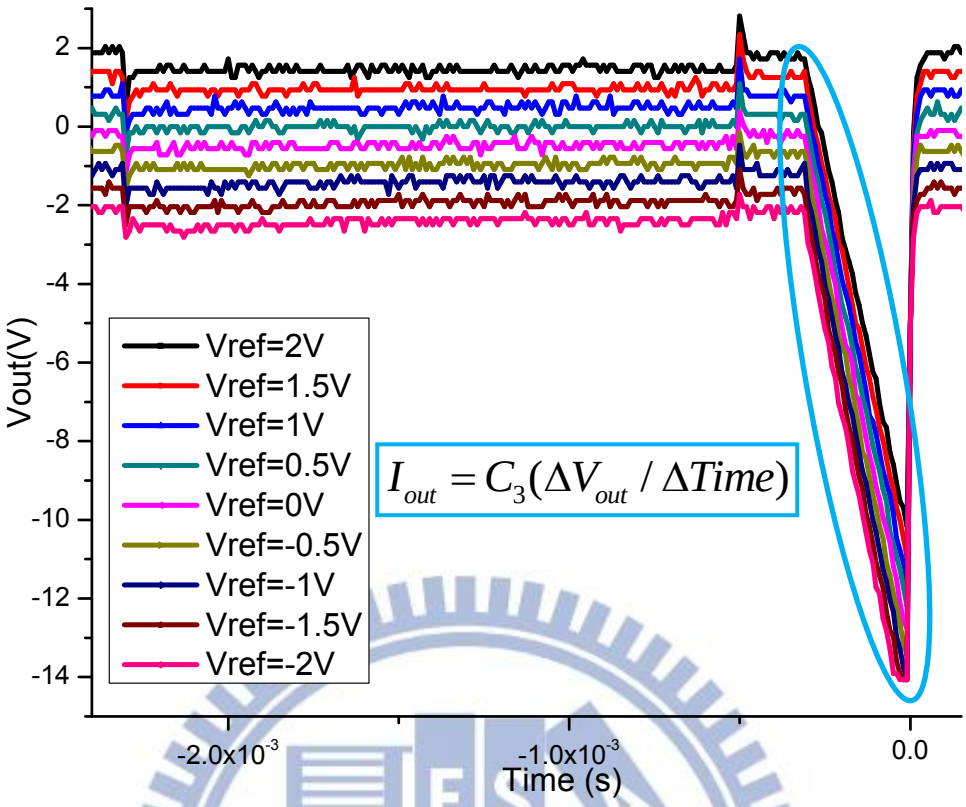


Fig. 3-11(b) The output voltage waveform

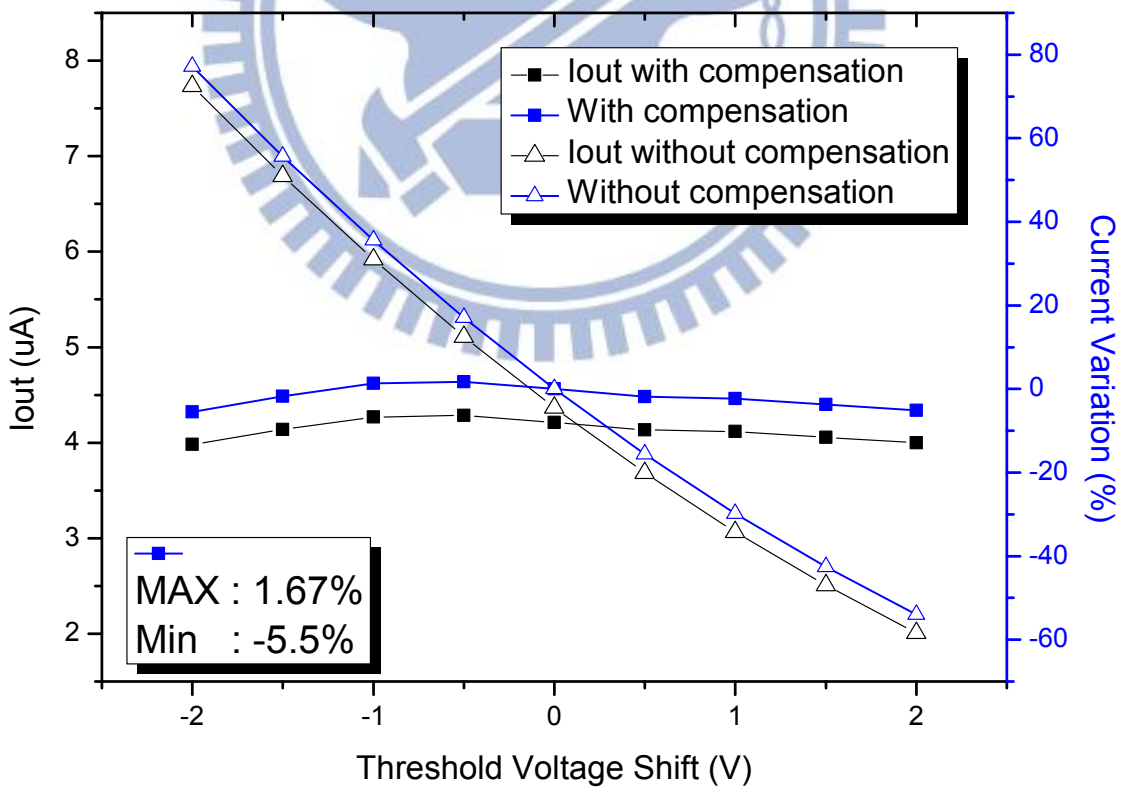


Fig. 3-12 The output current and the corresponding variation versus threshold voltage shift with and without the compensation

Chapter 4

Conclusions and Future Works

In this thesis, for the device noise measurement and analysis, the new index NiA is defined. In such a way, the noise is expressed in ampere, so that the calculation of SNR can be easy. In addition, since the noise is calculation by integration, the error induced by non-(1/*f*) dependence can be avoided. Furthermore, the noise formula is proposed. Using this formula, the relation between NiA and I_D can be well described. We can further represent SNR with respect to I_D. By plotting SNR versus I_D, several DUTs are compared to find that IGZO TFT is the best choice for the application of APS.

On the other hand, based on the current-programmed circuit, we propose a new calibration method to compensate the threshold voltage shift, mobility change, as well as the variation in the power dependence of I_D. Experimentally, we verify the function of the compensation.

In the future, we want to correlate the β parameter in the drain current equation to the A and α values in the noise formula both in experiment and in theory. The validation of the noise formula in other devices such as photo sensors is to be explored.

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