國　立　交　通　大　學

機械工程學系

碩士論文

振動式微環形陀螺儀之感測電路設計

The Design of Sensing Circuit for Micro-Vibrating Ring Gyroscope

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摘要

本論文之目的在探討微小環形諧振式陀螺儀的感測電路設計。微小環形諧振式陀螺儀是利用微機電製程所製造的微小結構，透過震動時結構的改變引起兩結構間的電容值改變，而這個電容值非常的微小，通常在 fF 等級。若是透過打線將訊號線外接到電路板上可能因訊號太小雜訊過大而無法量測出來，因此本論文將量測電路積體化，藉此減少打線的距離以及電路的雜訊。

目前被廣泛的使用在電容量測的電路有同步偵測電路以及切換式電容電路。切換式電容電路需要複雜的時脈電路以及有 MOS 作為開關所產生的雜訊，而同步偵測電路不需使用到開關以及複雜的時脈電路，並且可以消除放大器的寄生電容問題以及減少 1/f 的雜訊。所以選用同步偵測電路來作為這次的設計架構。

本論文將對整個同步偵測電路做介紹、電路分析、設計以及模擬。採 TSMC 0.35um, 2P4M, Mixed-mode, 3.3，5V 的製程參數來模擬及實現。

The Design of Sensing Circuit for Micro-Vibrating Ring Gyroscope

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Abstract

Probing into design of the capacitance detecting circuit for the micro gyroscope is the purpose of this thesis. Micro gyroscope is the small structure made with MEMS process. The sensing signal of this gyroscope due to the gap changes while the gyroscope shakes, then the capacitive value between the gap changes too. The capacitive value is very small and usually of fF grade. If we connect this signal to the sensing circuit on PCB, this signal can not be examined out because the signal/noise ratio is too small. So in this thesis, we try to design the capacitance detecting circuit in integrated circuit technology in order to reduce the noise of the sensing circuit.

Presently, the popular method in capacitance detecting circuit contains of the synchronous detection circuit and the switched capacitor sensing circuit. The switched capacitor sensing circuit needs complicated clock circuits and suffers from the noise of the MOS switch. However, the synchronous detection circuit doesn't. Besides, it can cancel the parasitic capacity and the *1/f* noise. So we select the synchronous detection circuit for use.

This thesis contains of examining circuit structure, circuit analysis, design, simulation and realization for the synchronous detection circuit with the model of TSMC 0.35um , 2P4M , Mixed-mode, 3.3, 5V.

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Chapter 1 Introduction

1.1 History

Nowadays, with the semiconductor manufacturing technology develop rapidly the MEMS (Micro Electro-Mechanical System) process also develop rapidly. It brings the mechanical structure size into micro scale and fabricates high performance sensor with low cost. The sensors fabricate with MEMS process contain of the accelerometers [1], the pressure sensor [2], and the gyroscopes [3]. Conventionally, gyroscopes, which detect the angel or angular velocity of an inertial object, have been widely employed as a core part of navigation apparatus for guided missiles, vessels or airplanes mainly. Micro gyroscopes have found large attention in recent years due to their low-cost, small-size, and some unique features making them ideal for several commercial and military applications, e.g. inertial navigation, control system, defense, avionics and space.

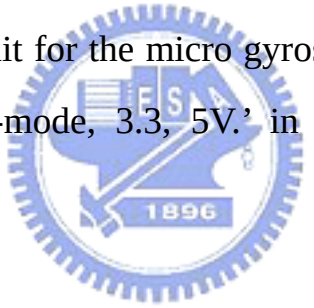
Our micro-vibrating ring gyroscope [4,5] is shown in Fig. 1.1 and Fig. 1.2. Fig. 1.1 is the overview of the gyroscope. It consists of the main ring, eight support rings and eight electrodes. Fig. 1.2 shows the top and detailed views of the structure includes the electrode. The main structure of micro-vibrating ring gyroscope is made by deep reactive ion etching (DRIE) of a silicon substrate is bonded to PYREX 7740 glass by anodic bonding.

1.2 Motive

Any MEMS sensor structure needs a circuit to read out the sensing signal.

With the micro gyroscopes structure, it needs a sensing circuit in order to read out the sensing signal. The signal/noise ratio is too small to read out the signal by connecting the signal to the circuit on PCB. And by this way, there exists parasitic capacitor at the wire bonding pad. This will influence the read out signal if the sensing circuit can not cancel it.

In the MEMS process, it is hard to combine the circuit and mechanical structure in the same process. This is because the structure needs high-aspect ratio and the circuit needs more process and more precise. So it needs to fabricate the mechanical structure and the circuit in different process. Finally, MEMS mechanical structures and all signal conditioning circuitry will be combined onto a monolithic IC [6,7] This In this thesis, we will design the capacitance detecting circuit for the micro gyroscope with the model of 'TSMC 0.35um , 2P4M , Mixed-mode, 3.3, 5V.' in order to realize it by ''TSMC 0.35um , 2P4M' process.



1.3 Research Orientation

Capacitance sensing circuit [8-10] can solve many different types of sensing and measurement problems especially for micro sensor. They are used for rotary and linear position encoding, liquid level sensing, touch sensing, sensitive micrometers, light switches and micro-gyroscope. With the MEMS process develop rapidly, more and more type of micro-sensor are presented. The micro-sensor usually uses the structure gap changes to response the sensing element and so do the micro-vibrating ring gyroscope.

The micro-vibrating ring gyroscope structure [4,5] illustrated as Fig 1.1 and Fig 1.2 had been well constructed. The natural frequency of the micro-gyroscope

is 20kHz. The constant capacity is 0.1pf and the mismatch capacity is 0.01pf.

First, we will introduce several circuits for capacitance sensing and their characteristics. The synchronous detection circuit is adopted as our circuit structure and then we will canvass it. Finally we will present how to design this circuit and simulation.

Chapter 2 Capacitance Sensing Techniques

In this chapter we will introduce the capacitance sensing techniques. It contains the capacitance sensing method, the sensing resolution, and the nonidealities in sensing circuit. Each circuit has its own advantages but also disadvantages. We need to trade off and select a circuit to use.

2.1 Capacitance Sensing Method

This section presents three type of capacitance sensing circuit and their basics circuit principle. Each of one has its advantages and also drawbacks.

2.1.1 Direct DC

Direct DC [11] is the simplest circuit. With a very high impedance amplifiers, capacitance changes can be measured as DC voltage differences, simply by charging the capacitor to be measured and connecting it to the amplifier input. As the charge is then nearly constant the capacitor voltage will vary as the reciprocal of capacitance or directly with spacing by the relationship $Q=CV$. The time constant RC where R is the amplifier input resistance and C the capacitance being measured must be greater then the time measurement period so as not to introduce a low frequency loss; thus an electrometer-type amplifier with input currents in the femtoampere region is often needed. Electret microphones use this method with a junction FET for an amplifier; the resistance to ground which is needed to keep the capacitor voltage from drifting outside the amplifier's linear range is contributed by the FET's input leakage

currents.

For direct DC circuits using an operational amplifier an input resistor of very high value is needed, or a bootstrap circuit can be used to increase the AC input resistance, as shown in Fig. 2.1.

2.1.2 Synchronous Detection Circuit

The concept of synchronous detection circuit [12] is to reduce the impedance of the sensing capacitance by modulating it by a high frequency voltage. Fig. 2.2 shows an implementation of the synchronous detection circuit. C is the initial capacitance, V_S is the high frequency sinusoidal voltage source, and C_P is the parasitic capacitance of the Operational Amplifier. In this implementation, two out-of-phase high frequency sensing signals are applied to the sense capacitors. If the sense capacitors differ, an amount of charge proportional to the mismatch and the amplitude of the sensing voltage will be integrated by the charge integrator, thus resulting in an output voltage which is a function of the mismatch of the sense capacitors. The high frequency output voltage is then amplified and demodulated down to baseband by the synchronous demodulator. Next, the low-pass filter removes the offset and the *1/f* noise of the electronics which is modulated up to high frequency by the demodulator. This offset and 1/f noise removal technique is commonly known as chopper stabilization. To set the DC voltage level at the amplifier input, which is a high impedance node, a large resistor is connected between the amplifier input and the output node. Sensitivities to parasitic capacitance is eliminated by the virtual ground condition at the amplifier input.

The signal transfer function of the synchronous detection circuit in Fig. 2.2 is

$$V_{out} = -\frac{\Delta C}{C_I} V_S \tag{2.1}$$

where V_S is the amplitude of the sensing voltage. The output noise of this circuit, assuming that noise from the front-end amplifier and the DC-setting resistor dominates, is

$$\frac{\overline{V_{on}^2}}{\Delta f} = \frac{\overline{V_n^2}}{\Delta f}\left(\frac{2C + C_I + C_p + C_{IP}}{C_I}\right)^2 \tag{2.2}$$

where $\overline{V_n^2} / \Delta f$ is the input-referred spectral density of the amplifier thermal noise and C_{IP} is the amplifier input capacitance.

2.1.3 Switched-Capacitor Sensing Circuit

In the switched-capacitor circuits [13,14], the DC-setting resistor is replaced by capacitors and switches. This results in smaller die area and much better matching. In switched-capacitor sensing circuit, the sense capacitor is reset to the ground or a reference level in each cycle, thus eliminating the need for a large resistor to set the DC level. The feedback feedthrough is eliminated by allocating a separate phase for the feedback operation. Furthermore, switched-capacitor sensing circuit offers more flexibility in the system integration because of the ability to allocate separate phases for different operation such as reset, sensing, feedback, and comparison.

Fig. 2.3 shows a typical implementation of the switched-capacitor sensing circuit. This circuit is identical to a switched-capacitor gain stage, except that the

input is capacitance variation instead of a voltage variation. During the reset phase, the sensed capacitor, the integrating capacitor, and the amplifier are reset to ground or a reference level. During the sensing phase, the sensing voltage $\pm V_S$ are applied to the two fixed electrodes of the sensing capacitors. An amount of charge proportional to the mismatch due to acceleration in the sensing capacitors $+C_S$ and $-C_S$ and the sensing voltage is integrated on C_I and produces an output voltage, which is then sampled by C_L. The transfer function of this this switched-capacitor sensing circuit is

$$V_O = \frac{\Delta C}{C_I} V_S \tag{2.3}$$

which is identical to that of the synchronous detection circuits.

In micromachined applications, however, the size of the sense capacitance is typically limited by the technology to a few hundred femtofarads, thus the switched-capacitor circuit suffers from a large sampling *(kT/C)* noise. The output-referred spectral density of the kT/C noise is

$$\frac{\overline{V_{kT/C}^2}}{\Delta f} = \frac{kT}{C_T}\frac{1}{f_s}\left(\frac{C_T}{C_I}\right)^2 \tag{2.4}$$

Where $C_T=2C+C_I+C_P+C_{IP}$ is the total capacitance at the amplifier summing node. And the spectral density of the amplifier noise sampled by the load capacitance *CL* is

$$\frac{\overline{V_{opamp}^2}}{\Delta f} = \left(\frac{C_T}{C_I}\right)^2 \frac{\overline{V_n^2} f_u \pi}{2 f_s \Delta f} \tag{2.5}$$

where $\overline{V_n^2}/\Delta f$ is the input-referred spectral density of the amplifier thermal

noise and f_u is the closed-loop bandwidth of the amplifier.

2.2 Sensing Resolution

Fundamentally, the resolution of a position sensing circuit is limited by the thermal noise of the sensing electronics or Brownian motion of the sense element. In practice, nonidealities often prevent the sensing circuit from achieving the fundamental resolution. Nevertheless, the fundamental sensing resolution provides us a benchmark to compare the achieved resolution to the fundamental limit and to compare the merits of different sensing techniques.

The sensing resolution is defined as the capacitance variation that results in an output signal which has a signal-to-noise ratio of one,

$$\sqrt{\overline{V_{no}^2}} = V_o = \frac{dV_o}{dC}\Delta C_{\min} = \frac{dV_o}{dC}\frac{dC}{dx}\Delta x_{\min} \tag{2.6}$$

Where $\sqrt{\overline{V_{no}^2}}$ is the output noise voltage of the sensing circuit. Rearranging this equation in terms of capacitance resolution and the position resolution,

$$\Delta C_{\min} = \frac{\sqrt{\overline{V_{no}^2}}}{\frac{dV_o}{dC}} \tag{2.7}$$

and

$$\Delta x_{\min} = \frac{\Delta C_{\min}}{\frac{dC}{dx}} = \frac{\sqrt{\overline{V_{no}^2}}}{\frac{dV_o}{dC}\frac{dC}{dx}} \tag{2.8}$$

Since this research focuses on the design of the sensing circuit, we will assume that the contribution from Brownian motion is negligible compared to the thermal noise of the sensing electronics. For the synchronous detection

circuit described in Section 2.1.2, the capacitance resolution can be calculated from the signal and the noise transfer functions in equation (2.1) and equation (2.2), assuming a large R to minimize its noise contribution, as

$$\sqrt{\frac{\overline{\Delta C_{\min}}}{\Delta f}} = \left(2C + C_I + C_P + C_{IP}\right)\sqrt{\frac{\overline{V_n^2}}{\Delta f}}\frac{1}{V_s} \tag{2.9}$$

For the switched-capacitor sensing circuit described in Section 2.1.3, the resolution can be calculated from the signal and noise transfer functions in equation (2.3) to equation (2.5) as

$$\sqrt{\frac{\overline{\Delta C_{\min}}}{\Delta f}} = \frac{1}{V_s}\sqrt{\left(\frac{kTC_T}{f_s}\right)_{\frac{kT}{C}} + \left(\frac{C_T^2\overline{V_n^2}f_u\frac{\pi}{2}}{f_s}\right)_{OpAmp}} \tag{2.10}$$

where the first term is due to the kT/C noise of switch S3, the second term is due to the amplifier thermal noise, and C_T is equal to $2C+C_I+C_P+C_{IP}$. The kT/C noise term, which is typically the dominant thermal noise source in micromachined applications, can be eliminated by correlated double sampling (CDS). Taking into account the kT/C noise cancellation and the factor-of-two amplifier noise increase due to double sampling, equation (2.10) becomes

$$\sqrt{\frac{\overline{\Delta C_{\min}}}{\Delta f}} = \frac{1}{V_s}\sqrt{\left(\frac{C_T^2\overline{V_n^2}f_u\frac{\pi}{2}}{f_s}\right)_{OpAmp}} \tag{2.11}$$

Comparing the sensing resolution of switched-capacitor sensing circuits to that of the synchronous detection circuits yields,

$$\frac{\Delta C_{\min,swcap}}{\Delta C_{\min,sync}} = \sqrt{\frac{\pi f_u}{f_s}} \tag{2.12}$$

This ratio is typically in the order of three to four due to the noise folding

and the double sampling, thus suggesting that the fundamental resolution of switched-capacitor sensing circuits is three to four times lower than that of synchronous detection circuits.

To conclude, the switched-capacitor sensing scheme eliminates the need for DC-setting resistor (R) and offers flexibility in system integration through multi-phase operations. On other hand, it has a lower fundamental resolution and requires more complicated clocking circuit.

2.3 Nonidealities in Sensing Circuit

Compared to the synchronous detection scheme, the switched-capacitor sensing scheme introduces switch charge injection and *kT/C* noise due to switching operations. These errors combining with the amplifier offset and *1/f* noise decrease the sensing resolution. In this section, we will investigate these errors and available techniques to eliminate them.

2.3.1 Amplifier Offset

In MOS amplifiers, offsets are caused by mismatches in the device dimension and the threshold voltage, and can be reduced by using large devices and common-centroid layout. The offset in a carefully designed MOS amplifier is in the range of a few millivoltages and typically overwhelm the output signal of the sensing circuit.

2.3.2 Amplifier 1/f noise

For a MOS transistor biased in the saturation region, the *1/f* noise is inversely proportional to the frequency and the gate capacitance of the device,

$$\frac{\overline{V_{1/f}^2}}{\Delta f} = \frac{K_f}{WLC_{ox} f} \tag{2.13}$$

Depending on the process, a typical value of K_f for NMOS can be greater than for PMOS by a factor of two or more. Typically, *1/f* noise is reduced by using PMOS devices or large devices. These techniques, however, do not work well in micromachined applications because mechanical signals concentrate in the low frequency range and often extend down to DC, thus requiring extremely large devices to suppress the *1/f* noise. Since *1/f* noise is essentially a slowly varying amplifier offset, offset-cancellation techniques can partially remove the *1/f* noise.

2.3.3 *kT/C* Noise

In switched-capacitor sensing circuits, *kT/C* noise is often larger than the amplifier thermal noise. Typically, *kT/C* noise can be reduced by increasing the size of the sampling capacitors. This, however, is not feasible in micromachined applications because the sense capacitance is usually limited to hundreds of femtofarads by the size restriction of the sense element. The other alternative to reducing the *kT/C* noise is to increase the sampling frequency. According to equation (2.4), the sampling frequency must be increased by 10 times in order to reduce the *kT/C* noise by 10dB. Such a large increase in the sampling frequency is not desirable because of increasing complexities in system design and high power consumption.

2.3.4 Amplifier Thermal Noise (for synchronous detection circuit)

The optimization of the amplifier thermal noise is based on the condition that is the Sense capacitance C and the parasitic capacitance C_P are considered

fixed variables since they are primarily determined by the fabrication process of the sense element. Fig. 2.2 shows a synchronous detection circuit. The input-referred thermal noise of the amplifier can be written as

$$\frac{\overline{V_n^2}}{\Delta f} = \frac{8kT}{3g_m} n_f \tag{2.14}$$

where $8kT/3g_m$ is the thermal noise of the input transistor and n_f is the ratio of the total amplifier noise to the input transistor noise. In a properly designed amplifier, the input devices are the main noise contributors; hence, n_f is approximately two due to the input source-coupled pair.

The output-referred noise spectral density is

$$\frac{\overline{V_{on}^2}}{\Delta f} = \frac{\overline{V_n^2}}{\Delta f}\left(\frac{2C + C_I + C_P + C_{IP}}{C_I}\right)^2 \tag{2.15}$$

where C_{IP} is the input capacitance of the amplifier. With C_S, C_I, and C_P fixed as stated in the assumptions, the charge integrator output noise becomes a function of only the amplifier input capacitance and the input-referred thermal noise of the amplifier, $\overline{V_n^2}$. The thermal noise, according to equation (2.14), can be reduced by increasing the transconductance of the input devices. Increasing the transconductance, however, requires increasing either the saturation voltage of the input devices, which in practice is limited by the supply voltage and the output swing, or enlarging the input devices . Larger input devices increase the amplifier input capacitance which results in the reduction in the feedback factor. Smaller feedback factor means high noise gain from the amplifier input to the output. For amplifiers with small input devices, the increase in transconductance dominates and the output-referred noise is decreased. For amplifiers with large

input devices, the reduction in feedback factor dominates and output-referred noise is increased.

The optimal size for the input devices can be calculated by the following steps. For a MOS transistor in the saturation region, the transconductance of the device can be related to the cutoff frequency f_T, the frequency where the magnitude of the common-source current gain falls to unity, as

$$g_m = 2\pi f_T C_{GS} \tag{2.16}$$

where C_{GS} is the gate capacitance of the device and is equal to the amplifier input capacitance C_{IP}. Substituting equation (2.16) into equation (2.14) and equation (2.14) into equation (2.15) yields

$$\frac{\overline{V_{on}^2}}{\Delta f} = \frac{(2C + C_I + C_P + C_{IP})^2}{C_{IP} C_I^2} \frac{4kTn_f}{3\pi f_T} \tag{2.17}$$

To find the optimal amplifier size, equation (2.17) is differentiated with respect to C_{IP}

$$C_{IP,opt} = 2C + C_I + C_P \tag{2.18}$$

This result states that, for a given saturation voltage, the amplifier input devices should have a gate capacitance equal to the summation of all other capacitances at the summing node. Substituting the optimal input device size and the amplifier noise into the capacitance sensing resolution given in equation (2.9),

$$\frac{\overline{\Delta C_{\min}}}{\Delta f} = \frac{4}{V_s^2}\left(2C + C_I + C_P\right)\frac{4kTn_f}{3\pi f_T} \tag{2.20}$$

This result suggests that small parasitic capacitance C_P, small integrating capacitor C_I, and short channel devices with high f_T improve the optimal capacitance resolution of the sensing circuit. Even though this equation implies

that small sense capacitance *C* improves the capacitance resolution.

2.4 Conclusion

In this chapter we discuss several circuits for capacitance detection and several nonidealities in those circuit.

The Direct DC circuit can not cancel the parasitic capacitance but it has simplest structure.

The synchronous detection circuit can cancel the parasitic capacitance, offset voltage *1/f* noise, and it doesn't have the *kT/C* noise because of it doesn't have switch. But it still has two drawbacks. The first is it needs a large resistor which large resistors requires large die area and has large parasitic capacitance which can lower the resolution, slow down the circuit, and add another pole to the amplifier frequency response. Second, synchronous detection is not suitable for applications which involve feedback loops because the low-pass filter adds phase delay to the loop transfer function.

The Switched-capacitor circuits replace resistors by capacitors and switches. This results in smaller die area and much better matching and tracking but it needs complicated clock circuit.

Finally, we select the synchronous detection circuit because of its simple structure and can cancel some nonidealities.

Chapter 3 Synchronous Detection Circuit Analysis

In this chapter we will analysis the synchronous detection circuit and introduce how it works. And then we will design a classical two-stage CMOS operational amplifiers for this circuit.

3.1 Signal Transfer function

The synchronous detection circuit will be analyzed for two case, differential capacitor sensing and single capacitor sensing circuit in this section.

3.1.1 Differential Capacitor Sensing Circuit

Fig. 3.1 shows an implementation of the synchronous detection circuit for differential capacitor. The feedback resistor R offers the DC path. The circuit can be expressed by these steps. At the inverter input node,

$$i_{total} = i_1 + i_2 + i_3 + i_4 \tag{3.1}$$

and each current can be expressed as

$$+V_s - V = \frac{1}{s\left(C + \frac{1}{2}\Delta C\right)} i_{total} \tag{3.2}$$

$$V - (-V_s) = \frac{1}{s\left(C - \frac{1}{2}\Delta C\right)} i_1 \tag{3.3}$$

$$V = \frac{1}{sC_P} i_2 \tag{3.4}$$

$$V - V_o = \frac{1}{sC_I} i_3 \tag{3.5}$$

$$V - V_o = i_4 R \tag{3.6}$$

Because of the feedback path, the inverter input node of Op-Amp can be assumed as virtual ground. When the inverter input node can be assumed virtual ground ($V=0$) because of the ideal Op-Amp, taking the equation (3.2), equation (3.3), equation (3.4), equation (3.5), equation (3.6) into equation (3.1) and then the transfer function can be expression as

$$V_s s\left(C + \frac{1}{2}\Delta C\right) = V_s s\left(C - \frac{1}{2}\Delta C\right) - V_o \frac{sRC_I + 1}{R} \tag{3.7}$$

$$V_o = -\frac{\Delta C s}{sC_I + 1/R} V_S \tag{3.8}$$

This is the transfer function of this circuit, and the parasitic capacitance C_P was reduced due to the inverter node was assumed as virtual ground. Fig. 3.2 shows the magnitude bode plot of this transfer function. This transfer function have one zero at 0 and one pole at $1/RC_I$, and it works as a high pass transfer function which has a constant gain $\Delta C / C_I$ after the input signal frequency is higher then $1/RC_I$. Then the transfer function of this circuit is

$$V_o = -\frac{\Delta C}{C_I} V_s \tag{3.9}$$

The resistor R usually has a large value in the range of mega-ohms to ensure low current noise and to avoid a null in the frequency response due to charge leakage. The large resistor R can also decrease the value of $1/RC_I$ and move the pole location more closed to image axis. Since the pole more closed to

the image axis, the more bandwidth of this circuit is.

3.1.2 Single Capacitor Sensing Circuit

Fig. 3.3 shows an implementation of the synchronous detection circuit for single capacitor. It almost the same as the circuit we presented in section 3.1.1. The different between two circuits is that only a capacitor C_S ($C_S = C + \Delta C$) and a carrier voltage V_S at the input node. Not every MEMS structure has differential capacitor for sensing. We can analysis this circuit as the same way in section 3.1.1. First, the total current is

$$i_{total} = i_1 + i_2 + i_3 \tag{3.10}$$

and each current can be expressed as

$$V_s - V = \frac{1}{s(C + \Delta C)} i_{total} \tag{3.11}$$

$$V = \frac{1}{sC_P} i_1 \tag{3.12}$$

$$V - V_o = \frac{1}{sC_I} i_2 \tag{3.13}$$

$$V - V_o = i_3 R \tag{3.14}$$

The transfer function of this circuit can be write as

$$V_o = -\frac{C + \Delta C}{C_I} V_s \tag{3.15}$$

About the C_I and R value is the same as the section 3.1.1.

The advantage of single capacitor sensing circuit is that it doesn't need

another invert carrier voltage $-V_S$ since this is not easy to have two signals that have -180° phase different. The defect is that the output voltage not only response the variation capacitor ΔC but also the constant capacitor C. When the variation capacitor is very smaller than the constant capacitor, the output voltage may not response the various capacitor. And this is influenced by the times of C_I and C.

3.1.3 Summary

The synchronous detection circuit can be realized for two type capacitance sensing. The general form of modulated signal is

$$V_O = -\frac{C_S}{C_I} V_S \tag{3.16}$$

And

$C_S = \Delta C$ for differential capacitor (3.17)

$C_S = C + \Delta C$ for single capacitor (3.18)

To compare those two type sensing circuit, Tab. 3.1 shows the result.

3.2 The Modulation-Demodulation Method

The synchronous detection circuit can cancel the *1/f* noise and operational amplifier offset voltage because of noises in low frequency band are modulated up to high frequency band and be removed by lowpass filter. In this section, we will explain how it works.

From section 3.1.1, we got the transfer function of the synchronous detection circuit. The transfer function from equation (3.9) is

$$V_o = -\frac{\Delta C}{C_I} V_s \tag{3.19}$$

ΔC is the mismatch of the two various capacitances. The ΔC can be assumed as a sinusoid function with a constant frequency, and V_S is also a sinusoid with a thirty times or above frequency than the ΔC. Then the ΔC and V_s can be wrote down as

$$\Delta C = A\sin \omega t \tag{3.20}$$

$$V_s = A_c \sin pt \quad (\omega >> p) \tag{3.21}$$

Taking equation (3.20), equation (3.21) into equation (3.19), then

$$V_o = \frac{AA_c}{2C_I}\left(\cos(\omega - p)t - \cos(\omega + p)t\right) \tag{3.22}$$

Where V_o is the sum of two cosine. Since $\omega >> p$, both $\omega - p$ and $\omega + p$ are in high frequency band. It is modulation that we say that modulated up the low frequency signal to high frequency. The high frequency (ω) signal is called "carrier". Fig. 3.4 shows the modulation process. Fig. 3.5 shows the spectrum of the modulated and demodulated signal.

Demodulation is mixed the original carrier to the modulated signal, the formula can be expressed as

$$V_{dem} = V_o V_s (3.20) \tag{3.23}$$

$$V_{dem} = \frac{AA_c}{2C_I}\left(\cos(\omega - p)t - \cos(\omega + p)t\right) A_c \sin \omega t \tag{3.24}$$

$$V_{dem} = \frac{AA_c^2}{4C_I}\left(\sin(2\omega - p)t - \sin(2\omega + p)t\right) + \frac{AA_c^2}{2C_I}\sin pt \tag{3.25}$$

Where V_{dem} is the signal be demodulated down. After the demodulation, V_{dem} contains three frequencies, one of them is the original frequency (p) of ΔC and the others are very high frequency than the ΔC. When V_{dem} pass through the lowpass filter, the high frequencies elements will be removed.

The *1/f* noise and offset voltage can partially remove by shifting them to high frequency. The *1/f* noise is a noise has magnitude inverse proportion to frequency. The offset voltage can be consider as the V_o adds a DC bias, and can be consider as a constant in the formula. This constant will be modulated up to high frequency during demodulation and thus it will be remove when V_{dem} pass through lowpass filter like the *1/f* noise be removed. Fig. 3.6 illustrates the process of demodulation.

3.3 Design concepts of two-stage operational amplifiers

The Fig. 3.7 shows a classical two-stage CMOS operational amplifier [15]. It contains two stages. The first stage consists of a differential amplifier converting the differential input voltage to differential currents. This differential current is applied to a current mirror load recovering the differential voltage. The second stage is a common source converting the second stage input voltage to current. This transistor is loaded by a current-sink load, which converts the current to voltage at the output. The C_C capacitance is a Miller capacitor. This is called 'Miller compensation method', which is applied by connecting a capacitor from the out put to the input of the second stage.

3.3.1 Small signal frequency response Model simplified

The small-signal model of two-stage operational amplifiers is illustrated as Fig. 3.8 where,

$$g_{ma} = g_{m1} = g_{m2} \quad , \quad R_a = r_{ds2} \| r_{ds4} \quad , \quad C_a \simeq C_{gs6} \tag{3.26}$$

and

$$g_{mb} = g_{m6} \quad , \quad R_b = r_{ds6} \| r_{ds7} \quad , \quad C_b \simeq C_L \tag{3.27}$$

By approximate calculation, the transfer function is as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{A_o\left[1 - s\left(C_C / g_{mb}\right)\right]}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)} \tag{3.28}$$

where

$$A_o = g_{ma} g_{mb} R_a R_b \tag{3.29}$$

$$p_1 \simeq \frac{-1}{g_{mb} R_a R_b C_C} \tag{3.30}$$

and

$$p_2 \simeq \frac{-g_{mb} C_C}{C_a C_b + C_b C_C + C_a C_C} \tag{3.31}$$

If C_b is much greater than C_a and C_C is greater than C_a, then equation (3.31) can be approximated by

$$p_2 \simeq \frac{-g_{mb}}{C_b} \tag{3.32}$$

It has a zero at right half-plane (RHP) as

$$z_1 = \frac{g_{mb}}{Cc} \tag{3.33}$$

The RHZ zero increase the phase shift but increases the magnitude.

3.3.2 Characteristics of two-stage operational amplifiers

Now, we will list some specifications In the deriving the design equation [15,16], we assume the transistor are long channel and define $S_i = (W/L)_i$.

(a.) Open Loop Gain

Assuming that M1 and M2 aer identical and that M3 and M4 are identical, the gain can be shown to be

$$A_o = g_{ma} g_{mb} R_a R_b \tag{3.34}$$

(b.) Systematic Input Offset Voltage

In order to reduce the input offset voltage, the drain voltage of M3 and M4 must be equal. This condition occurs when

$$\frac{S_3}{S_6} = \frac{S_4}{S_6} = \frac{S_5}{2S_7} \tag{3.35}$$

(c.) The Unit Gain Bandwidth *(GB)*

The Unit Gain Bandwidth is define as the frequency when the magnitude of the open loop OP Amp frequency response cross the 0 db.

$$GB = \frac{g_{m1}}{C_C} \tag{3.36}$$

(d.) Common mode Input Range *(ICMR)*

The common mode input voltage is upper-bounded by M3 and M4 entering the linear region and lower-bounded by M5 entering the linear region.

$$ICMR_{\max} = V_{dd} - \sqrt{\frac{I_5}{\beta_3}} - \left|V_{TO3}\right|_{(\max)} + V_{T1(\min)} \tag{3.37}$$

$$ICMR_{\min} = V_{ss} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1(\max)} + V_{DS5(\max)} \tag{3.38}$$

where $V_{DS(sat)} = \sqrt{\frac{2I_{DS}}{\beta}}$.

(e.) Slew Rate *(SR)*

Slew rate is defined as the maximum output-voltage rate , either positive or negative.

$$SR = \frac{I_5}{C_C} \tag{3.39}$$

(f.) Phase margin *(PM)*

If we assumed the PM we required is 60° and the zero is ten times higher than *GB*, then the second pole must be placed at least 2.2 times higher than *GB*. Finally, we can get the constrain as

$$C_C > 0.22C_L \tag{3.40}$$

$$g_{m6} \geq 10 g_{m1} \tag{3.41}$$

Using those constrain of above, we can get a classical two stage operational amplifiers which have some specifications we wish.

3.4 Conclusion

This chapter has presented the analysis and characteristic considerations of synchronous detection circuit and two-stage operational amplifiers. The design, simulation and experiment result will be presented in the following chapter.

Chapter 4 Simulation And Experiment

In this chapter, some simulations and experimental results about the operational amplifier and the synchronous detection circuit will be presented. Because of the MEMS structure and the sensing circuit are not fabricated in the same process, there will exist a parasitic capacitance at the wire bonding pad. In the chapter 3, it was found that the synchronous detection circuit can cancel the parasitic capacitor and that's the reason we select it as our sensing circuit.

4.1 Design and Simulation of The Operational Amplifier

In the section 3.3, a basic two-stage operational amplifier has been introduced. The operational amplifier plays an important role in the synchronous detection circuit. Simulation will be the subject of the following section.

4.1.1 Design of the Operational Amplifier

An ideal operational amplifier with a single-ended output has a differential input, infinite voltage gain, infinite input resistance, and zero output resistance. To base on these characteristics and the previous section discussion, some specifications are listed as Tab. 4.1 .

The operational amplifier will be fabricated with TSMC 0.35um , 2P4M , Mixed-mode, 3.3, 5V process and simulated by HSpice with the model which provided by TSMC. Fig. 4.1 is the schematic view of the operational amplifier. It consists an output stage which can decrease output resistor.

4.1.2 Simulation Result

Fig. 4.2 shows the frequency response of the operational amplifier. Tab. 4.2 lists the small-signal transfer characteristics of the operational amplifier. The voltage gain and phase margin are almost as our expectation. Although there are many equations to help us designing the MOS W/L ratio, it still needs to tune up some ratio in order to match the design specifications.

Fig. 4.3 is the layout view of the operational amplifier. It is better to make layout symmetrical.

Since the CMOS process has several lays to stack up a full circuit, there will have parasitic capacitors and resisters. Those will influence the ideal circuit performance. TSMC also provides the model of those parasitic capacitances and resisters. Post-simulation is a simulation that includes the effect of parasitic capacitors and resisters. It makes the simulation result more similar to the real.

Fig. 4.4 is the frequency response of the operational amplifier by post-simulation. Tab4.3 lists the small-signal transfer characteristics of the operational amplifier by post-simulation. Compare with the ideal simulation, voltage gain, input resister, bandwidth, and unit gain bandwidth are decreased.

4.2 Design and Simulation of The Synchronous Detection Circuit

In the section 3.1, two types of the Synchronous Detection Circuit had been presented. The C_I and R play an important role in both circuits. Equation (3.15) and equation (3.9) are the transfer functions. From equation (3.8), because

the transfer function is a high pass transfer function with a pole at $1/RC_I$, the frequency of modulated signal needs to be higher than the corner frequency in order to have a constant gain.

4.2.1 Designing The Synchronous Detection Circuit

From the section 3.1, the modulated signal can be expressed as

$$V_O = -\frac{C_S}{C_I}V_S \tag{4.1}$$

And

$$C_S = C + \Delta C \qquad \text{for single capacitor} \tag{4.2}$$

$$C_S = \Delta C \qquad \text{for differential capacitor} \tag{4.3}$$

The ΔC varies in 20KHz, so the carrier voltage V_S can be determined as 600KHz which is 300 times to ΔC. The frequency of modulated signals are 580KHz and 620KHz. The corner frequency $1/RC_I$ must be lower than 580KHz in order to keeps constant gain. To base on those constrains, we can determine the R and C_I.

4.2.2 Simulation Results

In single capacitor sensing type, we assume

$$C_S = C + \Delta C = 0.09,\ 0.1,\ 0.11\ pf \tag{4.4}$$

$$V_S = 1.5\sin(2\pi \times 600K)\ V \tag{4.5}$$

$$C_I = 1.5\,pf \tag{4.6}$$

$$R = 2M\Omega \tag{4.7}$$

Fig. 4.5 shows the frequency response of this circuit. The corner frequency is 53KHz and DC gain is -23.5dB when $C_S = 0.1pf$. The simulation result is the same as our theorem that presented in previous. The output signal wave form is shown in Fig. 4.6. According to the equation (4.1), the modulated signal can be determined as 0.09V, 0.1V, 0.11V when the Cs is 0.09pf, 0.1pf, 0.11pf. This result is also match the simulation result. While the capacitor is variously as

$$C_S = 0.1 + 0.01\sin\left(2\pi \times 20K\right) \tag{4.8}$$

The simulation as Fig. 4.7 indicates the modulated signal contains a low frequency 20KHz and the carrier with 600KHz.

In differential capacitor sensing type, we assume

$$C_S = 0.1 \pm \frac{1}{2}0.01\sin\left(2\pi \times 20KHz\right)\ pf \tag{4.9}$$

$$\pm V_S = 6\sin(2\pi \times 600K)\ V \tag{4.10}$$

$$C_I = 1.5pf \tag{4.11}$$

$$R = 2M\Omega \tag{4.12}$$

The corner frequency is the same as previous but the DC gain is -43dB when the $\Delta C = 0.01\ pf$ that different with previous simulation. Fig. 4.8 shows the frequency response of this circuit, it indicates the same result as the theorem.

Fig. 4.9 shows the modulated signal for the different capacitors sensing circuit. Because the output voltage only reflect the various capacitor ΔC. The amplitude of output voltage 0.05V is more than the theorem 0.04V.

4.3 Experimental result

In the previous section, design and simulation results had been presented. The circuit that shows in Fig. 4.10 is realized with TSMC 0.35μm 2P4M process. Some experiments are presented in the following section as a feasibility study. Because it's not easy to construct differential capacitors, the experiment takes the single capacitor sensing circuit as basic scheme.

4.3.1 Single Capacitor measurement

The measuring circuit scheme is indicated as Fig. 4.11. The sensing target capacitor is constructed by several 1p capacitors in series. The carrier voltage V_S is a fixed frequency signal. We turned up V_S amplitude to get the max output amplitude. The result is shown in Tab. 4.4. The result indicates that sensing capacitor contains some parasitic capacitor which is due to the series circuit. Fig. 4.12 shows the carrier voltage and modulated output signal wave form.

It can be plot a figure as Fig 4.13 that contains ideal capacitors and estimation capacitors. It indicates that both ideal capacitor and estimated capacitor have linear relationship although they are not equal.

4.3.2 Sweep Capacitor measurement

The major difference between sweep capacitor measurement and single capacitor measurement is that the carrier voltage V_S is fixed. In chapter 1, the capacitor we want to sense is 0.1±0.01pf. Moreover the basic theorem is the

modulation, so that the V_S is fixed in this experiment.

Fig. 4.14 is the scheme of sensing circuit. At the part of sensing capacitor, it consists of twelve 1pf capacitors in series and a switch. The switch turns the value of capacitors in series and the value of the sensing capacitor are 0.1+0.025pf, 0.1+0.011pf, 0.1pf, 0.1-0.01pf and 0.1-0.017pf. The measurement result shows in Tab. 4.5. The estimated capacitor is bigger then previous measurement. This might be due to the metal switch contains more parasitic capacitor. Fig. 4.15 shows the signal wave form and Fig. 4.16 shows the relationship between ideal capacitor various and estimated capacitor various (compare with 0.1pf). The figure illustrates the linearity between various capacitor and estimated capacitor.

4.4 Summary

In the measurement, the test plant is several capacitors in series. In the connected node, there exists a parasitic capacitor in each node which is typically 0.01pf. The more capacitors in series the worse measured result especially.

The results of design, simulation and measurement had been presented in this chapter. The result of simulation and measurement can demonstrate the feasibility of synchronous detection circuit. There is a serious drawback found during measuring experiment. The circuit fault easily when the sensing capacitor had been changed. This might be because the circuit suffers from the ESD when measuring experiment. This circuit doesn’t contain any protection. In order to increase reliability of the sensing circuit, protection circuits such as ESD and over current are indeed needed.

Chapter 5 Conclusion

In thesis, the major purpose is presented a capacitance sensing circuit. Chapter 2 illustrates three types of capacitance sensing techniques and two of them are discussed in chapter 3. The switched-capacitor sensing circuit is more suitable for closed loop application but circuit scheme is more complex then synchronous detection circuit. Moreover, a compensated circuit CDS which needs three phases clock is required to reduce several noises in the switched-capacitor sensing circuit.

The synchronous detection circuit has less complex structure and that is why it suffers from less noises. But it needs a resistor to provide a DC path and the resistor is very large.

The analysis, design, simulation and measurement of the synchronous detection circuit are presented in chapter 3 and chapter 4. From the frequency response simulation, the operation range of synchronous detection circuit is 300KHz~10MHz. The R and C_I are the key in this circuit. They determine the operation range and magnitude of output signal. From the experimental result, the synchronous detection circuit is feasible to measure capacitor.

Reference

[1] Bernhard E. Boser and Roger T. Howe, “Surfacer Micromachined Accelerometers”, *IEEE J. Solid-State Circuits*, Vol. 31, No. 3, pp. 366-375, Mar. 1996.

[2] K. Kasten, N. Kordas, H. Kappert, and W. Mokwa, “ Capactitive pressure sensor with monolithically integrated CMOS readout circuit for high temperature applications”, *Sensor and Actuators*, A 97-98, pp. 83-87, 2002.

[3] F. Ayazi and K. Najafi, “A HARPSS Polysilicon Vibrating Ring Gyroscope”, *Journal of Microelectromechanical Systems*, Vol. 10, pp. 169-179, 2001.

[4] Jui-Hong Weng, Wei-Hua Chieng, and Jenn-Min Lai, “Structural fabrication of a ring-type motion sensor”, *Journal of Micromechanic And Microengineering*, Vol. 14, pp. 710-716, 2004.

[5] Jui-Hong Weng, Wei-Hua Chieng, and Jenn-Min Lai, “Structural design and analysis of micromachined ring-type vibrating sensor of both yaw rate and linear acceleration,” *Sensor and Actuators*, A 117, pp. 230-240, 2005.

[6] C. Lu, M. Lemkin, and B. E. Boser, “A monolithic surface micromachined accelerometer with digital output”, *IEEE J. Solid-State Circuits*, Vol. 30, No. 12, pp. 1367-1373, Dec. 1995.

[7] Analog Devices, “ADXL50-Monolithic Accelerometer with Signal Condition”, Datasheet, 1993.

[8] B. Stefanelli, Jean-Paul Bardyn, A. Kaiser, and D. Billet, “ A Very Low-Noise CMOS Preamplifier for Capacitive Sensors,” *IEEE J. Solid-State Circuits*, Vol. 28, No. 9, pp. 971-978, Sep. 1993.

[9] S. Tedja, Jan Van der Spiegel, and Hugh H. Williams, “ A CMOS Low-Noise

and Low-Power Charge Sampling Integrated Circuit for Capacitive Detector/Sensor Interfaces," *IEEE J. Solid-State Circuits*, Vol. 30, No. 2, pp. 110-119, Feb. 1995.

[10]Bernhard E. Boser, " Electronic Interfaces for MEMS", 1996.

[11]Larry K. Baxter, "Capacitive Sensors Design and Applications," *the Sponsorship of the IEEE Industrial Electronics Society.*

[12]N. Womgkomet, "Position Sensing for Electrostatic Micropositioners," *Ph. D. Dissertation*, Univ. of California, Berkeley, 1998.

[13]R. C. Yen and P. R. Gray. "A MOS Switched-Capacitor Instrumentation Amplifier," *IEEE J. of Solid-State Circuits*, Vol. 17, No. 6, pp. 1008-1013, December 1982.

[14]Bernhard E. Boser, "Capacitive Sensing Circuits," 1996.

[15]M. Hershenson, S. Boyd, and T. H. Lee, "CMOS operational amplifier design and optimization via geometric programming," *Proc. 1st Int. Workshop Design Mixed-Mode Integrated Circuits Applicat.*, Cancun, Mexico, pp. 15-18, 1997.

[16]E. Allen, R. Holberg, "CMOS Analog Circuit Design,"2nd , *New York Oxford, Oxford university*, 2002.

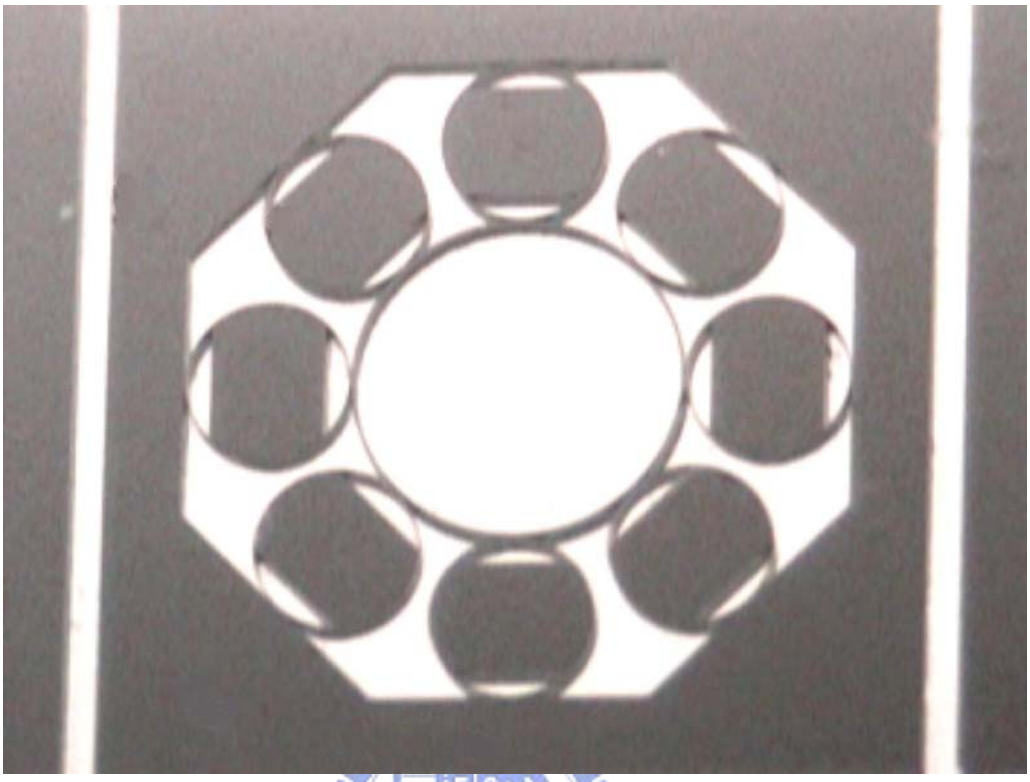


Figure 1.1 The structure of micro gyroscope

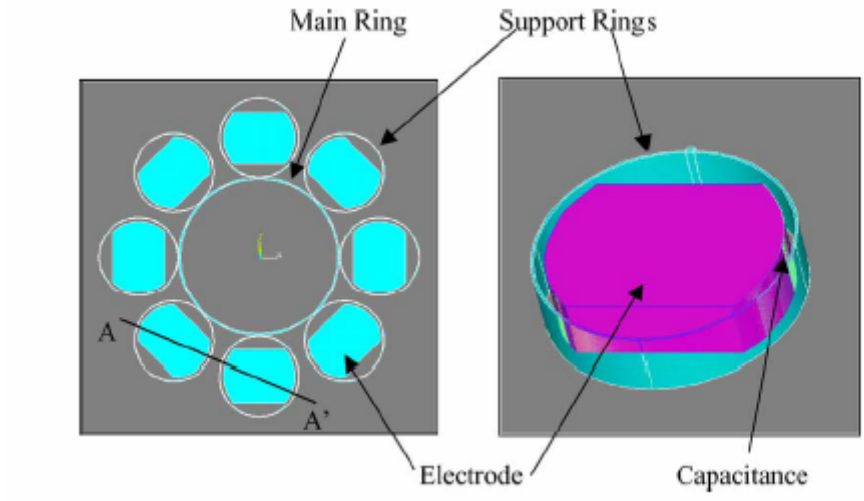


Figure 1.2 Top and detailed views of structure that includes electrodes.

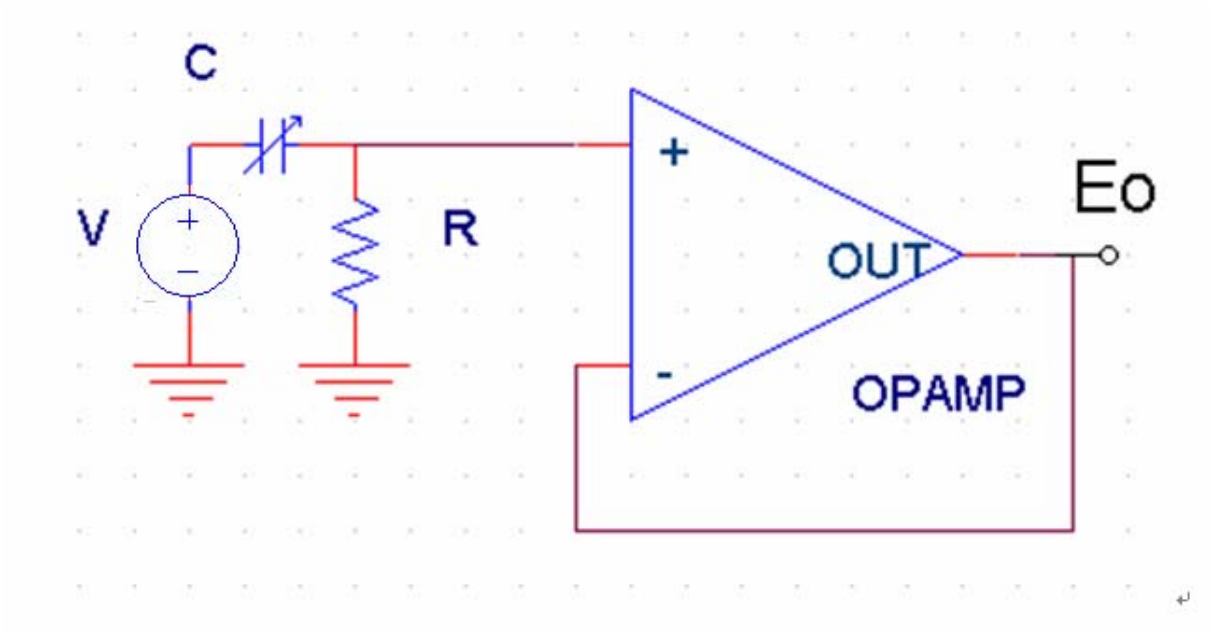


Figure 2.1 Direct detection circuit

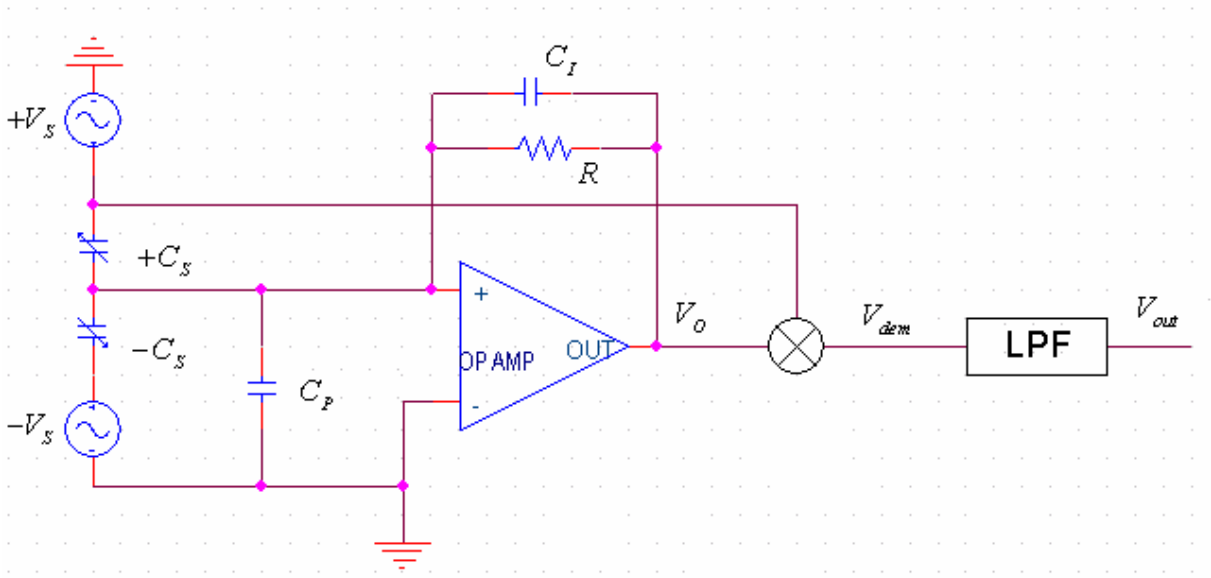


Figure 2.2 Synchronous detection circuit

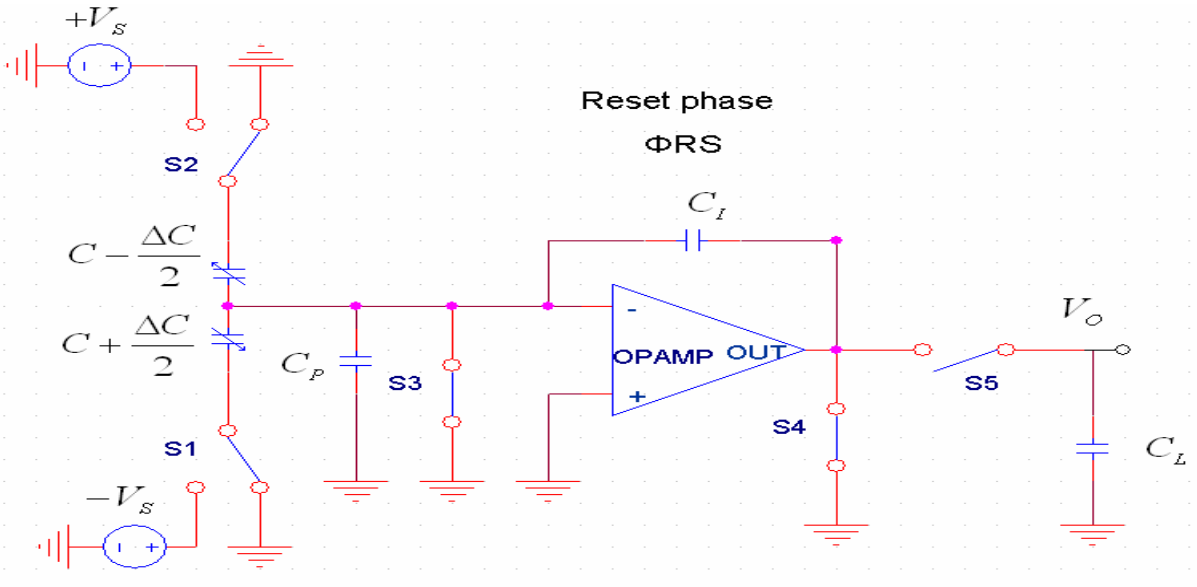


Figure 2.3(a) Reset phase

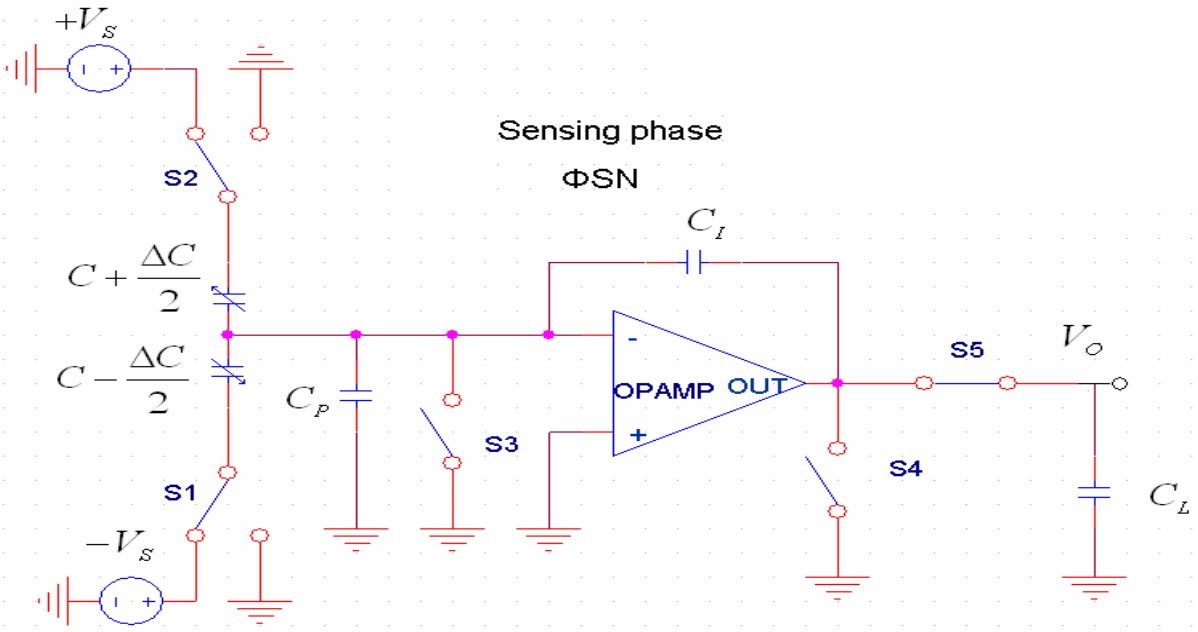


Figure 2.3(b) Sensing phase

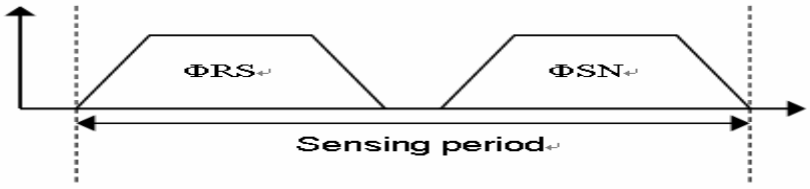


Figure 2.3(c) Sensing period

Figure 2.3 A typical implementation of the switched-capacitor sensing circuit

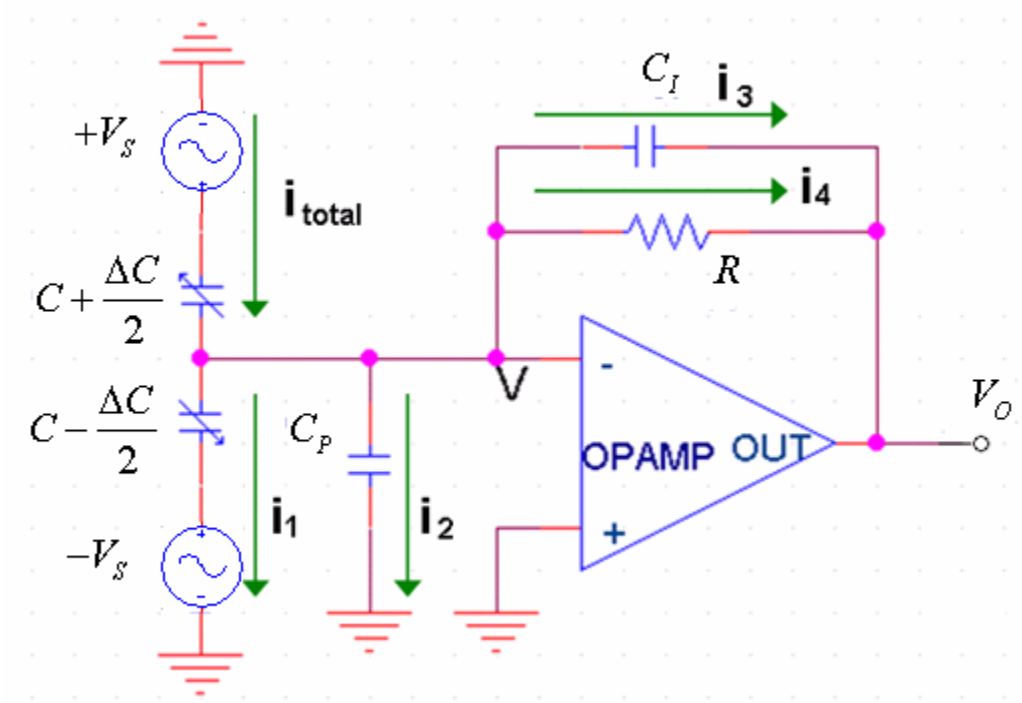


Figure 3.1 An implementation of the synchronous detection circuit for differential capacitor

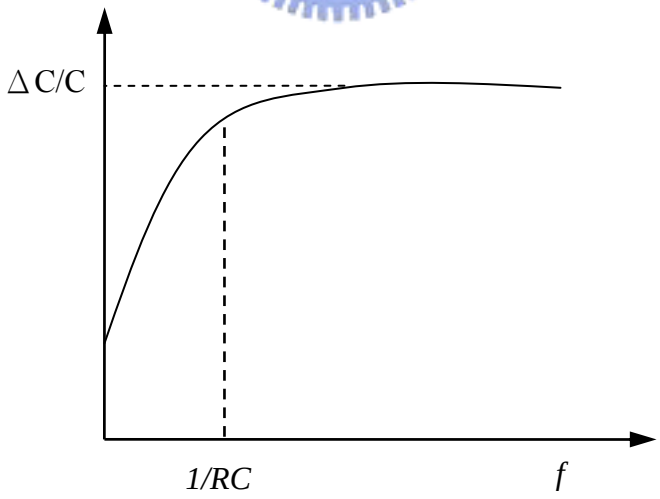


Figure 3.2 The magnitude of the circuit's bode plot

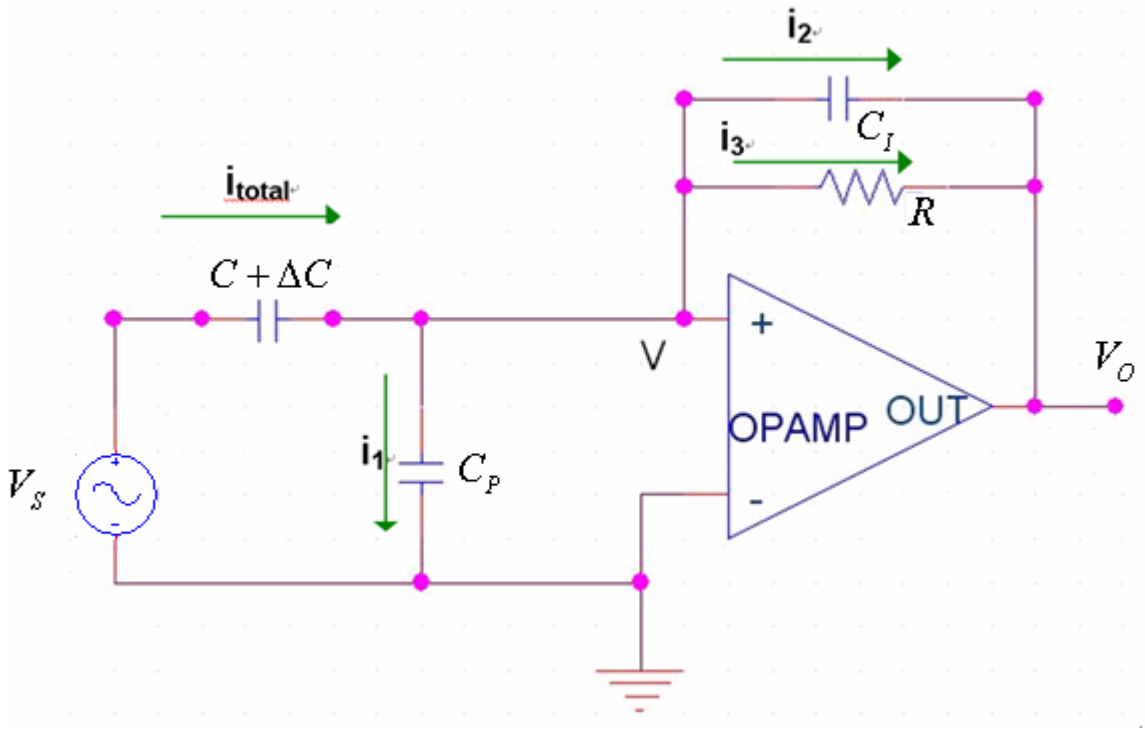


Figure 3.3 An implementation of the synchronous detection circuit for single capacitor.

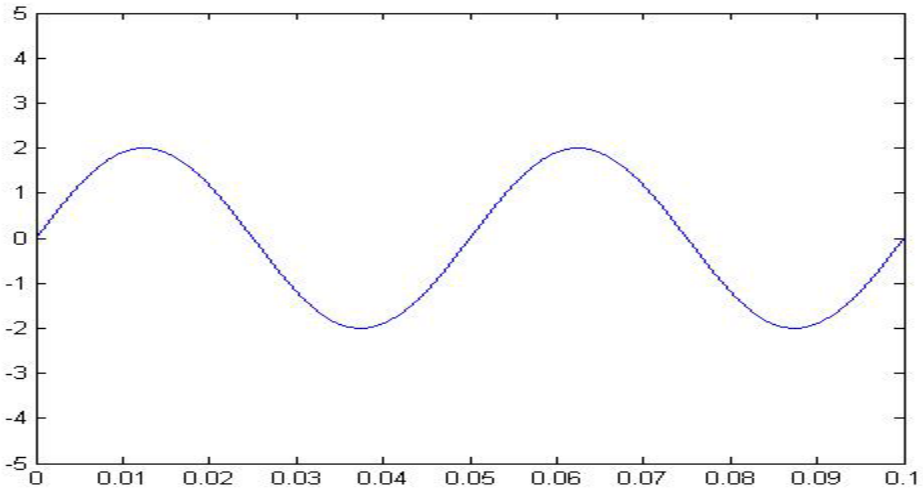


Figure3.4 (a) signal

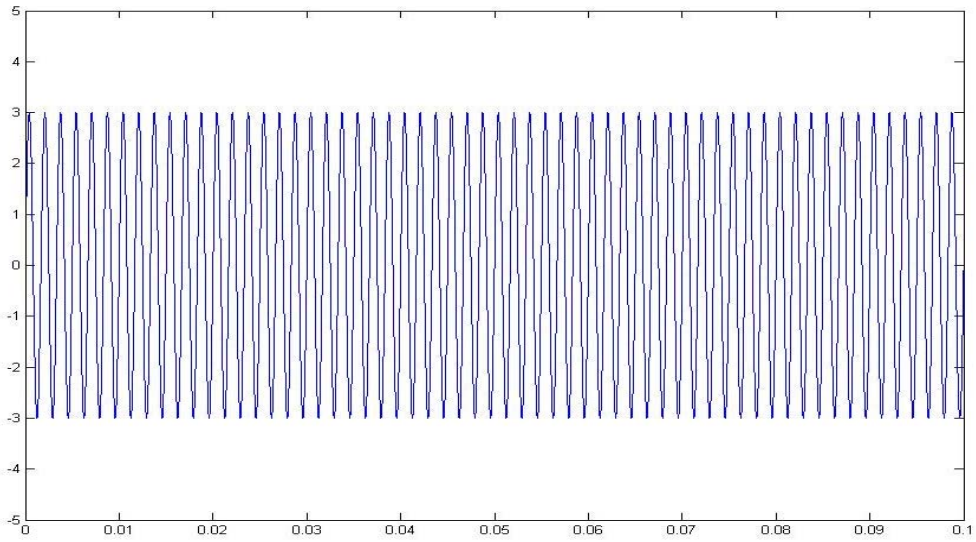


Figure 3.4(b) carrier

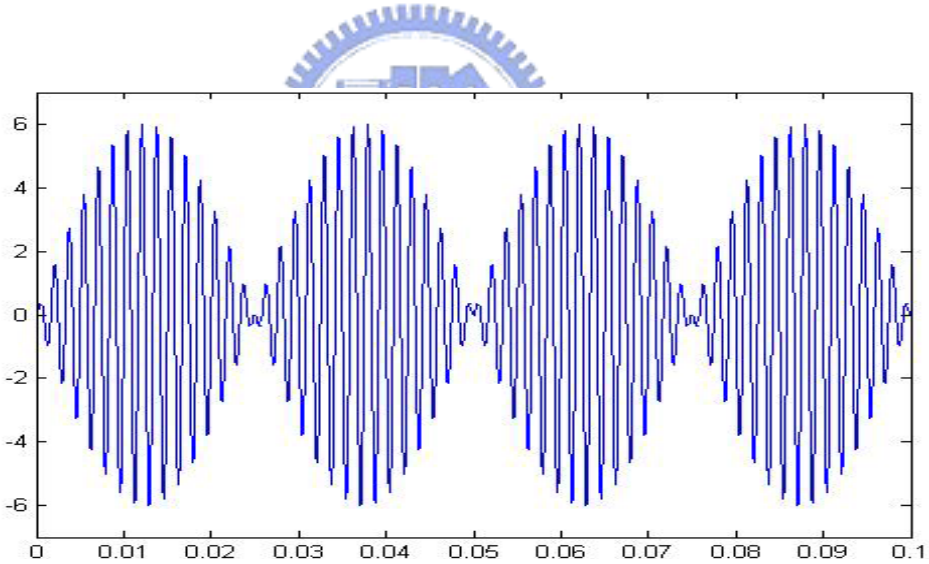


Figure 3.4(c) The modulated signal

Figure 3.4 The modulation process

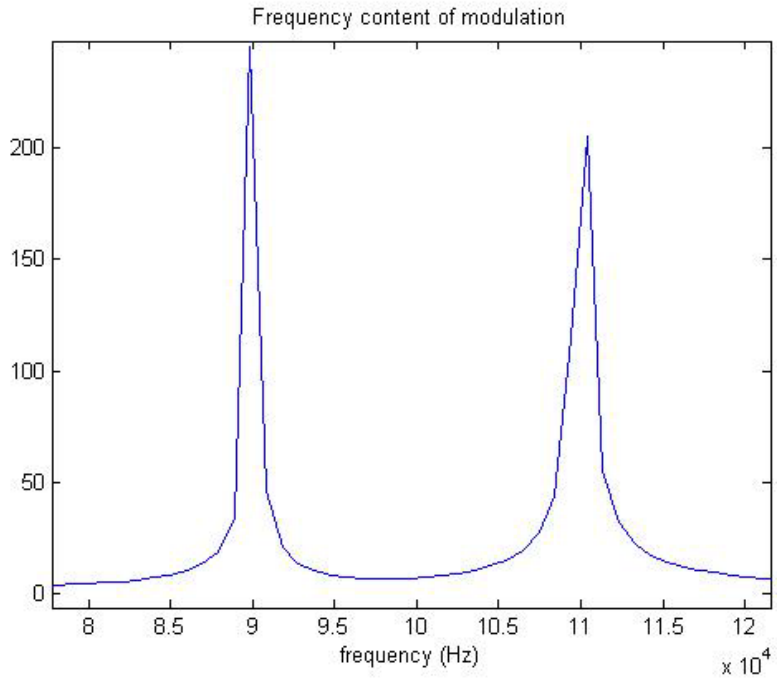


Figure 3.5(a) The spectrum of the modulated signal

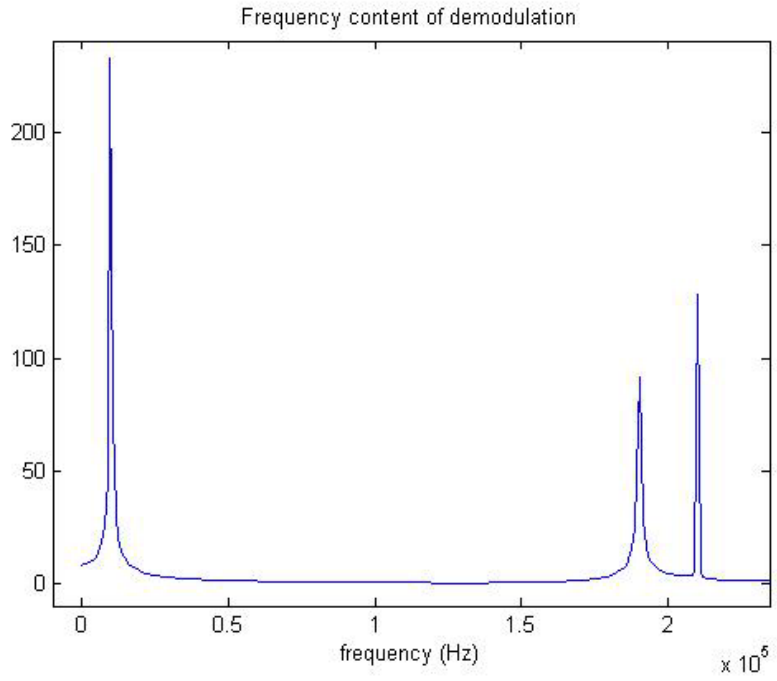


Figure 3.5(b) The spectrum of the demodulated signal

Figure 3.5 The spectrum of the modulated-demodulated signal
(with ω=100KHz , p=10kHz)

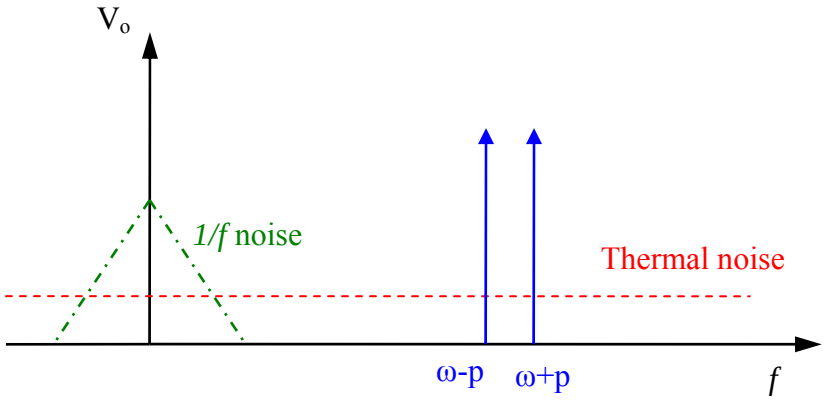


Figure 3.6 (a) The modulated signal spectra

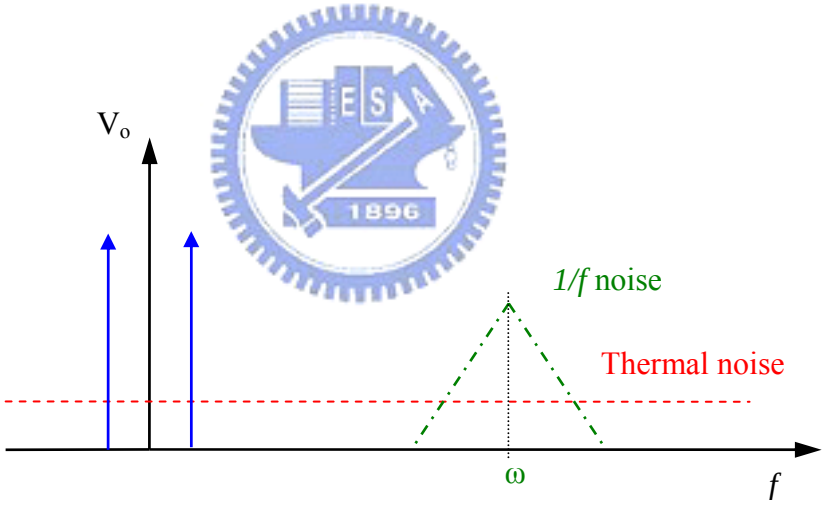


Figure 3.6 (b) The demodulated signal spectra

Figure 3.6 The *1/f* noise will be canceled during the modulation-demodulation

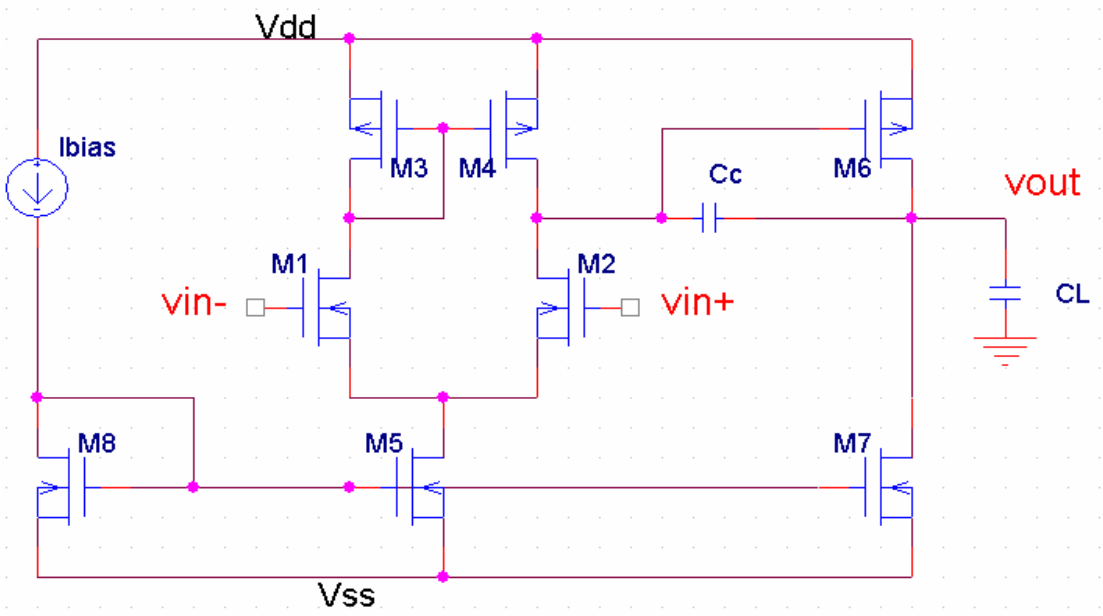


Figure 3.7 A classical two-stage CMOS operational amplifier

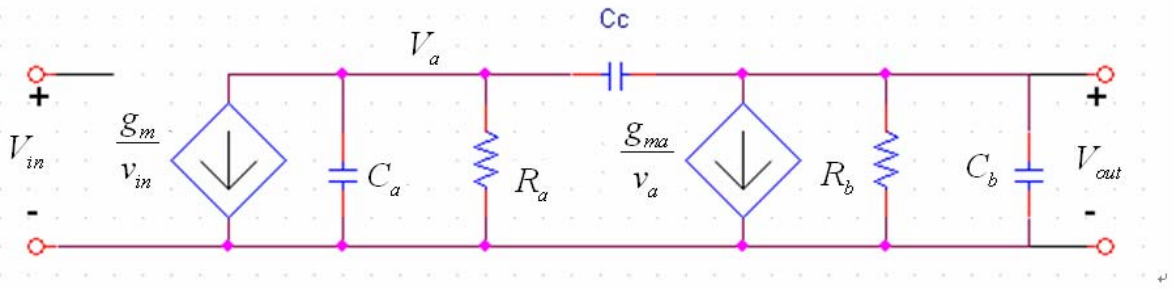


Figure 3.8 The small-signal model of two-stage operational amplifiers

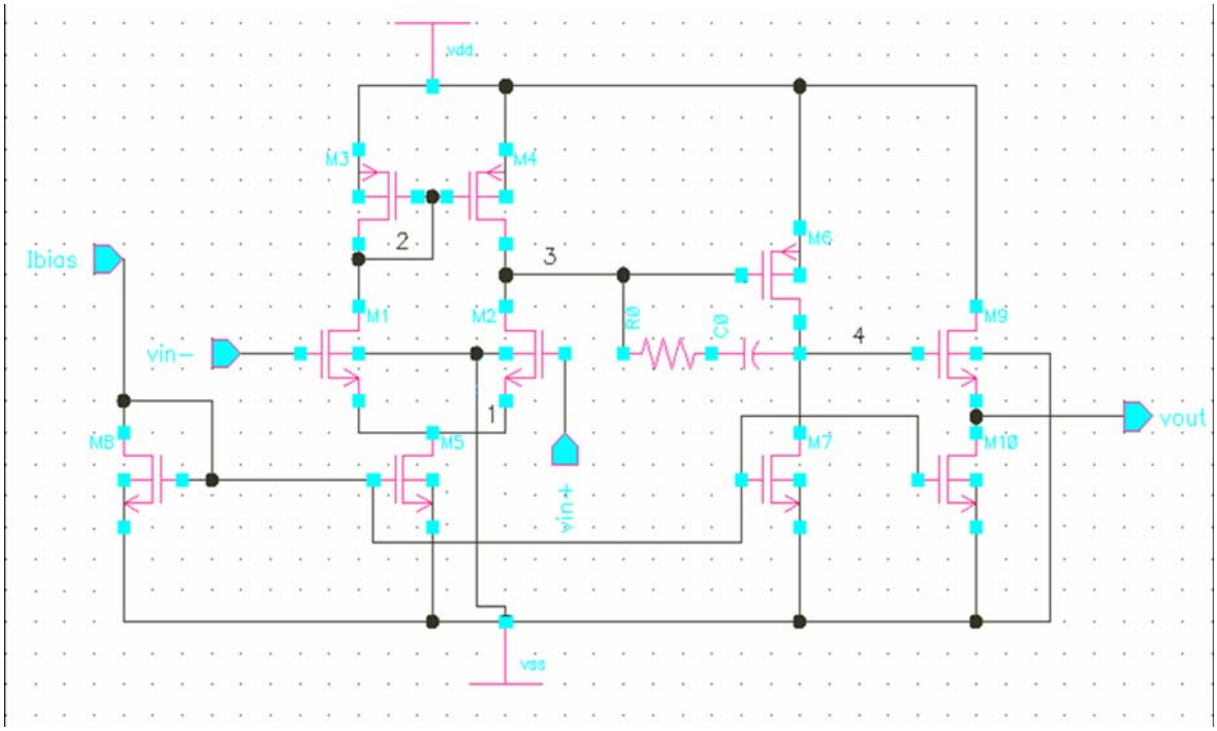


Figure 4.1 The schematic view of the operational amplifier

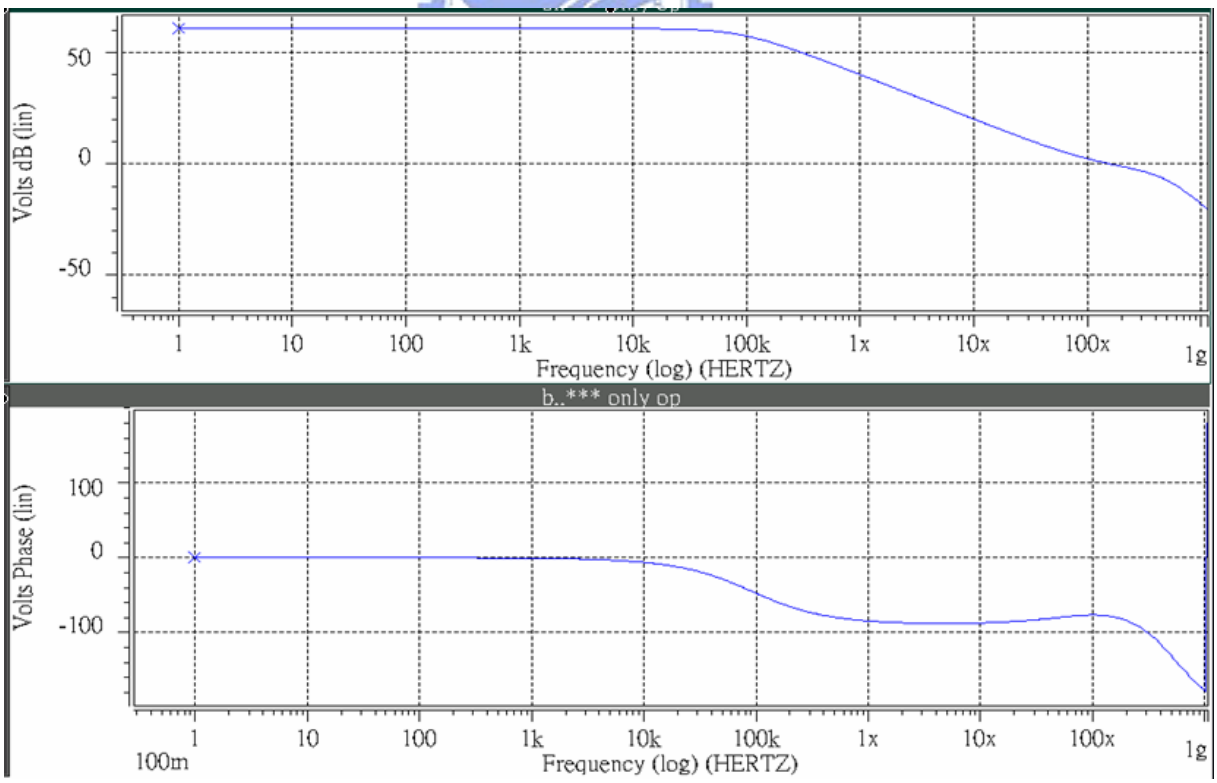


Figure 4.2 The bode plot of the operational amplifier

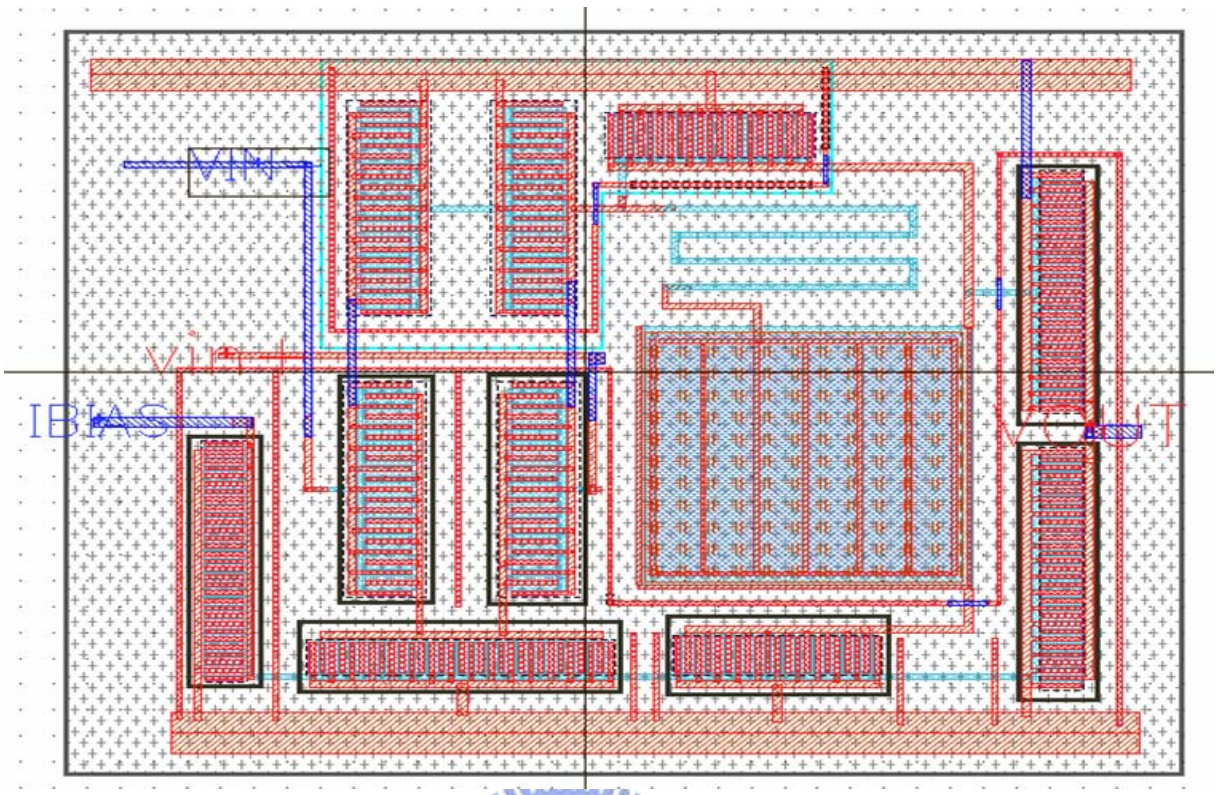


Figure 4.3 The layout view of the operational amplifier

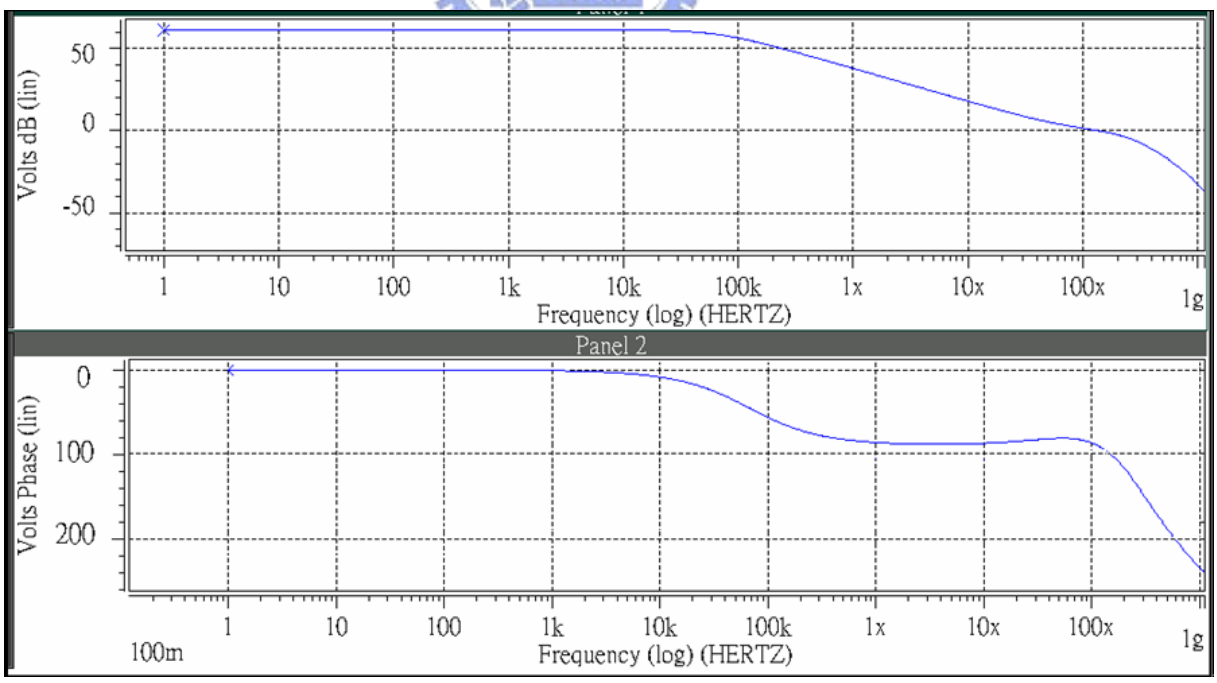


Figure 4.4 The frequency response of operational amplifier from post-simulation

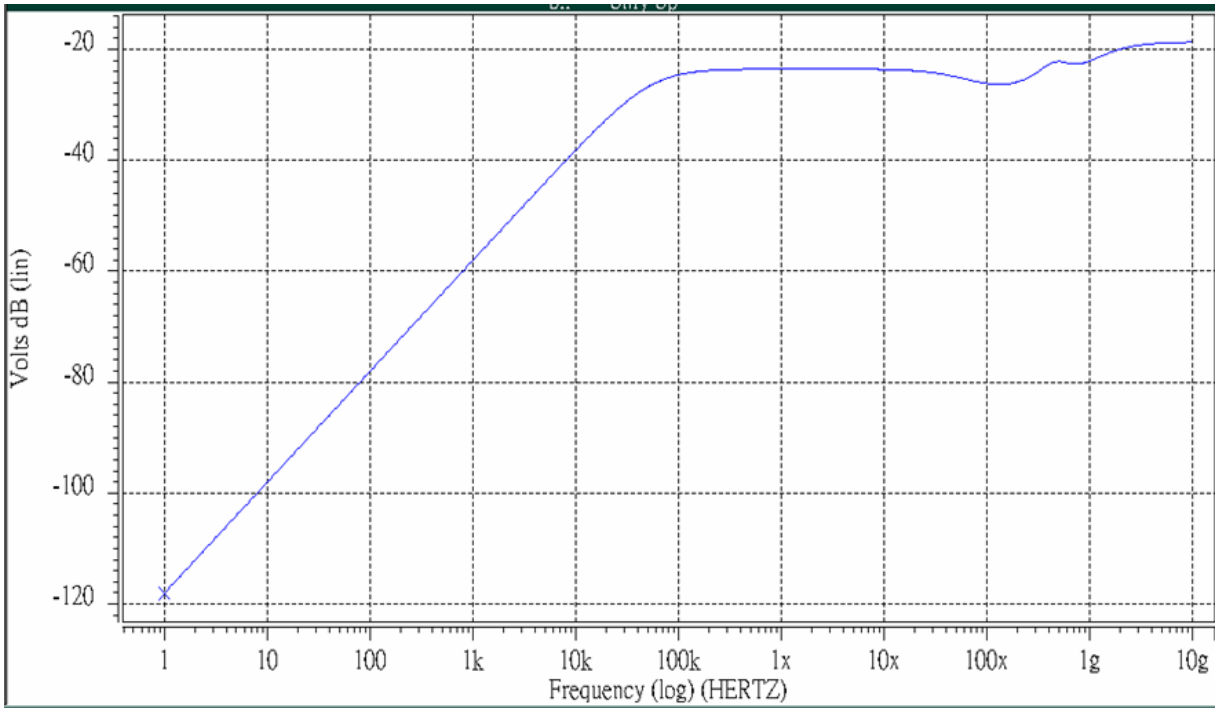


Figure 4.5 The frequency response of single capacitor sensing circuit

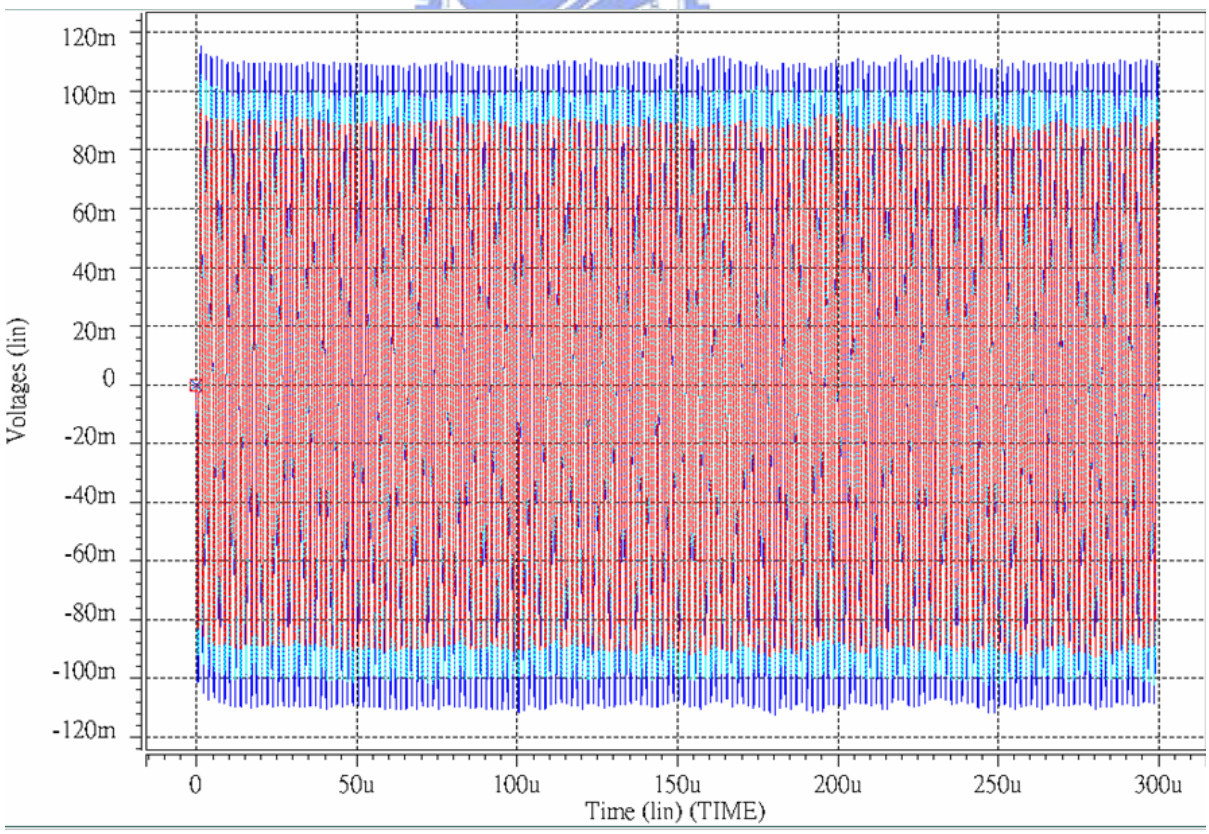


Figure 4.6 The output signal wave form of single capacitor sensing circuit

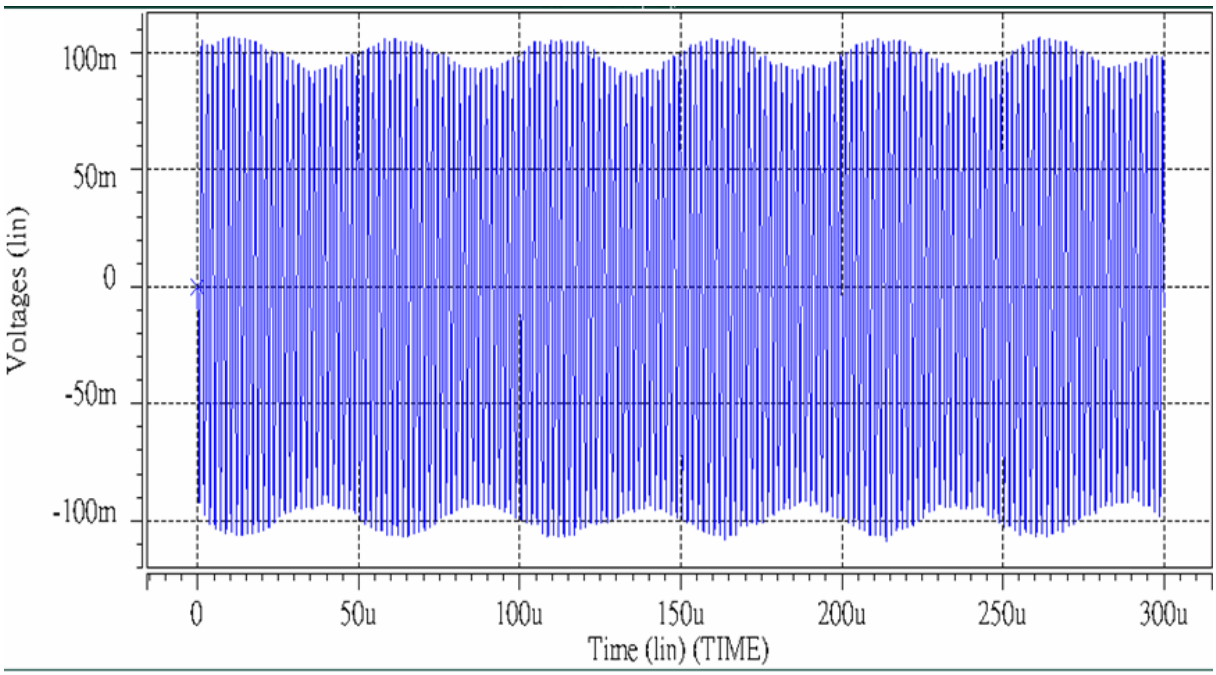


Figure 4.7 The modulated output signal of single capacitor sensing circuit

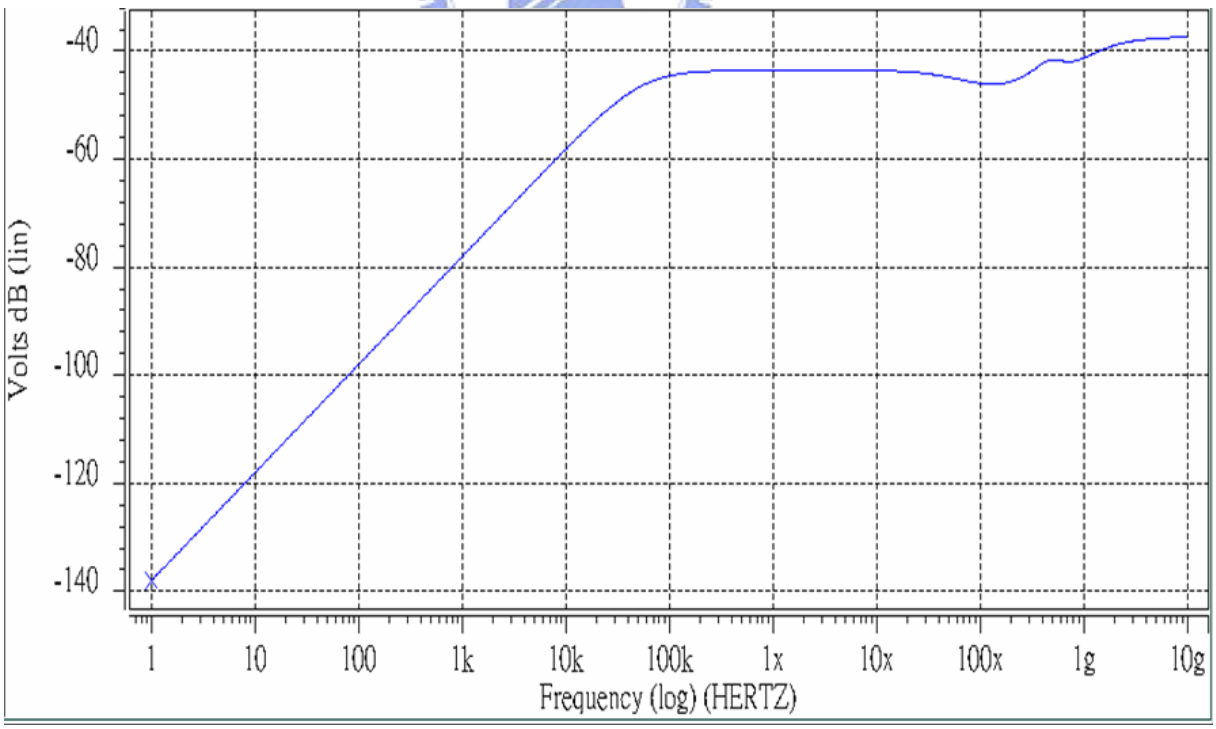


Figure 4.8 The frequency response of differential capacitor sensing circuit

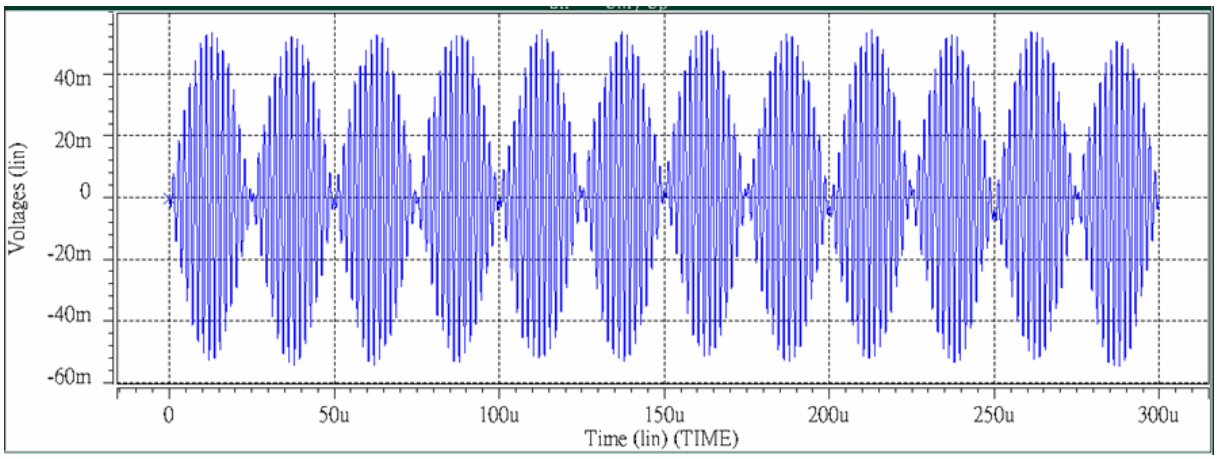


Figure 4.9 The modulated signal for the different capacitors sensing circuit

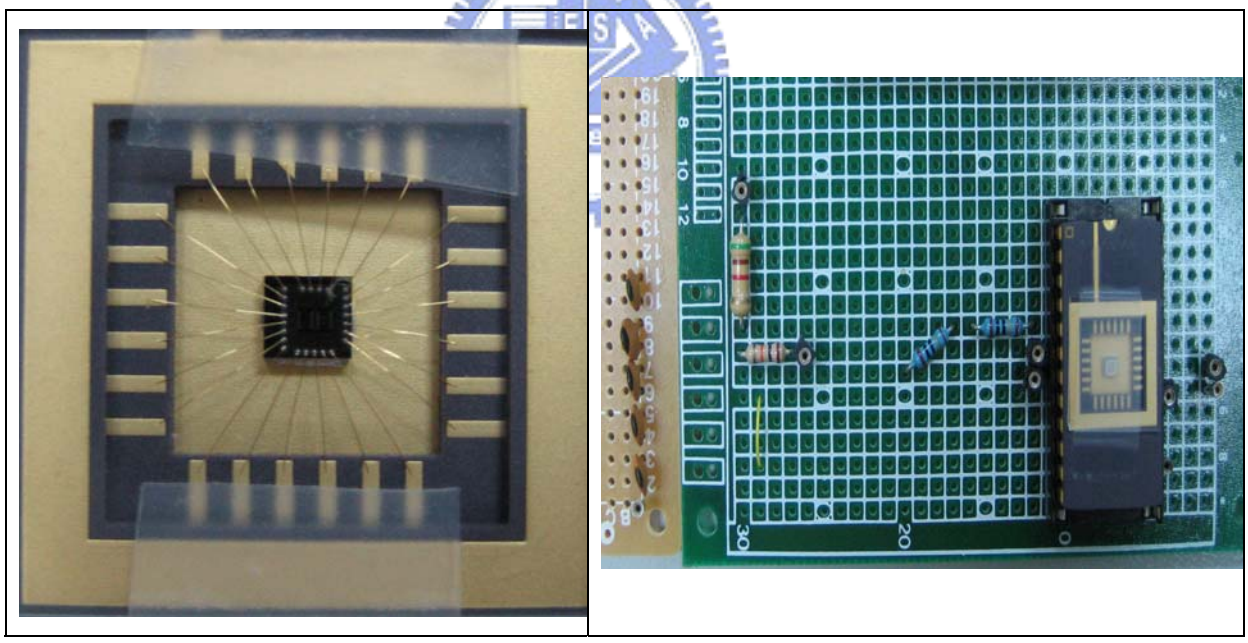


Figure 4.10 The picture of the synchronous detection circuit

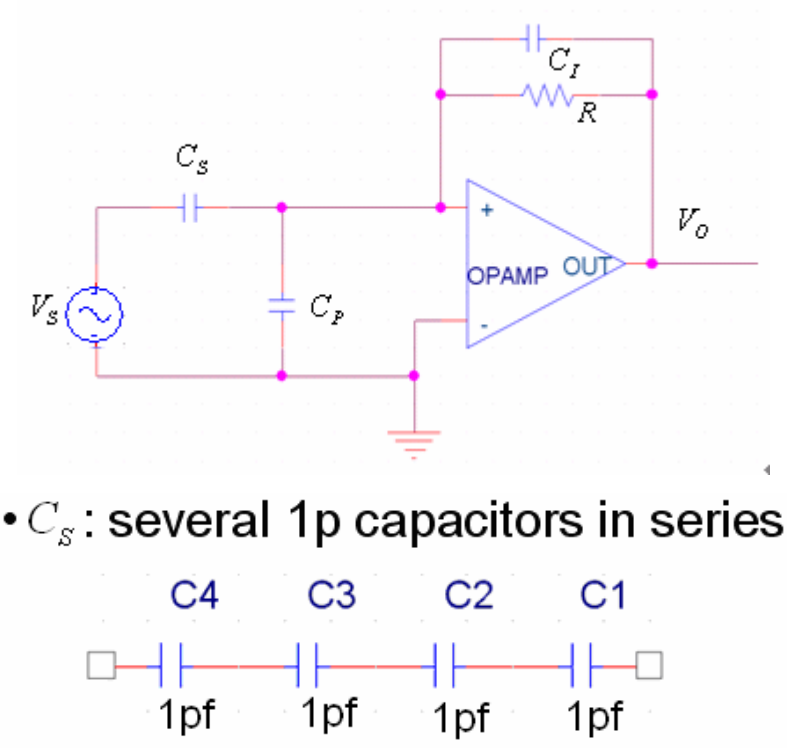


Figure 4.11 The measuring circuit scheme for single capacitor sensing

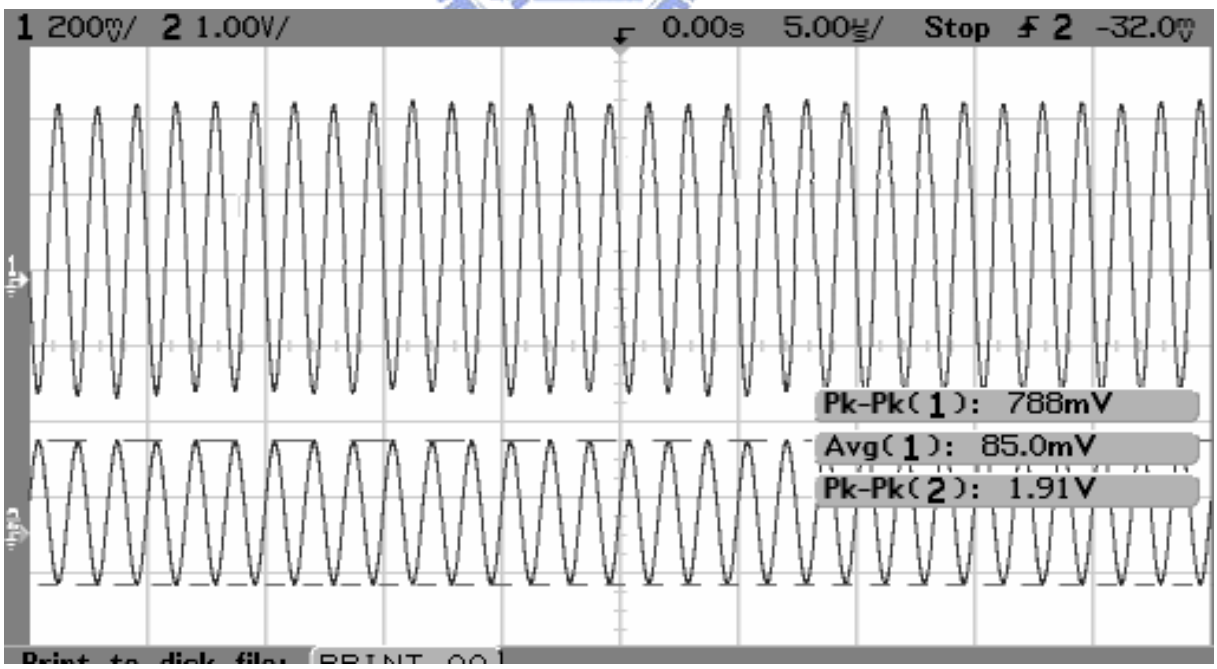


Figure 4.12 The carrier voltage and modulated output signal wave form

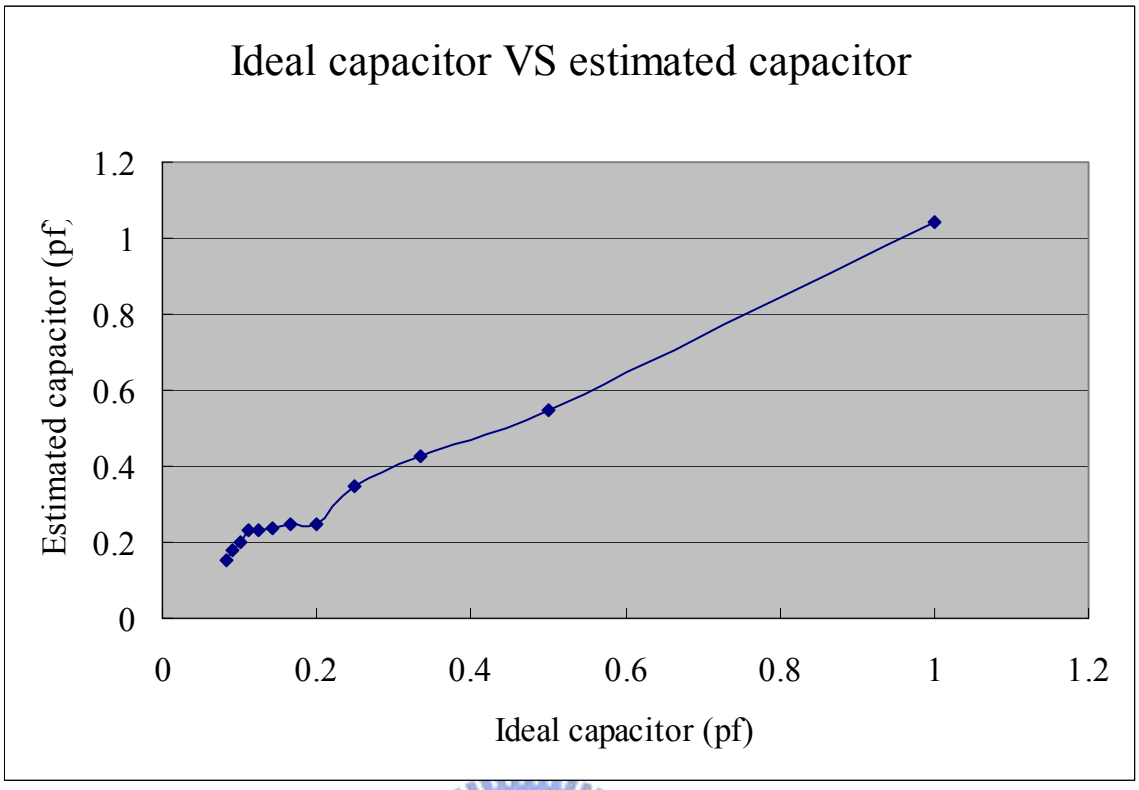


Figure 4.13 The ideal capacitor vs estimated capacitor

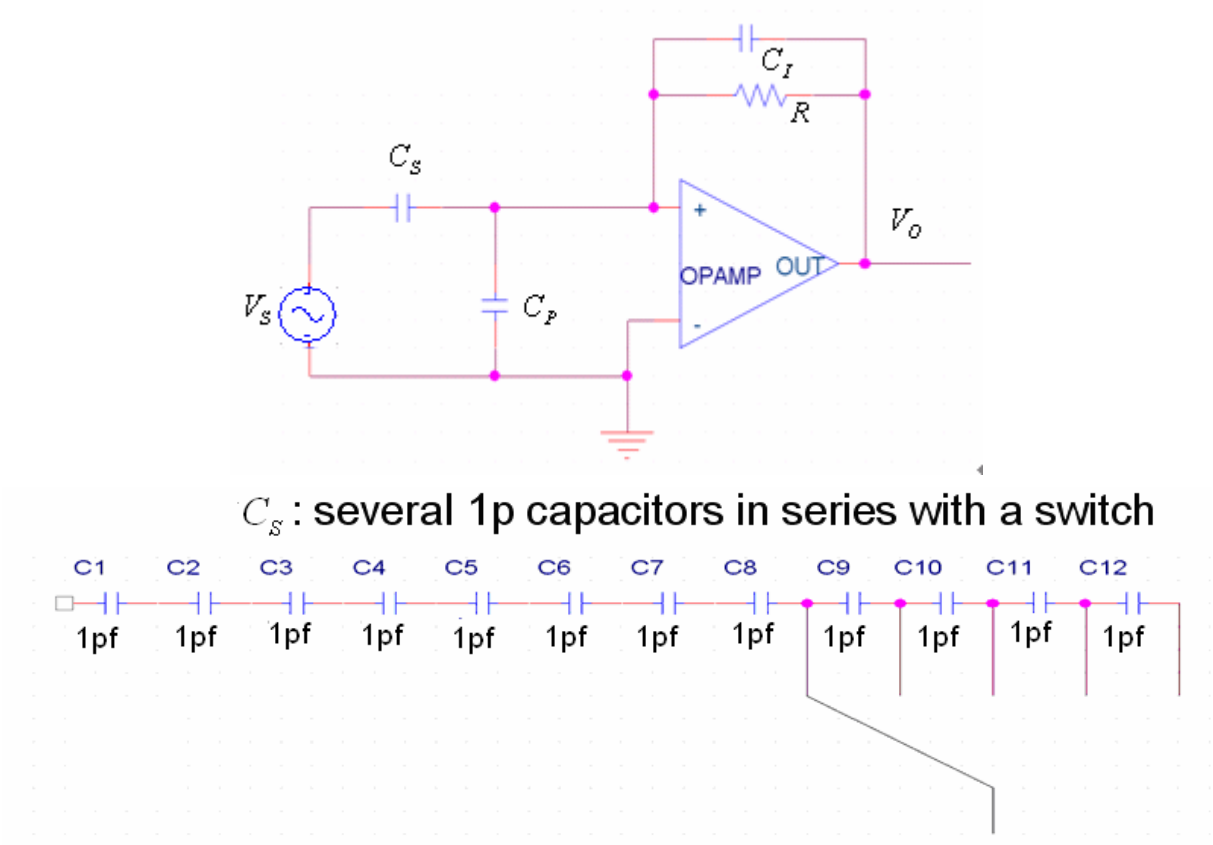


Figure 4.14 The scheme of sweep capacitor sensing circuit

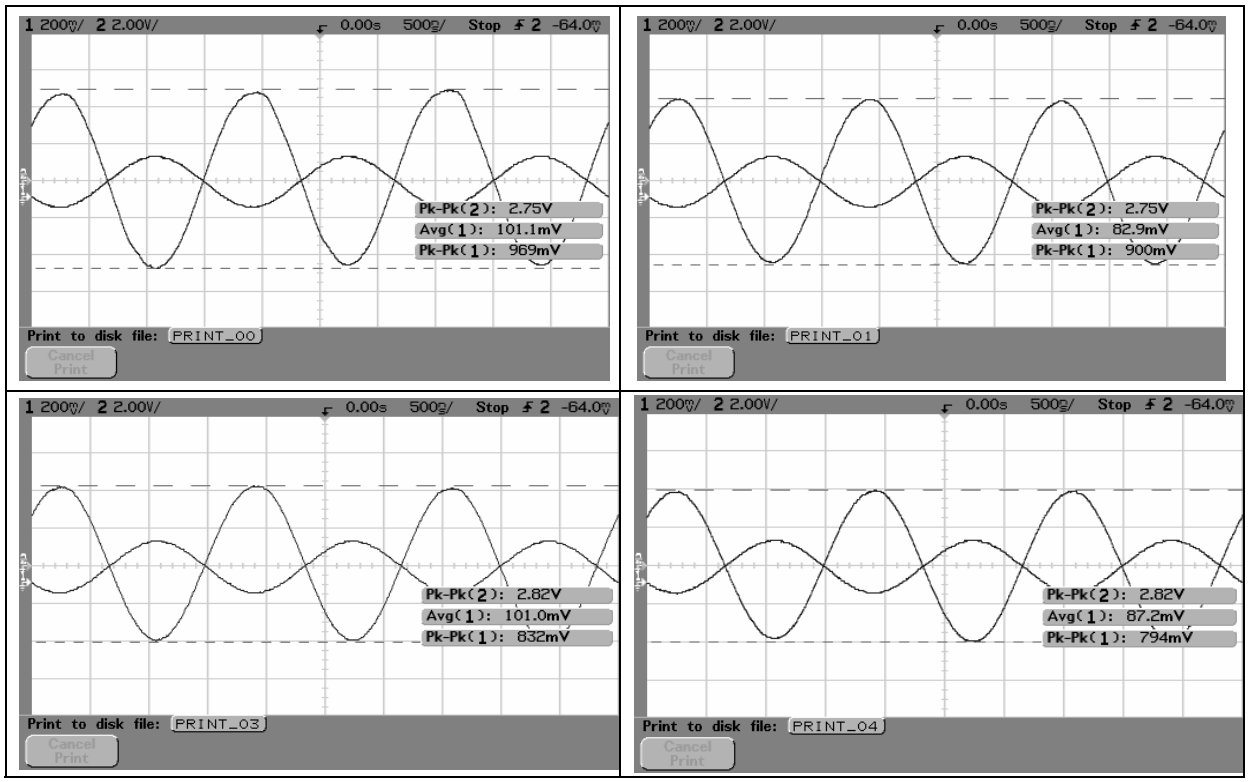


Figure 4.15 The signal wave form

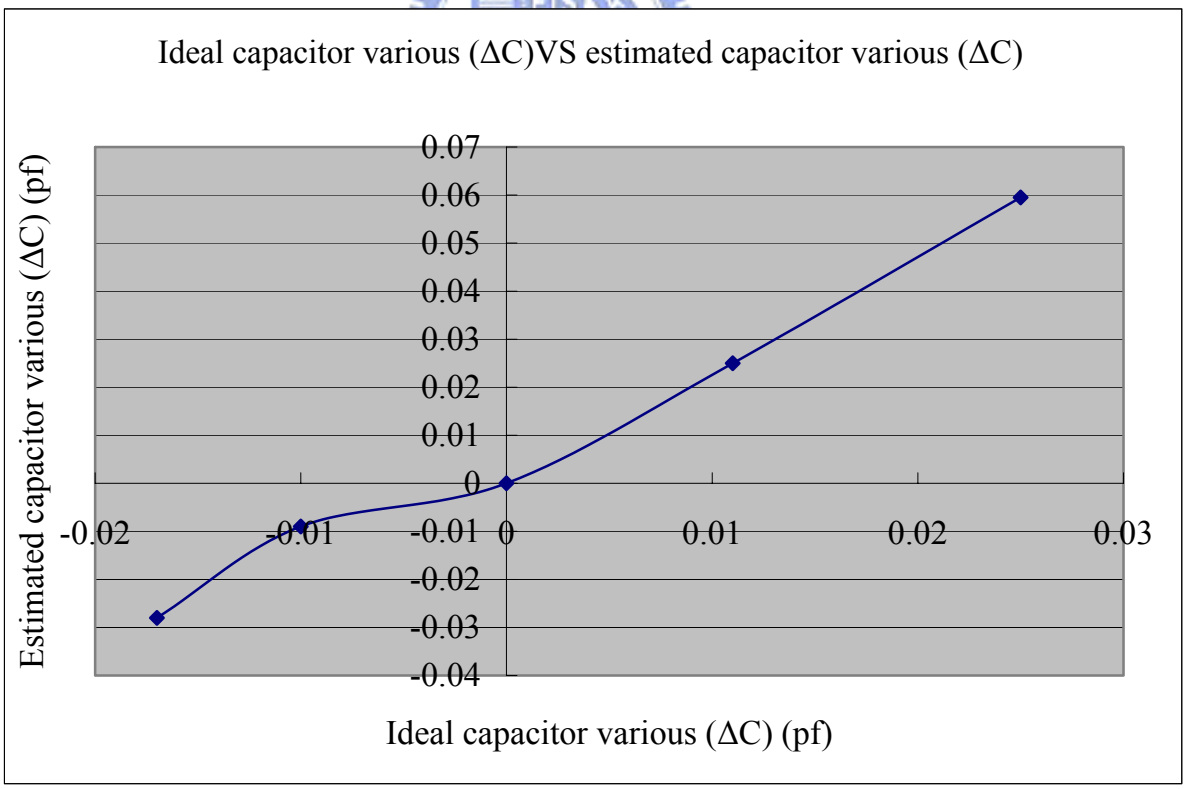


Figure 4.16 The ideal capacitor vs estimated capacitor various (compare with 0.1pf)

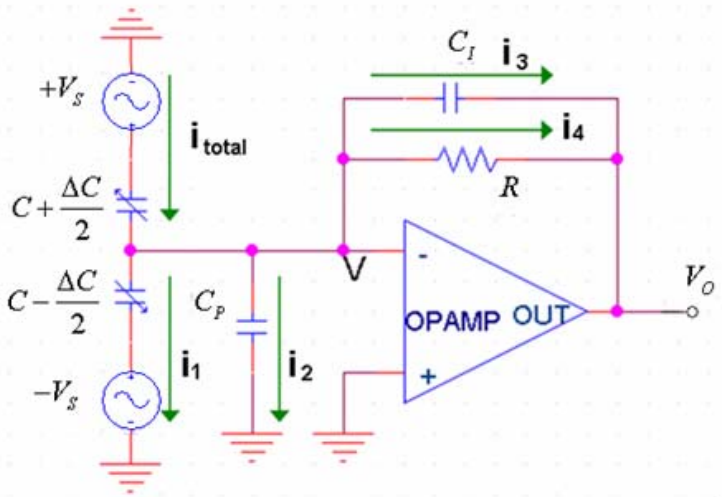
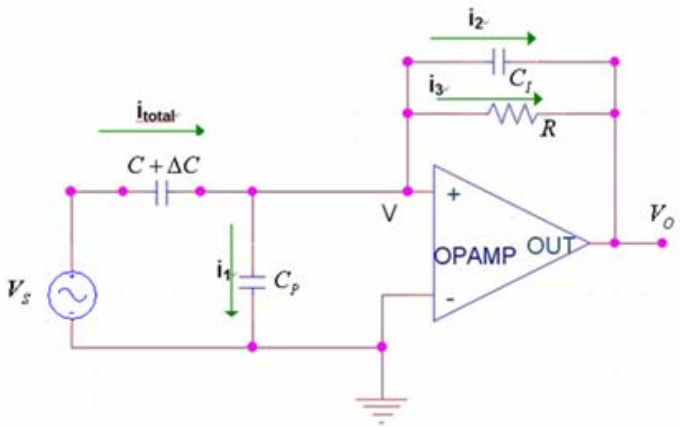
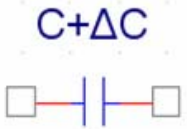
Type	Differential Capacitor Sensing	Single Capacitor Sensing
Schematic		
Capacitor type		
Transfer function	$V_O = -\frac{\Delta C}{C_I} V_S$	$V_O = -\frac{C_S}{C_I} V_S \qquad C_S = C + \Delta C$

Table 3.1 Compare with two types of synchronous detection circuit

Vdd=2.5V	Vss=-2.5V	SR≧40V/us	GB=100MHz
ICMR=-1 to 1.5V	Av≧1000	C_L=10pf	PM≧45°

Table 4.1 The specifications of design operational amplifier

Gain	P.M.	Unit Gain Freq.	3dB Freq.	Input Resister	Output Resister
1313 (62.36dB)	100°	158MHz	91.4KHz	$10^{20}\Omega$	146.7Ω

Table 4.2 The simulation specifications of design operational amplifier

Gain	P.M.	Unit Gain Freq.	3dB Freq.	Input Resister	Output Resister
11644 (61.32dB)	84.9°	135MHz	91.4KHz	$6.21\times10^{14}\Omega$	178.95Ω

Table4.3 The post-sim specifications of design operational amplifier

顆數	V	2	3	4	5	6
電容質	1	0.5	0.33	0.25	0.2	0.167
輸入振幅 V	0.5	1	1.5	1.5	2	2
輸出振幅 mV	0.347	0.365	0.425	0.347	0.333	0.328
估測電容質	1.041	0.548	0.425	0.347	0.249	0.246

顆數	7	8	9	10	11	12
電容質 pf	0.143	0.125	0.111	0.1	0.09	0.083
輸入振幅 V	2.5	3	3	3.5	4	4.5
輸出振幅 V	0.396	0.463	0.459	0.462	0.472	0.466
估測電容質 pf	0.237	0.2305	0.2295	0.198	0.177	0.155

Table 4.4 The measurement result of single capacitor sensing

顆數	8	9	10	11	12
電容質 pf	0.1+0.025p	0.1+0.011p	0.1p	0.1-0.01p	0.1-0.017p
輸入振幅 V	1.5	1.5	1.5	1.5	1.5
輸出振幅 V	0.425+0.0595	0.425+0.025	0.425	0.425-0.009	0.425-0.028
估測電容質 pf	0.4845	0.450	0.425	0.416	0.397

Table 4.5 The measurement result of sweep capacitor sensing