Chapter 1

Introduction

Micro-Electro-Mechanical Systems (MEMS) have been developed for pressure sensors, temperature sensors, accelerometers, gas chromatographs, and other sensor devices since 1970s. MEMS switches, as one of the MEMS devices that used mechanical movement to achieve a short circuit or an open circuit in a transmission line (Fig.1), were first developed in the early 1980s. The development of this miniature mechanical device came from the need of reducing leakage current which is existed in the electronic components made by solid states devices. Even though these miniature mechanical switches were developed 20 years ago, it is still remained a laboratory curiosity up to now.

The force required for the actuation of mechanical structures can be electrostatic, magnetostatic [5], piezoelectric, or thermo-actuation [11]. To date, only electrostatic-actuated type switches were commonly used due to its high operation reliability (100 million to 10 billion cycles) and the fabrication process compatibility with the IC fabrication process.

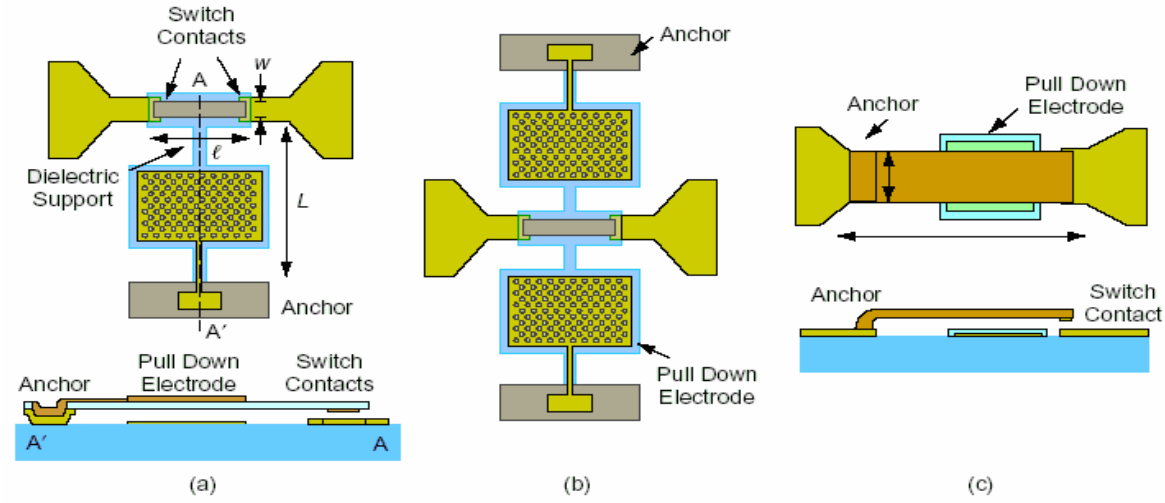


Fig. 1 [1]Broadside MEMS-series switches with (a) one electrode, (b) two electrodes, and (c) inline MEMS-series switches.

The advantages of MEMS switches over diode or FET switches are:

- Near-zero power consumption: Electrostatic actuation requires 20-80 V but does not consume any current, leading to the very low power dissipation (10-100 nJ per switching cycle).

- High electrical isolation: MEMS switches are fabricated with air gaps. Therefore, they have very low off-state capacitances (2-4 fF) which results in excellent isolation at the RF operation range of 0.1-40 GHz.

- Low insertion loss: MEMS switches with shunt operation have the insertion loss of -0.1 dB up to 40 GHz.

However, MEMS switches also have their share of problems, such as:

- Relatively low speed: The switching speed of most MEMS switches is around

2-40 μs. Certain communication and radar systems require faster switches.

- Power handling: Most MEMS switches cannot handle power more than 20-50 mW. MEMS switches that can handle 0.2-10 W with high reliability simply do not exist today.

- High-voltage drive: Electrostatic MEMS switches require 20-80 V for reliable operation, and this usually necessitates a voltage-up converter chip when used in portable telecommunication systems.

- Reliability: The life cycles of the mature MEMS switch designs are in the order of 0.1-10 billion cycles. However, many systems require switches with 20-200 billion operations for the life cycles. Also, the long-term reliability (years) has not yet been addressed.

- Packaging: MEMS switches need to be packaged in inert atmospheres (nitrogen, argon, etc.) and in very low humidity, resulting in hermetic or near-hermetic seals. Packaging costs are currently high. The packaging technique itself may adversely affect the reliability of the MEMS switches.

- Cost: MEMS switches can be fabricated, using surface micromachining techniques, on quartz, Pyrex, low-temperature cofired ceramic (LTCC) or even mechanical-grade silicon substrates, which could possibly achieve a low-cost fabrication process. However, one must add the cost of packaging and the high-voltage drive chip. It is, therefore, hard to beat a $0.30-0.60 single-pole double-throw 3-V FET switch, tested, packaged, and delivered.

Although MEMS switches are promising in reducing leakage current, their limited functions, which consist of "on" and "off" only, may tapered their applications. In 1999, A. Hirata, K. Machida, H. Kyuragi, and Maeda first demonstrated the concept of "**MEMS Logic Gate**" [27], which is a miniature mechanical device that can perform the Boolean logic functions. However, according to their device design, one design (mechanical structure design) can only perform a dedicated logic function. They need different structure designs to perform various logic functions, which could result in fabrication difficulties and higher fabrication cost. For this reason, we develop a mechanical switch which can perform logic functions the same as a solid-state device "NOR" or "NAND" gate does. Moreover, the newly designed mechanical structure can produce different logic functions by different electrical interconnect layouts without the need of different mechanical structure. As we all know, the logic functions of logic IC circuits came from the combination of thousands or millions of basic logic components, such as AND gate, NOR gate, NAND gate, NOR gate, together. (The truth table corresponding to the gate Input/Output relationship is listed below.). Therefore, one mechanical structure that can perform various logic functions represents a big progress in deploying these switches in practice.

In this project, the software **Coventoreware2004** [17] was used to check the key parameters of the proposed MEMS logic gates including, resonant frequency, damping coefficient, pull-in voltage and logic functions.

Table 1 Truth Table corresponding to Input/Output

Input\Output		OR	NOR	AND	NAND
A	1	1	0	0	1
B	0				
A	0	1	0	0	1
B	1				
A	0	0	1	0	1
B	0				
A	1	1	0	1	0
B	1				

Chapter 2

Design of MEMS Logic Gate

Fig. 2.1 shows the cartoon version of the proposed logic gate device. A tiltable doped poly-silicon plate is suspended by two torsional springs at the left and right, and is parted by the electrical isolation material such as silicon nitride.

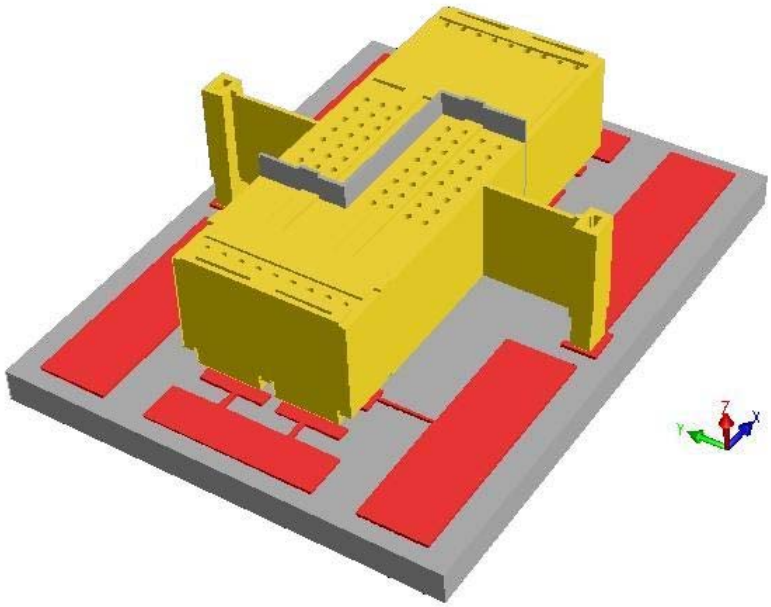


Fig. 2.1 The cartoon version of the logic device

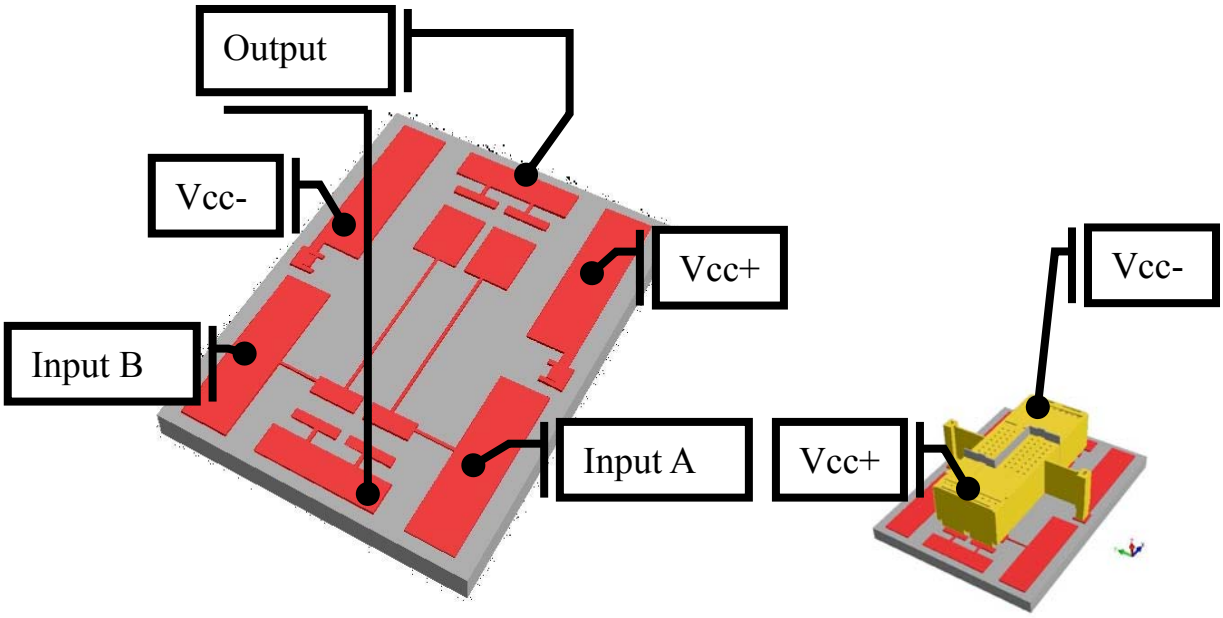


Fig. 2.2 Voltages distribution of the logic gate (NOR gate)

As shown in Fig 2.2, the bias voltages, V_{cc}^{+} and V_{cc}^{-}, are applied to two sides of moving plate through anchor structure and torsional bars, respectively. The two input signals, Input A and Input B, are applied to the electrodes positioned underneath the moving plate. Due to the voltages difference between input electrodes and the moving plate, the attractive electrostatic force is generated at two sides of moving plate, and thus results in a net torque on the plate structure. The plate is perforated for the ease of fabrication and the control of air damping effect during gate operation. The plate is tilted by the torque, and the dimples at both sides of the seesaw structure touch on the output pads and then supply voltage at the output terminals.

I. Lumped-modeling of MEMS Logic Gate

For the preliminary design, the lumped model method was used to explore the dynamic response of our proposed logic device. The dynamic system is modeled as a 2nd

order system which is composed of inertial moment J, damping coefficient δ, torsional spring constant K_θ, and torque M generated by electrostatic force. The total torque of the system is composed of the electrostatic torque, damping, inertial and the mechanical torque exerted by the springs on which the tiltable moving plate.

The dynamic response of such a system can be written as:

$$J\ddot{\theta} + \delta\dot{\theta} + K_\theta\theta = M \tag{1}$$

For the torsional spring constant $K_\theta = 2\dfrac{GJ_{spring}}{l_{spring}}$, where G denotes the shear modulus of the material, J_{spring} is the area moment of inertial, and l_{spring} is the length of each slender torsional spring.

1. System Response

By applying Laplace Transform on Eqn. (1), the frequency response is found to be:

$$\frac{\theta(j\omega)}{M(j\omega)} = \frac{1}{K_\theta}\left[\frac{1}{1-(\omega/\omega_0)^2 + j\omega/(Q\omega_0)}\right] \tag{2}$$

where $\omega_0 = \sqrt{K_\theta / J}$ is the resonance frequency(rad./sec.) and $Q = K_\theta/(\delta\cdot\omega_0)$ is the quality factor which are the two key parameters in determining the switching time for the dynamic systems. According to the reference [21], it is advantageous to have a structure with $0.5 \le Q \le 2$. A system with $Q \le 0.5$ would result in a slow switching time, while $Q \ge 2$ results in a long settling time. Furthermore, a high-Q structure will not affect the

switching speed of the device for $Q \geq 3$. However, it has a large effect on the settling time of the switch when it is released from the down-state position.

Electrostatic spring softening is a pheromone that is often encountered in devices using electrostatic force. It is due to the action of the nonlinear electrostatic torques contributes with negative sign to that of the linear mechanical torque, which leads to a smaller value of the effective spring constant at the operating point. Consequently, the resonant frequency varies with the electrostatic force at each operation point. It results in instability of the system where the resonant frequency of the system reduced to zero. Besides, it also has a great impact on the Quality factor, switching time, and etc.

2. Electrostatic Force

Electrostatic force is one of the major means in the MEMS devices; however, most of the equations for the electrostatic actuation are desired for its linear motions. Due to the torsional motion of our proposed device, we derived equations for the torsional motion under electrostatic actuation.

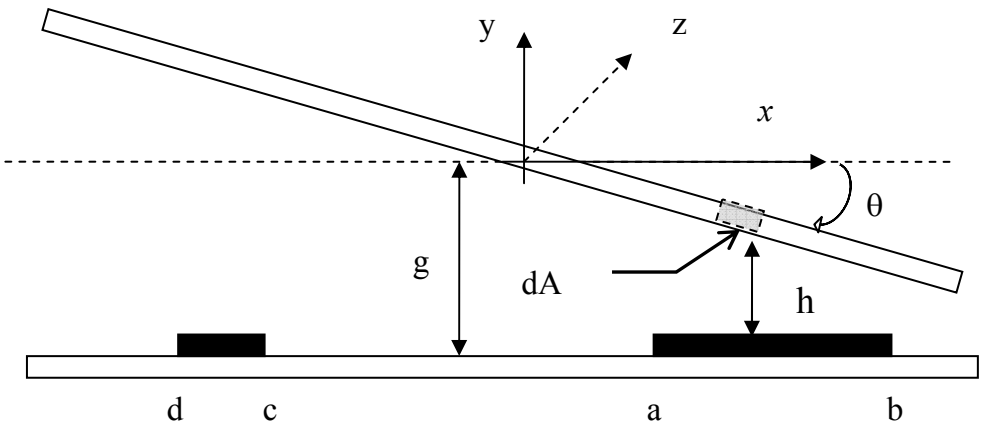


Fig. 3 Lateral view of the switch device

In a first-order approximation, the main-plate of the torsional gate is considered as tilt-able, rigid body; therefore, the only degree of freedom is the torsion angle θ as shown in Fig. 3. The differential capacitance of the infinitesimal element between the tilted plate and the underlying electrode is:

$$dC = \varepsilon \frac{dA}{h} = \frac{\varepsilon w dx}{g - x\sin\theta} \cong \frac{\varepsilon w dx}{g - x\theta} \tag{3}$$

The energy storied in the infinitesimal capacitance is:

$$dU = \frac{1}{2} V^2 dC = \frac{\varepsilon w V^2}{2} \frac{dx}{g - x\theta} \tag{4}$$

The differential force acting on a segment of each signal electrode is:

$$dF = \frac{dU}{dx} = \frac{\varepsilon w V^2}{2} \frac{dx}{(g - x\theta)^2} \tag{5}$$

Where ε denotes the electric permittivity, V the applied voltage, g is the gape between torsion axis and bottom signal electrodes. Let and a & b denotes the locations of the underlying electrodes, then we get the torque M :

$$M = \int_a^b x dF = \frac{\varepsilon w V^2}{2} \int_a^b \frac{x dx}{(g - x\theta)^2}$$

$$= \frac{\varepsilon w V^2 \left[(b-a)g\theta - (g - a\theta)(g - b\theta) \ln(\frac{g - a\theta}{g - b\theta}) \right]}{2\theta^2 (g - a\theta)(g - b\theta)}$$

$$= \frac{\varepsilon w V^2}{2\theta} (\frac{b}{g - b\theta} - \frac{a}{g - a\theta}) - \frac{\varepsilon w V^2}{2\theta^2} \ln(\frac{g - a\theta}{g - b\theta}) \tag{6}$$

The capacitance can be calculated from the electric field distribution $E(x) = V/(g - x\sin\theta)$ according to

$$q = \int_a^b \frac{\varepsilon w V}{g - x\theta} dx = \frac{\varepsilon w V}{\theta} \ln\left(\frac{g - a\theta}{g - b\theta}\right) \tag{7}$$

hence

$$C = \frac{q}{V} = \frac{\varepsilon w}{\theta} \ln\left(\frac{g - a\theta}{g - b\theta}\right) \tag{8}$$

If the actuator is driven by charge instead of voltages, q/C can be substituted for V in Eqn. (6), and the new equation is:

$$M = \frac{\varepsilon w V^2}{2(g - a\theta)(g - b\theta)} - \frac{qV}{2\theta} \tag{9}$$

3. Pull-in Voltage

"Pull-in" is an important behavior existed in most of the voltage-controlled electrostatic actuator. In order to explain it, we consider the force (torque) balance between the attractive electrostatic force that pulls the plate down and the restoring spring force that pulls the plate up. Due to the fact that the attractive electrostatic force is inverse proportional to the gap square and the restoring spring force is proportional to the gap, there could exist a plate position where the force (torque) balance is no longer hold. The unbalance between two forces could cause the plate snap to one direction which is known for "pull-in". Furthermore, the electrostatic force is generated by the actuation voltage applied to the electrodes. The specific voltage at which the equilibrium is lost is called pull-in voltage. Fig. 4 shows the mechanical and electrostatic torque vs. torsional angle

under different gate voltages.

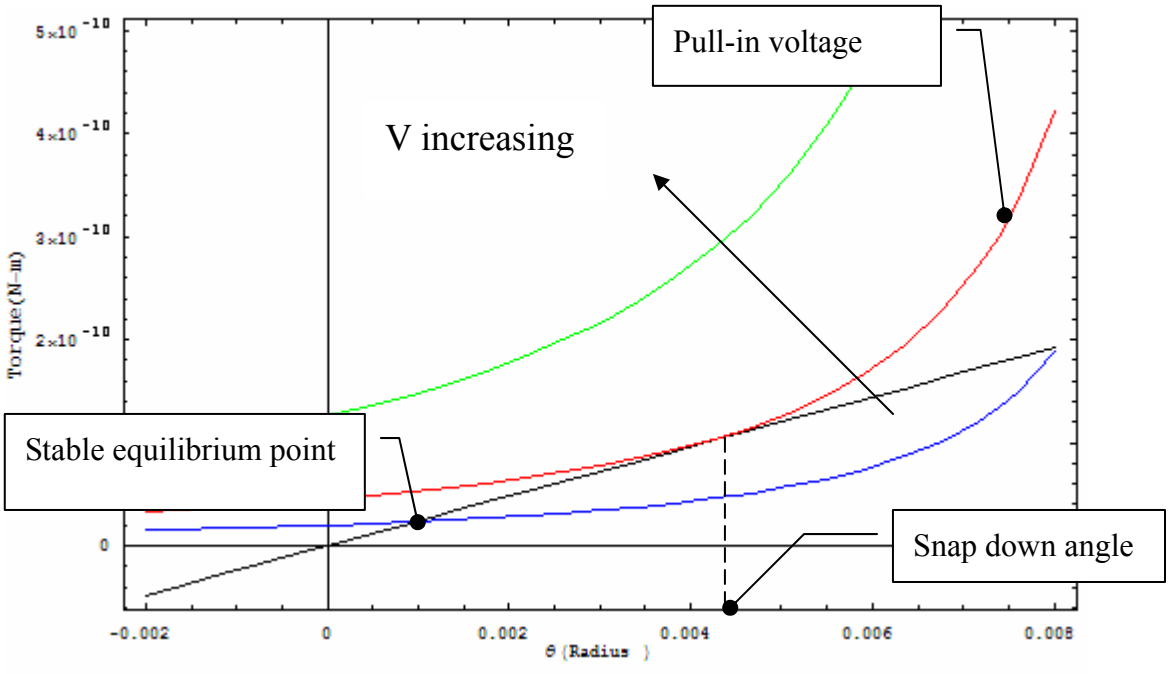


Fig. 4 Electrostatic and Mechanical forces under different voltages

At the happening of pull-in, the torque from electrostatic force must be tangential to the torque form mechanical spring:

$$\frac{\partial M}{\partial \theta} = K_\theta = \frac{T}{\theta} = \frac{M}{\theta} \tag{10}$$

$$\frac{(a-b)g\theta[3g^2 - 4(a+b)g\theta + 5ab\theta^2]}{(g-a\theta)^2(g-b\theta)^2} = 3\ln(\frac{g-b\theta}{g-a\theta}) \tag{11}$$

The above equation can be solved for the snap down angle θ_s. Furthermore, the pull-in voltage can be obtained from Eqn.(6).

$$V_{pull-in} = \sqrt{\frac{K_\theta \cdot \theta_s^3 (g - a\theta_s)(g - b\theta_s)}{\varepsilon w[(b-a)g\theta_s - (g - a\theta_s)(g - b\theta_s)\ln(\frac{g - a\theta_s}{g - b\theta_s})]}} \quad (12)$$

In our MEMS logic gate design, the applied voltage must be larger than pull-in voltage ($V > V_{pull-in}$) to ensure the plate could snap down to the input electrode and thus make contact to the output pads. Therefore, the pull-in voltage is one of the most important design parameters to ensure the proper operation of the proposed logic gate devices.

4. Damping Coefficient

The damping coefficient and the moment of inertial, as shown in Eqn. (1), can be calculated form the dimensions of the proposed device. From the linearized Reynolds equation the damping coefficient for a rectangular plate can be derived as $d\delta = \gamma / h^3$, where $\gamma = \frac{3\mu_e A^2}{2\pi}$ is a constant and depends on the geometry of the mainplate and the velocity of the gas, A is the area of the device, h is the gape, and μ_e is effective viscosity(See Appendix 3). The damping coefficient can be calculated as follows:

$$\delta = \gamma \int_{-L}^{L} \frac{|x|}{(g - x\theta)^3} dx$$

$$= \frac{3\mu_e A^2}{2\pi} \frac{L^2(g^2 + L^2\theta^2)}{g(g^2 - L^2\theta^2)^2} \quad (13)$$

where L is half length of the main-plate.

As it is shown in the equation, the damping coefficient is also dependent on the angle of the tilted plate.

II. Preliminary Design of MEMS Logic Gate

According to the performance requirements specified on most of the related reports, the proposed logic gates are designed to meet four performance requirements:

1. The proposed MEMS logic gate should perform the same function as of solid state logic gates.

2. The proposed MEMS logic gate should have the same mechanical (physical) structure and perform different logic functions by different electrical configurations. This approach is to reduce the fabrication complexity which is the same ideology as the development of solid state logic gate devices.

3. The operation voltage is less than 10 volts in order to be integrated into other IC devices in the future.

4. The switching speed is fast enough to cope with 20k Hz operation.

The concept of MEMS logic gate is a structure with five terminals similar to OP. In order to generate logic function by a mechanical structure, we design a moving plate that can tilt to the right or left depending on the various input voltage configurations. By applying a voltage larger than the “pull-in” voltage to the input terminal, the plate will snap to the output terminals on the right or left and thus make contacts at pads and thus voltage output.

Fig. 5 plots the torque for electrostatic force and torque from mechanical spring under various plate angles. The 3 lines represent torque with the input voltage

configurations (1,1), (1,0), (0,0), and the oblique straight line indicates the mechanical spring torque. To ensure the "pull-in" phenomenon happen, the straight line of mechanical torque should be bounded by the curves of electrostatic torque as showed in Fig. 5 .If not, the plate will stay at an equilibrium point without touching any output pads due to the torque balance between mechanical and electrostatic torques.

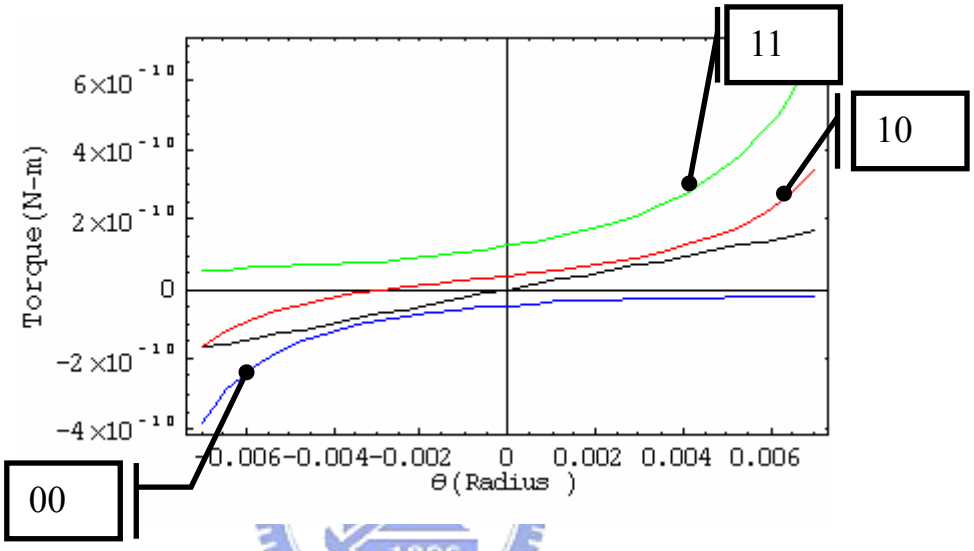


Fig. 5 Electrostatic and mechanical torque vs. plate angle θ

Another possible problem is that if a NOR gate operate, the torque distribution is shown in Fig. 6, would switch from (0,0) to (1,0). The NOR function with (1,0) input needs a positive torque to rotate the main-plate clockwise and then supply the signal "0" to output terminal. However, if the gap between plate and input electrodes is not designed properly, the (1,0) input voltages can only provide negative torque and thus the plate is mal-functionary, as the dot arrow shown in Fig. 6.

One of the solutions to the problem above is to have the dimple structures to control the range of rotation angle. Plus we can simultaneously minimize "stiction" between moving plate and output pads from happening by using dimple structures here.

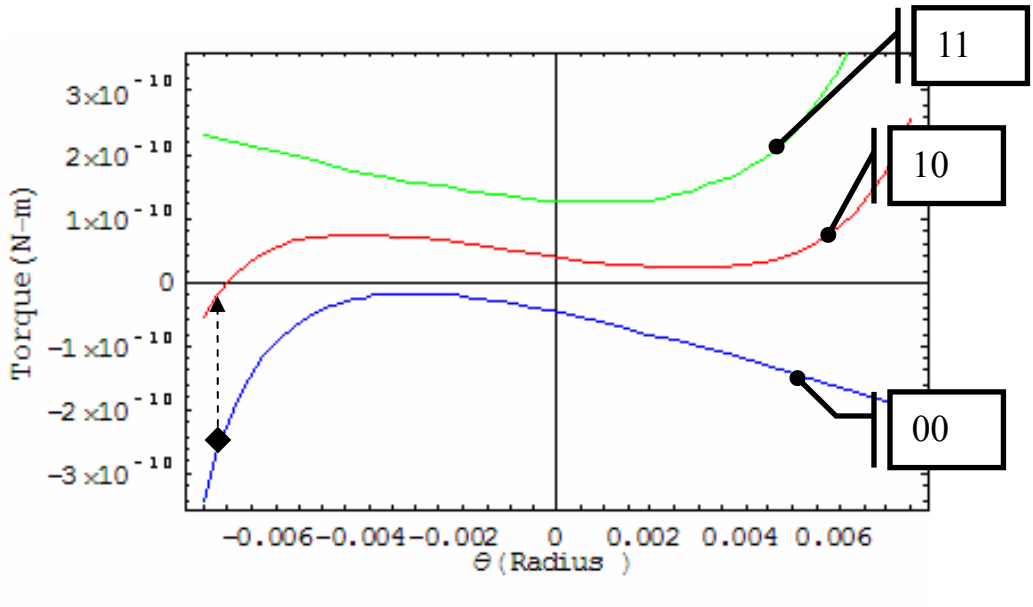


Fig. 6 Sum of electrostatic and mechanical torque vs. rotation angle

From this simulation result, we know that the proper range for the plate angle is -0.006~0.006. From previous discussions, we can design the proposed logic gate dimensions along with material properties in Table 2.

Table 2 System parameters

Density of Poly-Silicon	ρ	2230 kg/m^3
Young's Modulus of Poly-Si	E	160 G Pa
Passion ratio of Poly-Si	ν	0.22
Length of the mainplate	$2L$	250 μm
Width of the mainplate	W	100 μm
Thickness of the mainplate	t	3 μm
Length of each spring	l_{spring}	54 μm
Width of spring	w_{spring}	3 μm
Original gap	g	1μm
Width of each electrode	w	38μm
Inertial moment of the mainplate	J	8.71219×10^{-19} kg- m^2
Total torsional spring constant	K_θ	2.4×10^{-8}
Total spring constant in z-axis	K_z	40.65 N/m
Applied voltage	V	10 volt
Mechanical resonance frequency	ω_0	26.415k Hz
Location of electrodes from the rotation axis (in Fig.3)	a	50 μm
	b	100 μm
	c	85 μm
	d	100 μm

Chapter 3

Simulation Results

Because of the equations we derived before are just simplified 1-D model, an FEM solution used to check and mutually proof is quite essential. Here we'll use the software **Coventorware2004** as our tool to verify the key parameters, such as resonance frequency, pull-in voltage, damping coefficient, logic functions, multiple switching under different inputs, and so on.

1. Meshing of the device

For different meshing sizes of the devices may generate entirely different results in FEM analysis, so we have to make sure that if the simulations are worthy. Therefore, we can't stop varying meshing sizes and comparing the results until the computation converges to a value. Fig. 7 illustrates the meshing size used to analyze.

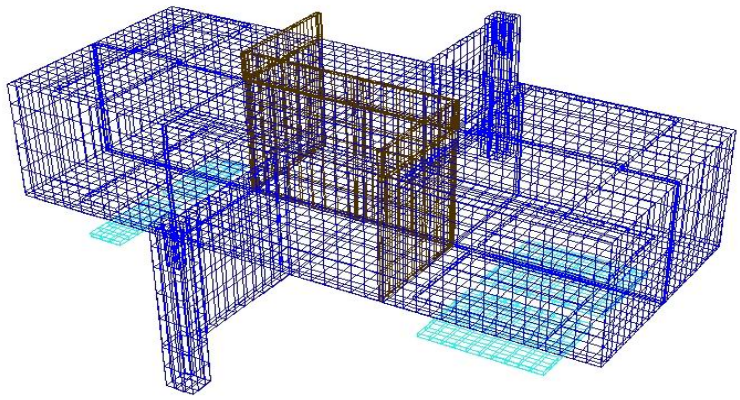


Fig. 7 Meshing of the plate for FEM-model analysis

2. Resonance modes

Modes analysis is used to check if different modes of the system are too close, if certainly, they will be easily excited together. Such the system will not satisfy our required. We need the gate with band width 20k Hz at least, and the 2nd mode of the gate is far away from the 1st one.

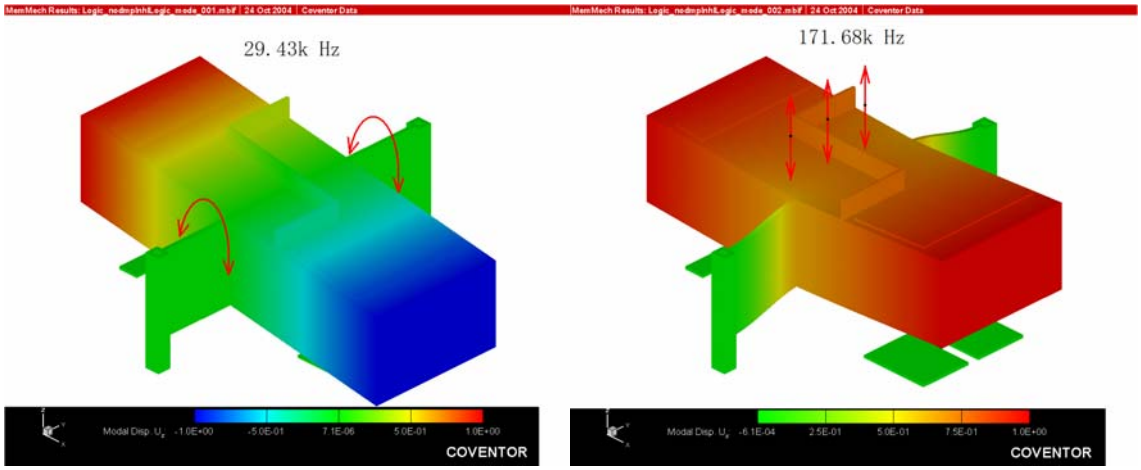
modeDomain

modeDomain	Frequency	Generalized Mass	Damping
1	2.943812E04	5.553956E-11	0.0
2	1.716865E05	1.141705E-10	0.0
3	1.939980E05	1.680641E-10	0.0
4	1.986592E05	6.487567E-11	0.0

Close

Fig. 8 Frequency for each mode of zero damping

The resonance modes of the main-plate have been studied using the **MemMech** simulation of **CoventorWare2004**. The meshing of the simplified devices structure by meshing tool is shown in Fig. 7.



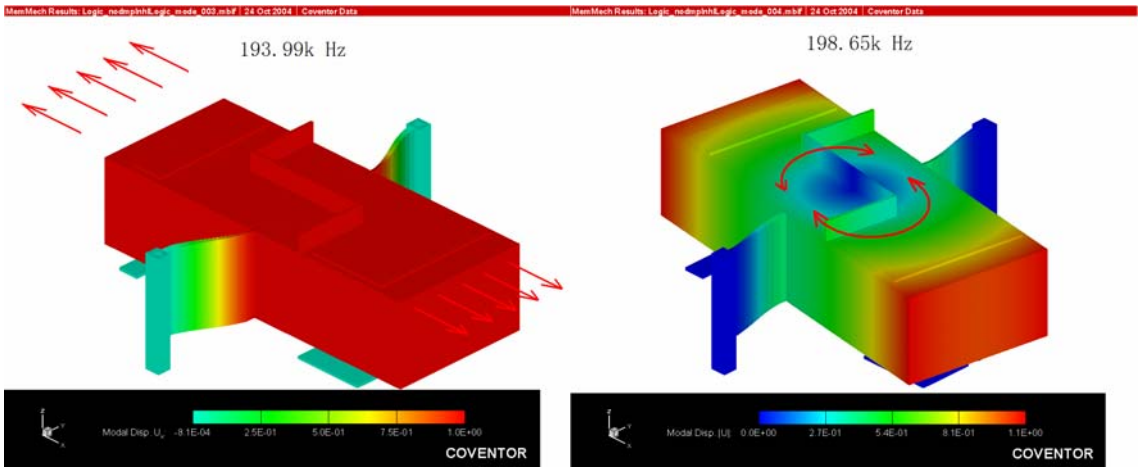


Fig. 9 Mode shapes from 1st to 4th mode

The results seem to imply that if we want other modes far away from the 1st one, their constraint should be much larger than 1st mode.

3. Logic functions of the device (NOR function)

We use CoventorWare to simulate the torsion of the device under different input signals. As Fig. 2.1, 2.2, 3 and Table 1 shows, the NOR gate should rotate counterclockwise under the input signal “0 0” and rotate clockwise under other inputs. Fig 10 shows the NOR gate operating under all situations from original state, and then we can sense signal at the output pads.

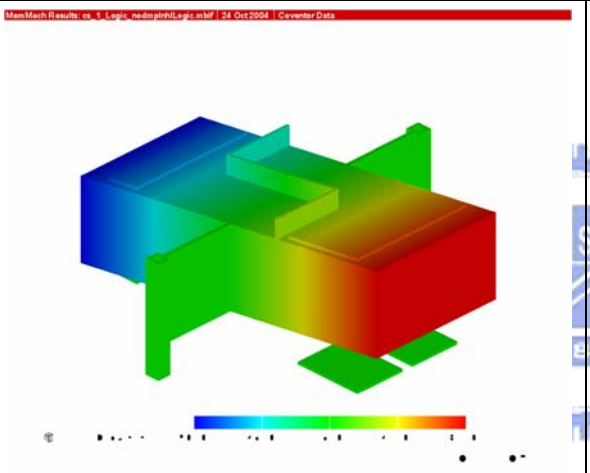
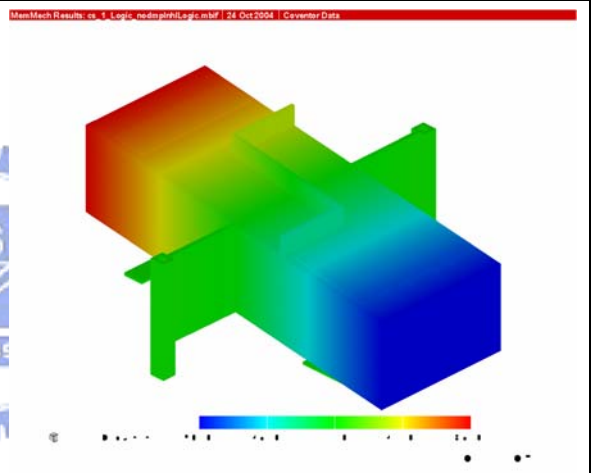
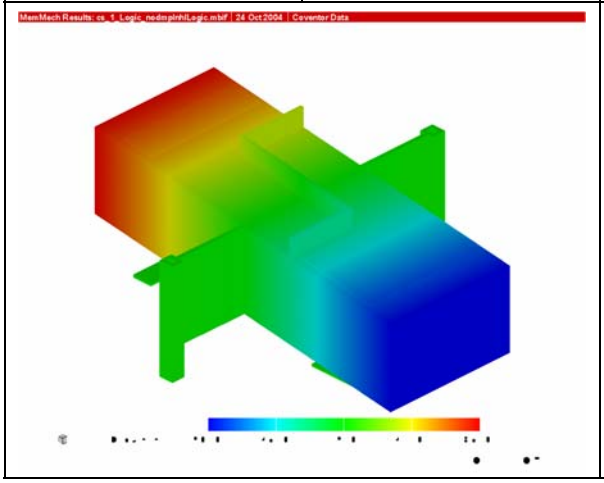
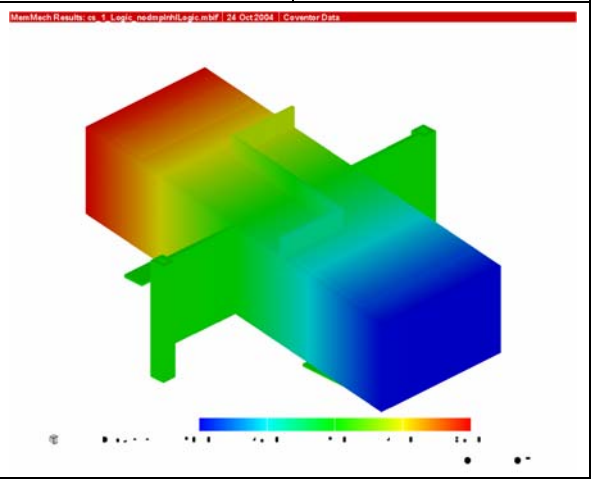
A=0	B=0	A=1	B=1
			
A=1	B=0	A=0	B=1
			

Fig. 10 Deformation of NOR gate under different input signals

4. Multiple runs for inputs one by one

Multiple simulations are quite essential for switching. For NOR gate, from the state 00 to state 10 the electrostatic torque might not pull back the main-plate if the rotation angle is smaller than -0.006 as Fig. 11 shows. The multiple simulation is used to check the switch won't fail when state translating.

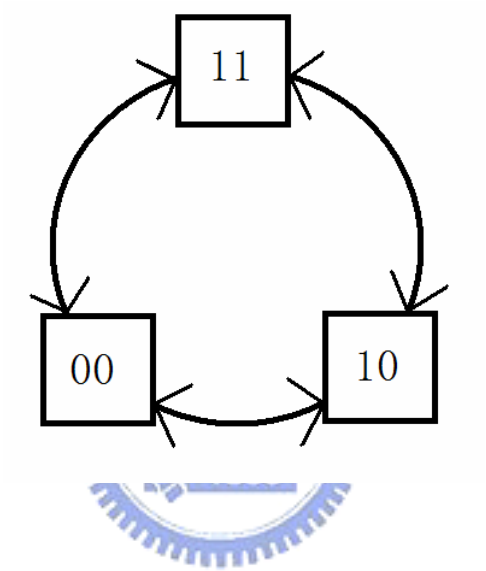


Fig. 11 Check if the gate fail from any state to others

Chapter 4

Fabrication Process and Problem discussion

I. Fabrication Process

The devices are fabricated in surface micromachining technology using standard silicon wafer as substrate. Figure 12 is the layout diagram of MEMS Logic Gate, and Fig 13 is the cross-section profile along lines A-A' and B-B'.

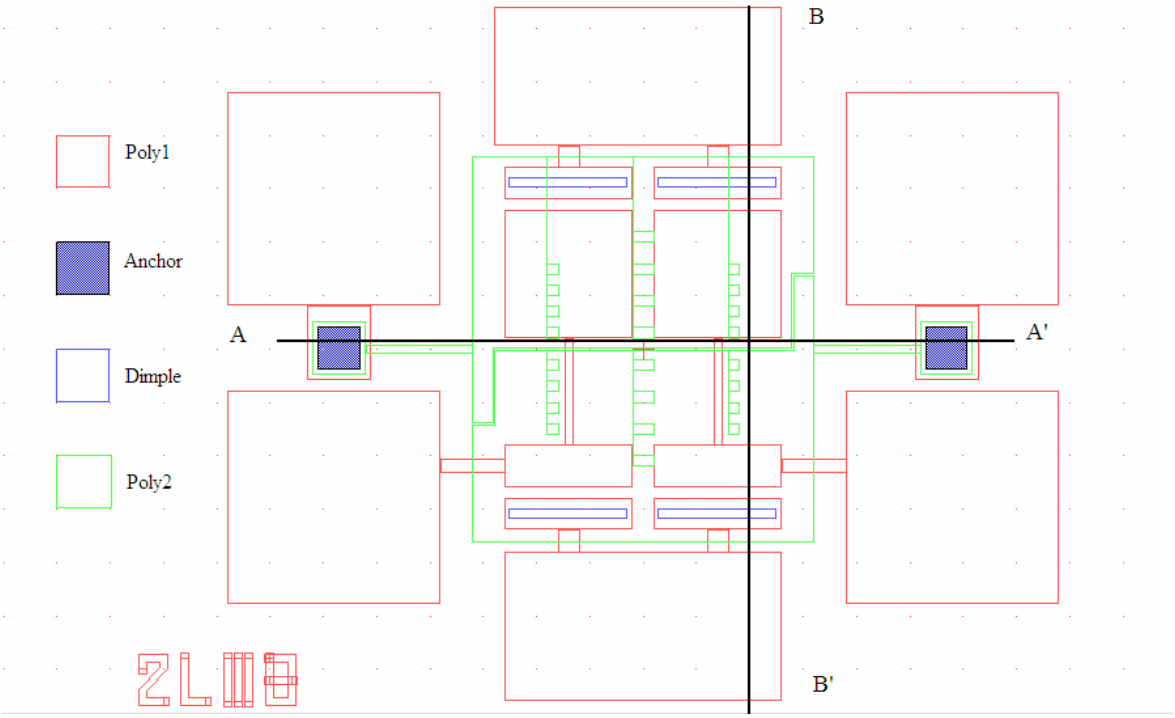
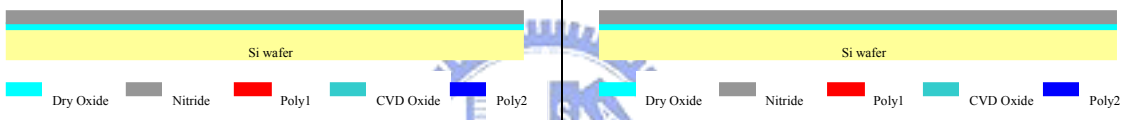


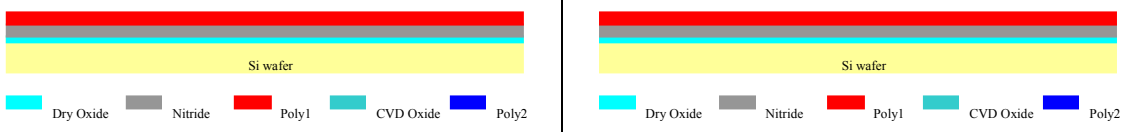
Fig12. Layout diagram of MEMS Logic Gates

Step1:Deposite dry oxide by furnace

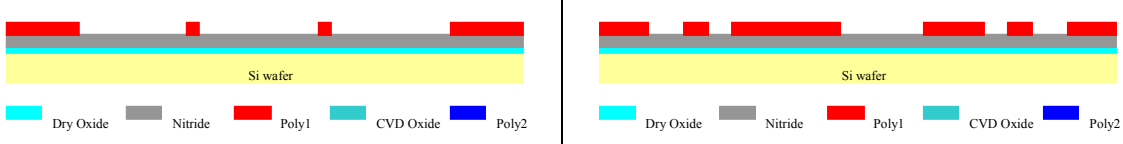
Step2: Deposit nitride by LPCVD



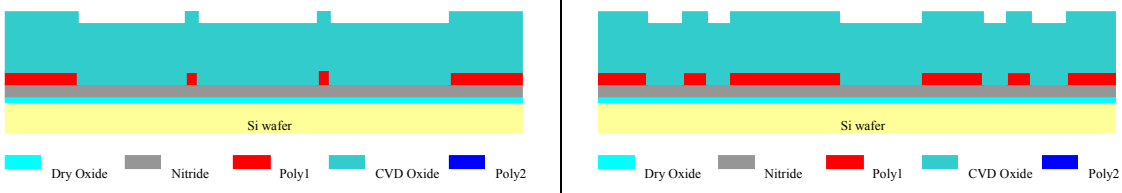
Step3: Deposit dopy poly1 by vertical furnace



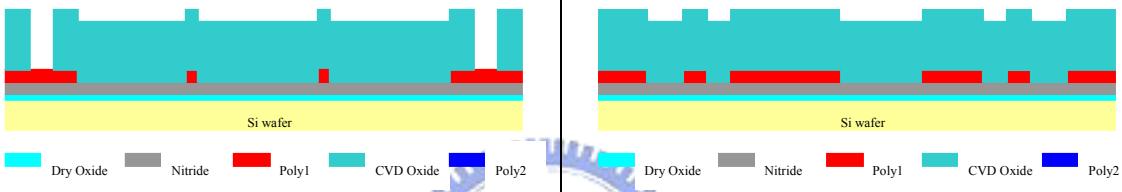
Step4: Etch dopy poly1 (Mask #1) by TCP Poly-Si Etcher



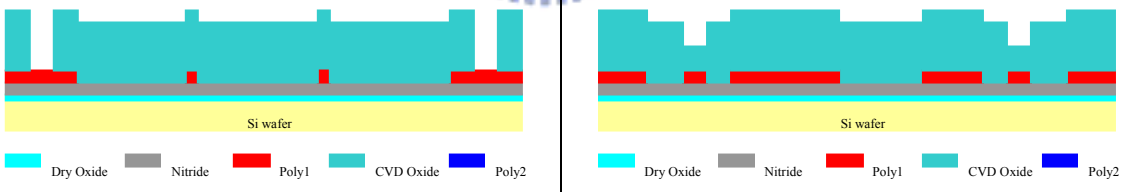
Step5: Deposit TEOS oxide by LPCVD



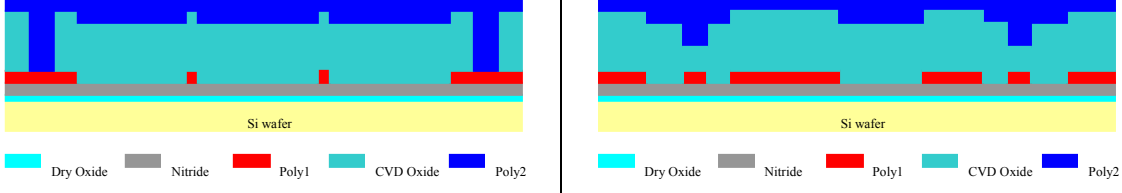
Step6: Dry etch poly1 (Mask#2) by Oxide Etcher to form the anchors



Step7: Dry etch poly1 (Mask#3) by Oxide Etcher to form the dimples



Step8: Deposit dopy poly2 by vertical furnace



Step9: Dry etch dopy poly2 (Mask#4) by TCP Poly-Si Etcher

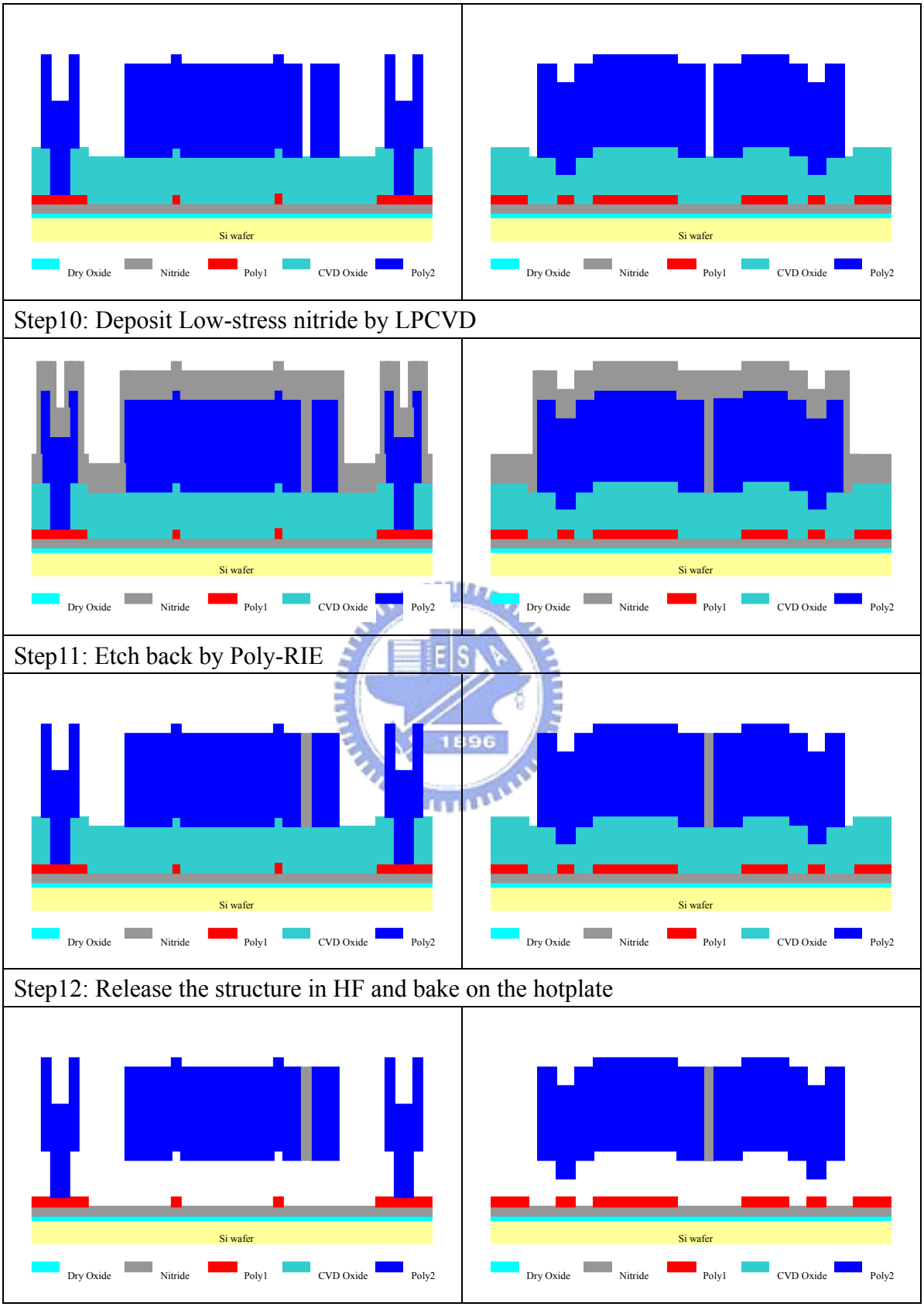


Fig.13 Cross section of MEMS Logic Gates

Step1. Use standard RCA cleaning process to clean the bare wafers, and then deposit dry oxide layer 350 A° thick in furnace as buffer layer.

Step2. Deposit nitride 1000 A° thick in LPCVD as isolation layer.

Step3. Grow dopy poly 3000 A° thick in vertical furnace.

Step4. Lithograph dopy poly1 with Mask #1 and dry etch in TCP Poly-Si Etcher as actuation electrodes and leading wires.

Step5. Deposit TEOS oxide 1μm thick in LPCVD as sacrificial layer.

Step6. Lithograph TEOS oxide with Mask #2 and dry etch 1μm deep in Oxide Etcher as anchor holes.

Step7. Lithograph TEOS oxide with Mask #3 and dry etch 0.5μm deep in Oxide Etcher as dimples.

Step8. Deposit dopy poly 2.2μm thick in vertical furnace to form the structure layer.

Step9. Lithograph dopy poly with Mask #4 and dry etch 2.2μm deep in TCP Poly-Si Etcher to shape up the devices.

Step10. Deposit nitride 0.7μm in LPCVD to fill the trench of each device.

Step11. Etch back 0.7μm to remove the unnecessary nitride by Poly-RIE.

Step12. Release the structure in HF etchant and bake wafers on hotplate.

II. Problems and discussion

In this section, the problems encountered during fabricating and solutions for each case will be indicated.

1. Lithography of thick PR

In order to resist the deeply poly silicon etching , enough thickness of PR is necessary. But it's hard to control lithography by manual control equipment for thick PR. Properly developing for the device's springs is incomplete for the trench, yet the appearance of trench is the over-developing for spring as Fig 14 indicates. In order to solve this problem, we plan to divide the device pattern into two masks such as sheet area pattern mask and spring line pattern mask respectively. Therefore, we can control the lithography parameters much easier.

Besides, the uniformity of lithography is another problem. After developing, there was a slight difference of patterns on each die of the wafer. On some parts of the wafer, the patterns did not develop completely due to underexposure. On the other parts, the patterns disappeared because of overexposure. See Fig. 15. We think that there are two possibilities about the uniformity. One is to assume that the warping of the wafer due to multiple depositing process and etching on one side of the substrate. In the contact printing process, the mask makes direct contact with photoresist on the wafer. However, because of the warping of the wafer, only a few points on the wafer really make direct contact with the mask, and most areas on the wafer surface have air gap between the mask and PR. We might solve the problem by both-side etching to balance the stress and get flatter substrate. Another possibility is the uniformity of UV light, and this remains to be solved.

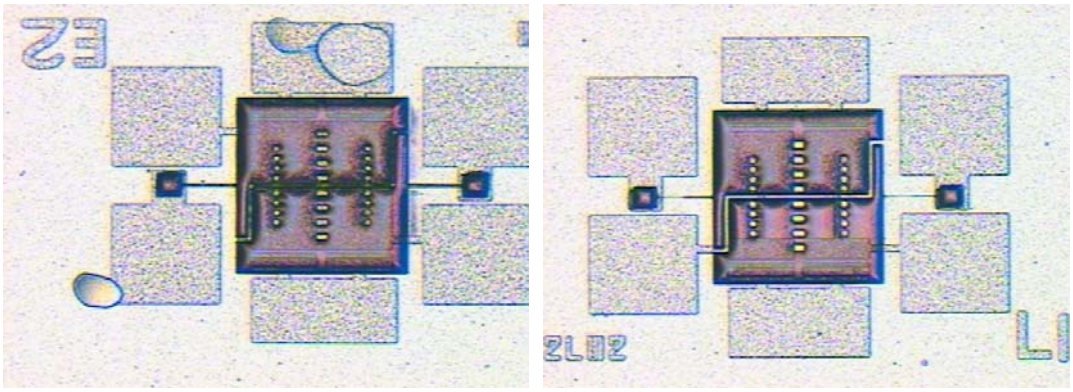


Figure 14 Poor space and line lithography

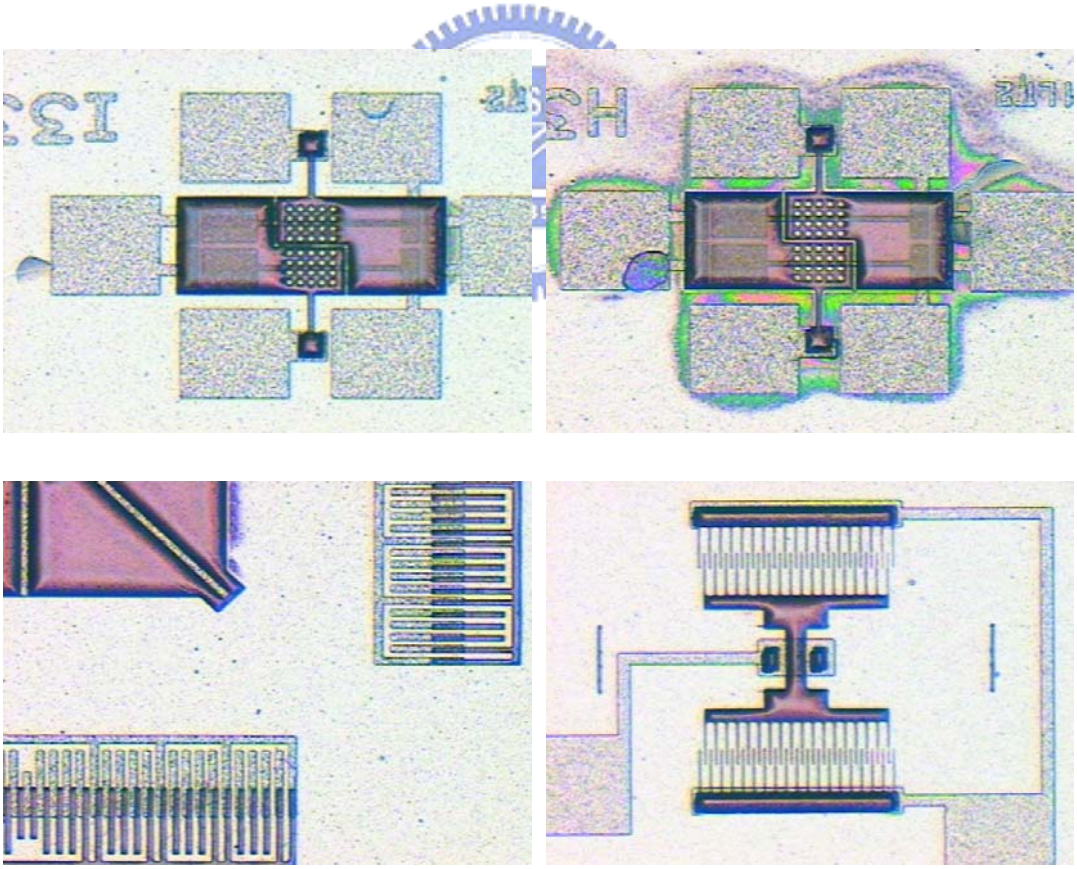


Fig 15 Poor uniformity in different regions on the same wafer

2. Cracks and curls of nitride

In the cause of isolating two parts of the logic gate, deep trench on 2nd poly silicon and fill it by insulating materials is necessary. We deposit 0.7μm thick nitride film by furnace and LPCVD in NDL first, and expect the conformal growing will fill up 1μm wide-2.2μm deep trench perfectly. But the internal stress of high temperature growing nitride causes the cracks in each die and curls in surroundings. The results are printed in Fig.16. For the following convenience, we use SC1 cleaning process to remove the curls outside the die. However, we have the awful spreading of the cracks. SC1 etchant can also attack oxide layer and then causes roughness and fractures on every die as Fig17 shows.

In order to overcome the film crack problem, we use LPCVD in SRC and PECVD in NDL to deposit low stress nitride individually. Figure 15 indicates the results after film growing, and by OM we can see that there are no cracks. This is because low stress silicon nitride typically has a tensile residual stress below 50MPa, and allowing its use in micromachining as a free standing film.

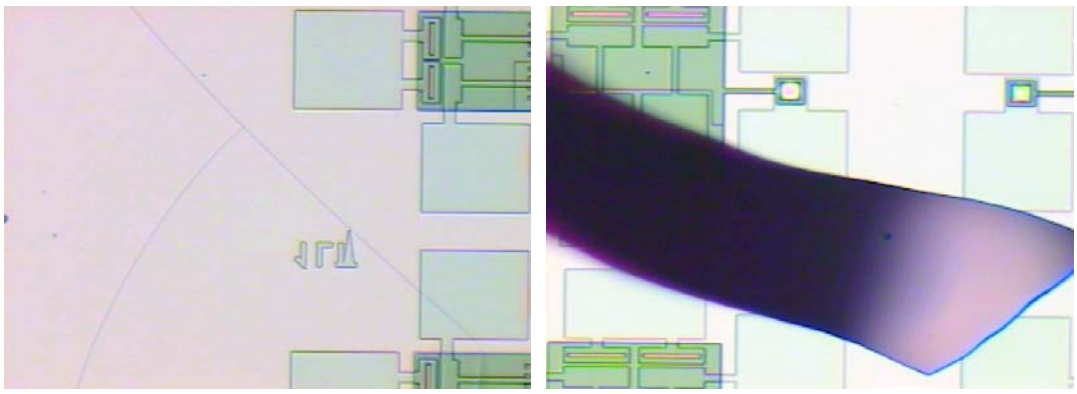


Fig16 Cracks and curls of the nitride film

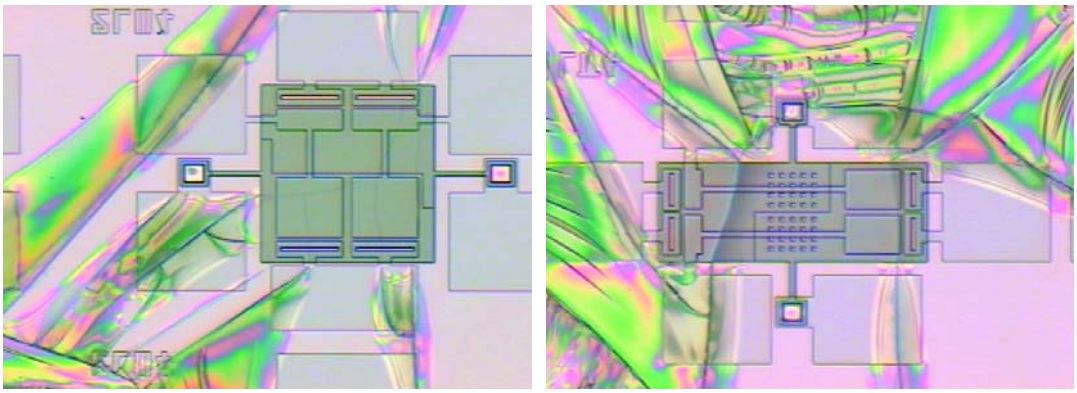


Fig.17 Spreading of the cracks after SC1 cleaning

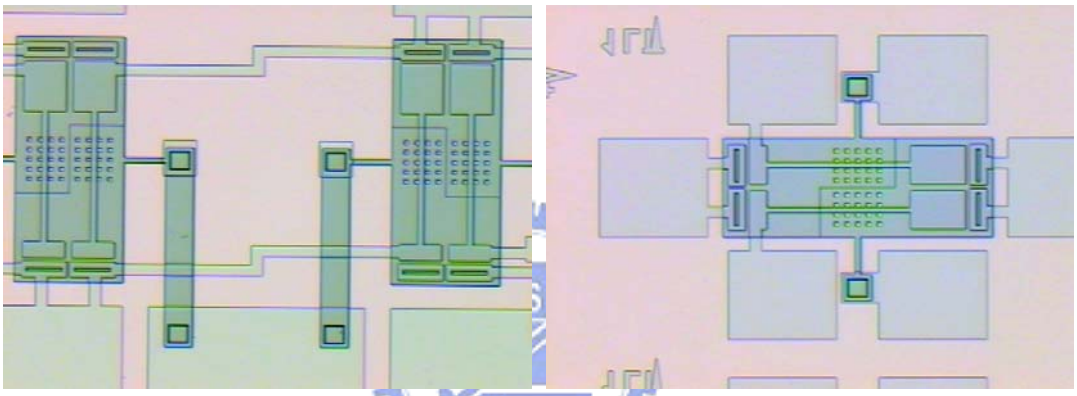


Fig.18 No cracks after LPCVD and PECVD low stress nitride growing

3. Over etch

Because of insufficient etching holes on the structures, more time for releasing oxide is needed. However, HF etchant will also attack nitride isolation layer. Such that the following undercutting of isolation nitride layer will be the peeling of touching pads (see figure 19). For example, the etching rate of 10:1 HF (10 H_2O: 1 49% HF) to silicon nitride is 11 A°/min. We use condensed HF (49% HF) to release the structure about 40 min. So, there is a possibility of over-etching from 1000A° thick nitride layer to substrate.

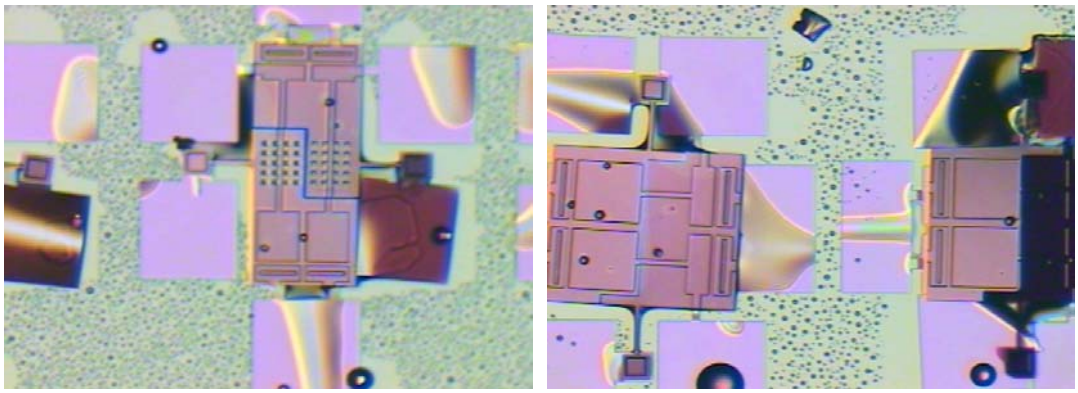


Fig.19 Peeling of touching pad due to over etching

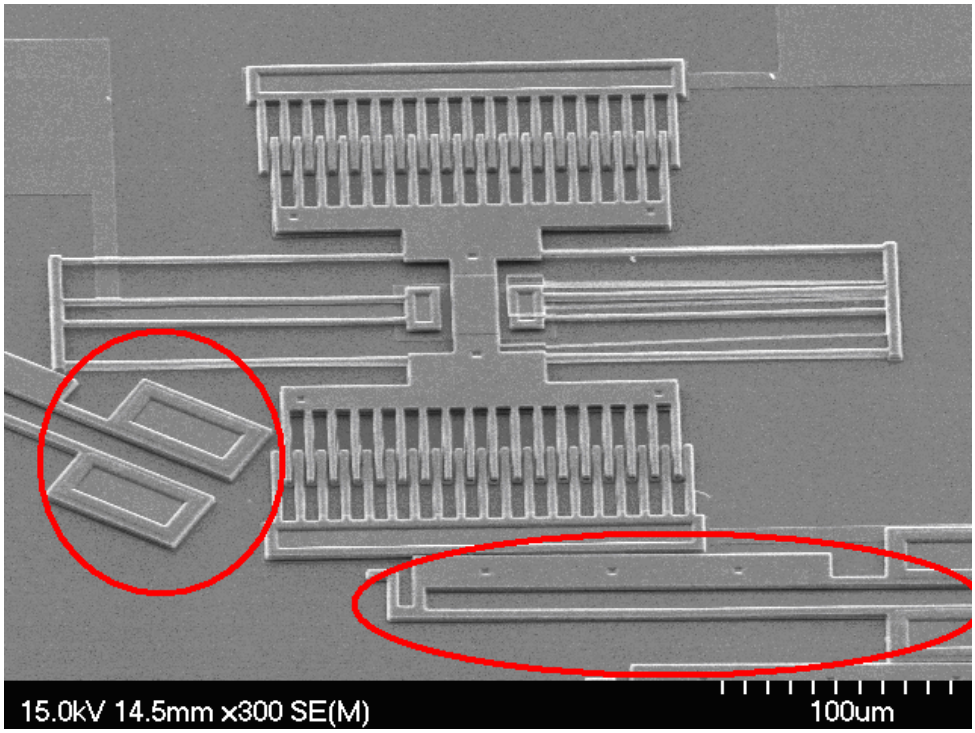


Fig. 20 Peeling of anchors due to over etching

4. Stiction

A standard HF release process is used to fully remove the sacrificial oxide underneath the structure layer. When we use the wet release etching, surface tension of liquor will pull the structures into contact with subtract, and during the final drying, they can adhere firmly together. This is the phenomenon so called “stiction” as figure 21 shows.

Methods of avoiding stiction include (1) the use of thin hydrophobic layer to reduce the attractive force, (2) the use of vapor or dry-etching release method, (3) various drying methods, such as drying with supercritical CO_2, to remove the liquid without permitting surface tension to act, (4) mechanical supports of the moveable structure such as dimples, (5) and geometry release methods “anti-stiction structures”.

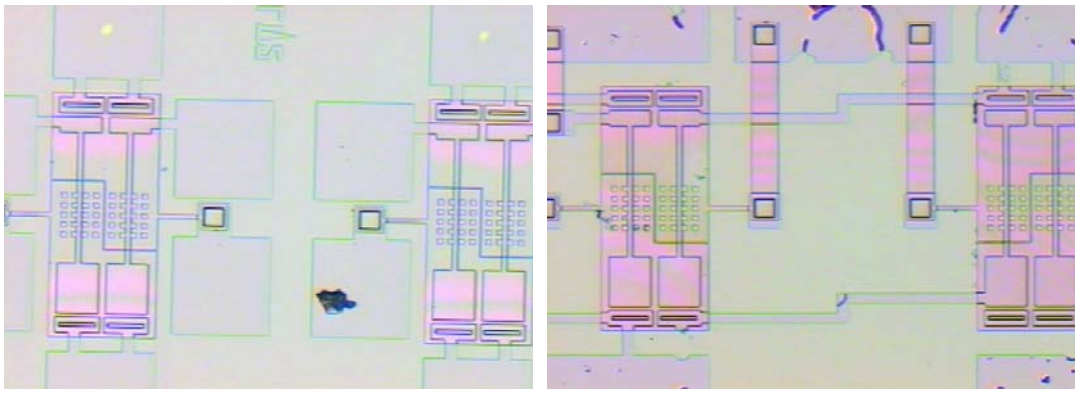


Fig21 Stiction after wet releasing

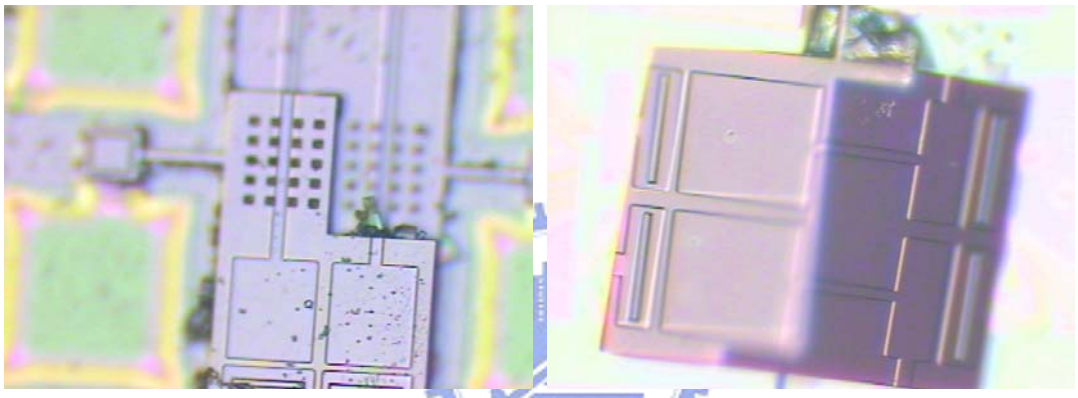


Fig.22 Stuck and folded structures due to surface tension

5. Trench filling

Well filled trench is a key point about the success of fabrication process. As figure 13 shows, isolation material is used to bind the two parts of device. Bad filling will cause inactive devices due to the separation of both parts after releasing. So we begin with LPCVD nitride, and then PECVD low stress nitride, finally LPCVD low stress nitride to fill the trench.

We star with LPCVD nitride. However, LPCVD silicon nitride cracks during growing film due to the high residual stress and thickness. LPCVD silicon nitride is usually used as

an etch mask, thermal oxidation mask, and wafer capping material due to its low permeability to moisture. To take into account the residual stress problem, we use PECVD and LPCVD to deposit low stress nitride.

The result after PECVD low stress nitride growing is shown in Fig 23, and we can see the trench doesn't be closed. This is because PECVD uses silane (SiH_4) as source material which is a perfectly symmetrical molecular, so the gas molecule will neither chemically nor physically absorb to the substrate surface. Besides, silane also has low surface mobility. For these reasons, PECVD nitride films always have overhangs at the step corners and normally have poor step coverage. We finally can see the re-opened trench after RIE etching in Fig. 24, and this will cause the failure of our devices.

And then we use LPCVD to deposit low stress nitride for the gap filling. Because of using dichlorsilane (SiH_2Cl_2) as source material, which has nonsymmetrical structure, we will have better step coverage. Furthermore, by reducing process pressure, the mean free path (MFP) of source increases. When MFP is longer than the gap depth, there will be very few collisions inside the gap. Thus, the source molecule will have little chance to go backward and reach the step corner from inside the trench. This effectively reduces the arriving angle and improves the step coverage. We can see the results after LPCVD low stress nitride depositing in Fig 25. Finally, we use RIE to etch back silicon nitride as Fig 26 indicates.

Consider the examples quoted above, we can know that LPCVD low stress nitride is not only good for trench filling but also has no crack problems.

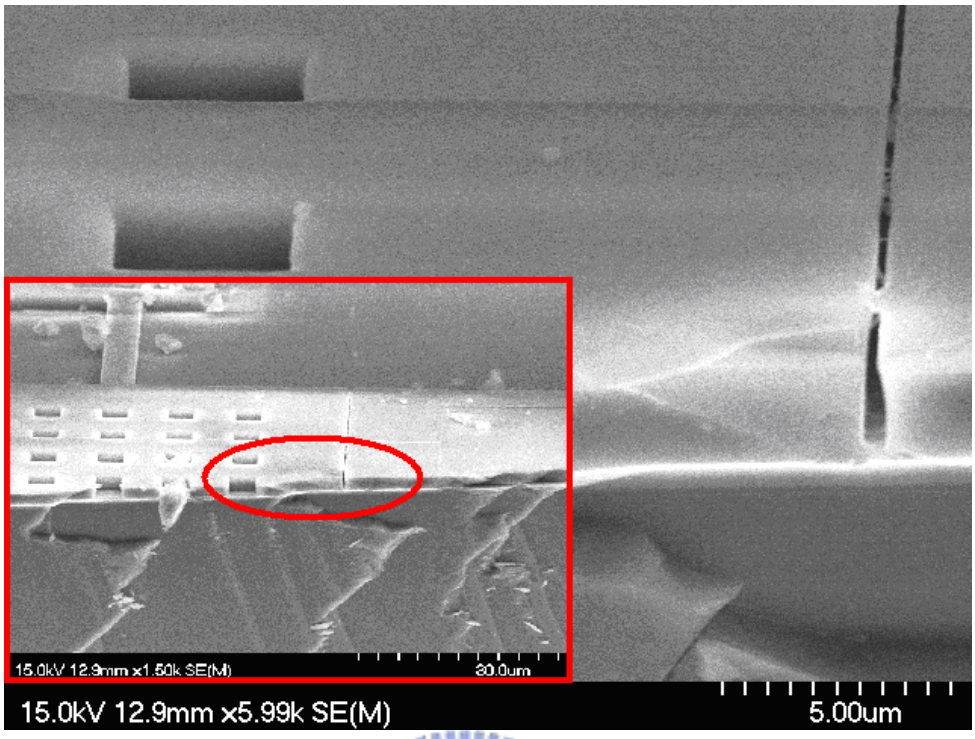


Fig 23 Bad fill of PECVD nitride before releasing

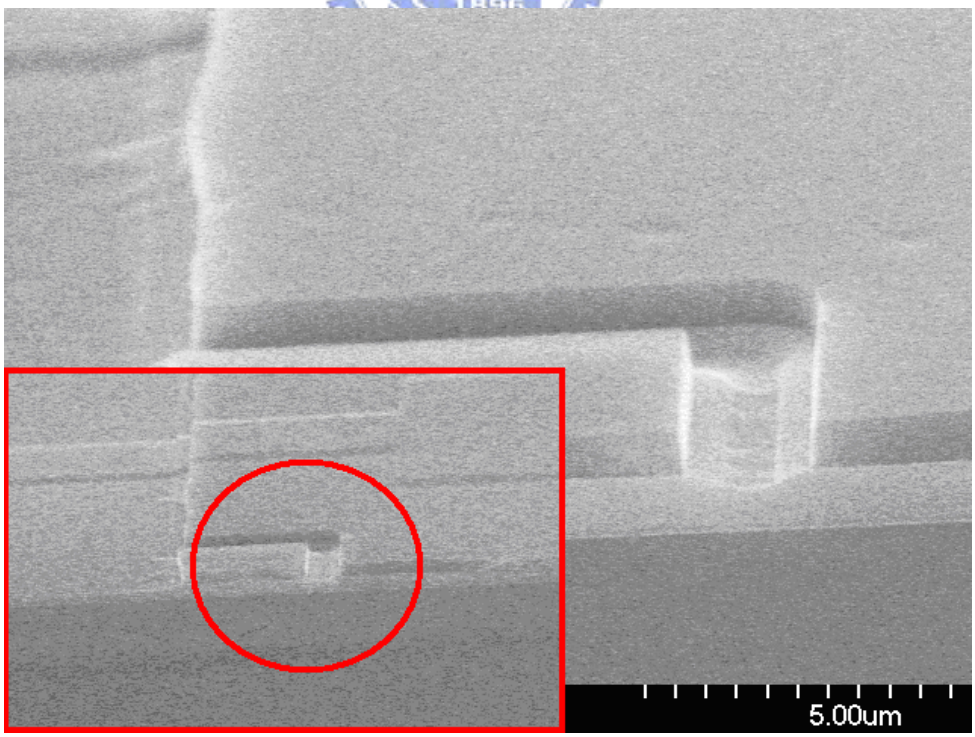


Fig.24 PECVD filled trench is re-opened and widened after etching back

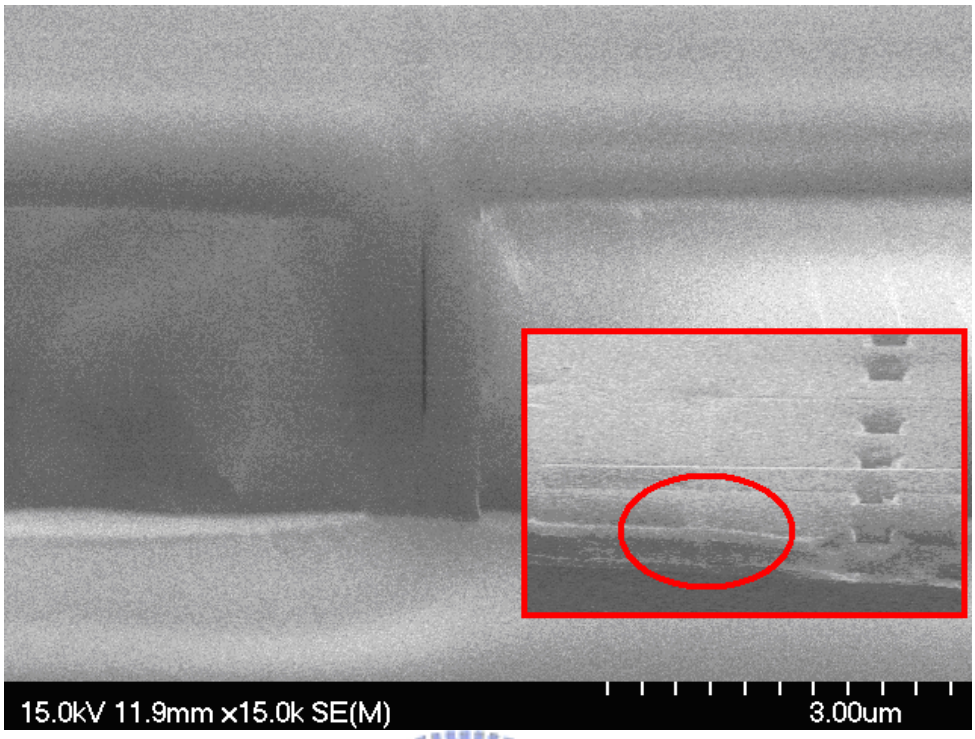


Fig 25 Better filling with of LPCVD nitride before releasing

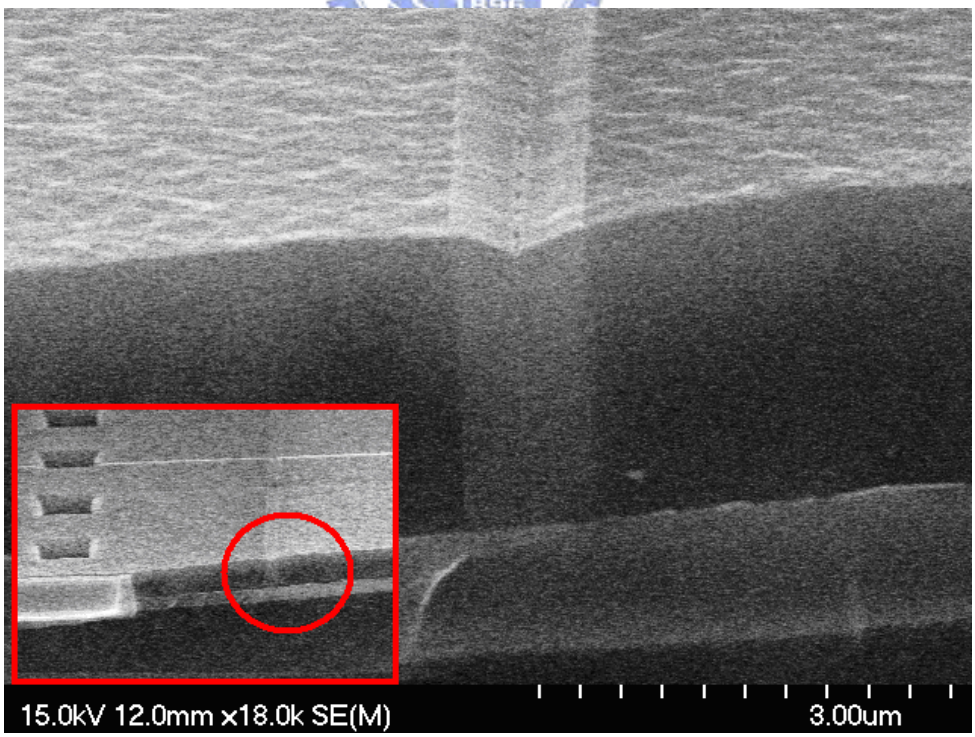


Fig.26 LPCVD filled trench after etching back

6. Sidewall nitride

Obviously we can know that LPCVD low stress nitride can fill the trench well as given in above. However, etching back not only planarizes the gap but also leaves sidewall nitride. See Fig. 27. The sidewall nitride could change mechanical properties such as spring constant and resonance frequency. Furthermore, the falling off sidewall nitride may cause the contaminations and interfere with other MEMS devices. So the elimination of sidewall nitride is necessary. We will present new process to solve the problem later.

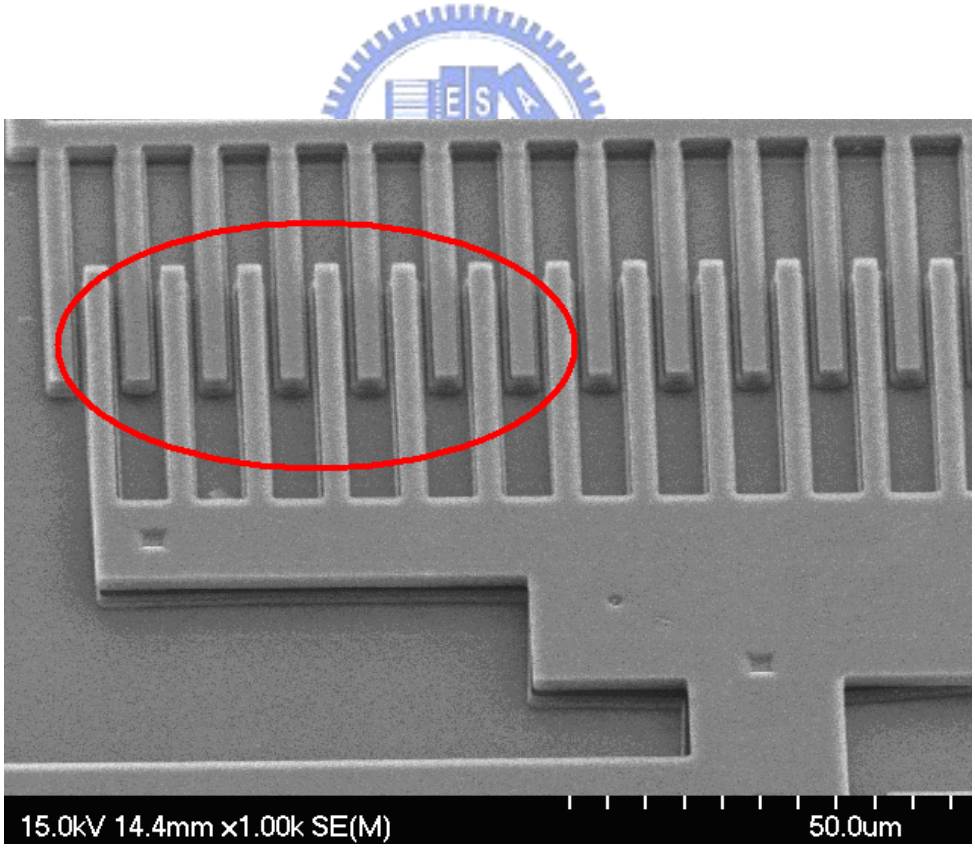


Fig27 Remaining nitride on sidewall

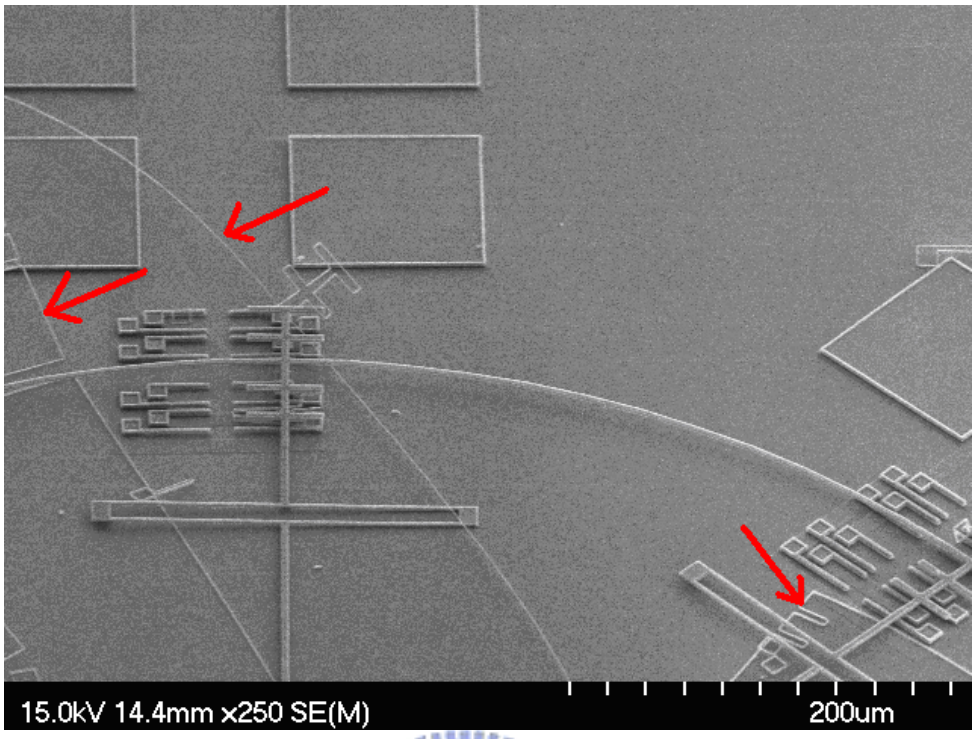


Fig.28 Falling off sidewall nitride after releasing

Conclusions

Although we couldn't finish the device in the end, we still prove the possibility of the see-saw structure. First, the newly designed mechanical structure can produce different logic functions by different electrical interconnect layouts and could be fabricated by surface micromachining. Second, we have verified the performance by software. Finally, we present a new fabrication process according to the problems we faced.

Future Work

I. Fabrication of MEMS Logic Gate

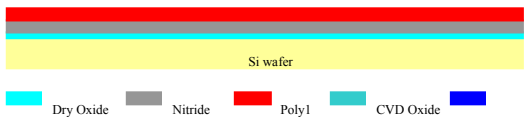
First, we'll try the new process which contains no metal and operate by poly to poly contact. And then we'll try to fabricate the devices with metal layers such that the metal to metal interface will have fewer contact resistance in the end.

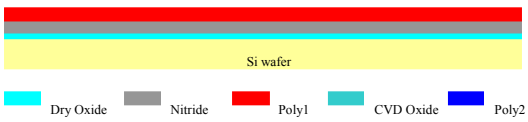
1. New Process

Due to the origin process exist some problems such as (1) the remaining of sidewall nitride, (2) voids in the filled trench, (3) too much releasing time because of insufficient releasing holes; we represent a new process to get over these.

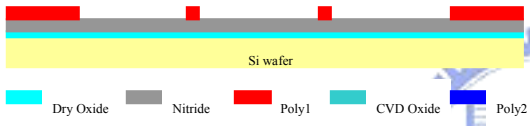
For the following convenience about releasing, space between each releasing hole is necessarily no more than 30 μ m. In addition, we only dig out the trench first and then filling it with nitride and poly in turn instead of prior process. After the later etching back, we define the shape of our devices. See step9 to step 13 in fig. 29. By the suchlike method, we neither have sidewall nitride because of nearly planar etching back, nor void in the trench due to better step coverage of poly.

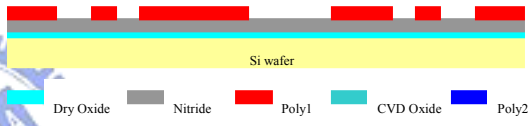
Step1~3:Deposite dry oxide/nitride/dopy poly



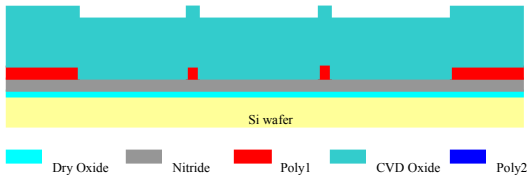


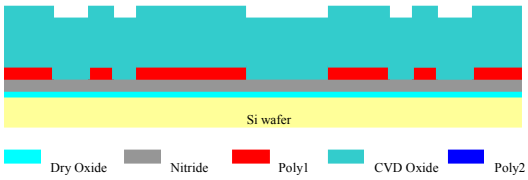
Step4: Etch dopy poly1 (Mask #1) by TCP Poly-Si Etcher



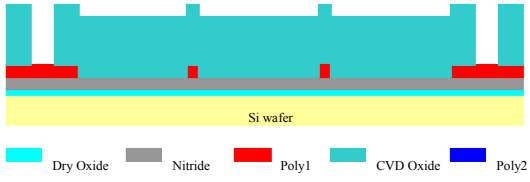


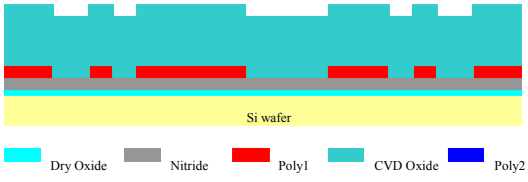
Step5: Deposit TEOS oxide by LPCVD



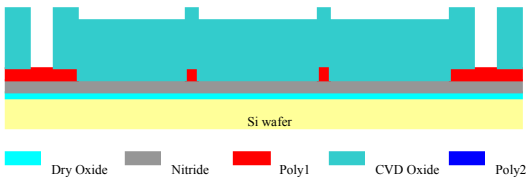


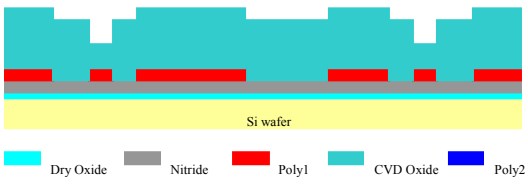
Step6: Dry etch poly1 (Mask#2) by Oxide Etcher to form the anchors



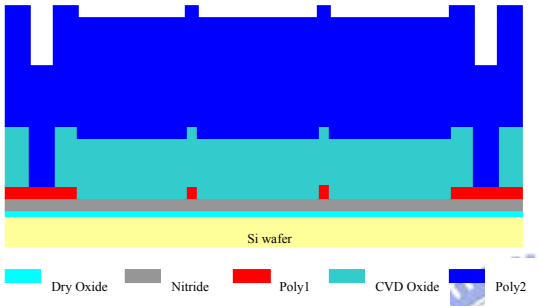


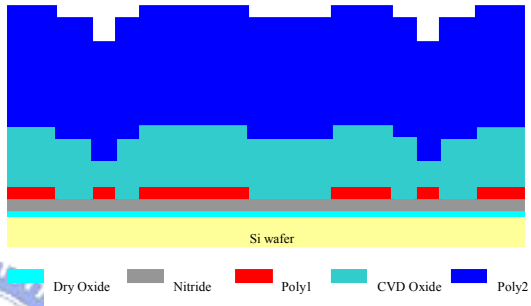
Step7: Dry etch poly1 (Mask#3) by Oxide Etcher to form the dimples



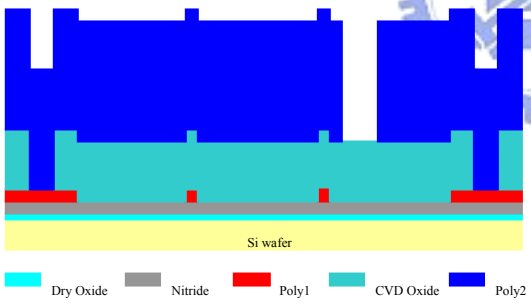


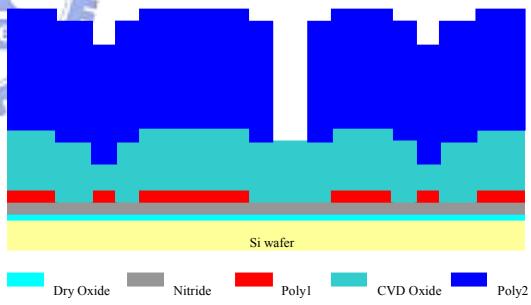
Step8: Deposit dopy poly2 by vertical furnace



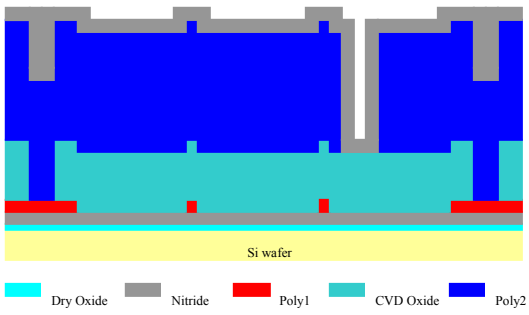


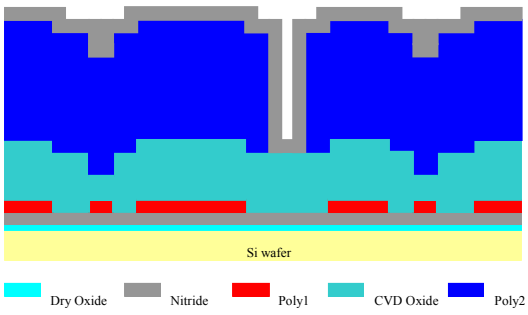
Step9: Dry etch dopy poly2 (Mask#4) to form the trench only by TCP Poly-Si Etcher



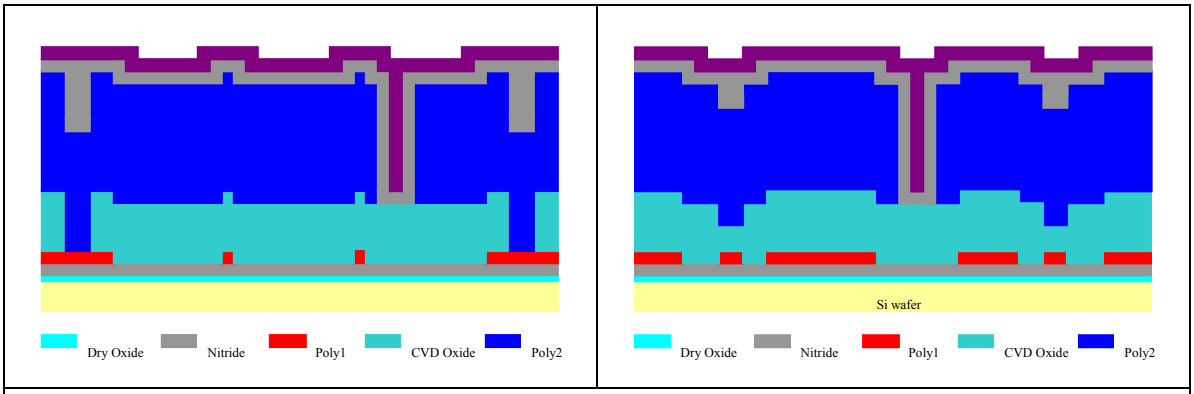


Step10: Deposit Low-stress nitride by LPCVD

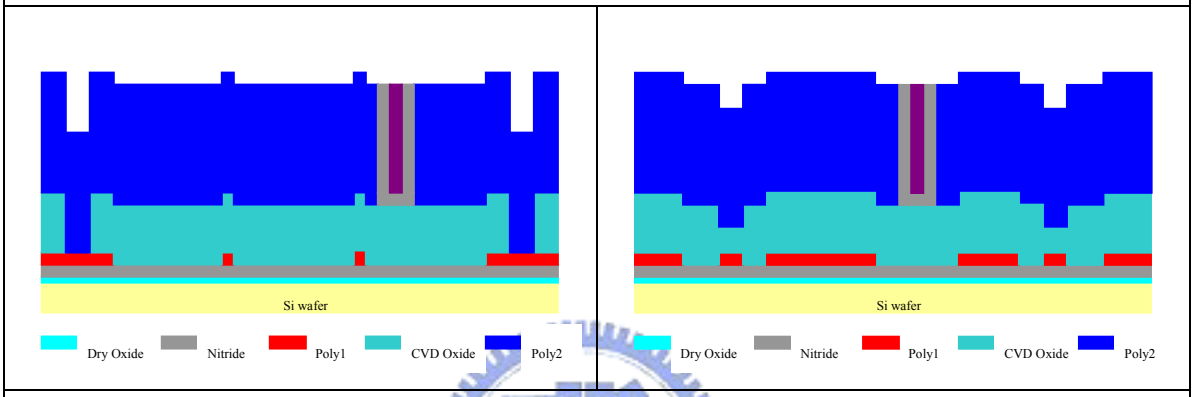




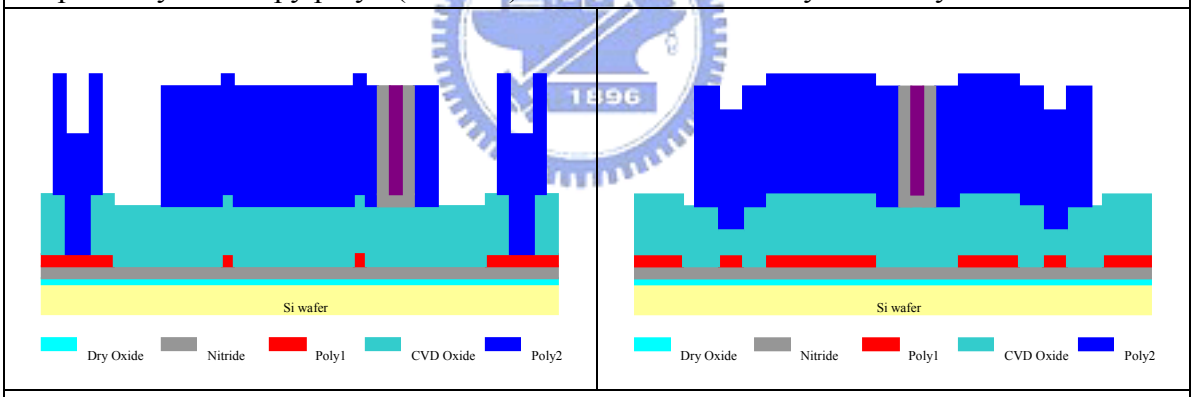
Step11: Deposit undoped poly by LPCVD to fill up the trench



Step12: Etch back to planarize the gap



Step13: Dry etch dopy poly2 (Mask#5) to define the device by TCP Poly-Si Etcher



Step12: Release the structure in HF and bake on the hotplate

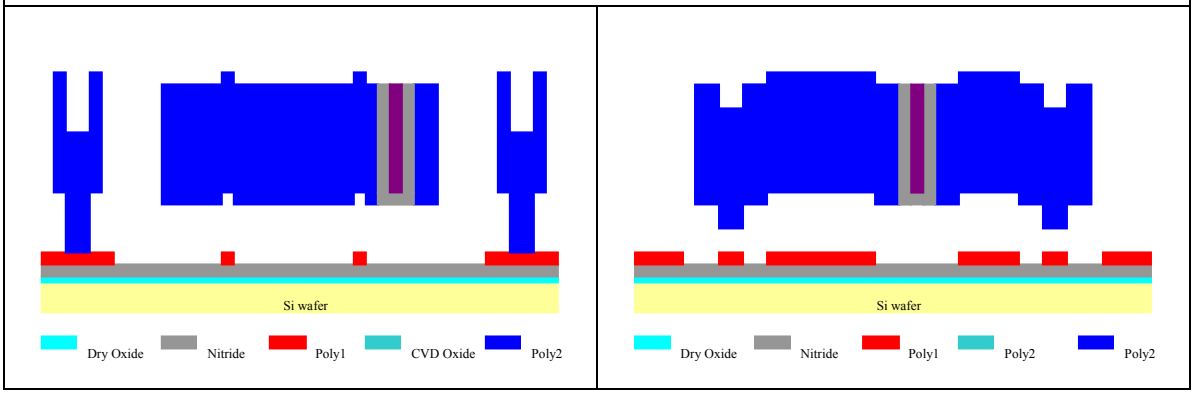
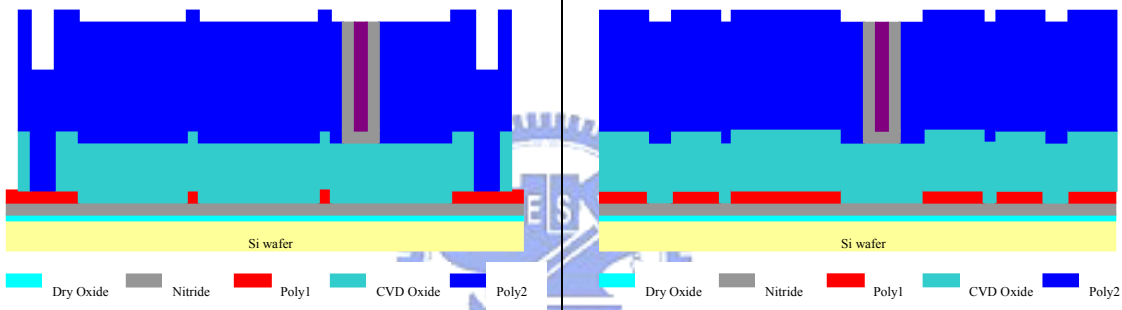


Fig 29 New process flow to fill the trench

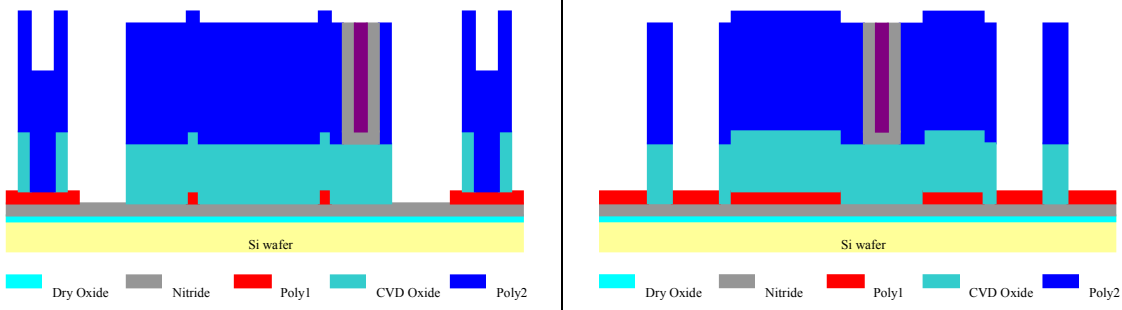
2. Metal Process

We can expect that full polysilicon-made structures will cause internal resistance problems in the device, including contact resistance at dimples and voltage drop at polysilicon leading wires. In order to reduce the contact resistance we use metal dimples as solutions. The key point of the metal process is that we use Ti as co-sacrificial layer with oxide. Such that we could release the structure in HF without etching metal Ni.

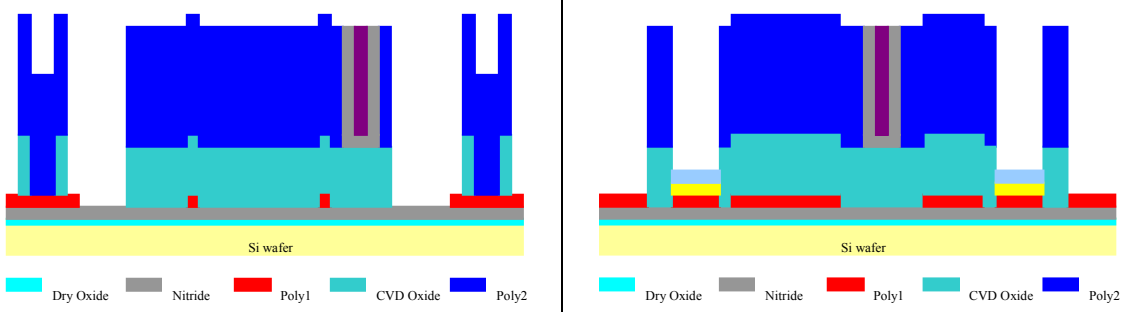
Step1~12: The same with Fig29



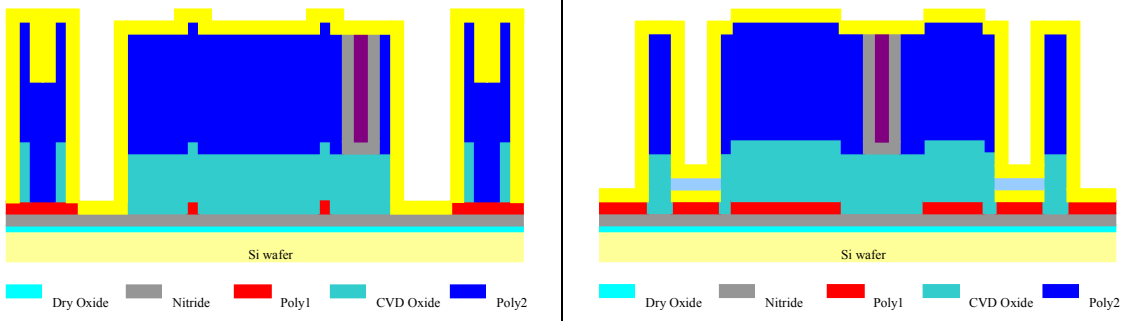
Step13: Define the device (Mask #5) by TCP Poly-Si Etcher



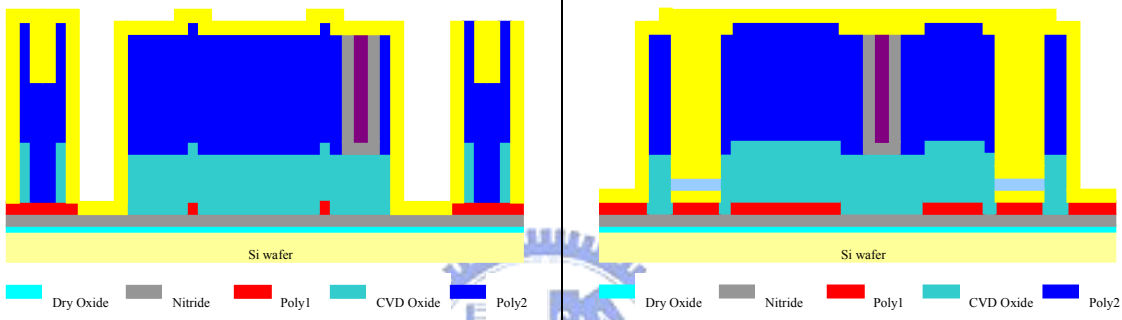
Step14~16: Deposit Ni/Ti by Dual E-Gun and then lift off (Mask #6)



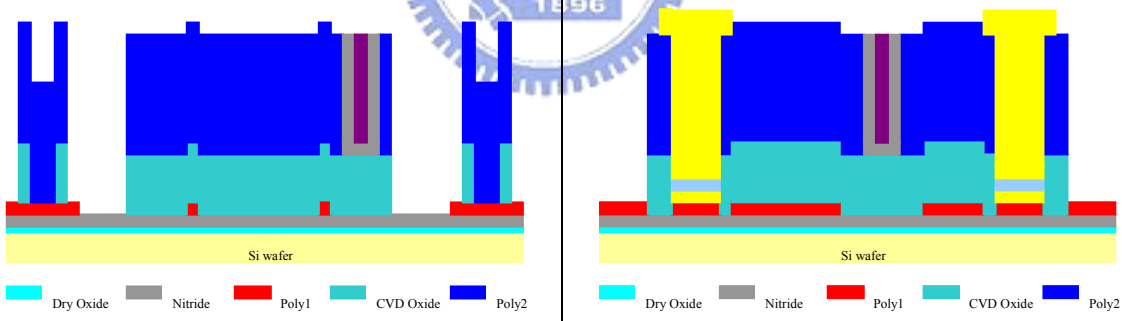
Step17: Deposit Ni on full wafer by sputter



Step18: Electroplate Ni to fill the trench up



Step19: Etch back Ni by Metal Etcher



Step20: Release the structure in HF and bake on the hotplate

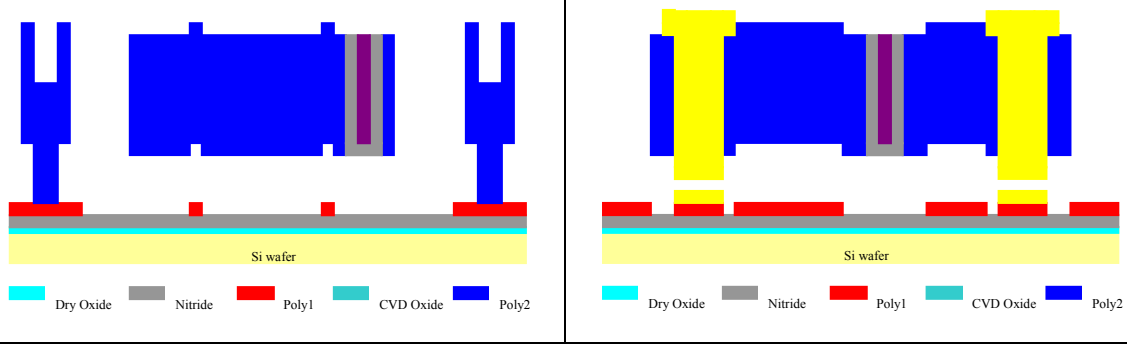


Fig 30 Metal process

II. Use the logic units to form various functions

After the success of the logic unit making, we'll attempt to realize other functions based on the basic units (NOR, OR).

III. Measure the parameters of performance

Use laser Doppler Vibrometer to determine the resonance frequency and other instruments to measure the parameters such as drive voltage and logic functions. And then compare these results to the computed ones.

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Appendix

I. Switching Time

1. At low pressure, $Q \geq 2$

Based on Raj K. Gupta and S. D. Senturia's[18][19] research, we can derive the switching time t_s from the macro model equation(Eq.1) for different situations.

At low pressure, that is for device with a small damping coefficient and $Q \geq 2$, the damping term in Eq.1 can be neglected. The equation of 1-D motion becomes ($\delta \approx 0$):

$$J\ddot{\theta} + K_\theta \theta = \mathrm{M} = const. \tag{14}$$

where the torque M is taken to be constant and equal to the initial applied torque. Solve the 2nd O.D.E., we have:

$$\theta(t) = \frac{\mathrm{M}}{K_\theta}[1 - \cos(\omega_0 \cdot t)] \tag{15}$$

At switching time is obtained using Eqn.1 and is defined when $\theta = \theta_0$, where θ_0 is the maximum torsion angle. The solution is :

$$t_s = \frac{\cos^{-1}(1 - \frac{K_\theta \cdot \theta_0}{\mathrm{M}})}{\omega_0} \tag{16}$$

2. At higher pressures, $Q \leq 0.5$

At higher pressure, the 1-D system will be damping-dominated, and the spring force will be negligible compared to the damping force, so we have:

$$J\ddot{\theta} + \delta\dot{\theta} = \mathrm{M} = const. \tag{17}$$

The same as the previous procedure, yielding:

$$\theta(t) = \frac{J\mathrm{M}}{\delta^2}(e^{\frac{-\delta t}{J}} - 1) + \frac{\mathrm{M}}{\delta}t \cong \frac{\mathrm{M}}{\delta}t \tag{18}$$

$$t_s \cong \frac{\delta \cdot \theta_0}{\mathrm{M}} \tag{19}$$

Another similar equation is derived by Raj K. Gupta and S. D. Senturia :

$$t_s = \frac{\delta \cdot \theta_0}{3\mathrm{M}} \tag{20}$$

For the damping-limited case, Eq.19 tends to overestimate the switching time and Eq.20 tends to underestimate the switching time.

II. Torsional Spring Constant of the Torsional Rectangular Bar

The maximum shear stress in a rectangular prismatic bar subjected to torsion may be expressed in the form:

$$\tau_{max} = \frac{T}{\alpha h w^2} \tag{21}$$

where α is a dimensionless constant obtained by the theory of elasticity solution and listed in table , and where the dimensions h and w satisfy $h/w \geq 1$.The angle of twist of a bar of length L can be expressed by :

$$T = \frac{GJ}{L} \cdot \theta = k_\theta \cdot \theta \qquad J = \beta h w^3 \tag{22}$$

where β is a dimensionless constant with values listed in Table

h/w	1	1.5	1.75	2	2.5	3	4	6	∞
α	0.208	0.231	0.239	0.246	0.258	0.267	0.282	0.298	0.333
β	0.141	0.196	0.214	0.229	0.249	0.263	0.281	0.298	0.333

Table 2 Torsion of Noncircular Prismatic Bars

III. Gas Fundamentals

Most of the damping in MEMS structures is given by squeeze film damping, so it's important to brief reviewing the fundamentals of gas motion. The air must be pushed from underneath the mainplate and the air molecules undergo several collisions in the gap between the plate and the bottom electrode when the MEMS structure is actuated. Several important numbers in fluid mechanics must be considered because they have a direct effect on the damping coefficient of the MEMS structure.

The mean-free path is the distance covered by a molecule in the gas successive collisions and is given by:

$$\lambda = \frac{1}{\sqrt{2}\pi N \sigma^2} \tag{23}$$

$$\lambda_a = (\frac{P_0}{P_a})\lambda_0, \tag{24}$$

where λ_0 is the mean free path at a pressure P_0.

The Knudsen number is a measure of the viscosity of the gas and is given by:

$$K_n = \frac{\lambda}{g} \tag{25}$$

A very small Knudsen number means that there are many collisions in the gap and the gas is viscous. When the gap height is on the order of the mean free (large K_n), particle-wall interactions become important, reducing the flow resistance, or viscosity (μ), through a "slip effect" where particles can have fewer interactions before escaping. For $g \geq 1$ μm, $K_n < 0.1$ at STP and the flow is assumed to be linearly viscous.

The coefficient of viscous μ is a measure of the resistance of a gas. The equation of viscosity is:

$$\mu = 0.1792\pi\rho\lambda\sqrt{2RT} \quad (26)$$

where R is the specific gas constant. An accurate equation of the viscosity for ideal and quasi-ideal gases such as air, and so on, was derived by Sutherland and is[25]:

$$\mu = 1.2566\times10^{-6}\sqrt{T}(1+\frac{\beta}{T})^{-1} \quad (27)$$

where $\beta = 110.33$ K, T is in Kelvin and the viscosity of ideal gases at STP is 1.845×10^{-5} kg/ms. The viscosity is directly depends on the pressure as seen by Eq. 22 and 24. The viscosity does change with the Knudsen number, since a high Knudsen number means that the gas experiences very few collisions and that the flow is not viscous anymore. A well-known equation was derived by Veijola et al[26].

$$\mu_e = \frac{\mu}{1+9.638K_n^{1.159}} \quad (28)$$

and is accurate to within ±5% for $0 \le K_n \le 880$. For $K_n = 0.026 - 0.08$, which corresponds to a gap height of 3-1μm, we find that $\mu_e = 0.87 - 0.66\mu$.