Impact of Self-Heating Effect on Hot Carrier Degradation in High-Voltage LDMOS

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Abstract

Self-heating induced transient hot carrier effects in high-voltage n-LDMOS are investigated. A novel LDMOS structure incorporating a metal contact in the bird's beak region is fabricated, which allows us to probe an internal voltage transient in hot carrier stress. The AC stress-frequency dependence of device degradation is characterized and evaluated by a two-dimensional numerical simulation. Our result shows that drain current degradation in AC stress is more serious than in DC stress because of the reduction of self-heating effect.

Introduction

Laterally diffused MOS (LDMOS) transistors have been widely utilized in today's high-voltage/high-current drivers and RF power amplifiers [1,2]. Due to large power consumption, self-heating effect (SHE) is significant in a LDMOS. In this paper, we will study SHE on hot carrier degradation in DC and AC stress modes. To this purpose, we fabricate a special LDMOS structure, which incorporates a metal contact in the bird's beak region. Thus, we can probe an internal voltage (V_I) transient due to SHE directly. Fig. 1 illustrates the device structure. Three regions of a LDMOS are indicated in the figure, including a channel region, an accumulation region and a field-oxide region. The contact is arranged in the accumulation region that the internal voltage V_I can be used as a monitor for hot carrier effects in the channel. The contact area is small enough that the device electrical characteristics are not affected.

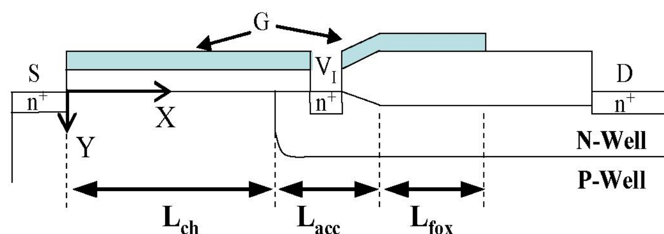

Fig. 1: Cross-section of a novel LDMOS structure. The metal contact (V_I) is arranged in the accumulation region with a n^+ implant. Three regions are indicated, including channel region (L_{ch}), accumulation region (L_{acc}), and field-oxide region (L_{fox}).

The device was processed in a 0.18μm CMOS technology with a gate oxide thickness of 100nm and a channel length of 3μm. The operation voltages are V_g=40V and V_d=40V. To eliminate SHE in measurement, a fast transient measurement setup including a digital oscilloscope is built, as shown in Fig. 2. Linear drain current (I_{dlin}@V_g/V_d=40V/0.1V) is measured to monitor device degradation under AC/DC stress. A three-region charge pumping technique [3, 4] is used to locate hot carrier damage area in the device and to identify the type of generated oxide traps. Two-dimensional device simulation is performed to calculate a temperature distribution and corresponding hot carrier effects.

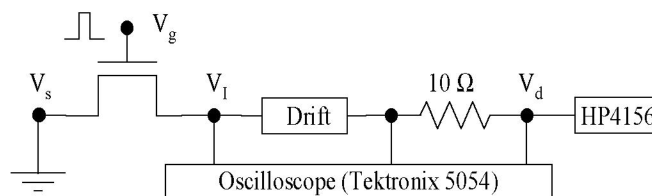

Fig. 2: Fast transient measurement setup for drain current and internal voltage (V_I) characterization. The external resistance (10Ω) is negligible compared to a total device resistance (~40V/10mA~4kΩ). A gate pulse and constant V_d are applied.

Results and Discussion

(a) Self-Heating Characterization

Fig. 3(a) shows a normalized drain current (I_d/W) versus V_d in small and large gate width devices in DC (Agilent 4156) measurement. The I_d/W in a linear region is nearly the same, indicating no process variations in these two devices. However, the larger width device exhibits a smaller I_d/W in the saturation region because of larger power consumption and thus a larger SHE. The reduction of the saturation current is attributed to self-heating induced mobility degradation [5,6]. Fig. 3(b) compares the I_d/W from a DC and from a fast transient measurement for the large width device. A larger I_d/W is noticed in the transient measurement because of the elimination of SHE. In addition, SHE is manifested in the internal voltage measurement results by Agilent 4156 and by the fast transient setup (Fig. 4). The larger V_I in a non-SHE

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condition is attributed to a higher mobility in accumulation region, thus resulting in a smaller drift region resistance. A larger internal voltage in non-SHE condition implies a stronger hot carrier stress in the channel region.

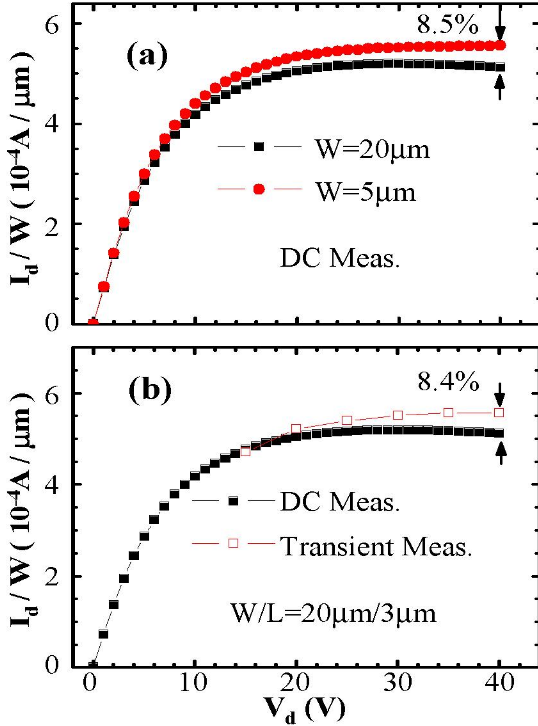


Fig. 3: (a) Normalized drain current (I_d/W) versus drain voltage in small and large gate width devices in DC measurement (Agilent 4156). (b) The I_d/W from a DC and a fast transient measurement for the large width device.

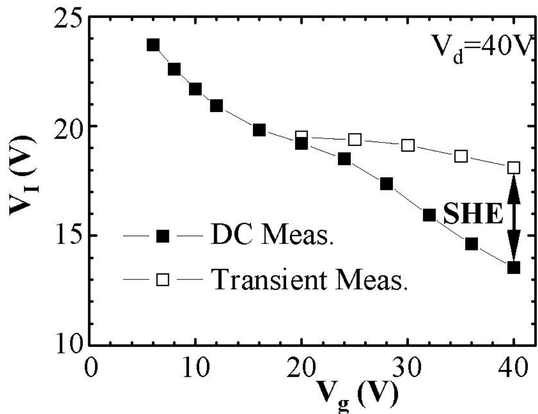


Fig. 4: Internal voltage versus gate voltage measured by Agilent 4156 and by a transient measurement setup.

(b) Degradation Characteristics in AC/DC Stress

Two stress modes (max. I_B, and max. I_g) are chosen in the study of hot carrier degradation in n-LDMOS. The I_g-V_g and I_B-V_g of a n-LDMOS are shown in Fig. 5. Fig. 6 shows AC and DC stress induced I_{dlin} degradations in the above two stress modes. Max. I_B stress shows a slight difference in I_{dlin} degradation between AC and DC stresses, implying that SHE is not important at a lower stress V_g. However, in maximum I_g stress, AC stress shows much more I_{dlin} degradation than DC stress. Moreover, strong stress-frequency (Fig. 7(a)) and duty cycle (Fig. 7(b)) dependence is observed. In Fig. 7(a), the I_{dlin} degradation increases with frequency and then becomes saturated. A corner frequency is found to be f_1=20 kHZ at a duty cycle=10%. In Fig. 8, we plot I_{dlin} degradation versus pulse duration, i.e., duty cycle/frequency, in AC stress. A corner time of ~5μs is obtained, suggesting that SHE becomes important as pulse duration is longer than ~5μs.

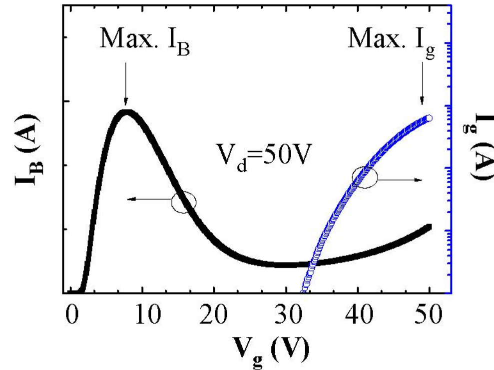


Fig. 5: Substrate current and gate current versus gate voltage in a LDMOS. Two hot carrier stress modes are shown, maximum I_B stress and maximum I_g stress.

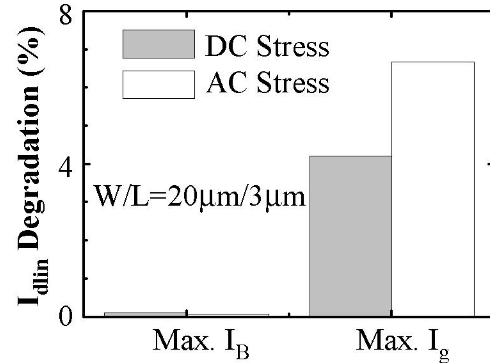


Fig. 6: Linear drain current degradation (V_g/V_d= 40V/0.1V) in two hot carrier stress modes. DC and AC stresses have the same cumulative stress time. AC stress has a frequency of 20kHz and a duty cycle of 10%.

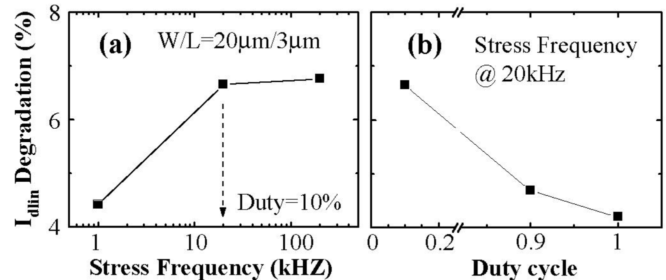


Fig. 7: (a) I_{dlin} degradation versus stress frequency with a duty cycle of 10%. A corner frequency (f_1) is around 20kHz. (b) I_{dlin} degradation versus duty cycle for a frequency of 20kHZ.

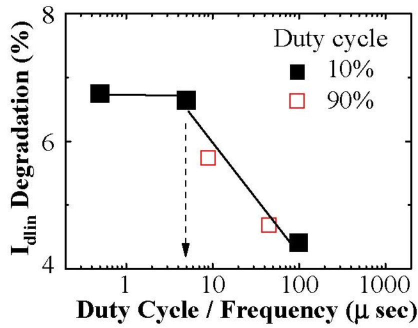


Fig. 8: I_{dlin} degradation versus pulse duration (=duty cycle/frequency) in AC stress. The corner time is around 5µs.

Fig. 9 shows a V_I transient in a pulsed gate and DC drain voltage condition. The V_I decreases with time due to SHE and the onset time of SHE is extracted to be around 5µs. This result is consistent with the findings from AC stress induced degradation (Fig. 8).

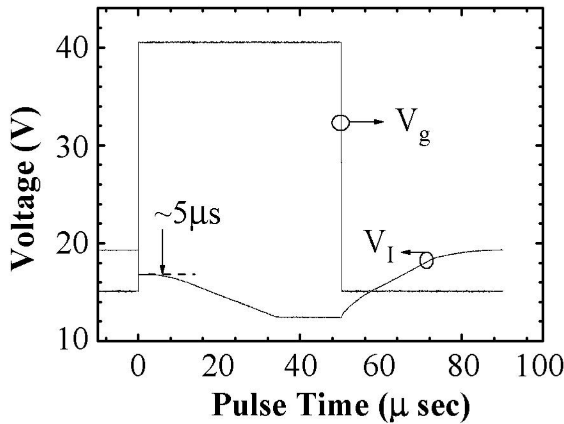


Fig. 9: The internal voltage (V_I) transient in a pulsed gate and DC drain voltage (V_d=40V) condition. The waveforms of V_I and V_g are plotted. The onset time for SHE is ~5µs.

A charge pumping measurement (I_{cp}) result is shown in Fig. 10. A distinguished three-stage feature in I_{cp} –V_{gL} is observed, corresponding to the three regions of a LDMOS respectively. By comparing the pre-stress and post-stress I_{cp} in each stage, we are able to separate interface trap (N_{it}) and fixed oxide charge (Q_{ox}) creation in each region of the device. The result in Fig. 10 reveals that AC stress generates more N_{it} in the channel region and more Q_{ox} in the accumulation region. The larger trap generation rate in AC stress results from a smaller temperature rise and thus a larger stress gate current (Fig. 11). The self-heating induced temperature change in a LDMOS is simulated by a two-dimensional numerical device simulation (Fig. 12). The ambient temperature in the simulation is 300K. In Fig. 12, the drift region shows a higher temperature change than channel region, implying a larger mobility degradation and thus a higher drift region resistance. The SHE is stronger at a higher V_g. The simulation also reveals a higher V_I in a non-SHE condition (Fig. 13). Good agreement between measurement and simulation is obtained in Fig. 13. Because of a larger V_I in the non-SHE condition, the simulated impact ionization rate is stronger in the non-SHE condition (Fig. 14). This feature also confirms our charge-pumping results in Fig. 10 and concludes a more serious I_{dlin} degradation rate in AC stress (Fig. 15).

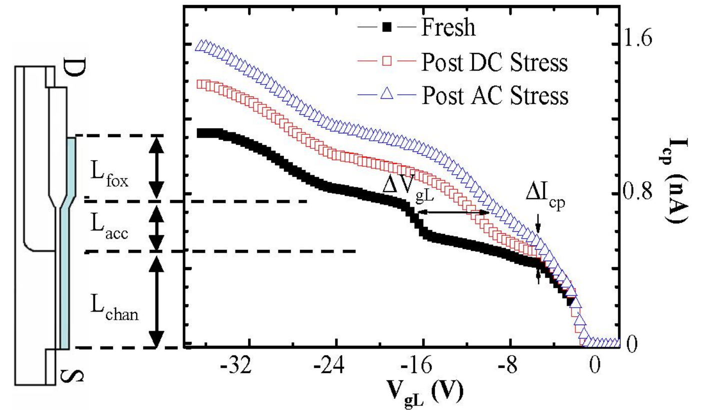


Fig. 10: Three-region charge pumping measurement results after maximum I_g AC and DC stress. A V_{gL} shift is in the accumulation region and a I_{cp} increase is in the channel region. For more details, see [3,4].

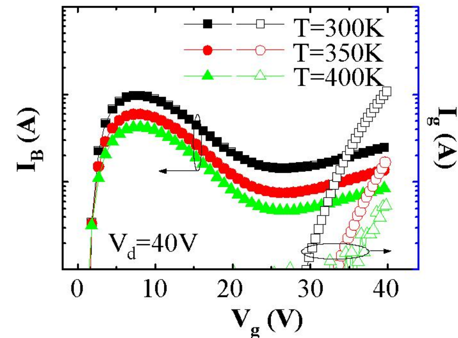
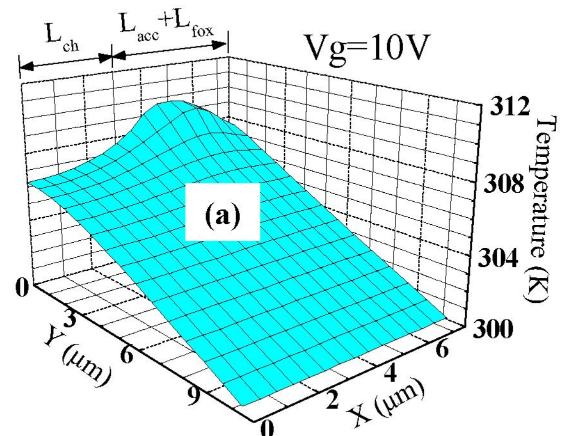


Fig. 11: Substrate current and gate current versus gate voltage for different temperatures.



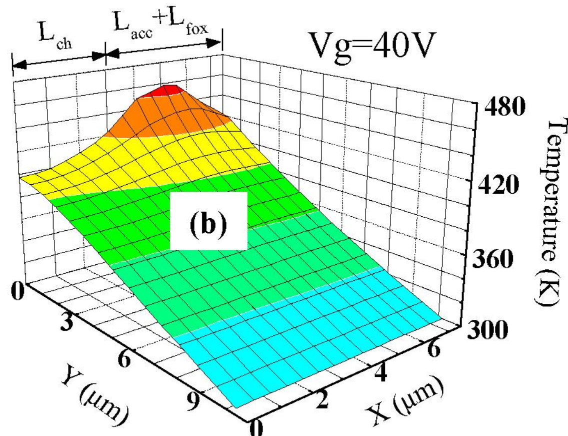


Fig. 12: Simulation of a temperature distribution with SHE. The ambient temperature is 300K. X and Y axes are indicated in Fig. 1. (a) V_g/V_d=10V/40V. (b) V_g/V_d=40V/40V.

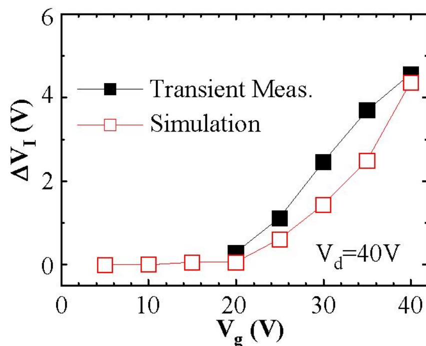


Fig. 13: Internal voltage change (V_I(non-SHE)-V_I(SHE)) versus gate voltage from measurement and from simulation.

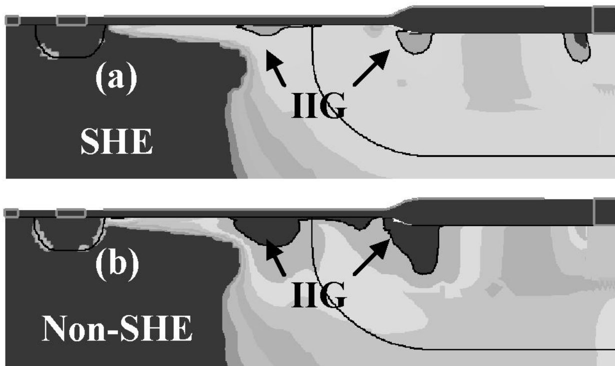


Fig. 14: Two-dimensional device simulation of impact ionization generation (IIG) rate at V_g/V_d=40V/40V. (a) SHE is included and (b) SHE is not included.

Conclusion

Transient self-heating effect in AC hot carrier stress in LDMOS has been studied by measuring an internal voltage. The extracted self-heating time is around 5μs. The AC stress at maximum I_g yields the worst hot carrier degradation because of the elimination of self-heating effect.

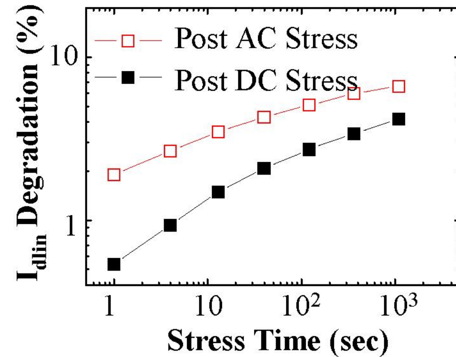


Fig. 15: I_{dlin} degradation rate after AC and DC stress in maximum I_g stress condition. The AC stress frequency is 20kHz and the duty cycle is 10%.

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