The Effect of IEC-Like Fast Transients on RC-Triggered ESD Power Clamps

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***Abstract*—Four power-rail electrostatic-discharge (ESD) clamp circuits with different ESD-transient detection circuits have been fabricated in a 0.18-μm CMOS process to investigate their susceptibility against electrical fast-transient (EFT) tests. Under EFT tests, where the integrated circuits in a microelectronic system have been powered up, the feedback loop used in the power-rail ESD clamp circuits may lock the ESD-clamping NMOS in a "latch-on" state. Such a latch-on ESD-clamping NMOS will conduct a huge current between the power lines to perform a latchup-like failure after EFT tests. A modified power-rail ESD clamp circuit has been proposed to solve this latchuplike failure and to provide a high-enough chip-level ESD robustness.**

***Index Terms*—Electrical fast-transient (EFT) test, electromagnetic compatibility, electrostatic discharge (ESD), ESD protection circuit, latchup, system-level ESD stress.**

I. Introduction

WHOLE-CHIP electrostatic-discharge (ESD) protection has become a major reliability concern for modern integrated circuits (ICs) fabricated by scaled-down CMOS technologies [1]–[4]. The power-rail ESD clamp circuit located between the $V_{\rm DD}$ and $V_{\rm SS}$ lines in CMOS ICs has been designed for comprehensive ESD protection against the unexpected ESD damages located at the internal circuits of chips [5]–[7]. When the pin of a CMOS IC is zapped under the positive-to-$V_{\rm SS}$ (PS-mode), negative-to-$V_{\rm DD}$ (ND-mode), pin-to-pin, or $V_{\rm DD}$-to-$V_{\rm SS}$ ESD-stress conditions, the power-rail ESD clamp circuit can provide a low-impedance path between the $V_{\rm DD}$ and $V_{\rm SS}$ lines to efficiently discharge ESD current. Therefore, the power-rail ESD clamp circuit designed with high turn-on efficiency and fast turn-on speed is necessary for whole-chip ESD protection. In addition, some modified designs to further enhance the on-chip ESD protection performance of power-rail ESD clamp circuits had been reported [8]–[13].

Recently, electrical fast-transient (EFT) test [14] and system-level ESD stress [15] directly on the IC level have attracted more attention. Very few have been published so far, and [16]–[18] did not really address such current issues. Moreover, there are extensive discussions going on regarding what electrical transients that the IC actually receives. This tendency results from not only the integration of more functional circuits in a single chip but also the strict requirement of reliability regulation on the microelectronic system equipped with CMOS ICs. The EFT-induced transients act as exponential voltage pulse, which is different from the underdamped sinusoidal voltage waveforms generated from the system-level ESD test. Such EFT-induced electrical transients could cause transient-induced latchup (TLU) failure via the inevitable parasitic silicon-controlled rectifier in CMOS ICs [19]. It has also been reported [20], [21] that some CMOS ICs are very susceptible to electrical transient disturbance or system-level ESD stress, even though they have passed some component-level ESD specifications of human-body model (HBM) [22], machine model (MM) [23], and charged-device model (CDM) [24].

In this paper, the malfunction or wrong triggering behavior among four different on-chip power-rail ESD clamp circuits under EFT tests is investigated [25]. For some power-rail ESD clamp circuits designed with feedback loop in ESD-transient detection circuits, a serious latchuplike failure is caused by the latch-on state of the ESD-clamping NMOS after the EFT test. Furthermore, a modified design with additional NMOS reset function into the power-rail ESD clamp circuit is proposed to overcome such a latchuplike failure.

II. Power-Rail ESD Clamp Circuits

To provide effective on-chip ESD protection, four different power-rail ESD clamp circuits had been reported [8]–[12], which are shown in Fig. 1(a)–(d) with the names of the following: 1) power-rail ESD clamp circuit with typical RC-based detection; 2) power-rail ESD clamp circuit with PMOS feedback; 3) power-rail ESD clamp circuit with NMOS+PMOS feedback; and 4) power-rail ESD clamp circuit with cascaded PMOS feedback in this paper. Those power-rail ESD clamp circuits have been designed in the same silicon chip and fabricated in a 0.18-μm CMOS process with oxide thickness of $\sim$40 Å to investigate their susceptibility to EFT tests.

A. Power-Rail ESD Clamp Circuit With Typical *RC*-Based Detection

The typical *RC*-based power-rail ESD clamp circuit is shown in Fig. 1(a) with a three-inverter buffer between the RC circuit and the ESD-clamping NMOS [8]. During the ESD zapping

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with the pulse rise time of ~10 ns, the voltage level at the $V_{\rm Filter}$ node is increased much more slowly than that on the $V_{\rm DD}$ power line, because the RC circuit is designed with a time constant on the order of microseconds. Due to the delay of voltage increase at the $V_{\rm Filter}$ node, the three-inverter buffer is powered by the ESD energy to conduct a voltage to the V_G node and then to turn on the ESD-clamping NMOS. The turned-on ESD-clamping NMOS, which provides a low-impedance path between the $V_{\rm DD}$ and $V_{\rm SS}$ power lines, will clamp the overstress ESD voltage to effectively protect the internal circuits against ESD damage. The turn-on time from the RC circuit is usually designed around ~100 ns to meet the half-energy discharging time of the HBM ESD current waveform. After the designed turn-on time of ~100 ns from the RC circuit, the residue of the ESD energy can be continually discharged through the ESD-clamping NMOS, which has been kept in the snapback region after being triggered on by the ESD-transient detection circuit during ESD stress. Under normal circuit operating conditions, the power-rail ESD clamp circuit must be kept off to avoid power loss from $V_{\rm DD}$ to $V_{\rm SS}$. To meet such a timing requirement, the RC time constant in the RC-based ESD-transient detection circuit is typically designed with 0.1–1 μs to achieve the design constraints [8].

B. Power-Rail ESD Clamp Circuit With PMOS Feedback

Another design consideration for the power-rail ESD clamp circuit is the circuit immunity to false triggering during a power-up condition. The power-rail ESD clamp circuit should be turned on when ESD stress appears across the $V_{\rm DD}$ and $V_{\rm SS}$ power lines but must be kept off when the IC is under a normal power-on condition. The RC time constant was usually designed around 0.1–1 μs to meet such a requirement. However, the large RC time constant used in the power-rail ESD clamp circuit may cause false triggering during a fast power-up condition with a rise time of less than 10 μs. The modified power-rail ESD clamp circuit incorporated with PMOS feedback, as shown in Fig. 1(b), was developed to mitigate such a mistrigger problem [9]. The transistor MPFB can help to keep the ESD-clamping NMOS off during the normal power-up condition.

C. Power-Rail ESD Clamp Circuit With NMOS+PMOS Feedback

In advanced CMOS technology with thinner gate oxide, the power-rail ESD clamp circuit with a large MOS capacitance in the RC timer had been found to cause significant standby power consumption due to the gate oxide leakage [10]. Thus, the power-rail ESD clamp circuit with small MOS capacitance is desired to combat the gate oxide leakage. It was reported that the power-rail ESD clamp circuit incorporated with a regenerative feedback network can be used to significantly reduce the RC time constant, as shown in Fig. 1(c) [11]. Transistors MPFB and MNFB in Fig. 1(c) provide a feedback loop to latch the ESD-clamping NMOS in the conductive state during an ESD-stress condition. With this feedback loop in the power-rail ESD clamp circuit, the dynamic currents of M_{P2}, M_{N2}, MPFB, and MNFB determine the critical voltage to trigger on the ESD-clamping NMOS. After the timing out of RC time constant in the ESD-transient detection circuit, transistor M_{P2} begins to conduct and increase the potential of the INV2OUT node. The settling potential of the INV2OUT node is set by the current balance between M_{P2} and MNFB. Thus, the device ratios of

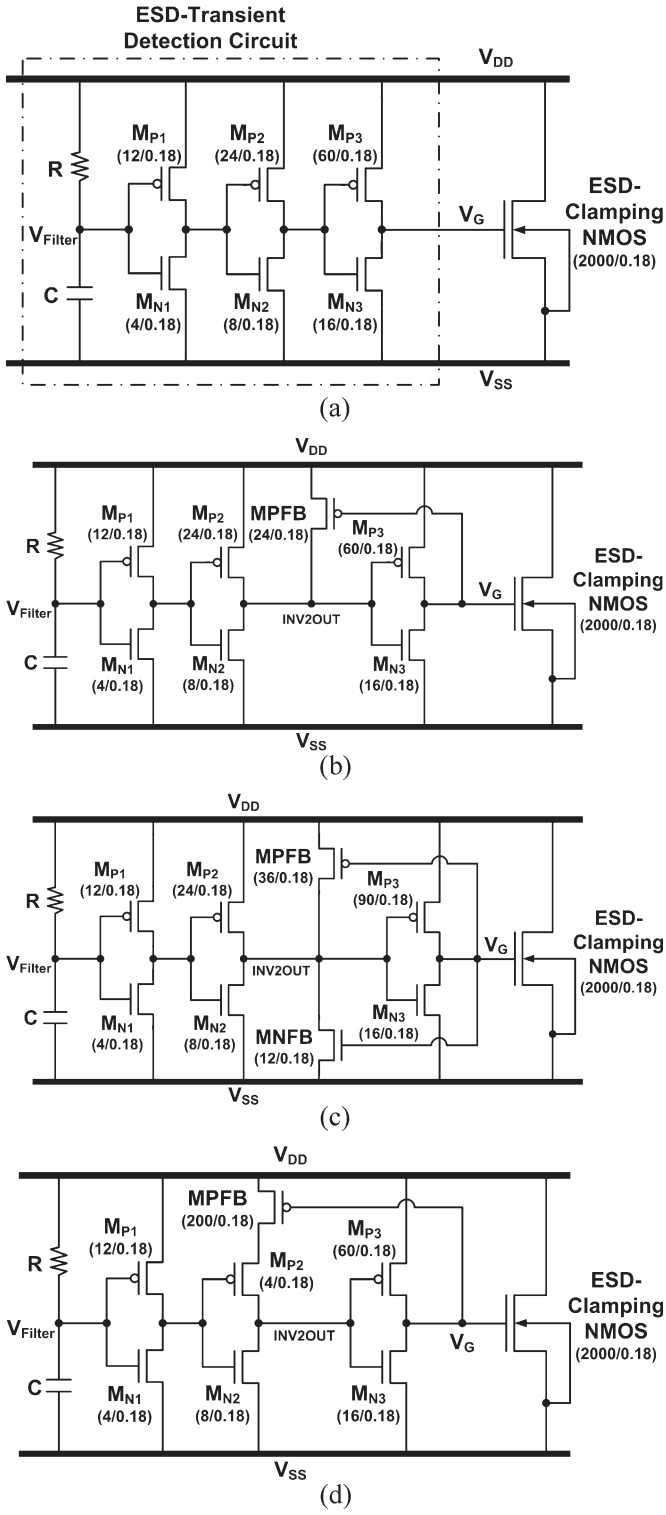

Fig. 1. Four prior power-rail ESD clamp circuits designed with (a) typical RC-based detection, (b) PMOS feedback, (c) NMOS+PMOS feedback, and (d) cascaded PMOS feedback. The device dimensions of transistors in each circuit realized in a 0.18-μm CMOS process are also indicated.

M_{P2} and MNFB in the power-rail ESD clamp circuit with NMOS+PMOS feedback should be appropriately selected.

D. Power-Rail ESD Clamp Circuit With Cascaded PMOS Feedback

Another RC-based power-rail ESD clamp circuit with cascaded PMOS feedback was also developed to reduce the RC time constant and solve the false-triggering issue during a fast power-up condition, as shown in Fig. 1(d) [12]. PMOS transistor MPFB is connected to form the cascaded feedback loop. During an ESD-stress condition, transistor MPFB is turned off, and the INV2OUT node is remained in a low-voltage state. Thus, the turn-on time of the ESD-clamping NMOS in this design can be longer than that of the typical RC-based power-rail ESD clamp circuit. If the ESD-clamping NMOS is mistriggered during a fast power-up condition or by an overvoltage noise under normal operating conditions, the voltage on the INV2OUT node can be recharged up toward $V_{\rm DD}$ by the subthreshold current of MPFB. Therefore, the ESD-clamping NMOS will not stay at the latch-on state and turn itself off after the fast power-up condition.

E. Realization in Silicon Chip

Some simulations have been provided to realize the aforementioned four power-rail ESD clamp circuits in the CMOS process. The corresponding device dimensions of all transistors in these four power-rail ESD clamp circuits realized in a 0.18-μm CMOS process are also shown in Fig. 1(a)–(d). To simply the comparison for the latchup-like failure in this paper, the RC values in the ESD-transient detection circuits of these four power-rail ESD clamp circuits are set with the same R of 50 kΩ and C of 2 pF in silicon fabrication. For EFT verification, the test chips are packaged in the 40-pin side-brazed package without classical filtering on the evaluation printed circuit board.

In the inset of Fig. 2, a $V_{\rm DD}$ power-on waveform with a rise time of 0.1 ms and a voltage height of 1.8 V is applied to the $V_{\rm DD}$ line of the power-rail ESD clamp circuits. During such a $V_{\rm DD}$ power-on transition, the voltage waveforms on the V_G node among the four power-rail ESD clamp circuits are shown in Fig. 2. The V_G peak voltages in Fig. 2 are all below the threshold voltage ($\sim$0.44 V) of the NMOS, so the ESD-clamping NMOS in these four power-rail ESD clamp circuits will be kept off after the $V_{\rm DD}$ power-on transition.

In the inset of Fig. 3, a fast-ramp voltage with a rise time of 10 ns is used to simulate the rising edge of the HBM ESD pulse. The pulse height of the fast-ramp voltage set of 5 V is used to monitor the voltage on the V_G node before the occurrence of drain breakdown at the ESD-clamping NMOS. As shown in Fig. 3, among these four power-rail ESD clamp circuits, the voltage waveforms on the V_G node are simultaneously increased when the fast-ramp voltage is applied to $V_{\rm DD}$, whereas $V_{\rm SS}$ is grounded. With the NMOS+PMOS feedback or cascaded PMOS feedback in the power-rail ESD clamp circuits, the turn-on time (with V_G being greater than its threshold voltage) of the ESD-clamping NMOS is really extended much longer than the default 100-ns RC time constant in the traditional design of Fig. 1(a) with typical RC-based detection.

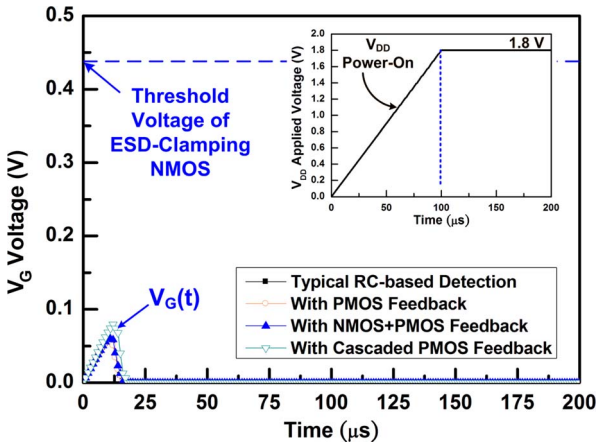

Fig. 2. HSPICE-simulated voltage waveforms on the V_G node among the four prior power-rail ESD clamp circuits under a normal $V_{\rm DD}$ power-on transition with a 0–1.8-V ramp voltage applied to $V_{\rm DD}$. The rise time of $V_{\rm DD}$ ramp voltage is 0.1 ms in this simulation.

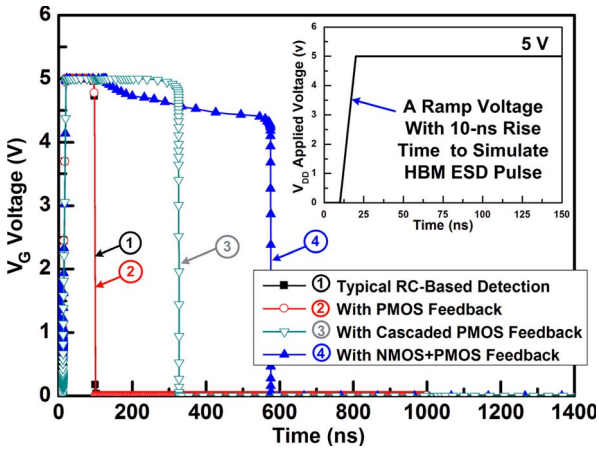

Fig. 3. HSPICE-simulated voltage waveforms on the V_G node among the four prior power-rail ESD clamp circuits under an ESD-stress condition. A 0–5-V ramp voltage with a rise time of 10 ns is used to simulate the rising edge of the HBM ESD pulse before the drain breakdown on the ESD-clamping NMOS.

III. EFT Test

A. Measurement Setup

The IEC 61000-4-4 standard [14] has defined the immunity levels and test methods to verify the electronic equipment against repetitive EFTs. The EFT test is a test with repetitive bursts consisting of a number of fast pulses, which can be coupled into the power supply, control, signal, and ground ports of the electronic equipment. The minimum start values of the pulse peak are $\pm$200 V from the EFT tester. For EFT pulses with a repetition frequency of 5 kHz, the measured voltage waveforms with EFT voltages of $-$200 and $+$200 V on a 50-Ω load are shown in Fig. 4(a) and (b). With the impedance matching to 50 Ω, the measured pulse peak is half of the input EFT voltage. Therefore, the measured pulse peaks are $-$100 and $+$100 V in Fig. 4(a) and (b), respectively. The waveform of a single EFT pulse has a rise time of $\sim$5 ns and a pulse duration (time interval at half of the peak EFT voltage) of $\sim$50 ns. With

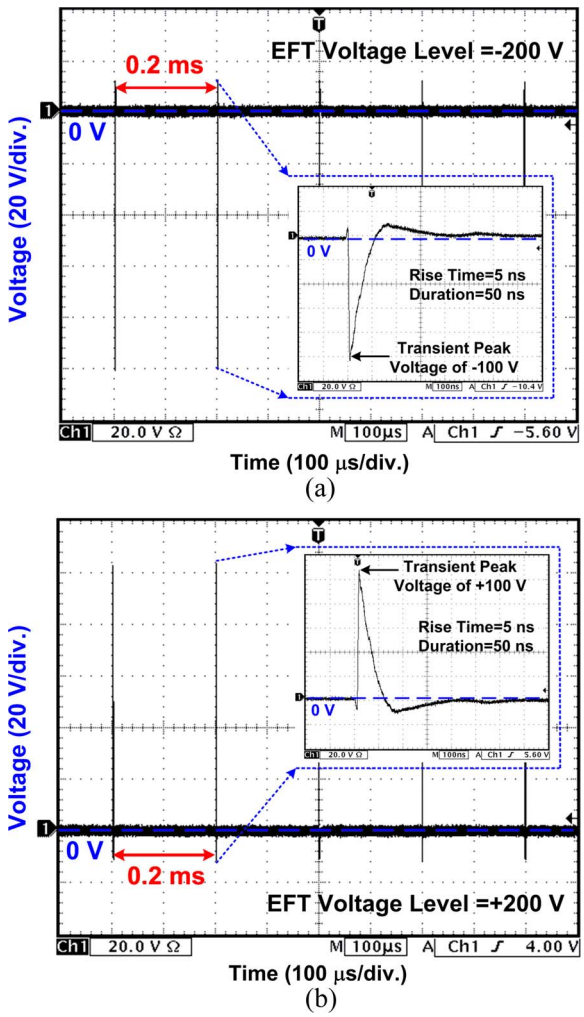

Fig. 4. Measured voltage waveforms of EFT pulses on a 50-Ω load with a repetition rate of 5 kHz and EFT voltages of (a) −200 V and (b) +200 V.

an EFT repetition frequency of 5 kHz, the time interval between each pulse is 0.2 ms. By EFT regulation, the application time should be longer than 1 min, and both positive and negative polarities must be applied.

The measurement setup for the EFT test on a CMOS IC under a power-up condition is shown in Fig. 5. A supply voltage of 1.8 V is used as $V_{\rm DD}$, and the EFT generator is connected directly to the device under test (DUT) through a cable in this paper. The voltage and current waveforms on the DUT (at the $V_{\rm DD}$ node) during/after the EFT test are monitored by a digital oscilloscope. With such a measurement setup, the susceptibility of different power-rail ESD clamp circuits against EFT tests can be evaluated. Before any EFT zapping, the initial $V_{\rm DD}$ voltage level on the IC is measured to make sure the correct bias of 1.8 V. If the latchuplike failure occurs after EFT zapping, the potential on $V_{\rm DD}$ node will be pulled down to a much lower level due to the latch-on state of the ESD-clamping NMOS, and $I_{\rm DD}$ will be significantly increased.

B. Measurement Results

With the EFT measurement setup shown in Fig. 5, the $V_{\rm DD}$ and $I_{\rm DD}$ transient responses can be recorded by the oscilloscope

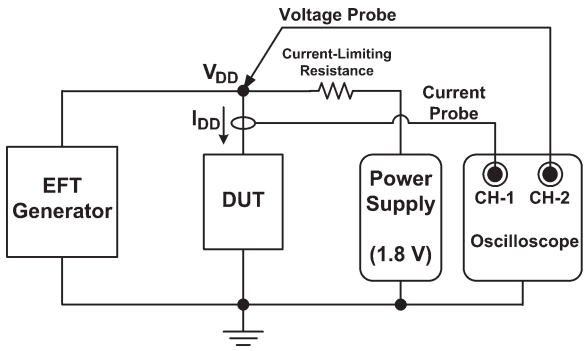

Fig. 5. Measurement setup for a direct EFT test on a CMOS IC in the DUT powered with 1.8-V supply. The $V_{\rm DD}$ and $I_{\rm DD}$ transient waveforms are recorded by a digital oscilloscope with a sampling rate of 5 GS/s.

to clearly indicate whether the latchuplike failure occurs or not. For the power-rail ESD clamp circuits designed with typical RC-based detection or with PMOS feedback, the latchuplike failure does not occur after EFT tests because $I_{\rm DD}$ is still kept at zero, even though the EFT voltage is as high as −800 or +800 V.

Fig. 6(a) and (b) shows the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient responses on the power-rail ESD clamp circuit designed with NMOS+PMOS feedback under the EFT test with EFT voltages of −200 and +200 V, respectively. After the EFT test with an EFT voltage of −200 V, the latchuplike failure can be initiated in this power-rail ESD clamp circuit, because $I_{\rm DD}$ is significantly increased and $V_{\rm DD}$ is pulled down, as shown in Fig. 6(a). The latchuplike failure can also be found in Fig. 6(b) due to the EFT test with an EFT voltage of +200 V. All the PMOS and NMOS devices in the ESD-transient detection circuits have been surrounded with double guard rings in the layout to guarantee no latchup issue in this part [26]. This implies that the feedback loop in the ESD-transient detection circuit is locked after the EFT test and continually keeps the ESD-clamping NMOS in the latch-on state. From the observed voltage and current waveforms, such a $I_{\rm DD}$ is conducted by the latch-on state of the ESD-clamping NMOS after EFT tests. For the power-rail ESD clamp circuit designed with cascaded PMOS feedback, the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient responses are shown in Fig. 7(a) and (b) under the EFT test with EFT voltages of −200 and +500 V, respectively. A similar latchuplike failure also occurs in this power-rail ESD clamp circuit due to the latch-on state of the ESD-clamping NMOS after EFT tests.

The susceptibility among the aforementioned four power-rail ESD clamp circuits against EFT tests is listed in Table I. From the experimental results, the power-rail ESD clamp circuit designed with NMOS+PMOS feedback is highly sensitive to TLU-like failure. The power-rail ESD clamp circuits designed with typical RC-based detection or with PMOS feedback are free to such a latchuplike failure under EFT tests.

The failure location after the EFT test has been inspected, as shown in Fig. 8. The failure is located at the $V_{\rm DD}$ metal line from the $V_{\rm DD}$ pad to the power-rail ESD clamp circuit, which was drawn with a metal width of 30 μm in the test chip. The current continually that is conducted through the latch-on state of the ESD-clamping NMOS, which is drawn with a large device dimension W/L of 2000 μm/0.18 μm for consideration

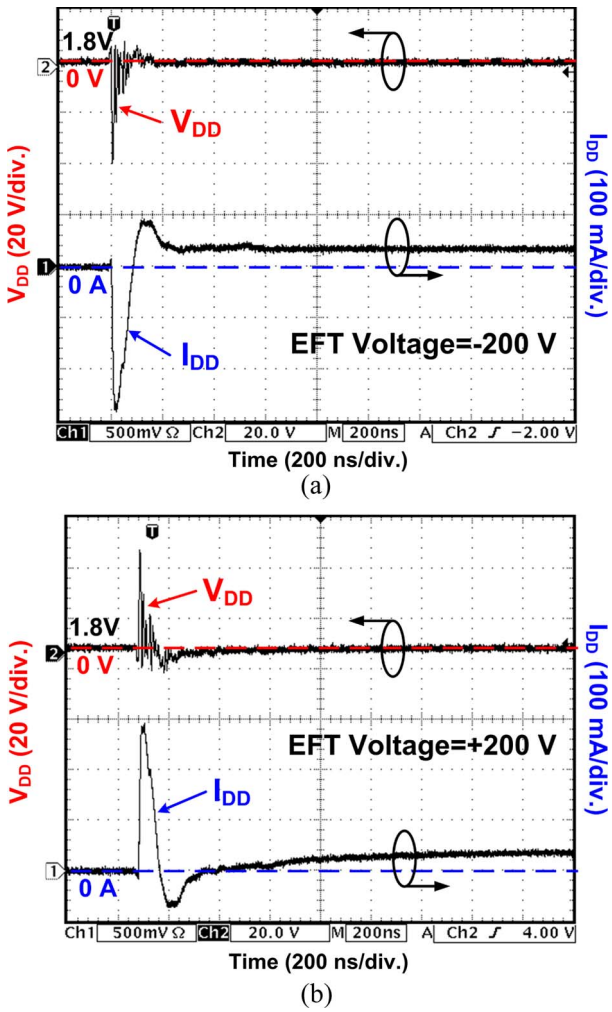

Fig. 6. Measured V_{DD} and I_{DD} transient waveforms on the power-rail ESD clamp circuit with NMOS+PMOS feedback under an EFT test with EFT voltages of (a) −200 V and (b) +200 V. Latchuplike failures occur after the EFT test with increased I_{DD} and decreased V_{DD}.

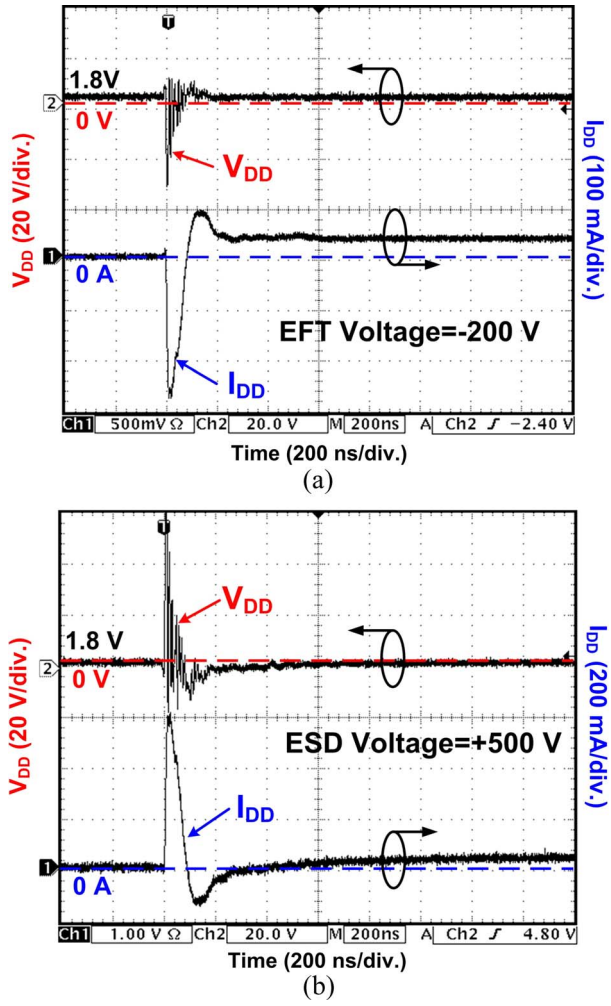

Fig. 7. Measured V_{DD} and I_{DD} transient waveforms on the power-rail ESD clamp circuit with cascaded PMOS feedback under an EFT test with EFT voltages of (a) −200 V and (b) +500 V. Latchuplike failures occur after the EFT test with increased I_{DD} and decreased V_{DD} voltage.

of high ESD robustness, causes such a burned-out failure on the metal line after EFT tests.

IV. Modified Power-Rail ESD Clamp Circuit

In order to meet the EFT regulation, a modified design on the power-rail ESD clamp circuit without suffering a latchuplike failure is highly desired for CMOS ICs. It was ever reported that a power-rail ESD clamp circuit with a traditional rise time detector and a separated on-time control circuit can improve the immunity to false triggering [13]. In this paper, another modified power-rail ESD clamp circuit is proposed to avoid such a latchuplike failure. This new modified power-rail ESD clamp circuit can provide a high-enough chip-level ESD robustness but without suffering the latchuplike failure during the EFT test.

A. Power-Rail ESD Clamp Circuit With NMOS Reset Function

Fig. 9 shows the modified power-rail ESD clamp circuit with NMOS reset function to overcome the latchuplike failure, which is realized with NMOS+PMOS feedback and an additional NMOS device (M_{NR1}) to provide the reset function after EFT tests. When the ESD-clamping NMOS is latched on, the NMOS device (M_{NR1}) will be turned on after the time-out of RC time constant. Thus, the gate potential (V_G) of the

TABLE I
Comparison on Susceptibility Against EFT Tests Among the Four Prior Power-Rail ESD Clamp Circuits and the Modified Power-Rail ESD Clamp Circuit With NMOS + PMOS Feedback and NMOS Reset Function

Power-Rail ESD Clamp Circuits	Positive EFT Voltage	Negative EFT Voltage
Typical RC-Based Detection	Over +800 V	Over -800 V
With PMOS Feedback	Over +800 V	Over -800 V
With NMOS+PMOS Feedback	Under +200 V	Under -200 V
With Cascaded PMOS Feedback	+500 V	Under -200 V
With NMOS+PMOS Feedback and NMOS Reset Function	Over +800 V	Over -800 V

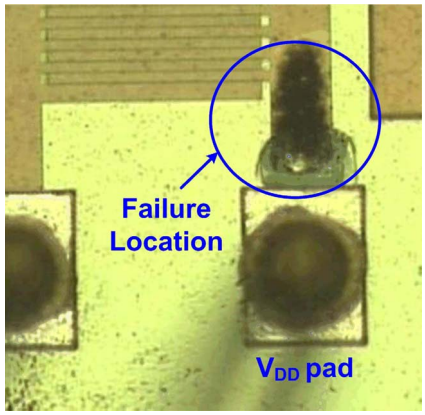

Fig. 8. Failure location of the power-rail ESD clamp circuit after EFT tests. The metal line connected between the V_{DD} pad and the ESD-clamping NMOS is burned out due to the EFT test.

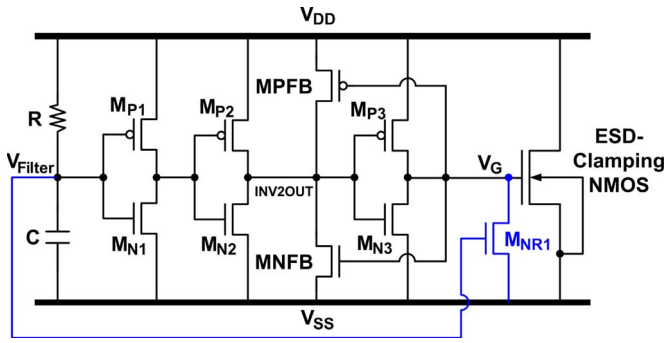

Fig. 9. Modified power-rail ESD clamp circuit designed with NMOS+PMOS feedback and additional NMOS reset function to overcome the latchuplike failure.

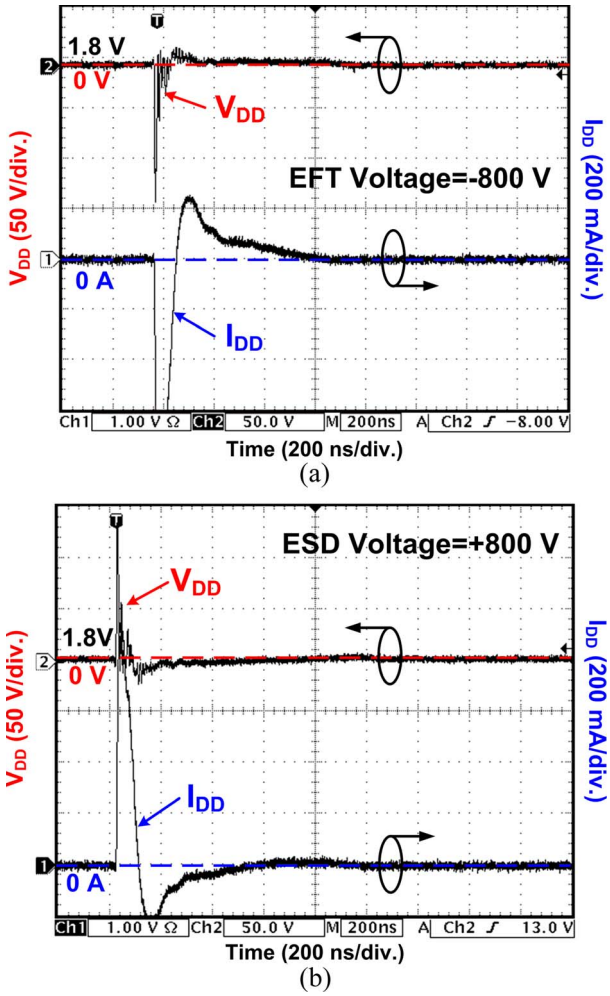

Fig. 10. Measured V_{DD} and I_{DD} transient waveforms on the modified power-rail ESD clamp circuit with additional NMOS reset function under an EFT test with EFT voltages of (a) −800 V and (b) +800 V. No latchuplike failure occurs in this EFT test.

ESD-clamping NMOS will be pulled down toward 0 V to release the "latch-on" state after EFT tests. Compared with the power-rail ESD clamp circuit with NMOS+PMOS feedback, the modified power-rail ESD clamp circuit with NMOS reset function has a shorter turn-on time of ∼380 ns on the V_G waveform by simulation when a 5-V ESD-like voltage ramp is applied to V_{DD}. The simulated V_G waveform is similar to those shown in Fig. 3.

B. Experimental Results

The measured V_{DD} and I_{DD} transient responses on the modified power-rail ESD clamp circuit under EFT tests with EFT voltages of −800 and +800 V are shown in Fig. 10(a) and (b), respectively. After the EFT test with a negative (positive) EFT voltage of −800 V (+800 V), the latchuplike failure does not occur in Fig. 10(a) [Fig. 10(b)], where neither I_{DD} is not increased nor V_{DD} is not pulled down after EFT tests. The susceptibility of the modified power-rail ESD clamp circuit with NMOS reset function against EFT tests has also been included in Table I for comparison with prior works.

To verify the chip-level ESD robustness among the power-rail ESD clamp circuits studied in this paper, the ESD-clamping NMOS has been drawn with the same large device dimension $(W/L = 2000\ \mu\text{m}/0.18\mu\text{m})$ for fair comparison. Therefore, the layout area of these five different power-rail ESD clamp circuits is dominated by the ESD-clamping NMOS, which is drawn as 95 μm × 80 μm. An ESD-transient detection circuit only occupies a smaller part in the whole layout area of each power-rail ESD clamp circuit, which is around 40 μm × 80 μm in the silicon chip. The modified power-rail ESD clamp circuit with NMOS reset function and the aforementioned four different power-rail ESD clamp circuits can all pass an HBM ESD stress of over ±8 kV and a CDM ESD stress of over ±1 kV in the 40-pin side-brazed package when the die size of the test chip is 1500 μm × 1500 μm.

V. Conclusion

Some of the advanced on-chip power-rail ESD clamp circuits with feedback loop have been found to suffer a latchuplike failure after EFT tests. The feedback loop used in the power-rail ESD clamp circuits provides a lock function to keep the ESD-clamping NMOS in a "latch-on" state. The latch-on ESD-clamping NMOS conducts a huge current between the V_{DD} and V_{SS} lines to perform this latchuplike failure after EFT tests. A modified design on the power-rail ESD clamp circuit with NMOS+PMOS feedback, with the additional NMOS reset

function to turn off the ESD-clamping NMOS after EFT tests, has been successfully verified in a 0.18-μm CMOS process. The modified power-rail ESD clamp circuit with NMOS reset function can sustain the EFT voltage of over $\pm$800 V without causing a latchuplike failure after EFT tests. The chip-level ESD robustness of the modified power-rail ESD clamp circuit with NMOS reset function can still be kept as good as those of the prior power-rail ESD clamp circuits with feedback loop.

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