IMPACT OF GATE TUNNELING LEAKAGE ON PERFORMANCES OF PHASE LOCKED LOOP CIRCUIT IN NANOSCALE CMOS TECHNOLOGY

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ABSTRACT

The influence of gate tunneling leakage on the circuit performances of phase locked loop (PLL) in nanoscale CMOS technology has been investigated by simulation. The basic PLL with second-order loop filter is used to simulate the impact of gate tunneling leakage on performance degradation of PLL in a standard 90-nm CMOS process. The MOS capacitors with different oxide thicknesses are used to investigate this impact to PLL. The locked time, static phase error, and jitter of second-order PLL are degraded by the gate tunneling leakage of MOS capacitor in loop filter.

INTRODUCTION

To reduce the power consumption in CMOS VLSI systems, the supply voltage V_{DD} has been scaled down to 1 V, or even sub-1 V. The gate-oxide thickness of the MOS transistor becomes thinner to reduce normal operation voltage (V_{DD}). The thinner gate oxide causes large gate-leakage current (tunneling current) [1], [2].

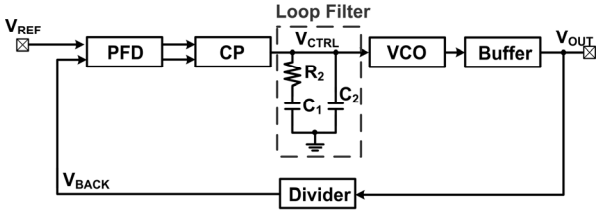
In PLL, the capacitor of loop filter needs a large capacitance to make PLL stable. The MOS capacitor with a larger capacitance per area was often used in PLL to reduce the silicon cost, but the PLL performance is degraded due to the large gate tunneling leakage. Recently, circuit design techniques to compensate the gate tunneling leakage of MOS capacitor in PLL have been reported in nanoscale CMOS processes [3]-[7]. The MOS capacitor realized with thick oxide has a less gate tunneling leakage [3]. The capacitor with multi-metal structure was used to avoid the gate tunneling leakage [4]. The thin-oxide MOS capacitor with opamp compensated technique is developed to reduce the gate leakage [5], [6]. The loop filter with gate tunneling leakage compensator was also developed [7]. However, the impact of gate tunneling leakage on PLL performance has no detailed investigation and analysis in nanoscale CMOS technology.

In this work, the influence of gate tunneling leakage on performances of the phase locked loop (PLL) is investigated and analyzed in a standard 90-nm CMOS process. The operating voltage of MOSFET device is 1 V. The gate tunneling leakage of MOS capacitance is simulated by HSPICE with BSIM4 model. The BSIM4 model has been included with the gate tunneling leakage effect [1], [2]. The MOS capacitors with different oxide thicknesses are used to investigate this impact to PLL.

PHASE LOCKED LOOP

The PLL is a necessary building block in many very large scale integrated circuits (VLSI). The demand for low-jitter PLLs has become especially strong in advanced nanoscale CMOS process. A PLL is basically an oscillator whose frequency is locked onto some frequency component of an input signal. Fig. 1 shows the basic PLL with second-order low-pass loop filter structure [8]. A PLL consists of a phase/frequency detector (PFD), a charge pump (CP), a loop filter, a voltage-controlled oscillator (VCO), a buffer, and a frequency divider (divided by N).

In this work, the PLL with second-order low-pass loop filter is used to investigate the impact of gate tunneling leakage of MOS capacitor on PLL performances. The design parameters and simulated results of second-order PLL are shown in Table 1. The results of second-order PLL are simulated by HSPICE with a standard 90-nm CMOS HSPICE model. The loop filter (C_1, C_2, and R_1) in second-order PLL is developed and simulated with ideal capacitor and resistor in Table 1. The MOS capacitor is usually used to realize the on-chip capacitor to reduce the chip area. The second-order loop filter structure can be realized with PMOS or NMOS devices, respectively.



PFD: Phase-Frequency Detector
CP: Charge Pump
VCO: Voltage Control Oscillator
Buffer: Differential Input to Single Output Converter
Divider: Frequency Divider (divided by N)

FIGURE 1. THE BASIC PHASE LOCKED LOOP WITH SECOND-ORDER LOW-PASS LOOP FILTER STRUCTURE.

TABLE 1. THE DESIGN PARAMETERS AND SIMULATED RESULTS OF SECOND-ORDER PLL IN A STANDARD 90-nm CMOS PROCESS

Design Parameters of PLL in a Standard 90-nm CMOS Process			
Operating Voltage	1 V	C1	85.172 pF
Input Frequency	25 MHz	C2	8.782 pF
Output Frequency	200 MHz	R1	3.2168 KΩ
Charge Pump Current	50 μA	Phase Margin	57 °
Divided by N	8	Loop Bandwidth	1.8 MHz
VCO Gain	625 MHz	Damping Factor	≈ 1.1
Simulated Results of PLL in a Standard 90-nm CMOS Process			
Locked Time	1.3 μsec	Output Jitter at 200 MHz	2.68 psec
Static Phase Error	45 psec	Total Power Consumption	4.8647 mW

EFFECT OF MOS CAPACITOR WITH GATE TUNNELING LEAKAGE ON PERFORMANCES OF PLL

The C_1 and C_2 capacitors of low-pass loop filter in PLL, as shown in Fig. 1, are replaced by MOS capacitors with different oxide thicknesses to investigate the impact of gate tunneling leakage on PLL performances. The capacitances of MOS capacitors C_1 and C_2 are 85.172 pf and 8.782 pf under gate voltage of 0.492 V, respectively. Fig. 2 shows the simulated control voltage (V_{CTRL}) transition waveform to find the locked time for MOS capacitors with different oxide

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thicknesses. The thin-oxide MOS capacitors (1-V NMOS and 1-V PMOS) have longer locked time and cause larger ripple voltage V_r than that realized with thick-oxide MOS capacitor (1.8-V NMOS), when the phase difference between V_{REF} and V_{BACK} is kept constant. The simulated static phase error (Δt) in time domain for the MOS capacitors with different oxide thicknesses is shown in Fig. 3. The thin-oxide MOS capacitors (1-V NMOS and 1-V PMOS) cause larger static phase error (Δt) than that of thick-oxide MOS capacitor (1.8-V NMOS). The simulated jitter under MOS capacitors with different oxide thicknesses in second-order PLL is shown in Fig. 4. The thin-oxide MOS capacitors (1-V NMOS and 1-V PMOS) cause larger jitter than that of thick-oxide MOS capacitor (1.8-V NMOS) in second-order PLL, due to the large ripple voltage at V_{CTRL} node.

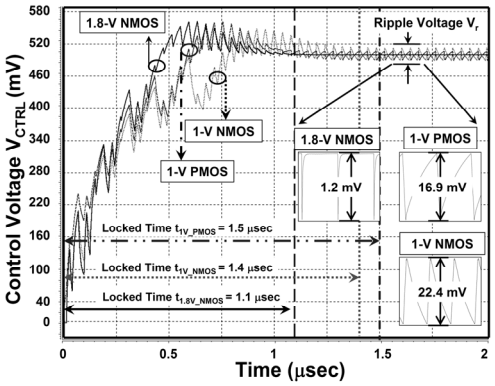

FIGURE 2. THE SIMULATED CONTROL VOLTAGE WAVEFORMS TO FIND THE LOCKED TIME UNDER MOS CAPACITORS WITH DIFFERENT OXIDE THICKNESSES IN SECOND-ORDER PLL.

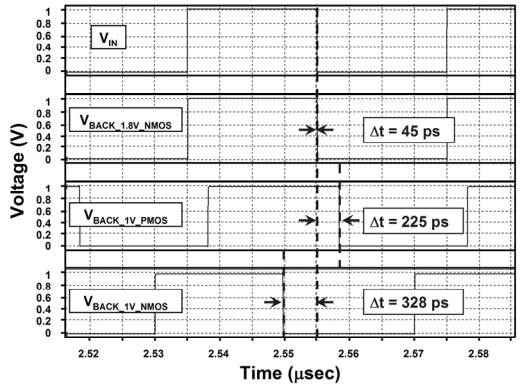

FIGURE 3. THE SIMULATED VOLTAGE WAVFORMS TO FIND THE STATIC PHASE ERROR (Δt) UNDER MOS CAPACITORS WITH DIFFERENT OXIDE THICKNESSES IN SECOND-ORDER PLL.

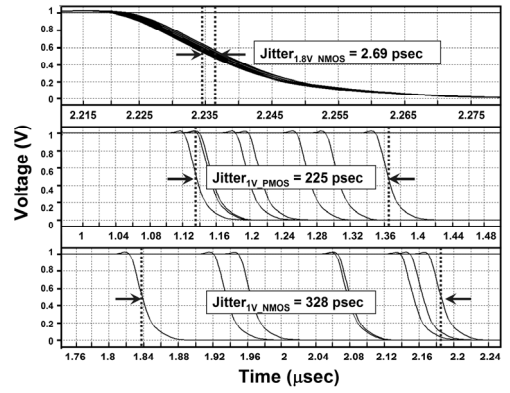

FIGURE 4. THE SIMULATED VOLTAGE WAVEFORMS TO FIND THE JITTER UNDER MOS CAPACITORS WITH DIFFERENT OXIDE THICKNESSES IN SECOND-ORDER PLL.

The dependence of different input signal frequencies on jitter and ripple voltage under different oxide thickness in the MOS capacitor is shown in Fig. 5. The high input signal frequency of V_{REF} has a small jitter, and low input signal frequency has a large jitter in second-order PLL with gate tunneling leakage.

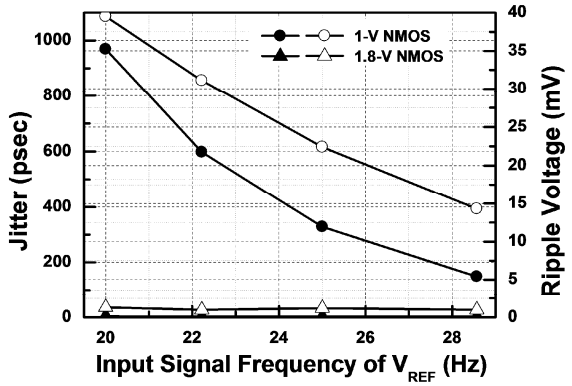

FIGURE 5. THE DEPENDENCE OF DIFFERENT INPUT SIGNAL FREQUENCIES ON JITTER AND RIPPLE VOLTAGE UNDER DIFFERENT OXIDE THICKNESS DEVICES IN THE MOS CAPACITOR.

CONCLUSION

The influence of gate tunneling leakage on circuit performances of second-order PLL has been analyzed and investigated in a standard 90-nm CMOS process. The locked time, static phase error, and jitter of second-order PLL are all degraded by gate tunneling leakage of MOS capacitor in loop filter. The MOS device with high threshold voltage and thick oxide thickness can be used to realize the MOS capacitor in the loop filter for achieving low-jitter and low-cost second-order PLL. The new circuit design technique on loop filter realized with thin-oxide MOS capacitor in PLL should be further developed to compensate such gate leakage issue in nanoscale CMOS technology.

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