# High-Speed Multilevel Wrapped-Select-Gate SONOS Memory Using a Novel Dynamic Threshold Source-Side-Injection (DTSSI) Programming Method

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***Abstract*—A high programming speed with a low-power-consumption wrapped-select-gate poly-Si-oxide-nitride-oxide-silicon memory is successfully demonstrated using the novel dynamic threshold source-side-injection programming technique. The select gate embedded in such particular memory structure acts like a dynamic MOSFET resulting in programming current ($I_{\rm PGM}$) that can be enhanced in this DT mode, easily attaining a high programming speed of about 100 ns. It still doubles the memory density by achieving the 2-bit/cell operation with MLC under DT mode.**

***Index Terms*—Dynamic-threshold, memory, poly-Si-oxide-nitride-oxide-silicon (SONOS).**

## I. Introduction

RECENTLY, traditional poly-Si-oxide-nitride-oxide-silicon (SONOS) memory devices have encountered considerable challenges and demands, such as increasingly serious short-channel effects, nitride storage layer thickness reduction, lower write/erase voltage, and critical gate injection current [1]. As the device is scaled down, short-channel-effect control becomes increasingly difficult when attempting to adjust the doping profiles at the channel and pocket without degrading device performance [2]. This implies that both performance and excessive memory power consumption must be simultaneously considered if the conventional channel-hot-electron method is to be used in programming [3].

In order to solve the lower program-efficiency problem, source-side-injection (SSI) was developed for high-speed and low operation voltage in EPROM with a sidewall gate structure (called SIEPROM) [4]. By applying a similar scheme, excellent SONOS memory characteristics with higher data retention and endurance in a particular memory structure has been demonstrated [5]. In addition, SONOS memories with the multiple-bit-cell and multiple-level-cell (MLC) scheme, to increase density without increasing die size, have been intensively studied [6].

In this letter, a high-performance wrapped-select-gate (WSG)-SONOS Flash memory with high density is developed using a dynamic threshold SSI (DTSSI) programming method. A faster programming speed with quite low power consumption was easily achieved while maintaining highly reliable endurance and retention.

## II. Device Structure and DTSSI Scheme

Fig. 1 shows the cross section of the WSG-SONOS memory structure with 2-bit/cell operation, an equivalent cell size is 3.5 $F^2$ for each bit here by using 0.18-$\mu$m node technology [7], [8]. The top oxide, nitride, and bottom oxide thickness are 10, 8, and 5 nm, respectively. The WSG ($n^+$-poly-Si, $L/W = 0.18\ \mu{\rm m}/0.36\ \mu{\rm m}$) acts as an assistant gate for accomplishing the high-speed MLC operation with DTSSI. The thickness of the isolation nitride on the top of the selected gate was $\sim$100 nm. The material of the word gate was $n^+$-poly-Si. In this letter, the operation scheme of DTSSI (DT mode) was executed by connecting the WSG to p-well electrically under programming, as shown in Fig. 1, implying the $V_{\rm th}$ of an embedded MOSFET in WSG-SONOS memory should be smaller than 0.7 V, or the parasitical bipolar junction leakage current will boost violently. The constant current (0.1 $\mu$A) method was utilized here to define the $V_{\rm th}$ of WSG-SONOS memory. Additionally, band-to-band hot-hole (BTBHH) erase was used to recombine the electrons in the nitride storage layer [8].

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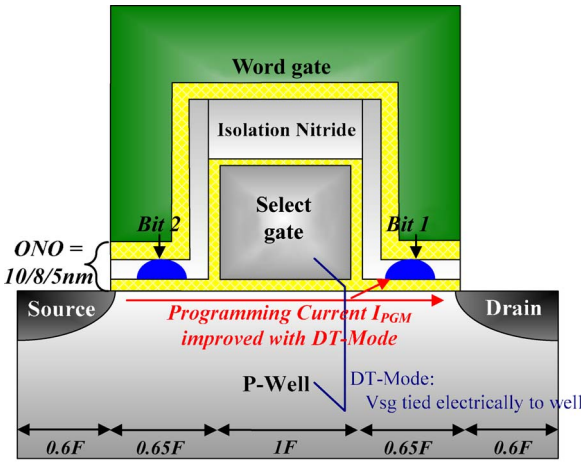


| Multi-level states: "10" state、"01" state、"00" state<br>DT-Mode: $V_{WL}$=8V、$V_{WL}$=9V、$V_{WL}$=10V<br>Normal-Mode: $V_{WL}$=9V、$V_{WL}$=10V、$V_{WL}$=11V | | | | | | |
|---|---|---|---|---|---|---|
| Bit 1 operation | Mode | $V_{WL}$ | $V_D$ | $V_S$ | $V_{SG}$ | $V_{Well}$ |
| Program | DT | 8~10V | 4V | 0V | 0.45V | 0.45V |
| | Normal | 9~11V | 4V | 0V | 0.45V | 0V |
| Erase | Normal | -4V | 6V | 0V | 0V | 0V |
| Read | Reverse | Sweep 0-6V | 0V | 1.8V | 1.6V | 0V |

Fig. 1. Cross section with operation scheme under DT and normal mode of WSG-SONOS memory.

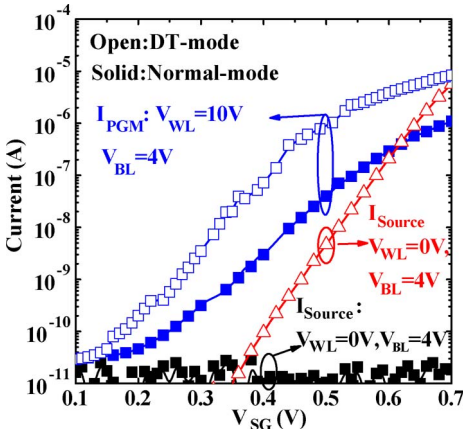


Fig. 2. $I_{\mathrm{PGM}}$–$V_{\mathrm{SG}}$ characteristics of WSG-SONOS memory under DT and normal modes, respectively.

## III. Results and Discussion

Fig. 2 shows the $I_{\mathrm{PGM}}$–$V_{\mathrm{SG}}$ of WSG-SONOS memory under DT and normal mode under the same programming condition ($V_{\mathrm{WL}} = 10$ V, $V_{\mathrm{BL}} = 4$ V). In DT mode, the threshold voltage ($V_{\mathrm{th}}$) will decrease dynamically due to body effect [9]. As a result, the programming current ($I_{\mathrm{PGM}}$) at DT mode can be greatly enhanced, up to 450% over normal mode at the range of $V_{\mathrm{SG}} = 0.25 \sim 0.65$ V. Although the programming current is greatly enhanced, it is only 4 $\mu$A in the extreme condition ($V_{\mathrm{SG}} = 0.65$ V), as shown in Fig. 2. This makes low-power operation possible. In addition, the junction leakage characteristics of the WSG-SONOS memory under DT and normal modes are also shown in Fig. 2. In an exemplary array of a NOR-type architecture, the junction turn-on voltage of the well-source is about 0.64 V. However, the select gate voltage is only 0.45 V while operated under DTSSI where junction leakage is still lower than 1 nA, indicating the major enhancement of $I_{\mathrm{PGM}}$ comes from the increase of inversion charge density [9]. The total leakage current will be high (in milliamperes) when the block size of memory is larger than 1 MB. Hence, a suitable block size needs to be compromised between program speed and power consumption.

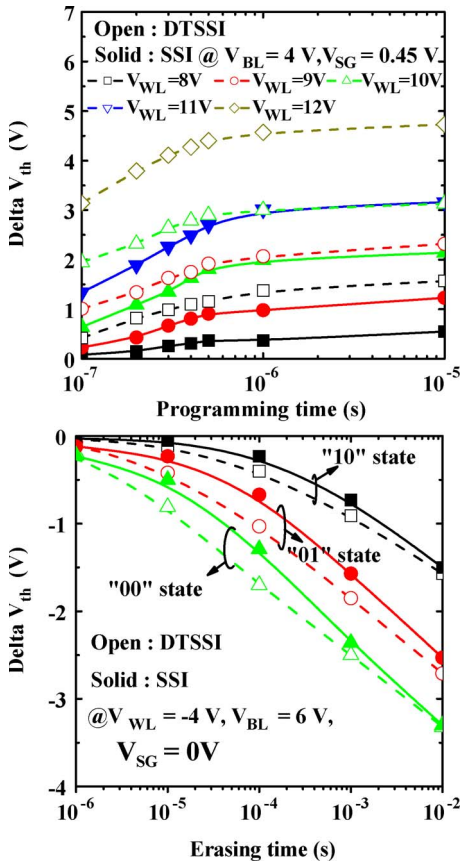


Fig. 3. High program and erase speed of MLC WSG-SONOS memory in DT and normal modes.

The programming characteristics of the WSG-SONOS memory under DT and normal mode are shown in Fig. 3. Clearly, the memory window can be substantially increased when the device is operated using the DTSSI technique. In DT mode, the $V_{\mathrm{th}}$ shift exceeds 1 V ("10" state), 2 V ("01" state), and 3 V ("00" state) at $V_{\mathrm{SG}} = 0.45$ V, while the programming time of the MLC operation is only 1 $\mu$s for $V_{\mathrm{WL}} = 8,\ 9,$ and 10 V, respectively. Furthermore, the MLC was achieved in a very short writing time of only 100 ns when $V_{\mathrm{WL}} = 9,\ 10,$ and 12 V were applied in DT mode. In addition, Fig. 3 also shows the erasing characteristics of the MLC of the WSG-SONOS memories. Here, the initial states before erasing are programmed to "10," "01," and "00" states under each modes, respectively, and the BTBHH erasing voltage was used at $V_{\mathrm{WL}} = -4$ V and $V_{\mathrm{BL}} = 6$ V. The MLC erasing characteristics of the WSG-SONOS memory can be realized in DT mode at a higher speed

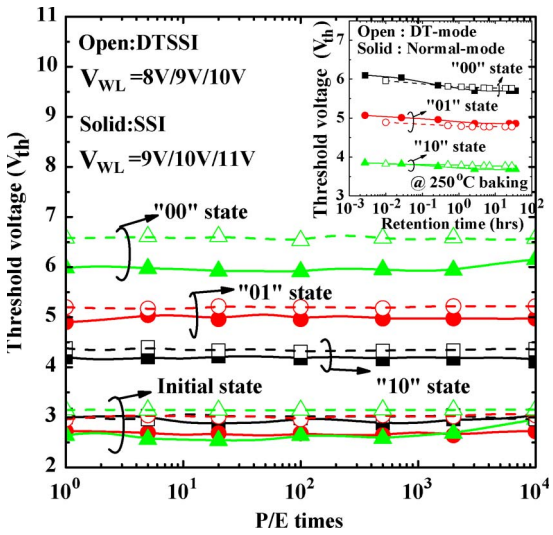


Fig. 4. Endurance characteristics with different multilevel states of WSG-SONOS memory by DT and normal modes (at $V_{\rm BL} = 4$ V, $V_{\rm SG} = 0.45$ V), cycling up to $10^4$ times, respectively. Inset shows data retention characteristics with multilevel operation under both modes at high-temperature 250 °C baking. The cell is uncycled.

than in normal mode. This is due to the spatial distribution of the charge storage layer under DT mode which is dissimilar to normal mode [10].

Fig. 4 shows the endurance characteristics of the WSG-SONOS memory with MLC operation under DT and normal mode, respectively. The MLC operation is programmed with $V_{\rm WL} = 9,\ 10,$ and 11 V in normal mode, and $V_{\rm WL} = 8,\ 9,$ and 10 V in DT mode for 1 $\mu$s. The bit-line voltage remains at 4 V while programming under DT and normal mode. The MLC memory window is almost identical even after 10-k P/E cycling. In normal mode, however, the window of the "00" state is preserved, but both values increase with repeated cycling, indicating incomplete erasure [11], or more interface state generation in the bottom oxide [12]. On the other hand, DT mode exhibits a better P/E cycling performance, resulting in a negligible $V_{\rm th}$ shift owing to the lower word-gate bias, which normally induces interface-state generation at high-voltage bias. Thus, the DTSSI scheme can also improve the reliability of the WSG-SONOS under MLC operation.

The data retention characteristics of the WSG-SONOS memory under DT and normal mode are shown in the inset of Fig. 4. Initially, the charge loss results from the detrapping process in which the trapped electrons tend to migrate and redistribute in the silicon nitride under high-temperature operation [13]. Fortunately, this charge loss saturates and the different states of multilevel operation can easily be discerned. The $V_{\rm th}$ shift of the "00" state is less than 0.2 V even after 28 h at extremely high-temperature (250 °C) baking in DT mode.

## IV. Conclusion

A high-performance and highly reliable 2-bit/cell MLC WSG-SONOS memory using the novel DTSSI technique is successfully demonstrated in this letter. Under DTSSI, extremely fast 100-ns cell writing time in the WSG-SONOS memory at very low power consumption can be achieved. Furthermore, improved reliability in data retention and greater endurance were also demonstrated in the WSG-SONOS memory with DTSSI operation.

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