國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

多重感測器讀取之可調式增益介面電路三軸加速度計單晶設計

Design of Three-axis Accelerometer with Tunable Gain Interface for Multi-sensors

研究生：林執中 Chih-Chung Lin

指導教授：溫瓌岸 博士 Dr. Kuei-Ann Wen

中華民國一〇二年九月

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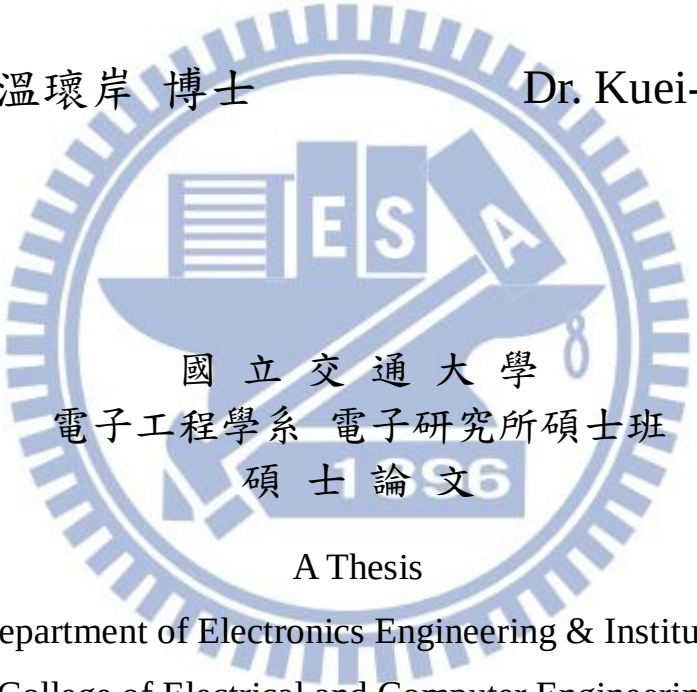

國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

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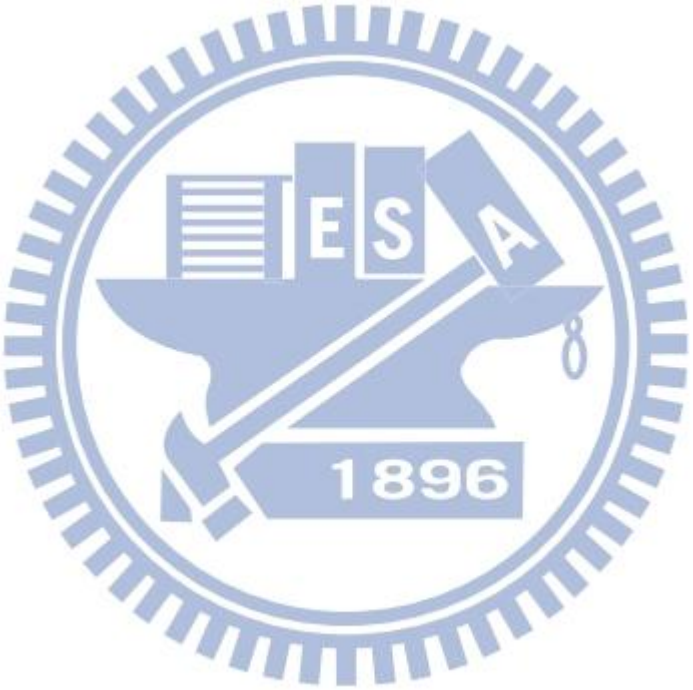
摘　要

本論文提出一單晶片採用分時多工之多種感測器讀取之可調式增益介面電路三軸加速度計設計。而此感測系統在標準 0.18um 製程下製作。此讀出電路的輸入等效雜訊在 100Hz 的頻寬下爲 65.4 nV/√Hz，功率消耗爲 14.16μW，靈敏度爲 100mV/g，加速度計操作範圍設計在-4g 到 4g。在本設計中，三軸加速度計的電容變化值相近，所以只需一組讀出電路。X，Y，Z 三軸的電容變化在施加 1g 的加速度下模擬分別爲 0.37,0.4,0.33fF。而一個擁有較小電容值變化的感測器也在此設計中。此感測器的電容值變化在施加 1g 的加速度下爲 15aF。本讀出電路設計由四級組成。第一級爲一個使用雙相關取樣的電容轉電壓轉換器。此級可以

減小放大器的偏移、閃爍雜訊、開關的電荷注入，和 kT/C 雜訊。此外，在第一級的控制訊號可以決定要讀取哪一個感測器。第二級也使用雙相關取樣去放大第一級的輸出信號，並且減小放大器的非理想效應。第三級爲一個積分器，而積分器的增益是和積分電容成反比。因此，藉由調整積分電容可以完成可調增益的功能，使不同的感射器擁有相似的輸出振幅。第四級爲採樣和維持。藉由從第一級產生的四組控制訊號，它可以分開從積分器輸出的混和訊號，始分時多工得以完成。



Design of Three-axis Accelerometer with Tunable Gain Interface for Multi-sensors

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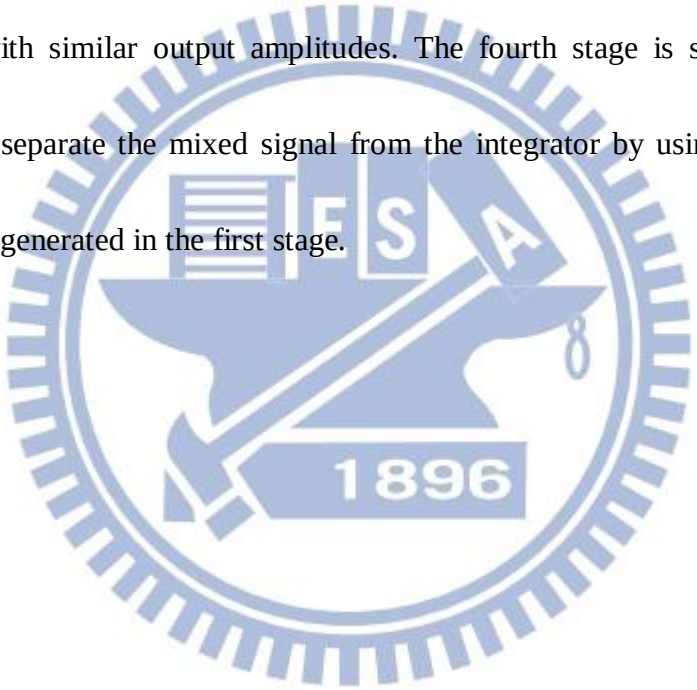
ABSTRACT

A monolithic three-axis accelerometer with tunable gain analog front end circuit using time division to read multi-sensors signals in 0.18μm CMOS MEMS process is proposed. The circuit input referred noise is 65.4 $nV/\sqrt{Hz}$ under 100Hz, the power consumption is 14.16μW, the sensitivity is 100mV/g and the linear range is +/- 4g. In this design, the three-axis accelerometer capacitance changes are designed with similar mechanism, so a single read out circuit can be used. The X, Y, Z axis capacitance changes under 1g acceleration are simulated to be 0.37,0.4,0.33 femtofarad respectively. An additive sensor with smaller capacitance change under 1g acceleration of 15 attofarad is also designed in. The universal readout circuit schematic composes four stages. The first stage is a capacitance to voltage convertor

combining with correlated double sampling to reduce the interference from amplifier offset, flicker noise, charge injection, and kT/C noise. In addition, the control signal can decide which sensors to be read. The second stage also uses CDS technique to amplify signals from the first stage and to suppress the non-ideal effects. The third stage is an integrator, and the gain is inversely proportional to integration capacitance. In this way, tunable gain can be achieved by adjusting integration capacitance to make two sensors with similar output amplitudes. The fourth stage is sample and hold (S&H). It can separate the mixed signal from the integrator by using four different control signals generated in the first stage.



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林執中

2013 年 7 月

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List of Figures and Tables

Chapter 1 Introduction

Recently, accelerometers are widely applied to a variety of consumer applications. With integrated circuit process technology growing mature, MEMS (Micro Electro Mechanical System) mechanical components [1] [2] are integrated into readout circuit, making future products tend to be integrated, miniaturized, low prices, and low power consumption. Therefore, monolithic CMOS (Complementary Metal Oxide Semiconductor) MEMS sensors integrated with circuits will be applied to wide range of applications. In this thesis, a monolithic three-axis accelerometer with tunable gain analog front end circuit using time division to read multi-sensors signals in 0.18um CMOS MEMS process is presented. By using some non-overlapping control signals and variable gain amplifier, a sole readout circuit can be designed to read three-axis signals and an additional sensor with smaller capacitance change.

1.1 Motivation

In MEMS applications, a CMOS MEMS accelerometer has superiorities of low power dissipation, low temperature coefficient, and simple structure. However, CMOS MEMS accelerometers fabricated by standard IC (Integrated Circuit) process have small sensing capacitance (usually is several femtofarad) with operating frequency under several hundred Hz. Therefore, the major design target is to reduce low frequency noise and DC offset introduced from readout circuit. Besides,

accelerometers are used extensively for portable devices, so low power consumption is also a significant consideration. The CDS (Correlated Double Sampling) [3-9] technique can reduce low frequency noise and DC offset by extracting signals from the difference of the two non-overlap phases to reduce the amplifier offset, l/f noise, charge injection, and kT/C noise. In the proposed architecture, only CDS is used. According to [3], there are three different CDS techniques: I. Gain Uncompensated SC (Switch Capacitance) Amplifier, II. Narrowband Gain Compensated SC Amplifier, and III. Wideband Gain-Compensated SC Amplifier. The second technique is chosen because sensors signals are normally slow, and these signals are not moderated to high frequency in this design, so amplifiers in readout circuit can be designed with narrow bandwidth, with low bias DC current to reduce power dissipation. Furthermore, this circuit technique does not need a reset of the output. Therefore, the op-amp slew rate and settling time are relaxed, making power consumption lower.

Lately, various kinds of sensors such as accelerometers, gyroscopes, piezometers, magnetometers and so on are packed in a single control system like smart phone. The sensitivities of these sensors are usually in different levels, for example, the sensitivities of magnetometers are generally 30~40 times smaller than accelerometers. Due to the sensors different sensitivities, various kinds of sensors need multiple sets of readout circuit and cause not only bigger area but also more power consumption.

Therefore, if a single universal readout circuit can adjust gain in a large range to provide different sensors with similar sensitivities and can distinguish different sensing signals, then the chip area can be smaller and the power dissipation can be lower.

With monolithic CMOS process of MEMS and ASIC (Application-Specific Integrated Circuit) being available, it is possible to integrate more sensors as well as more circuitries on the same substrate. This work is trying to develop novel design to have a sole readout circuit for multiple sensors with different scales of sensitivity levels. With tunable gain stage being designed, it will be possible to make the sensor integration being more compact for low power and small area applications.

1.2 Organization

The thesis presents the highly integrated C to V circuit with the one three-axis accelerometer. In chapter 2, introduction and implementation of the three-axis MEMS accelerometer will be presented. The proposed readout C-to-V circuit will be reported in chapter 3. In chapter 4, co-simulations and implementation of the circuit with the accelerometer will be presented. In chapter 5, the measurement results will be displayed. The conclusion and future work will be given in chapter 6.

Chapter 2 CMOS MEMS Accelerometer

2.1 CMOS MEMS Fabrication

2.1.1 Process

The CMOS MEMS process consists of two parts. First part is TSMC 0.18μm mixed-signal/RF CMOS process. This process includes one poly-silicon layer and six metal layers, and the layer definition is illustrated in Figure 2.1 [10].

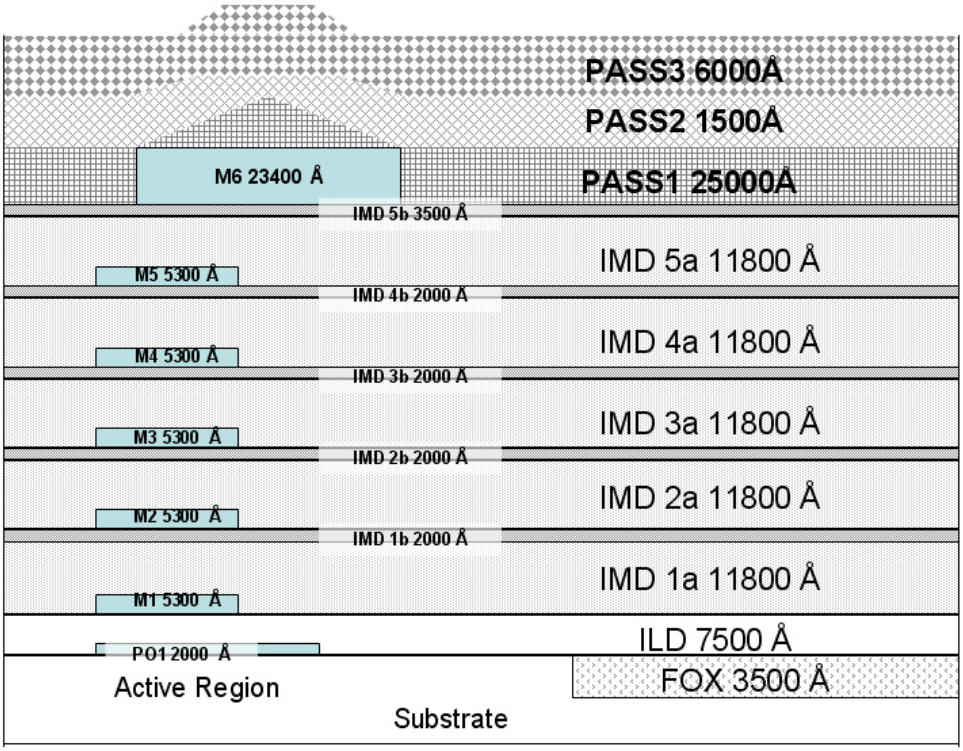


Figure 2.1: Cross section view of CMOS layers [10]

The second part is the micromachining process. After the standard CMOS process, the passivation layer above the microstructure which can protect the circuit is removed. For post micromachining process, an RLS mask is defined to pattern the photoresist (PR), and the area without PR is etched by both the anisotropic silicon oxide dry

etching (DRIE, Figure 2.2 (b)) and the isotropic silicon substrate dry etching (Figure 2.2 (c)). The microstructures will be released after the isotropic silicon substrate dry etching.

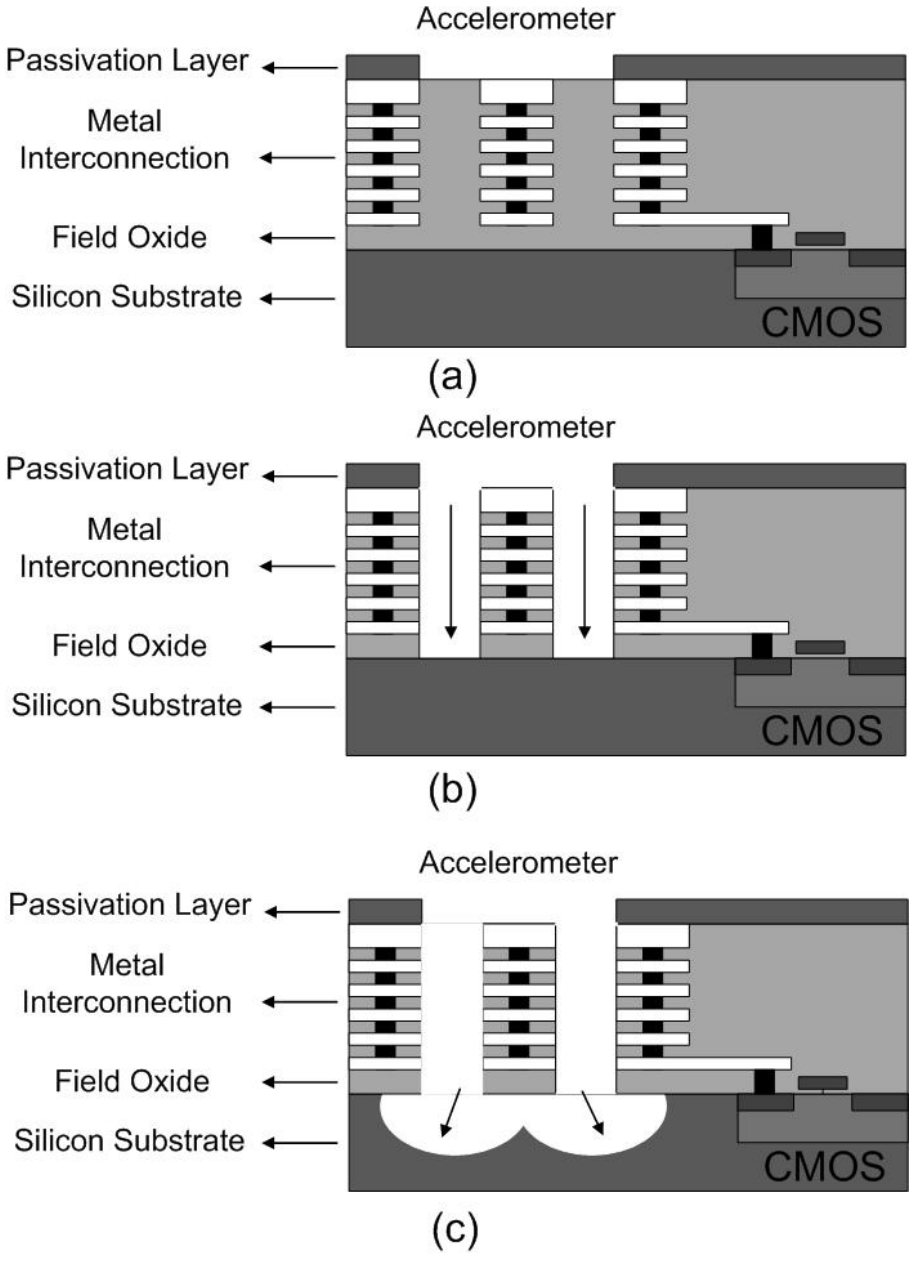


Figure 2.2: Cross-section view of MEMS process flow: (a) After completion of CMOS, (b) After anisotropic oxide etching, and (c) After isotropic substrate etching to release the accelerometer

2.1.2 CMOS MEMS Layout Rules

MEMS design should obey both the design rule of TSMC CMOS Process and CIC (National Chip Implementation Center) CMOS MEMS process to construct the structure of CMOS / MEMS devices successfully and avoid to damaging CMOS circuits. The definitions of layout locations of multiple layers are shown in Figure 2.3 and are used to define the distance constrains. In CMOS process, the passivation mask (PAD) is used to define the MEMS structure part and remove the silicon-nitride (passivation). To ensure the oxide etching process, PAD mask needs to overlap the RLS mask which defines the area for doing post etching process and is illustrated in Figure 2.4.

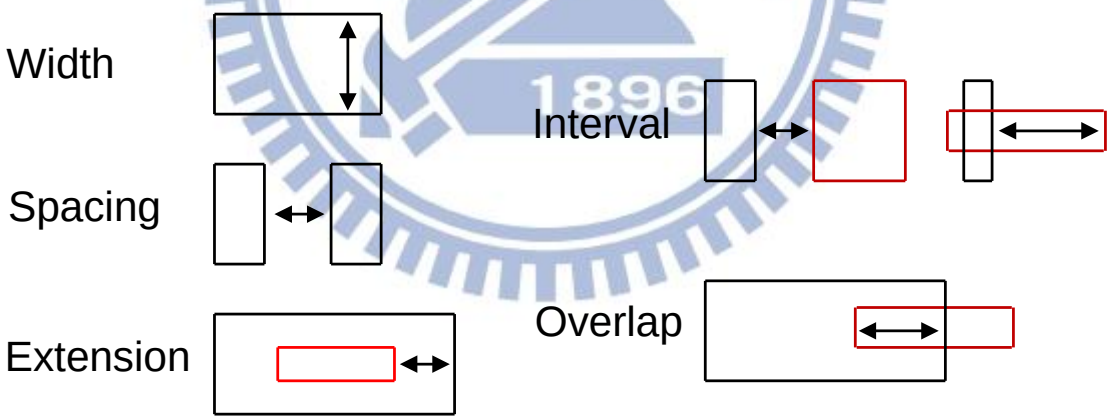


Figure 2.3: The definitions of layout locations

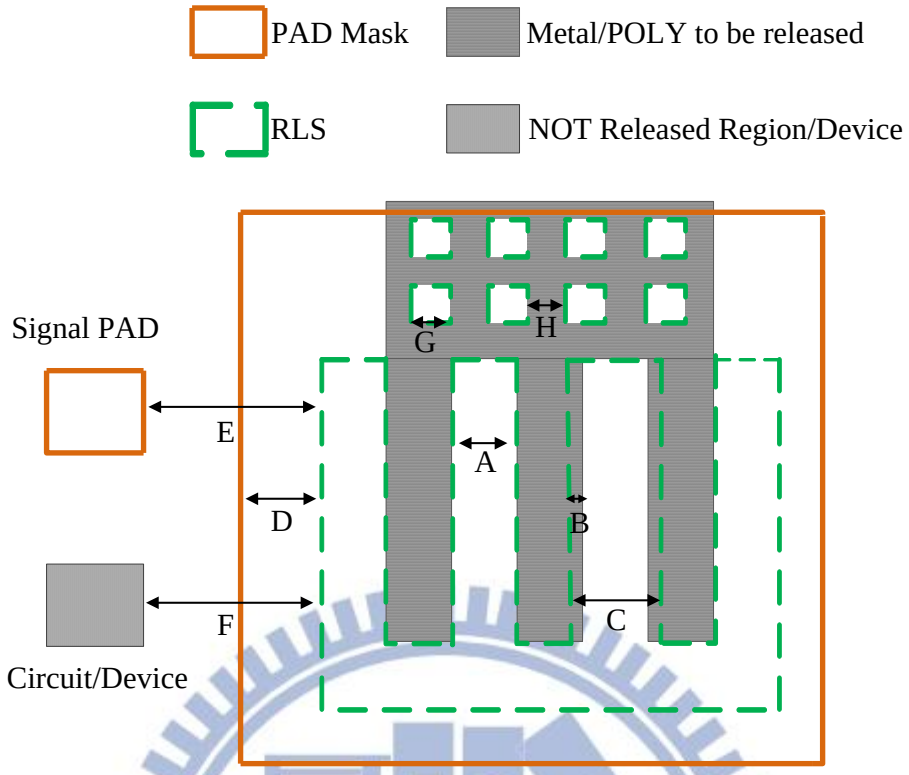


Figure 2.4: RLS-mask design rule

In CMOS process, the RLS mask defines the MEMS etching region, and the design rules are shown in Table 2.1 [10] and Figure 2.3. Using large metal region as the hard-mask (overlap with RLS mask) will cause polymer, so the metal width overlapping with RLS mask is limited to 1 μm. In addition, because the silicon substrate in the RLS region will be etched, electronic circuits are not allowed in or near the RLS region. The latest RLS design roles for square etching holes limit that the ratio of the lateral undercut with respect to the width of etching hole is 1:1, and the width of etching hole is limited to be equal to 8μm. However, this constrain still needs to be discussed.

Table 2.1: The definitions of RLS-mask in CMOS MEMS process [10]

Rule #	Description	Rule (μm)
RLS.PASS.1	Min./Max. extension of PAD mask over RLS mask	A 1um
RLS.W.1	Min. Width of RLS	A 4μm
RLS.W.2	Exact Width of RLS etching hole in proof mass	G 8μm
RLS.W.3	Exact Width of frame in proof mass	H 8μm
RLS.METALx.1	Max. overlap of RLS on Metal (For using Metal as hard mask)	B 1μm
RLS.Poly.1	Overlap of RLS on POLY should be avoided	B 0μm
RLS.S.1	Min. Spacing between RLS regions	C 4μm
RLS.PASS.1	Min./Max. extension of PAD mask over RLS mask	D 1um
RLS.PASS.2	Min. Interval between wide RLS (width > 25um) and SIGNAL PAD	E 100μm
RLS.PASS.3	Min. Interval between RLS (width =< 25um) and SIGNAL PAD	E 50μm
RLS.ACTIVE.1	Min. Interval from wide RLS (width > 25um) to component with Substrate doping	F 100μm
RLS.ACTIVE.2	Min. Interval from RLS (width =< 25um) to component with Substrate doping	F 50μm
RLS.CO.W.1	Min. and Max. width of CONTACT	W 0.22 um
RLS.VIA1-4.W.1	Min. and Max. width of VIA1-4	W 0.26 um
RLS.VIA5.W.1	Min. and Max. width of VIA5	W 0.36 um

2.2 The Three-Axis Accelerometer Design

2.2.1 Working Principle of Accelerometer

The schematic of the three-axis accelerometer is shown in Figure 2.5 [8]. The three-axis accelerometer is composed of the proof mass, etching holes, comb fingers, springs, torsional beams and the ridge frame. The rigid frame is designed to handle the comb fingers curling problem. The etching holes can make the proof mass to suspend by DRIE process. The three-axis accelerometer structure can be simplified to be a mass-spring-damper system. The working principle of the three-axis accelerometer is that the external acceleration generates an inertial force on the proof mass. Then the proof mass drives electrode plates to move, producing a capacitance change (ΔC) with fix electrode plates. Because the sensing principles of X, Y axis and Z axis are different, I separate the three-axis accelerometer to two parts for easier explanation.

First, the schematic of the X, Y axial accelerometer is shown in Figure 2.6 and can be simplified to be a mass-spring-damper system as shown in Figure 2.7. The direction of X axis and Y axis acceleration can be sensed by moving the electrode plates as shown in Figure 2.8 (a).

The inertial force caused by acceleration induces the displacement of the proof mass. By using the mass-spring-damper system (Figure 2.6), the motion of the

accelerometer can be described as differential equation

$$m\ddot{x} + b\dot{x} + kx = ma_{in} \tag{2.1}$$

where m, b, k, a_{in}, and x are the mass of the accelerometer, the damping coefficient, the spring constant, the external acceleration, and the displacement of the proof mass. Therefore, the accelerometer is equivalent to the two fully differential capacitances as shown in Figure 2.8 (b) where C_s is the stationary capacitances and ΔC is the capacitance change. The relation between C_s andΔC can be described as

$$\Delta C = \frac{Cs*X}{d} \tag{2.2}$$

where d is the gap between two comb fingers and X is the displacement of the proof mass. This capacitance change can be read by the designed readout circuit and the value of the external acceleration can be decided. Taking Laplace transform of Eq. (2.1), the transfer function of acceleration to displacement in s-domain is

$$\frac{X(S)}{A_{in}(S)} = \frac{1}{s^2+s\frac{b}{m}+\frac{k}{m}} = \frac{1}{s^2+s\frac{\omega_n}{Q}+{\omega_n}^2} \tag{2.3}$$

where $Q = \frac{m\omega_n}{b}$ is designed to affect the setting time for open-loop operation of the accelerometer and $\omega_n = \sqrt{\frac{k}{m}}$ is the natural frequency.

With the first order approximation from Eq. (2.1), and because the input frequency is much lower than the natural frequency ω_n, the equation of mechanical sensitivity could be simplified as

$$\frac{x}{a_{in}} = \frac{m}{k} = \frac{1}{{\omega_n}^2} \tag{2.4}$$

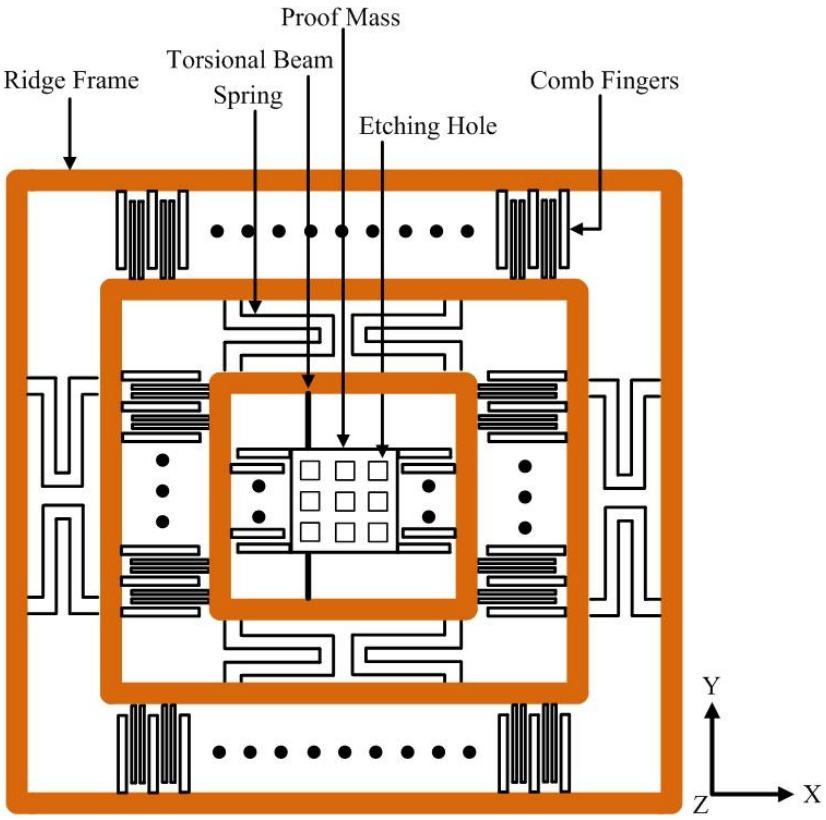


Figure 2.5: The three-axis accelerometer layout view

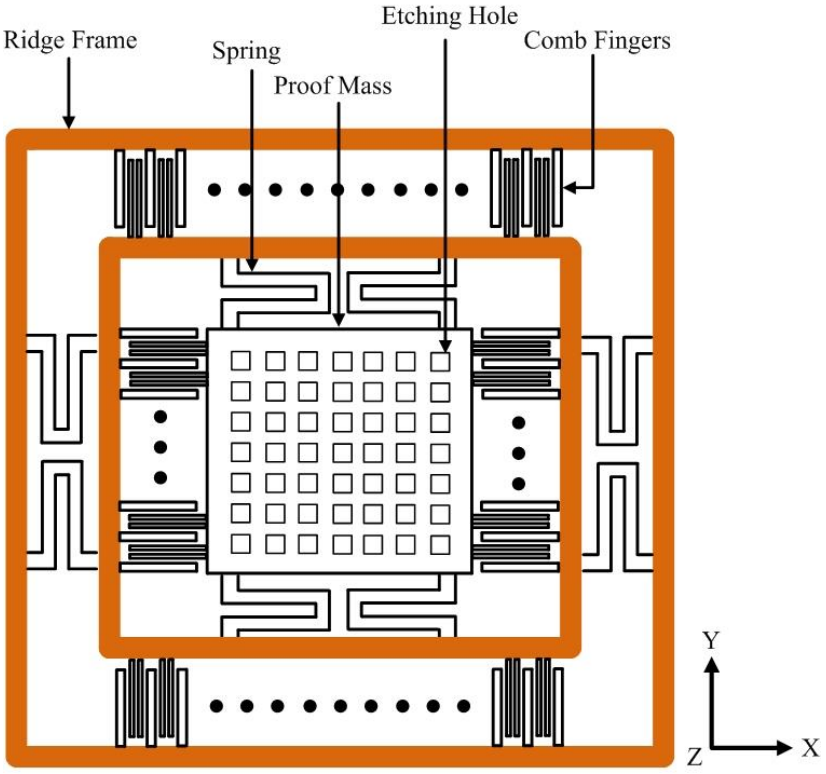


Figure 2.6: The accelerometer layout view of X, Y axis

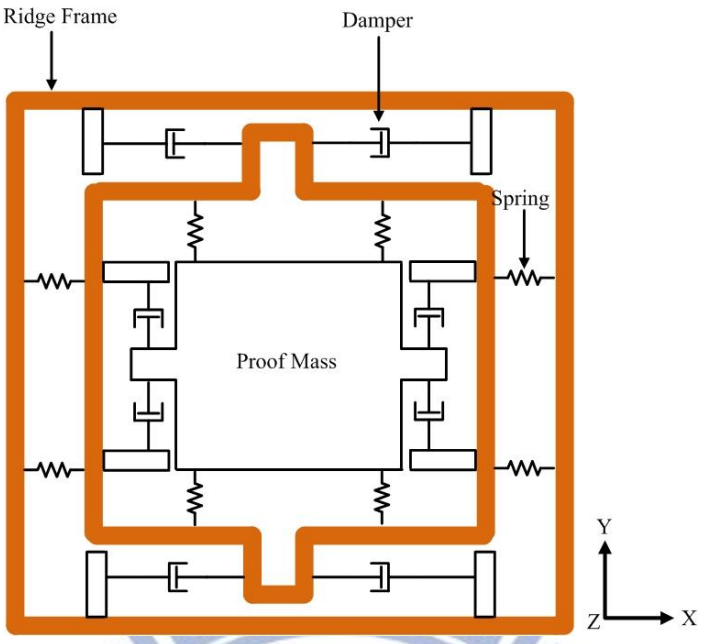
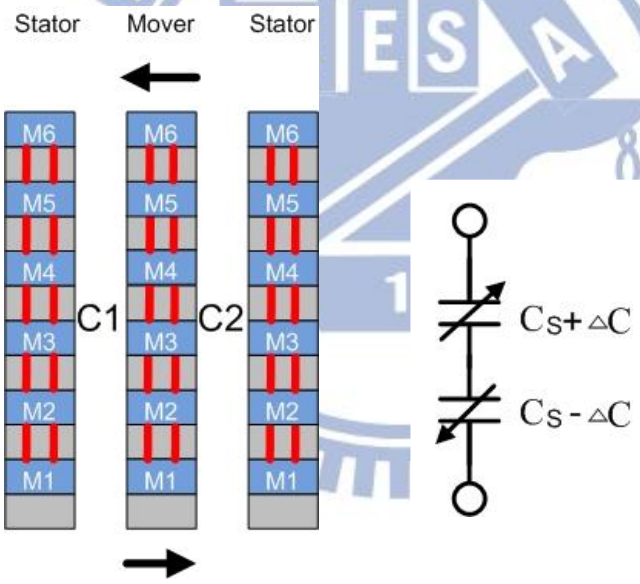


Figure 2.7: Mechanical parameter model of X, Y axis



(a) (b)

Figure 2.8: (a) The X, Y axis sensing fingers (b) The schematic of the equivalent capacitors

Second, the schematic of the Z axis accelerometer is shown in Figure 2.9 and can be simplified to be a mass-spring-damper system as shown in Figure 2.10. The

direction of Z axis acceleration can be sensed by rotating electrode plates as shown in Figure 2.11 (a). The inertial force caused by acceleration induces the rotation angle of the proof mass. However, because the rotation angle is small, it can be simplified as the displacement, and the relation between C_s andΔ C can be described as

$$\Delta C = \frac{Cs*X}{L} \tag{2.5}$$

where L is the thickness of metal 2 and metal 3 layers and one layer of oxide as shown in Figure 2.11 (a) and X is the displacement of the proof mass. Because the thickness of metal 2, metal 3, metal 4, metal 5 layers are the same, which is illustrated in Figure 2.1, the stationary capacitances C_1 and C_2 are matched. In addition, due to the rotation angle can be simplified as the displacement, the transfer function and the sensitivity of the Z axis accelerometer are the same as shown above. Like X,Y axis accelerometer, the Z axis accelerometer is equivalent to the two fully differential capacitances as shown in Figure 2.11 (b) where C_s is the stationary capacitances and Δ C is the stationary capacitance change.

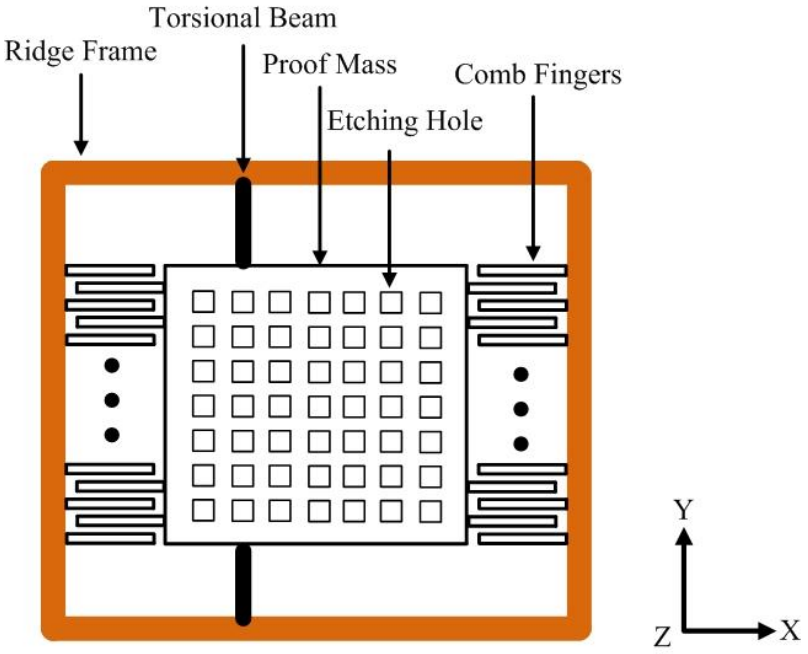


Figure 2.9: The accelerometer layout view of Z-axis

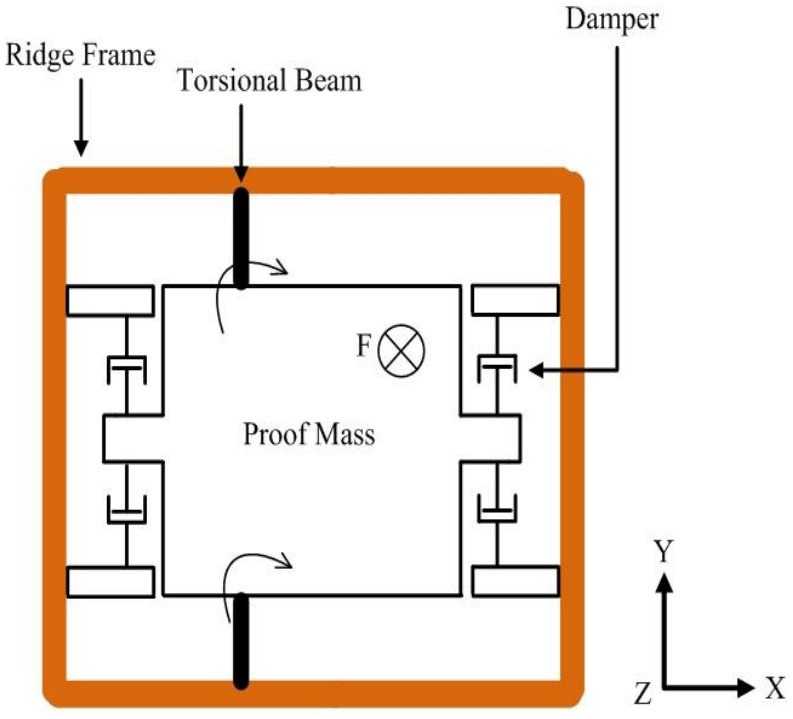


Figure 2.10: Mechanical parameter model of Z axis

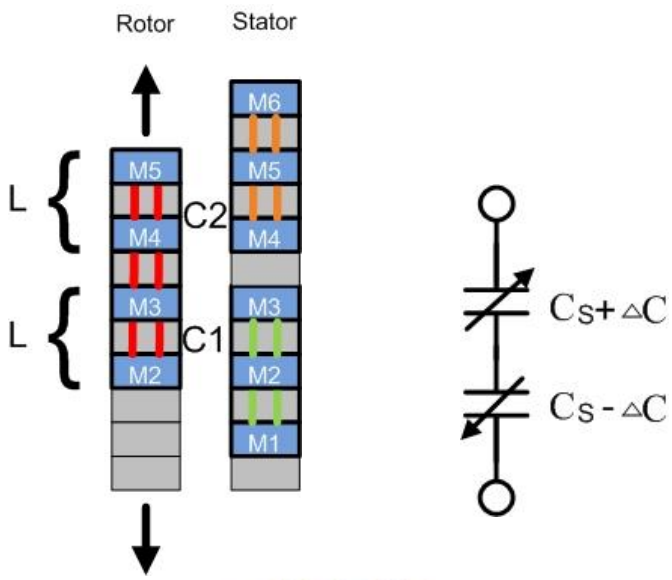


Figure 2.11: (a) The Z axis sensing fingers (b) The schematic of the equivalent capacitors

2.2.2 Spring Constant and torsional spring constant

Figure 2.12 shows the folded-beam spring used in the accelerometer. The spring constant is given by

$$k = Et\left(\frac{W}{L}\right)^3 / N \tag{2.6}$$

where k is the spring constant, E is the multilayer structure effective young's modulus of elasticity, t, W, L, and N are thickness, the width and length of the beam, and the turns, respectively. In accelerometer design, the width of beam is 4 μm, and the thickness of beam is about 10 μm.

The torsional beam is shown in Figure 2.13 and torsional spring constant k_t is [11]

$$k_t = \frac{2GW_s^3 t}{3L_s} \tag{2.7}$$

where G is the shear modulus, W_s, L_s and t are the width, length, and thickness of

the beam, respectively.

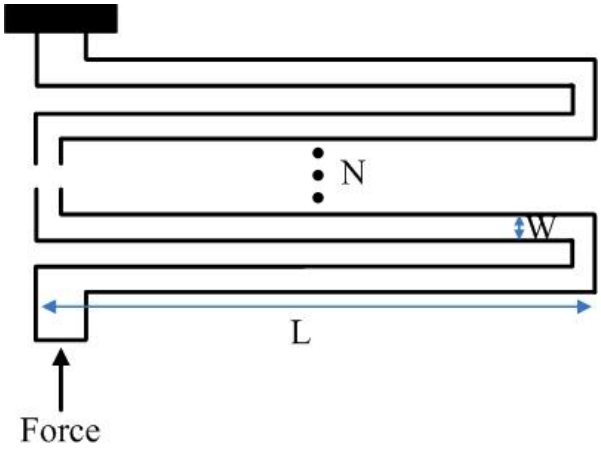


Figure 2.12: Folded-beam

Figure 2.13: Torsional-beam

2.2.3 Squeeze Film Damping

The squeeze film damping between the parallel-plate comb capacitor fingers in the out-of plane of the three-axis accelerometer is the dominant damper [8], and its formula is given as

$$b_{squeeze} = 7.2 N_{gap} \mu l_{ov} \frac{t^3}{d^3} \tag{2.8}$$

where $b_{squeeze}$, Ngap, μ, lov, t, d are squeeze film damping coefficient, the number of air gaps, the viscosity of the air, the finger overlap, thickness, and the initial gap between a rotor and stator, respectively. The μ value is 1.85×10^{-6} N · s/m^2 and the viscosity of the air under atmospheric pressure at the room temperature.

The shear damping between two parallel comb fingers is given as

$$b_{shear} = N_{gap}\mu\frac{A}{d} \tag{2.9}$$

where b_{shear}, Ngap, μ, A are the shear damping coefficient, the number of air gaps, viscosity of the air and the finger overlap area, respectively.

2.2.4 Brownian Noise

A direct consequence of air damping is the thermal-mechanical noise, a random force generated by the Brownian motion of ambient molecules and is called Brownian noise. For accelerometers, the power spectral density of the Brownian noise is

$$\overline{a_n^2} = \frac{4k_BTb}{9.8^2m^2}\ {}^{G^2}/_{Hz} \tag{2.10}$$

where k_B is the Boltzmann constant and equals to $1.381\text{x}10^{-23}$ JK^{-1}, T, b, m are the absolute temperature, the squeeze film or shear damping coefficient and mass, respectively.

2.3 Accelerometer Simulation

2.3.1 Microstructure Geometry Parameters

The three-axis accelerometer layout is first drawn in Cadance environment. After the three-axis accelerometer layout is finished, the layout file is imported to CoventorWare [12]. With the CMOS MEMS process file provided by the CIC, the imported layout file can be converted to a 3-D model as shown in Figure 2.14 and this 3-D model can be analyzed by mechanical simulations in CoventorWare. The process and material parameters of the designed three-axis accelerometer are listed in Table

2.2. The parameter of permittivity affects the value of sensing capacitance. The density of SiO_2 and Al are oxide and metal layers and they affect the weight of sensors. The designed geometry parameters of the accelerometer are listed in Table 2.3. The finger gaps of the accelerometer are design to be 4μm to follow the design rule. The size of etching hole is 7x7 μm^2 and the ratio of metal width to hole with is 5:7.

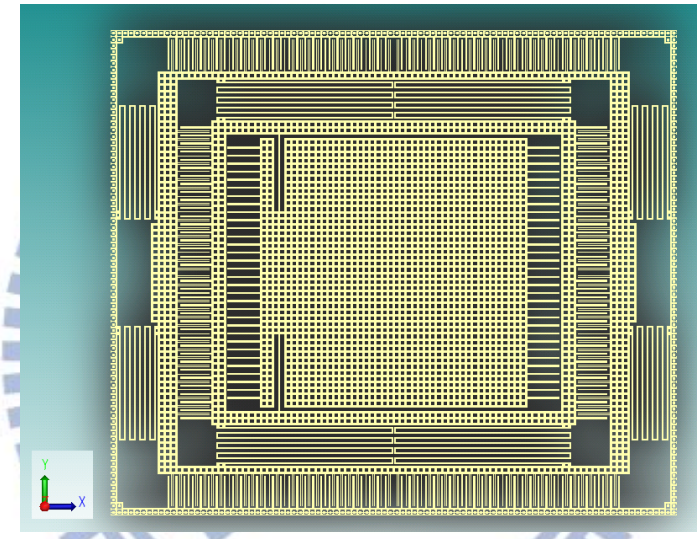


Figure 2.14: The 3D model of the 3-axis accelerometer

Table 2.2: Process and material parameters of the designed accelerometer

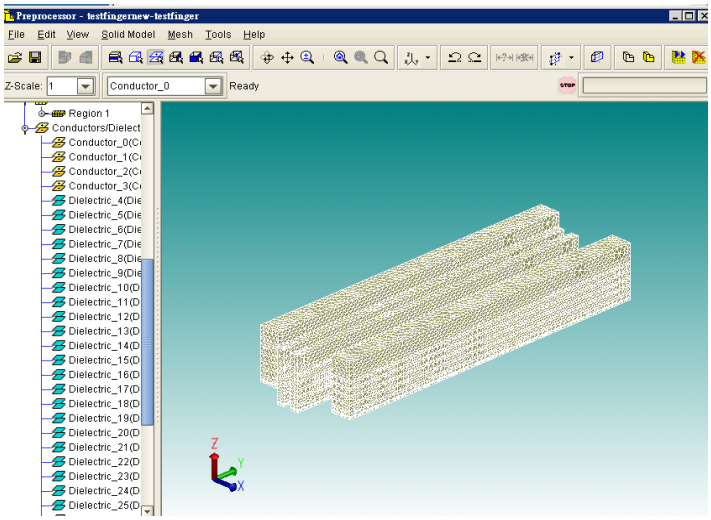
Process and Material parameters	
Temp(K)	293.15
Boltzmann(kb)	1.381E-23
Permittivity(Eox)	8.854E-18 F/μm
Young's modulus(SiO_2)	7.5E+10
Young's modulus(Al)	7.0E+10
Structure thickness(t)	10.49μm
SiO2 density	2.2E-15 kg/μm^3
Al density	2.3E-15 kg/μm^3
Viscosity(μ)	1.85E-6

Table 2.3: Designed accelerometer geometry parameters

Parameter		Value	Unit
Proof–mass	Area	533.2*533.2	μm^2
	Area of each holes	7*7	μm^2
	Pitch of each holes	5	μm
Comb-finger	No. of comb cells (X/Y/Z)	116/96/88	N/A
	Length of comb (X/Y/Z)	62.8/62.8/62.8	μm
	Width of comb (X/Y/Z)	4/4/4	μm
	Gap (X/Y/Z)	4/4/4	N/A
Folded-spring	No. of beam	4	N/A
	Width of beam	4	μm
	Length of beam (X/Y)	351.3/287.1	μm
	Gap	4	N/A
Rotated-beam	Width of beam	4	μm
	Length of beam	150.8	μm

2.3.2 Three-axis accelerometer Simulation

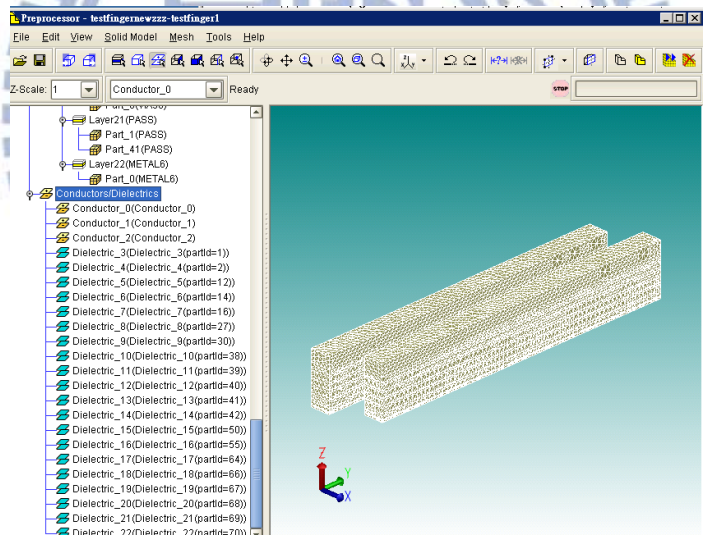
By using CoventorWare electrostatic analyzer, we can simulate the stationary capacitances of X, Y, Z axis in one pair of comb finger. Figure 2.15 (a) illustrates the stationary capacitances of X, Y axis in one pair of comb finger and Figure 2.15 (b) shows the stationary capacitances of Z axis in one pair of comb finger.



Capacitance Matrix (pF)

	Conductor_0	Conductor_1	Conductor_2	Conductor_3
Conductor_0	6.949437E-03	-3.246606E-04	-2.151399E-03	-4.47337E-03
Conductor_1	-3.246606E-04	3.015967E-03	-5.385008E-04	-2.152811E-03
Conductor_2	-2.151399E-03	-5.385008E-04	3.015143E-03	-3.252483E-04
Conductor_3	-4.47337E-03	-2.152811E-03	-3.252483E-04	6.951432E-03

(a)



Capacitance Matrix (pF)

	Conductor_0	Conductor_1	Conductor_2
Conductor_0	1.292957E-02	-1.159883E-02	-1.330732E-03
Conductor_1	-1.159883E-02	1.279348E-02	-1.194655E-03
Conductor_2	-1.330732E-03	-1.194655E-03	2.525385E-03

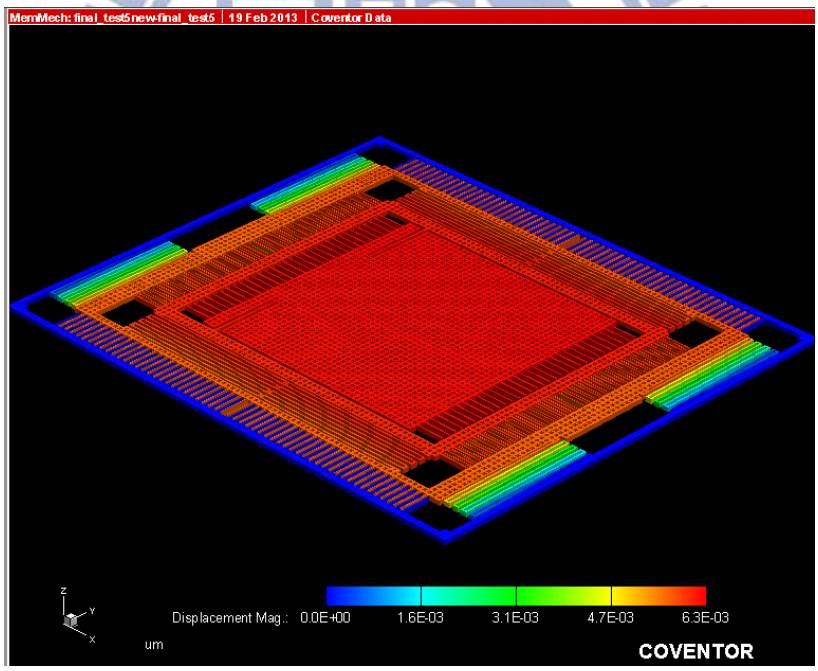
(b)

Figure 2.15: The stationary capacitances in one pair of comb finger (a) X, Y axis (b) Z axis

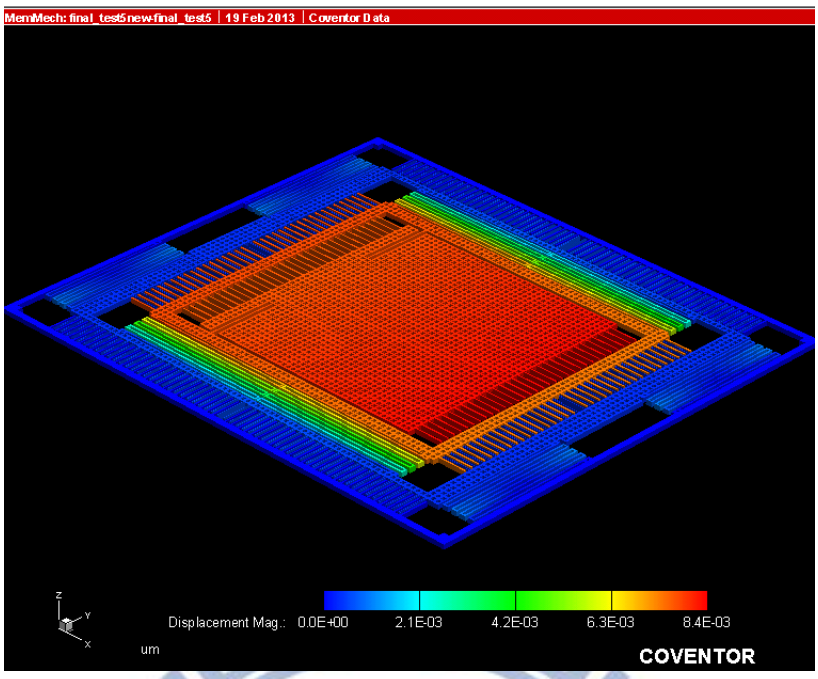
Table 2.4: The stationary capacitances in one pair of comb finger

The stationary capacitances in one pair of comb finger	Three-axis accelerometer
X, Y axis	2.15*E-03 pF
Z axis	1.33*E-03 pF

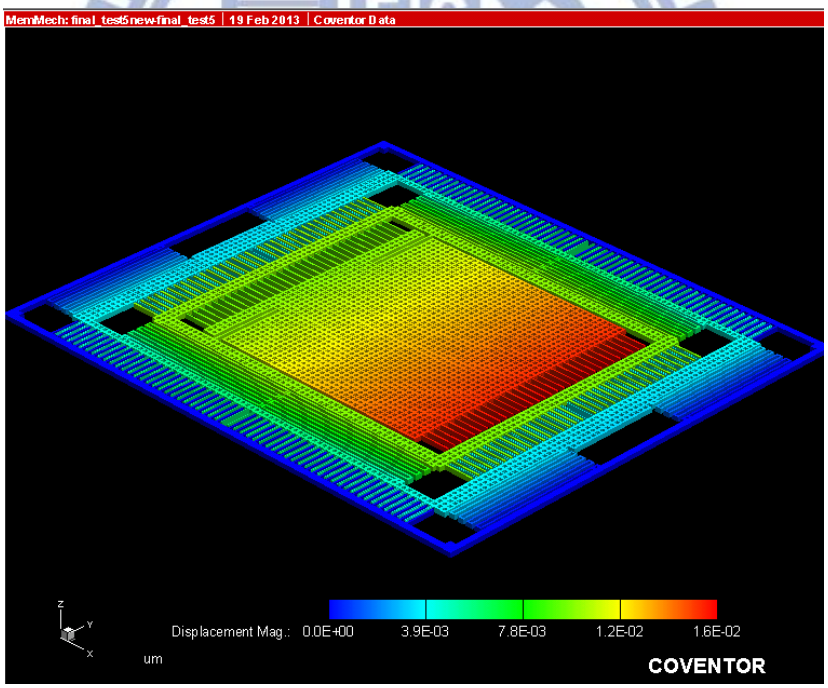
Then, by using CoventorWare mechanical analyzer, we can simulate the displacements of the X, Y, Z axis under 1g acceleration, respectively and resonant frequency. Figure 2.16 (a) (b) (c) illustrates the displacement of X, Y, Z axis under1g acceleration, respectively and Figure 2.17 shows the three-axis accelerometer resonant frequency.



(a)



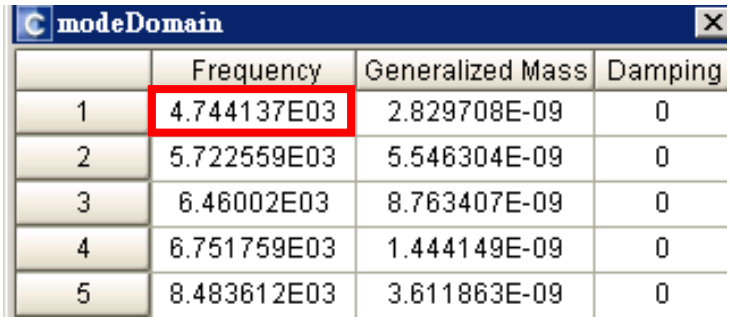
(b)



(c)

Figure 2.16: The displacement of three-axis under1g acceleration (a) X-axis (b) Y-axis

(c) Z-axis



modeDomain

	Frequency	Generalized Mass	Damping
1	4.744137E03	2.829708E-09	0
2	5.722559E03	5.546304E-09	0
3	6.46002E03	8.763407E-09	0
4	6.751759E03	1.444149E-09	0
5	8.483612E03	3.611863E-09	0

Figure 2.17: The three-axis accelerometer resonant frequency

By using Eq. (2.2) and Eq. (2.5), we can calculate the capacitance change of X, Y, Z axis, respectively. After getting one pair of capacitance change, multiplied by the number of comb fingers, we can get the total capacitance change of X, Y, Z axis, respectively under 1g acceleration. Table 2.5 shows the displacements and the capacitance changes of X, Y, Z axis.

Table 2.5 Displacements and the capacitance change of X, Y, Z axis

	Three-axis accelerometer	
Resonant frequency	4.744*E03	HZ
Displacement under 1g acceleration (X/Y/Z)	6/8/16	nm
Capacitance change (X/Y/Z)	0.37/0.4/0.33	fF

Last, by Eq. (2.8) and Eq. (2.9), we need the squeeze film and shear damping coefficient to calculate the Brownian noise. By using CoventorWare DampingMM analyzer, we can simulate the damping coefficient in squeeze film and shear condition. Figure 2.18 (a) (b) shows the simulation results of damping coefficient in squeeze film and shear in one pair of comb finger. According to the simulation results, we can see the damping coefficient of shear is smaller than squeeze film. Therefore, the Brownian noise is dominant in X,Y axis. The total damping coefficient can be

calculated by multiplied by the number of comb fingers.

Damping Force Coefficient

	Frequency (Hz)	Damping Coefficient (N/(m/s))
point 1	10	1.209961E-07
point 2	3.593814E01	1.209961E-07
point 3	1.29155E02	1.209961E-07
point 4	4.641589E02	1.209961E-07
point 5	1.668101E03	1.209961E-07
point 6	5.994843E03	1.209961E-07
point 7	2.154435E04	1.209961E-07
point 8	7.742637E04	1.209954E-07
point 9	2.782559E05	1.209869E-07
point 10	1.0E06	1.208767E-07

(a)

Damping Force Coefficient

	Frequency (Hz)	Damping Coefficient (N/(m/s))
point 1	10	5.922166E-09
point 2	3.593814E01	5.922166E-09
point 3	1.29155E02	5.922166E-09
point 4	4.641589E02	5.922167E-09
point 5	1.668101E03	5.92218E-09
point 6	5.994843E03	5.922352E-09
point 7	2.154435E04	5.924566E-09
point 8	7.742637E04	5.953109E-09
point 9	2.782559E05	6.311447E-09
point 10	1.0E06	9.713422E-09

(b)

Figure 2.18: Damping coefficient by DampingMM analysis (a) squeeze film (b) shear

After getting the damping coefficient, we can get the mass of the three-axis accelerometer simulated in CoventorWare. Then we can calculate the Brownian noise to be 5.21μg/√Hz.

Chapter 3 Capacitance to Voltage Circuit Design

3.1 System Architecture

The block diagram of the system architecture is shown in Figure 3.1. The first stage is a capacitance to voltage convertor (CVC) combing with correlated double sampling (CDS) [6-7] to reduce the interference from amplifier offset, flicker noise, charge injection, and kT/C noise. In addition, the EN signal can decide which sensors to be read and a signal generator generating three non-overlap control signals to read three-axis signals by time division [13-14]. The second stage also uses CDS technique to amplify signals from the first stage and suppress non-ideal effects. The third stage is an integrator [15], and the gain is inversely proportional to integration capacitance. Therefore, adjusting integration capacitance can make two sensors with similar output amplitudes. Furthermore, the control signals ON1~ON4 can adjust integration capacitance size to have different gains. The fourth stage is S&H. It can separate the mixed signal from the integrator by using four different control signals generated in the first stage.

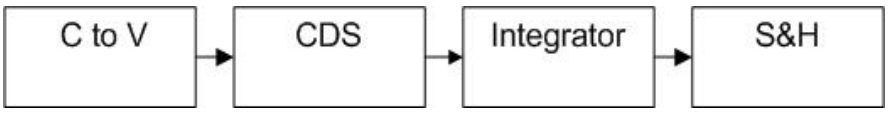


Figure 3.1: Block diagram of the capacitive sensor readout circuit

The universal readout circuit schematic and the system specification are illustrated in Figure 3.2 and Table 3.1. As discussed before, the CDS structure “Narrowband

Gain Compensated SC Amplifier" is chosen and used in the first and second readout circuit stage. Then, this CDS structure will be discussed in the next section.

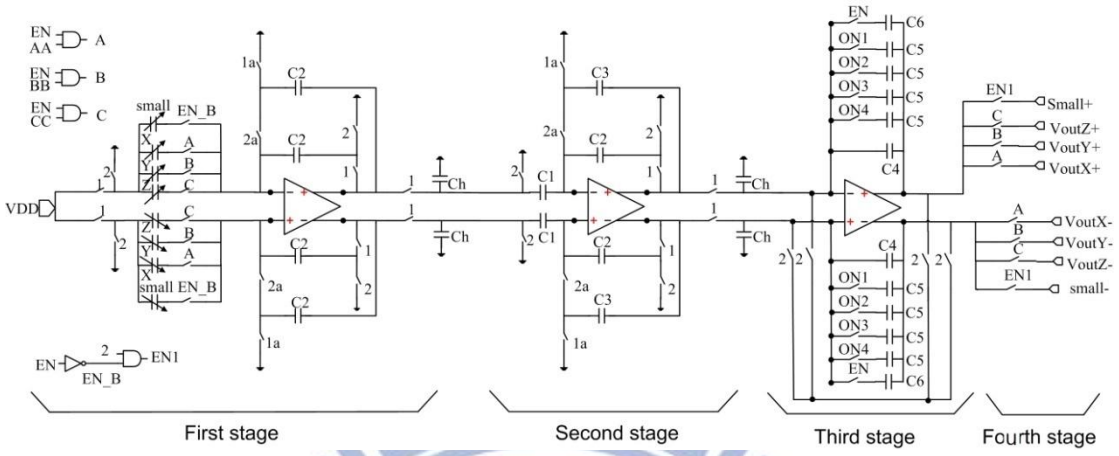


Figure 3.2: Universal readout circuit schematic

Table 3.1: System specification

Input sensing range	±4g (8g)
Circuit voltage	0V to 1.8V
Bandwidth	100Hz
Sensitivity	100mV/g
Noise	65.4nV/√Hz
Power	14.16μW
Chip size	2.79 mm^2

3.2 Narrowband Gain-Compensated SC Amplifier

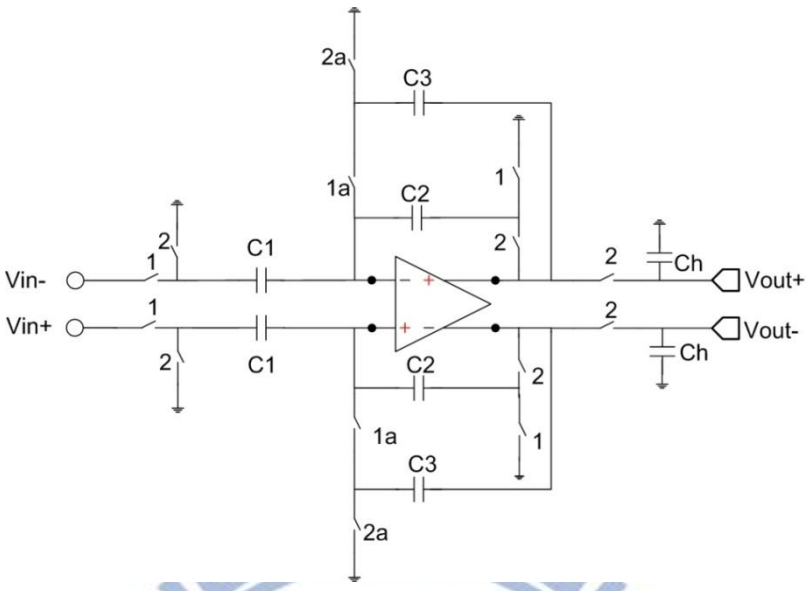


Figure 3.3: The schematic of the narrowband gain-compensated SC amplifier

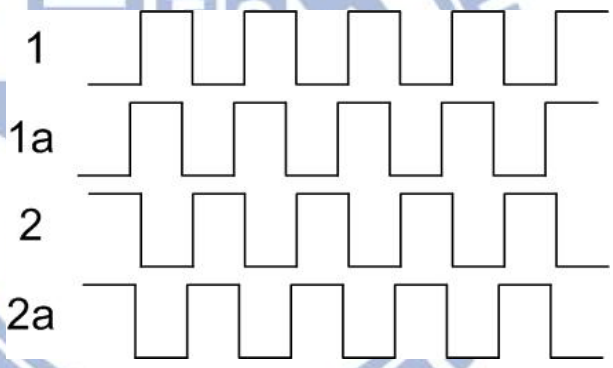


Figure 3.4: Timing diagram of the clock signals in Figure 3.3

Figure 3.3 shows the schematic of narrowband gain-compensated SC amplifier [3] [16-17]. This circuit architecture is used in the first and second stage readout circuit design. There are four clock signals in Figure 3.3 and the timing diagram of the clock signals is illustrated in Figure 3.4. The clock signals 1 and 2 are two non-overlapping phases, and the clock signal 1a is slightly sooner than clock signal 1 and clock signal 2a is slightly sooner than clock signal 2. Therefore, switches which are controlled by

clock 1a and 2a connected to grounds are disconnected sooner than other switches to suppress nonlinearities causing by channel charge injection. There are lots of switches in Figure 3.3, but only switches connected to op-amp input need to take into consideration. For clarification, the half circuit is used to illustrate why channel charge injection can be ignored. Figure 3.5 shows when switch S1 turns off, it will inject a charge Δ q1 in C2, and causes an error voltage $\frac{\Delta q1}{C2}$ (because node X is virtue ground, the charge Δ q1 will inject to C2). However, this error voltage is independent of input, because node X is virtue ground. By using channel charge equation,

$$Q_{ch} = WLC_{OX}(V_G - V_S - V_{TH}) \tag{3.1}$$

we can calculate that $\Delta q_1 = WLC_{OX}(V_{clk} - V_x - V_{TH})$ and it is a fixed value because V_x is independent of V_{in}. The fixed value Δq_1 means that it will cause a DC offset at output, but this can be canceled easily by using differential operation. The charge injection cause by turning off switch S2 shows in Figure 3.6. The charge Δ q2 will change the voltage at node P about $\frac{\Delta q2}{C1}$, and the output voltage will change $\frac{-\Delta q2}{C2}$. However, when S3 turns on, Vp voltage will change to ground, the total voltage change of Vp is 0-Vin = -Vin, and it makes total output voltage change to be $V_{in}\frac{C1}{C2}$. The voltage change over time at node P and Vout are shown in Figure 3.7. In other words, intermediate voltage change does not affect the final output

voltage. The switch S3 is connected to ground, so its channel charge injection can also be neglected.

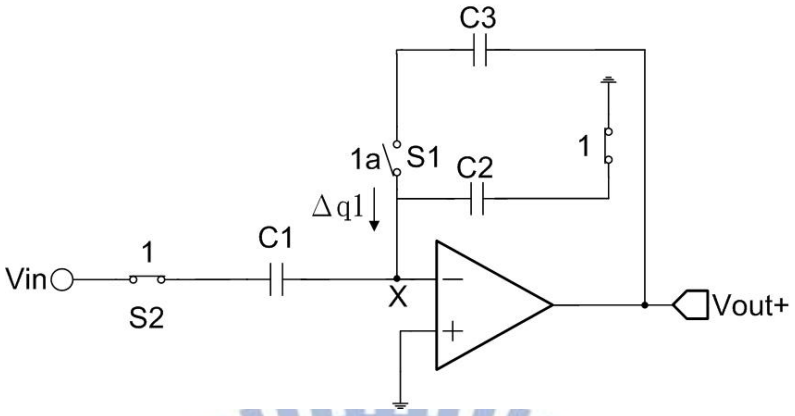


Figure 3.5: Charge injection when switch S1 is off

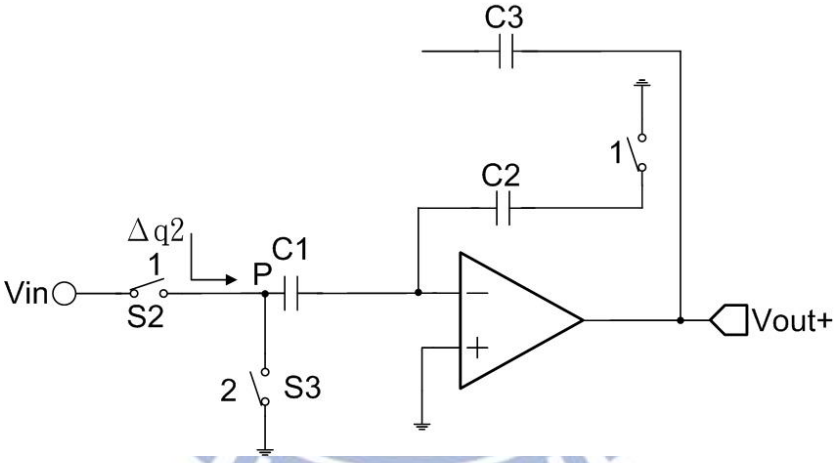


Figure 3.6: Charge injection when switch S2 is off

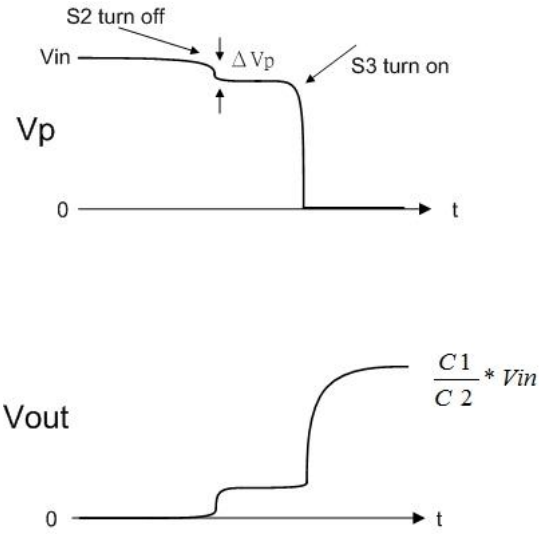


Figure 3.7: Vp and Vout voltage change over time

After that, we can see the parasitic capacitance will not affect the output voltage. Figure 3.8 shows that there are six parasitic capacitances, Cp1~Cp6. Parasitic capacitances Cp2, Cp3, Cp5 have little effect since they are connected to virtual ground, and parasitic capacitances Cp4, Cp6 also have little effect since they are driven by output. The parasitic capacitance Cp1 is continuously being charged to Vin and discharged to ground. When clock phase 1 is high, the parasitic capacitance Cp1 is charged to Vin, and does not affect capacitance C1 charge. And when clock phase 2 is high, Cp1 is discharged through the clock phase 2 switch attached to its node and does not affect the charge accumulate on capacitance C2. Thus, although the parasitic capacitance may slow down settling time behavior, they do not affect the final output voltage.

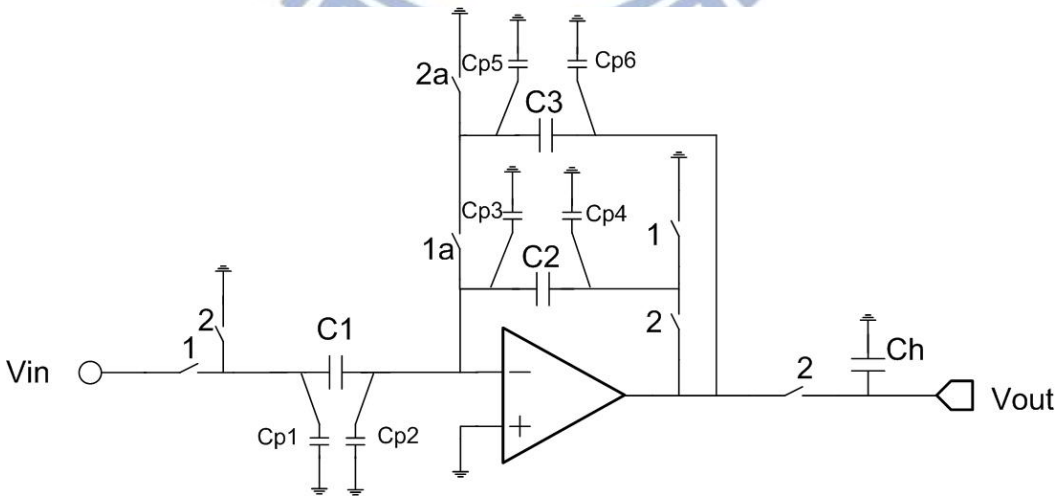


Figure 3.8: The parasitic capacitance effects

In Figure 3.9, the op-amp dc offset voltage effect and low frequency noise source like

flicker noise is considered. The capacitance C_1 and C_2 play a role in the signal charge redistribution, and the capacitance C_3 works as a S&H branch which hold the output voltage generating in clock phase 2. By using charge conservation mechanism in two different clock phases, we can derive the output voltage. When clock phase 1 → 1 (Figure 3.10), C1 samples the difference between the input Vin and op-amp negative input, has a charge [Vin-V(n-1/2)]*C1 on C1, and C2 discharges to V(n-1/2)*C2. Then when clock phase 2 → 1 (Figure 3.11), C1 discharges into C2, and C1 has a charge [–V(n)*C1] and C2 has a charge [Vout(n)-V(n)]*C2 . The two clock phases have the same charge, and we can write

$$\left[\mathrm{Vin} - \mathrm{V}\left(\mathrm{n} - \frac{1}{2}\right)\right]\mathrm{C}_1 + \mathrm{V}\left(\mathrm{n} - \frac{1}{2}\right)C_2 = \left[-\mathrm{V(n)C}_1\right] + [\mathrm{Vout(n)} - \mathrm{V(n)}]C_2 \qquad (3.2)$$

and we can derive the output voltage is

$$\mathrm{Vout}(n) = \frac{\mathrm{C}_1}{C_2}\mathrm{Vin} + \mathrm{V_e(n)} \qquad (3.3)$$

$$V_e(n) = \left(1 + \frac{\mathrm{C}_1}{C_2}\right)[\mathrm{V(n)} - \mathrm{V}(\mathrm{n} - \frac{1}{2})] \qquad (3.4)$$

where $\mathrm{V_e(n)}$ is an error voltage and V(n) is op-amp offset voltage plusing low frequency noise source like flicker noise. If the input signal bandwidth is much smaller then $\frac{\mathrm{f_{CLK}}}{2}$, in other words, if the input signal is significantly oversampled, then $\mathrm{V_{out}}$ does not vary much from one clock phase to the next clock phase. Therefore, for a finite op-amp gain $\mathrm{A_0}$, the signal voltage $-\frac{\mathrm{V_{out}}}{\mathrm{A_0}}$ at virtual ground is a slowly changing signal which can be almost cancelled by the CDS switching C_1 and C_2 in

two clock phases showing in Eq. (3.4). According to ref [17-19], the transfer function in Z transform is expressed as

$$H(Z) = \frac{V_{out}(Z)}{V_{in}(Z)} = \frac{C_1}{C_2}\frac{az^{-\frac{1}{2}}}{1-bz^{-1}} \tag{3.5}$$

where *a* and *b* are respectively given by

$$a = \frac{1}{1+\frac{C_1+C_2}{C_2A_0}} * \left[1 - \frac{C_1+C_2}{A_0C_3+C_1+C_2+C_3}\right] \tag{3.6}$$

$$b = \frac{\frac{C_1+C_2}{A_0}*\left[C_2+C_3+\frac{C_1C_2}{A_0}\right]}{\left[C_2+\frac{C_1+C_2}{A_0}\right]*\left[C_3+\frac{C_1+C_2+C_3}{A_0}\right]} \tag{3.7}$$

According to Eq. (3.5), this circuit is a non-inverting and integrating SC amplifier with a delay of one half clock cycle. In addition, the op-amp dc offset voltage (V_{off}) has no effect on the transfer function.

In low frequency applications, z is approximately equal to one, and the Eq. (3.5) can be simplified as

$$H(1) = \frac{V_{out}}{V_{in}} = \frac{C_1}{C_2}\frac{a}{1-b} = \frac{C_1}{C_2}\left[1 - \frac{C_1+C_2}{C_2A_0^2}\right] \tag{3.8}$$

The second term in parentheses in Eq. (3.8) is the gain error caused by the finite op-amp gain. However, the magnitude of the gain error is inversely proportional to the square of A_0 rather than A_0. Therefore, the SC amplifier's dependence on op-amp gain is majorly reduced. Circuits with this property are called gain-enhanced or gain-squaring stages.

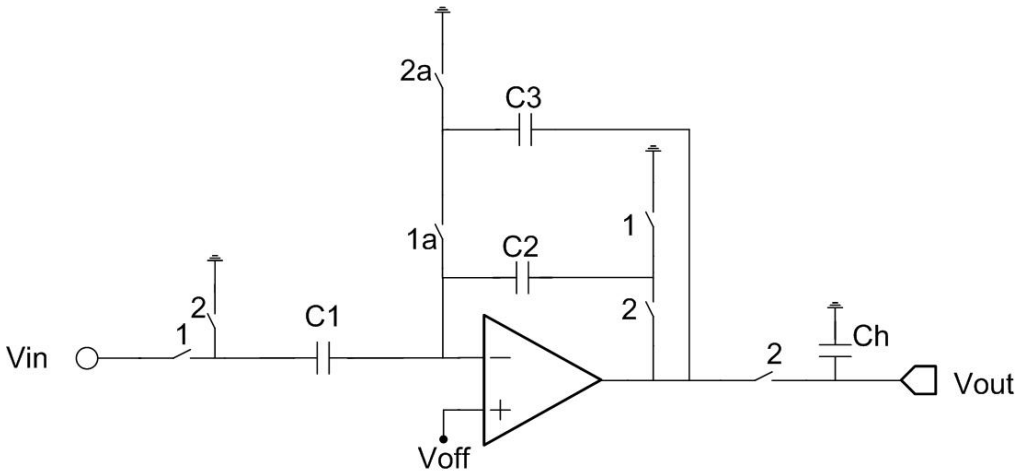


Figure 3.9: Half circuit of narrowband gain-compensated SC amplifier with offset

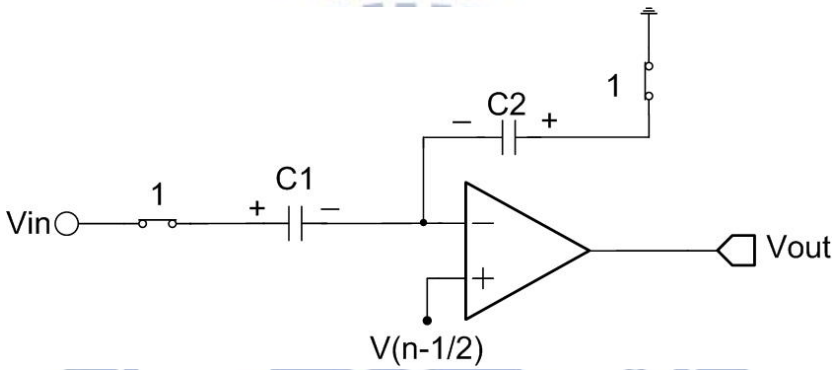


Figure 3.10: When clock phase 1 is high

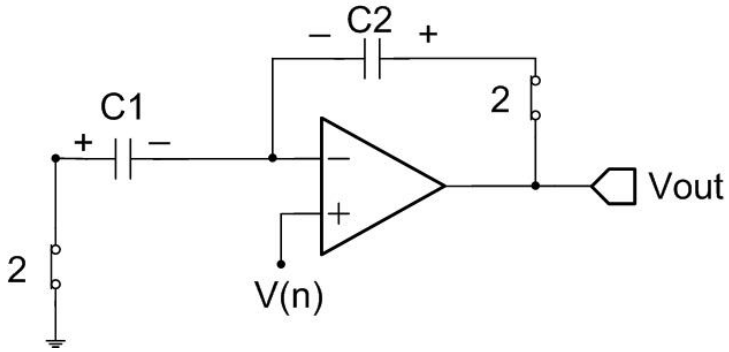


Figure 3.11: When clock phase 2 is high

Figure 3.12 illustrates the clock phases and waveforms of the output. When clock phase 1 → 1, and the sample phase begins, there is a small voltage step ΔV, where is

$$\Delta V = V_{off} - \frac{V_{out}}{A_0} - \frac{C_1}{C_3}\Delta V_{in} \tag{3.9}$$

at the output, where ΔV_{in} is the change of V_{in} during clock phase 2 is high interval. This voltage step happens because when clock phase $2 \rightarrow 1$, C_3 is disconnected from ac ground to virtue ground. However, the charge on C_3 must be fixed, so there is a voltage step at output. The ΔV is normally in a order of a few millvolts, so the op-amp in this circuit schematic does not require a high slew rate or a fast settling time. Therefore, the low tail current of op-amp can be used to reduce power consumption. The simulation results of the narrowband gain-compensated SC amplifier are illustrated in Figure 3.13 (a) (b) (c) and Table 3.2 and the input signal amplitude is 100mV and frequency is 100Hz and the ratio of capacitance $\frac{C_1}{C_2}$ is 2.

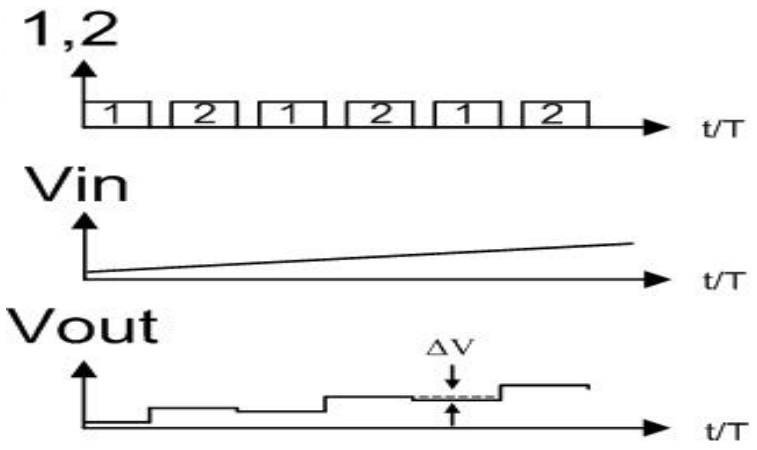


Figure 3.12: Clock phases and waveforms of output

(a)

(b)

(c)

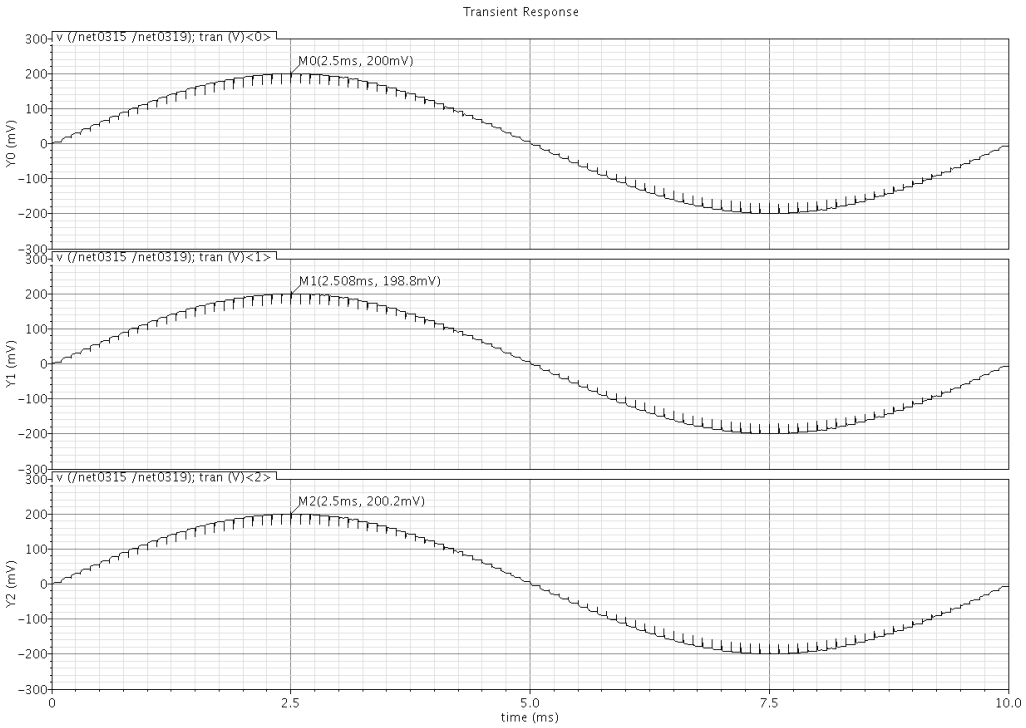


Figure 3.13: The narrowband gain-compensated SC amplifier output simulation results (a) TT (b) SS (c) FF corner

Table 3.2: The amplitude in three corners

	TT	FF	SS
Amplitude	200 mV	198.8 mV	200.2 mV

3.3 The capacitance to voltage convertor (CVC)

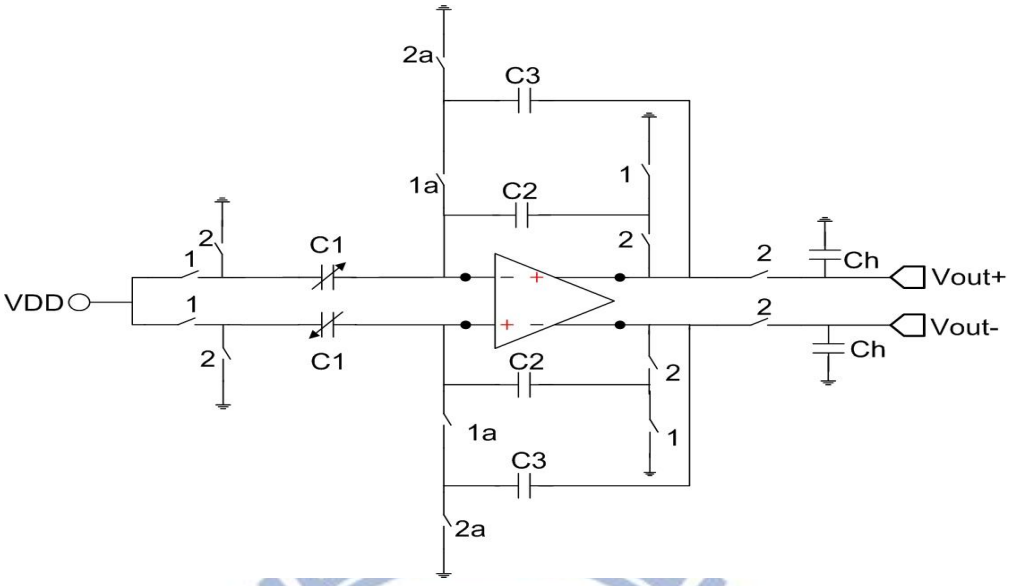


Figure 3.14: The schematic of the capacitance to voltage convertor

Figure 3.14 shows the schematic of the capacitance to voltage convertor (CVC) [6-7]. According to Eq. (3.4), we can derive the output voltage as

$$[(V_{out+}) - (V_{out-})] = D_{vout} = \frac{1}{2} * \left[\frac{VDD*(C+\Delta C) - VDD*(C-\Delta C)}{C_2}\right] \quad (3.10)$$

$$= 2 * \frac{\Delta C}{C_2} * VDD \quad (3.11)$$

where D_{vout} is the differential output voltage and C is the stationary capacitances of sensors and ΔC is the capacitance change of sensors. From Eq. (3.11), we can derive the sensitivity of the CVC stage as

$$\frac{D_{vout}}{\Delta C} = 2 * \frac{VDD}{C_2} \quad (3.12)$$

In this design, the VDD is 1.8 volts and the C_2 is 100fF. However, the op-amp DC biasing voltage is 600 millvolts instead of 0 volt. By calculation, the first stage sensitivity $\frac{D_{vout}}{\Delta C}$ is 9mV/fF. In other words, if the sensor has 1 femtofarad

capacitance change, it will generate 9 millvolts at the output. The simulation results of the CVC are shown in Figure 3.15 and Table 3.3 and the capacitance change is set to 0.35fF so the calculated output voltage of the CVC is 3.15 millvolts.

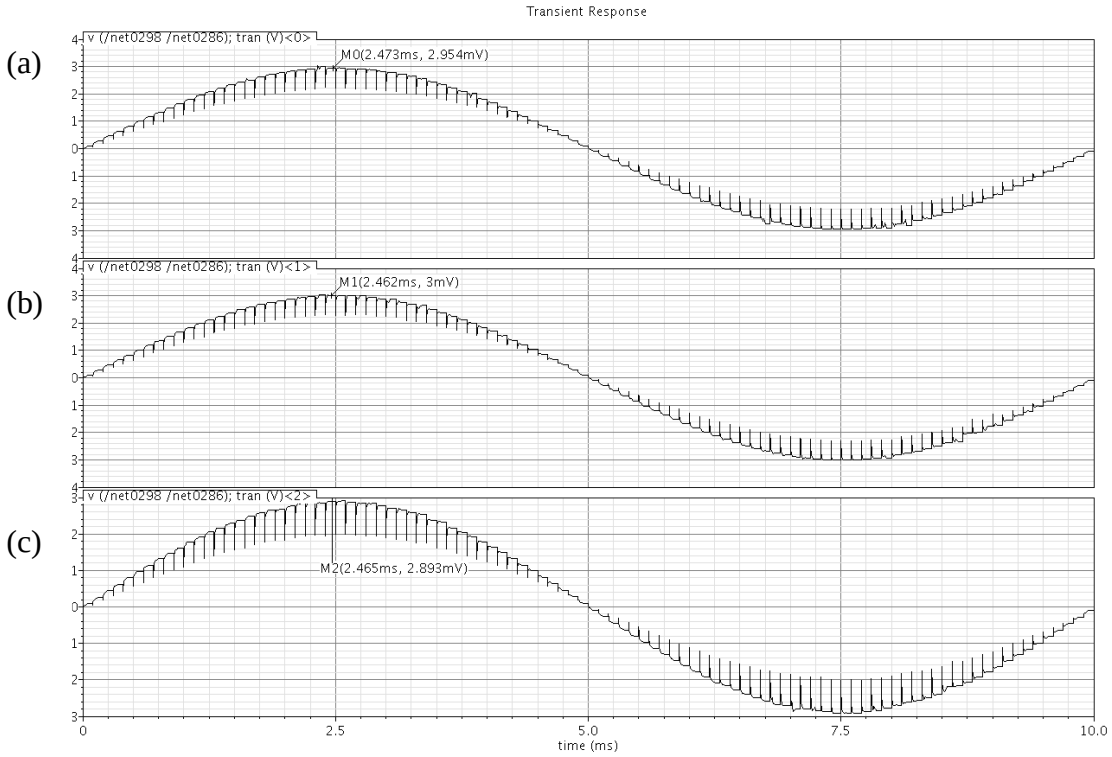


Figure 3.15: The CVC output simulation results (a) TT (b) FF (c) SS corner

Table 3.3: The CVC output amplitude

	TT	FF	SS
Amplitude	2.95 mV	3 mV	2.89 mV

3.4 Amplifier

The amplifier schematic is shown in Figure 3.16. It is designed as a single stage for

low power consumption. The small signal voltage gain can be expressed as.

$$A_v \approx \mathrm{g_{m3}} * (\mathrm{r_{01}} || \mathrm{r_{03}}) \tag{3.13}$$

The amplifier has a pole and can be written as.

$$\omega_p = \frac{1}{\mathrm{R_{out}} * \mathrm{C_L}} \tag{3.14}$$

Because the differential operation is used, the amplifier need a output common mode feedback (CMFB) to define the output dc voltage. In this design, the PMOS (M3,M4) currents must equal to NMOS currents (M1,M2). Figure 3.17 shows that, if both currents are not match, there is a current difference $(\mathrm{I_P} - \mathrm{I_N})$ flowing into amplifier output resistance, generating a output voltage error $(\mathrm{I_P} - \mathrm{I_N})(\mathrm{R_P} || \mathrm{R_N})$. Because $\mathrm{R_P} || \mathrm{R_N}$ is a large resistance, the voltage error is high. The CMFB working principle can be illustrated as follow:

The drain currents in M7 and M8 are

$$I_{d7} = \frac{-I2}{2} - g_{m7} \frac{(\mathrm{Vout2} - \mathrm{VCM})}{2} \tag{3.15}$$

$$I_{d8} = \frac{-I3}{2} - g_{m8} \frac{(\mathrm{Vout1} - \mathrm{VCM})}{2} \tag{3.16}$$

These currents are summed in diode-connected M5 to give current

$$I_{d5} = -I_{d7} - I_{d7} = \mathrm{I2} + g_{m7}(\frac{\mathrm{Vout1} + \mathrm{Vout2}}{2} - \mathrm{VCM}) \tag{3.17}$$

$$= \mathrm{I2} + g_{m7}(V_{OC} - VCM) \tag{3.18}$$

Since I2 = I3, and g_{m7} = g_{m8}. Eq. (3.18) shows that the current through M5 includes a dc term I2 plus a term that is proportional to $V_{OC} - VCM$. The current I_{d5}

is mirrored by M1 and M2 to generate the tail current in the amplifier, which controls the output CM voltage. For example, if V_{OC} > VCM, the current I_{d5} will increase, and the currents I_{d1} and I_{d2} also increase, making V_{OC} drop and vise versa. The simulation results of the amplifier ac response (Figure 3.18, Figure 3.19 and Table 3.4), the input common mode range (Figure 3.20), the CMFB (Figure 3.21 and Table 3.5) and the input referred noise (Figure 3.22 and Table 3.6) are illustrated as below.

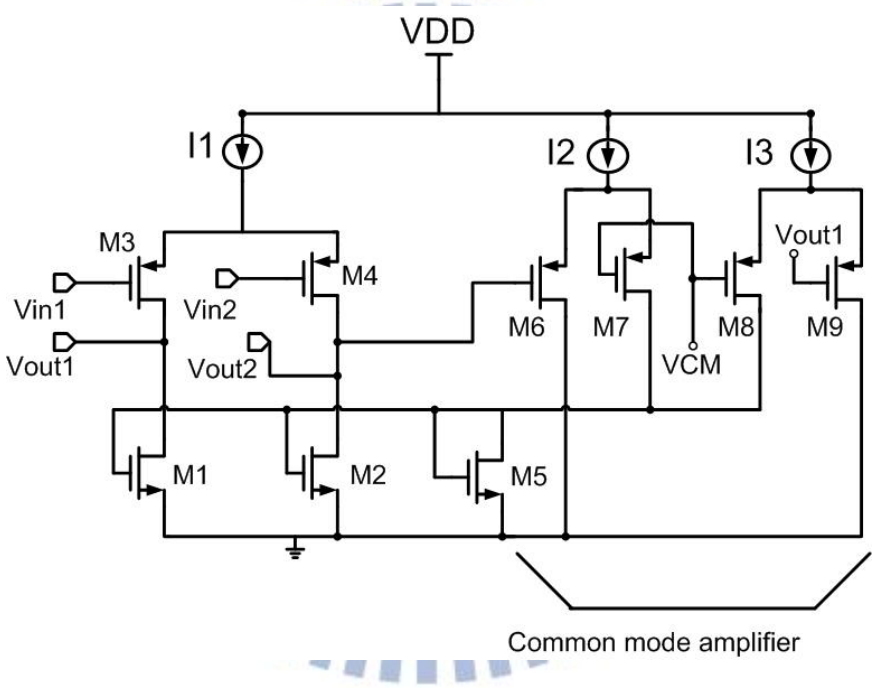


Figure 3.16: Single stage amplifier schematic

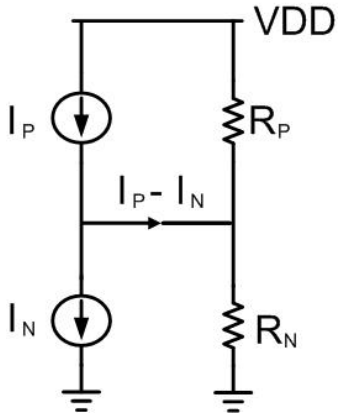


Figure 3.17: Amplifier simplified model

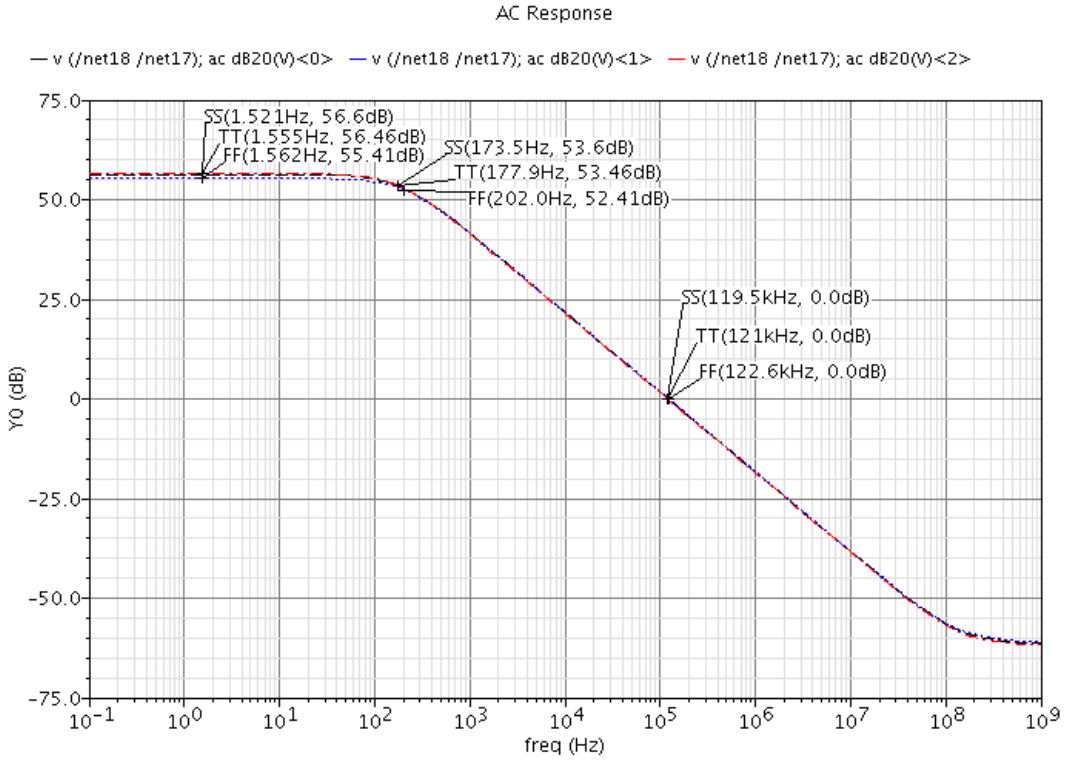


Figure 3.18: DC gain, 3dB frequency and unit frequency simulation

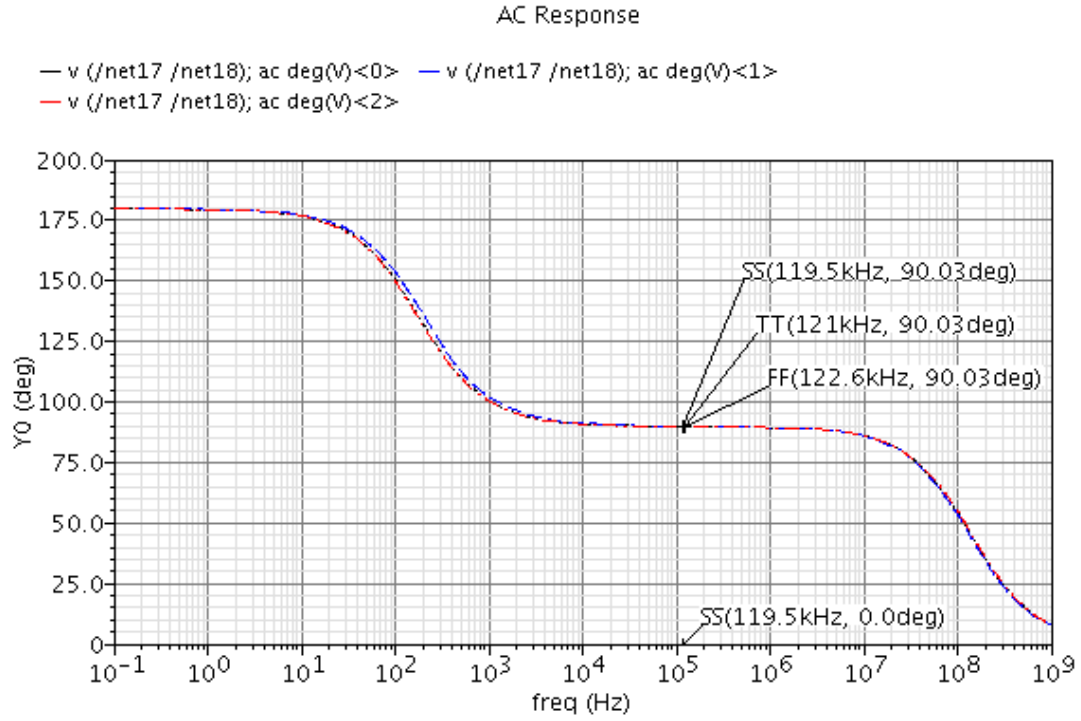


Figure 3.19: Phase margin simulation

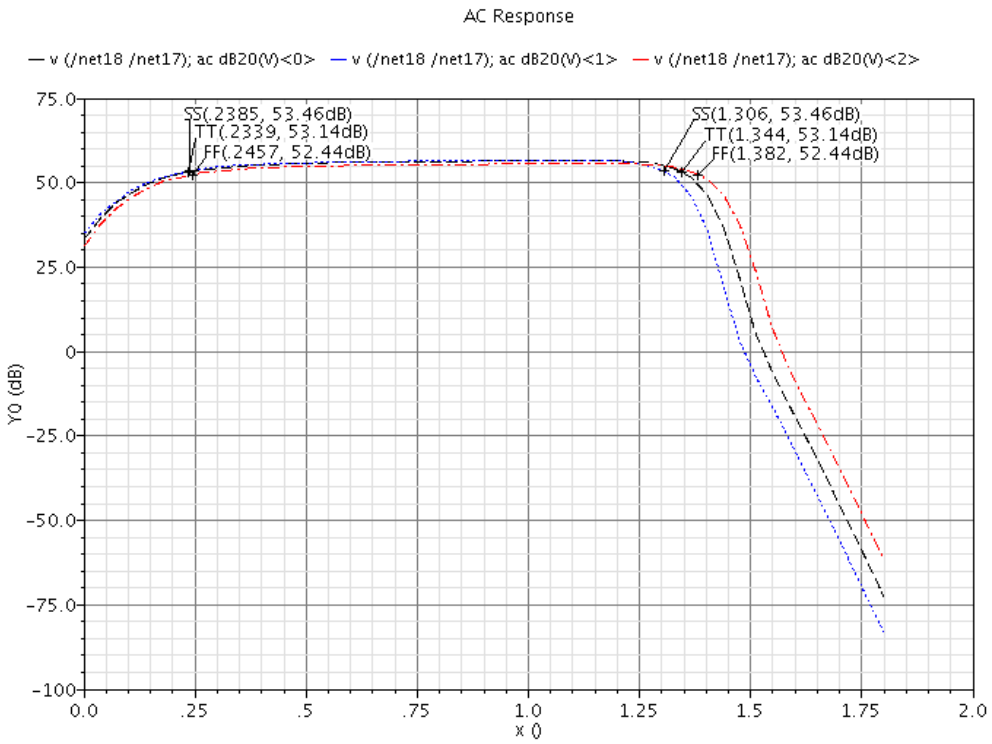


Figure 3.20: Input common mode range simulation

Table 3.4: Amplifier simulation results

	TT	FF	SS
DC gain	56.46dB	55.41dB	56.6dB
3dB frequency	177.9Hz	202Hz	173.5Hz
Unity frequency (With 1pF)	121kHz	122.6kHz	119.5kHz
Phase Margin	90.03Deg	90.03Deg	90.03Deg
ICMR	0.23V~1.34V	0.25V~1.38V	0.24V~1.3V
power	0.718μW	0.72μW	0.717μW

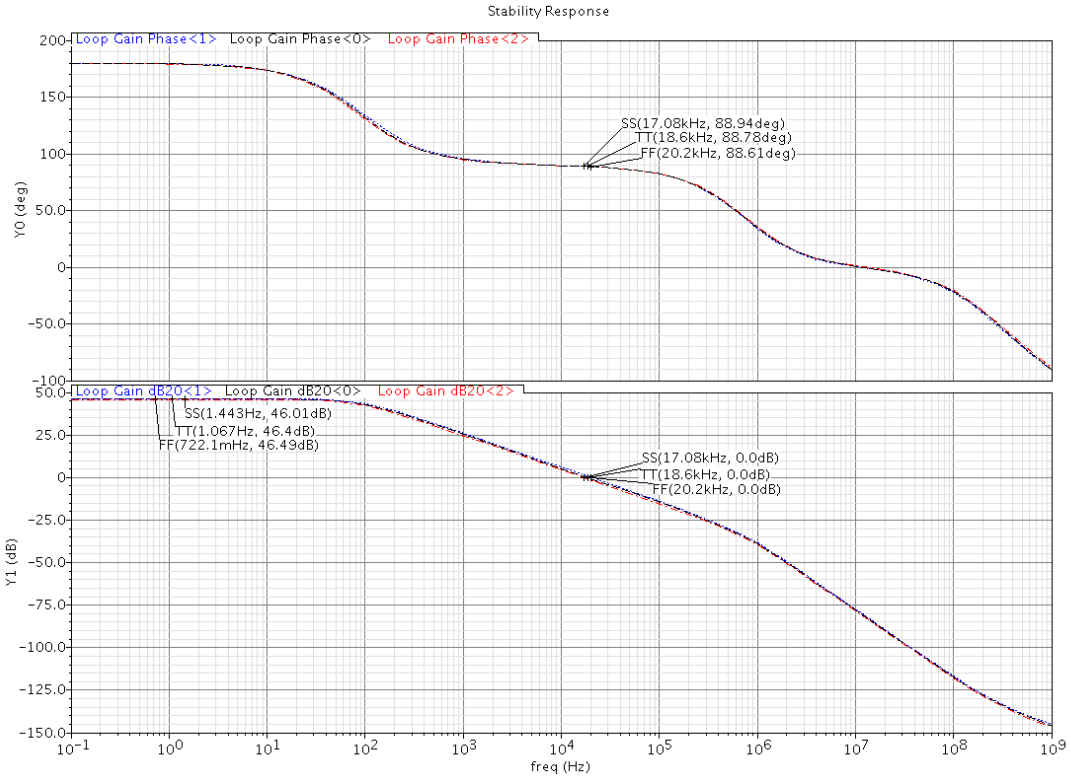


Figure 3.21: Common mode feedback loop simulation

Table 3.5: CMFB simulation results

	TT	FF	SS
Loop gain	46.4dB	46.49dB	46.01dB
Unity frequency	18.6kHz	20.2kHz	17.08kHz
Phase margin	88.78Deg	88.61Deg	88.94Dreg

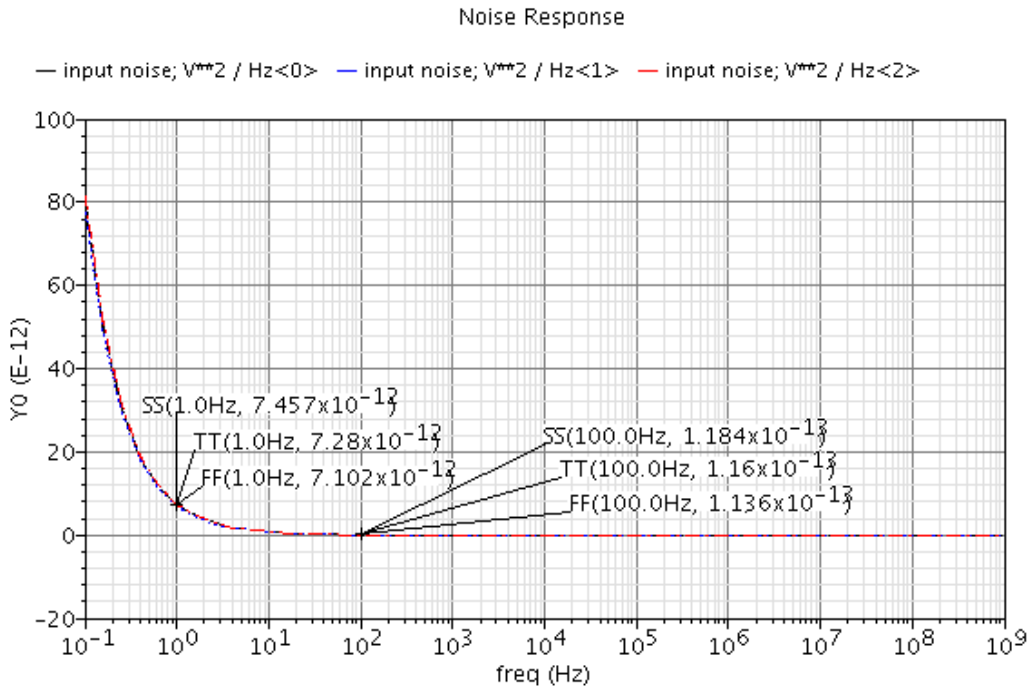


Figure 3.22 Input referred noise simulation

Table 3.6: Input referred noise simulation results

	TT	FF	SS
Input referred noise	615 nV/√Hz	608 nV/√Hz	622 nV/√Hz

3.5 Bias circuit

Figure 3.23 illustrates the schematic of bias circuit [20]. In this design, the self-biasing technique is used to reduce the power supply sensitivity and the bias circuit composes three parts: current mirror, current source and start-up circuit. The bias circuit working principle is that current source generates a current I_{OUT} and current mirror forces I_{IN} equal to I_{OUT}. Therefore, this feedback loop can generate a

stable current, and this current can be used to bias amplifier. However, in the plot of Figure 3.24, two intersections are shown. Point A is the desired operating point, and the point B is an undesired operating point because $I_{IN} = I_{OUT} = 0$. The zero-current state can be avoided by using a start-up circuit to ensure that some current flows in the transistors in the reference. In Figure 3.23, transistors M4, M5 form a current mirror, and the relation between I_{IN} and I_{OUT} can be express as.

$$I_{IN} = \frac{(W/L)_4}{(W/L)_5} I_{OUT} \tag{3.19}$$

Transistors M1, M2 and resistance R form a current source and the current I_{OUT} can be written as

$$I_{OUT} = \frac{V_{TH} + \sqrt{\frac{2I_{IN}}{k'(W/L)_1}}}{R} \tag{3.20}$$

From Eq. (3.20), the I_{OUT} is proportional to threshold voltage, so we call this bias circuit to be V_{TH} reference and we can see that I_{OUT} is independent of VDD. Transistors M6, M7, M8 form the start-up circuit. If the circuit is in the undesired zero-current state, the gate-source voltage of M1 would be less than a threshold voltage. As a result, M6 is off and M7 operates in the triode region, pulling the gate-source voltage of M8 up to VDD. Therefore, M8 is on and pulls down the gates voltage of M4 and M5. This action causes current to flow in M4 and M5, avoiding the zero-current state.

The dependence on temperature is another important aspect of the performance of

biasing circuit. The fractional temperature coefficient TC_F can be expressed as.

$$TC_F = \frac{1}{I_{OUT}} \frac{\partial I_{OUT}}{\partial T} \tag{3.21}$$

We can differentiate Eq. (3.20), and substitute into Eq. (3.21) gives

$$TC_F \approx \frac{1}{V_{TH}} \frac{\partial V_{TH}}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T} \tag{3.22}$$

where $\frac{\partial V_{TH}}{\partial T} \approx -2mV/_{\circ C}$ and Table 3.7 shows the bias current varying with temperature. Figure 3.25 illustrates the start-up simulation. The VDD has a rising time, and we can see that the start-up circuit will first turn on, and then turn off. After the start-up circuit turns off, the bias circuit generates a stable gate voltage for M3, and M3 can generate a stable bias current.

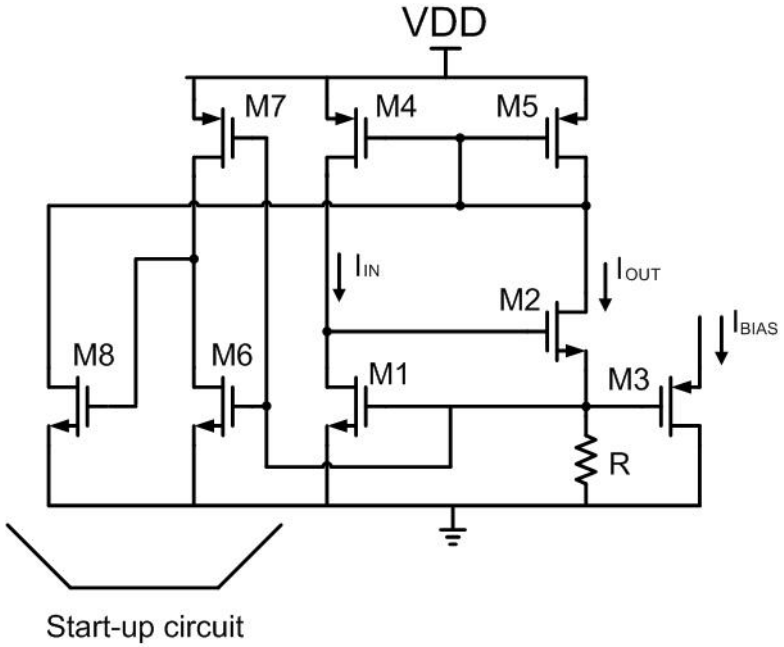


Figure 3.23: Self-biasing V_{TH} reference with start-up circuit

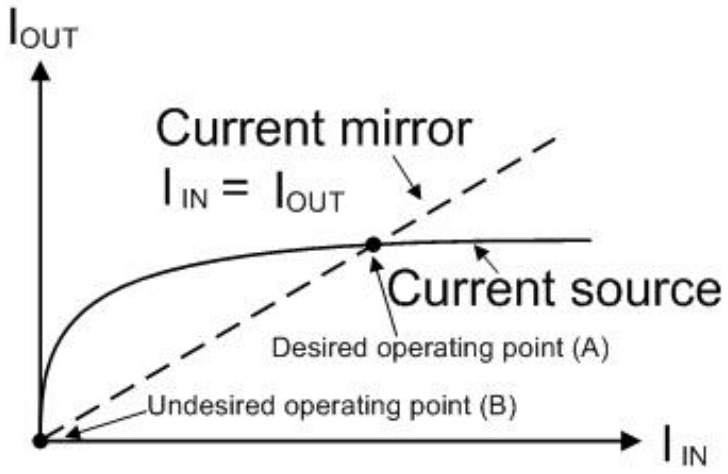


Figure 3.24: Two operating points

Table 3.7: Bias current varying with temperature

Temperature	I_{BIAS} (TT)	I_{BIAS} (FF)	I_{BIAS} (SS)
20℃	98.1nA	99.3 nA	97.8 nA
40℃	96.8 nA	97.5 nA	97.1 nA
60℃	95.4 nA	95.8nA	96.1 nA
80℃	94 nA	94 nA	95.1 nA

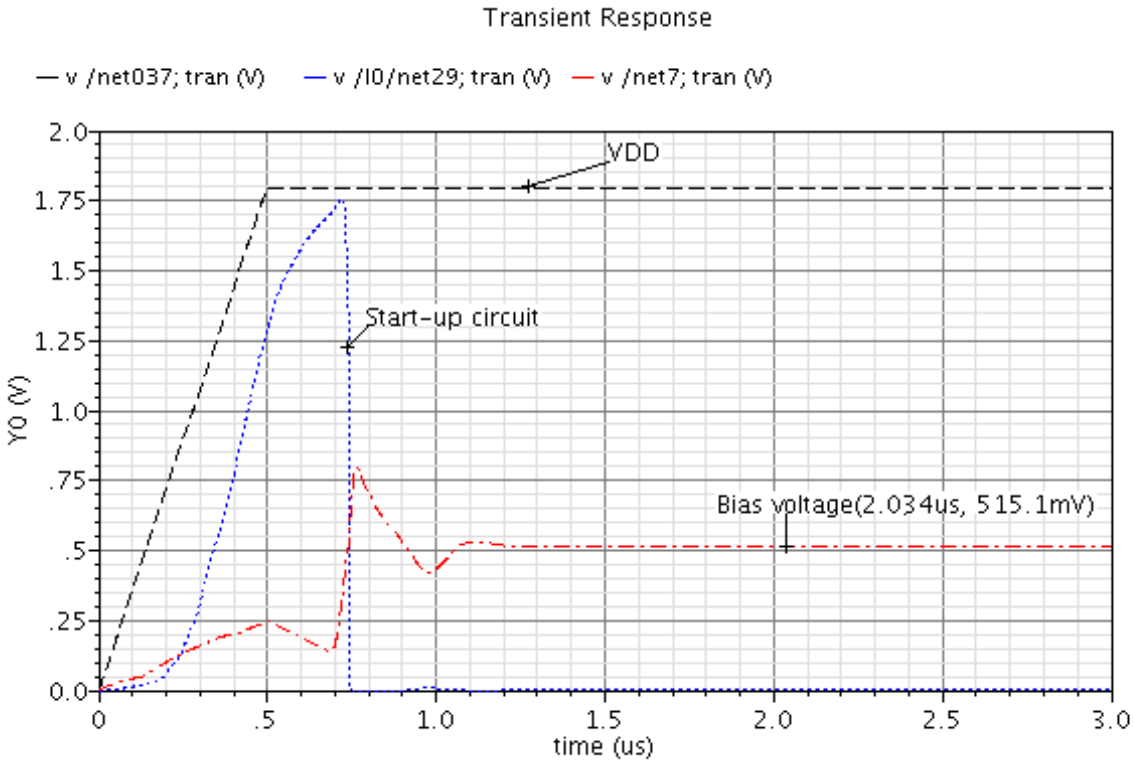


Figure 3.25: Start-up simulation

3.6 Clock Generator

The first stage CVC and the second stage CDS needs two phases clocks 1a, 2a and two phases clocks with delay 1, 2. Figure 3.26 shows the two phases non-overlapping clock generator, and the delay can be decided by the size of the two inverters.

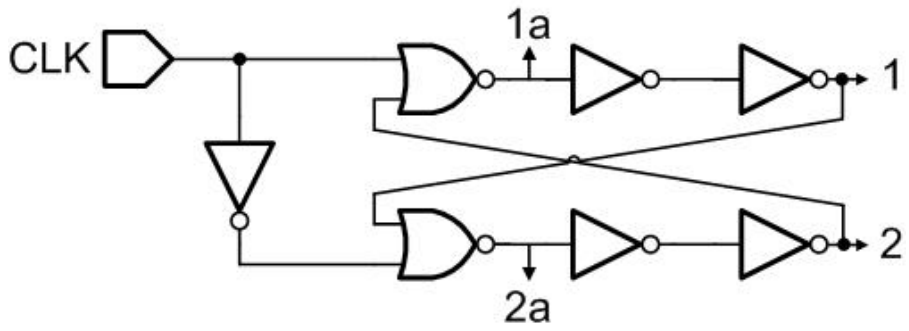


Figure 3.26: Two non-overlapping clock generator

3.7 Three phases control signals generator

In the first stage, the CVC needs three non-overlapping clock signals to read three axis accelerometer signals by time division. Figure 3.27 shows the signals generator generates three non-overlapping clocks AA, BB, CC and the three clocks to do the and operation with EN, generating control signals A, B, C. Figure 3.28 shows the simulation results.

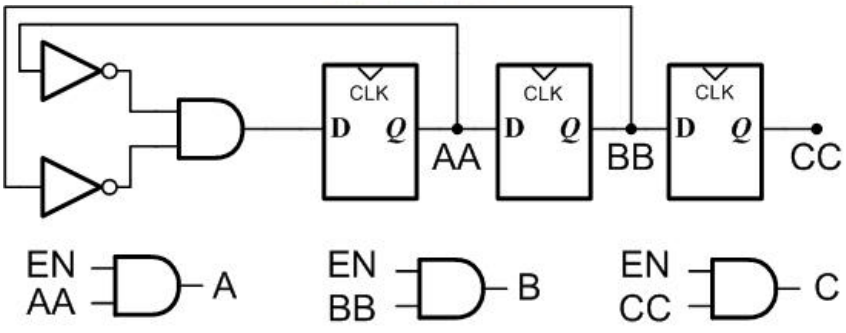


Figure 3.27: Control signals generator

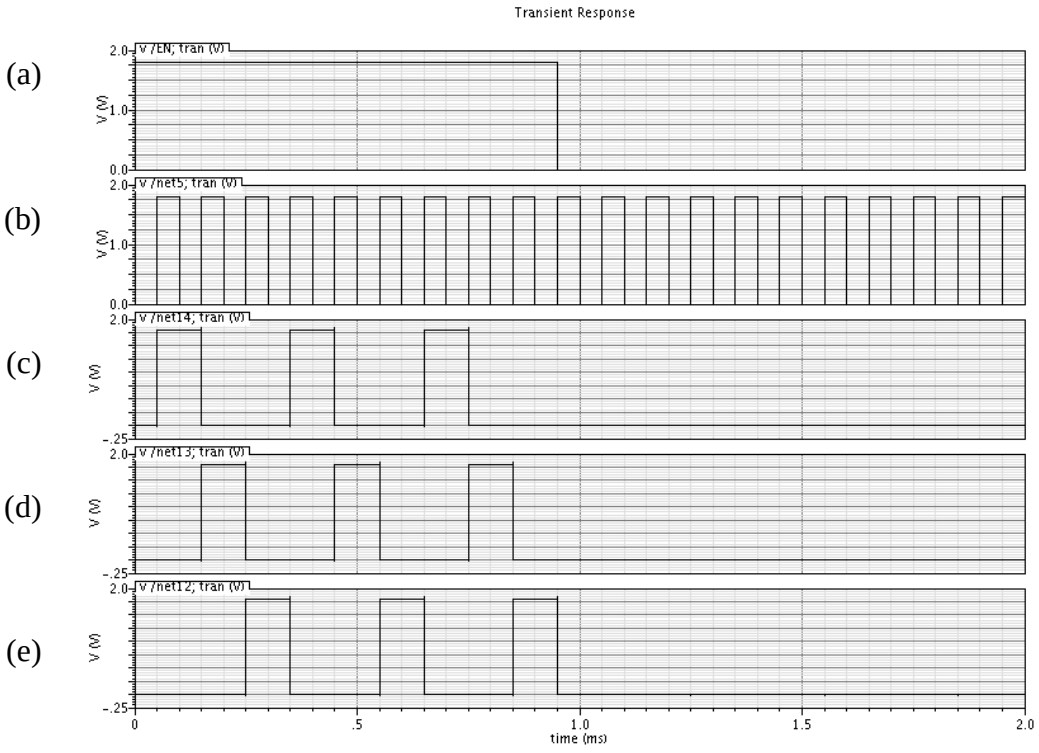


Figure 3.28: Control signals simulation results (a) EN (b) CLK (c) A (d) B (e) C

3.8 The First stage

The first stage schematic is illustrated in Figure 3.29 and is similar to CVC stage which is described before as shown in Figure 3.14. Instead of one pair capacitances, the four pairs capacitances contain a three-axis accelerometer (X, Y, Z) and additive sensor with smaller capacitance change (small). There are four control signals which are A, B, C, and EN_B. The three non-overlapping signals A, B, C are described before as shown in Figure 3.28 and EN_B is EN inversed. The control signal EN can decide which sensors to be read. When EN is high, the three non-overlapping signals will be generated, and the three-axis accelerometer will be read. Inversely, when EN is low, additive sensor with smaller capacitance change will be read. In this design, the three-axis accelerometer capacitance changes under 1g acceleration are simulated to be 0.37,0.4,0.33 femtofarad respectively. An additive sensor with smaller capacitance change under 1g acceleration of 15 attofarad is also designed in. The simulation results of the first stage are shown in Figure 3.30~3.33 and Table 3.8. In order to see the three-axis accelerometer signals more clearly, 1g, 2g, 4g acceleration are given for X, Y, Z axis respectively, and 1g acceleration is given for additive sensor.

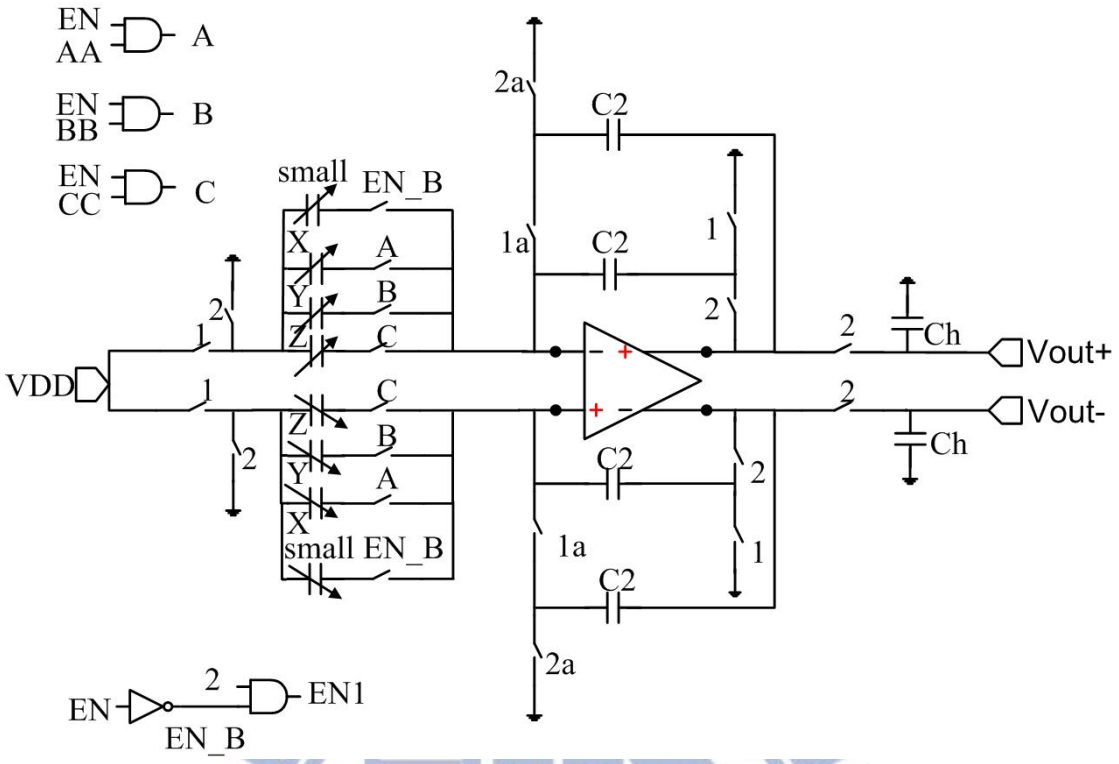


Figure 3.29: The schematic of the first stage

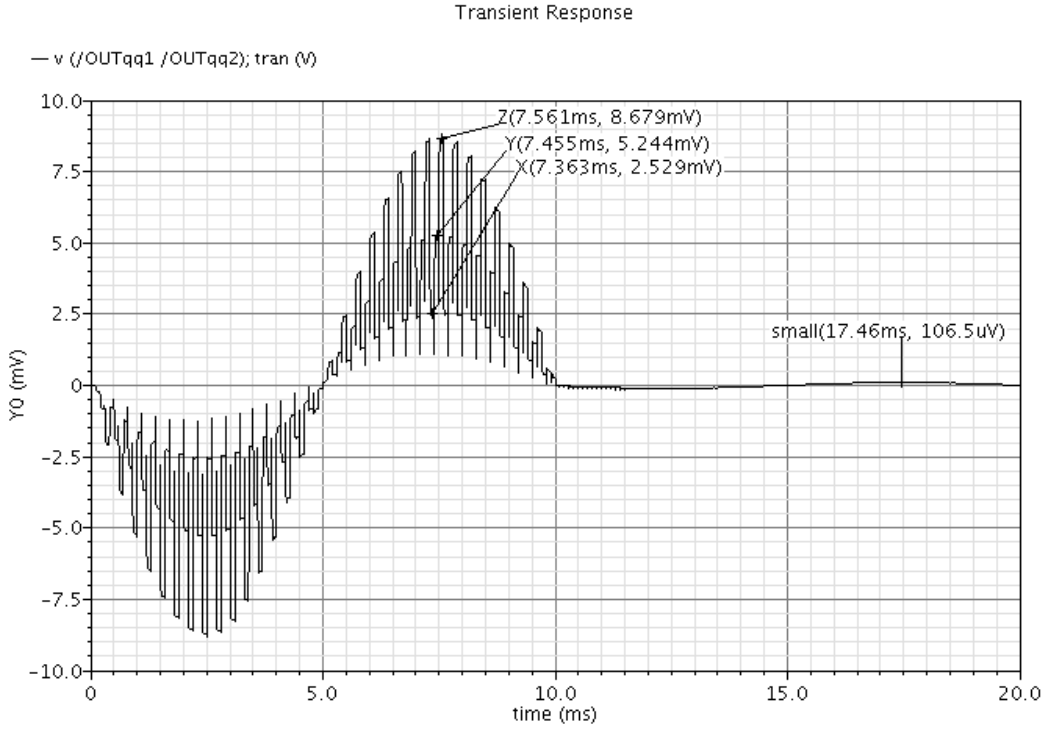


Figure 3.30: The first stage output simulation results in TT corner

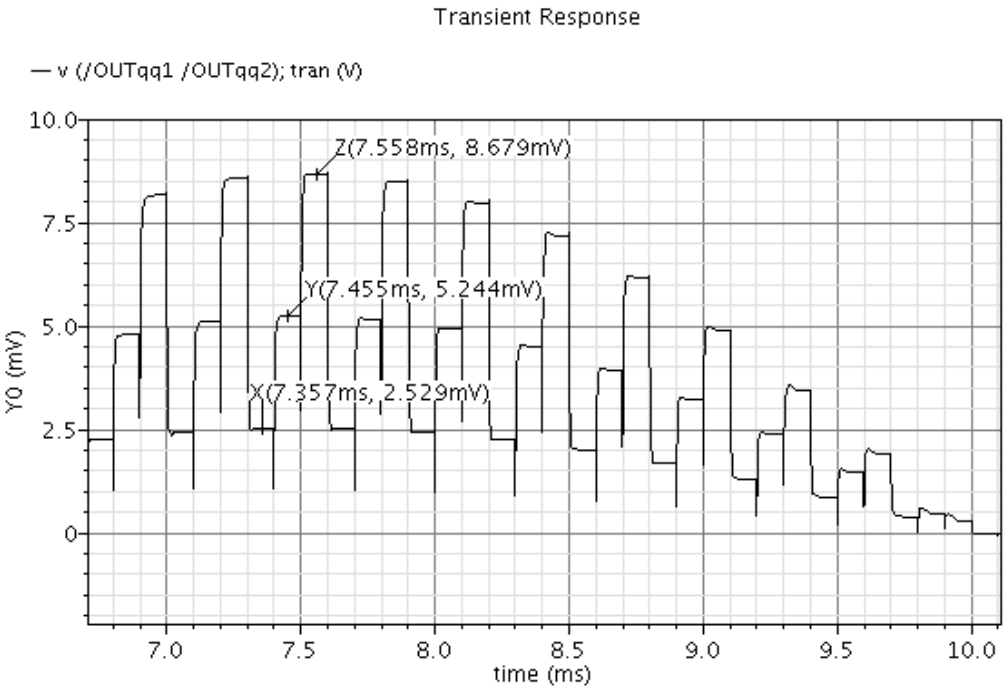


Figure 3.31: The closer look of Figure 3.30

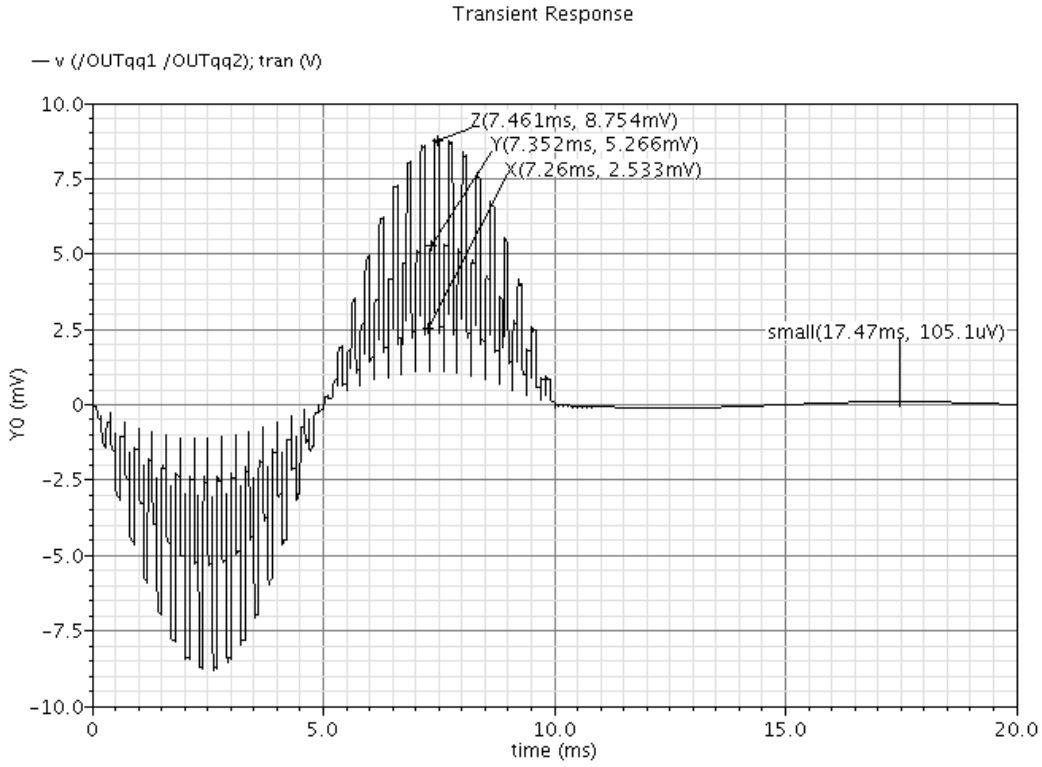


Figure 3.32: The first stage output simulation results in FF corner

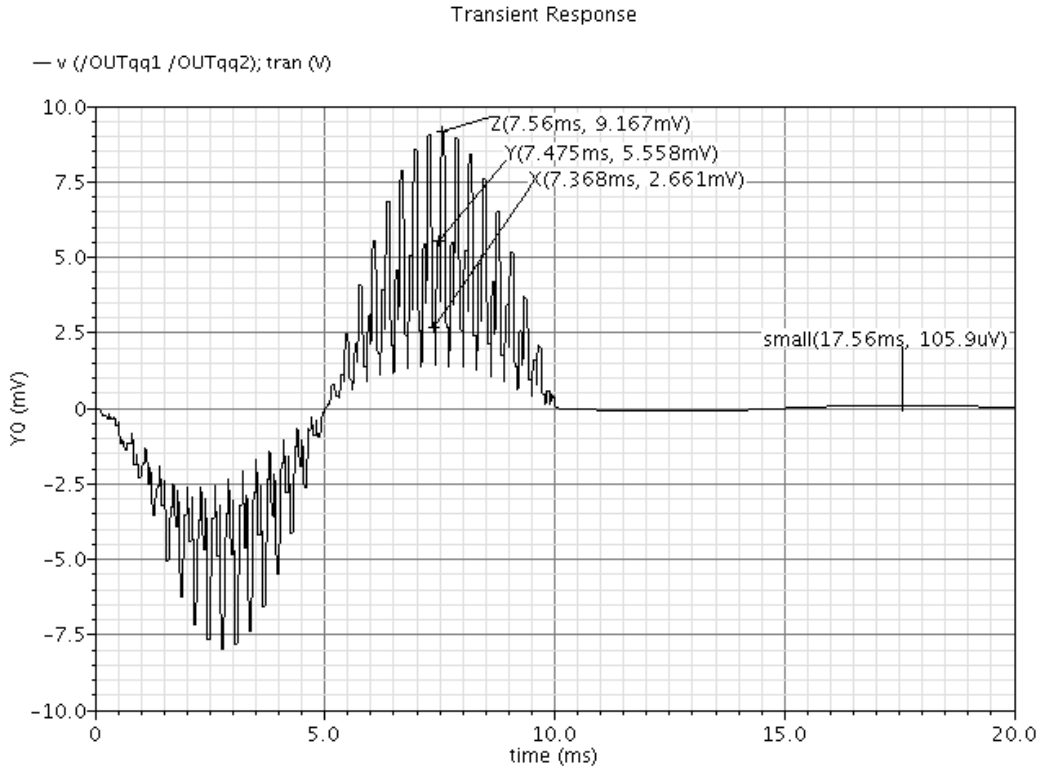


Figure 3.33: The first stage output simulation results in SS corner

Table 3.8: The amplitude of the first stage

Amplitude	TT	FF	SS
X	2.52mV	2.53 mV	2.66 mV
Y	5.24mV	5.26 mV	5.56 mV
Z	8.68mV	8.75mV	9.16mV
small	106.5uV	105.1uV	105.9uV

3.9 The Second and Third stage

The schematic of the second and the third stage is shown in Figure 3.34. The second

stage is an amplifier stage and the operating principle is described before. It can amplify both three-axis accelerometer and additive sensor with smaller capacitance change signals the same times and the gain of second stage is $\frac{C1}{C2}$. The third stage is an integrator and it can integrate the signal from the second stage. In the third stage, there are four switches called clear switches and are controlled by clock phase 2. When clock phase 2 is high, the integrator's input and output will short together to reset output, and when clock phase 2 is low, the integrator will integrate the signal. The reason why the integrator needs clear switches is that because only when clock phase 1 is high, the desired signal will be generated from second stage, and the integrator can integrated it. However, if without clear switches, when clock phase 1 is low, the integrator will integrate the undesired signal and causes error. In other words, the clear switches can not only avoid error but also save power. (Because the integrator does not integrate when clock phase 2 is high.) The gain of the integrator is inversely proportional to integration capacitance. In this way, tunable gain can be achieved by adjusting integration capacitance to make two sensors with similar output amplitudes. There are two different integration capacitances C4, C6 and C4 is always connected to integrator and C6 is controlled by EN. When read three-axis accelerometer (EN is high), the bigger integration capacitance C6 connects to integrator, to make amplification smaller. And when read additive sensor, the smaller

integration capacitance C4 connects to integrator, to make amplification higher. The capacitance C4 is always connected to integrator because C4 is much smaller than C6 and the two capacitances in parallel have little effect on C6. In addition, the control signals ON1~ON4 can adjust integration capacitance size to have different gains. And the gain adjustable range is 1 to 5 times. The simulation results are shown in Figure 3.35 ~ 3.39 and Table 3.9 and the operation frequency of the both sensors are 100Hz. In addition, the tunable gains simulation results will be shown in the fourth stage.

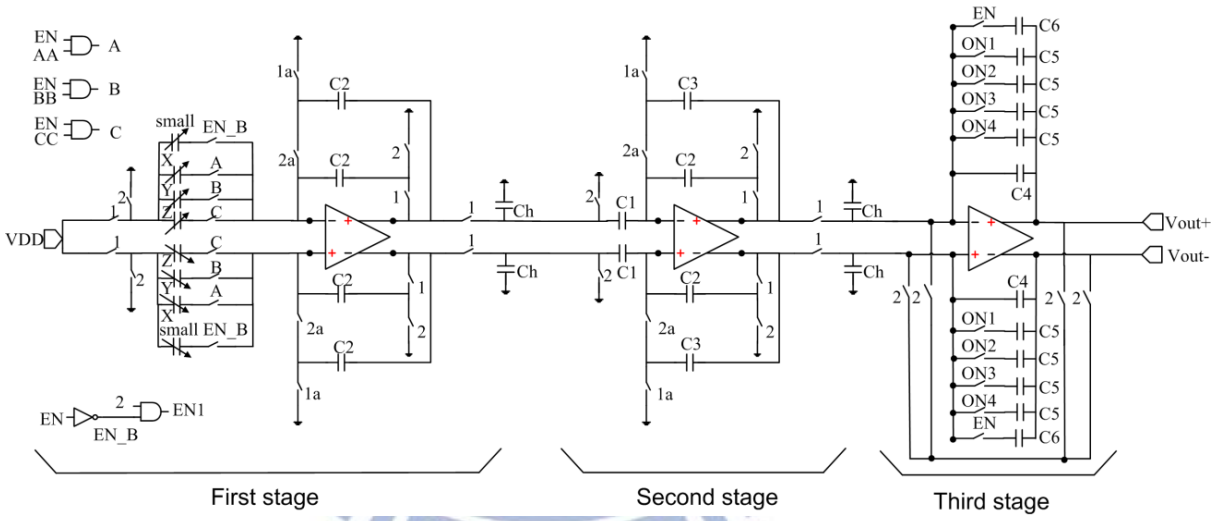


Figure 3.34: The schematic of the second and the third stage

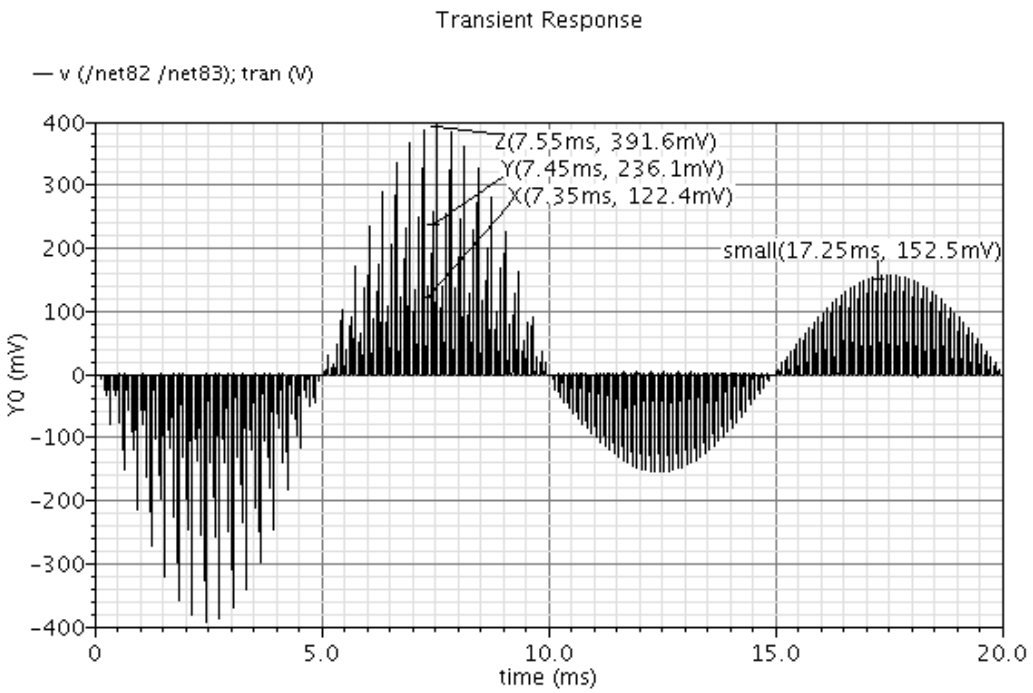


Figure 3.35: The third stage output simulation results in TT corner

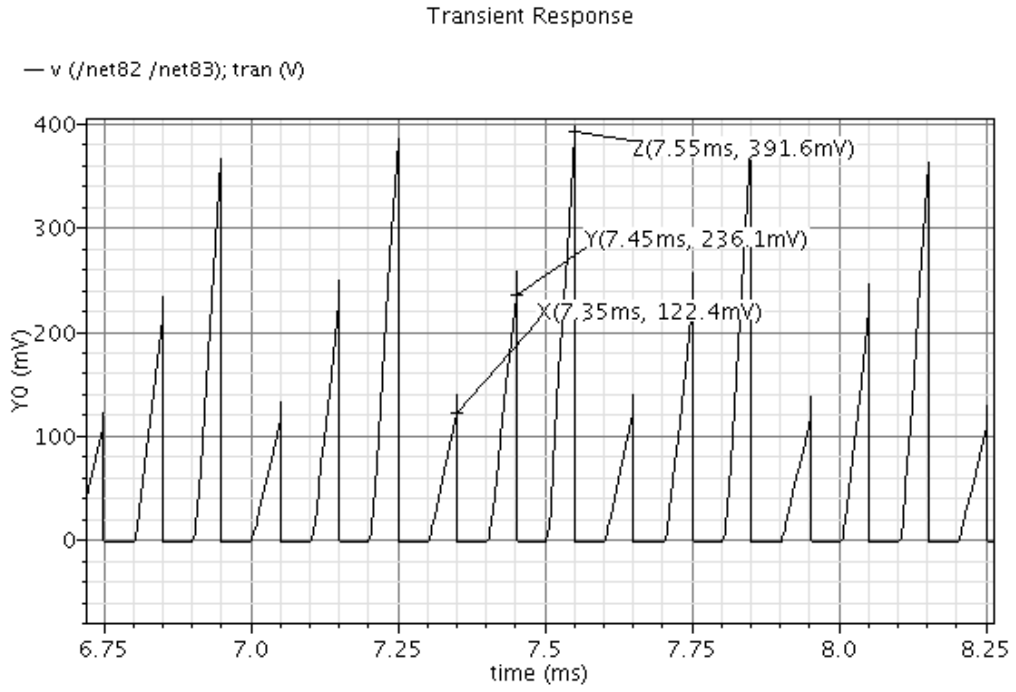


Figure 3.36: The closer look of Figure 3.35 for three-axis accelerometer signal

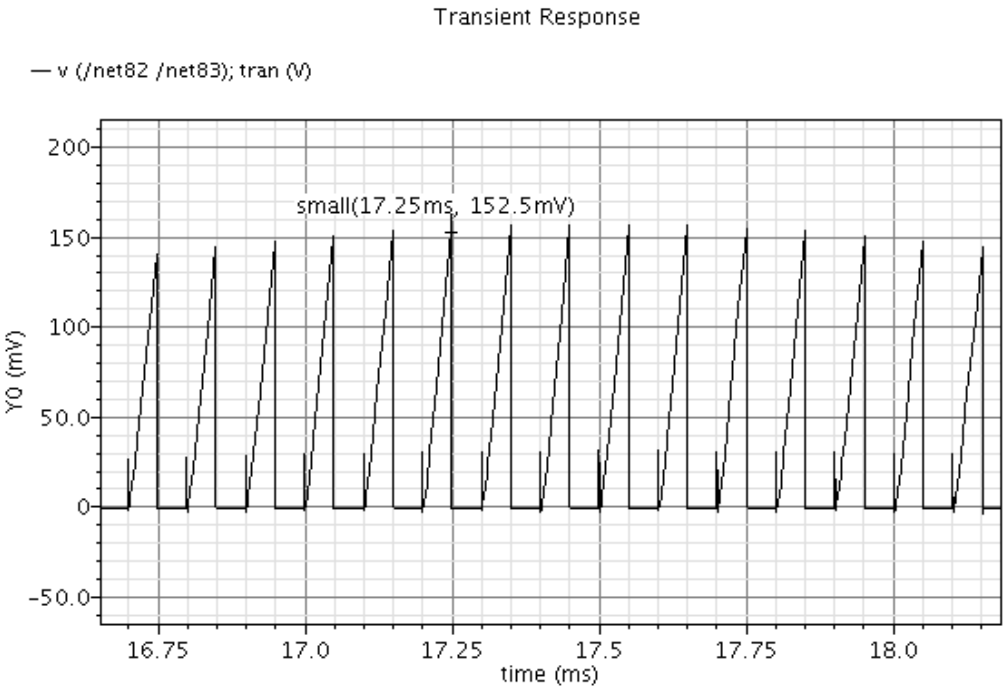


Figure 3.37: The closer look of Figure 3.35 for another sensor signal

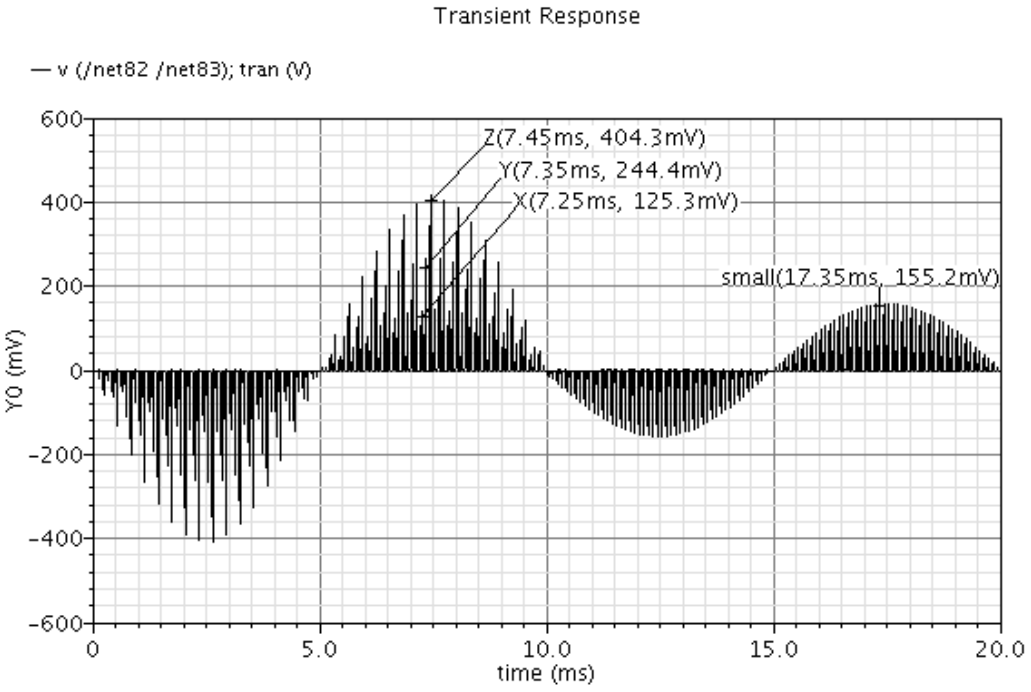


Figure 3.38: The third stage output simulation results in FF corner

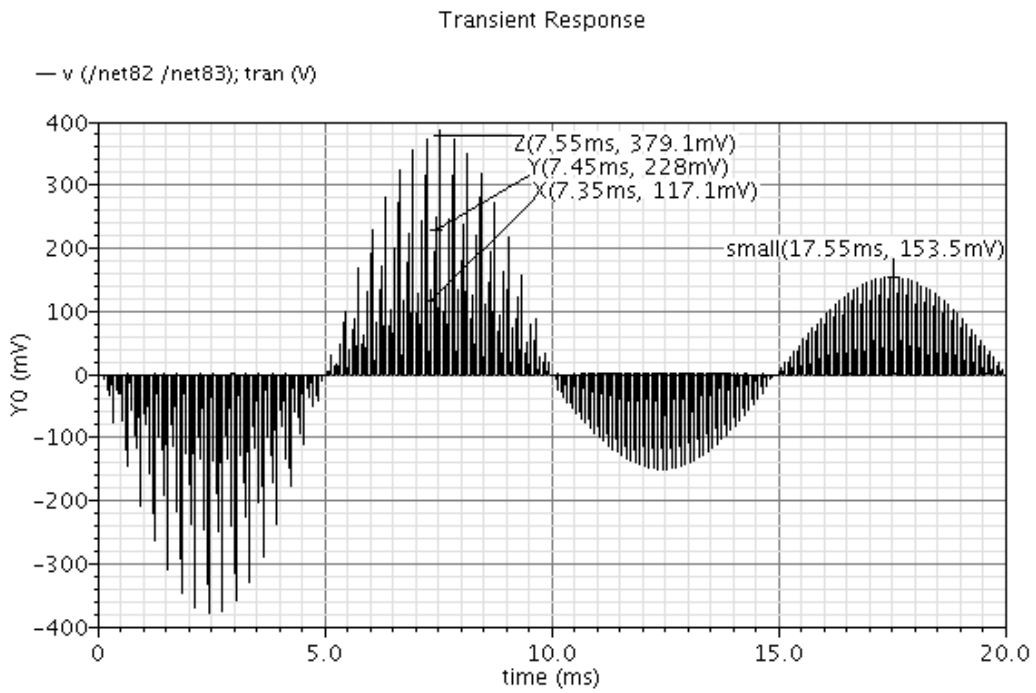


Figure 3.39: The third stage output simulation results in SS corner

Table 3.9: The amplitude of the third stage

	TT	FF	SS
X-axis	122.4 mV	125.3 mV	117.1 mV
Y-axis	236.1 mV	244.4 mV	228 mV
Z-axis	391.6mV	404.3 mV	379.1 mV
additive sensor	152.5 mV	155.2 mV	153.5 mV

3.10 The Fourth stage

The fourth stage is a S&H stage as shown in Figure 3.40. It can separated the mixed signal from the third stage and generated eight outputs VoutX+, VoutY+, VoutZ+,

small+, VoutX-, VoutY-, VoutZ-, and small- respectively. The control signals (A, B, C, EN1) in the fourth stage have been already generated in the first stage and by using these control signals, the time division function can be achieve. The simulation results are illustrated in Figure 3.41 ~ 3.43 and Table 3.10. These simulation results show the fourth stage differential output waveform in different corners. We can see the mixed signals from the third stage (Figure 3.35) are separated by the control signals. Figure 3.44 ~ 3.52 and Table 3.11 ~ 3.13 show the fourth stage differential output waveform by adjusting the integration capacitance C5. The markers M0~M4 in Figure 3.44 ~ 3.52 represent how many control signals ON1~ON4 are high. For example, M0 means all ON1~ON4 are low, so the integration capacitance is the smallest making the output amplitude the highest. The capacitances C5 and C6 have the same value (900fF), so the tunable gain range is 1~5 times.

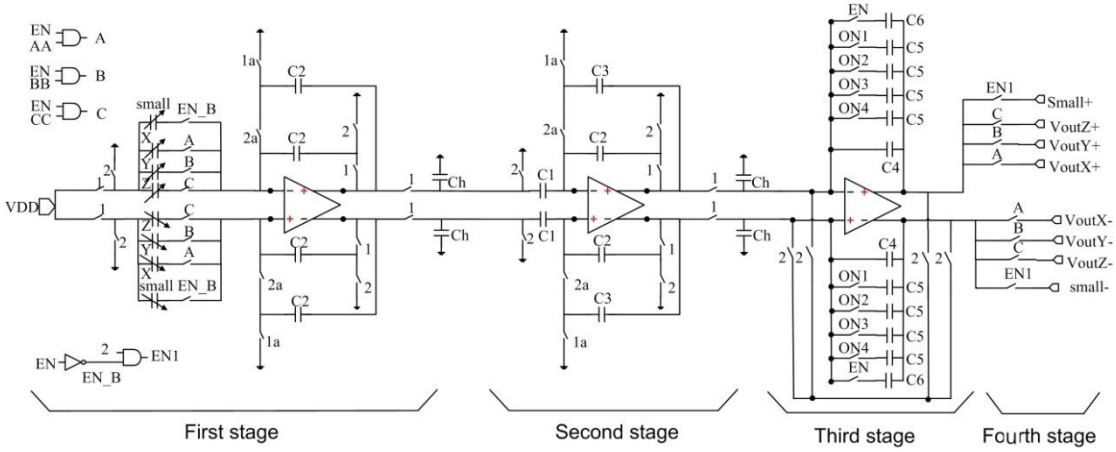


Figure 3.40: The schematic of fourth stage

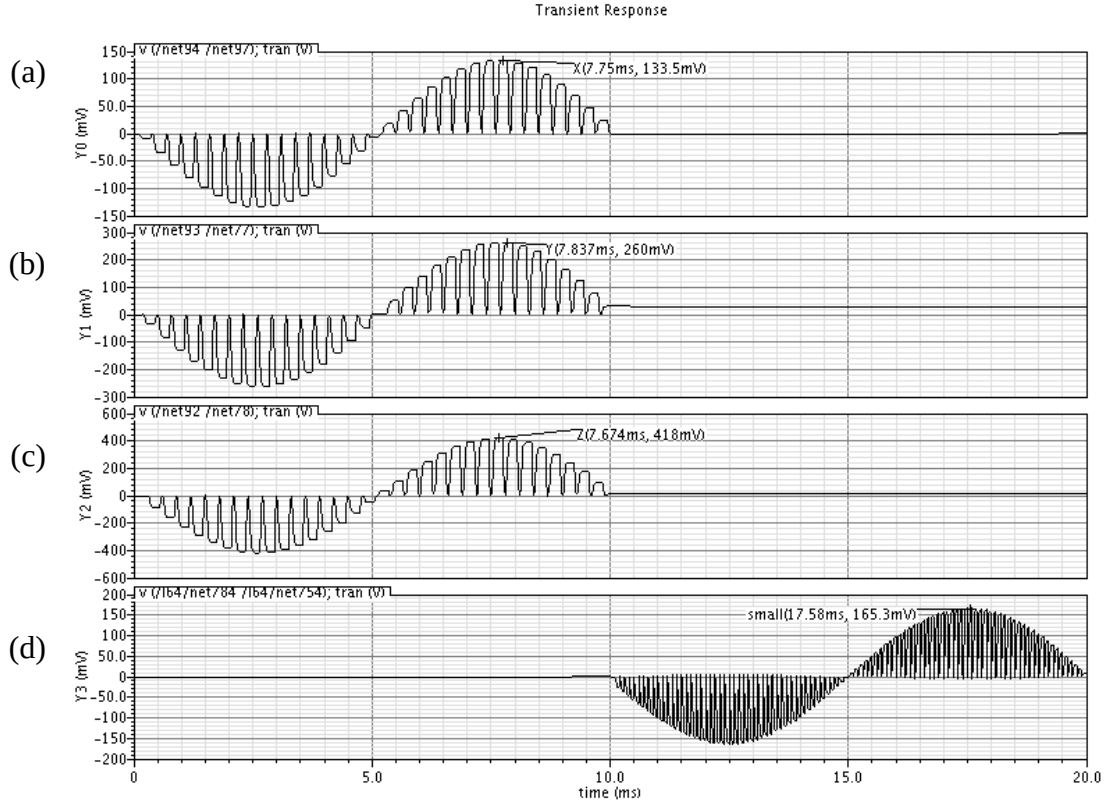


Figure 3.41: The fourth stage output simulation results in TT corner (a) X-axis output

(b) Y-axis output (c) Z-axis output (d) Additive sensor output

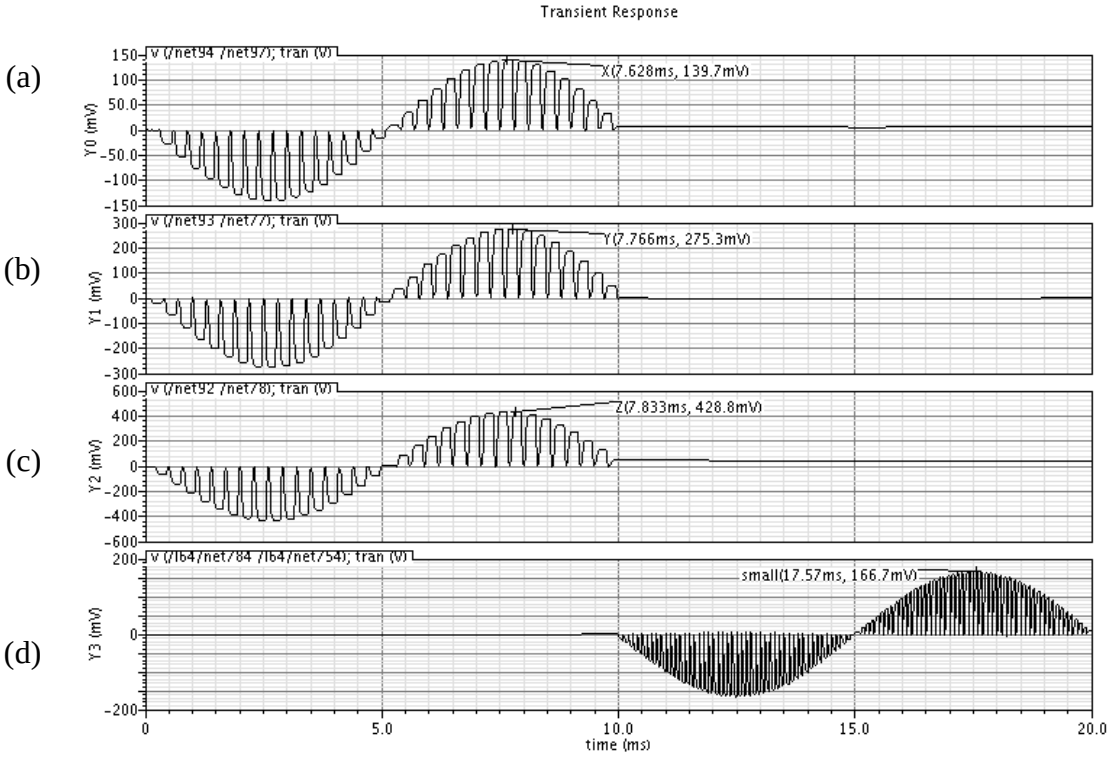


Figure 3.42: The fourth stage output simulation results in FF corner (a) X-axis output

(b) Y-axis output (c) Z-axis output (d) Additive sensor output

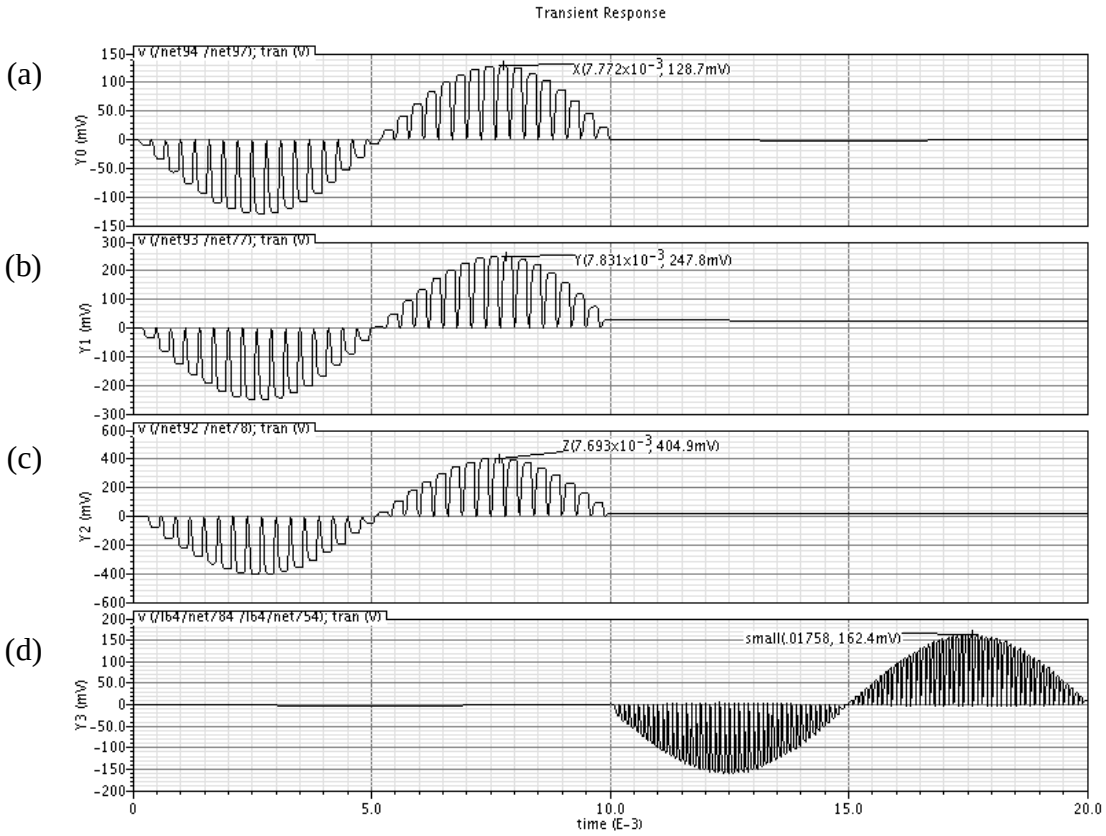


Figure 3.43: The fourth stage output simulation results in SS corner (a) X-axis output

(b) Y-axis output (c) Z-axis output (d) Additive sensor output

Table 3.10: The amplitude of the fourth stage

	TT	FF	SS
X-axis	133.5 mV	139.7 mV	128.7 mV
Y-axis	260 mV	275.3 mV	247.8 mV
Z-axis	418mV	428.8 mV	304.9 mV
Additive sensor	165.3 mV	166.7 mV	162.4 mV

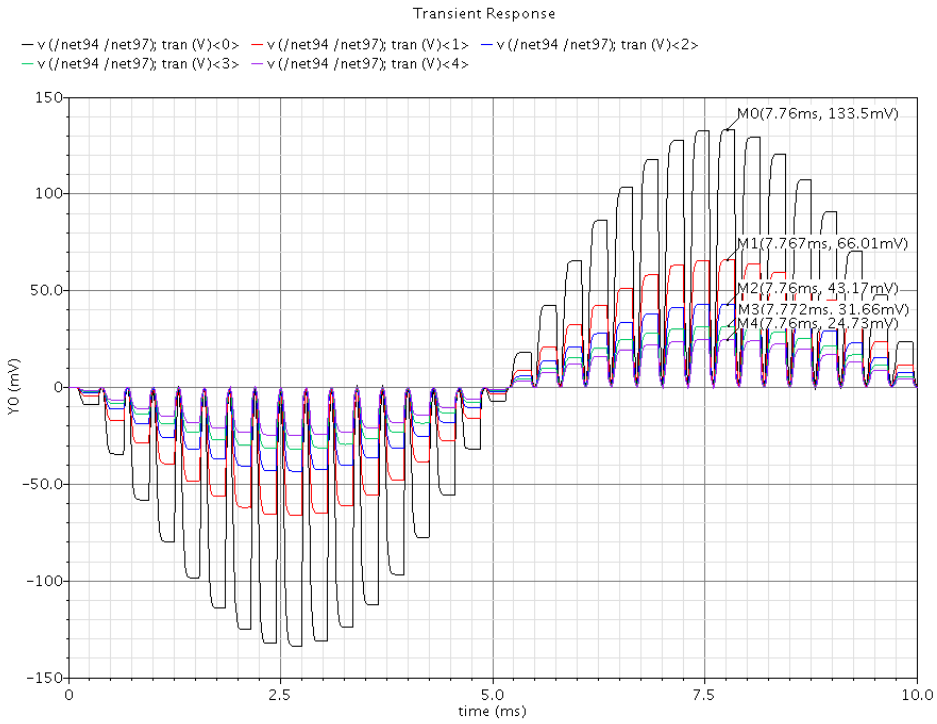


Figure 3.44: The fourth stage simulated X-axis output waveform by adjusting the integration capacitance in TT corner

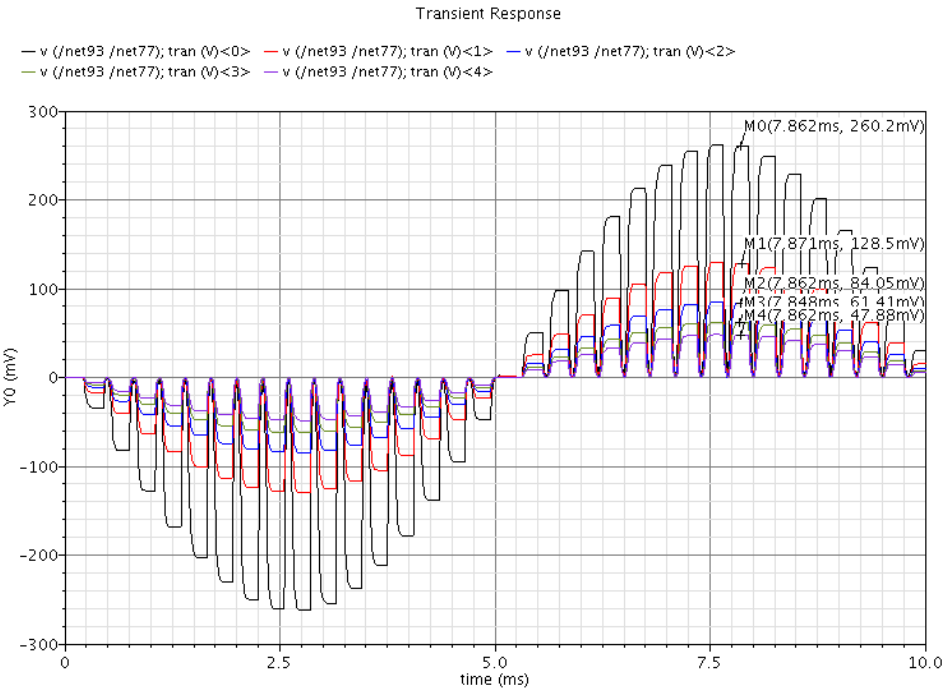


Figure 3.45: The fourth stage simulated Y-axis output waveform by adjusting the integration capacitance in TT corner

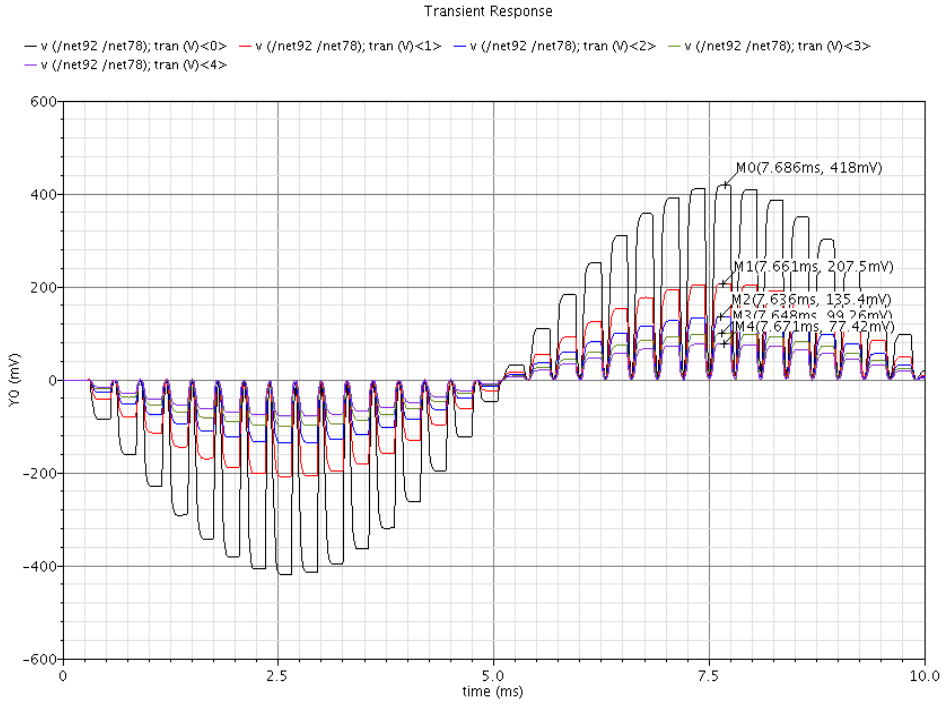


Figure 3.46: The fourth stage simulated Z-axis output waveform by adjusting the integration capacitance in TT corner

Table 3.11: The fourth stage simulated output amplitude in TT corner

	X-axis	Y-axis	Z-axis	ON1	ON2	ON3	ON4
Amplitude TT	133.5mV	260.2mV	418 mV	low	low	low	low
	66.01mV	128.5mV	207.5mV	low	low	low	high
	43.17mV	84.05mV	135.4mV	low	low	high	high
	31.66mV	61.41mV	99.26mV	low	high	high	high
	24.73mV	47.88mV	77.42mV	high	high	high	high
Times	5.4	5.43	5.4				

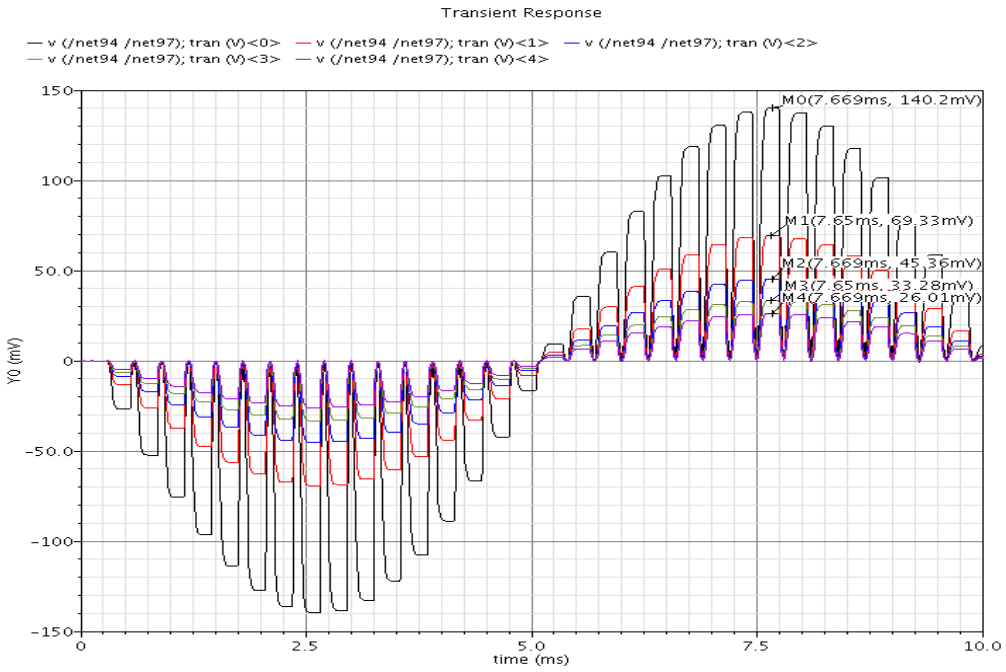


Figure 3.47: The fourth stage simulated X-axis output waveform by adjusting the integration capacitance in FF corner

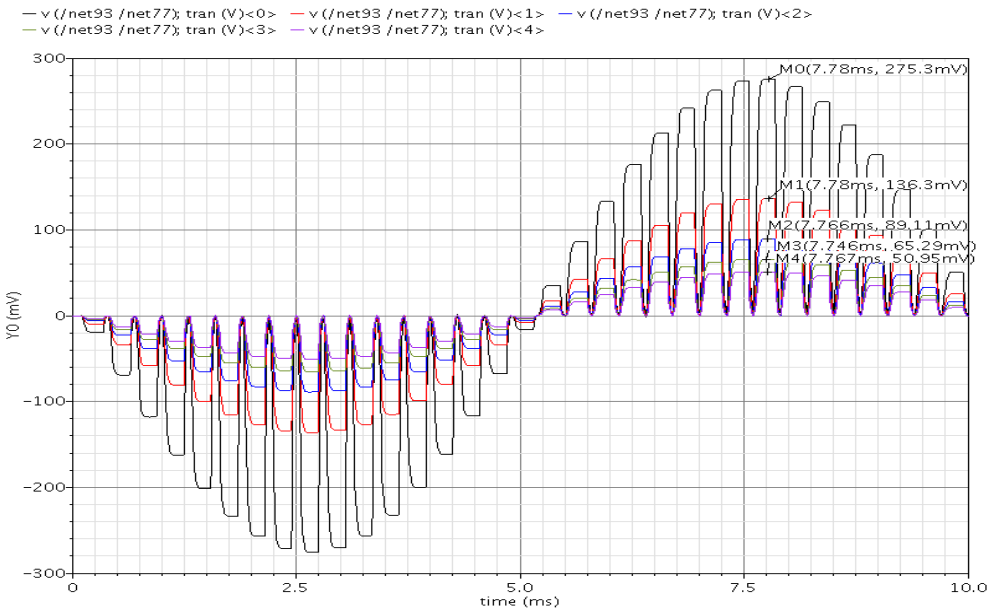


Figure 3.48: The fourth stage simulated Y-axis output waveform by adjusting the integration capacitance in FF corner

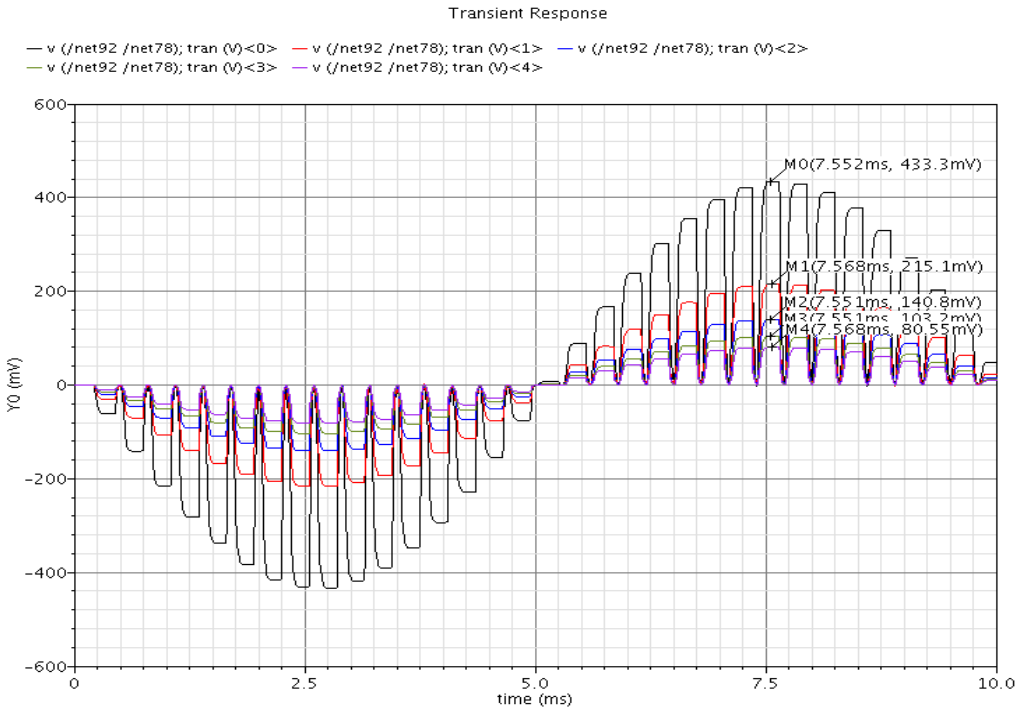


Figure 3.49: The fourth stage simulated Z-axis output waveform by adjusting the integration capacitance in FF corner

Table 3.12: The fourth stage simulated output amplitude in FF corner

	X-axis	Y-axis	Z-axis	ON1	ON2	ON3	ON4
Amplitude FF	140.2mV	275.3mV	433mV	low	low	low	low
	69.33mV	136.3mV	215.1mV	low	low	low	high
	45.36mV	89.11mV	140.8mV	low	low	high	high
	33.28mV	65.29mV	103.2mV	low	high	high	high
	26.01mV	50.95mV	80.55mV	high	high	high	high
Times	5.4	5.4	5.37				

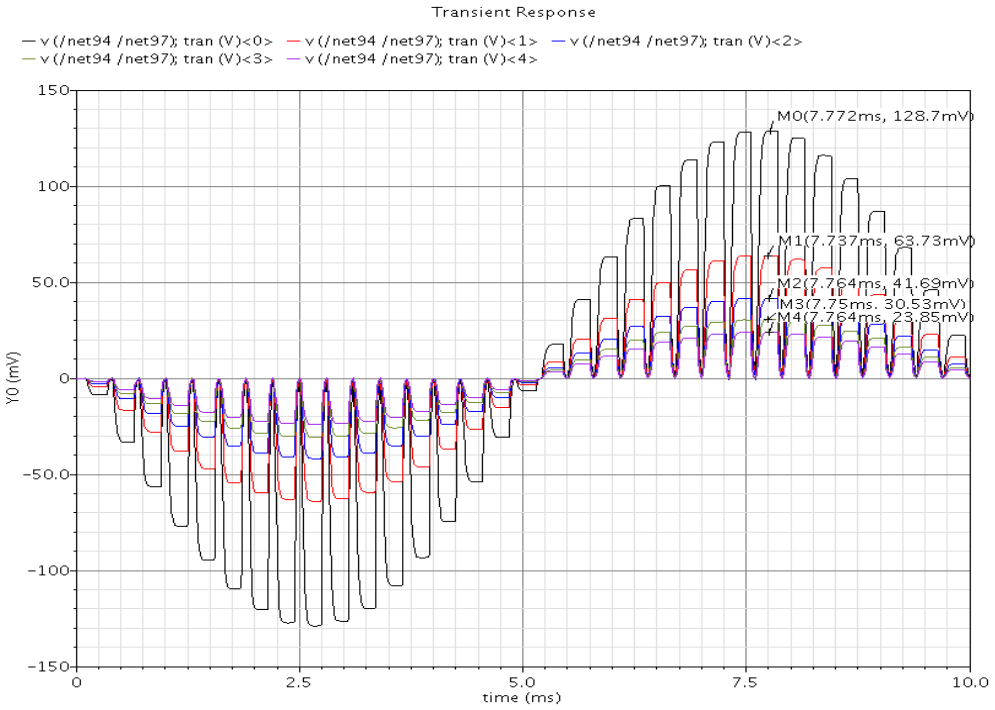


Figure 3.50: The fourth stage simulated X-axis output waveform by adjusting the integration capacitance in SS corner

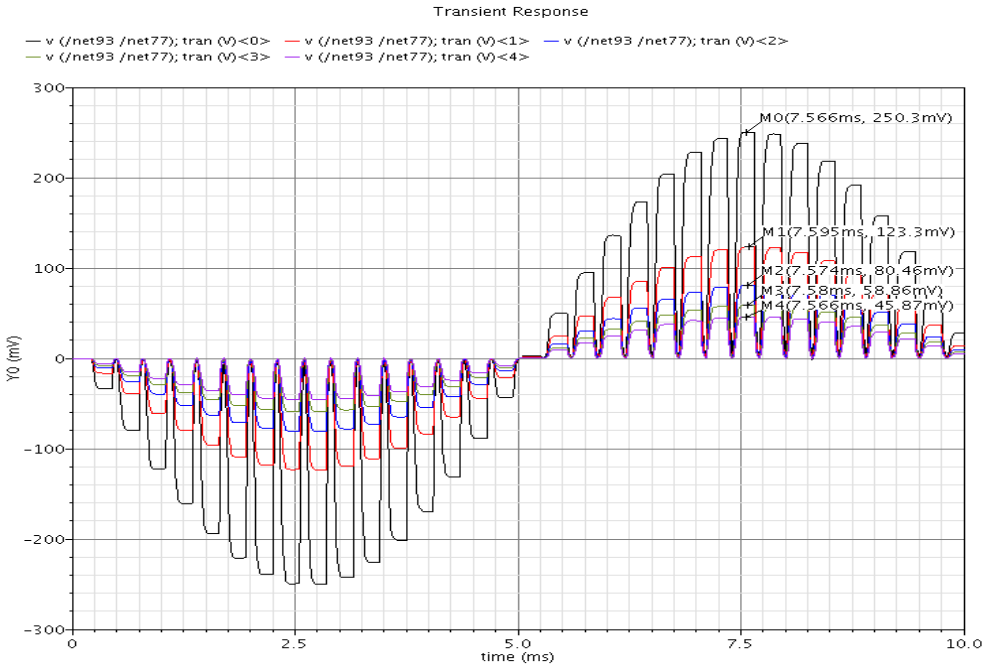


Figure 3.51: The fourth stage simulated Y-axis output waveform by adjusting the integration capacitance in SS corner

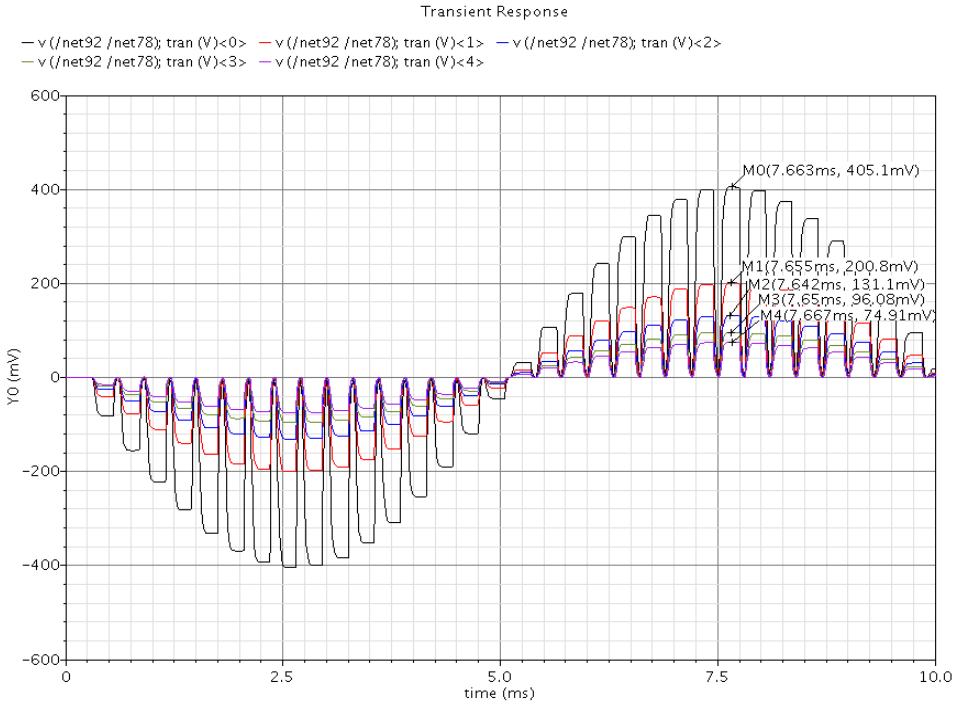


Figure 3.52: The fourth stage simulated Z-axis output waveform by adjusting the integration capacitance in SS corner

Table 3.13: The fourth stage simulated output amplitude in SS corner

	X-axis	Y-axis	Z-axis	ON1	ON2	ON3	ON4
Amplitude SS	128.7mV	250.3mV	405.1mV	low	low	low	low
	63.73mV	123.3mV	200.8mV	low	low	low	high
	41.69mV	80.46mV	131.1mV	low	low	high	high
	30.53mV	58.86mV	96.08mV	low	high	high	high
	23.85mV	45.87mV	74.91mV	high	high	high	high
Times	5.4	5.45	5.41				

Chapter 4 MEMS and ASIC Co-Simulation

4.1.1 The Flow of MEMS and ASIC Co-Simulation

As shown in Figure 4.1, the design flow for the accelerometer design and co-simulated with readout circuit is illustrated. The three-axis accelerometer layout is first drawn in Cadance environment. After the three-axis accelerometer layout is finished, the layout file is imported to CoventorWarea. With the CMOS MEMS process file [10] as shown in Figure 4.2 provided by the CIC, this layout file can be converted to a 3-D model and can be analyzed by mechanical simulations in CoventorWare. After the simulations are finished, we can get the parameters like the stationary capacitances, displacement, and resonant frequency. By Eq. (2.2) and Eq. (2.5), we can calculate the capacitance change. Imports these parameters into the Verilog-A model which is described in Eq. (4.1) and shown in Figure 4.3 and this Verilog-A model can be co-simulated with the readout circuit. Then we can check the sensitivity whether meets the specification or not. If not meets the specification, we can adjust the accelerometer layout or readout circuit to come up to the required standard. Last, according to the final co-simulation results, the final design is determined to be implemented.

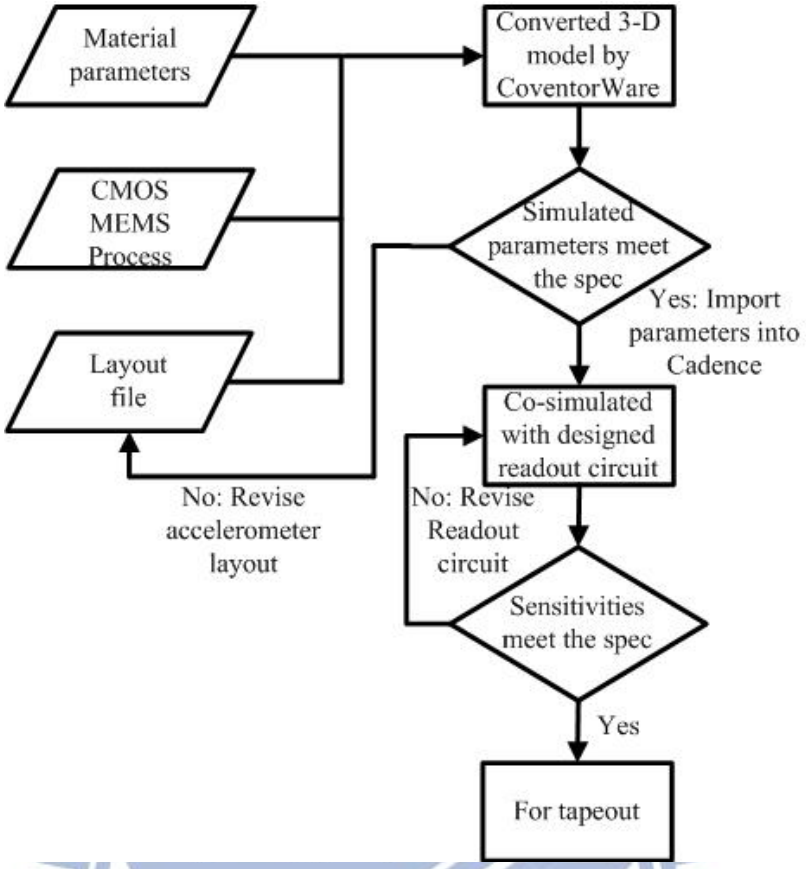


Figure 4.1: The flow of co-simulation

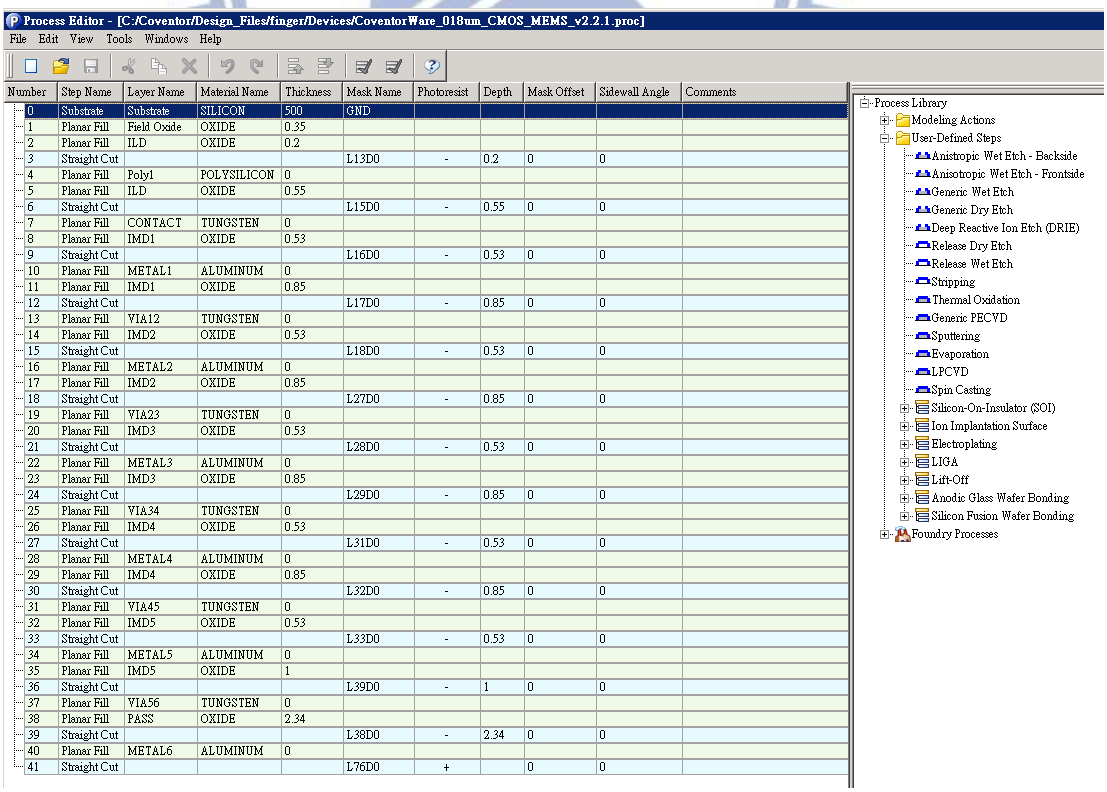


Figure 4.2: The process file

$$Cc = Cs + \Delta C * V \tag{4.1}$$

where Cc is the total capacitance, Cs is the stationary capacitances, ΔC is the capacitance change, and V is a sine wave. The amplitude of V represents the size of acceleration. For example, the amplitude of 1V represents 1g acceleration.

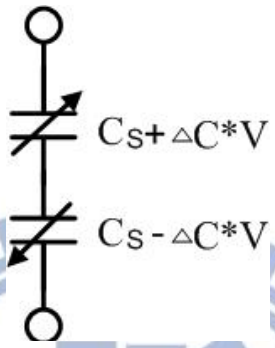


Figure 4.3: The equivalent capacitors of the linear model

4.3.1 System Simulation

Based on the Verilog-A model, the accelerometer can be transferred to hardware language for system simulation. The proposed readout circuit and the CMOS MEMS three-axis accelerometer is manufactured by TSMC 1P6M 0.18um CMOS mix-signal technology. The readout circuit is simulated in Cadence design environment using Spectre simulator. The readout circuit works with supply voltage 1.8V and the CDS clock frequency is 10kHz and the input signal clock frequency is 100Hz. The previous layout simulation (pre-simulation) of three corners is shown in Table 4.1 and the post layout simulation (post-simulation) of three corners is shown in Figure 4.6 ~ 4.8 and Table 4.2. However, in this tape out, it is not area efficiency to implement two sensors

in a single chip with similar operation principle. Therefore, I modify the original system architecture as shown in Figure 4.4 and the modified architecture is shown in Figure 4.5. In Figure 4.5, only the first stage has been modified, and the additive sensor has been replaced by a fixed value capacitance and a sinewave input signal. As discussed before, the CVC stage output waveform is $2 * \frac{\Delta C}{C_2} * VDD$ and the narrowband gain-compensated SC amplifier output waveform is $\frac{C_1}{C_2} Vin$. The output waveforms of both architectures are similar, only the variable changes from ΔC to Vin. Therefore, changing the amplitude of Vin is like changing the acceleration. In addition, the modified architecture can not only save area, but also can test the readout circuit work or not if sensor is not suspended. The modified architecture pre-simulation and post-simulation results are shown as below.

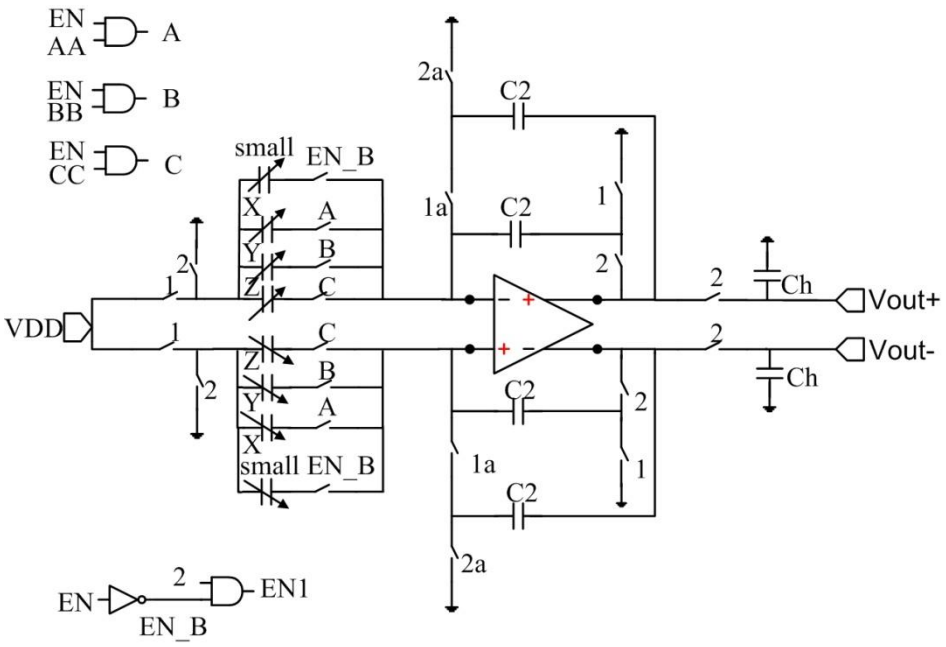


Figure 4.4: Original first stage architecture

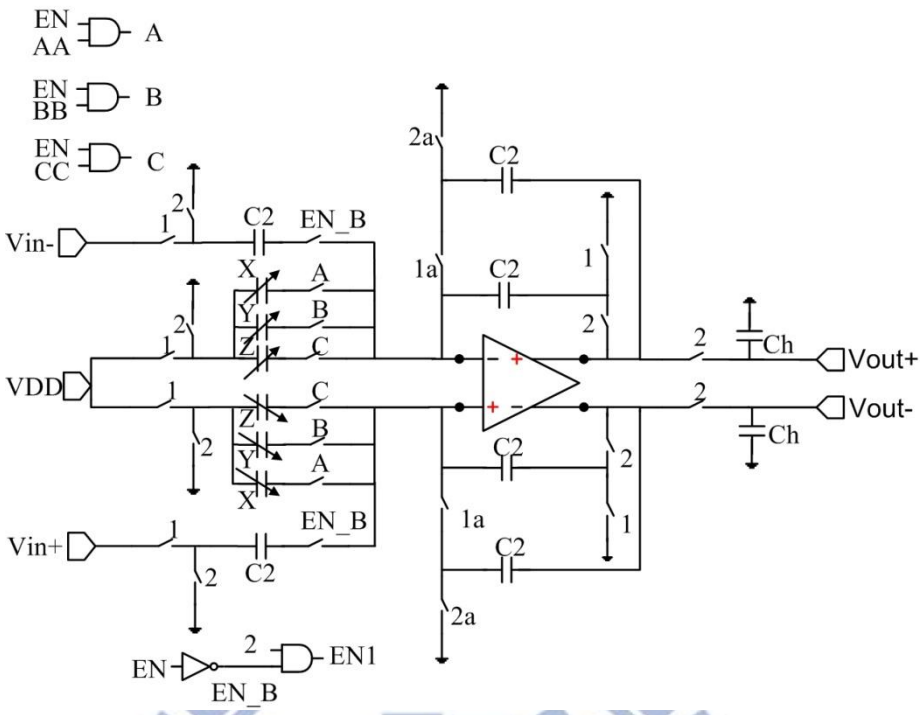


Figure 4.5: The modified first stage architecture

Table 4.1: pre-simulation of three corners

	X-axis	Y-axis	Z-axis	small
Amplitude (TT)	146.4 mV	283.9 mV	456.7 mV	296.7 mV
Times (TT)	5.4	5.43	5.4	
Amplitude (FF)	152.7 mV	299 mV	466.8 mV	302.9 mV
Times (FF)	5.4	5.4	5.37	
Amplitude (SS)	140.4 mV	273.5 mV	442.4 mV	292.3 mV
Times (SS)	5.4	5.45	5.41	

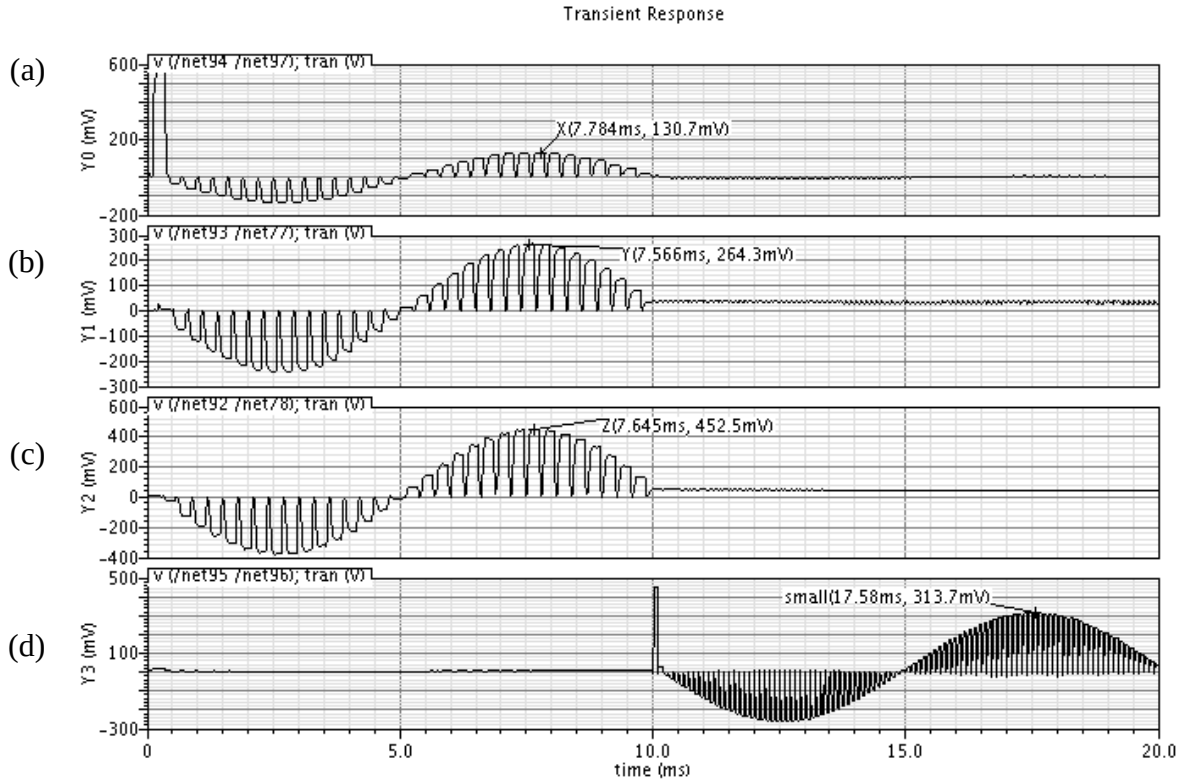


Figure 4.6: The post-simulation results in TT corner (a) X-axis output (b) Y-axis output (c) Z-axis output (d) Another sensor output

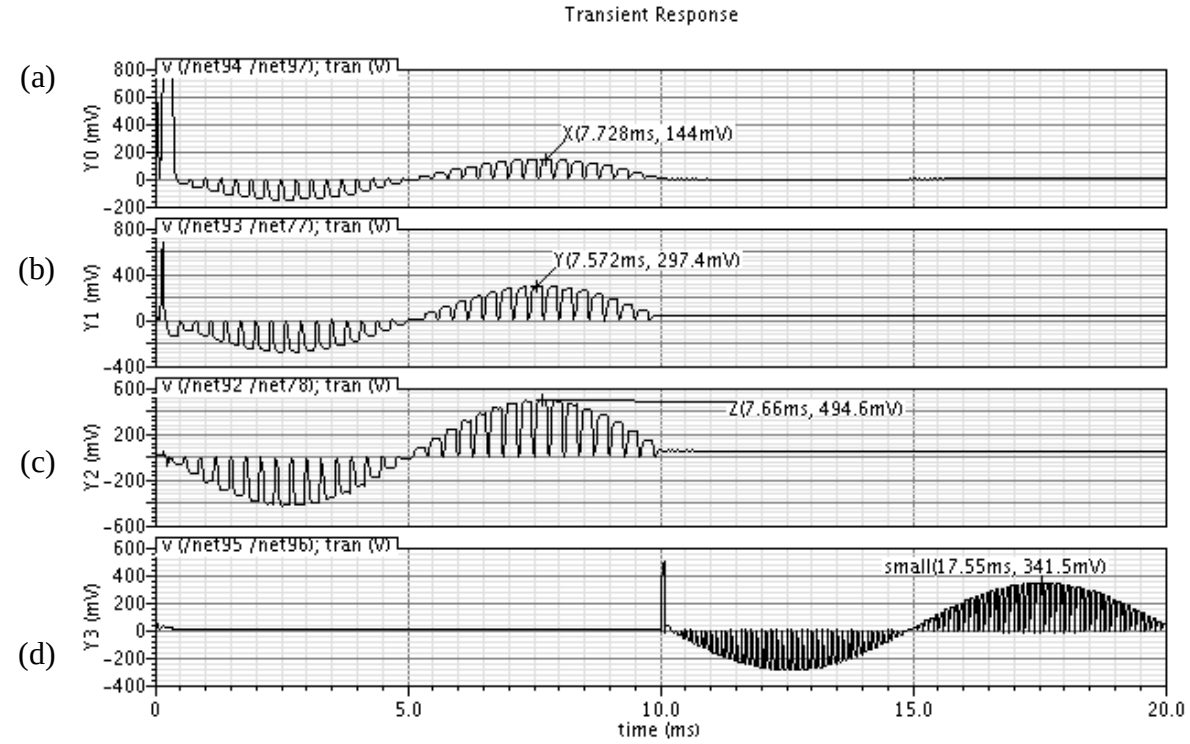


Figure 4.7: The post-simulation results in FF corner (a) X-axis output (b) Y-axis output (c) Z-axis output (d) Another sensor output

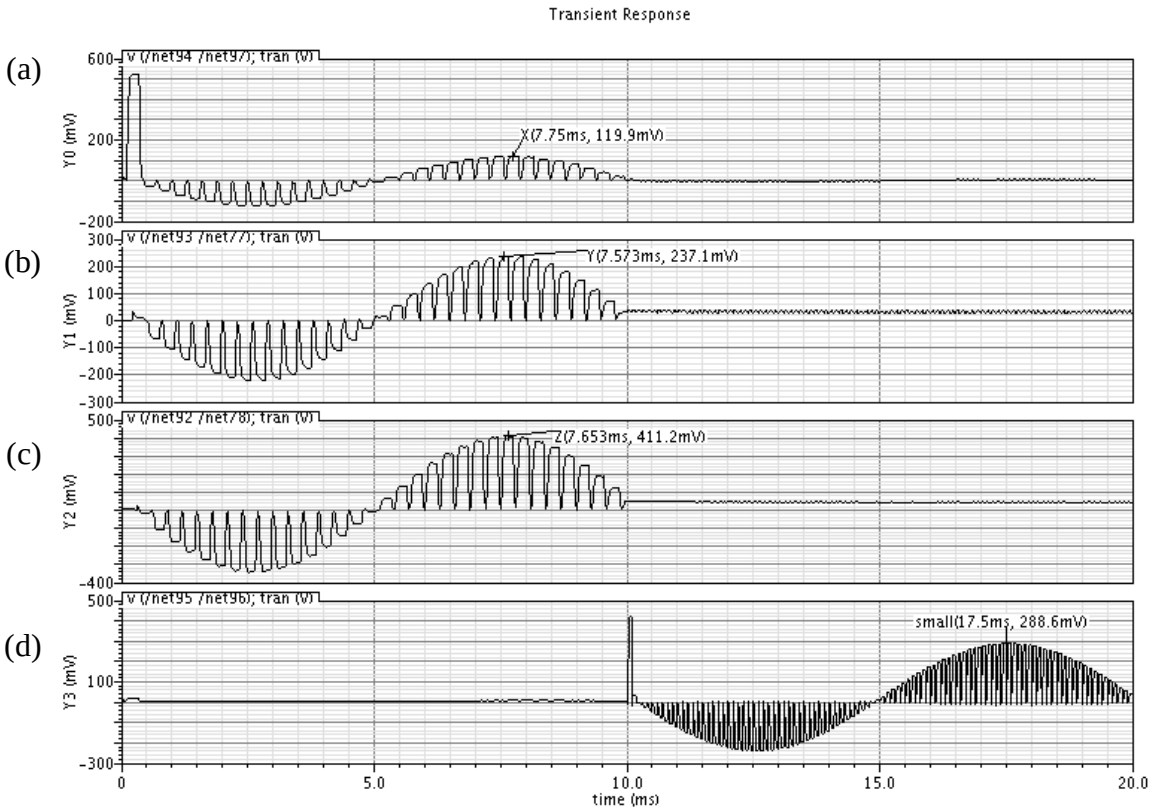


Figure 4.8: The post-simulation results in SS corner (a) X-axis output (b) Y-axis output (c) Z-axis output (d) Another sensor output

Table 4.2: post-simulation of three corners

	X-axis	Y-axis	Z-axis	small
Amplitude (TT)	130.7 mV	264.3 mV	452.5 mV	313.7 mV
Times (TT)	5.2	5.24	5.2	
Amplitude (FF)	144 mV	297.4 mV	494.6 mV	341.5 mV

Times (FF)	5.2	5.2	5.16	
Amplitude (SS)	119.9 mV	237.1 mV	411.2 mV	288.6 mV
Times (SS)	5.2	5.25	5.22	

4.3.2 The universal readout circuit noise simulation

The universal readout circuit input referred noise is simulated by the Spectre RF software. Because the output signals are discrete, the noise simulation is achieved by periodic noise analysis. Figure 4.9 illustrated the square noise power in three corners. The input referred noise can be calculated by the square root of integrating the square noise power from 1Hz to 100Hz (the designed bandwidth) and dividing by the bandwidth. The calculation results are listed in Table 4.3. In addition, the input referred noise of the universal readout circuit without CDS is also simulated, and is shown in Figure 4.10 and the calculation results are listed in Table 4.4. The power consumption simulations are listed in Table 4.5.

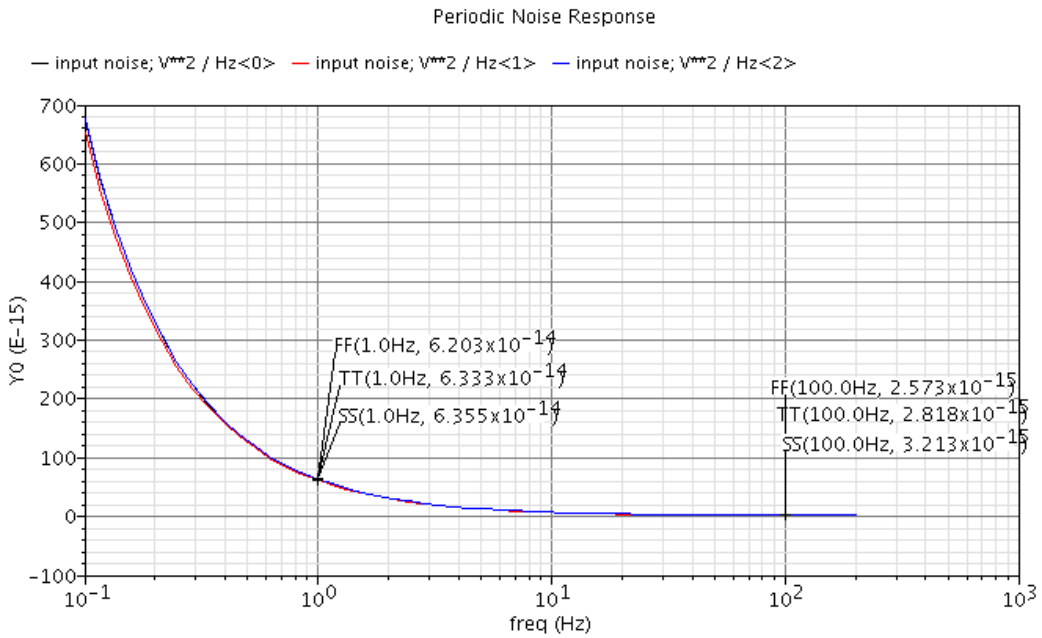


Figure 4.9: The square noise power with CDS

Table 4.3: Input referred noise with CDS

	TT	FF	SS
Input referred noise with CDS	65.4nV/√Hz	63.7 nV/√Hz	67.6 nV/√Hz

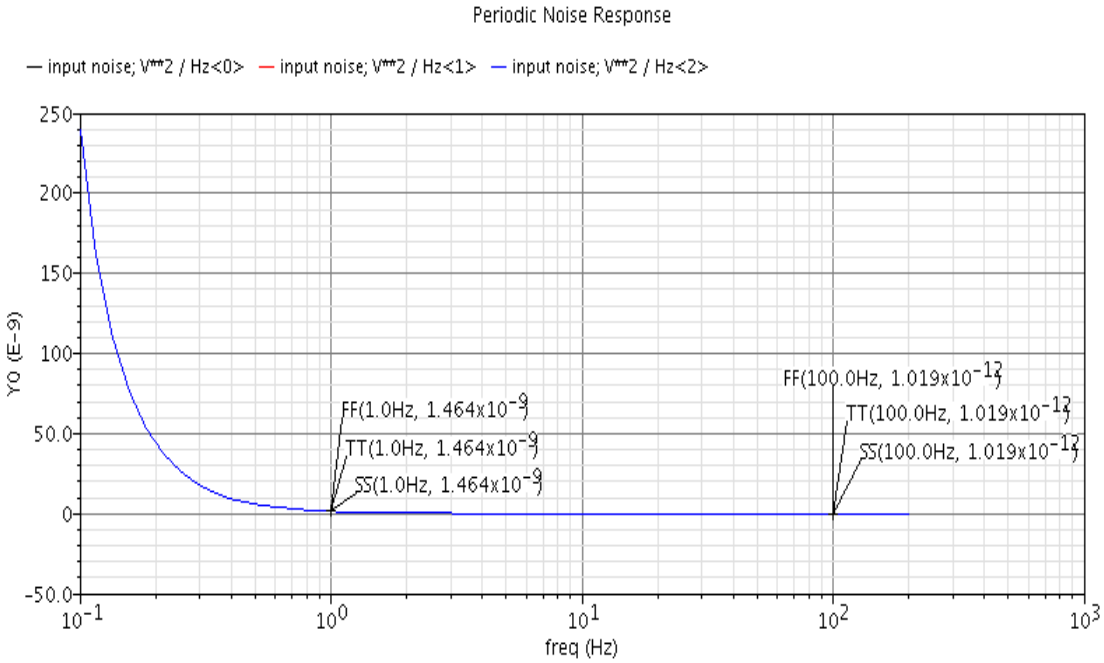


Figure 4.10: The square noise power without CDS

Table 4.4: Input referred noise without CDS

	TT	FF	SS
Input referred noise without CDS	4.1uV/√Hz	4.1uV/√Hz	4.1uV/√Hz

Table 4.5: The power consumption

	TT	FF	SS
Power	14.16μW	34.67μW	34.65μW

4.4 Physical layout

There are two times of tape out schedule on October 22 2012, (T18-101E) and February 25, 2013, (T18-102A) had been experimented during this thesis period.

4.4.1 The first tape out

The physical layout of the first tape out is illustrated in Figure 4.11 (a). This layout includes a three-axis accelerometer and two sets of readout circuits but cannot read additive sensor. One can read the sensor signal (Part A in Figure 4.11 (a)) and the other can read external sinewave input signal to test the functionality (Part B in Figure 4.11 (a)). The total layout area is 1333um*1507um. The label names of the bond pads are shown in Figure 4.11 (b). VDDA and GNDA are the power and ground of the analog circuits. VDD and GND are the power and ground of the ESD protection circuits. MV is the op-amp output CM dc voltage. CLK is the digital clock. OUTUPX, OUTUPY, OUTUPZ, OUTSUPX, OUTSUPY, OUTSUPZ are the differential outputs of the X, Y, Z axis. ON1~ON4 are the digital inputs. IN1, IN2, OUTUP1, OUTSUP1 are the differential inputs and outputs of the testing circuit. Table 4.6 shows the comparison with other works and the date of chip out is April 2, 2013.

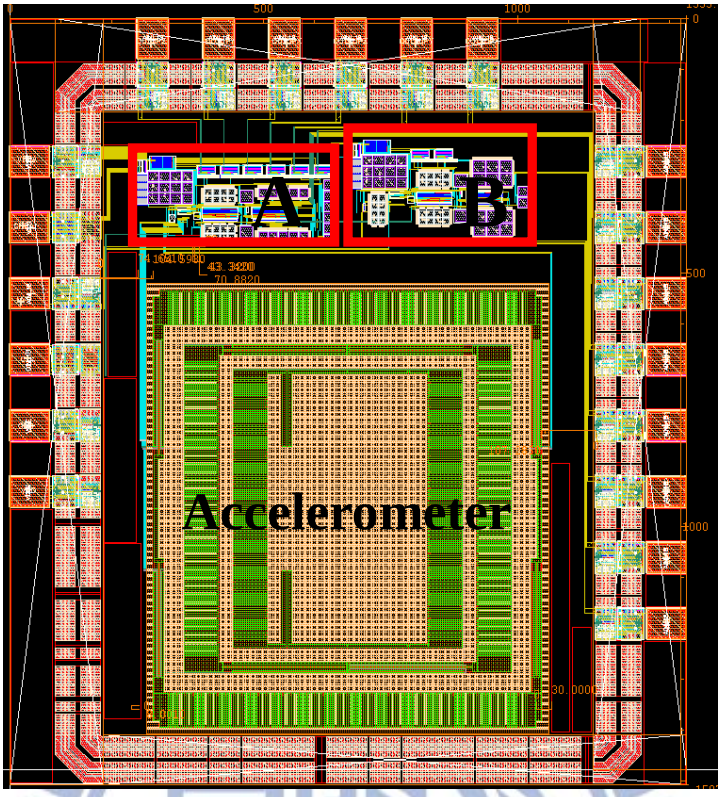


Figure 4.11 (a): Physical layout of the first tape out

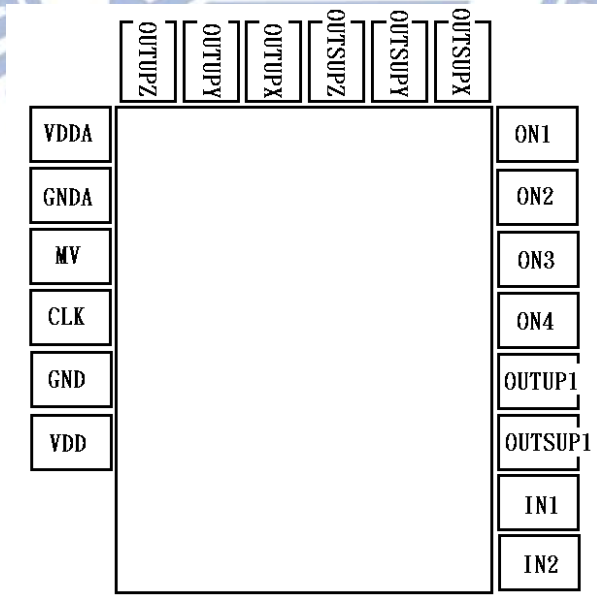


Figure 4.11 (b): The bonds PADs of the first tape out

Table 4.6: The comparison with other works

	2010[21]	2012[9]	2011[22]	2011[8]	This work
Process	0.35um CMOS technology	TSMC 0.18um	0.8um CMOS technology	0.18um CMOS technology	0.18um CMOS technology
CKT architecture		Dual Chopper+ CDS	Chopper+ CDS+ S/H	Chopper+ CDS	CDS
Power consumption	17.8mW	0.62mW	8.38mW	36uμW	15.98μW
Supply voltage	3.3V	1.8V	5V	1.8V	1.8V
Sensitivity	0.55V/g	6570.8~ 119.8mV/g	9980mV/g	150mV/g	100mV/g
Noise floor	N/A	12.57nV/√Hz	N/A	9.82nV/√Hz	169nV/√Hz

4.4.2 The Second tape out

The physical layout of the second tape out is illustrated in Figure 4.12 (a). This layout includes a three-axis accelerometer and a readout circuit which can read additive sensor. Like discussed before, the additive sensor has been replaced by a fixed value capacitance and a sinewave input signal. Therefore, unlike the first tape out, I do not need an additive test circuit. The total layout area is 1693um*1647um. The label names of the bond pads are shown in Figure 4.12 (b). VDDA and GNDA are the power and ground of the analog circuits. VDD and GND are the power and ground of the ESD protection circuits. MV is the op-amp output CM dc voltage. CLK is the digital clock. OUTUPX, OUTUPY, OUTUBZ, OUTSUBX, OUTSUBY, OUTSUBZ are the differential outputs of X, Y, Z axis. ON1~ON4 and EN are the digital inputs. VIN1, VIN2, OUT_UP, OUT_SUB are the differential inputs and

outputs of the readout circuit. Table 4.6 shows the comparison with other works.

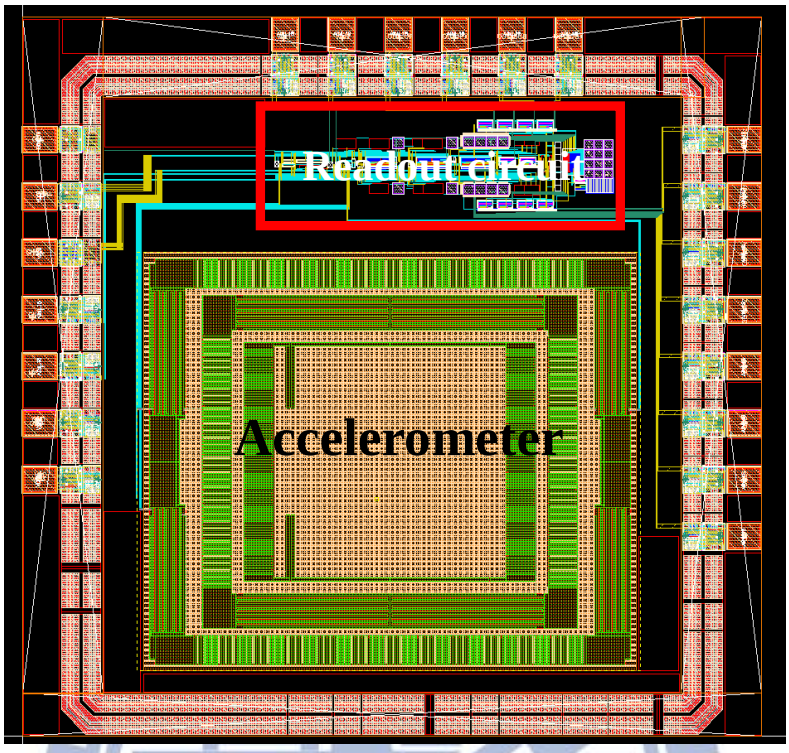


Figure 4.12 (a): Physical layout of the second tape out

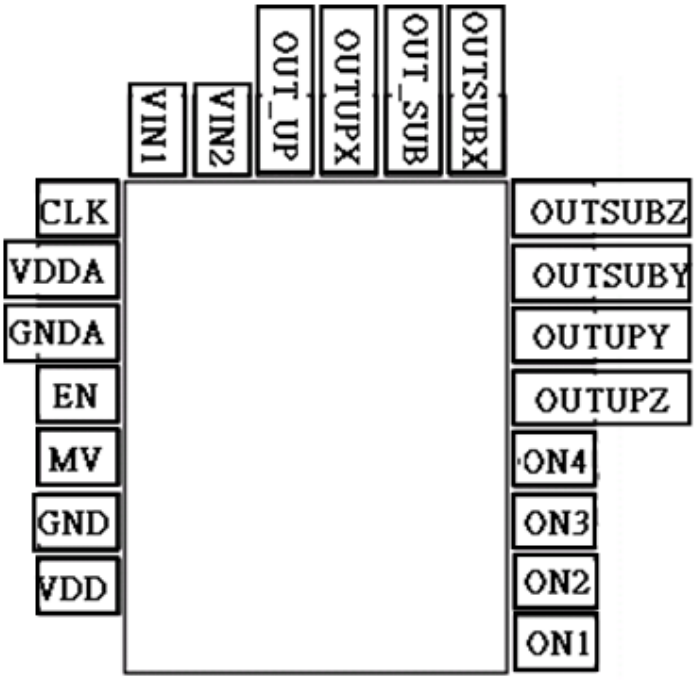


Figure 4.12 (b): The bonds PADs of the second tape out

Table 4.7: The comparison with other works

	2010[21]	2012[9]	2011[22]	2011[8]	This work
Process	0.35um CMOS technology	TSMC 0.18um	0.8um CMOS technology	0.18um CMOS technology	0.18um CMOS technology
CKT architecture		Dual Chopper+ CDS	Chopper+ CDS+ S/H	Chopper+ CDS	CDS
Power consumption	17.8mW	0.62mW	8.38mW	36μW	16.8μW
Supply voltage	3.3V	1.8V	5V	1.8V	1.8V
Sensitivity	0.55V/g	6570.8~ 119.8mV/g	9980mV/g	150mV/g	100mV/g
Noise floor	N/A	12.57nV/√Hz	N/A	9.82nV/√Hz	66.8nV/√Hz

Chapter 5 Measurement

5.1 Measurement Results of T18-101E (The first tape out)

A monolithic three-axis accelerometer with tunable gain analog front end circuit using time division to read three-axis accelerometer signals in 0.18μm CMOS MEMS process is implemented in T18-101E. In this design, an additive test readout circuit is designed in. Like discussed before, the accelerometer signals ΔC is changed to Vin. Therefore, by using external sinewave generated from function generator, we can check the readout circuit works correctly or not if the accelerometer is not suspended. The measurement results of the three-axis accelerometer and test readout circuit are shown as below.

5.2 The three-axis accelerometer measurement

In this tape out, the readout circuit is manufactured by TSMC, and the three-axis accelerometer is manufactured by APM (Asia Pacific Microsystems, Inc). However, due to the unstable CMOS MEMS post process, the three-axis accelerometer is not suspended in DRIE step. By using SEM (scanning electron microscope) provided by CIC, I can check where the three-accelerometer is not suspended. Figure 5.1 shows the physical layout of the three-axis accelerometer and the line is the position where the accelerometer is cut by SEM and the characters A~K are the different regions of the accelerometer.

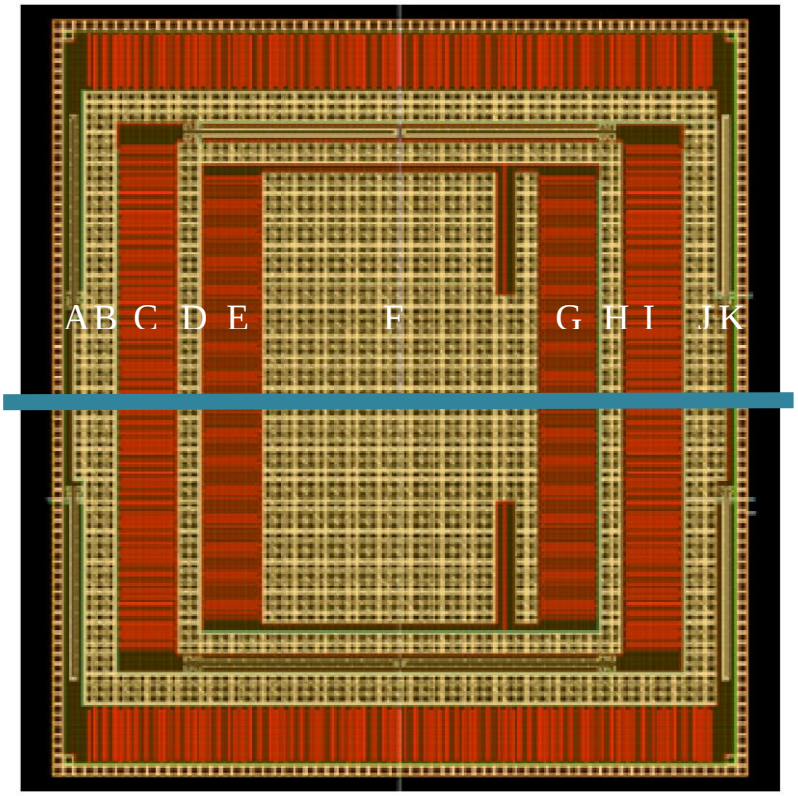


Figure 5.1: The physical layout of the three-axis accelerometer and the position where as cut by SEM

Figure 5.2 shows the result of the three-axis accelerometer in the unpackaged die as cut by SEM. We can see that some fingers are moved after being cut. This illustrates that fingers are suspended in DRIE step.

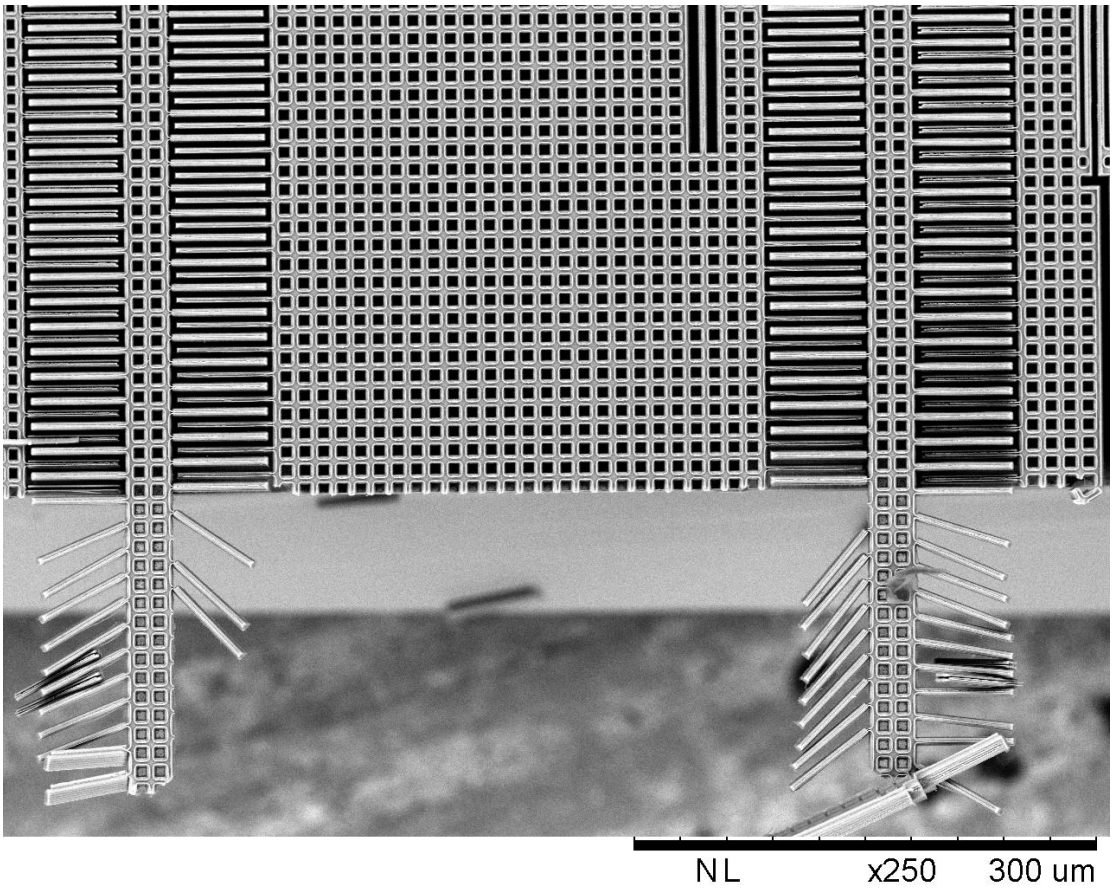


Figure 5.2: The result of the three-axis accelerometer is cut by SEM

Figure 5.3 shows the cross-sectional view of the three-axis accelerometer. The circles in Figure 5.3 show that the oxide and silicon are etched incompletely in DRIE step, and the rectangles show that the oxide and silicon are etched completely in DIRE step. The characters A~K are the positions of the three-axis accelerometer in Figure 5.1. According to Figure 5.3, we can see the positions A (springs), C (fingers), E (fingers), G (fingers), I (fingers), K (springs) are suspended successfully and the positions B (frame), D (frame), F (proof mass), H (frame), J (frame) are not suspended. The possible reason is that the RLS regions of springs and fingers are much bigger than frames and proof mass (Figure 2.14). Therefore, the oxide and silicon are etched

completely in the springs and fingers regions but are etched incompletely in the frame and proof mass regions. It makes the whole three-axis accelerometer not suspended and cannot move when acceleration is applied.

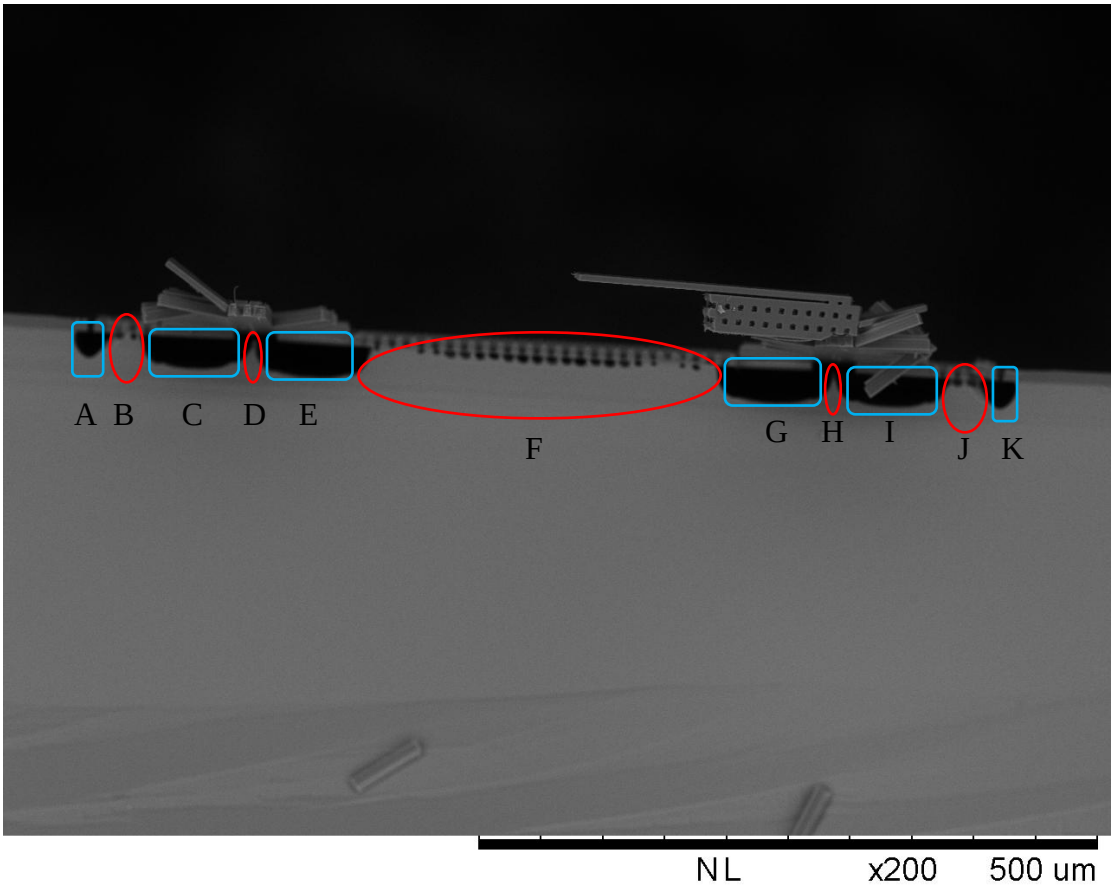


Figure 5.3: The cross-sectional view of the tree-axis accelerometer

Figure 5.4 shows the closer look of the proof mass region (region F in Figure 5.1). We can see that the oxide is etched incompletely in anisotropic oxide etching step. Therefore, the substrate (silicon) is etched unsuccessfully for sure in the isotropic silicon substrate etching step. In addition, from Figure 5.4, we can see that the degree of oxide etching is different with the same size of etching holes. This means in anisotropic oxide etching step, the concentration of the etching solution is not the

same in different regions of the three-axis accelerometer. This is another possible reason for the three-axis accelerometer is not suspended.

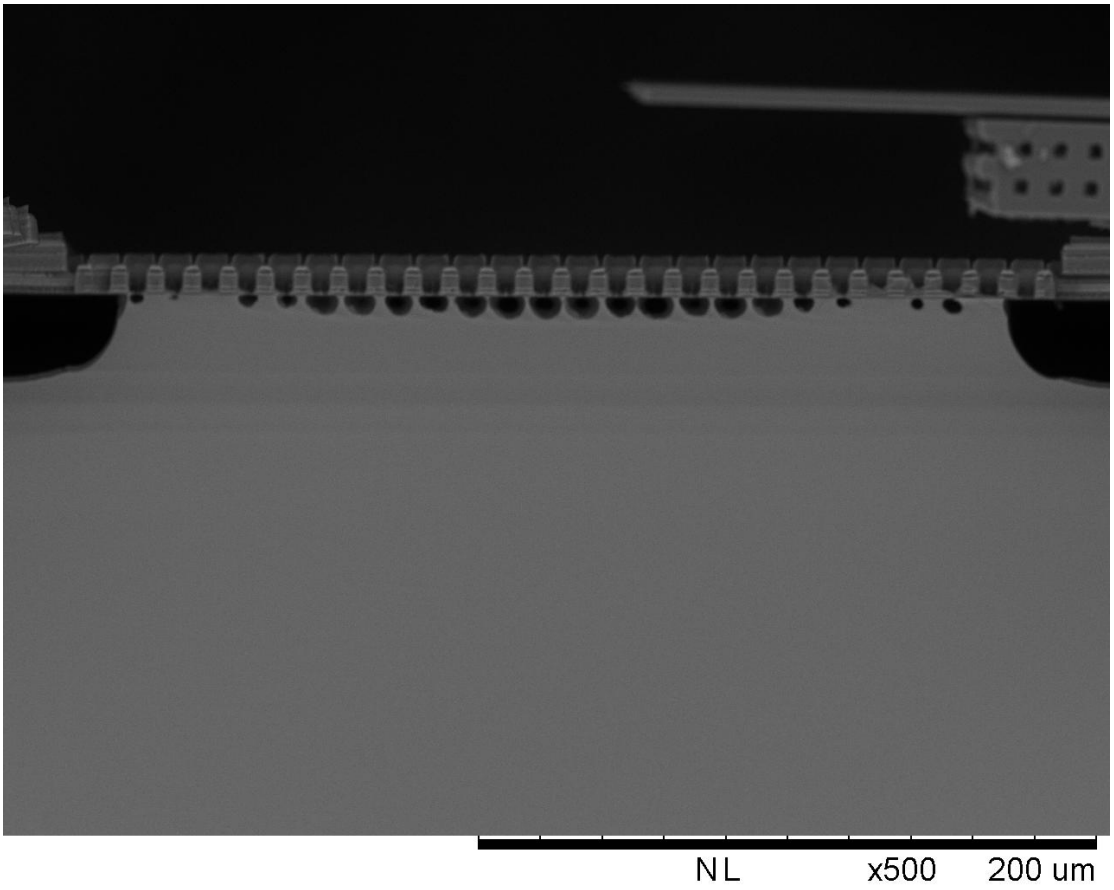


Figure 5.4: The closer look of Figure 5.3 in the proof mass region

We used white light interferometer to check the dies and Figure 5.5 shows the results of the three-axis accelerometer in the unpackaged dies. The line in the upper left corner of Figure 5.5 means the position where will show the surface profile in the upper right corner of Figure 5.5. The surface profile means the height of the surface. If the height of the surface is the same, in other words, the line in the surface profile is flat, this means the structure probably is not suspended. Otherwise, if the line in the surface profile is not flat, this means the structure is suspended and is curved by

thermal stress. According to the surface profile in Figure 5.5, we can see the line is rather straight. So the whole structure of the three-axis accelerometer is not suspended in the unpackaged dies.

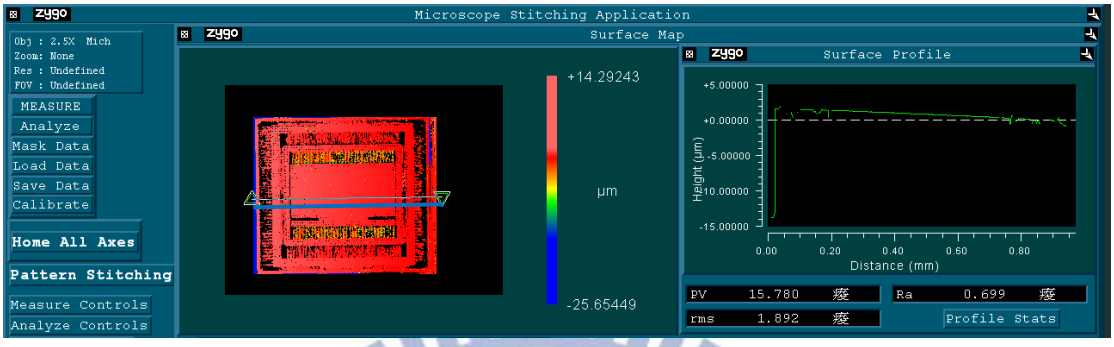


Figure 5.5: The result of the three-axis accelerometer in unpackaged die

Figure 5.6 shows the result of the three-axis accelerometer in the packaged die. According to the surface profile, we can see the edge of the three-axis accelerometer is suspended, but the region in the middle of the three-axis accelerometer (the proof mass region) is not. So the whole structure still cannot move while being applied acceleration.

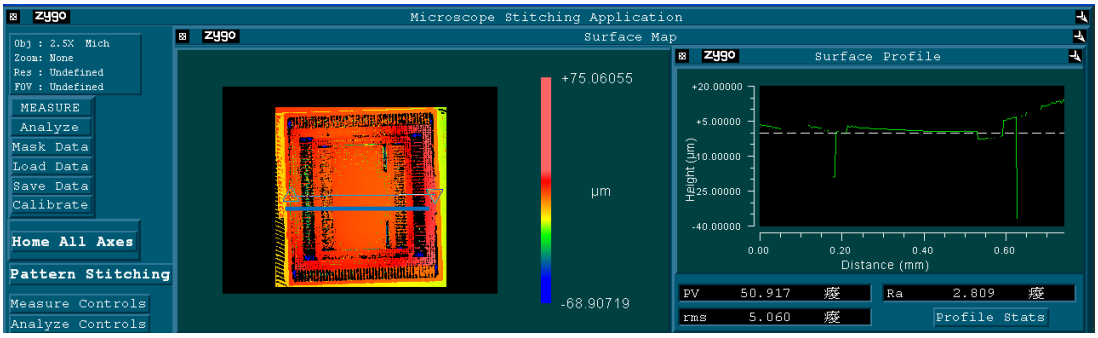


Figure 5.6: The result of the three-axis accelerometer in packaged die

From Figure 5.7, we can see the edge of the proof mass is suspended, but the area in

the middle of the proof mass is not. Figure 5.8 shows the surface profile of the Y axis frame. We can see the entire frame is suspended, because there is no flat part. Figure 5.9 shows the surface profile of X axis frame. Like Figure 5.8, the entire frame is suspended. According to Figure 5.6 ~ 5.9, the edge of the three-axis accelerometer is suspended successfully, but the middle of the three-axis accelerometer is not suspended. Therefore, the accelerometer cannot move when acceleration is applied. Therefore, we only can check the test readout circuit whether works functionally or not. The measurements of the test readout circuit will be shown in the next section.

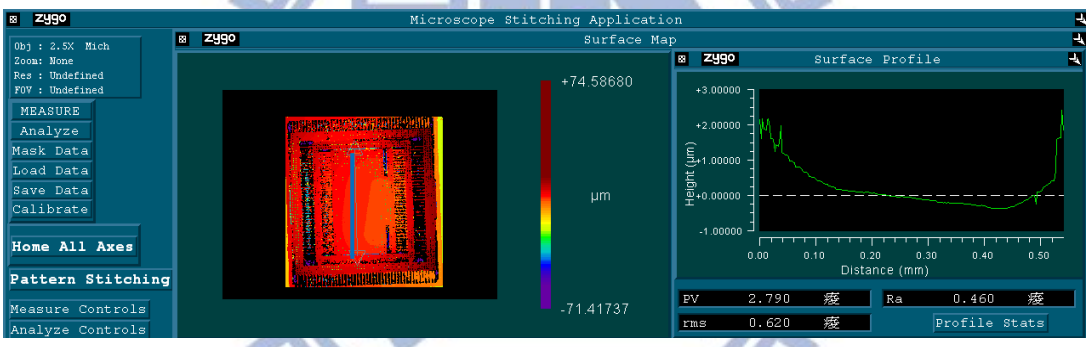


Figure 5.7: The result of the three-axis accelerometer in packaged die

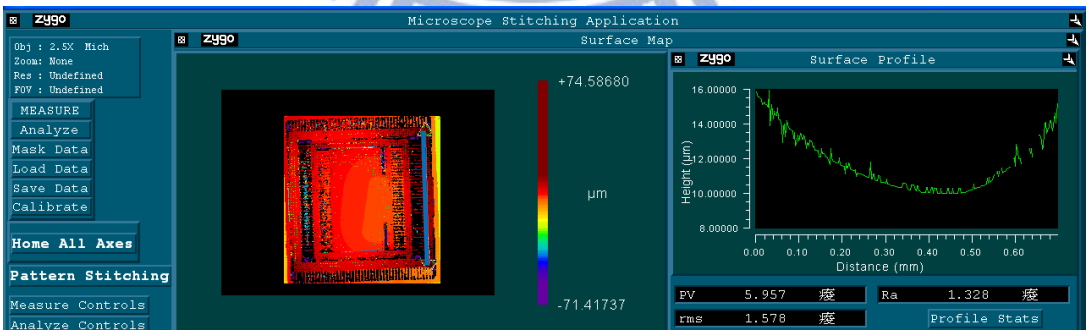


Figure 5.8: The result of the three-axis accelerometer in packaged die

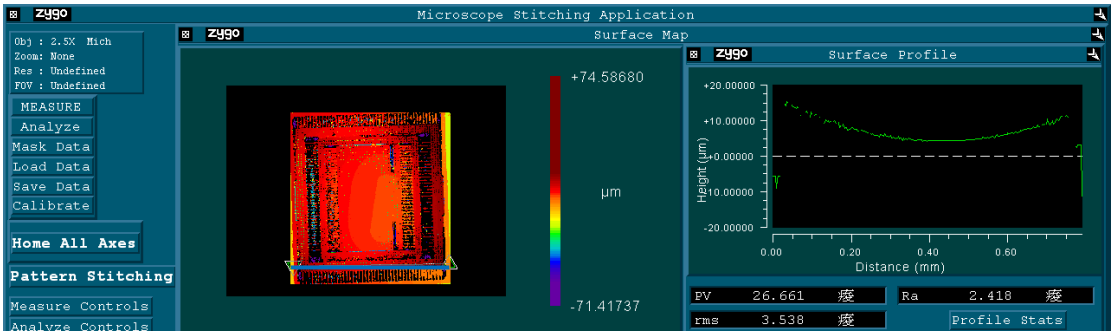


Figure 5.9: The result of the three-axis accelerometer in packaged die

5.3 The test readout circuit measurement

5.3.1 The test readout circuit measurement environment

Figure 5.10 shows the circuit measurement instruments and the instruments setup. The measurement instruments include the power supplies, function generator, oscilloscope, multimeter and RT_Pro spectrum analyzer. The two power supplies provide 1.8V to the VDD and 0.6V to the output CM dc bias voltage, respectively. The function generator provides the 10K Hz clock signal to the CDS and 100~400Hz sinewave input signal. The oscilloscope is used to observe the transient output waveform. The multimeter is used to measure the output dc voltage and the total current flowing through the VDD. The RT spectrum analyzer is used to measure the ac response like noise and so on.

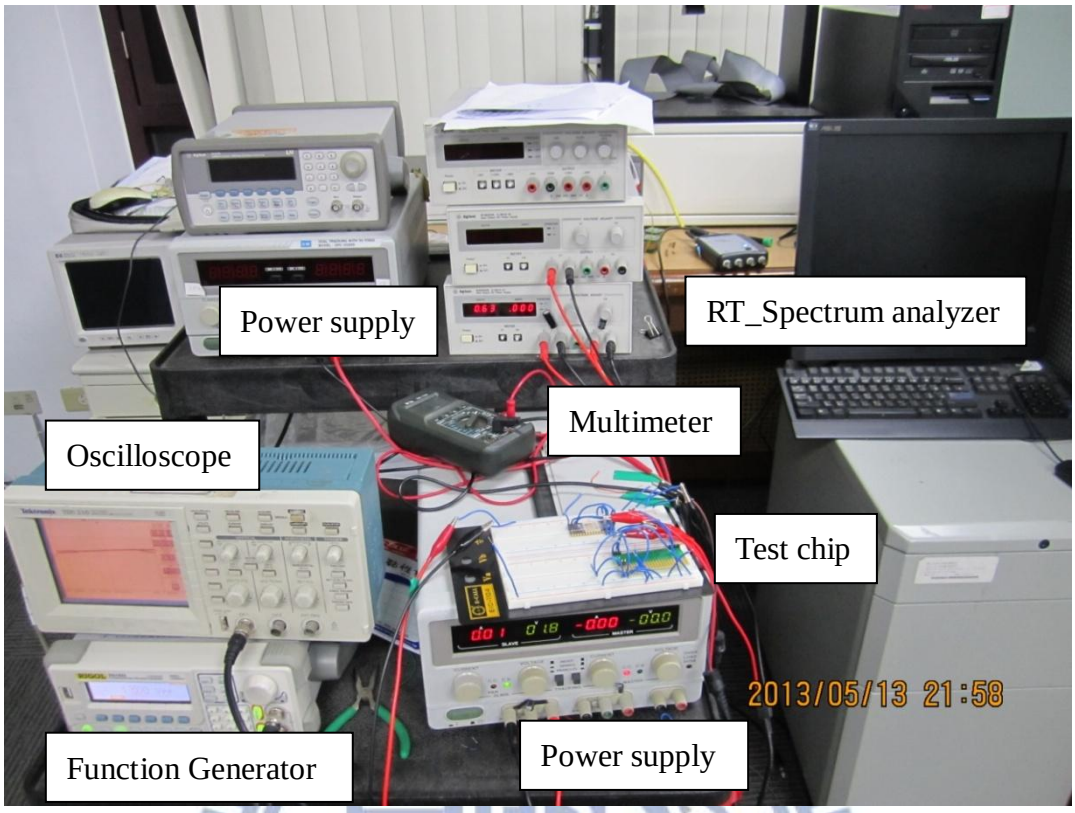


Figure 5.10: The circuit measurement instruments and setup

Figure 5.11 shows the test chip which is packaged (32 S/B) by CIC (Die in package (DIP)) and is placed in the PCB board for measurement. Due to the unsuspended three-axis accelerometer, the test chip can only do the electrical measurement but not able to do the mechanical measurement. The electrical measurement results are illustrated in the next section.

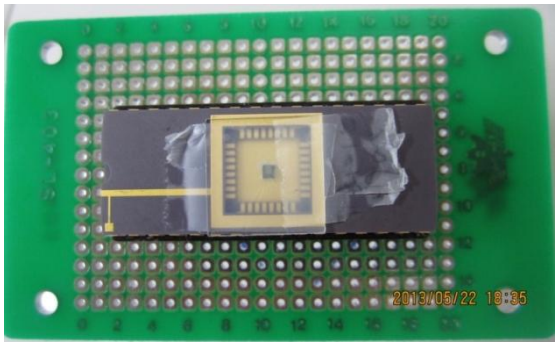


Figure 5.11: The test chip

5.3.2 The test readout circuit measurement results

Figure 5.12 shows the schematic of the test circuit. It is composed of three stages. The first stage is the CDS, the second stage is the integrator, and the third stage is the S&H. The values of the capacitances C1, C2, C3 are 600fF, and C4 is 3pF. The input sinewave is applied to Vin+, and Vout+ is connected to the oscilloscope and the RT_Spectrum analyzer.

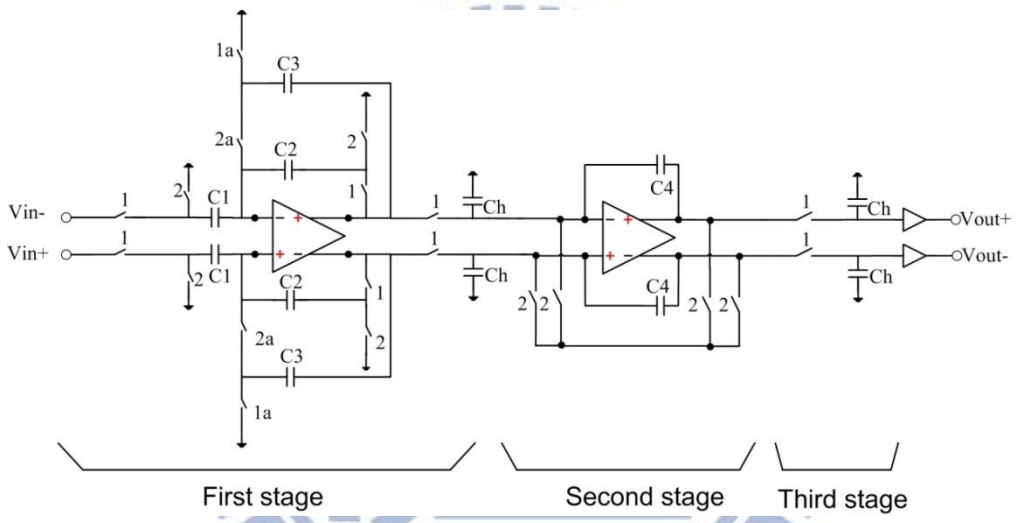
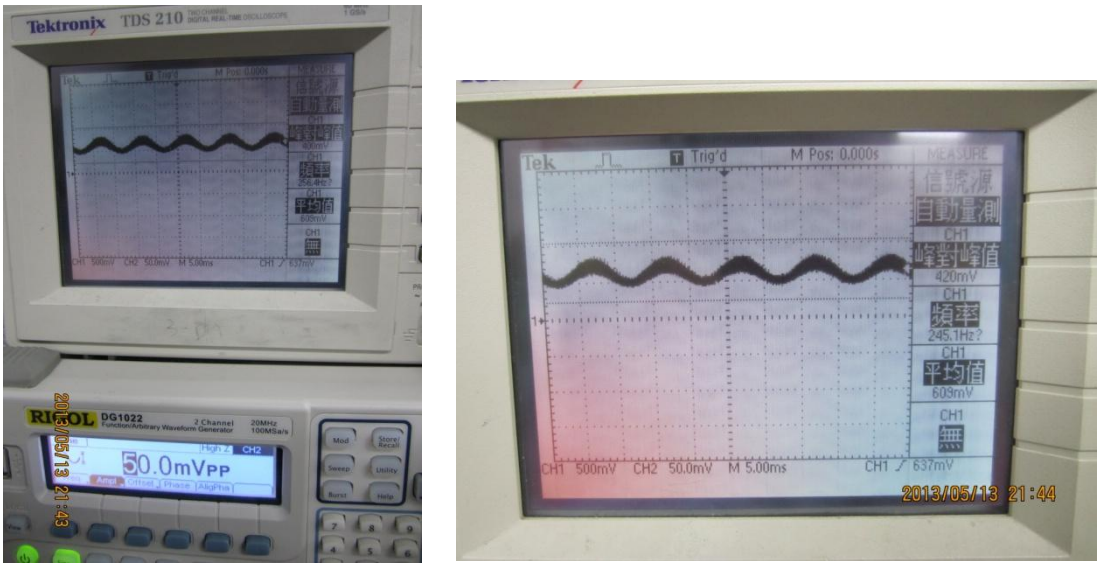


Figure 5.12: The schematic of the test circuit

In my design, the system bandwidth is 100Hz, and the sensitivity is 100mV/g, and the linear range is +/- 4g. Therefore, the max output amplitude is 400mV, or in other words, the Vpp (Vpeak to peak voltage) is 800mV. Figure 5.13 (a) shows the output waveform when the input signal is a 100Hz, 50mVpp sinewave. Figure 5.13 (b) shows the output amplitude is 420mVpp and the output dc voltage is 609mV.



(a) (b)

Figure 5.13 (a): 100Hz, 50mVpp input sinewave and output waveform; (b): Closer look of the output waveform in Figure 5.13 (a)

Figure 5.14 (a) shows the output waveform when the input signal is a 100Hz, 100mVpp sinewave. Figure 5.14 (b) shows the output amplitude is 600mVpp and the output dc voltage is 603mV. Figure 5.15 (a) (b) show the closer look of the output waveform. It is similar with the simulation results. The amplitude of the sharp corners in Figure 5.15 (b) is smaller than the simulation result because the capacitances of the oscilloscope are bigger than the loading capacitances when I simulated. Therefore, the high frequency signal is filtered out, making the amplitude of the sharp corners smaller.

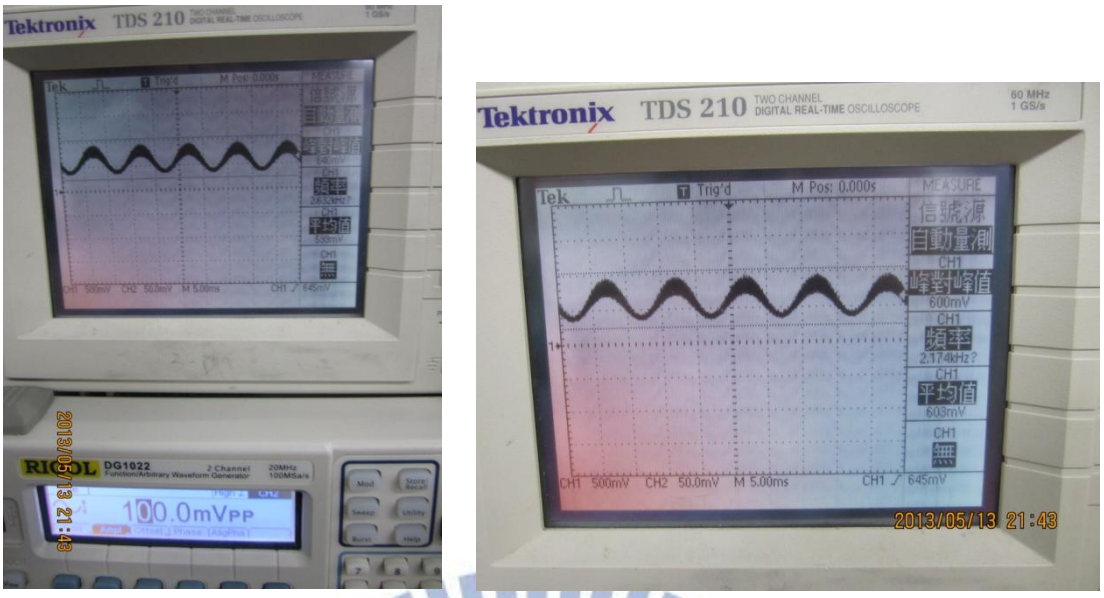
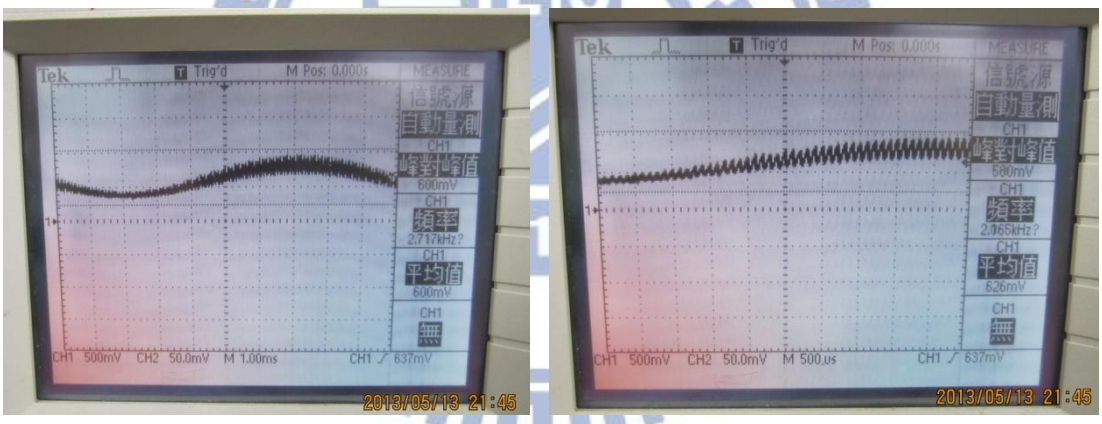


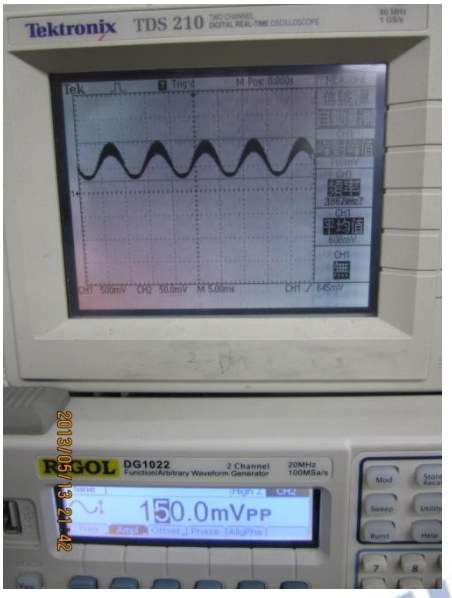
Figure 5.14 (a): 100Hz, 100mVpp input sinewave and output waveform; (b): Closer look of the output waveform in Figure 5.14 (a)



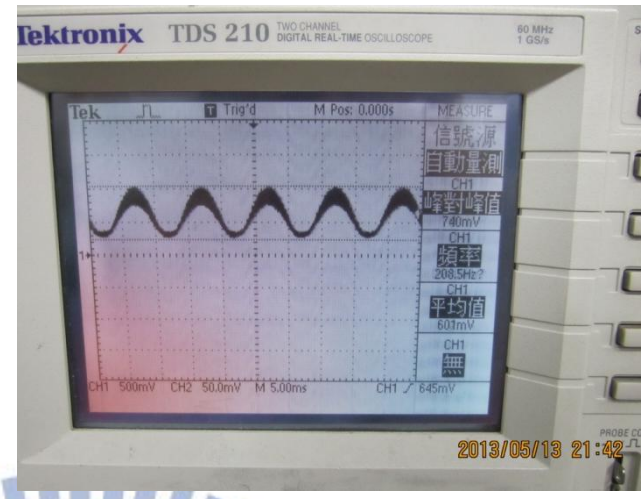
(a) (b)

Figure 5.15 (a): Closer look of Figure 5.16; (b): Closer look of Figure 5.17 (a)

Figure 5.16 (a) shows the output waveform when the input signal is a 100Hz, 150mVpp sinewave. Figure 5.16 (b) shows the output amplitude is 740mVpp and the output dc voltage is 601mV.

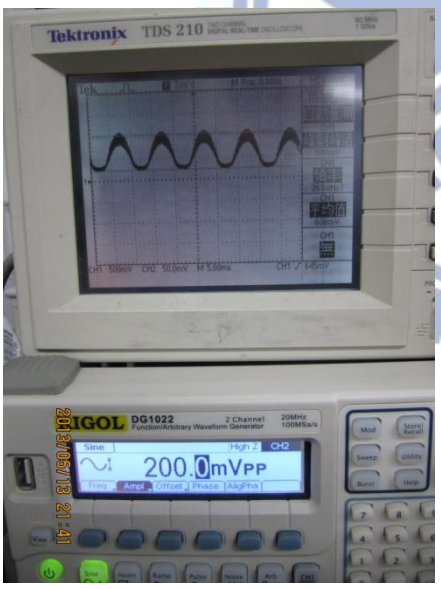


(a)

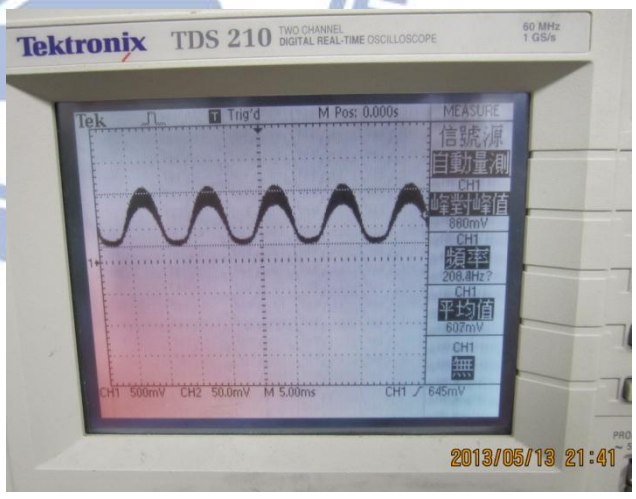


(b)

Figure 5.16 (a): 100Hz, 150mVpp input sinewave and output waveform; (b): Closer look of the output waveform in Figure 5.16 (a)



(a)



(b)

Figure 5.17 (a): 100Hz, 200mVpp input sinewave and output waveform; (b): Closer look of the output waveform in Figure 5.17 (a)

Figure 5.18 and Table 5.1 show the comparison of T18-101E between post-simulation

and measurement. The linearity of measurement becomes poor and the gain is smaller when the amplitude of input signal is higher.

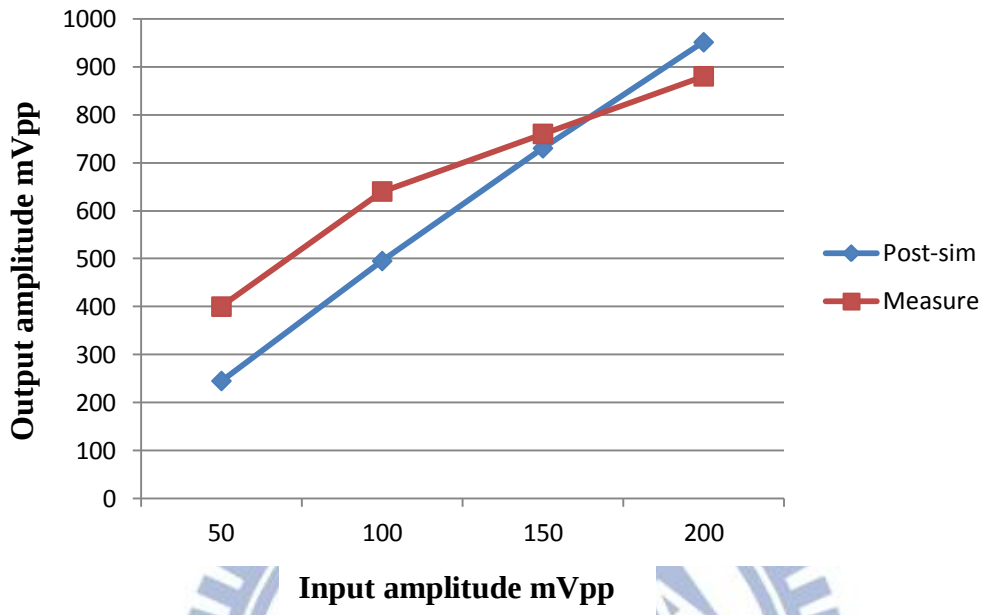


Figure 5.18: The comparison of T18-101E between simulation and measurement

Table 5.1: The comparison of the output amplitude between simulation and measurement

Input amplitude	Post-sim output amplitude	Measurement output amplitude
50 mV	245 mV	400 mV
100 mV	495 mV	640 mV
150 mV	730 mV	760 mV
200 mV	951 mV	880 mV

Next, the measurement results of the readout circuit noise will be shown as below. Figure 5.19 shows the ac response and the FFT (Fast Fourier Transform) of the sinewave which is generated by function generator. The noise floor of the function generator is -56dB mV, which is 1.8uV/√Hz. In other words, the output noise which is contributed by function generator is 1.8uV/√Hz. Figure 5.20 shows the ac response and the FFT of the readout circuit output when the input is a 100Hz, 50mVpp sinewave. The noise floor is -30dB mV, which is 30uV/√Hz. Dividing by gain, and subtracts the noise generated by the function generator, the input referred noise can be calculated as 1.61uV/√Hz. In addition, because the output waveform of the readout circuit is not a pure sinewave (Figure 5.15 (b)), the amplitude of the harmonic is big. Also we can calculate the SNR (Signal to Noise Ratio) is 69dB.

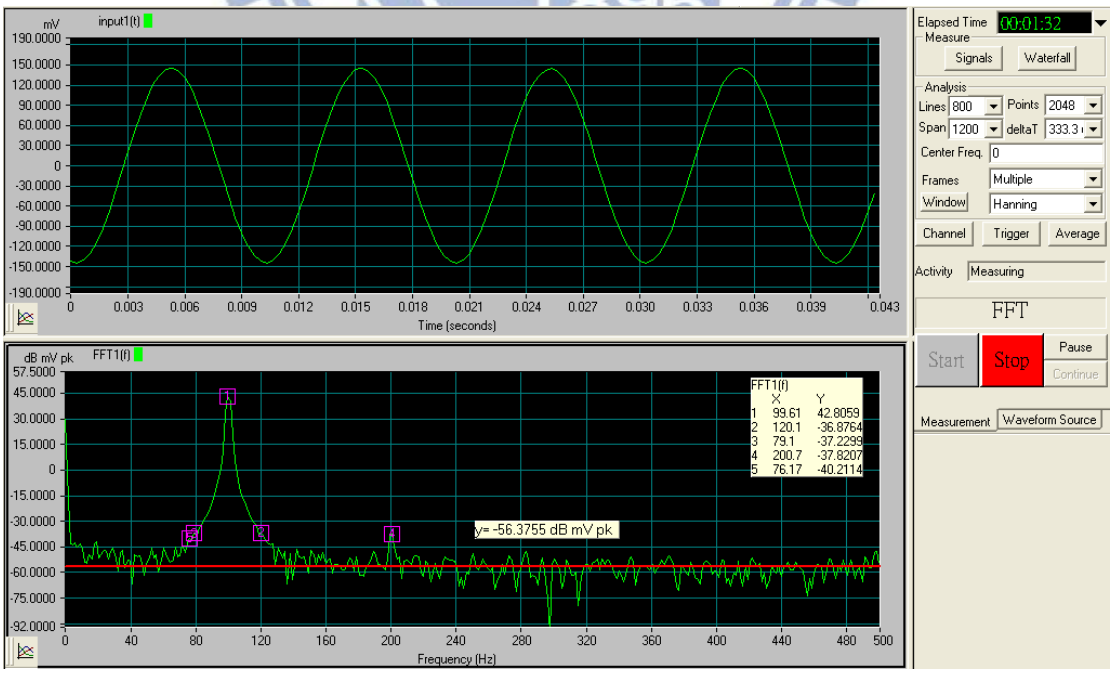


Figure 5.19: The ac response and the FFT of the function generator

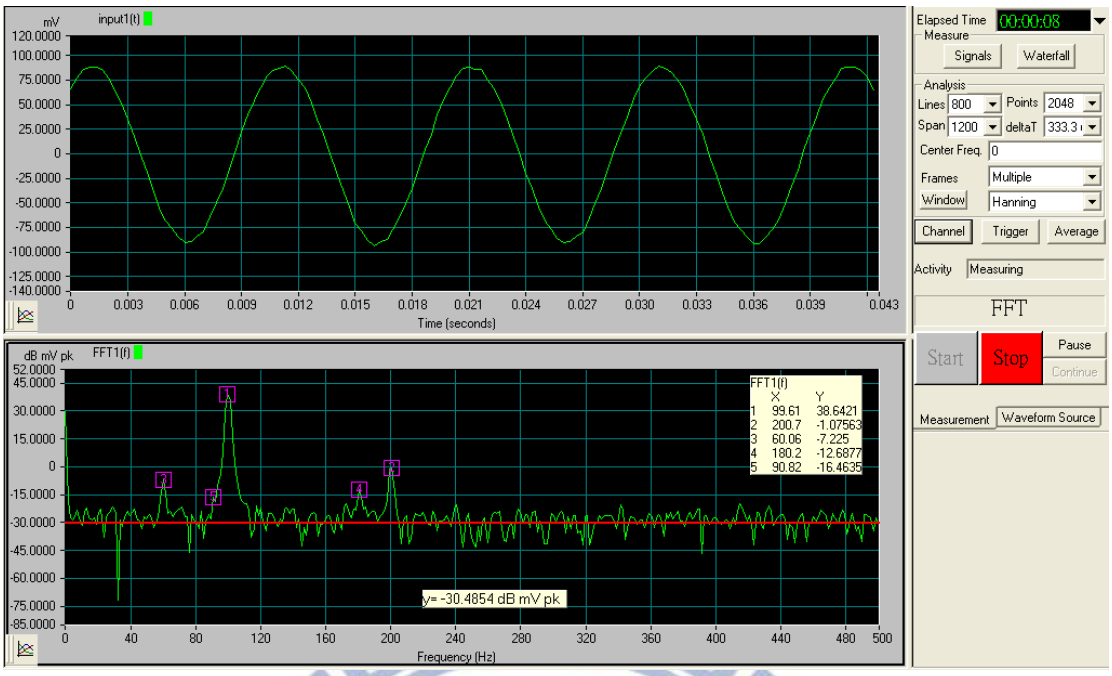


Figure 5.20: The ac response and the FFT of the readout circuit output when the input signal is 100Hz, 50mVpp

Figure 5.21 ~ 5.23 shows the ac response and the FFT of the readout circuit output when the amplitude of the input signal are 100mVpp, 150mVpp and 200mVpp, respectively. And the readout circuit measurement results of the noise floor and SNR are illustrated in Table 5.2.

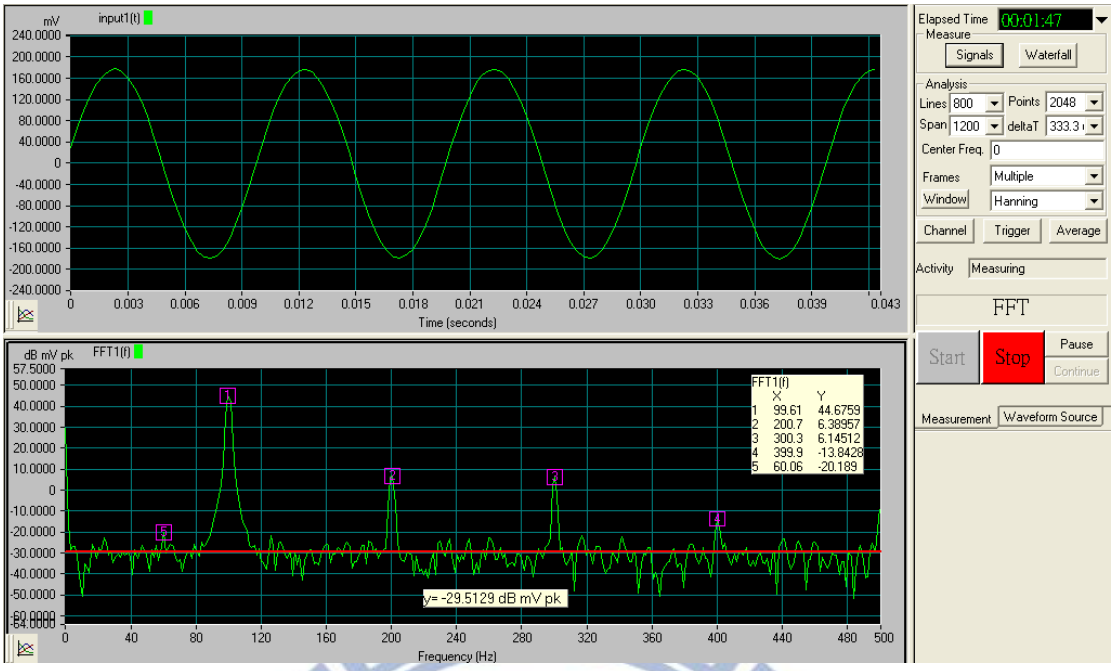


Figure 5.21: The ac response and the FFT of the readout circuit output when the input signal is 100Hz, 100 mVpp

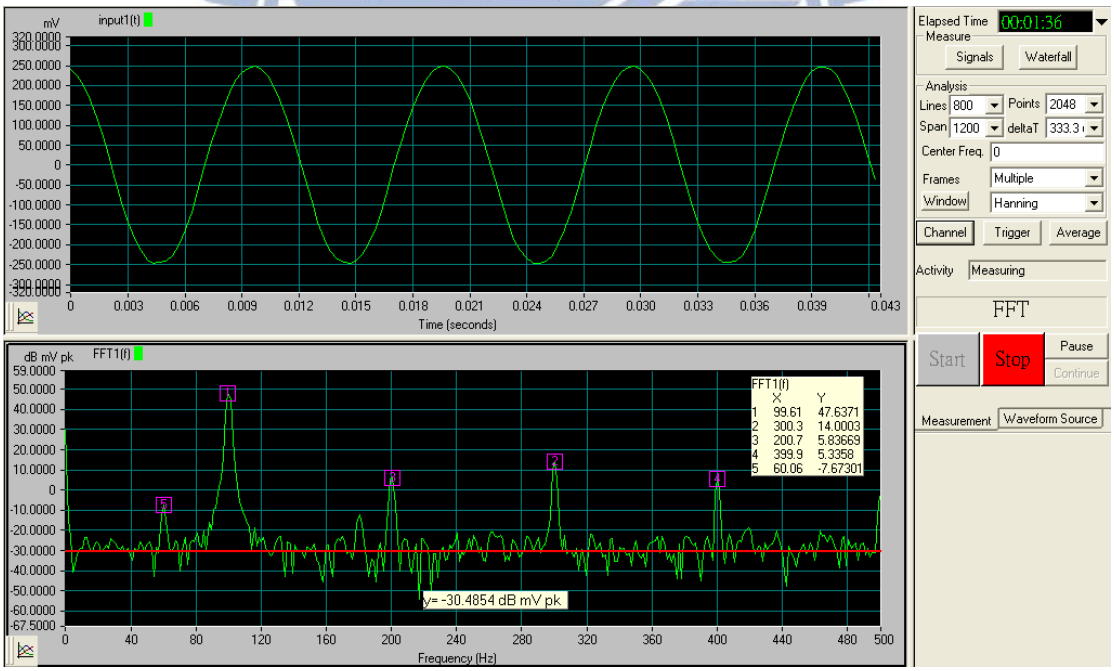


Figure 5.22: The ac response and the FFT of the readout circuit output when the input signal is 100Hz, 150 mVpp

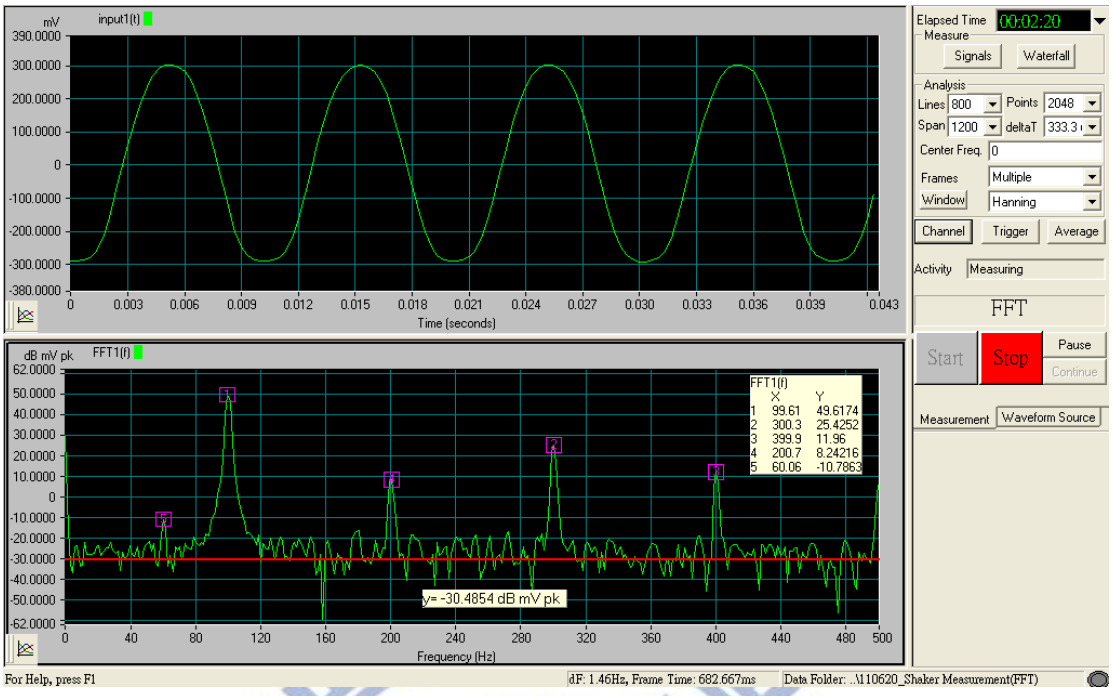


Figure 5.23: The ac response and the FFT of the readout circuit output when the input signal is 100Hz, 200 mVpp

Table 5.2: The noise floor and SNR of the readout circuit

Input amplitude	50mVpp	100mVpp	150mVpp	200mVpp
Noise floor	-30.5dB mV	-29.5 dB mV	-30.5 dB mV	-30.5 dB mV
SNR	69 dB	74 dB	77.6 dB	79.6 dB

Figure 5.24 ~ 5.26 show the ac response and the FFT of the readout circuit output when the frequency of the input signal are 200Hz, 300Hz, 400Hz, respectively. We can see the fundamental frequency is followed by the input frequency change. The ac

response and the noise floor are similar when input signal is 100Hz.

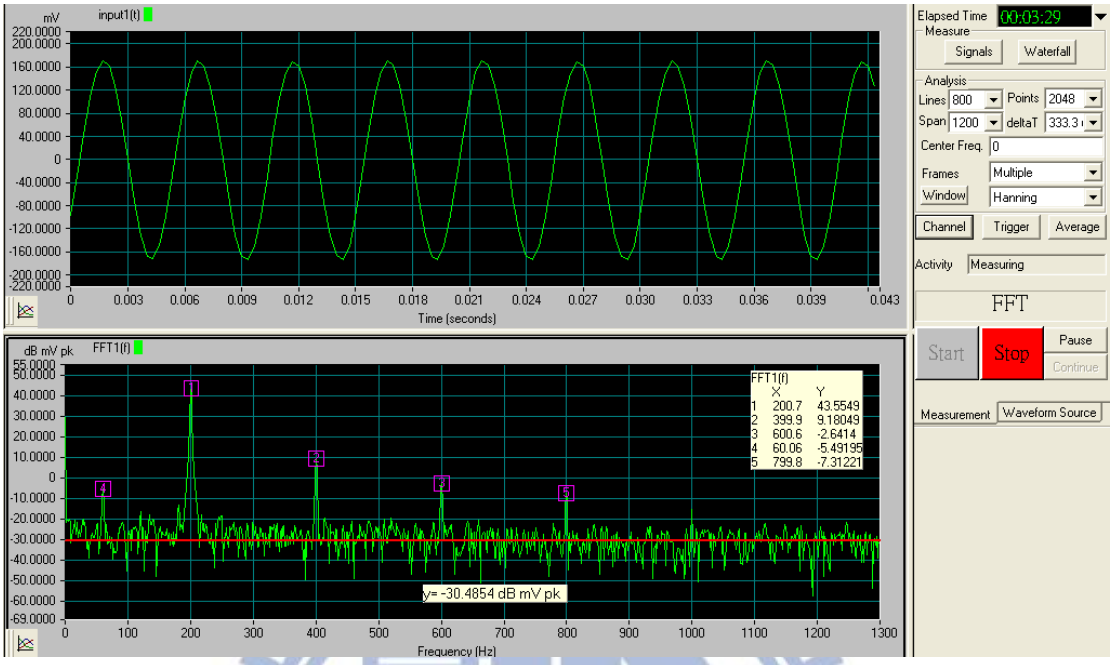


Figure 5.24: The ac response and the FFT of the readout circuit output when the input signal is 200Hz, 100 mVpp

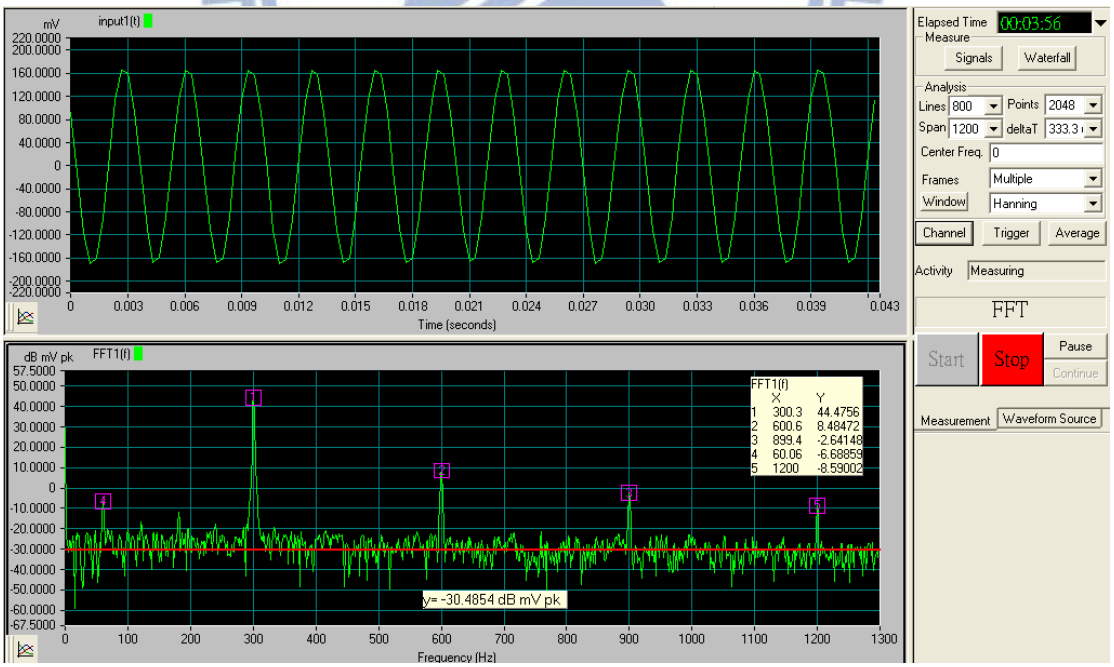


Figure 5.25: The ac response and the FFT of the readout circuit output when the input signal is 300Hz, 100 mVpp

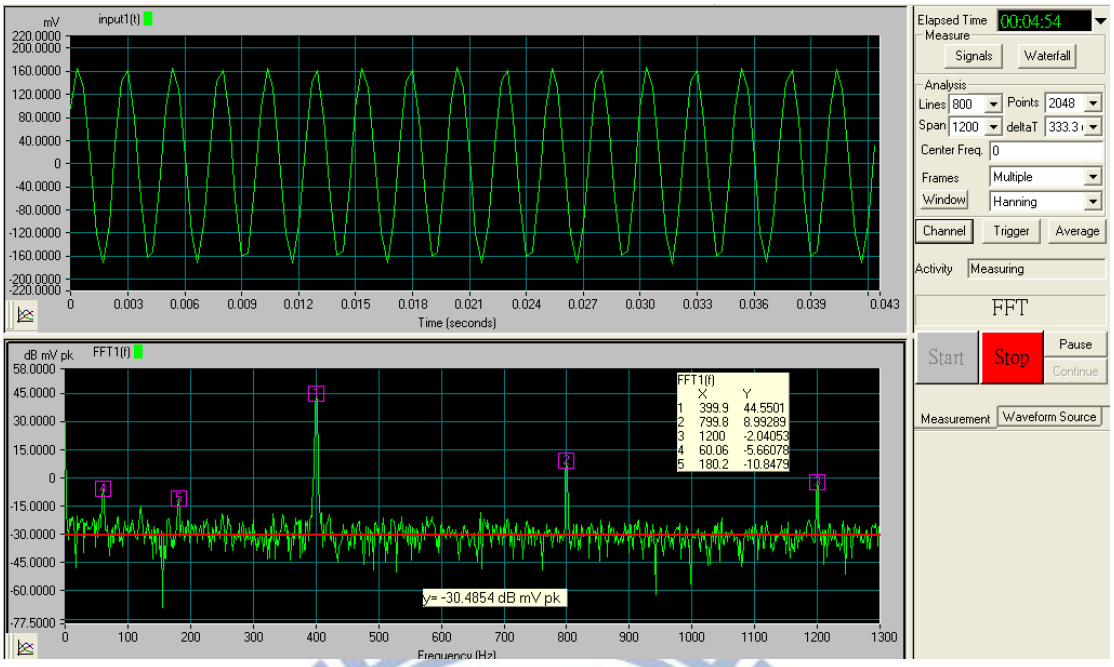


Figure 5.26: The ac response and the FFT of the readout circuit output when the input signal is 400Hz, 100 mVpp

After that, the power consumption of the readout circuit is also measured. By using multimeter to measure the current flowing through the VDD, the current is 0.23mA. Multiplying by the VDD voltage 1.8V, the power consumption of the readout circuit can be calculated as 414μW. The power consumption of the test readout circuit simulated in Cadence is 16μW. The comparison of the input referred noise and the power consumption between simulation and measurement results are shown in Table 5.3.

Table5.3: The comparison of the input referred noise and the power consumption between simulation and measurement results

	Post-sim	Measurement	Degradation
Input referred noise	169 nV/√Hz	1.61 uV/√Hz	9.5
Power consumption	118 μW	414 μW	3.5

5.4 The three-axis accelerometer and circuit remeasurement

The CIC remake the three-axis accelerometer and readout circuit for me and the accelerometer is suspended successfully this time. By using the SEM to observed the accelerometer (Figure 5.27, Figure 5.28), we can find the fingers having some offset shown as Figure 5.29.

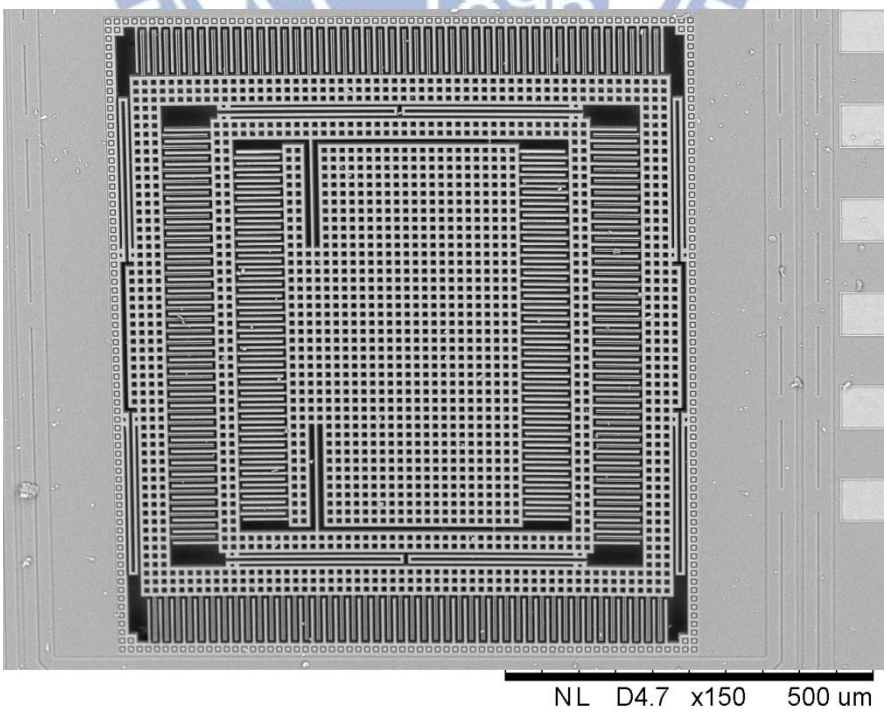


Figure 5.27: The SEM photo of the three-axis accelerometer

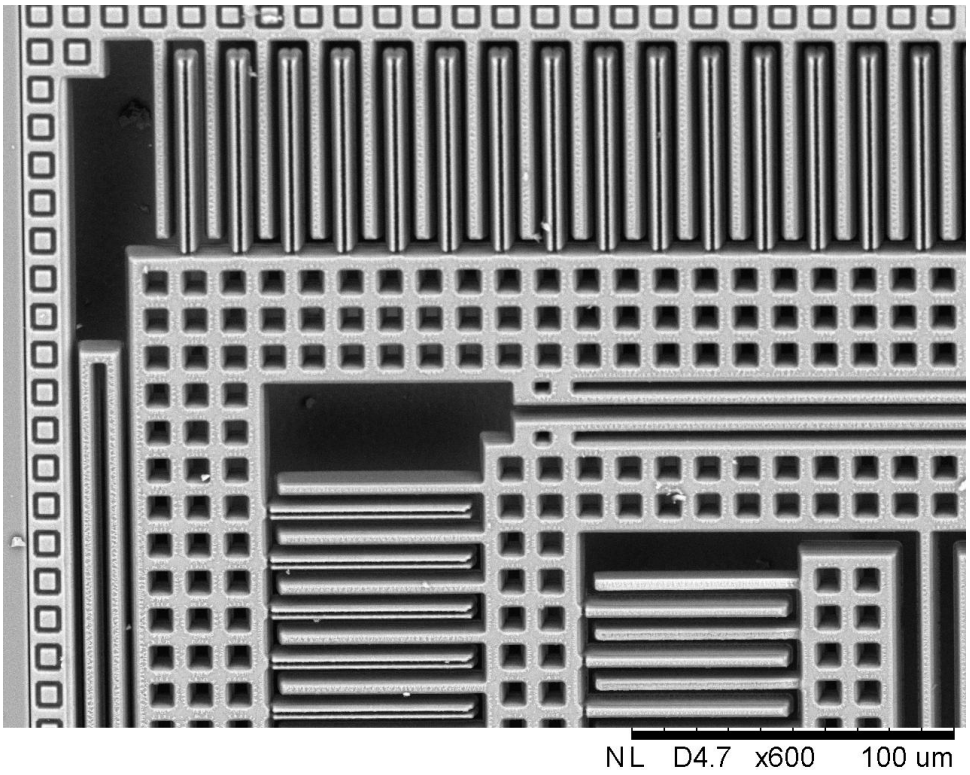


Figure 5.28: The SEM photo of the three-axis accelerometer

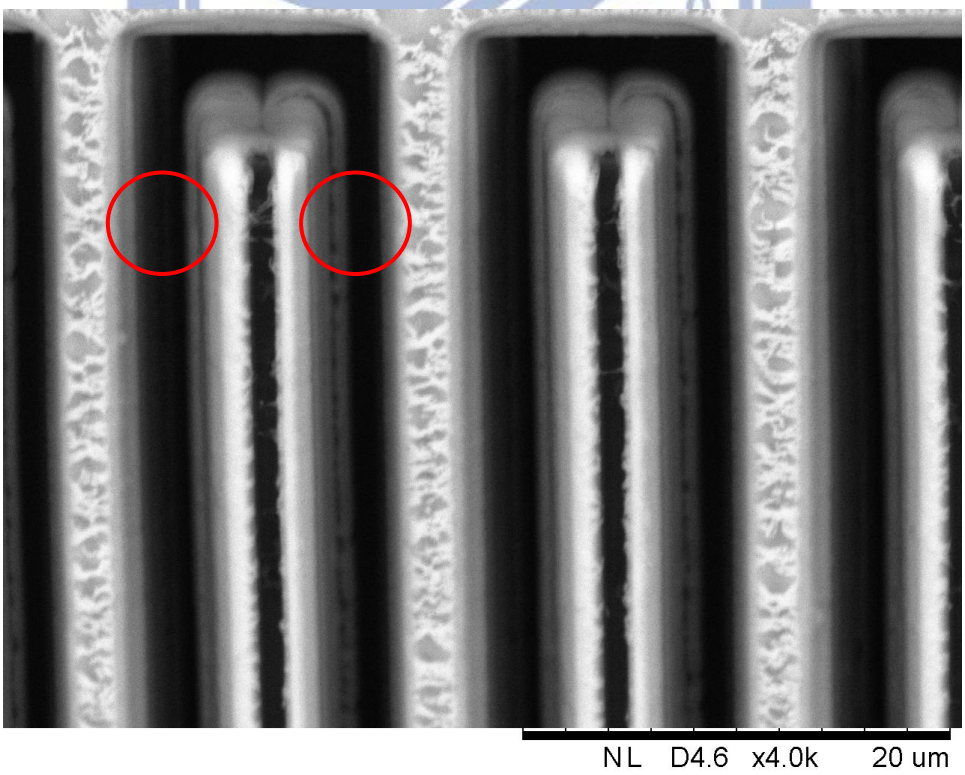


Figure 5.29: The SEM photo of the three-axis accelerometer fingers

By using MEMS motion analyzer (MMA) to measure the resonant frequency, we can obtain the three-axis accelerometer resonant frequency is 15k Hz shown in Figure 5.30.

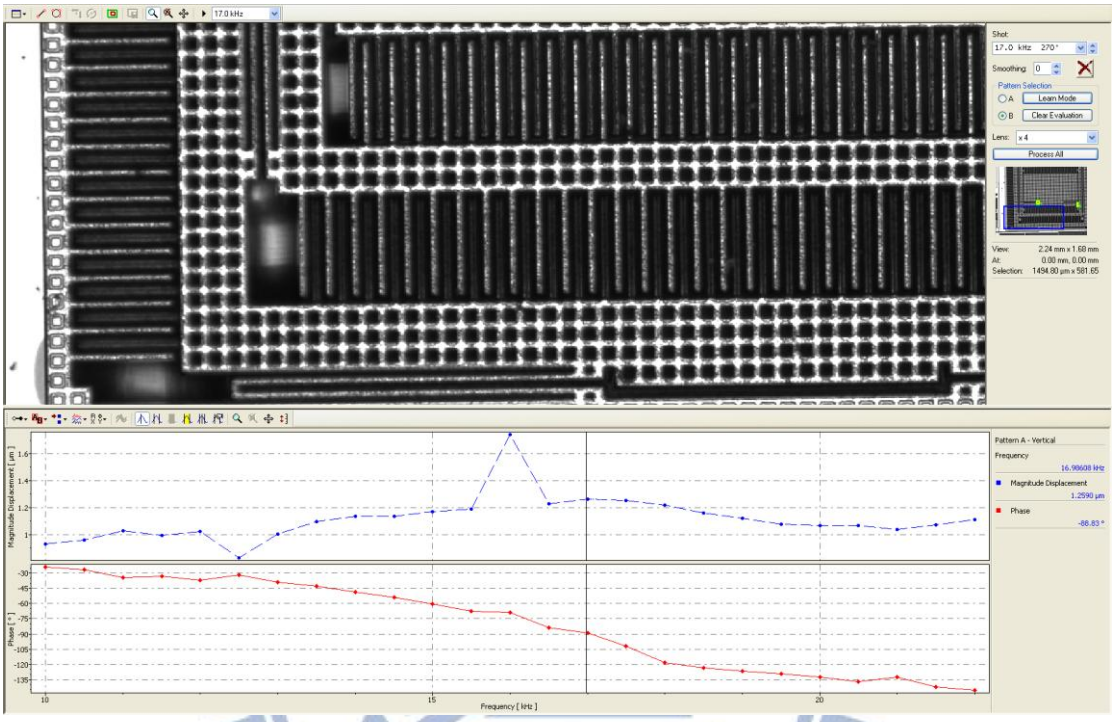


Figure 5.30: The resonant frequency of the three-axis accelerometer

However, this resonant frequency value is much higher than the simulation in Coventorware (4k Hz). Probably because the material parameters are not very accurate, and we used only one layer material to simulate, therefore, the simulated and measured resonant frequencies have a large difference. This means the spring is much harder, the accelerometer almost cannot move when applying acceleration (1g~9g). We measured the mismatch of the fingers and the measured result is shown as Figure 5.30.

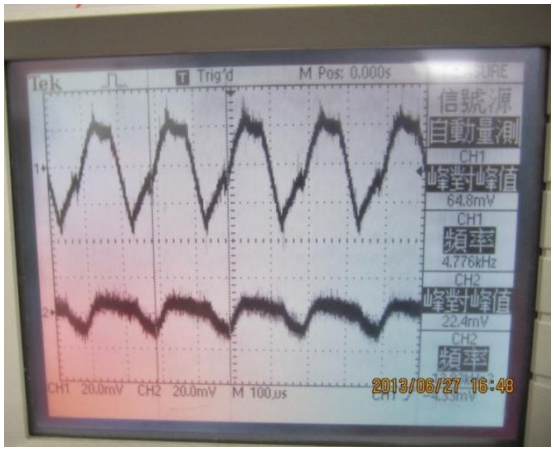


Figure 5.31: The measured result of the three-axis accelerometer

By using RT_Pro spectrum analyzer, we can measure the small output signal changes.

Figure 5.32 ~ Figure 5.36 show the FFT of the readout circuit output applying 100Hz , 1g ~ 3g acceleration. We can calculate the SNR, and it shows in Table 5.4.

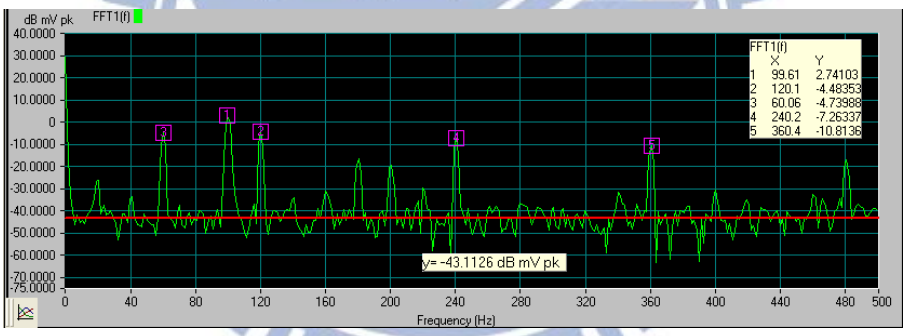


Figure 5.32: The FFT of the readout circuit output applying 100Hz, 1g acceleration

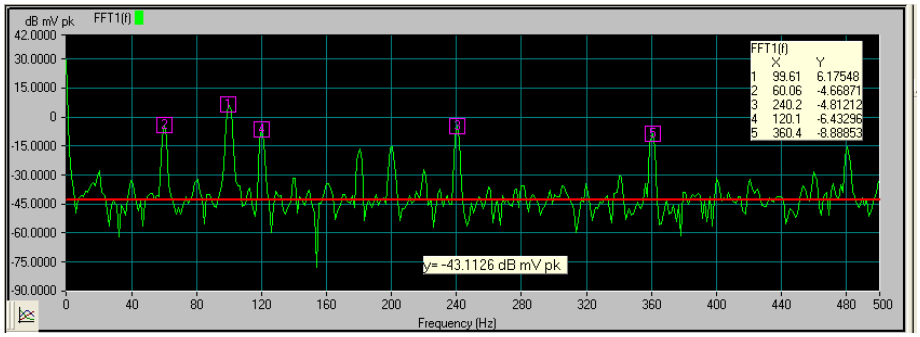


Figure 5.33: The FFT of the readout circuit output applying 100Hz, 1.5g acceleration

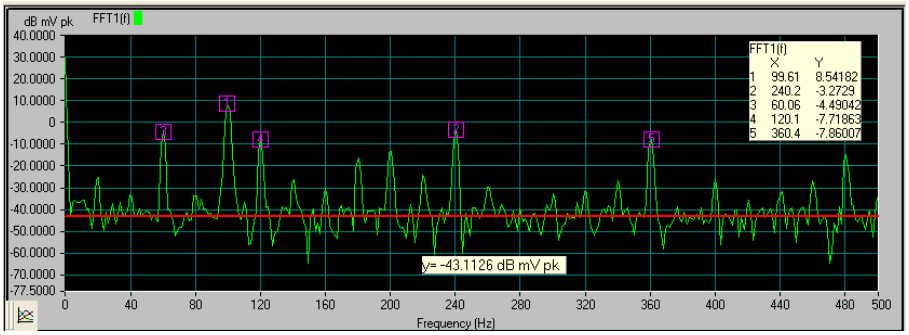


Figure 5.34: The FFT of the readout circuit output applying 100Hz, 2g acceleration

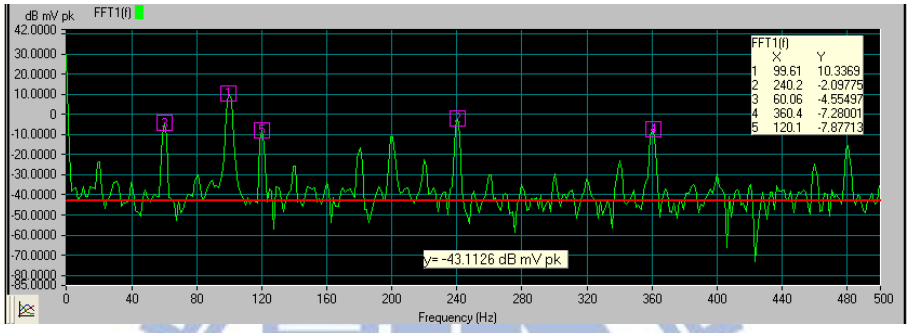


Figure 5.35: The FFT of the readout circuit output applying 100Hz, 2.5g acceleration

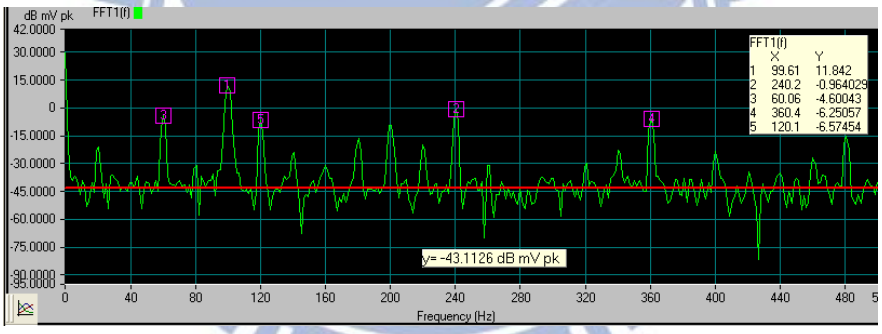


Figure 5.36: The FFT of the readout circuit output applying 100Hz, 3g acceleration

Table 5.4: The SNR of the readout circuit

Input acceleration	1g	1.5g	2g	2.5g	3g
SNR	45.8 dB	49.2 dB	51.6 dB	53.4 dB	54.9 dB

Chapter 6 Conclusions and Future Work

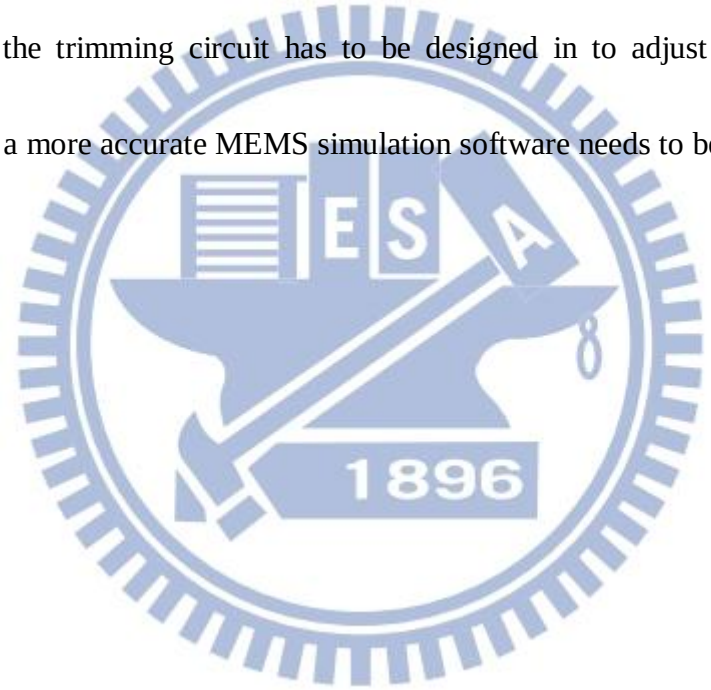
6.1 Conclusions

A monolithic three-axis accelerometer with tunable gain analog front end circuit using time division to read multi-sensors signals has been demonstrated in this work. Due to monolithic CMOS process of MEMS and ASIC being available, it is possible to integrate more sensors on the same substrate. This work has a single readout circuit and tunable gain stage for multiple sensors with different scales of sensitivity levels. It will be possible to make the sensor integration being more compact for low power consumption and small area applications.

In the first tape out, the three-axis accelerometer is integrated with the readout interface on a single chip in standard CMOS process. However, due to the unstable CMOS MEMS post process, the three-axis accelerometer cannot be suspended completely. This causes the sensitivity (acceleration to voltage) cannot be measured. Because an additive test readout circuit is designed in, we can measure the readout circuit and test the functionality when the accelerometer is failed. According to the readout circuit measurement results, the function works correctly. The measured input referred noise is 1.61 uV/√Hz, the SNR is 79.6 dB and the power consumption is 414μW.

6.2 Future Work

In this work, the control signals EN and ON1 ~ ON4 (shown in Figure 3.2) are all digital signals. Therefore, it provides an easy interface for future integration with MCU (Micro programmed Control Unit). In addition, the readout circuit output waveform (shown in Figure 3.41) also provides a chance for future integration with ADC (Analog to Digital Convertor). Moreover, due to the unstable CMOS MEMS post process, the trimming circuit has to be designed in to adjust the capacitance mismatch and a more accurate MEMS simulation software needs to be applied.



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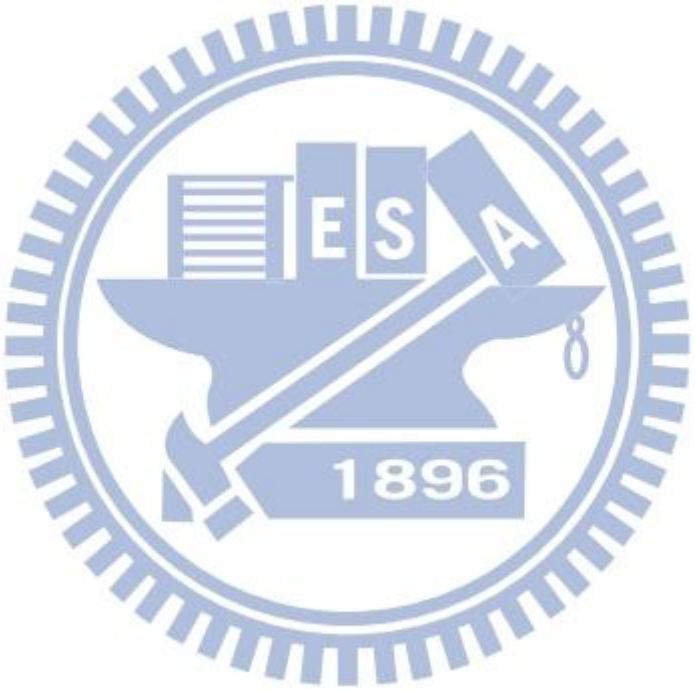

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英文論文題目：
Design of Three-axis Accelerometer with Tunable Gain Interface for Multi-sensors

中文論文題目：
多重感測器讀取之可調式增益介面電路三軸加速度計單晶設計