國立交通大學

電子工程學系 電子研究所

博士論文

具有源極汲極應變矽鍺與嵌入式矽鍺通道之28奈米和下世代P型金氧半場效電晶體特性之研究

Study on the Electrical Characteristics of the PMOSFETs with the Strained SiGe S/D and Embedded SiGe Channel for the 28 nm Node and Beyond

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中華民國一0二年六月

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研究生：游明華　　Student：Ming-Hua Yu

指導教授：鄭晃忠 博士　　Advisor：Dr. Huang-Chung Cheng

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摘要

在此論文中，分別針對應變源極汲極矽鍺與嵌入式矽鍺通道等二項工程提出不同結構與技術改善以提昇 28 奈米 P 型電晶體元件特性。針對應變源極汲極矽鍺，我們探討製程參數所造成的鬆弛性矽鍺對 P 型電晶體元件特性之通道應力衰減與矽基材缺陷形成的影響。針對嵌入式矽鍺通道，我們提出一種新穎製程方式可製作具高載子移動率，不須矽表面覆蓋卻有著較佳的閘極氧化層完整性(Gate Oxide Integrity, GOI)，來應用於 28 奈米電晶體元件特性之改善。

首先，針對源極汲極的矽鍺電晶體，對於製程流程上的離子佈值與毫秒式退火造成應變矽鍺的部份鬆弛性，所造成的通道應力衰減與缺陷形成於底下矽基材內而造成大量漏電，同時也造成晶片的大量彎曲變形有礙於黃光曝光的製程之 28 奈米 P 型電晶體元件特性。低能量砷離子佈值僅造成 11% 應變矽鍺的部份鬆弛性，在後續的毫秒式退火下 並不會造成缺陷形成於矽基材上而造成大量漏電，同時也不會造成晶片的大量彎曲變形。然而中能量砷離子佈值僅造成 51% 應變矽鍺的部份鬆弛性，在後續的毫秒式退火下，會造成缺陷形成於矽基材上而造成 100 倍大量漏電，同時也造成晶片的大量彎曲變形從壓應變到拉伸應變。藉由離子佈值種類的改變由砷變成磷離子和砷離子佈值的順序變化可以得到機乎完全應變無鬆弛的矽鍺而有 10% 趨動電流的改善。進一步高能量砷離子佈值造成 75% 應變矽鍺的大部份鬆弛性，在後續的毫秒式退火下，又不會造成缺

陷形成於矽基材上，同時也不會造成晶片的大量彎曲變。此一現象了解與探討，有助於28 奈米 P 型電晶體元件特性的改善。

針對應變矽鍺的鍺含量與後續退火條件來探討其所成應變矽鍺的部份鬆弛性，在後續的毫秒式退火下，是否也會造成缺陷形成於矽基材上以及晶片的大量彎曲變形。經由實驗得知 27%的鍺含量和 600 秒 800 度都會造成應變矽鍺的中等部份弛性，在後續的毫秒式退火下，也會造成缺陷形成於矽基材上與晶片的大量彎曲變形。因此不管是用離子佈值或長時間退火亦或應變矽鍺的鍺含量高低所造成應變矽鍺的中等部份鬆弛性，都會造成缺陷形成於矽基材上與晶片的大量彎曲變形從壓應變到拉伸應變，因此好的矽鍺後製程設計，對 28 奈米電晶體元量產顯得重要。另外，了解矽鍺與毫秒式退火造成缺陷現象是否與矽鍺面積圖案有關而顯得格外重要。由實驗得知矽鍺佔種面積 10%以上時會有嚴重的晶片彎曲變形，當矽鍺區域面積大於 0.2 毫米平方時，即時矽鍺佔種面積 10%以下時，也會有缺陷形成於矽基材內且有大量漏電。所以一個良好的矽鍺面積設計對 28 奈米電晶體元量產顯得格外重要。

其次，針對通道工程的改善，我們提出一種新穎製程方式可製作具高載子移動率的嵌入式矽鍺通道，不須矽表面覆蓋卻有著較佳的閘極氧化層完整性(Gate Oxide Integrity, GOI)，來應用於 28 奈米電晶體元件特性之改善。藉由源極汲極凹槽蝕刻時，緊接著額外的氣體蝕刻將(110)晶格面移除而停在(111)晶格面，並將源極與汲極打通而形成懸空的閘極與氧化層。由於此蝕刻氣體並不會與氧化層反應，所以可以再利用矽鍺沉積得到矽鍺通道。如此的結構可以得到較佳的載子移動率約 26%電導通率增益(Gm)與 8% Ion_Ioff 增益特性改善。同時閘極氧化層並不會被破壞且矽鍺不會與閘極氧化層反應而形成鍺氧化層，所以可以得到與矽氧化層相同的完整性與低漏電，如此一個新穎的結構可用於 28 奈米電晶體以及更進階的三維電晶體元件特性之改善

最後，本論文所提之應變源極汲極矽鍺與嵌入式矽鍺通道等二項工程改善不僅在 28 奈米電晶體展現優越的特性及其在下世代也極具潛力。

Study on the Electrical Characteristics of the PMOSFETs with the Strained SiGe S/D and Embedded SiGe Channel for the 28 nm Node and Beyond

Student : Ming-Hua Yu Advisor : Dr. Huang-Chung Cheng

Department of Electronics Engineering &
Institute of Electronics
National Chiao Tung University

ABSTRACT

In this thesis, the strained SiGe source/drain (S/D) and the epitaxial SiGe channel of the PMOSFETs with the technique improvement and novel structures have been systematically investigating to boost device performance for the 28 nm node and beyond. For the former one, the impacts of the process parameters on the relaxation of the strained-SiGe induced channel stress degradation and defect formation in the under-layered Si substrate are discussed. For the later one, a novel technique to create the suspending stacked gate and subsequently to fill in an embedded SiGe channel (ESC) between the gate oxide and under-layered Si substrate has been proposed for the first time to enhance the drive current gain of the 28 nm PMOSFETs.

At first, for the source/drain engineering of the epitaxial strained SiGe, the degree of strained-SiGe relaxation caused by implantation significantly affected the channel stress and the formation of defects in the underlying Si substrate as well as wafer bending when the millisecond anneal (MSA) was applied to the S/D strained-SiGe in 28nm PMOSFET devices for resistance reduction. Proper implantation species selection from Arsenic (As) to Phosphorus (P) was chosen to provide a relaxation-less strained-SiGe and enhanced the channel stress. It could achieve a 10% higher current gain. The defect-free underlying Si in the millisecond-annealed 28 nm PMOSFETs devices exhibits a decrease in the junction leakage current by four orders of magnitude. A new approach to modify the implantation conditions was also developed to achieve a relaxation-less strained-SiGe layer and defect-free underlying Si substrate for the 28nm PMOSFETs.

For the process parameter effects on the strained-SiGe relaxation, the formation of the induced defects in the underlying Si substrate associated with the interaction of the partly relaxed strained-SiGe layer and subsequent millisecond annealing (MSA) has been explored. Three kinds of methods including the post-SiGe implant, post-SiGe soak anneal and in-situ Ge at.% effect that were used to boost the device performance were investigated how to avoid the strained-SiGe relaxation and defect formation in the underlying Si during the MSA. All of them revealed the same phenomena that the medium relaxation of the strained SiGe either by the post-implant, post-soak anneal, or Ge content would cause significant wafer bending during the MSA. A well-controlled post-implant, post-thermal budget and Ge content must be

considered to avoid wafer bending and defect formation for the advanced PMOSFETs.

A design rule of the strained SiGe S/D with different active area sizes to form the defects in the underlying Si substrate during the MSA has been also proposed for the 28nm PMOSFETs. As the ratio of total SiGe area to whole wafer was less than 10%, the wafer bending was acceptable small for the following lithographic limitation. Therefore, a well-designed ratio of global SiGe area to whole wafer area is important to avoid large wafer warpage in the integration of the SiGe and MSA. We also came out the critical SiGe area to avoid the defect formation in the underlying Si substrate during the MSA. With the local SiGe area size smaller than 0.2um2, upon MSA there is no defect formation in the underlying Si and the junction leakage could be controlled as low as those of the non-MSA process. Therefore, a well-designed ratio of the global SiGe area to the whole wafer and local SiGe area size were proposed for the 28nm CMOSFETs volume production.

Secondly, for the channel engineering of epitaxial strained SiGe, a novel technique to create the suspending stacked gate oxide and subsequently to fill in an embedded SiGe channel (ESC) between the gate oxide and under-layered silicon substrate has been proposed for the first time to fabricate the 28nm PMOSFETs. Without the Si surface passivation on the embedded SiGe channel, such an ESC structure could achieve p-FETs transconductance (Gm) gain of 26% higher as well as Ion_Ioff performance gain of 8% higher than those of conventional strained Si p-FETs with the S/D SiGe. Better S/D resistance (Rsd) in the resistance versus gate length plot and improved swing slop of Id_Vgs plot indicates the higher mobility in the ESC devices. Moreover, the off-state gate current and reliability stressing of the ESC structure are also comparable to the conventional ones. From the X-ray photoelectron spectrum (XPS) analysis, only the Si-O bonding and no Ge-O bonding at the SiGe/SiO_2 interface could be accounted for this superior gate oxide integrity for the ESC and strained Si structure. Therefore, such a novel technique with an ESC structure is very promising for the 28 nm pMOSFETs devices and beyond.

Finally, the strained SiGe source/drain (S/D) and the novel embedded SiGe channel of the PMOSFETs with the structure and technique improvement are promising to boost device performance for the 28 nm node and beyond.

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Chapter 1

Introduction

1.1 Overview of SiGe alloy for semiconductor

For the past few decades, continuous focus on Moore's Law transistor scaling has provided increasing CMOS transistor performance and density. First stated in 1965, Moore's law describes the technology advancement over the past 40 years which has allowed the number of transistors on a chip to double about every two years [1]. This phenomenal progress has been made possible by continual downscaling of the metal-oxide-semiconductor field-effect transistor (MOSFET) to smaller physical dimensions. MOSFETs have the remarkable feature that as they become smaller they also become cheaper, consume less power, become faster, and enable more functions per unit area of silicon. As a result, denser silicon integrated circuits (ICs) can be realized, offering superior performance at reduced cost per function for the advanced next technology generation.

For much of this time, Moore's Law transistor scaling meant classic scaling, where oxide thickness (*Tox*), transistor length (*Lg*) and transistor width (*W*) were scaled by a constant factor (*1/k*) in order to provide a delay improvement of *1/k* at constant power density. However, in recent years, classic scaling has become less influential, having been supplanted by the use of performance enhancers (such as strain and high-k metal gate). The literature has reported the significant role that SiGe has played in the past on enhancing CMOS transistor performance, provide some information on present and developing uses of SiGe for CMOS scaling, and speculate on the role that SiGe will play in future CMOS technology generations [2-3]

1.2 Why SiGe

As we knew that Ge material shows higher electron and hole carrier mobility than those of Si material. Ge and Si present their drift electron mobility 3900, 1500 cm^2/V-s, respectively, and 1900 and 490 cm^2/V-s for drift hall mobility. Mobility is simply related to carrier inter-scattering time and effective mass in semiconductor material. Let's discuss how Ge atoms and Si atoms demonstrate different effective mass in the semiconductor. Consider 1-dimension periodic atom with potential, U, to affect carrier transport in the series of atoms. Assume carrier wave function follow Schrödinger time independent equation, then the wave function is reduced to the relationship of energy and space. In order to follow continuous boundary conditions of carrier transport at the atomic potential well, a relation of energy (E) and momentum (K) is established, so called E-K diagram. Free electron in the reduced E-K diagram boundary shows no band gap between two energy states. However, for semiconductor material, such as Ge and Si atoms, they show 2U of band gap among two energy states at the boundary, lower one is valance band, the upper one is conduction band. One can obtain 1-D E-K diagram to determine the curvature of conduction band, which indicates effective mass of carrier. For Ge, the curvature of conduction band valley is smaller than that of Si. Therefore, Ge shows small effective mass than that of Si resulting in higher mobility than Si.

1.3 Global strain by SiGe at substrate

Biaxial tensile strain is of particular interest for NMOS silicon channels. Strain can be introduced by epitaxial growth of lattice mismatched Si on SiGe [4-5]. Because the Si lattice is smaller than the SiGe (or Ge) lattice, the Si layer will be stretched in two directions (biaxially). This biaxial stretching places the channel in biaxial tension and breaks the symmetry of the six-fold conduction band valleys. The out-of-plane valleys (lower transport mass) drop in energy, thus electrons move to populate these lower mass valleys. Furthermore, the energy separation between valleys is increased, reducing scattering between bands and valleys. The work in this area was done by Welser in 1992, when he first quantified the strain enhancement for NMOS in strained Si on relaxed SiGe. This was followed with a series of comparative studies with both strained and unstrained Si surface channels. That repopulation and reduction of scattering due to valley splitting with stress resulted in a reduction of biaxial stress at high fields. Strained Si on relaxed SiGe is just one of several process options for obtaining biaxial strain using Si/SiGe systems as shown in Fig.1.3.1.

However, in the past decade, in the most recent technology nodes, much effort has been directed towards increasing the carrier mobility and thus improving Ion by biaxial strain engineering. The wafer-level strain methods such as tensile-stressed Si on relaxed $Si_{1-x}Ge_x$ did not make their way to high volume production due to high defect density in the underlying SiGe layer, which was not favorable for junction leakage. It is difficult to obtain a relaxed $Si_{1-x}Ge_x$ buffered layer without dislocation formation and propagation into to upper tensile silicon layer where electrons transport.

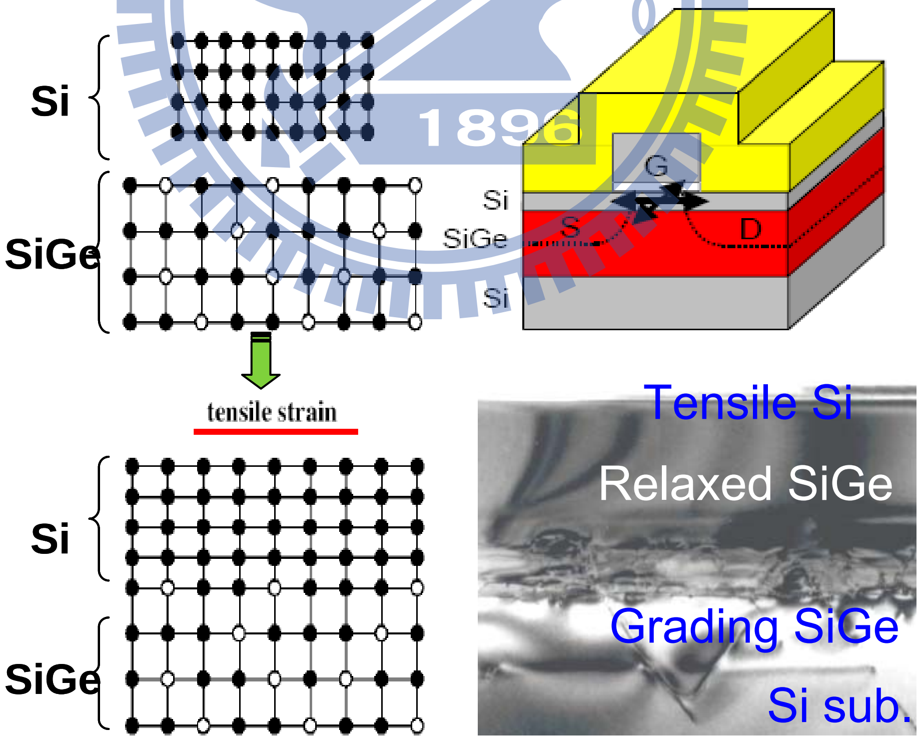


Figure 1.3.1 The global strain formation by SiGe at blanket substrate with tensile Silicon on relaxed SiGe, which shows high defect density (Welser, J. et.al, IEDM, 1992)

1.4 Local strain by SiGe at source/drain region

Another method of implementing SiGe/Si system in the semiconductor to achieve strained silicon is uniaxial compressive stress, which is along <110> channel direction and that is of particular interest for PMOS silicon channels as shown in Fig.1.4.1. Uniaxial strain can be produced by growing lattice mismatched SiGe inside Si source-drain regions. Because the SiGe lattice is larger than the Si lattice, and because the source-drain regions run parallel to the channel, the SiGe layer will push on the source-drain regions (and thus the channel) in only one direction as shown in Fig.1.4.2 and Fig.1.4.3 [6-8]. This single direction pushing places the channel in uniaxial compression and both warps and splits the valence band structure of silicon. The band warping produces improved effective transport mass for the heavy hole band. The uniaxial stress further increases the light-hole to heavy-hole band separation reducing the inter-band scattering. Uniaxial strain along <110> channel direction has a significant advantage over biaxial strain due to the presence of shear strain components which are responsible for strong anisotropic warping of the bands leading to repopulation of carriers to the band structure regions with the lighter transport mass. Hence, a strained SiGe at the source/drain region provide a uniaxial compressive stress to Si channel and push other two directions to become tensile stress due to poison ratio effect which is preferred for PMOS device performance enhancement as shown in Fig. 1.4.4 and Fig. 1.4.5.

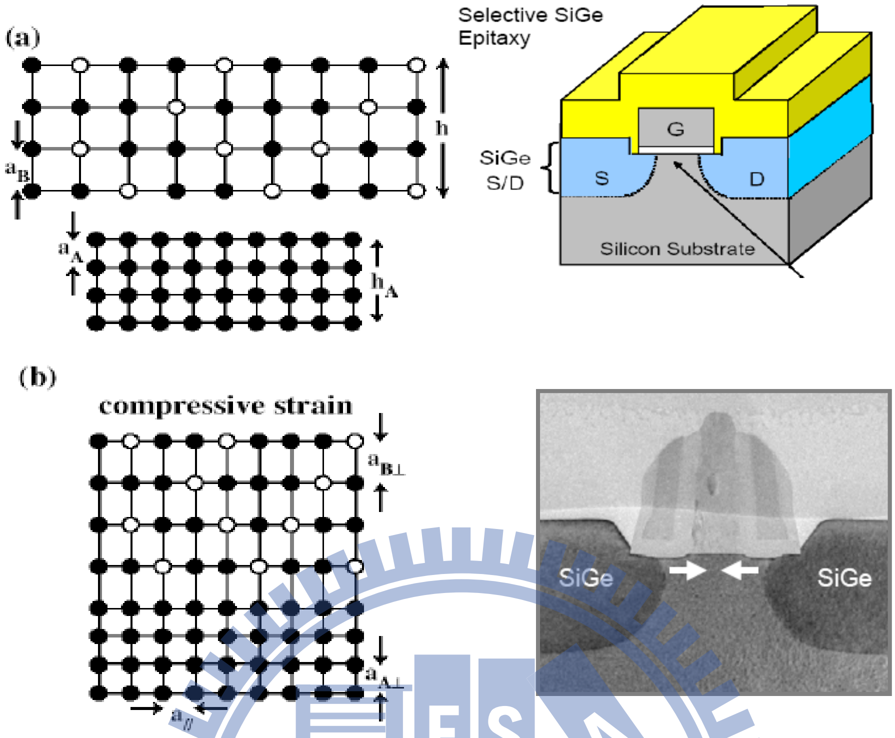


Figure 1.4.1 The local strain by SiGe at source/drain region with uniaxial strain, which shows almost fully strained SiGe and very low defect density (Thompson, S. et.al. IEDM 2002).

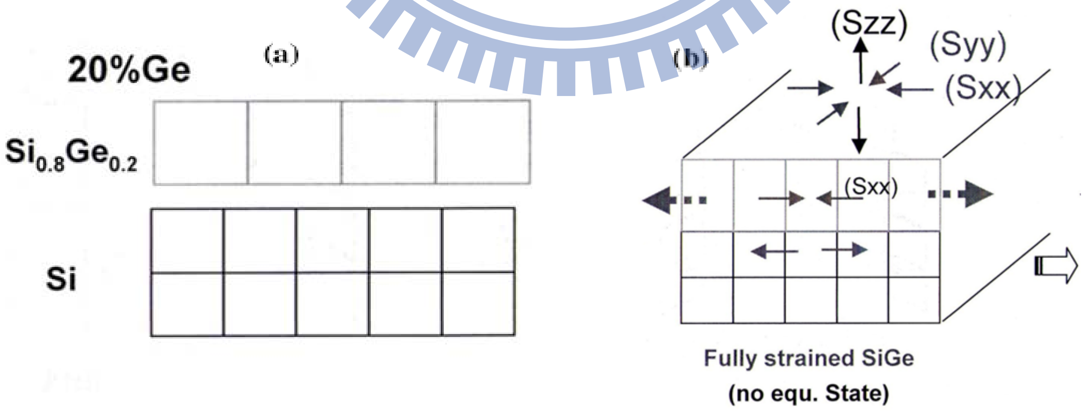


Figure 1.4.2 (a) $Si_{0.8}Ge_{0.2}$ shows large lattice constant than silicon. (b) fully strained SiGe on the silicon substrate (not equilibrium state)

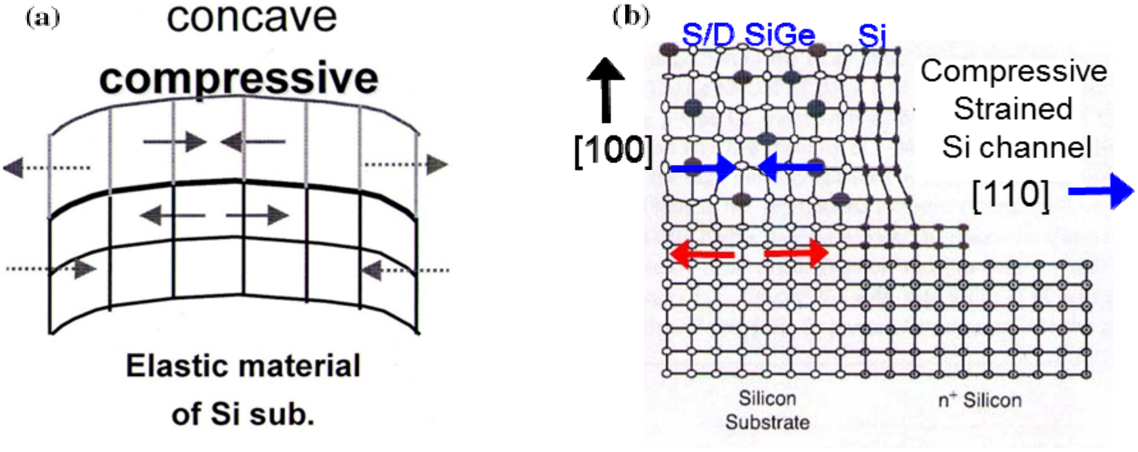
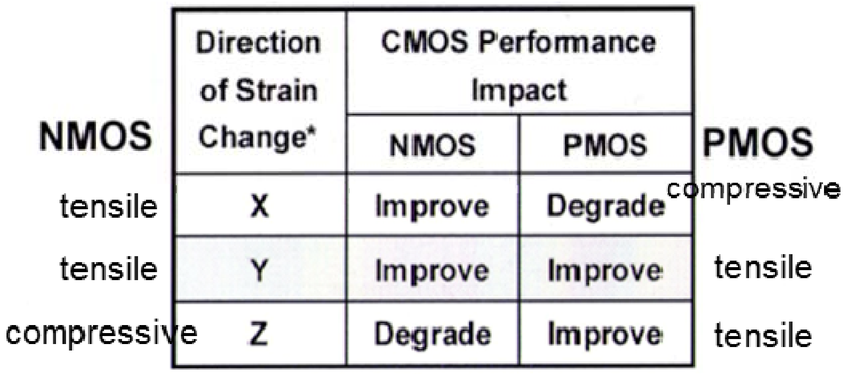


Figure 1.4.3 (a) equilibrium state of blanket strained SiGe on Si and wafer bending (b) schematic plot of strained SiGe in the S/D region (Thompson, S. et.al. IEDM 2002).

Figure 1.4.4 The local compressive stress by SiGe at source/drain region with uniaxial strain along <110>, and tensile stress for other two direction. (Lim, Ji-Song et. al, TED, 2004)



NMOS	Direction of Strain Change*	CMOS Performance Impact		PMOS
		NMOS	PMOS	
tensile	X	Improve	Degrade	compressive
tensile	Y	Improve	Improve	tensile
compressive	Z	Degrade	Improve	tensile

Figure 1.4.5 NMOS and PMOS preference strain direction and performance impact (Lim, Ji-Song et. al, TED, 2004)

Therefore, a fully strained SiGe at the source/drain region with low interfacial defect density demonstrates a uniaxial compressive stress to Si channel and provide huge PMOS device performance boosting and its low defect density make it easy to implement at advanced CMOSFETs process and volume production.

1.5 Measurement techniques for strain by XRD and Raman scattering

X-ray diffraction (XRD) and Raman scattering are the most common techniques for assessing strain on large area and nano-beam and convergent beam diffraction (NBD and CBED) are the most common techniques used for assessing strain within the channel region, but not mature yet for strained-SiGe measurement.

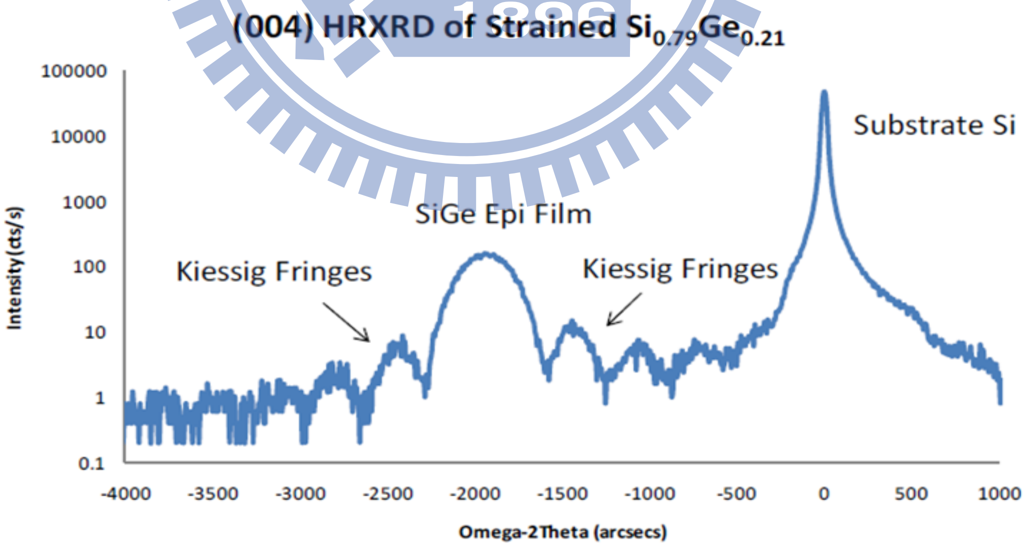


Figure 1.5.1 The XRD shows silicon peak and SiGe epitaxial layer with good fringe profile. (Kelin J. et. al, ECS Trans. 2010)

In an X-ray diffraction measurement, the sample is mounted on a goniometer and rotated

XRD uses Bragg scattering at x-ray wavelengths to determine the configuration of atoms in a crystal to produce a diffraction pattern. XRD can determine epitaxial layer in-plane and out of plane strain components through analysis of symmetric and asymmetric diffraction patterns as shown in Fig.1.5.1. For SiGe samples of interest, XRD can determine the Ge content in buffer and graded layers, the strain of SiGe buffer and epitaxial layer and determine dislocation type and density. However, XRD cannot measure small structures, has limited depth resolution and poor sensitivity to ultrathin films/surface layers.

Raman scattering is the inelastic scattering of photons from vibration–induced phonon modes in a material. Raman scattering is a two–photon process ($h\omega_{laser} - h\omega_{scattered} = h\omega_{phonon}$) whose probability is dependent on the polarizability change in the bond during phonon motion [9]. A laser source is typically used for Raman spectroscopy and the recorded spectrum shows the scattering intensity relative to the shift in frequency of the laser. In crystalline materials such as silicon and SiGe, the presence of stress causes a shift of phonon peak positions as shown in Fig.1.6.1. The magnitude and direction of the shift can be correlated to the amount and sign (compressive/tensile) of the strain. By accessing the Ge-Ge, Si-Ge and Si-Si phonon modes one can derive Ge content and strain independently for SiGe systems including Si epitaxial layers. Inherently Raman is an indirect measure of the lattice constant(s) of the system and suffers from phonon broadening effects such as laser heating. As such, XRD offers better accuracy and precision, but Raman is much faster, has a significantly better spot size (~1 micron), and delivers improved surface sensitivity (dependent on laser wavelength).

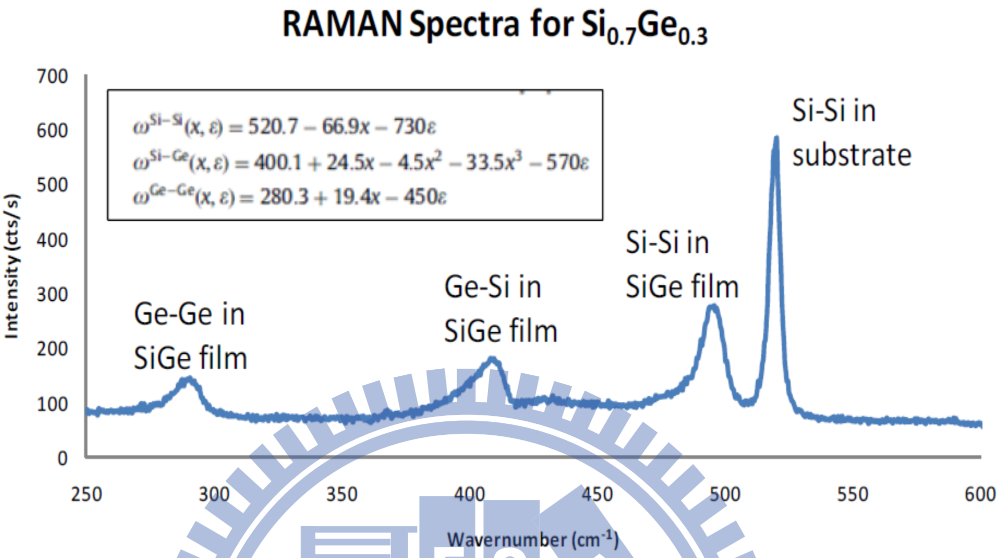


Figure 1.6.1 The Raman spectra of SiGe epitaxial layer on the silicon substrate. (Kelin J. et. al, ECS Trans. 2010)

1.6 Roadmap of epitaxial SiGe for PMOSFETs

In order to maintain the historical 17% per year performance improvement rate, various novel processes and materials have been introduced to the bulk Si-MOSFET structure. Figure 1.7.1 shows the insertion of the new materials for Intel's logic PMOSFET technologies. While the use of strain as a performance enhancer is expected to continue as a key contributor to the CMOS scaling roadmap. Epitaxial SiGe was used at Source/drain region of PMOSFET device performance enhancement for the first time for 90nm technology. Then source/drain recess shape was modified to boost pFETs device performance from 65nm to 32nm. A 3-D device structure was implemented from 22nm. After that, the most intriguing future use of Ge or

SiGe in CMOS scaling is as a high mobility replacement for the Si channel. Recall that Ge was the primary transistor material from the invention of the transistor in 1947 until the 1960s, when MOS became technologically important. The two most critical reasons for switching from Ge to Si for early MOS technology remain the two most critical issues today; namely the poor quality of GeO2 compared to SiO2 and the smaller band gap of Ge compared to Si. The critical changes between 1960 and 2010 leading to reconsideration of Ge channels are: 1. advent of manufacturable high-k technologies, 2. decreasing voltages of modern products, and 3. development of highly quantum confined devices, which increase the effective band gap.

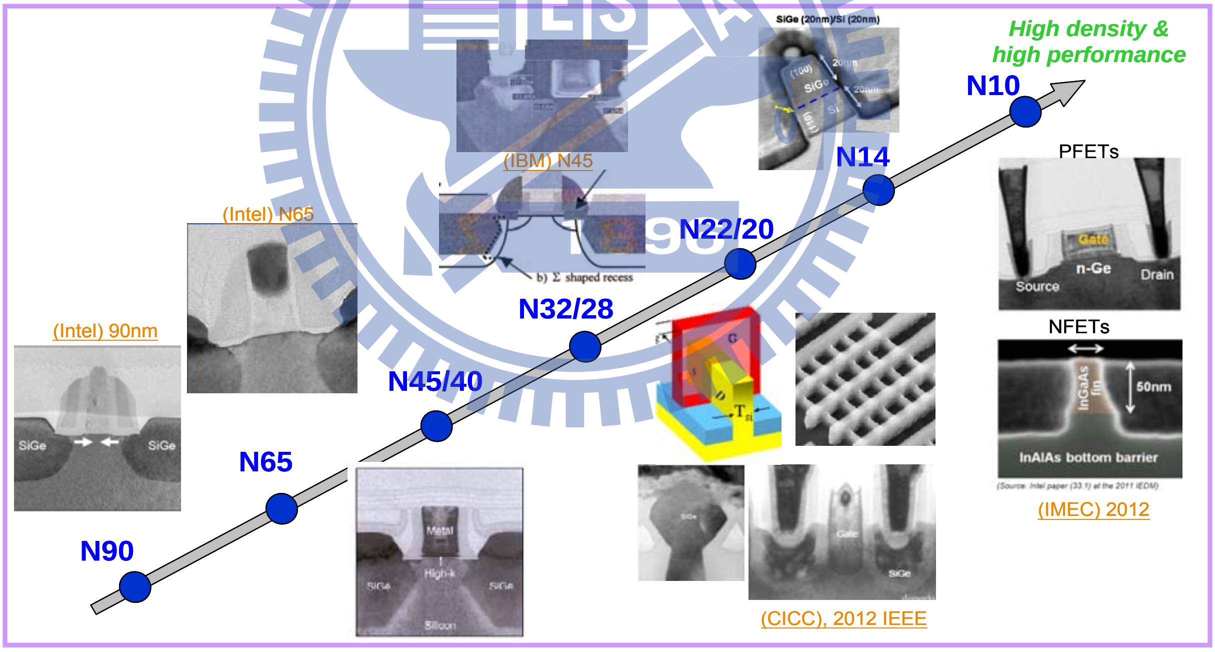


Figure 1.7.1 The epitaxial SiGe and source/drain recess profile evolution for PMOSFETs and beyond. (James, D. et al. CICC, 2012)

Competitive dielectric thicknesses without degrading mobility, the key challenge with Ge (and SiGe) is that both industry and academic data show rapid degradation in mobility with decreasing electrical oxide thickness. The primary model for this degradation is poor quality germanium oxide at the Ge/dielectric interface. Thus, the goal is to create a high quality interface between the dielectric and the SiGe [10-14].

Scaling CMOS to and beyond the 22 nm node will probably require structural changes to the planar silicon transistor and/or use of high-mobility channel material. The advanced transistor structures such as multi-gate FET (MuGFET) is seen as potential replacements for the bulk MOSFET because of their inherent superior electrostatic integrity. Another promising alternative is the adoption of germanium (Ge) as the channel material. p-channel Ge-MOSFETs have been proposed for highly-scaled high-performance technology due to higher bulk mobility of holes in Ge.

1.7 Motivation

Epitaxial SiGe at source/drain (S/D) region for pFETs drive current enhancement has been pursued aggressively in scaled CMOS technologies and significant carrier mobility enhancement at strained Si channel have been reported. Increasing Ge concentration in the S/D SiGe region is a straightforward method without extra process flow / profile change and device parameter tuning to boost device performance as PFETs scaling down. However, Ge content is inevitable to continuous increment in the S/D SiGe due to the critical thickness effect that increasing Ge content in the S/D SiGe would cause misfit dislocation formation in the interface of SiGe and Si substrate. Hence, for high Ge content at S/D region, strain loss due to misfit dislocation formation at the SiGe/Si substrate made real carrier mobility lower than that of theoretical fully strain. In order to meet target of device performance for the technology generation, suppressing the dislocation formation of epitaxial SiGe at S/D region caused by post-SiGe implantation and thermal budget is very important for 28nm CMOS volume production.

Since we would investigate the implant species effect on S/D strained SiGe relaxation as well as implantation sequence effect and resultant defect formation once strained SiGe was relaxed by post process. Meanwhile, how strain loss of S/D SiGe affected device performance. On the other hand, to investigate in more detail the impact of MSA on the leakage current of embedded SiGe S/D junctions with SiGe area size dependency is very important. Particular emphasis is to come out a well-designed rule of the S/D strained *SiGe area* with MSA process to avoid wafer large warpage and defect formation. The resultant design rule of active SiGe area can obtain a as low junction leakage as that of non-MSA process or non-SiGe process to volume production of 28nm CMOSFET and beyond.

In order to further boost device performance in 28nm PMOSFETs and beyond, another approach to channel strain engineering is SiGe channel, which was considered as a promising candidate in the nano pMOSFETs for the performance boost-up. As we knew that higher carrier mobility about three times in the SiGe material than that of Si. Hence, carrier transport in the SiGe channel is good candidate to boost device performance. We would demonstrate a novel embedded SiGe channel (ESC) structure composed of strained SiGe channels without extra Si surface passivation to show potentially superior hole mobility and superior gate oxide integrity.

1.8 Thesis Organization

In this thesis, various structures and techniques are studied for the fabrication of high-performance 28nm PMOSFETs through the source/drain (S/D) and channel engineering of epitaxial strained SiGe. In addition, the process parameters to impact of strained-SiGe relaxation induced channel stress degradation and defect formation on device performance are investigated as well.

In chapter 2, for source/drain engineering of epitaxial strained SiGe, the degree of strained-SiGe relaxation caused by implantation importantly affected the channel stress and the formation of defects in the underlying Si substrate as well as wafer bending when millisecond anneal (MSA) was applied to the S/D strained-SiGe in 28nm PMOSFET devices.

In chapter 3, For process parameter effects on strained-SiGe relaxation, the formation of the induced defects in the underlying Si substrate associated with the interaction of the partly relaxed strained-SiGe layer and subsequent millisecond annealing (MSA) has been explored. Three kinds of methods including post-SiGe implant, post-SiGe soak anneal and in-situ Ge at.% effect that were used to boosting device performance were investigated how to avoid strained-SiGe relaxation and defect formation in the underlying Si during MSA.

In chapter 4, a design rule of S/D SiGe with different active area size to form defects in the underlying Si substrate during MSA has also been proposed for 28nm PMOSFETs.

In chapter 5, for channel engineering of epitaxial strained SiGe, a novel technique to create the suspending stacked gate oxide and subsequently to fill in an embedded SiGe channel (ESC) between the gate oxide and under-layered silicon substrate has been proposed for the first time to fabricate the 28nm PMOSFETs.

Finally, summary and conclusions as well as recommendation for further research are given in chapter 6 and chapter 7, respectively.

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Chapter 2

The investigation for the underlying Si defects induced by the relaxation in strained-SiGe layer following the millisecond annealing for the 28nm PMOSFETs

2.1 Introduction

Strain engineering and material innovation have been critical to improve the performance of CMOS devices over the past few years. For instance, selective epitaxially SiGe is used in source/drain regions to introduce uniaxially compressive stress into PMOSFETs, substantially enhancing the carrier mobility and the drive current, which is very difficult to be achieved by the conventional Si technology [1-4]. Therefore, introducing a high quality of epitaxial SiGe layer at source/drain for device performance boosting is very crucial for the advanced PMOSFETs. By growing a epitaxial strained-SiGe layer in the S/D region with suitable process condition of Ge content and SiGe thickness a compressive fully strained SiGe stressor to PFET channel was achievable as shown in Fig.2.1.1. In fact, the strained SiGe layer was psudomophic state and with Ge content increasing the strained SiGe thickness was reduced dramatically. Meanwhile, as deposition temperature of the epitaxial SiGe layer was raised, the critical thickness (fully strained SiGe thickness) was also reduced. Hence, growing a fully strained SiGe at source/drain region with proper deposition temperature and Ge content as well as thickness was very important for channel stress enhancement. Fig.2.1.2. showed a strained SiGe at source/drain region and it provided an uniaxial stress to channel. If one considered 1.2% of strain formed by S/D SiGe, the corresponding carrier mobility enhancement was significantly exhibited 60% improvement over un-strained one as shown in Fig. 2.1.3. Hence, S/D strained SiGe is an important knob for device boosting for 28nm CMOS and beyond.

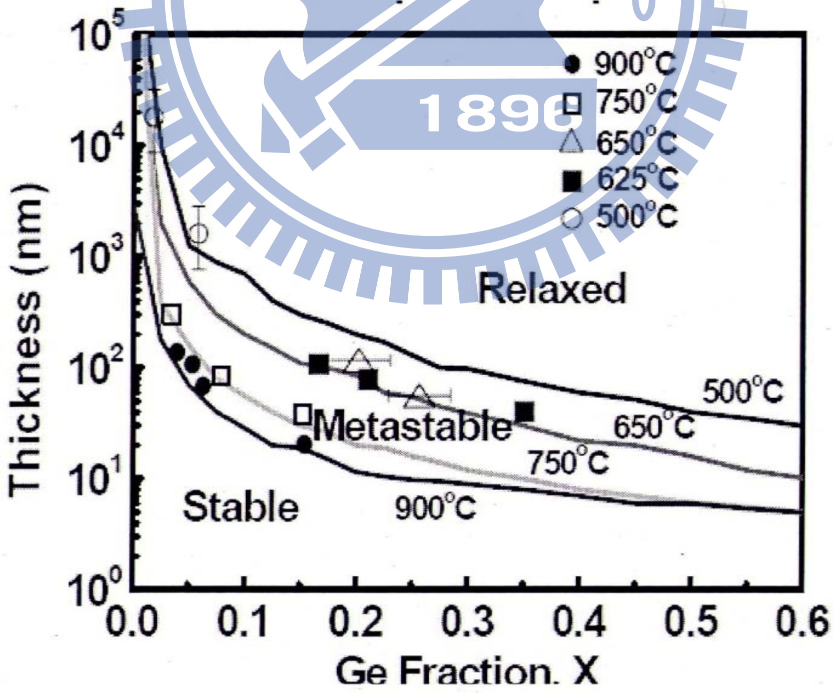


Figure 2.1.1 The strained-SiGe Ge fraction and temperature effect on strained thickness (D.C. Houghton, et. al. J. Appl. Phys. 1991)

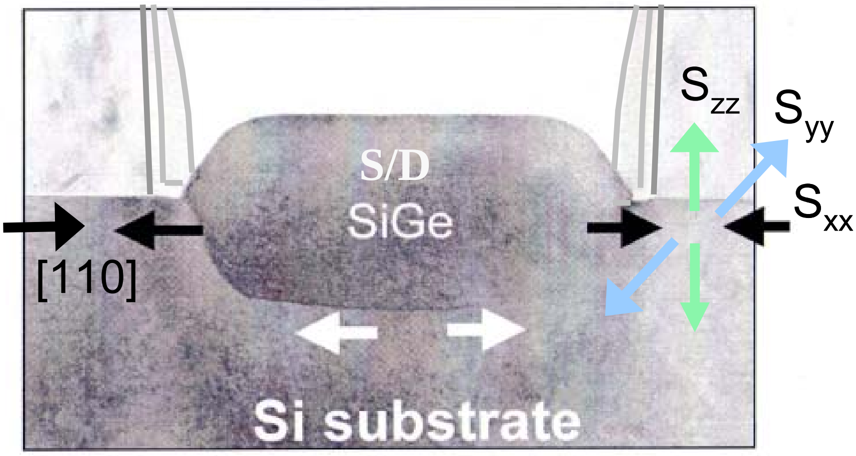


Figure 2.1.2 The S/D strained SiGe structure and its uniaxial stress to Si channel (Thompson, S. et.al. IEDM 2002).

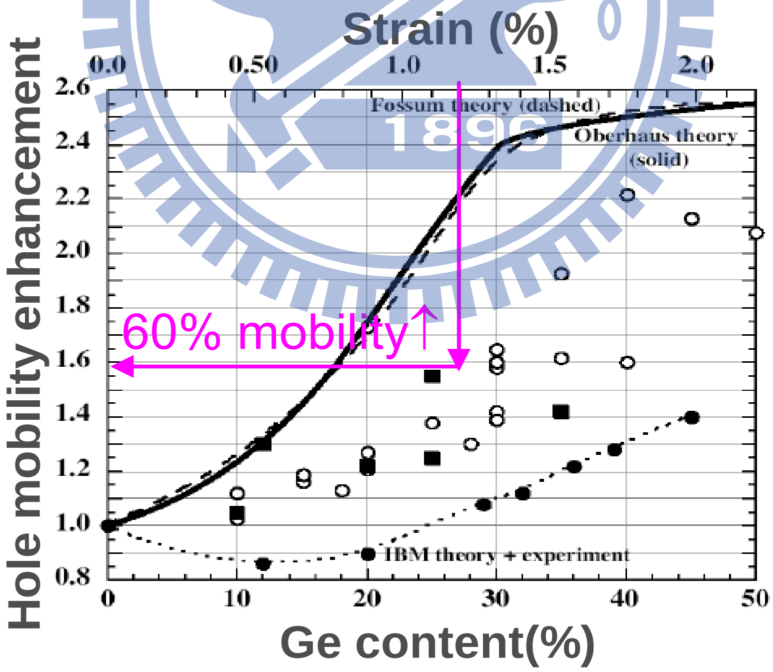


Figure 2.1.3 The strained-SiGe Ge content effect on hole mobility enhancement. (D.C. Houghton, et. al, ICPS 2004)

2.2 Motivation

2.21 Why we need S/D SiGe for 28nm device performance

Epitaxial SiGe at source/drain (S/D) region for pFETs drive current enhancement has been pursued aggressively in scaled CMOS technologies and significant carrier mobility enhancement at strained Si channel have been reported. Increasing Ge concentration in the S/D SiGe region is a straightforward method without extra process flow / profile change and device parameter tuning to boost device performance as PFETs scaling down as shown in Fig.2.2.1. However, Ge content is inevitable to continuous increment in the S/D SiGe due to the critical thickness effect that increasing Ge content in the S/D SiGe would cause misfit dislocation formation in the interface of SiGe and Si substrate. Hence, for high Ge content at S/D region, strain loss due to misfit dislocation formation at the SiGe/Si substrate made real carrier mobility lower than that of theoretical fully strain as shown in Fig.2.2.2. In order to meet target of device performance for the technology generation, suppressing the dislocation formation of epitaxial SiGe at S/D region caused by post-SiGe implantation and thermal process is very important for 28nm CMOS volume production.

In this work, we would investigate the implant species effect on S/D strained SiGe relaxation as well as implantation sequence effect and resultant defect formation once strained SiGe was relaxed by post process. Meanwhile, how strain loss of S/D SiGe affected device performance.

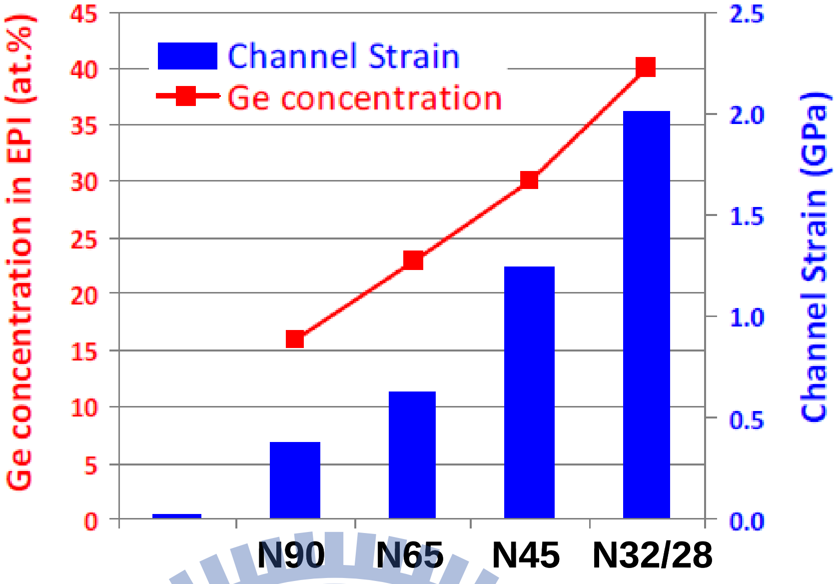


Figure 2.2.1 The strained-SiGe Ge fraction and channel strain for technology node. (Kelin J. et. al, ECS Trans. 2010)

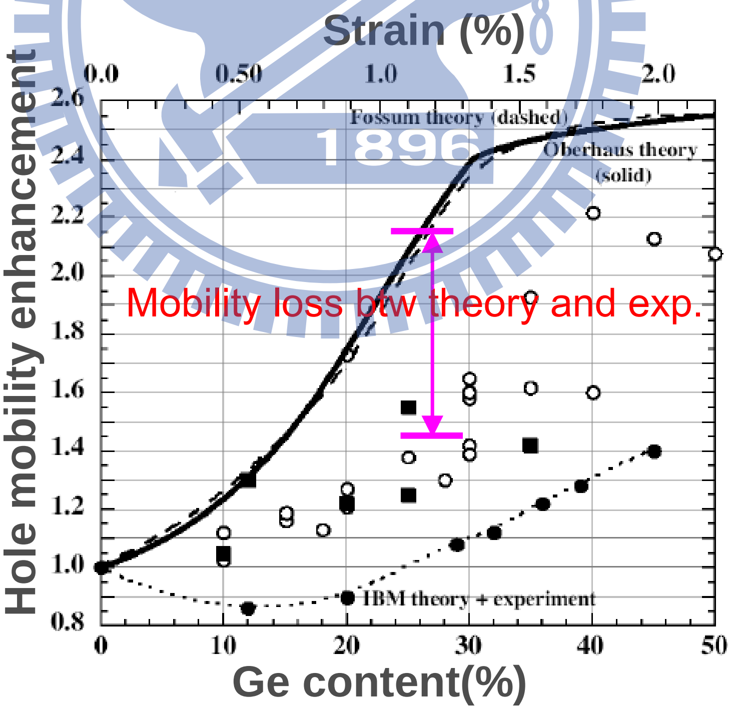


Figure 2.2.2 The mobility loss between theory and experiment for various Ge content.

2.2.2 Why we need millisecond anneal (MSA) for 28nm pMOSFETs

Source/drain strained-SiGe with low resistivity, formed using a well controlled doping concentration and by minimizing the short channel effect associated with a shallow doping profile, is important in CMOS device scaling as shown in Fig.2.2.3. Fig.2.2.4 showed that spacer resistance, R_{spr} (R_{ext} + $R_{S/D}$) dominated the 60% total resistance of PFET. In order to provide a low resistance of R_{spr} R, a high Boron activation is necessary to be achieved by very high temperature anneal to recover implanted Boron as shown in Fig.2.2.5. Recently, millisecond annealing (MSA, flash annealing or laser annealing) [5-7], which promotes dopant activation but causes less dopant diffusion at high annealing temperature,

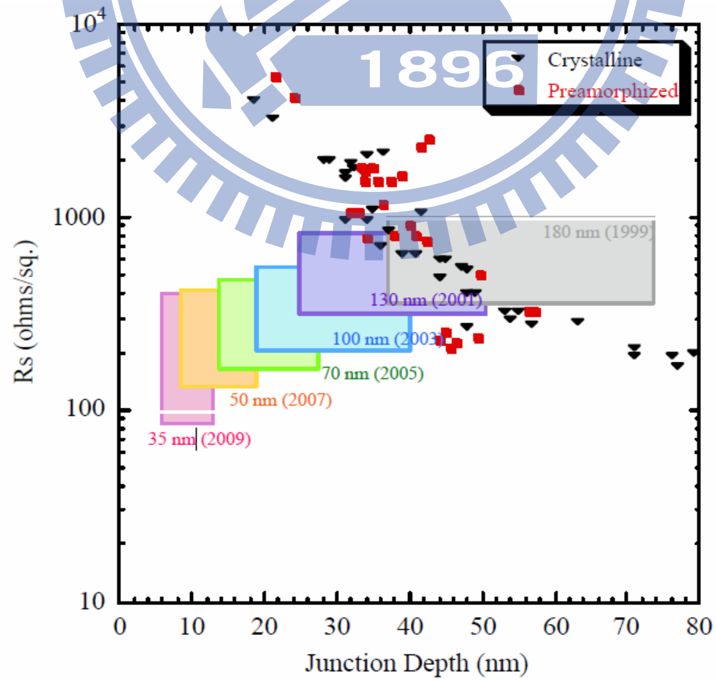
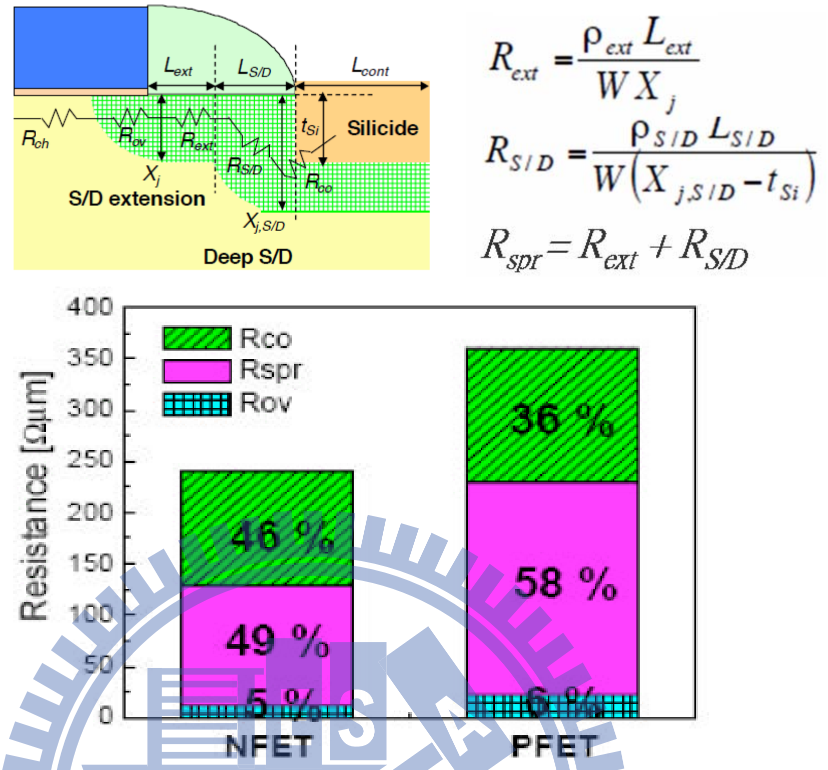


Figure 2.2.3 The Rs performance under scaling junction depth for technology node. (S. D. Kim, et. al. IEDM, 2005)



$$R_{ext} = \frac{\rho_{ext} L_{ext}}{W X_j}$$

$$R_{S/D} = \frac{\rho_{S/D} L_{S/D}}{W\left(X_{j,S/D} - t_{Si}\right)}$$

$$R_{spr} = R_{ext} + R_{S/D}$$

Figure 2.2.4 The spacer resistance dominates 58% of total resistance of PFET. (S. D. Kim, et. al. IEDM, 2005)

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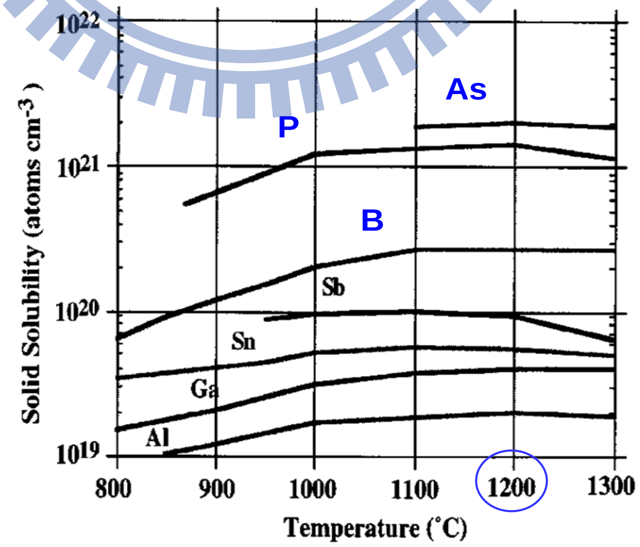

Figure 2.2.5 Solid solubility of Boron reaches saturation at high temperature. (T. Ito, et. al. SSDM, 2001)

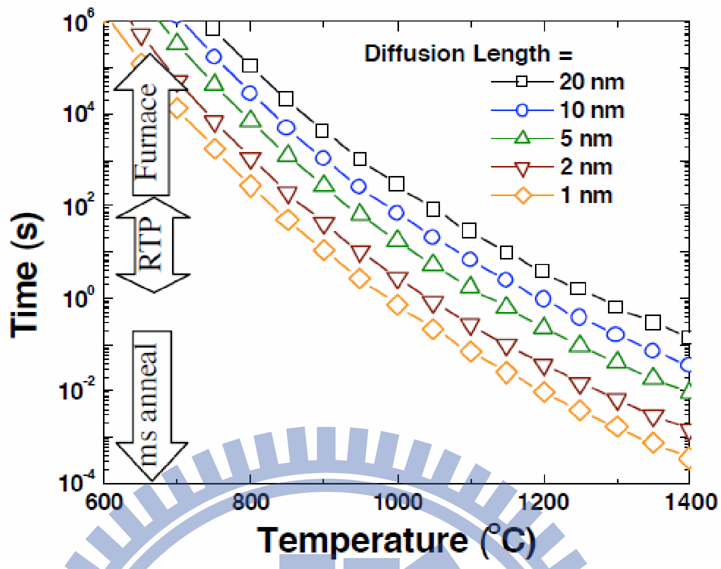

Figure 2.2.6 Anneal temperature and time effect on Boron diffusion length (B. J. Cho, et. al. Int. Workshop Junction Technology, 2004)

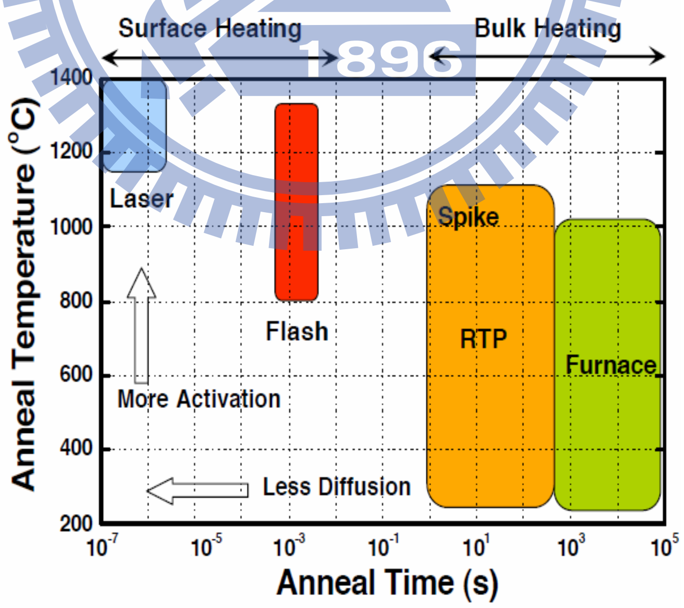

Figure 2.2.7 The surface heating of laser anneal enables to show millisecond anneal with less diffusion. (B. J. Cho, et. al. Int. Workshop Junction Technology, 2004)

has emerged as an alternative approach for high-performance CMOS devices as shown in Fig.2.2.6 and Fig.2.2.7. Therefore, the combination of strained-SiGe in the source/drain regions as channel stressors and MSA process is a candidate method for improving the performance of devices based on the 28 nm technology. However, the relaxation of the strained-SiGe layer due to the large thermal stress that is induced by MSA may make such a combination challenging. [8-11]

The aim of this work is to elucidate defect formation that results from the combination of strained-SiGe and subsequent MSA processes and its impact on strain loss of S/D SiGe as well as device performance. Under certain implantation conditions, the MSA process induced defects in the underlying Si and degraded device performance. The phenomenon of defect formation by the MSA treatment is therefore modeled and discussed, and the effective integration of strained-SiGe and MSA process for fabricating 28nm PMOSFETs is proposed.

2.3. Experiments

2.3.1. Fabrication process – S/D SiGe first prior to implant

A series of PMOSFETs with SiON gate oxide (Equivalent Oxide Thickness, EOT=12A and Gate length, Lg=28nm) were fabricated using source/drain strained-$Si_{1-x}Ge_x$ (x nearly~0.35) and in-situ Boron doping with a 100nm-thick layer on 300mm (001) Si wafers. The pocket implant was conducted in SiGe pattern wafers by implantation using Arsenic (As), at energy of approximately 35keV with titled 35° and a dose of $3E13cm^{-2}$ to suppress the short channel effect (SCE). Spike rapid thermal annealing (RTA) around 1000˚C was carried out to recover the damage induced by implantation and to activate the dopants. Laser MSA annealing at around 1200˚C for 500μs then performing to enhance dopant activation, was as plotted in Fig. 2.3.1.

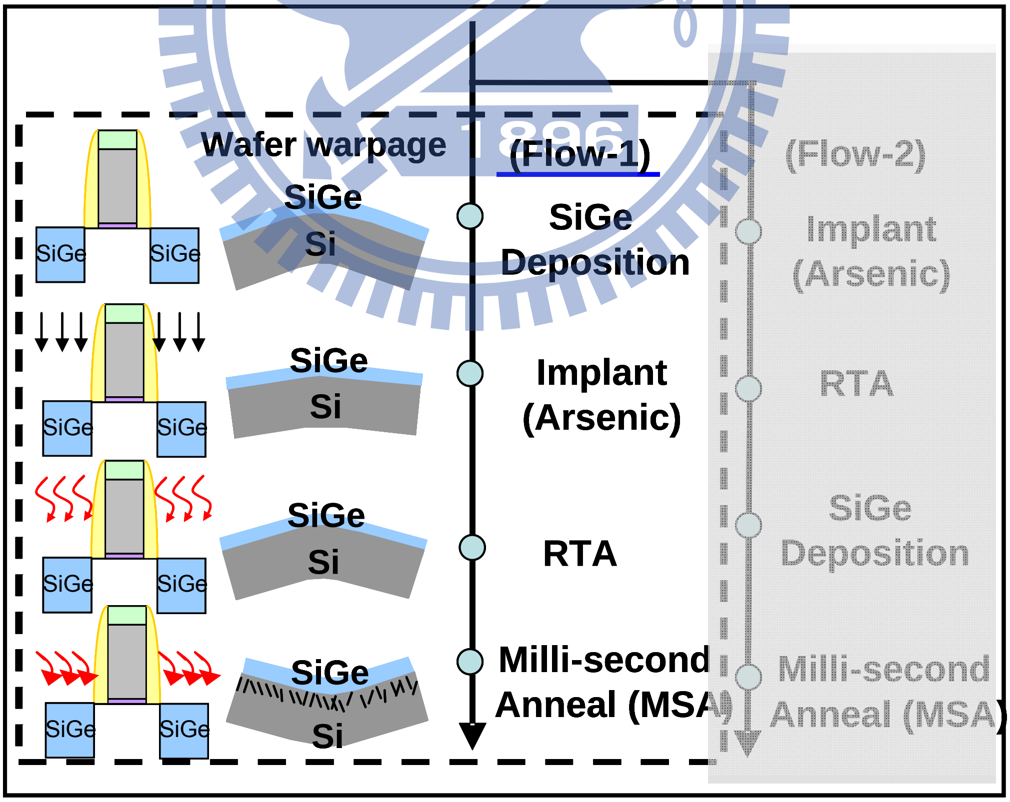

Figure 2.3.1 The Process flow of the source/drain SiGe followed by implantation, then subsequent MSA was conducted.

2.3.2. Fabrication process – S/D SiGe last

For another process sequence of implantation followed by S/D SiGe deposition was explored as well, as shown in Fig. 2.3.2. A pocket As implant at energy of approximately 35keV and a dose of 3E13cm^{-2}. Spike rapid thermal annealing (RTA) around 1000°C was carried out to recover the damage induced by implantation. An S/D recess etch and extra pre-surface clean to provide a good interfacial quality for following SiGe deposition. Same as flow-1, SiGe first, a MSA was conducted to provide low resistance. The subsequent formation of nickel silicide on SiGe, the deposition of a contact etching stop layer (CESL) and metallization were conducted for the standard process. Then, the performance of the PMOSFETs was evaluated. For comparison, PMOSFETs without a source/drain SiGe structure were also fabricated by a similar process sequence.

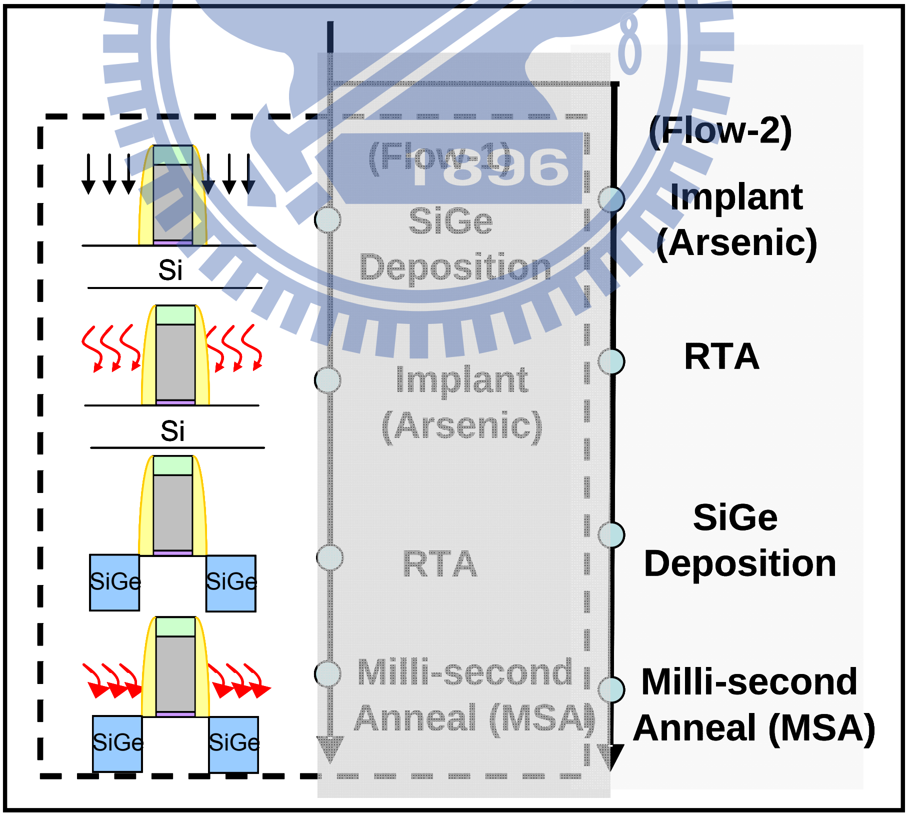

Figure 2.3.2 The Process flow of implantation followed by the S/D SiGe, then subsequent MSA was conducted.

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2. 4 Results and Discussion

2.4.1 Defect formation in the underlying Si for S/D SiGe and MSA

As shown in Fig. 2.4.1, PMOSFETs with implanted SiGe devices that had undergone RTA and MSA processes exhibited higher junction leakage about four orders of magnitude than that of those without implanted SiGe or millisecond anneal device at SiGe area size of 25um^2, implying that the high junction leakage was caused by the combination of the implanted SiGe and millisecond annealing.

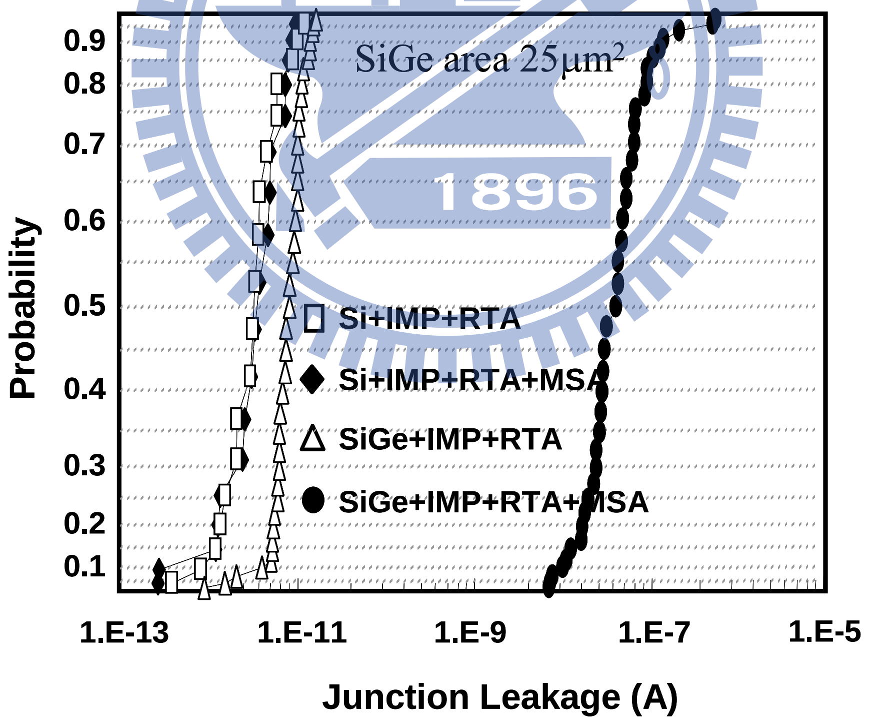

Figure 2.4.1 The implanted SiGe PMOSFETs device with RTA and MSA processes exhibits higher junction leakage than that of those without implanted SiGe or millisecond anneal device.

The severe crystal defects observed in the cross-sectional TEM (XTEM) of Fig.2.4.2, which led to the significant junction leakage, were identified in the SiGe devices followed the MSA process. However, the TEM selective area diffraction demonstrates that the implanted strained-SiGe layer and the underlying Si substrate remained single crystalline. Surprisingly, the defects were observed not only in the SiGe layer but also in the underlying Si substrate to a depth of 2μm. Since MSA employed pulsed surface heating with millisecond peak widths at temperatures below the melting point 1418°C of Si at the surface of the wafer (Fig. 2.4.3) [12-13], the very large thermal stress associated with the huge thermal gradient at SiGe wafer surface few micro meters caused dramatic wafer bending would generate many defects in the strained-SiGe layer and the underlying Si substrate. Hence, the formation of defects in the SiGe and Si substrate by the enormous thermal stress that was produced by millisecond annealing was further established.

In comparison, Fig.2.4.4 shows to apply a small thermal gradient treatment of 5°C/sec to the implanted SiGe wafer with one thermal cycle. Fig2.4.5 revealed that under the small thermal gradient treatment did not produce these defects in the underlying Si. Therefore, small thermal gradient treatment on implanted SiGe would not cause defect formation in the underlying Si substrate but large thermal gradient at SiGe surface would cause defect formation in the underlying Si.

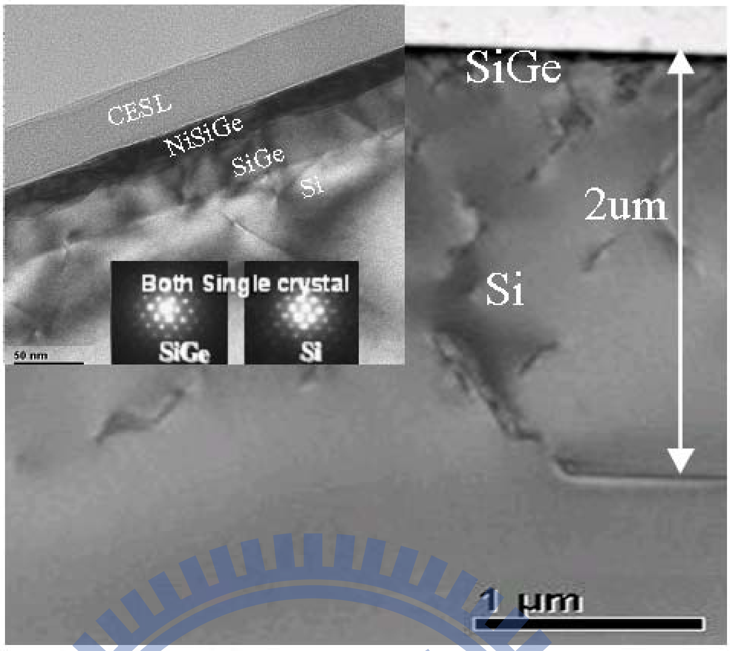

Figure 2.4.2 The TEM of the implanted SiGe wafer with the RTA and MSA process shows high defect density in the relaxed SiGe layer as well as in the underlying Si substrate.

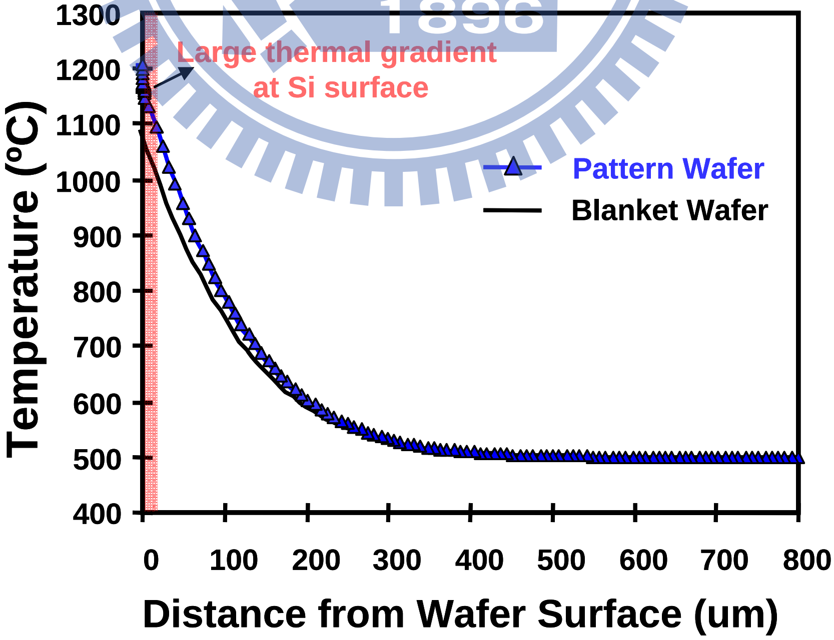

Figure 2.4.3 Simulated MSA wafer temperature profile and exhibited large temperature gradient close wafer surface.

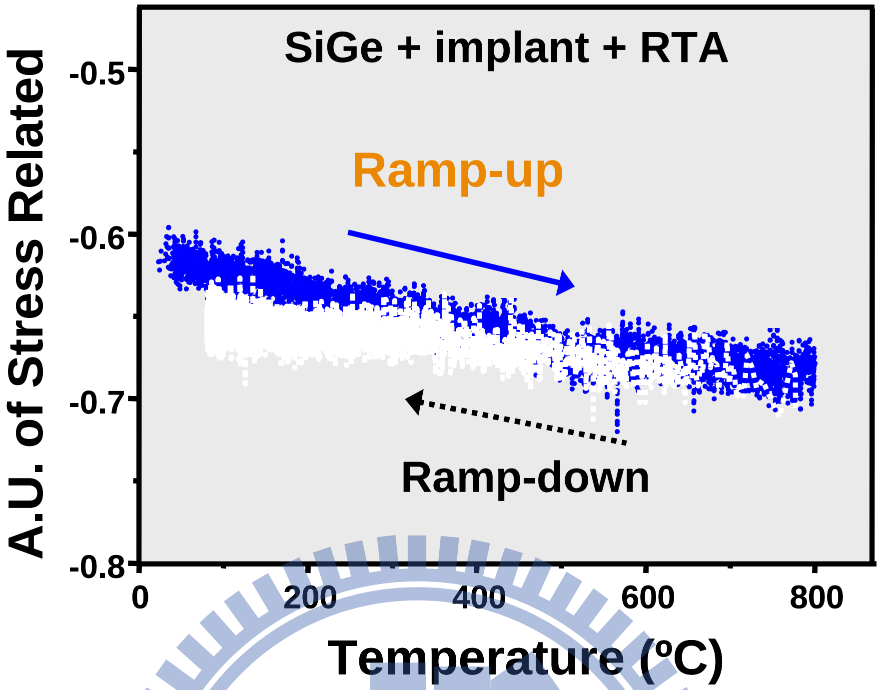

Figure 2.4.4 Small temperature ramp-up and ramp-down on implanted SiGe.

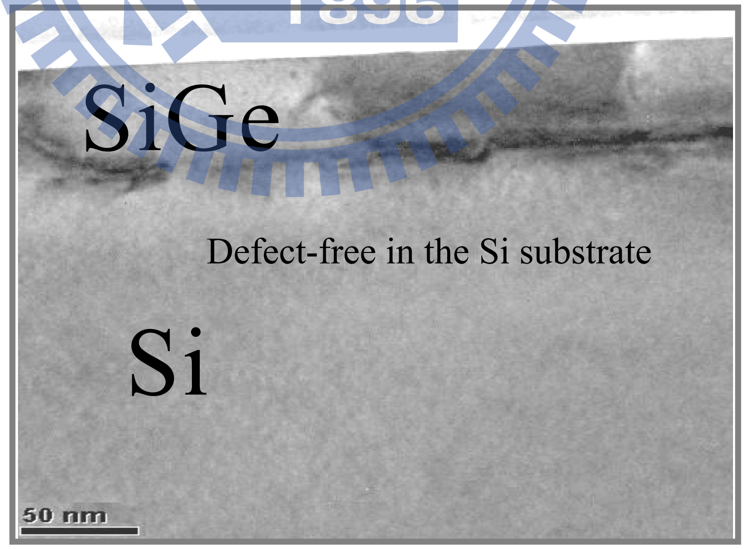

Figure 2.4.5 TEM showed defect-free in the underlying Si under small thermal gradient on implanted strained SiGe.

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To investigate the relationship between the formation of defects in the underlying Si substrate and the combination of implanted SiGe and MSA process on the pattern wafer, identical processing conditions were applied to blanket Si (001) wafers and the corresponding optically measured wafer bow height, which revealed the degree of wafer warpage [14-15], was as plotted in Fig. 2.4.6 The strong correlation between wafer bow height and density of defects observed in the Si substrate was well established. From Fig. 2.4.6, the 100nm-thick strained-$Si_{1-x}Ge_x$ (x nearly 0.35) introduced a compressive film stress with wafer concave downward, then the subsequent medium implantation projection range (Rp) using Arsenic (As), at an energy of approximately 50keV and a dose of 3E13cm^{-2} to make species to reach medium position of the strained-SiGe layer, damaged the upper portion of the strained-SiGe layer, and partially relaxed stress in the strained-SiGe, reducing wafer warpage. Following spike RTA, the implant-damaged strained-SiGe layer was repaired, but not completely. The subsequent MSA caused significant wafer warpage and plastic deformation from its initial compressive to its final high tensile state. Then, defects in the underlying Si substrate were observed as shown in the TEM image. Meanwhile, large wafer warpage up to 150µm in tensile state impacted critical lithography stage, such as contact-hole lithography. For comparison, a strained-SiGe sample directly underwent the MSA process, exhibiting no change in bow height, while its underlying Si was defect-free and did not have warpage-induced lithographic limitation. This result implies that some relaxation of strain

SiGe caused by implantation considerably changes the bow height and causes the formation of defects in the underlying Si for strained-SiGe that undergoes MSA as shown in Fig2.4.7.

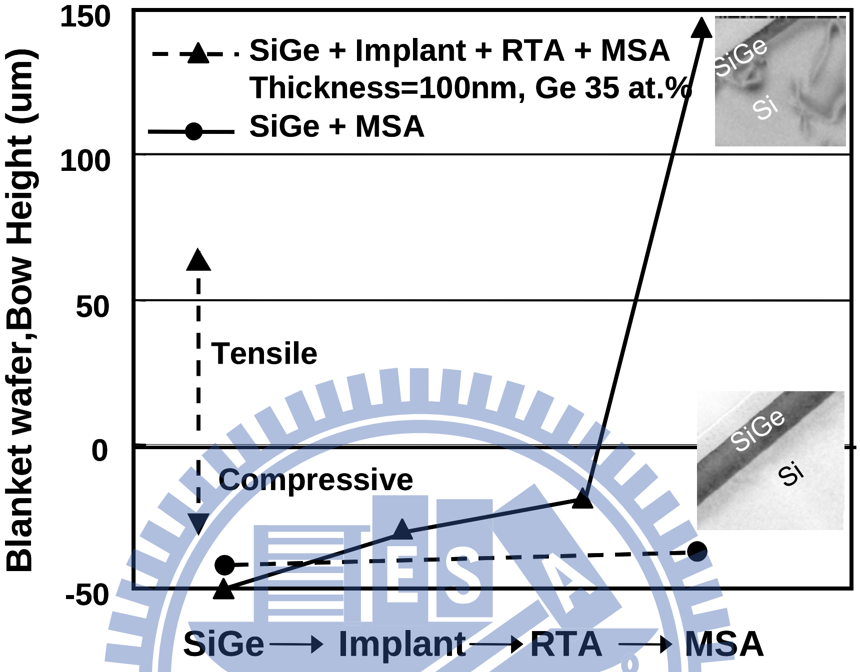

Figure 2.4.6 Change in bow height of strained-SiGe wafer associated with following implantation, RTA and subsequent MSA. A fully strained-SiGe sample directly underwent MSA, exhibited no change in bow height.

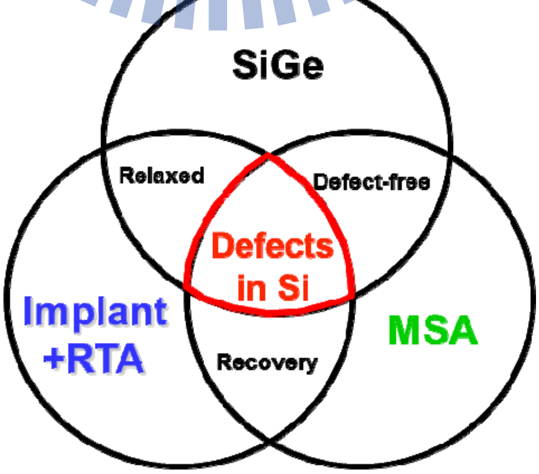

Figure 2.4.7 The combination of implanted strained SiGe and MSA form defects in the underlying Si substrate

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2.4.2. Dopant species effect on strain relaxation of SiGe and device performance

To eliminate the relaxation of strain SiGe by post-SiGe medium implantation range Rp of n-type species, As, implantation conditions are modified to prevent strain relaxation, defect formation and warpage-induced lithographic limitation. Accordingly, a lighter atom, phosphorus (P), with energy of around 20KeV with tilted 25° and a dose of $4e13cm^{-2}$ was used to give the same medium implantation range Rp of As, and minimize the SCE properties. In the inset of Fig. 2.4.8, TEM image indicates that a medium implantation Rp of the species, As, was employed into strained-SiGe layer and led to a clear pre-amorphous implant (PAI) layer in the SiGe layer. Varying As implant dosage in the SiGe layer to cause different level of PAI was investigated as shown in Fig.2.4.9. It was concluded that As implant dosage over $3E13cm^{-2}$ would cause PAI layer in the strained SiGe. The result was also feed to simulation result by the kinetic Monte Carlo (kMC) model. The degree of the As induced implantation damage in SiGe was defined during simulation that Si atoms had moved one-third of the way from original position toward vicinity [16-18]. Since As atoms are large, the damaged layer of pre-amorphorized implantation resulted in the large relaxation of strain SiGe and severely affected the pseudomorphic SiGe. The following RTA process was unable to recover relaxed strained-SiGe, which was indicated from the broadening XRD rocking curve of SiGe in Fig. 2.4.10. Therefore, subsequent MSA produces defects in the underlying Si substrate, as revealed by the XRD rocking curve of the broadening Si peak in

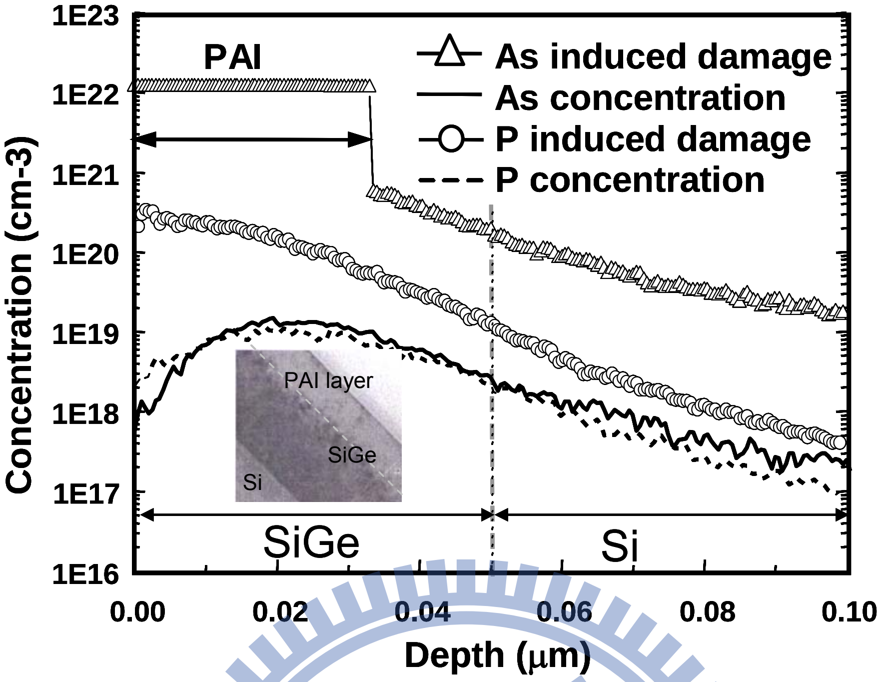


Figure 2.4.8 Simulated that implant species arsenic (As) and phosphorus (P) at the comparable implant energy and concentration caused different degrees of damage in the strained SiGe layer

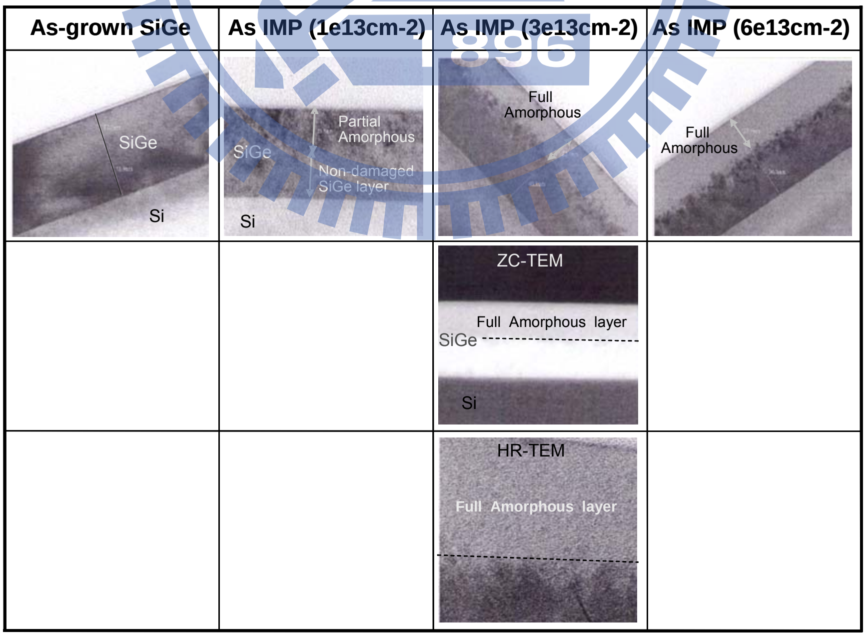


Figure 2.4.9 The As implant dosage effect on PAI layer formation in SiGe

Fig. 5(b). Nevertheless, phosphorus, which has a small atomic size as compared to As, implanted at a concentration close to that of the As atoms, did not cause PAI in the strained-SiGe layer, as shown in Fig. 2.4.8. Therefore, the subsequent spike RTA process enabled the non-PAI SiGe to be almost fully recovered as strained-SiGe, and the following MSA did not cause defects in the underlying Si, as revealed by the tight SiGe profile and shaper Si peak in the XRD rocking curve of phosphorus. Figure 2.4.10 also presents results of a simulation of fully strained-SiGe samples as a reference. The figure reveals that the strained-SiGe was almost fully recovered. Hence, well-controlled implantation in the source/drain SiGe is required to prevent strain relaxation and defect formation.

Properly selecting implanted species to form almost fully strained-SiGe enables Si channel stress to be increased to further boost the device drive current. In Fig. 2.4.11, the Raman measurements reveal the relaxation of strained-SiGe by various implanted species on the Si channel stress of the Si substrate. Post-SiGe arsenic implantation caused large strained-SiGe relaxation, reducing the effective stress in the Si channel below that associated with SiGe relaxation by phosphorus.

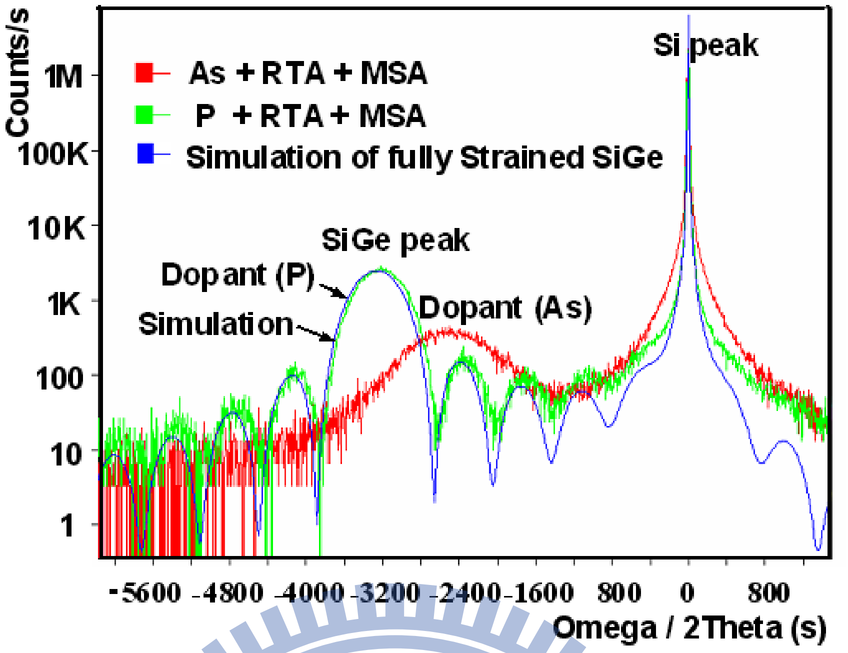


Figure 2.4.10 The relaxation of strained-SiGe is a function of dopant impurities, determined from the XRD rocking curve.

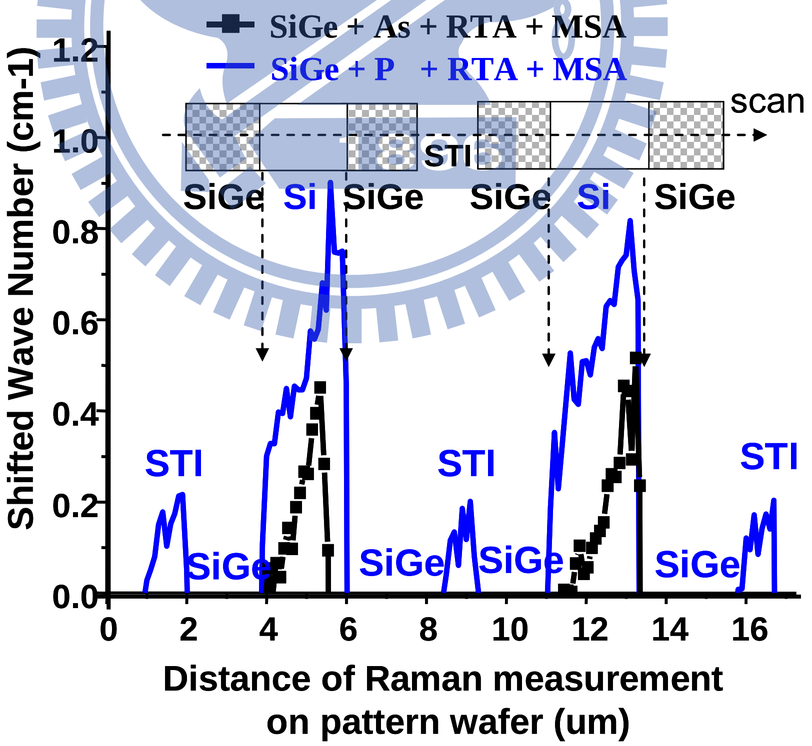


Figure 2.4.11 Raman measurements (wave number shifts) indicated the relaxation of strained-SiGe is associated with post implanted species, As and P, and their effects on the Si channel stress in Si

The 10% higher drive current (Id,sat) gain of PFET devices versus Lmin (minimum gate length) associated with post-SiGe phosphorus due to less strain relaxation of S/D SiGe than that associated with arsenic in Fig. 2.4.12, was consistent with Raman measurements. Fig. 2.4.13 plots the relationship of the dopant species and the junction leakage in PMOSFET devices. Upon RTA and MSA thermal treatment, post-SiGe phosphorus implantation can result in an almost fully strained-SiGe layer and does not form defects in the underlying Si substrate. Minimized the leakage current to a level comparable to those of PMOSFET devices are fabricated using a non-SiGe process.

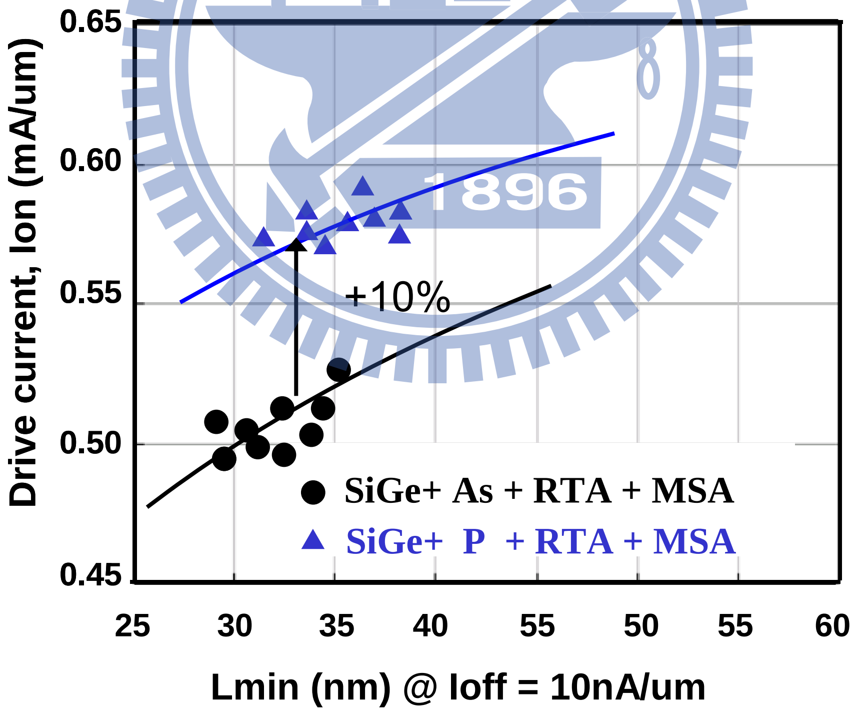


Figure 2.4.12 Drive current, Ion-Lmin was affected by the implanted As and P induced damage effect in the strained-SiGe layer, which causes various degrees of strain relaxation upon the RTA and MSA.

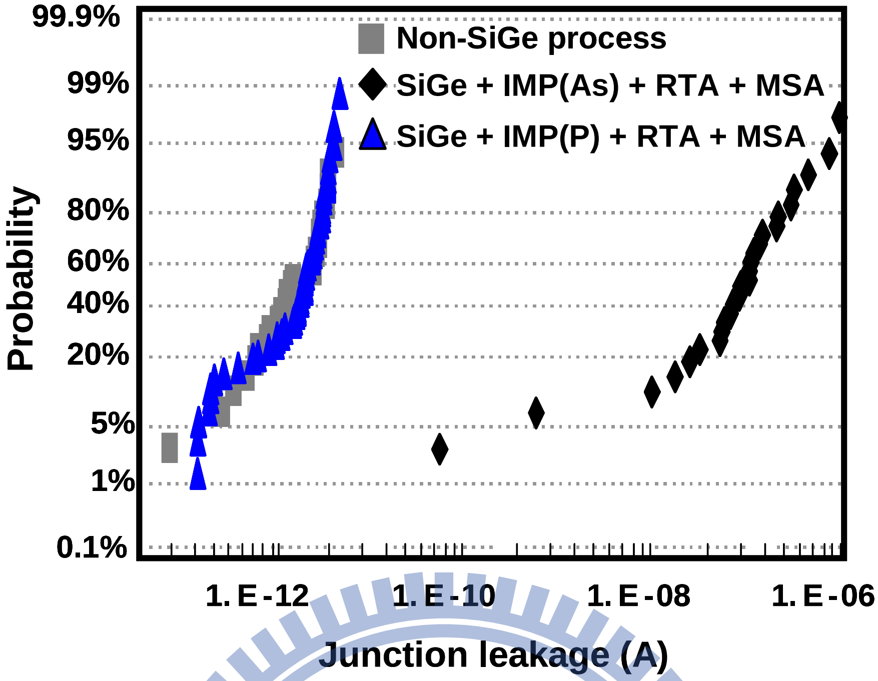
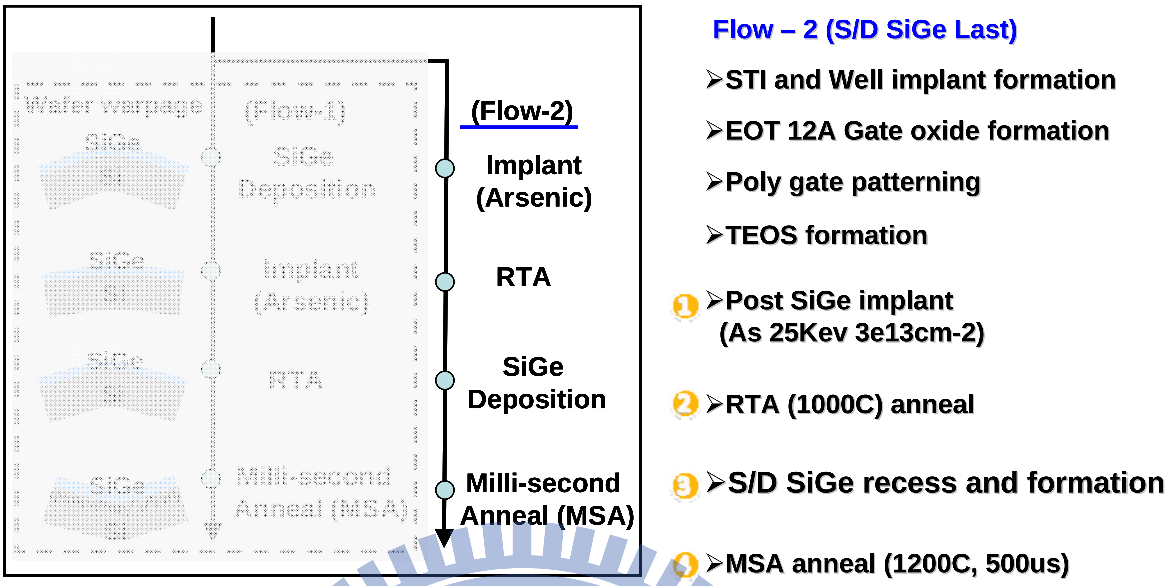


Figure 2.4.13 Improvement in the P+/n well junction leakage by the post-SiGe implantation of species, P, reduces the relaxation of strained-SiGe and yields a defect-free underlying Si substrate upon RTA+MSA.

2.4.3 Implant sequence effect on strain relaxation of S/D SiGe and device performance

On the other hand, changing the sequence of the implantation species, As, from post-SiGe implantation process to Pre-SiGe implantation process, as revealed Flow-2 in Fig.2.4.14, enables a less relaxed strained-SiGe to be achieved, increasing the drive current gain. Figures 2.4.15 and 2.4.16 present the device performance of PMOSFETs and junction leakage current of pre-SiGe implantation sequence. As implantation and RTA process prior to strained-SiGe layer were conducted to present a low level of strain relaxation. MSA did not cause low degree of strained-SiGe relaxation to reveal large wafer warpage change and did not form defects in the underlying Si substrate. Then, PMOSFET devices had an Id,sat gain of



Flow – 2 (S/D SiGe Last)

- ➢STI and Well implant formation
- ➢EOT 12A Gate oxide formation
- ➢Poly gate patterning
- ➢TEOS formation
- ① ➢Post SiGe implant (As 25Kev 3e13cm-2)
- ② ➢RTA (1000C) anneal
- ③ ➢S/D SiGe recess and formation
- ④ ➢MSA anneal (1200C, 500us)

Figure 2.3.14 The Process flow of implantation followed by the S/D SiGe, then subsequent MSA was conducted.

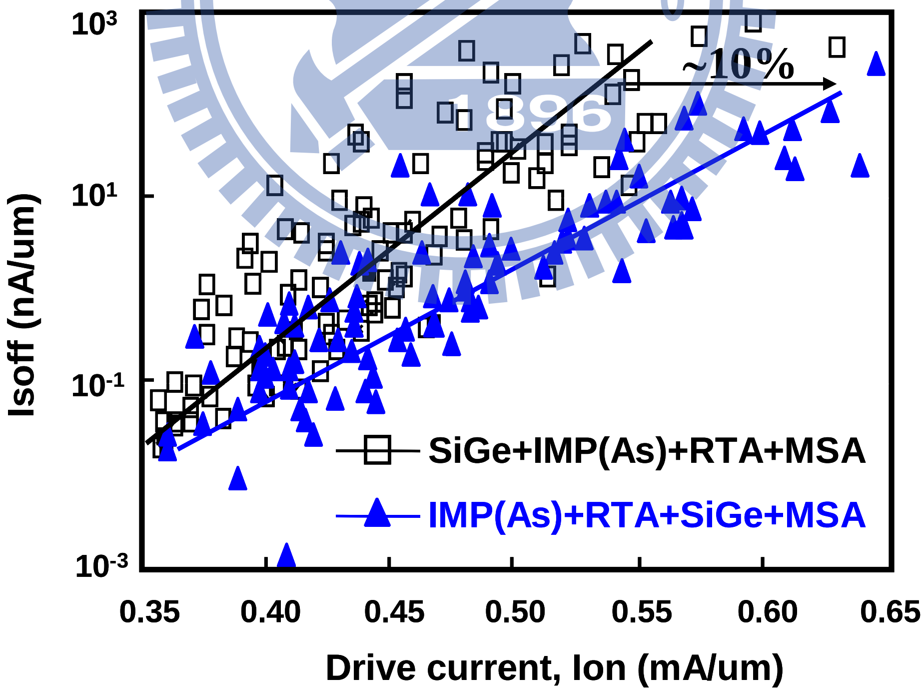


Figure 2.4.15 Improvement of Ion-Ioff by the change in sequence of SiGe and implantation. Implantation prior to SiGe deposition exhibited less strain relaxation and a higher channel stress.

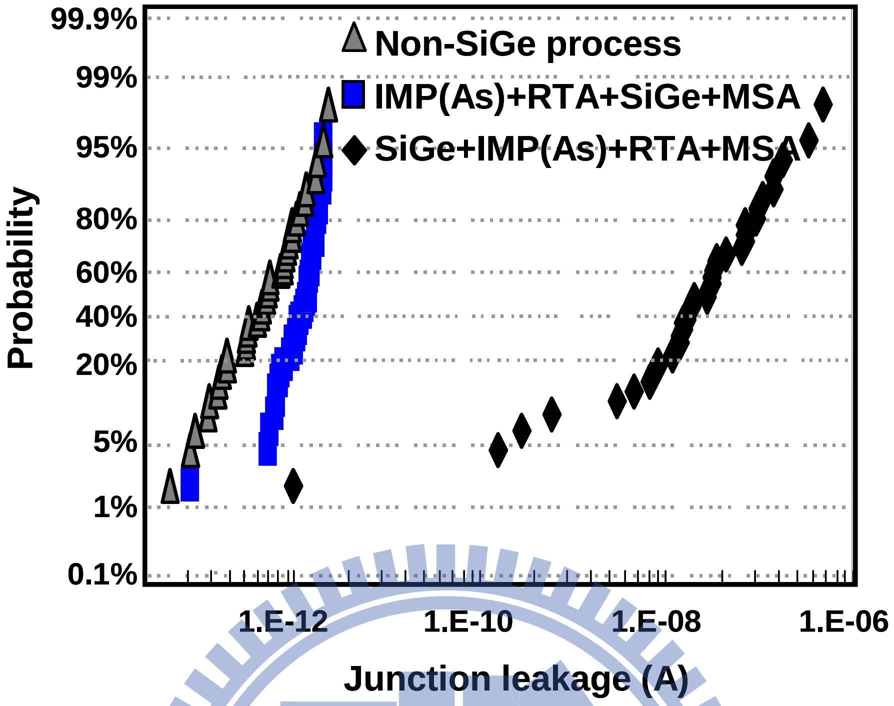


Figure 2.4.16 Upon MSA, implantation following the SiGe process sequence results in low strain relaxation and few defects in the underlying Si, and consequently improved junction leakage.

around 11% due to the low degree of strained-SiGe relaxation because of non-implantation in the strained-SiGe layer and a significantly improved junction leakage than that of those post-SiGe implantation process.

2.5 Mechanism

To understand the formation of defects in the underlying Si during the MSA of implanted strained-SiGe, three implantation conditions - low energy (15keV) of shallower implantation Rp, medium energy (50keV) of medium implantation Rp and high energy (70keV) of deep implantation Rp, made implanted species, As, reach the surface, medium and bottom of the 100nm-thick strained-SiGe blanket wafer, respectively. The three samples with different implantation conditions were followed by RTA and MSA, causing 11%, 51% and 75% relaxation of strained-SiGe. The relaxation percentage of the strained SiGe was calculated from bow height change ratio before implant as well as after implant and RTA. High-resolution X-ray diffraction reciprocal space maps (HR XRD RSMs) [19] were obtained to characterize the relaxation of strain SiGe and the defects in the underlying Si, as shown in Fig.2.4.17(a)(b)(c). For the case of 11% relaxation of strained-SiGe, the MSA did not significantly degrade the lightly relaxed strained-SiGe and did not produce defects in the underlying Si substrate, presented in the TEM image, and as revealed by results of the tight XRD RSM patterns of the Si. In Fig.2.4.17 (b), the medium implantation Rp, RTA process and subsequent MSA caused a 51% strained-SiGe relaxation, which was consistent with a weak SiGe diffraction peak in RSM pattern. MSA of such remarkably relaxed strained-SiGe formed many defects in the underlying Si, as shown in the TEM image, corresponding to the broadening of the Si RSM pattern in the most {111} direction by the defects. Finally, in Fig. 2.4.17 (c), a more deeply implanted Rp, the RTA process and subsequent MSA caused an almost 75% relaxation of strained-SiGe, and produced numerous dislocations in SiGe, which result is related to the very weak SiGe diffraction RSM pattern. MSA applying to a high relaxation of strained-SiGe wafers does not form defects in the underlying Si, as presented in the TEM image, indicating a slightly broadened Si RSM pattern, due to the clarity of the Si.

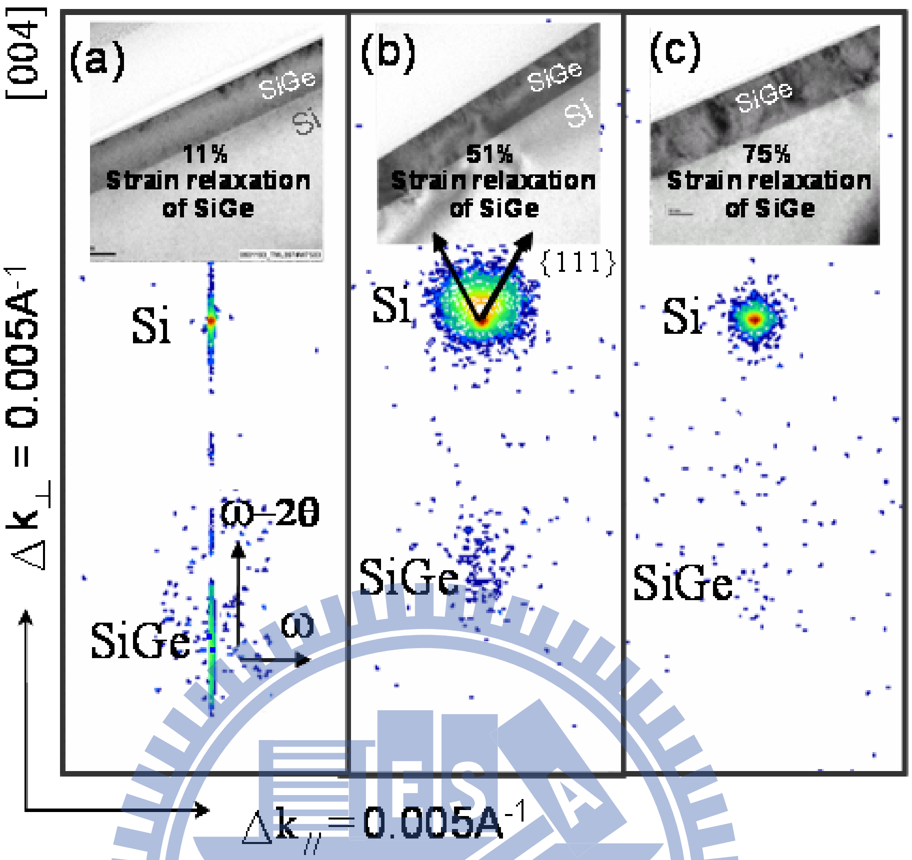


Figure 2.4.17 High-resolution X-ray diffraction reciprocal space maps (HR XRD RSMs) and TEM of strained-SiGe and underlying Si following implantation under various energy and RTA and MSA, associated with various strained-SiGe relaxation (a) No defect formation for 11% relaxation of strain SiGe. (b) Defects in the underlying Si for 51% strained-SiGe relaxation. (c) 75% relaxation shows the almost completely relaxed strained-SiGe with weak diffraction peak, and defect-free in the underlying Si.

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Hence, the degree of strained-SiGe relaxation determines whether defects are formed in the underlying Si substrate under millisecond annealing. Figure 2.4.18 the TEM image reveals that upon MSA, the formation of defects or their injection into underlying Si was observed because strained-SiGe underwent moderately medium strain relaxation. Neither excessively low nor excessively high strained-SiGe relaxation was associated with any defect injection into the underlying Si.

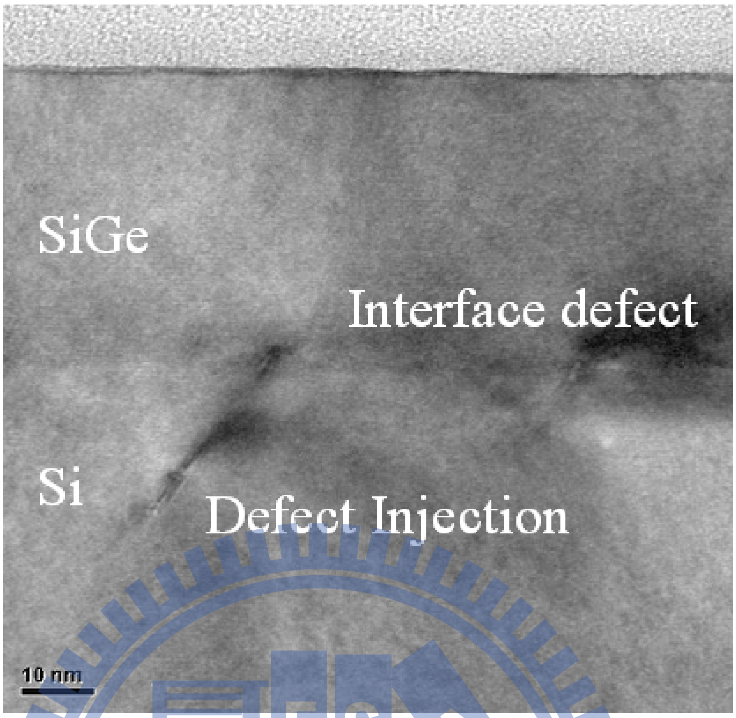

Figure 2.4.18 Upon MSA, TEM image showed that relaxed strained-SiGe caused injection of defects into underlying Si.

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Therefore, Fig. 2.4.19 plots a correlation between the relaxation of strain SiGe and the injection of defects, obtained from the bow height of the SiGe wafer and the corresponding full width at half maximum (FWHM) of the Si XRD peak, respectively [20]. In designing a high performance of CMOS devices with strained-SiGe and MSA, pseudomorphic relaxation of strain SiGe of less than 11% must be maintained to ensure favorable channel stress to boost the drive current and an absence of defect formation in the Si to ensure a low junction leakage current.

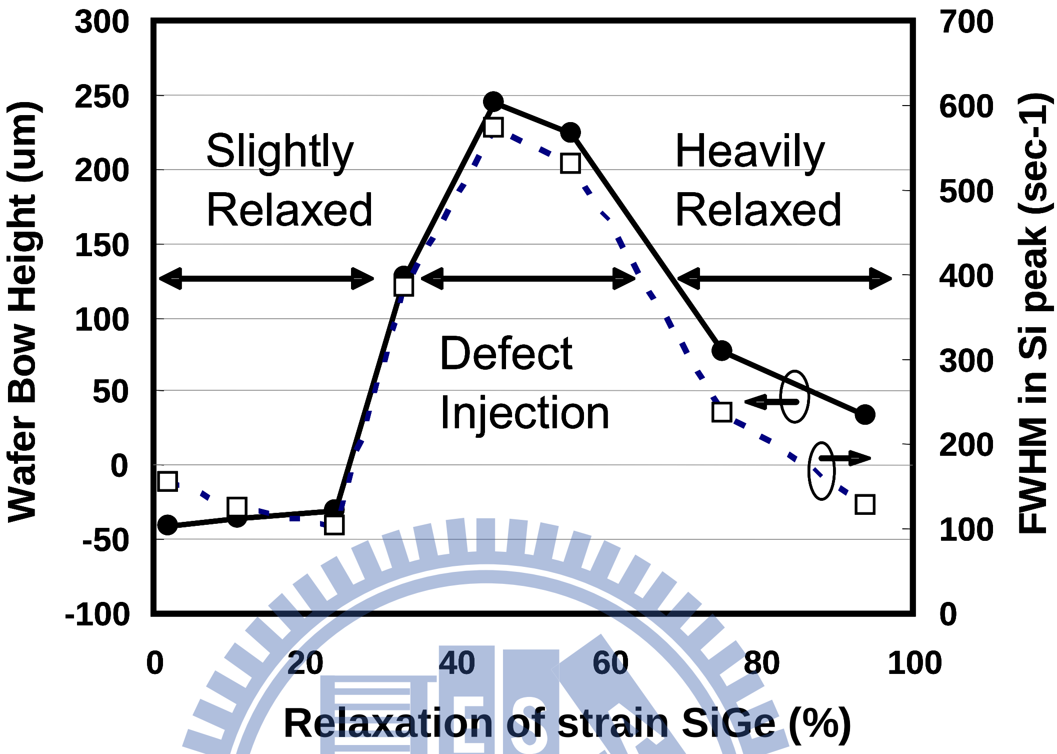

Figure 2.4.19. Correlation between relaxation of strain SiGe and injection of defects, determined from wafer bow height and full width at half maximum (FWHM) of Si XRD peak.

The stress of the strained-SiGe layer on the Si substrate can be calculated using Stoney's well-known equation, which assumes uniform biaxial film stress:[21]

$$\sigma_{SG} = \frac{E_S}{6(1-\nu_S)} \frac{d_s^{\,2}}{d_f} k \quad , \qquad (1)$$

where E_S and ν_S denote the Young's modulus and Poisson ratio of the substrate; d_s is the thickness of the Si substrate; d_f is the thickness of the strained-SiGe layer, and k is the wafer curvature.

When MSA was performed using pulsed surface heating with a millisecond peak width at a temperature of around 1200°C at the surface of the Si wafer without SiGe layer, as shown

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in Fig. 3(b), the very high thermal stress caused by the huge thermal gradient induced very large wafer bending, which can be expressed as, [22]

$$\sigma_{MSA} = \frac{E_{S,T}}{1-\nu_S}\alpha\Delta T \quad , \tag{2}$$

where α is the thermal expansion coefficient; $E_{S,\ T}$ is Young's modulus at the MSA temperature, and ΔT is the effective temperature difference between the surface of the wafer and the position of zero temperature gradient, where $\partial T/\partial x=0$. Since the MSA chamber was thermally insulated, the decrease in the temperature across the Si substrate is given by, [23]

$$T = T_f + A_1 \exp\left(\frac{-x}{x_c}\right), \tag{3}$$

where T_f is the temperature at zero temperature gradient across the wafer. The experimental MSA temperature profile across the surface of the wafer was fitted using parameters T_f, A_1, and x_c set to 490°C, 814°C and 106μm. Therefore, the effective temperature difference due to the thermal gradient is represented by

$$\Delta T = \frac{a}{x_T}[\int_0^{x_T} (T_f + A_1 \exp(\frac{-x}{x_c}))dx - x_T T_f] \quad , \tag{4}$$

where x_T=396μm, and a=0.4 to fit the experimental data in Fig. 3(b). Accordingly, the magnitude of the MSA thermal stress across Si wafer surface was,

$$\sigma_{MSA} = \frac{E_{S,T}}{1-\nu_S}\alpha\frac{a}{x_T}[\int_0^{x_T} (T_f + A_1 \exp(\frac{-x}{x_c}))dx - x_T T_f] \quad .$$

The MSA thermal tensile stress in this experiment at approximately 1200°C for 500μs was thus around 0.6GPa. The thermal stress caused by MSA pulse heat in the Si surface region, d_f, is given by Stoney’s equation,

$$\sigma_{Si} = \frac{E_{S,T}}{6(1-\nu_S)} \frac{d_s^{\ 2}}{d_f} k, \tag{5}$$

The bow height (B) that is induced by stress is,

$$B = \frac{r^2 k}{2}, \tag{6}$$

where r denotes radius of the wafer, and k is the curvature of the wafer. Substituting Eq. (5) into Eq. (6) yields the k value, and the bow height of Si wafer following the MSA process is given by

$$B \approx d_f \left(\frac{r}{d_s}\right)^2 \alpha \Delta T \frac{E_{S,T}}{E_S}. \tag{7}$$

Given the experimental parameters, the change in the bow height of the pure Si wafer without SiGe layer during the MSA process was small, at around few 10µm.

The bow height, however, changed significantly around 150µm when the relaxation of the strained-SiGe was introduced into the MSA process. When both of the film stress and the thermal stress have been determined, the wafers bow height of the strained-SiGe and MSA was as presented in Fig. 10(b). It was modeled using the Gaussian function to obtain an empirical formula to illustrate the bow height change of the SiGe wafer by the compressive stress of the strained-SiGe layer and tensile stress of the MSA, as follows.

$$B = y_0 + \frac{A}{f_{in}\sqrt{2\pi}} \exp\{-2[\frac{b(1-R)\sigma_{SG} - \sigma_{MSA}}{f_{in}}]^2\}, \tag{8}$$

where y_0, A, and b are constants; R is the relaxation of strained-SiGe and f_{in} is the interaction factor,

$$f_{in} = m\sigma_{SG} + n\sigma_{MSA},$$

where m and n are also fitting constants. According to Eq. (8), the bow height reached its maximum when b(1-R)σ_{SG} was close to σ_{MSA}. Therefore, the bow height depended on both the magnitude of the strained-SiGe film stress and the MSA thermal stress. Shallow implant Rp in the surface region would cause only an 11% relaxation of the whole strained-SiGe layer, and the compressive film stress was sufficiently high to resist wafer bending associated with MSA thermal tensile stress. Hence, the bow height was negative as compressive as that of the initial strained-SiGe film. When implantation is performed using medium projection range Rp to induce 51% relaxation of the strained-SiGe, the film stress, σ_{SG}, was reduced by a factor (1-R) showing lower shear yielding stress for deformation during MSA thermal stress as shown in Fig. 2.4.20 [24-29], and was then too small to resist the MSA tensile stress and the relaxed strained-SiGe wafer buckled in the maximum tensile state. This phenomenon is described by a *second moment of inertia* as shown in Fig. 2.4.21 [30-31], which demonstrates that a suddenly large deformation or over-bending occurred when the applied force exceeded a critical stress or over shear stress for yielding. At the experimental condition, while strained-SiGe relaxation is over around 20%, large SiGe wafer bending occurred under applying MSA tensile stress corresponding to the concept of the second moment of inertia.

When deep implantation of Rp destroyed most of the strained-SiGe layer at close to 75% relaxation, the yield-point of relaxed strained-SiGe was further reduced to cause much bending under MSA process. However, the 75% relaxation of strained SiGe was formed with lots of interfacial misfit dislocations and low-density of coherent bonding with Si substrate. The highly relaxed strained-SiGe film is then expanded and contracted along with the externally thermal stress and would not cause any residual strain to the underlying Si substrate during the MSA thermal cycle.

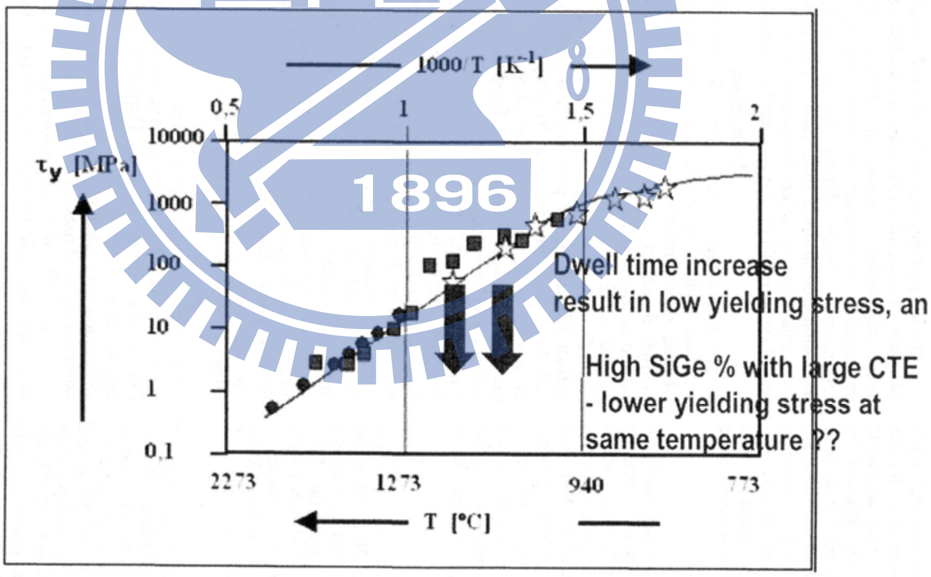

Figure 2.4.20 the shear stress of yielding point of silicon is linearly dependent on the annealing temperature. (S.P. Nikanorov, et. al., Materials Science and Engineering, 2006)

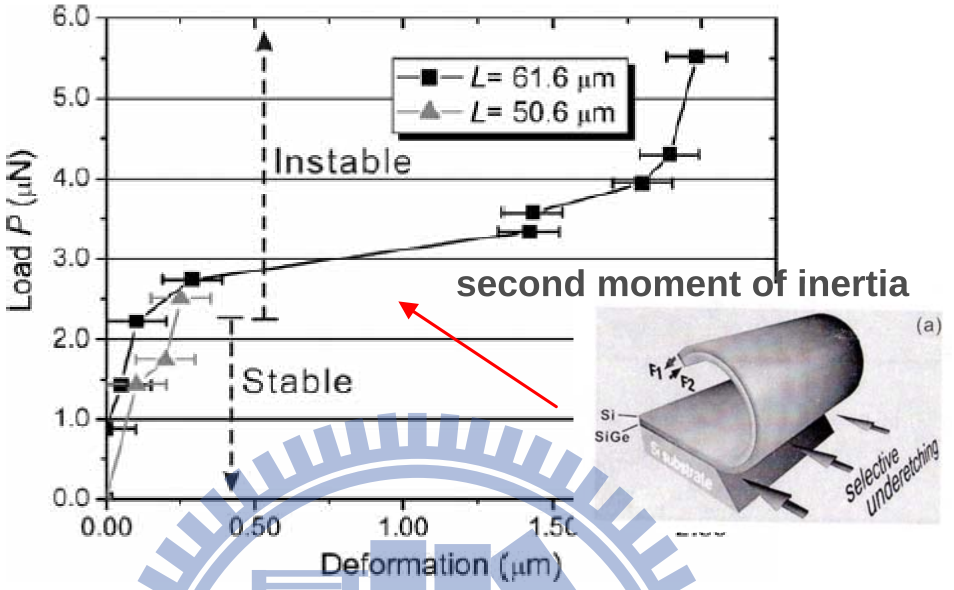

Figure 2.4.21 the second moment of inertia shows large over-bending while external loading over critical point. (L. Zhang et. al. NSTI-Nanotech, 2006)

We would like to investigate for a MSA acting on the relaxation of the strained SiGe when defect formed in the underlying Si substrate and how the wafer underwent such a significant bending during MSA process. The relaxation of the strained SiGe induced defect formation in the underlying Si substrate is taken place during MSA ramp-up or cool-down that is a puzzle for us. A model of MSA temperature ramp-up and cool down acting on a medium-level of relaxed strained-SiGe to caused defect formation in the underlying Si and wafer bending was therefore proposed. In Fig. 2.4.22, by using micro-second camera and comparing wafer shape with the ellipsometer wafer bow height to investigate real-time wafer bending during MSA heating and cooling on the medium relaxed SiGe wafer. The wafer showed a little compressive bending after SiGe deposition at initial stage. At the next stage the coefficient of thermal expansion is greater for SiGe than for Si such that the SiGe layer expanded more than the silicon substrate during MSA surface heating. The surface expansion induced a compressive stress exceeding the lower yielding stress of the relaxed strained-SiGe caused a significant compressive bending approaching wafer bow height near -185um from -30um. Thus, brittle silicon substrate suffered a great tensile stress to generate lots of defects into plastic deformation as shown in Fig. 2.4.23 (a) and (b).

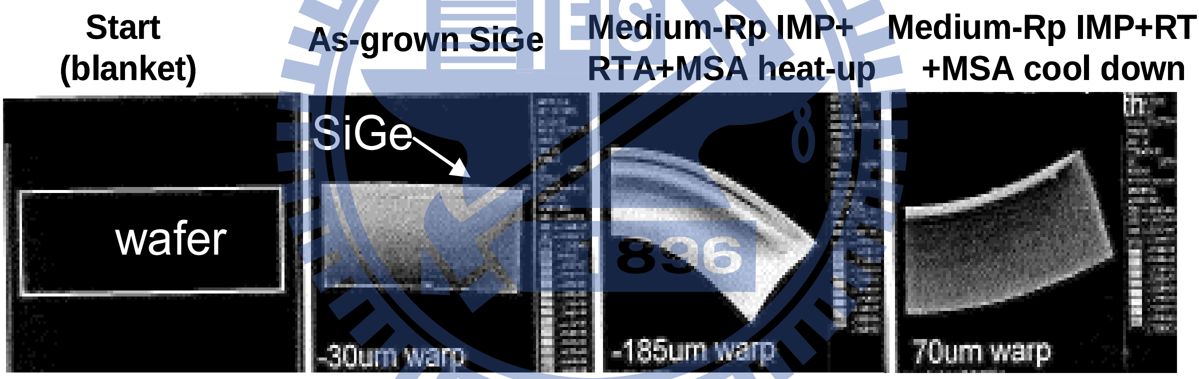

Figure 2.4.22 (a) Real-time micro-second camera image of wafer warpage change associated with as-grown SiGe and the MSA temperature ramp-up and cool down.

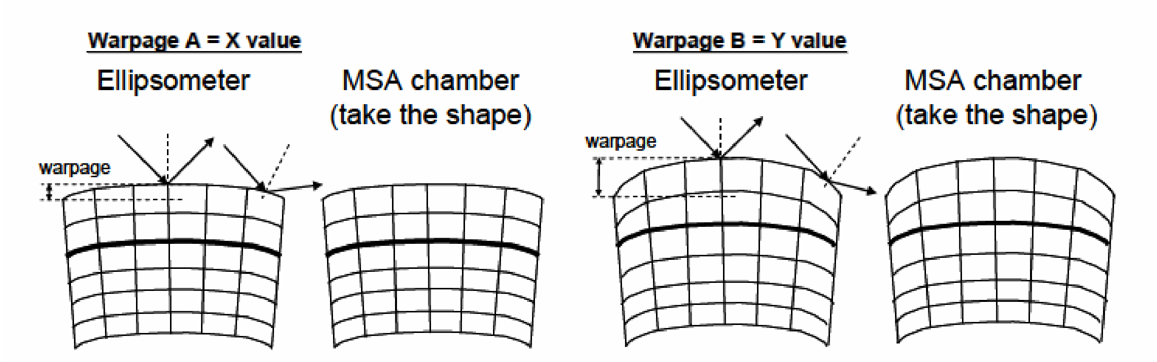

Figure 2.4.22 (b) the metrology concept of how to in-situ measure wafer warpage

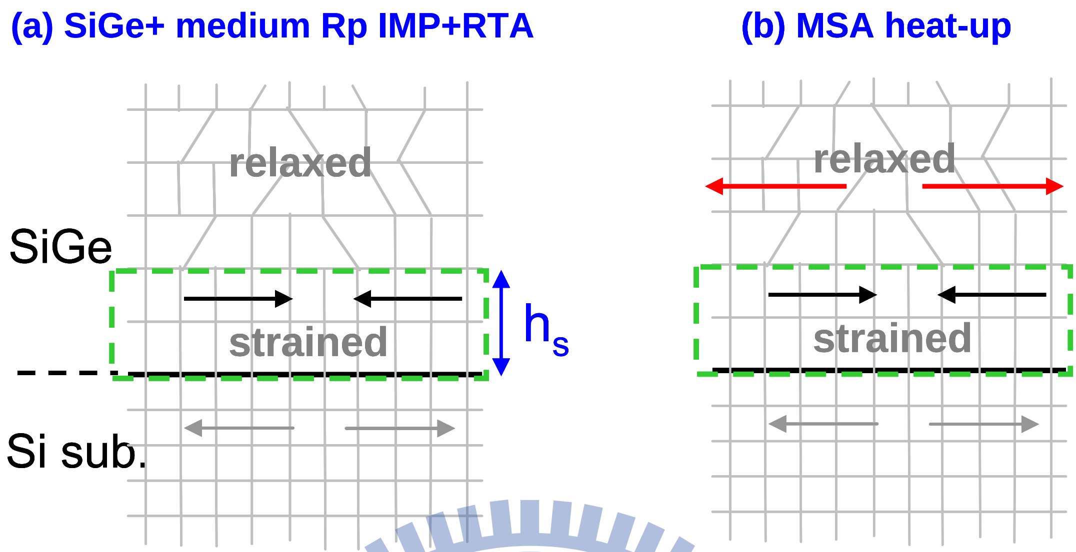

Figure 2.4.23 (a)(b) microscope of lattice deformation during post-implant, RTA and MSA temperature heat-up

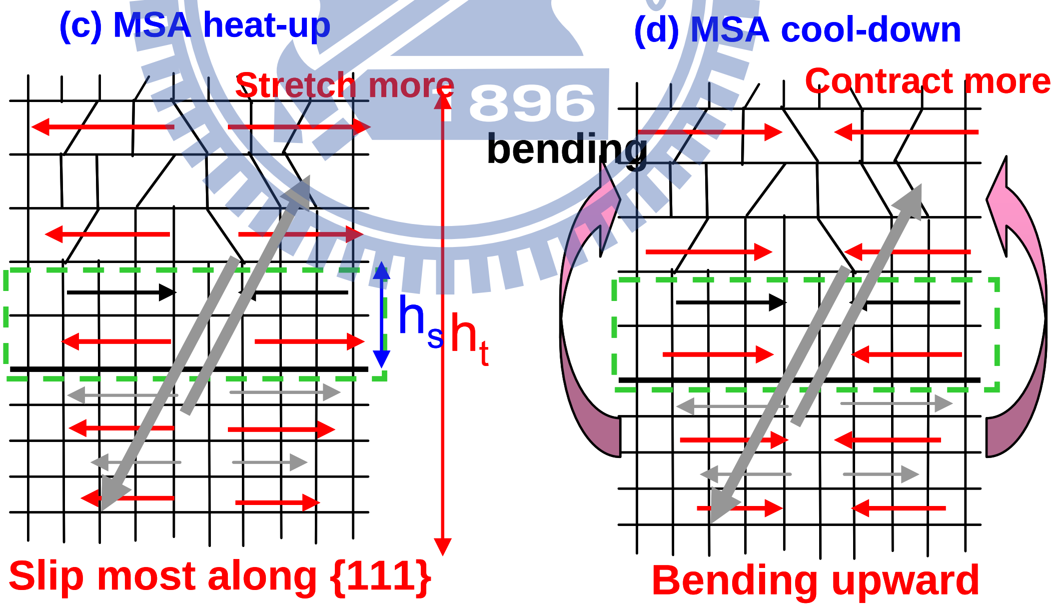

Figure 2.4.23 (c)(d) microscope of lattice deformation and wafer bending during MSA heat-up and MSA temperature cool-down

During MSA cooling the relaxed strained-SiGe wafer at the final stage, the compressive over-bending of the surface relaxed strained-SiGe layer with a significant plastic deformation contracted more than silicon substrate to become highly tensile bending approximate 70um as shown in Fig.2.4. 22 (a), Fig. 2.4.23 (c) and (d) while MSA temperature cooled down. Hence, defect formation in the underlying Si substrate for a medium relaxation of the strained SiGe wafer in the MSA temperature ramp-up step and a significant wafer bending from compressive state to highly tensile state took place during MSA temperature cooling down step.

Fig. 2.4.24 schematically plots the mechanism of the MSA effects on the various implanted strained-SiGe wafers. When the damaged amorphous layer (α layer) by implantation was near the strained SiGe surface, corresponding to shallow implantation Rp, the remained thick and good crystalline strained-SiGe with high yielding stress of deformation can resist the compressive stress of the surface expansion during MSA heat up and the tensile stress of the surface contract during MSA cooling. Therefore, there is no defect formation in the underlying Si substrate as well as no wafer bending to tensile state. However, once the damaged PAI reached to a medium Rp, the remarkably relaxed strained-SiGe with relatively lower yielding stress of deformation followed with RTA would led to a too-thin strained-SiGe to withstand the large thermal stress during MSA. Meanwhile, the underlying Si substrate encountered a tremendous tensile stress during MSA temperature heating up, resulting in defects in the underlying Si along {111} lowest energy slip planes and wafer bending from compressive to tensile state during MSA cool down. Furthermore, high-energy implant with a deep Rp to the SiGe/Si interface would form a significantly relaxed SiGe with numerous interfacial misfit dislocations and low-density of coherent bonding with Si substrate. The highly relaxed strained-SiGe film is then expanded and contracted freely along with the externally thermal stress and would not cause any residual strain to the underlying Si substrate during the MSA temperature heating up and cooling down. Hence, highly relaxed strained SiGe over 75% would not also cause defect formation in the underlying Si substrate and significant wafer bending from compressive to tensile state.

As a result, we know how to control the relaxation degree of strained SiGe and the mechanism of defect formation in the underlying Si substrate and significant wafer bending during MSA cycle. A good process design for strained SiGe source/drain to boost device performance and to avoid defect formation in the underlying Si substrate resulting in junction leakage current is established for 28 nm node PMOSFETs.

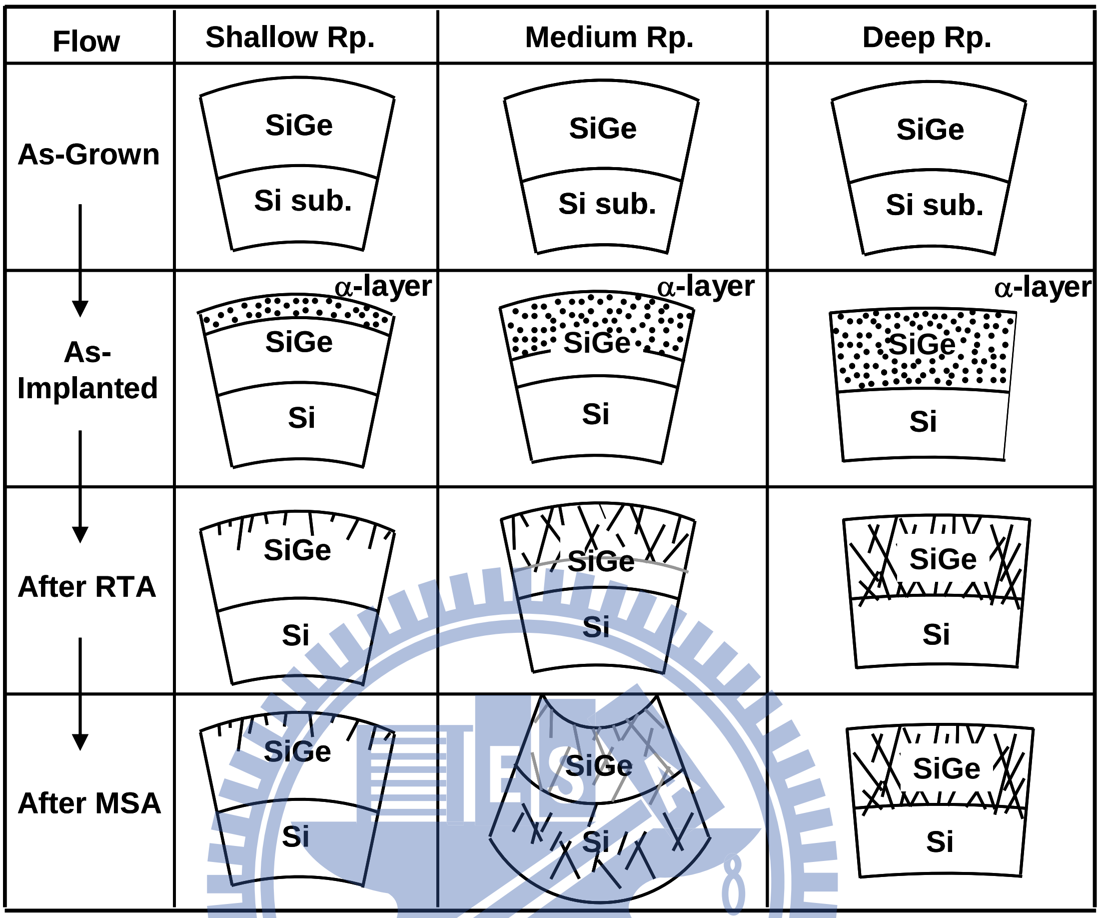

Figure 2.4.24 Schematic plot of various implantations Rp to thickness of SiGe layer, change in wafer bow height and resultant injection of defects in underlying Si substrate.

2.6 Summary

The degree of strained-SiGe relaxation importantly affected the channel stress and the formation of defects in the underlying Si substrate as well as wafer bending when MSA was applied to the S/D strained-SiGe in 28nm PMOSFET devices. Low-energy As implantation to cause shallower Rp in the strained-SiGe surface induced low-level 11% of relaxation and did not generate defects in the underlying Si, because the remaining strained-SiGe was sufficiently thick to resist wafer bending by the tensile stress associated with MSA thermal treatment. However, moderate relaxation 51% of the strained-SiGe by medium-energy As implantation revealed the partly relaxed SiGe with lower shear stress of yielding deformation was unable to withstand the significantly compressive stress of the surface expansion to form defects in the underlying Si substrate during MSA heating and more surface contraction of high CTE of SiGe to cause over-bending in the tensile state during MSA cooling. In addition, the 75% relaxation of the SiGe layer by high-energy implantation would for lots of interfacial misfit dislocations and low-density of coherent bonding with Si substrate. The highly relaxed strained-SiGe film is then deformed freely along with the externally thermal stress direction and would not cause any residual strain to the underlying Si substrate during the MSA thermal cycle. Therefore, proper implantation conditions were chosen to provide a relaxation-less strained-SiGe and boost the channel stress, achieving a 10% current gain. The defect-free underlying Si in millisecond-annealed 28 nm PMOSFETs devices exhibits a decrease in the junction leakage current by four orders of magnitude.

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Chapter 3

Relaxation of strained SiGe by post-Implant, thermal and Ge content following millisecond anneal induced wafer bending and defects in the Si

3.1 Introduction

Strain engineering has been widely used to improve the CMOS device performance in past few years. Epitaxially SiGe is generally used in PMOSFET source/drain region to introduce compressive strain, enhancing the channel carrier mobility and increasing the drive current. Moreover, millisecond annealing (MSA, flash or laser annealing) [1-4], is associated to promote the dopant activation with less dopant diffusion to control short channel effect and enhance drive current to approach higher performance CMOS device. However, the relaxation of strained-SiGe induced by large thermal gradient of MSA may make such the integration challenging [5-9]. Defect formation in the underlying Silicon substrate resulting from the combination of relaxed strained-SiGe and subsequent MSA processes was elucidated [10].

The high Ge-content or post-SiGe anneal induced dislocation in the SiGe layer. The dislocation formation energy was calculated and the critical thickness of strained SiGe layer was defined as shown in Fig. 3.1.1 and Fig.3.1.2, respectively. Therefore, one can obtain

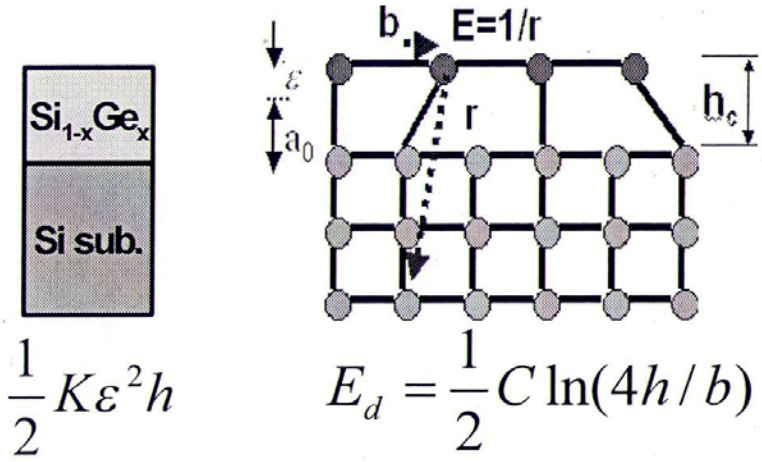

Figure 3.1.1 Single dislocation energy while dislocation formed in SiGe layer

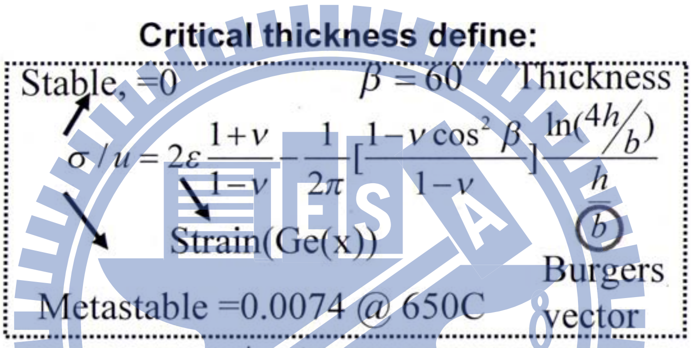

Figure 3.1.2 dislocation formed in SiGe for energy required in equilibrium. (J.Y. Tsao, et.al. PRL, 1986)

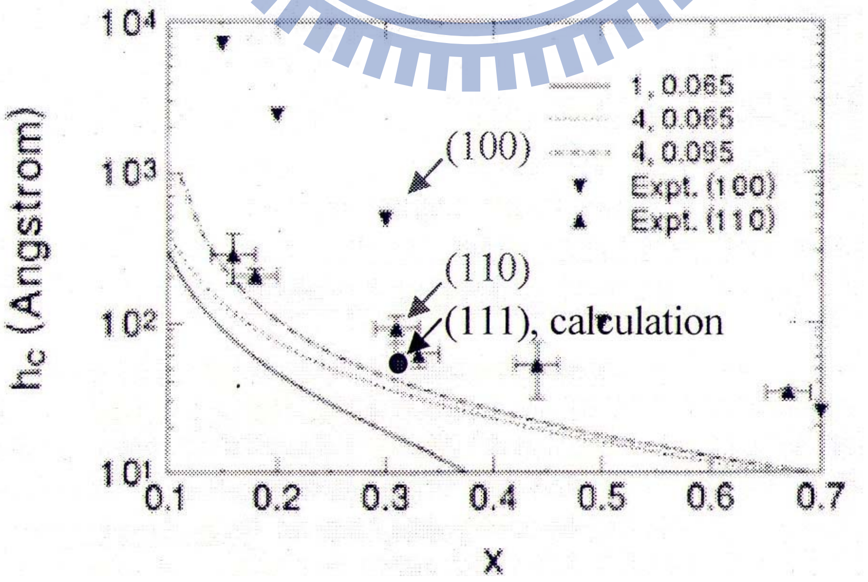

Figure 3.1.3 Critical thickness of SiGe Ge content for different lattice plane (111), (110) and (100). (J.Y. Tsao, et.al. PRL, 1986)

dislocation formation dependency of lattice planes. Knowing the dislocation formation and preventing it in the combination of SiGe and MSA in the process flow is crucial for 28nm PMOSFETs.

3.2 Motivation

Epitaxial SiGe at source/drain (S/D) region for pFETs drive current enhancement has been pursued aggressively in scaled CMOS technologies and significant carrier mobility enhancement at strained Si channel have been reported. Increasing Ge concentration in the S/D SiGe region is a straightforward method for device performance boosting as PFETs scaling down. However, Ge content is inevitable to continuous increment in the S/D SiGe due to the critical thickness effect that increasing Ge content in the S/D SiGe would cause relaxation by forming misfit dislocation in the interface of SiGe and Si substrate as shown in Fig.3.2.1. Furthermore, post-SiGe thermal would also cause relaxation of strained SiGe by revealing dislocation propagation along (111) lattice plane as shown in Fig.3.2.2 as well as post-implantation induced relaxation of strained SiGe mentioned in the last chapter.

In order to meet target of device performance for the technology generation, suppressing the high Ge-fraction induced dislocation formation of epitaxial SiGe at S/D region and post-SiGe implantation and thermal process caused relaxation of strained SiGe are very

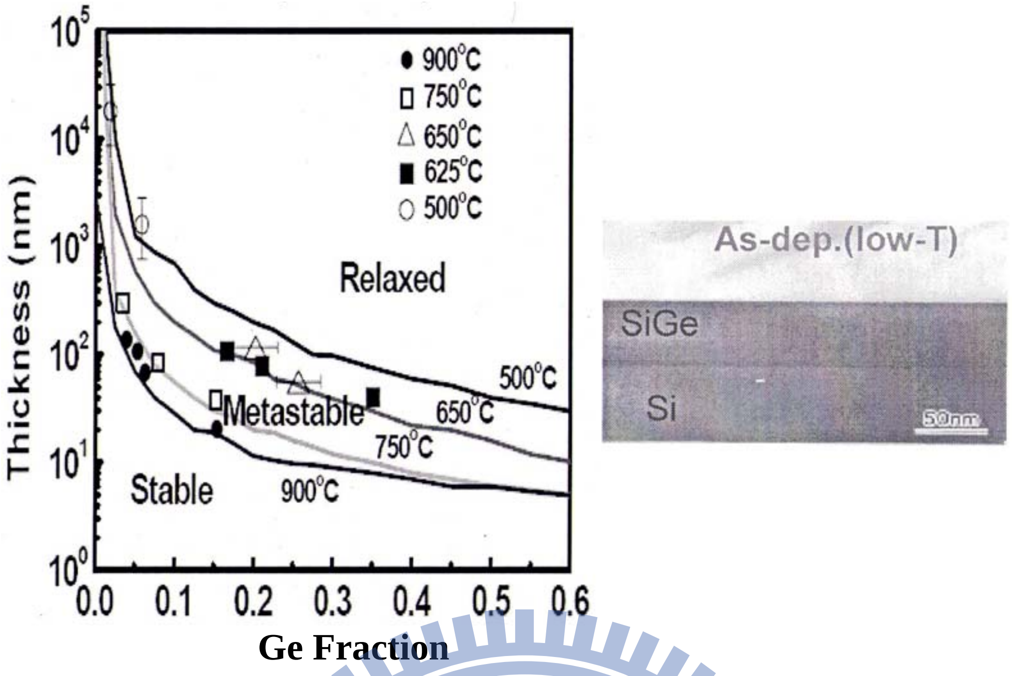

Figure 3.2.1 The strained-SiGe Ge fraction and temperature effect on strained SiGe thickness and its strained SiGe TEM image. (D.C. Houghton, et. al, JAP, 1994)

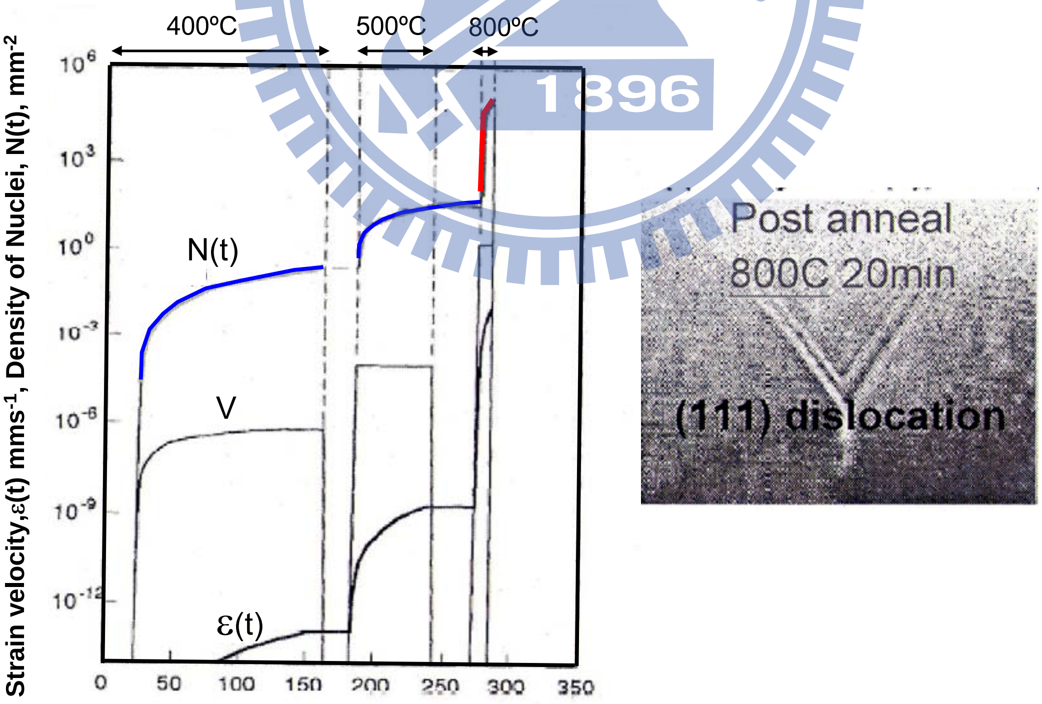

Figure 3.2.2 Dislocation propagation at high post-SiGe anneal temperature and its TEM image. (D.C. Houghton, et. al, JAP, 1994)

important for 28nm CMOS volume production.

In this work, three methods including post-SiGe implant, post-SiGe soak anneal and higher Germanium (Ge) content, would cause relaxed strained-SiGe and defect formation during the subsequent MSA are investigated.

3.3 Experiments

Three process flows of strained SiGe wafers with MSA to study wafer bow change and defect formation were shown in Figure 1. In the Fig.3.3.1-flow (a), the strained $Si_{1-x}Ge_x$ (x~0.35) with 100nm-thick layers were deposited on a series of 300 mm (001) p-type Si wafers of 5–10 ohm-cm nominal resistivity. The SiGe wafers were implanted by Arsenic with various implant energy conditions, from shallow to deep project range (Rp), at energy range from 15KeV to 75KeV with dose of 3E13cm^{-2}. Implanted strained SiGe wafers following spike rapid thermal annealing (RTA) around 1000°C were then carried out to recover the damage. The different relaxation levels of strained-SiGe wafers were conducted by laser MSA annealing at around 1200°C for 500μs. In the flow (b), four Si wafers were deposited with different Ge content of strained $Si_{1-x}Ge_x$ (x~0.2, 0.27, 0.33, 0.4) with about 100nm-thick layer. Those four wafers were implanted using Arsenic (As), at energy of 50keV and a dose of 3E13cm^{-2}. Same as flow (a), RTA were then carried out to recover damage induced by implantation. The relaxed SiGe wafers were following with laser MSA annealing. In the flow (c), 4 SiGe samples of fixed Ge content (35 at.%) were carried out to conduct different soak annealing 800°C, 60sec, 600sec, 900sec, and 1200sec, respectively. Then those four wafers were only directly conducted by the same laser MSA annealing to study the bow height change.

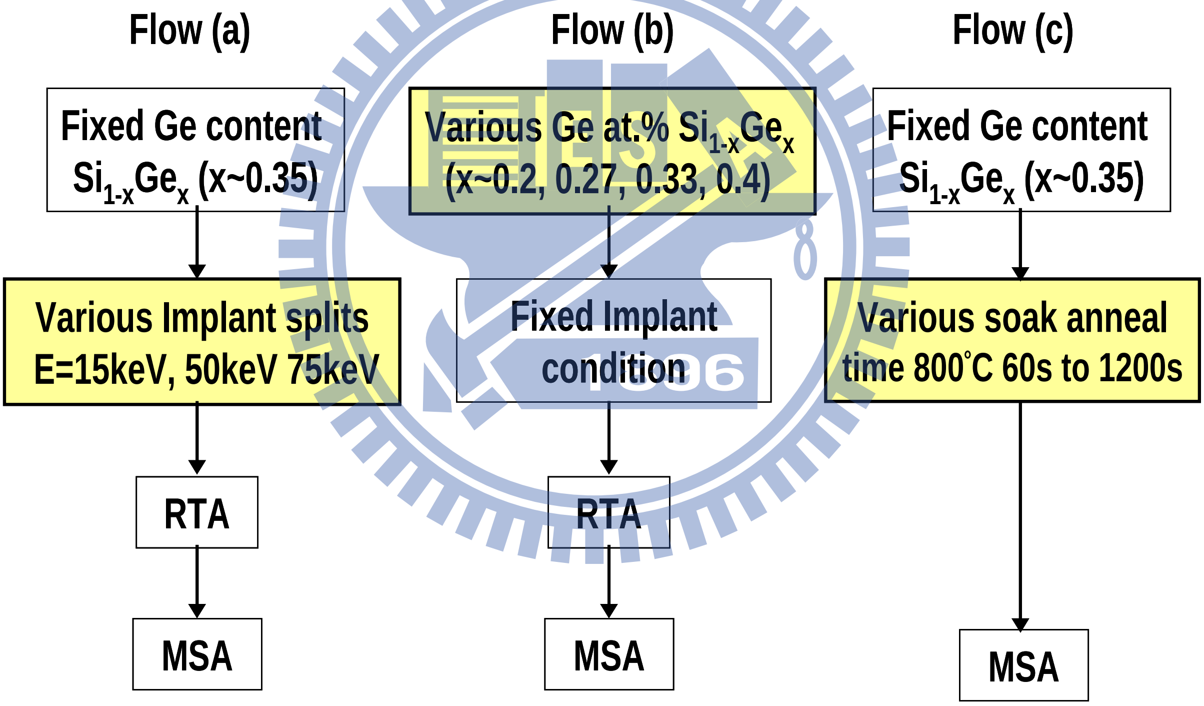

Figure 3.3.1 Process flow of the relaxation of strained SiGe associated to (a) various implant conditions, (b) various Ge contents SiGe, and (c) various soak anneal time

3. 4 Results and Discussion

3.4.1 Implant effect on relaxation of strained SiGe

In figure 3.4.1, the bow height change of stained SiGe wafer with subsequent implant, RTA and laser MSA annealing process is revealed. At initial stage a 100nm-thick layer strained-$Si_{1-x}Ge_x$ (x nearly~0.35) was deposited and it introduced a compressive film stress. Then the subsequent implantation process, by using Arsenic (As) with medium projection range (Rp) near 40nm with an energy of 50keV and a dose of 3E13cm^{-2} , damaged an upper portion of strained SiGe layer and caused partial relaxation, in which bow height changed to less compressive state. Following spike RTA treatment could not fully recover the damaged strained-SiGe and still kept the wafer in compressive state near -20um. The subsequent MSA caused significant SiGe wafer bow height from compressive to highly tensile state near 150um. The TEM image showed significant defect formation in the underlying Si substrate. For comparison, a strained-SiGe sample directly underwent MSA process and it did not cause significant bow height change and still maintained SiGe wafer at compressive state. The TEM image shows that no defect is formed in strained SiGe film and underlying Si substrate. That indicates upon MSA only certain level of relaxation of strained SiGe wafer results in significant bow height change from compressive to high tensile state and defect formation in the underlying Si substrate. In contrast, non-relaxed strained SiGe upon MSA did not show obvious bow height change.

Fig. 3.4.2 plots a correlation between the relaxation of implanted strained-SiGe during MSA and the bow height change of the SiGe wafer. The three SiGe samples with low, medium and high Rp implantation conditions were followed by RTA, causing 11%, 51% and 75% relaxation of strained-SiGe, respectively. For the case of 11% relaxation of strained-SiGe, the MSA did not significantly degrade the lightly relaxed strained-SiGe keeping bow height in compressive state and did not produce defects in the underlying Si substrate shown as in the TEM image. The medium implantation Rp, subsequent RTA process caused a 51% relaxation of strained-SiGe. MSA at such remarkably relaxed strained-SiGe caused significant bow height change from compressive to tensile state and formed many defects in the underlying Si, as shown in the TEM image. Finally, a more deeply implanted Rp, the RTA process caused an almost 75% relaxation of strained-SiGe, and produced numerous dislocations in the SiGe film. MSA applying to a high relaxation of strained-SiGe wafer resulted in bow height at less tensile state and did not form defects in the underlying Si, as presented in the TEM image. In designing a high performance of CMOS devices with strained-SiGe and MSA, pseudomorphic relaxation of strain SiGe of less than 11% must be maintained to ensure favorable channel stress to boost

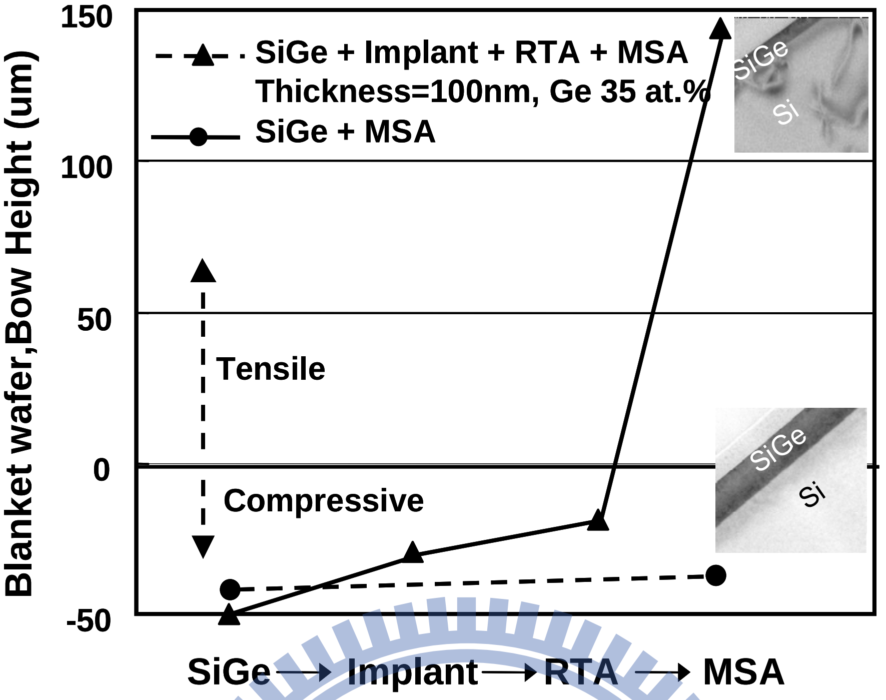

Figure 3.4.1 Bow height change of strained-SiGe wafer associated with following implant, RTA and subsequent MSA, causing large SiGe wafer bending. A fully strained-SiGe sample directly underwent MSA, exhibited no wafer bending

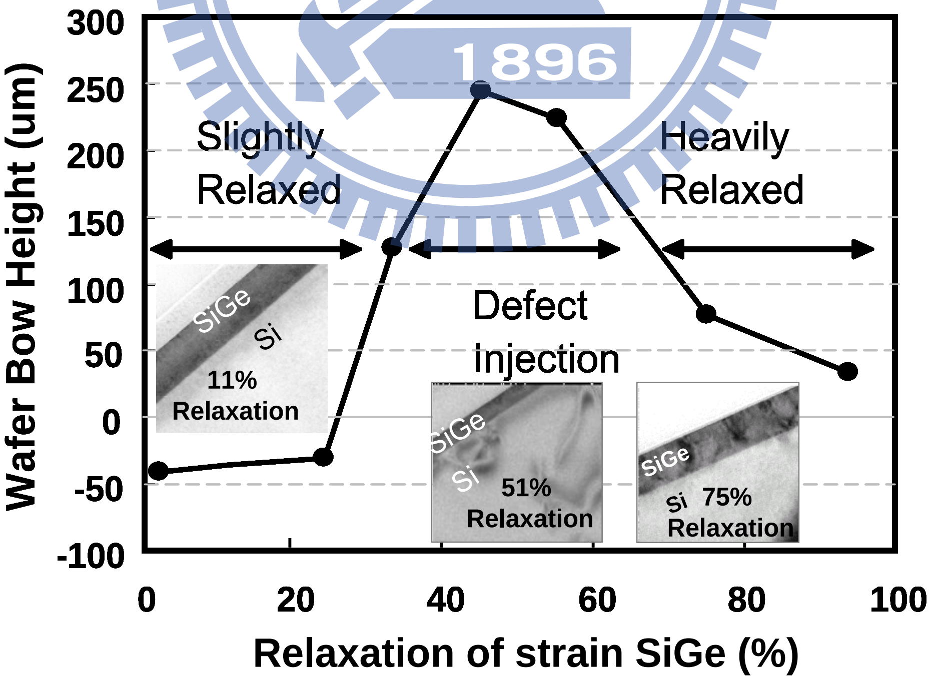

Figure 3.4.2 Correlation between the relaxation of strained SiGe and injection of defects, determined from wafer bow height.

the drive current and an absence of defect formation in the Si to ensure a low junction leakage current.

3.4.2 In-situ doped Ge content effect on relaxation of strained SiGe

To investigate how high Ge at.% of SiGe can be achieved to avoid strain relaxation and defect formation during MSA process in advanced nano devices, four strained $Si_{1-x}Ge_x$ samples (x=0.2, 0.27, 0.33, and 0.44) and their interaction with MSA are explored. Fig.3.4.3 plots step-by-step bow height change of four SiGe wafers with different Ge content, subsequent implant, RTA and laser MSA annealing process flow. Higher Ge content showed higher compressive bow height than that of lower Ge content. After the subsequent medium Rp of Arsenic at energy of approximately 50keV and a dose of 3E13cm^{-2}, then high Ge content of strained SiGe wafer lose most of initial compressive stress. RTA is unable to recover back to original as-deposited bow height state and the strain loss is 64%. In contrast, the other three Ge 20 at.%, 27 at.% and 33 at.% of SiGe wafers loss their strain of 10%, 29% and 50%, respectively. After MSA step, Ge27 at.% of strained SiGe wafer revealed the largest bow height change among those conditions. Fig.3.4.4 shows the same phenomena of various relaxation degree of strained SiGe with different Ge content and their interaction with MSA causing large wafer bow change. It indicates Ge content near 27 at.% on blanket

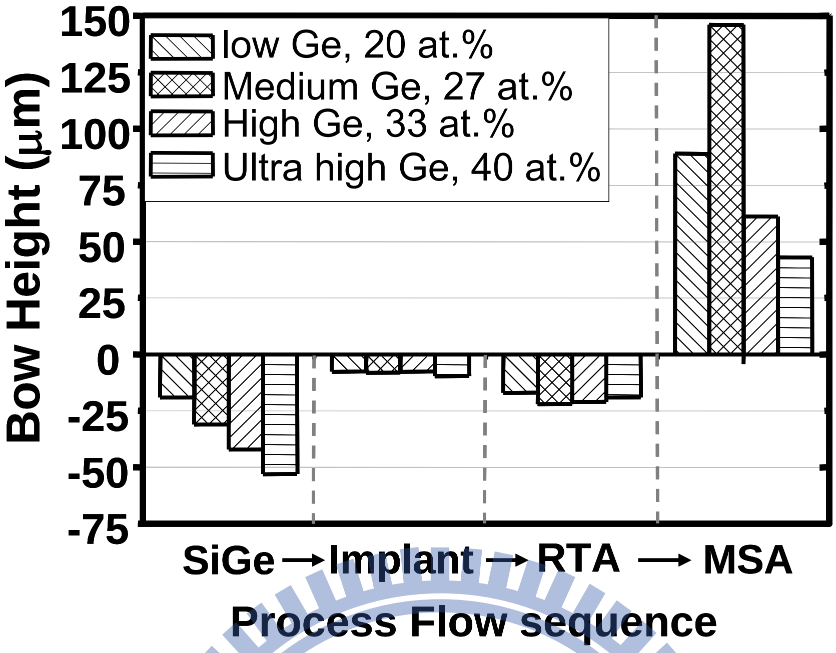

Figure 3.4.3 Bow height change of four Si wafers with following $Si_{1-x}Ge_x$ deposition (x=0.2, 0.27, 0.33 and 0.44), implant of Arsenic, spike rapid anneal (RTA), and laser MSA annealing.

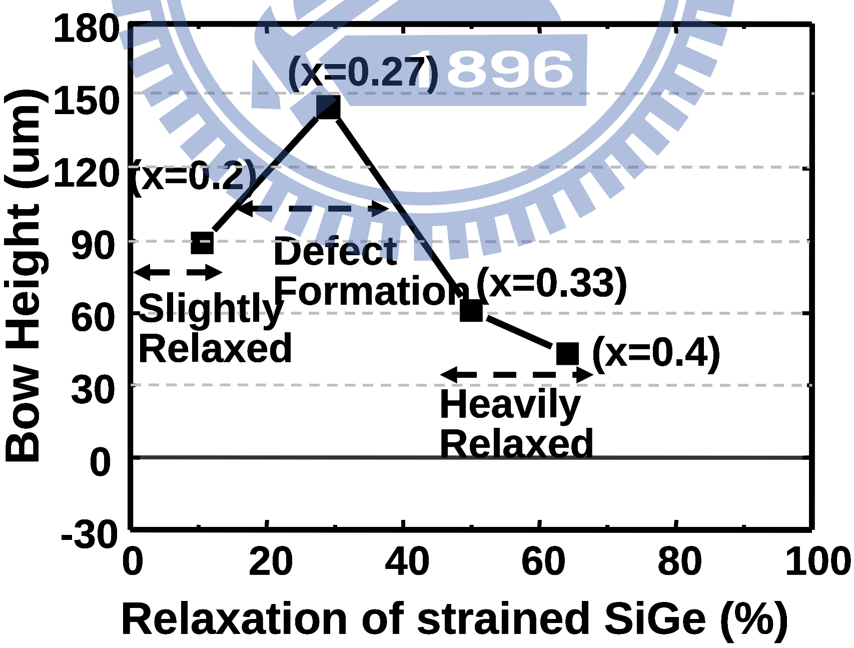

Figure 3.4.4 Correlation between the relaxation of strained SiGe and wafer bow height after laser MSA annealing.

wafer would cause about 35% relaxation of strained SiGe and induce large wafer bending during MSA.

3.4.3 Post-SiGe soak anneal effect on relaxation of strained SiGe

Fig.3.4.5 reveals the post-SiGe soak annealing effect on relaxation of strained $Si_{1-x}Ge_x$ (x~0.35) and its interaction with MSA causing dramatic wafer bow change. Post-SiGe implant causes damage at the upper portion of strained SiGe layer, instead post-SiGe soak anneal makes strained-SiGe relaxed by forming misfit dislocations at interface of SiGe/Si substrate. The four SiGe samples with the subsequent soak annealing 60sec, 600sec, 900sec, and 1200sec at 800°C caused 12%, 35%, 63%, and 74% relaxation of strained SiGe, respectively, then were directly followed by MSA to study the phenomena of large wafer bending and defect formation. The strained SiGe wafers with soak annealing 800°C of 60sec resulted in 12% relaxation of strained SiGe. Upon MSA, bow height was measured -15um in compressive state. No defect formation was observed in the underlying Si substrate as shown in the TEM picture of Fig. 3.4.6 (a). The strained SiGe wafer with soak annealing 800°C of 900sec resulted in 63% relaxation with SiGe surface migration. Upon MSA, bow height turned to high tensile state, up to 415um. The TEM image in Fig.3.4.6 (b) obviously shows the defect formation not only in SiGe film but also in underlying Si substrate. Finally, a longer soak annealing time caused an almost 74% relaxation of strained-SiGe, but the post MSA caused bow height to less tensile state with 365um. Hence, the relaxation at upper portion of strained SiGe layer by implant or relaxation from interface of SiGe/Si by post-soak anneal is not the key factor to cause wafer bow change during MSA, the relaxation degree of strained SiGe is the key to cause significant wafer bending during MSA. Therefore, thermal budget larger than 800°C/60sec to prevent relaxation over 10% is necessary to be carefully integrated in strained SiGe, soak annealing and following MSA processes.

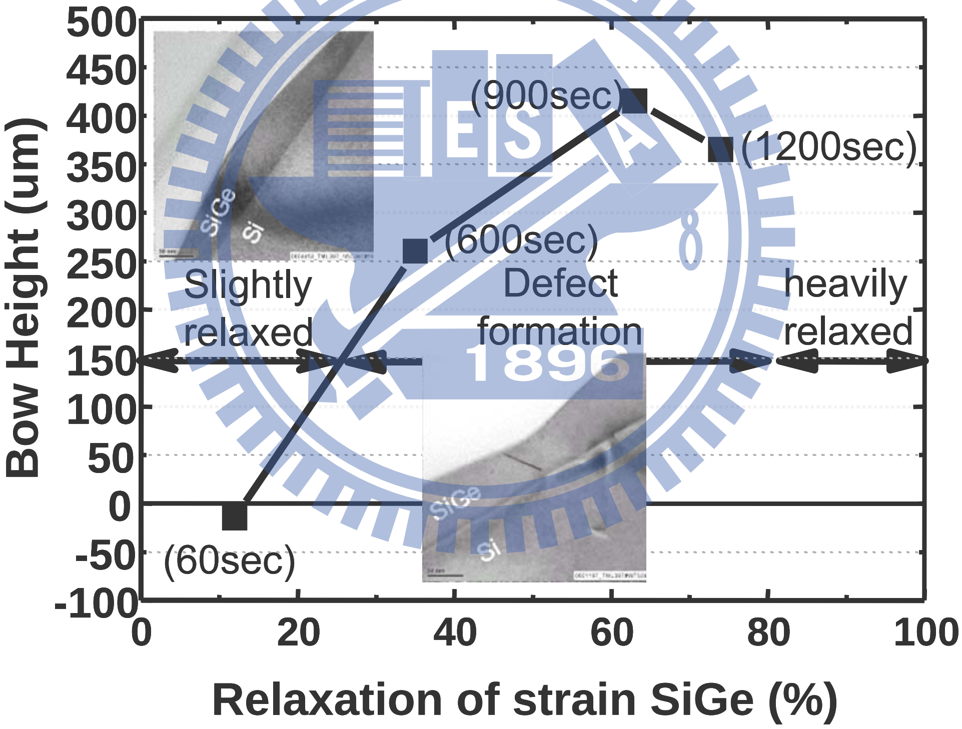

Figure 3.4.5 Upon MSA, correlation of bow height change and post-SiGe various soak thermal annealing causing relaxation of strained-SiGe. Medium relaxation of strained-SiGe by post-SiGe soak annealing also caused defect formation in the underlying Si substrate.

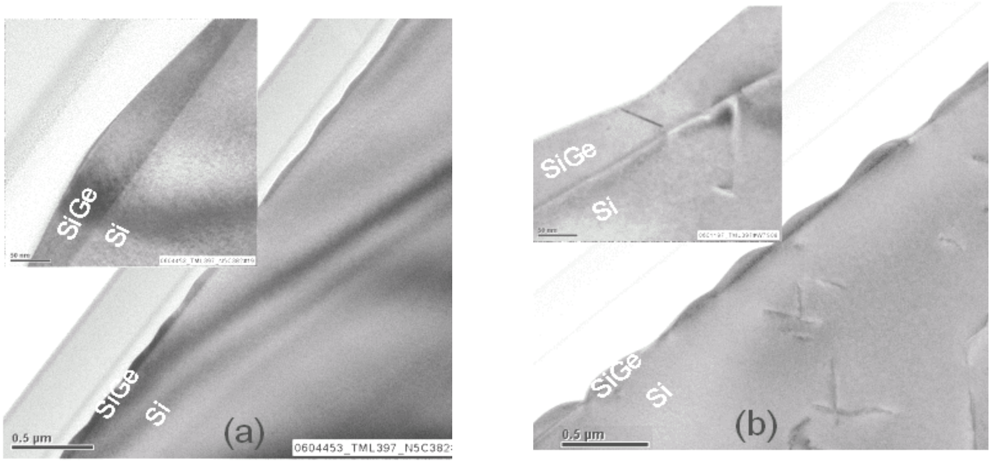

Figure 3.4.6 upon MSA, different degree of strained-SiGe relaxation caused by post soak anneal (a) 12% relaxation of strained SiGe did not show defects in Si (b) 36% relaxation of strained SiGe showed defects in the underlying Si

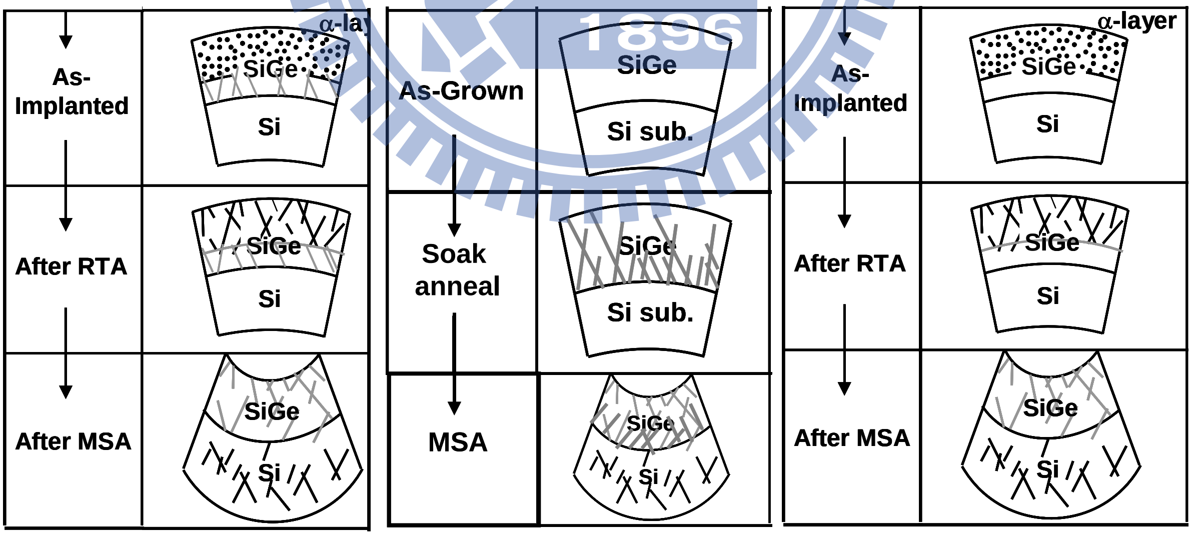

Figure 3.4.7 The schematic plot of in-situ Ge content, soak anneal and implant effect on defect formation in the underlying Si during MSA

The schematic plot of in-situ Ge content, soak anneal and implant effect on defect formation in the underlying Si during MSA as shown in Figure 3.4.7. All of the three methods including in-situ Ge fraction, post-SiGe implant and thermal anneal caused relaxation of strained SiGe and defect formation in the underlying Si substrate during MSA. The key message we need to know is the relaxation degree of strained SiGe to cause defect formation, instead of what methods used to cause relaxation. Therefore, suppressing the total relaxation level of strained SiGe below 10% is important to avoid defect formation in Si for 28nm PMOSFETs volume production.

3.5 Summary

We have concluded that the degree of strained-SiGe relaxation importantly caused wafer bending as well as the defect formation in the underlying Si substrate when MSA was applied to the relaxed strained-SiGe wafers. In either cases of post-SiGe implant or post-SiGe soak annealing or in-situ Ge at.% resulting in relaxation of strained SiGe, low relaxation less than 10% did not cause large SiGe wafer bending during MSA. Upon MSA medium relaxation level indeed caused significant SiGe wafer bow height change from compressive to high tensile state as well as defect formation in the underlying Si substrate. The key message we need to know is the relaxation degree of strained SiGe to cause defect formation, instead of what methods used to cause relaxation. Therefore, suppressing the total relaxation level of strained SiGe below 10% is important to avoid defect formation in Si for 28nm PMOSFETs volume production.

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Chapter 4

Pattern Dependency of Strained SiGe Relaxation Induced Defects in the underlying Si and Wafer Bending with the MSA

4.1 Introduction

Strain engineering is one of the unavoidable enhancement for deep-submicrometer CMOS, providing the necessary performance enhancement through the increase of the low-field mobility with strain [1-4]. In the case of pFET transistors, the use of the SiGe at source/drain (S/D) regions is a viable method to create uniaxial compressive strain in the channel, resulting in enhancing the hole mobility. The scalability of this method down to the 28 nm node and beyond has been demonstrated, but will require an increase of the Ge content (x, in percent) of the S/D regions to boost device performance and millisecond anneal to sustain a well junction profile with suppression of short channel effect (SCE). As discussed in the last chapter, defect formation and its resultant junction leakage current are unavoidable to appear while relaxed strained-SiGe and MSA were applied to be integrated in 28nm CMOSFET [5-11]. The phenomenon of defect formation induced by SiGe and MSA could exhibit SiGe area dependency that is a key topic we need to investigate and overcome in volume production of 28nm CMOSFET. Some literature has reported that the SiGe relaxation by a post-SiGe thermal anneal revealed dependent on Ge content and its area size. By forming a SiGe buckling layer on the viscous BPSG (Boron Phosphorus Silica Glass) as shown in Fig. 4.1.1, the compressively strained SiGe layers on the BPSG can relax during the thermal oxidation. Lateral thermal expansion and counterforces caused by the viscous BPSG produce compressive stresses during thermal oxidation at high temperature. Bending out of the nominal plane by viscous flow of the underlying BPSG layers at a temperature can relieve compressive stresses in thin semiconductor films. Therefore, a phenomenon of strained SiGe buckling was investigated with different Ge content and SiGe area size effect as shown in Fig. 4.1.2 and the corresponding higher defect density at large SiGe area size as shown in Fig. 4.1.3 [12-14]. We would also like to investigate the pattern dependency of the interaction of the strained SiGe and MSA for 28 nm PMOSFETs production.

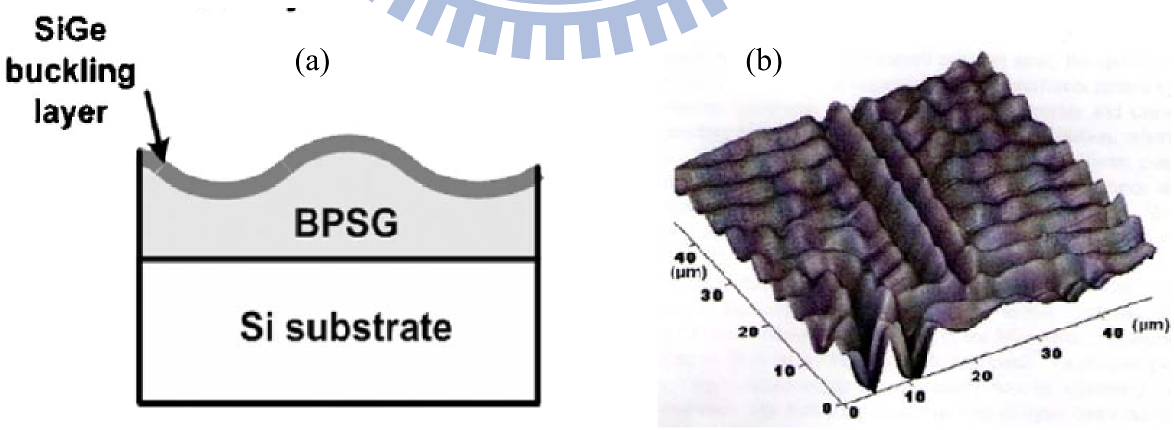

Figure 4.1.1 (a) A SiGe buckling layer on a viscous BPSG layer to see the relaxation of strained SiGe layer by post-SiGe thermal anneal (b) the buckling SiGe layer revealed undulation. (C.Y. Yu, et. al. J. Appl. Phys. 2006)

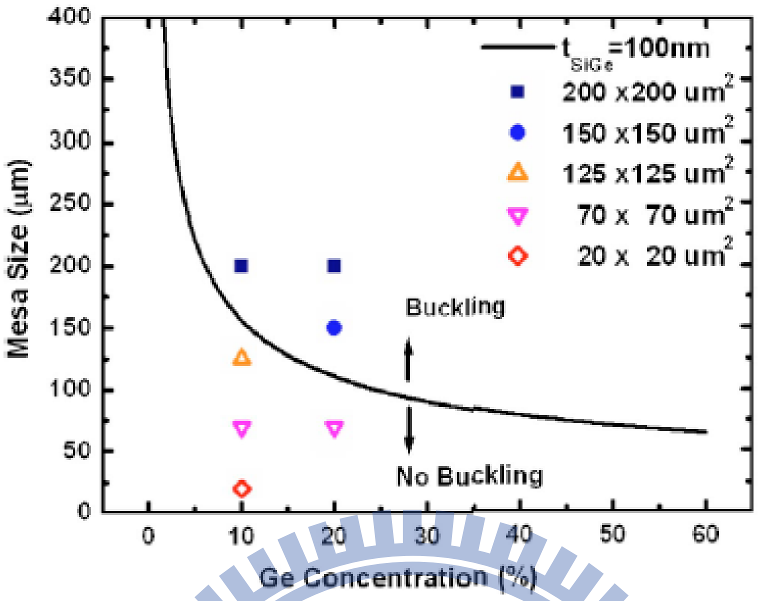

Figure 4.1.2 Critical mesa size vs Ge concentration with a SiGe thickness of 100 nm. Solid symbols indicate the buckled films, and open symbols indicate the unbuckled films. (C.Y. Yu, et. al. J. Appl. Phys. 2006)

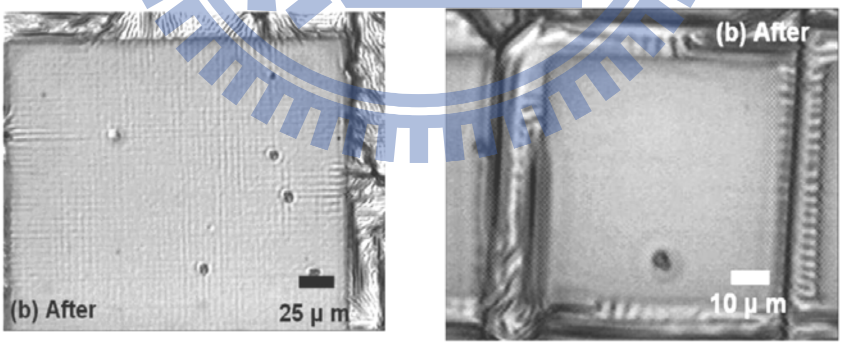

Figure 4.1.3. Optical micrograph images of varying dimension of Si0.8Ge0.2 layers on the viscous oxide after thermal oxidation at 960 °C for 6 minutes. (C.Y. Yu, et. al. J. Appl. Phys. 2006)

4.2. Motivation

One concern related with embedded S/D SiGe processing in PFETs is the junction leakage, which is affected by different processing parameters, such as S/D recess etch, pre-surface clean, Ge content and post implant and thermal anneal, combined with MSA that we will investigate in our work. It has been shown recently that leakage current increase exponentially with the Ge content which could increase SiGe dislocation density in the SiGe junction area as shown in Fig. 4.2.1 [15-17]. An implanted P/N junction region in the SiGe layer caused different degree of dislocation density and junction leakage was raised with increment of dislocation density in the SiGe layer. To suppress post-SiGe process induced defect formation and resultant high junction leakage current is very important while S/D SiGe was applied to advanced CMOSFET.

The aim of the research is to investigate in more detail the impact of MSA on the leakage current of embedded SiGe S/D junctions with SiGe area size dependency. Particular emphasis is to come out a well-designed rule of "*(1) ratio of total SiGe area to whole wafer area, (global area effect) (2) the SiGe area size (local area effect)*" with MSA process to avoid wafer large warpage and defect formation. The resultant design rule of active SiGe area can obtain a as low junction leakage as that of non-MSA process or non-SiGe process to volume production of 28nm CMOSFET and beyond.

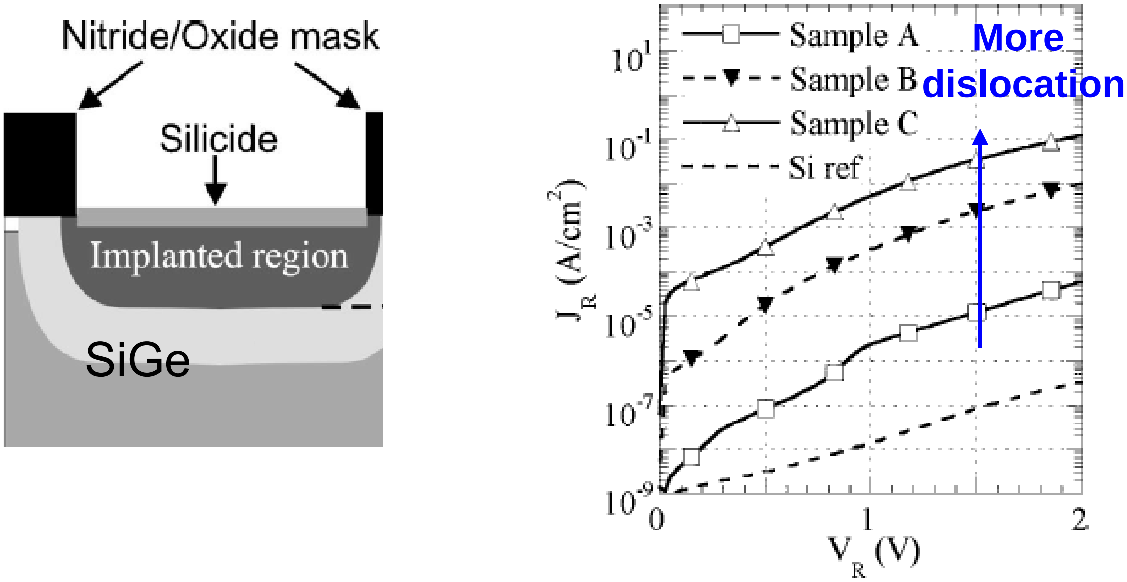

Figure 4.2.1. (a) The structure of implanted SiGe to form P/N junction. (b) high dislocation of SiGe sample caused high junction leakage current. (Geert Eneman, et.al. APL. 2005)

4.3 Experiments

A series of PMOSFETs with SiON gate oxide (Equivalent Oxide Thickness, EOT=12A and Gate length, Lg=32nm) were fabricated using source/drain 100nm-thick strained-$Si_{1-x}Ge_x$ (x nearly~0.35) and in-situ Boron doping with different ratio of total SiGe area to whole wafer area on 300mm (001) Si wafers. The ratio of total SiGe area to whole wafer are designed at 2%, 8%, 12%, 20% and 100% (blanket SiGe wafer) as shown in Fig.4.3.1. Then the pocket implant was conducted in SiGe pattern wafers with different area ratio by implantation using Arsenic (As), at energy of approximately 50keV and a dose of 3E13cm^{-2} for the short channel effect (SCE) control. Spike rapid thermal annealing (RTA) around 1000°C was carried out to recover the damage induced by implantation and to activate the dopants. Laser MSA annealing at around 1200˚C for 500μs then performing to enhance dopant activation, was as plotted in Fig. 4.3.2.

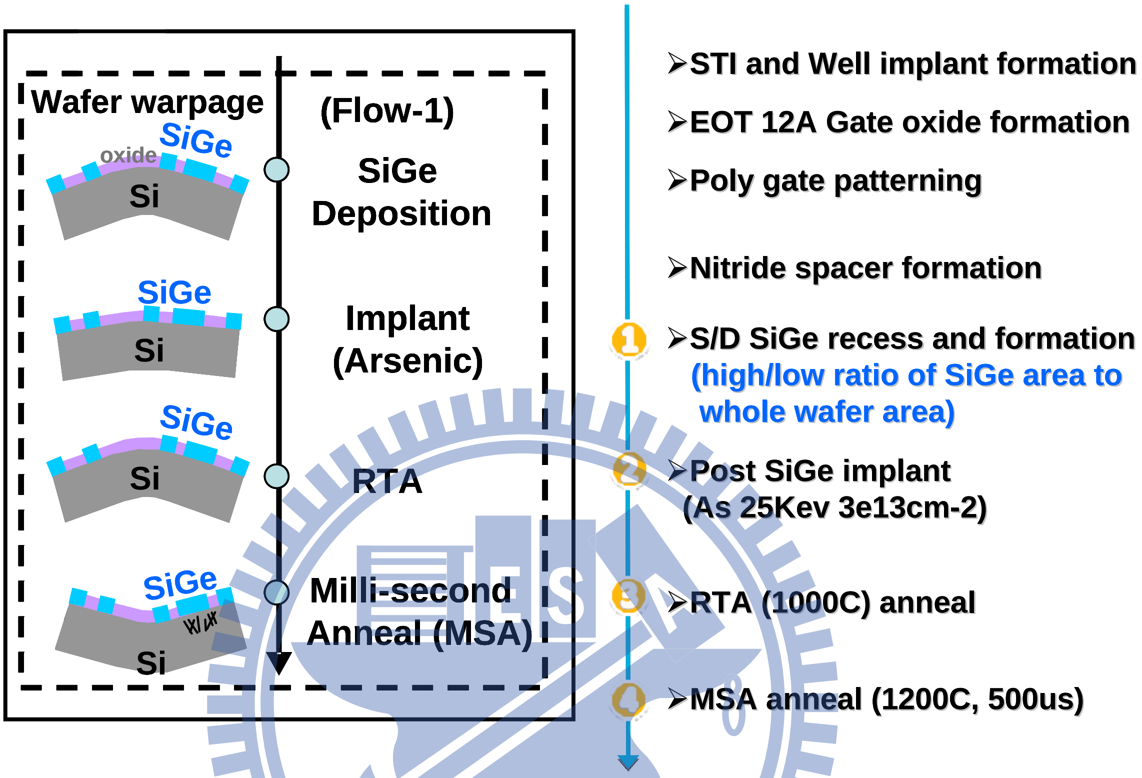

Figure 4.3.1. The S/D strained SiGe with different ratio of total SiGe area to whole wafer are designed and followed with As implant, RTA and MSA

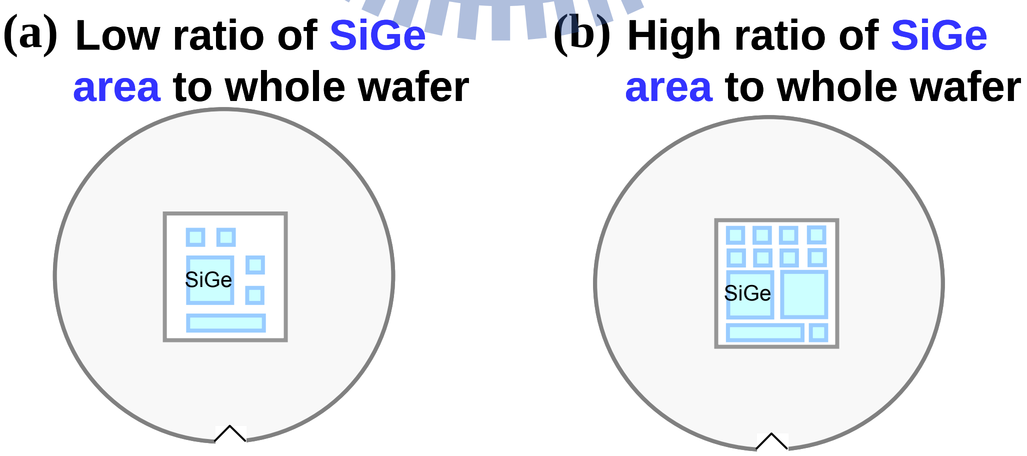

Figure 4.3.2. The schematic plot of (a) low ratio of total SiGe area and (b) high ratio of total SiGe area to whole die area.

4. 4 Results and Discussion

4.4.1 Global effect: ratio of total SiGe area to whole wafer and its effect on wafer warpage with MSA

Fig. 4.4.1 shows that the pattern SiGe wafer bow height change was affecting by the ratio of total SiGe area to total wafer area with the following implant, RTA and MSA process. For blanket wafer fully covered with SiGe, 100% ratio of total SiGe area, the wafer bow height of relaxed strained-SiGe with MSA revealed large value in tensile state and was gradually reduced while total SiGe area ratio was decreased. As we proposed the two factors caused defect formation in the underlying Si substrate while MSA was applied on the relaxed strained-SiGe.

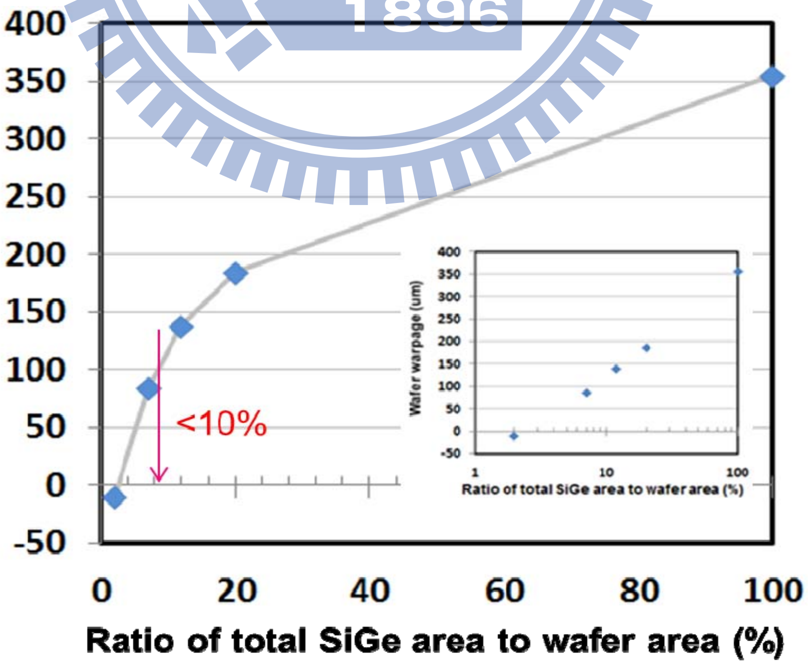

Fig. 4.4.1 shows the pattern SiGe wafer warpage was affecting by the ratio of total SiGe area to total wafer area with the following implant, RTA and MSA

One is the larger CET of SiGe than that of Si, and the other is the lowered yield stress of relaxed strained-SiGe during high temperature. Therefore, the more SiGe area in the portion of wafer, the larger surface expansion and the higher wafer bow height.

As the ratio of total SiGe area was less than 10%, the wafer bow height was acceptable for the following lithographic limitation. Therefore, a well-designed ratio of total SiGe area to whole wafer area is important to avoid large wafer warpage in the integration of SiGe and MSA and get rid of lithographic limitation due to high wafer warpage.

4.4.2 Local effect: relation of SiGe area and defect formation in the underlying Si substrate with MSA

Fig 4.4.2 (a) exhibits the schematic plot of pattern wafer bow height change following process flow of SiGe, implantation, RTA and MSA. The ratio of total SiGe area to whole wafer area was controlled at around 2% to verify local SiGe area size effect on defect formation in the underlying Si substrate during MSA. The pattern SiGe wafer warpage was close flat after MSA and supposes that there was no defect formation in the underlying Si substrate due to the small value of wafer bow height. However, large SiGe area of 25um2 showed high defect density up to 2um depth in the underlying Si substrate after MSA as shown in the Fig 4.4.2 (b). In contrast, at the same pattern SiGe wafer the nearby small SiGe

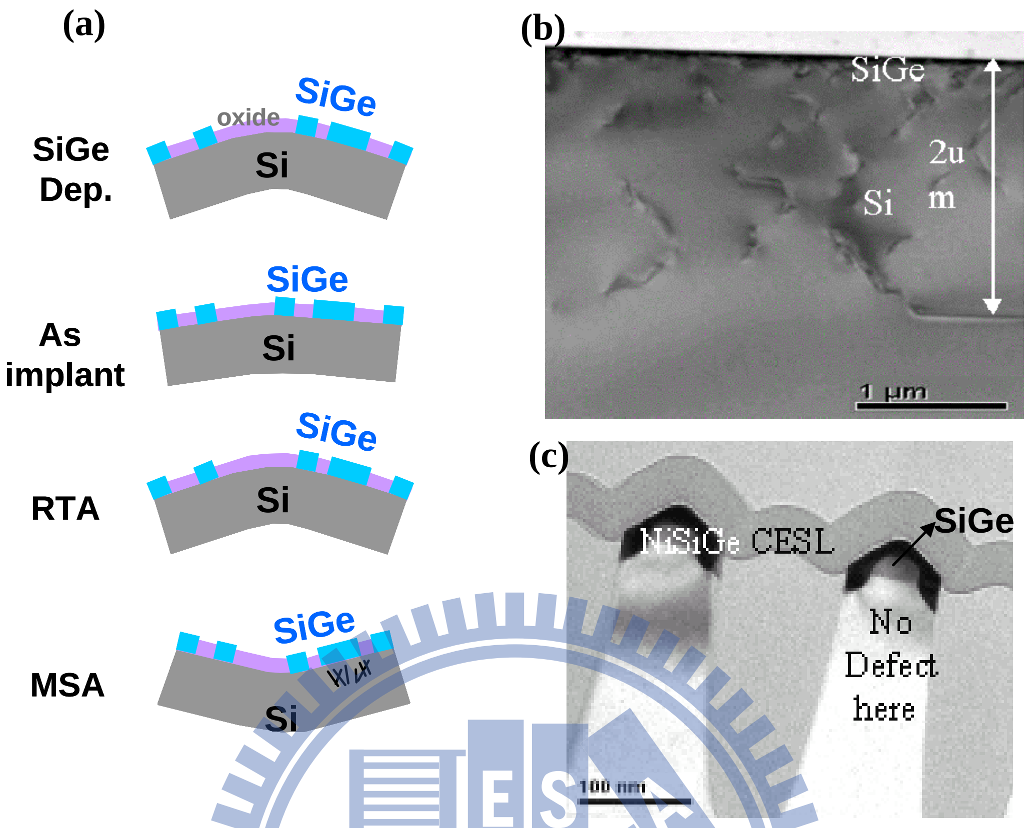

Fig 4.4.2 (a) exhibits the schematic plot of pattern wafer bow height change following process flow of SiGe, implantation, RTA and MSA (b) defect formation in Si for large SiGe area (c) defect free in Si for small SiGe area.

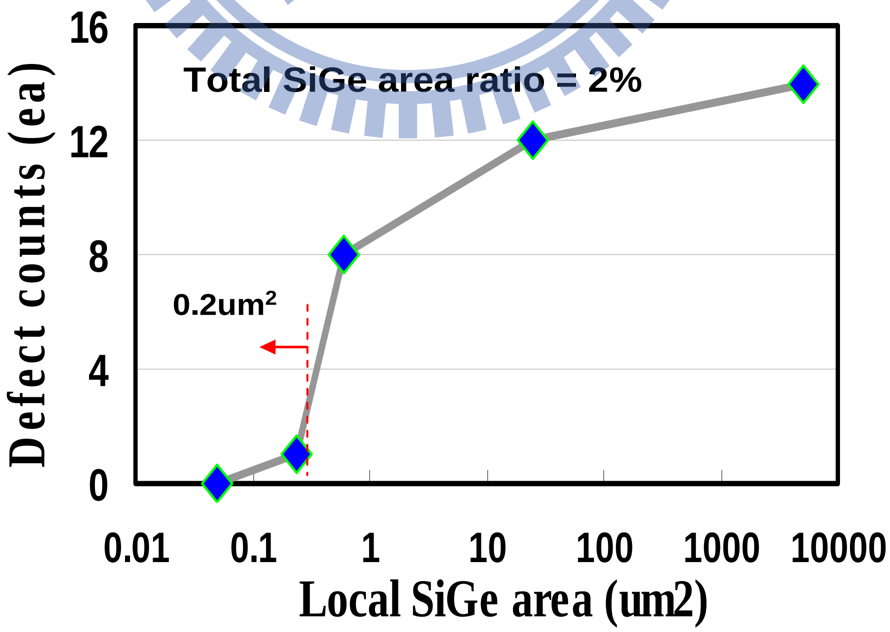

Fig. 4.4.3 illustrates that the defect density counting per unit length at TEM image could dramatically decrease while local SiGe area was less than 0.2um2

pad with area size around 0.02 um2 did not exhibit defect formation at all in the underlying Si substrate after MSA. It is obvious that the phenomenon of MSA on implanted strained-SiGe causing defect formation in the underlying Si substrate has SiGe area size dependency.

Fig. 4.4.3 illustrates that the defect density counting per unit length at TEM image could dramatically decrease while local SiGe area was less than 0.2um2. A well-designed rule of local SiGe area to avoid defect formation in the underlying Si substrate with the combination of SiGe and MSA process is very important for 28nm CMOSFET and beyond.

4.4.3 Simulated SiGe area effect on defect formation during MSA

Active SiGe area dependency: Simulated SiGe area size effect on SiGe strain was showed in Fig. 4.4.4. When source/drain SiGe was surrounding by SiO_2 – like the stress absorber, SiGe/Si interface stress was reduced. Stress absorption effect of the SiO_2 was feeble in large SiGe area size to have higher SiGe/Si interface stress, which was unstable and was prone to form misfit dislocation by post-SiGe implant and RTA, resulting in defect injection when MSA was applied. The active SiGe area size dependency on defect formation during MSA was further discussed to verify the correction of mechanism that we have proposed in chapter 2.4

From the mechanism we proposed in chapter 2.4, there are two factors affecting defect formation in the underlying Si substrate while MSA was applied on the relaxed strained-SiGe.

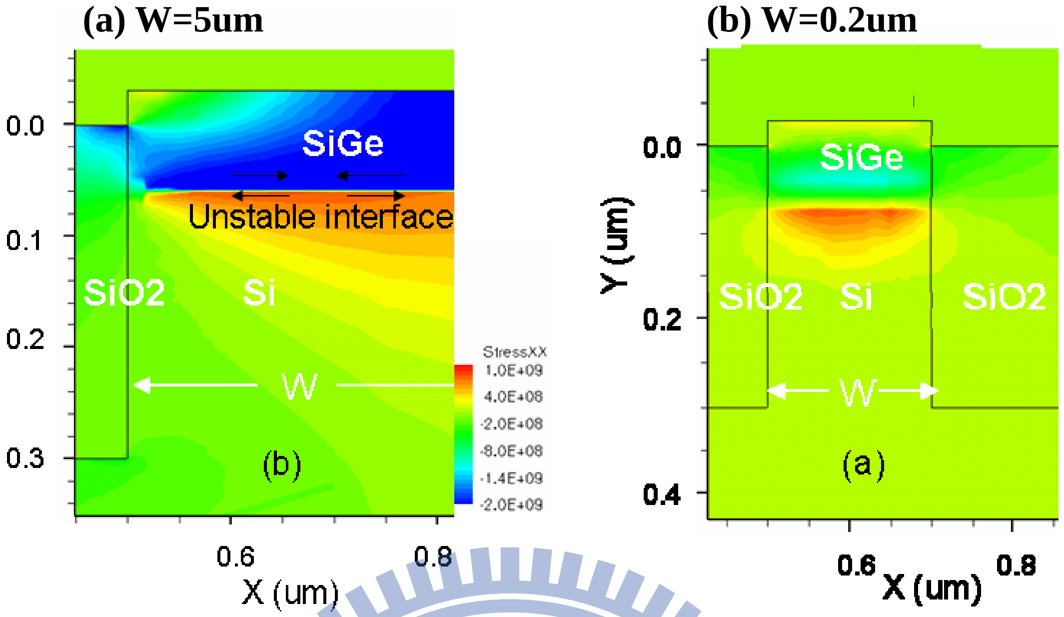

Figure 4.4.4. Simulated size effect of SiGe strain under the same Ge% (a) W=5um (b) W=0.2um and both SiGe length=0.5um devices.

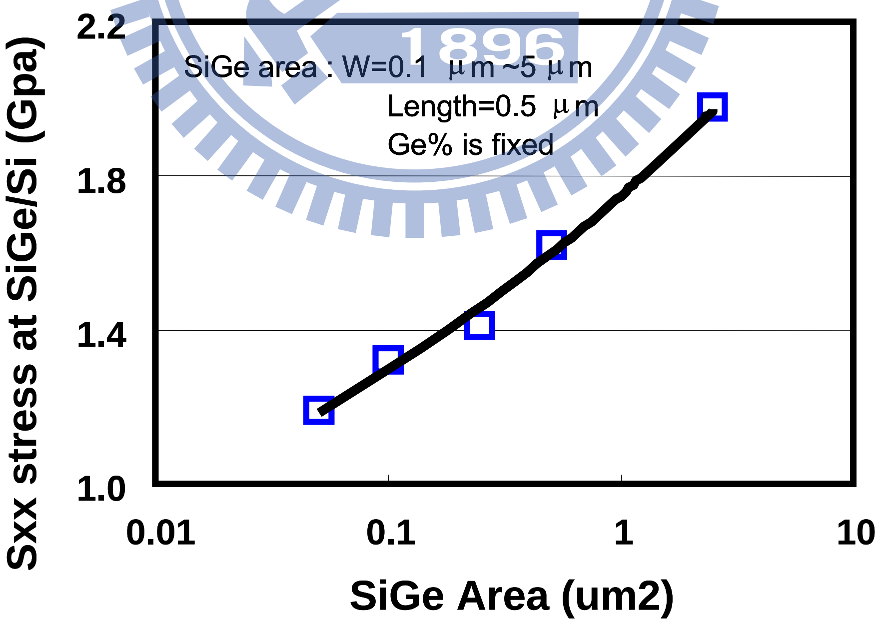

Figure 4.4.5. Simulated stress at SiGe/Si interface as a function of the size of SiGe area.devices.

One is the larger CET of SiGe than that of Si, and the other is the lowered yield stress of relaxed strained-SiGe during high temperature. Therefore, it is unavoidable that the larger SiGe area revealed larger surface expansion during MSA heat-up as expressed as below,

$$\Delta L = \alpha L (\Delta T) \qquad (1)$$

α is thermal expansion coefficient, L is the dimension of SiGe area, and T is the MSA heat-up temperature. Hence, large SiGe area revealed higher SiGe strain than that of small SiGe area and large SiGe area showed large surface expansion and caused defect formation during MSA. In contrast, small SiGe area demonstrated small surface expansion and would not cause defect formation during MSA.

4.4.4 SiGe area effect on junction leakage with MSA

Fig. 4.4.6 shows the correlation of SiGe area and junction leakage, which was dependent on SiGe source/drain active area size. The larger SiGe area size was displayed, the higher junction leakage revealed. It shows that upon MSA, junction leakage was dependent on implanted SiGe area. MSA on implanted Si did not show junction leakage dependency on the implanted Si area and implanted SiGe with RTA also showed low junction leakage. However, MSA on large implanted-SiGe area around 25um2 mentioned in the previous section was caused defect formation in the underlying silicon substrate as shown in the inset TEM of Figure, which resulted in junction leakage about 4-order higher than that of non-MSA SiGe process. The junction leakage gradually reduced as SiGe area was decreased. While upon MSA, the implanted SiGe area was close to 0.05um^2 and it did not cause defect formation due to the small surface expansion during MSA heat-up and showed the junction leakage as low as non-MSA process. We have to find out the critical SiGe area to suppress defect formation during MSA. From the figure that we knew the critical SiGe area was around 0.2 um^2 that is important for design rule to combine SiGe and MSA process in the 28nm CMOSFET.

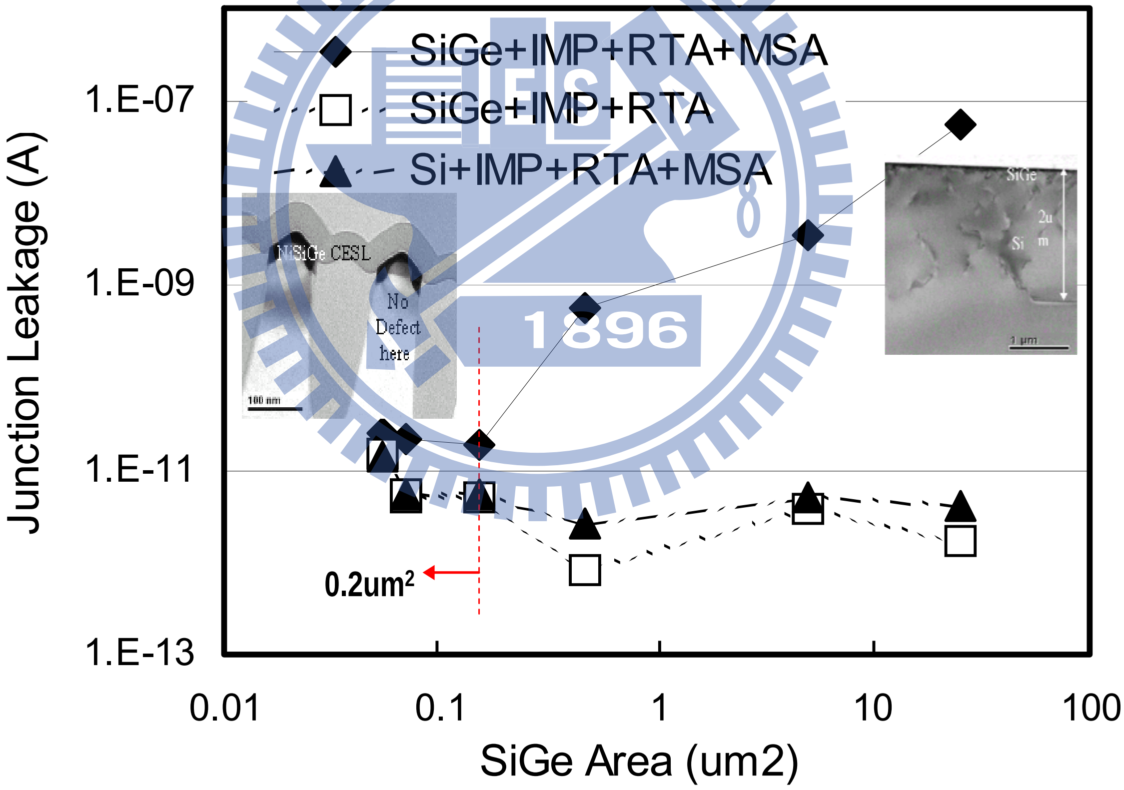

Figure 4.4.6. MSA induced junction leakage current at different size of the active SiGe area.

4.5 Summary

In this chapter a design rule of S/D SiGe with different active area size to form defects in the underlying Si substrate during MSA have been proposed for 28nm CMOSFET.

First, as the ratio of total SiGe area to whole wafer was less than 10%, the wafer bow height was less than 100um after MSA and that was acceptable for the following lithographic limitation. Therefore, a well-designed ratio of total SiGe area to whole wafer area is important to avoid large wafer warpage in the integration of SiGe and MSA and get rid of lithographic limitation due to high wafer warpage.

Second, we have found out the critical SiGe area to avoid defect formation in the underlying Si substrate during MSA. From the figure we knew the critical SiGe area was less than 0.2 um^2 that is important for design rule to combine SiGe and MSA process.

With the SiGe area size smaller than 0.2um2 the junction leakage of SiGe to substrate can be controlled as low as that of non-MSA process. Therefore, a well-designed rule of total SiGe area ratio to whole wafer and local SiGe area size were proposed to avoid defect formation in the underlying Si substrate for 28nm CMOSFET volume production.

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Chapter 5

Novel Technique to Fabricate 28 nm p-MOSFETs Possessing Gate Oxide Integrity on the Embedded SiGe Channel without Silicon Surface Passivation

5.1 Introduction

The last few years have seen the Si/SiGe material system widely integrated into CMOS technology. The 4.2% lattice mismatch between Si and Ge can be used to obtain the strained layer, where electron (in Si under tension) and hole (in SiGe under compression) transport is improved. Epitaxial SiGe at source/drain (S/D) region for pFETs drive current enhancement has been pursued aggressively in scaled CMOS technologies [1-2]. However, the S/D strained SiGe of the pFETs performance improvement is getting diminished because the volume left for this S/D SiGe stressor is getting smaller and smaller for the advanced technology node [3]. Channel stress was dramatically decreased as the source/drain recess depth and the source/drain SiGe dimension are scaled down as shown in Fig.5.1.1(a). Inevitably mobility degradation and device performance degradation with gate length scaling has been reported as shown in Fig.5.1.1(b). There have several methods of S/D epitaxial SiGe process to boost device performance as CMOS scaling. Increasing Ge content or enlarge S/D

SiGe volume or using SiGe channel are the candidates for device performance boosting that have been worldwide discussed. Therefore, finding a good way of epitaxial SiGe process for device performance boosting is necessary for 28nm CMOS and beyond.

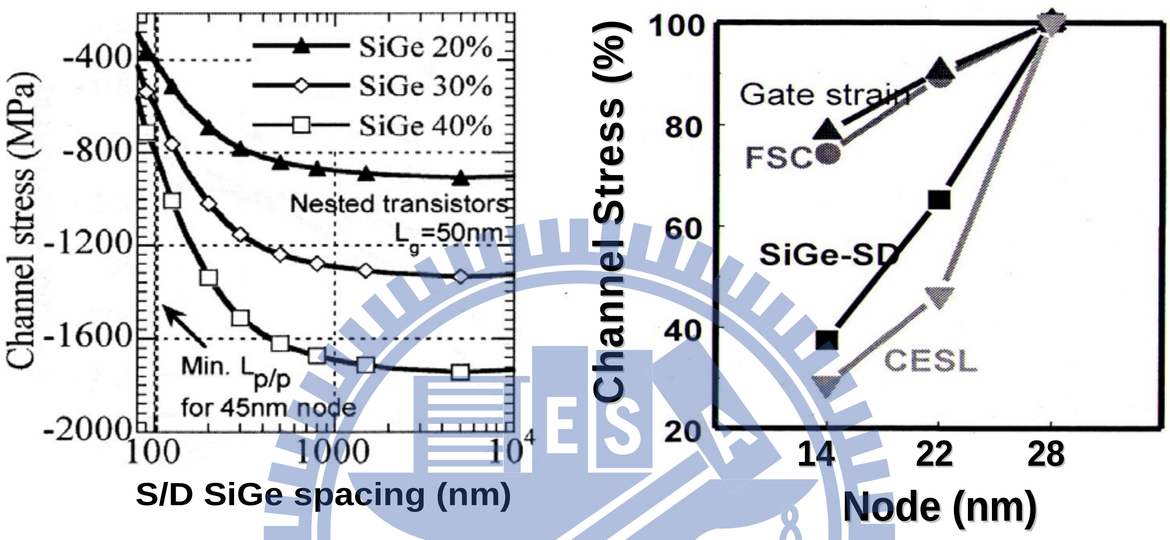

Figure 5.1.1 (a) Channel stress was dramatically decreased as the S/D recess depth and the S/D SiGe dimension are scaled down. (b) Inevitably mobility degradation and device performance degradation with gate length scaling. (Geert Eneman, et. al. TED, 2006)

5.2 Motivation.

Increasing Ge concentration in the S/D SiGe region is a straightforward method without extra process flow / profile change and device parameter tuning to boost device performance as PFETs scaling down. However, Ge content is inevitable to continuous increment in the S/D SiGe due to the critical thickness effect that increasing Ge content in the S/D SiGe would cause misfit dislocation formation in the interface of SiGe and Si substrate. Unfortunately, high Ge content loss more strain and results in lower channel stress that would cause opposite result to degrade device performance. In general, Ge content over 50% is very difficult to integrate in the advanced CMOS process flow unless a robust S/D SiGe profile or a well-designed implant and thermal process flow.

On the other hand, widening S/D SiGe volume to shorten the proximity of the S/D SiGe to gate stack is getting attraction to increase channel stress for device performance enhancement [4-5]. Tetsuji has reported that deposition of epitaxial SiGe layer at the lightly doping drain (LDD) region by extra pre-etch process enabled to boost device performance [6]. However, Extension of S/D SiGe to gate stack also faced limitation in scaled CMOS technologies because we can not push S/D SiGe layer into the channel region unless process flow was changed.

Another approach to channel strain engineering is SiGe channel, which was considered as a promising candidate in the nano pMOSFETs for the performance boost-up [7-10]. As we knew that higher carrier mobility about three times in the SiGe material than that of Si. Hence, carrier transport in the SiGe channel is good candidate to boost device performance because channel length did not scale very much and drive current did not loss as that of S/D SiGe while CMOS scaling. However, in order to integrate SiGe channel, one needs to provide a thin Si cap on SiGe channel to prevent Germanium oxide (GeO_x) formation during gate oxide growth as shown in Fig.5.2.1. Thicker Si surface passivation capping layer near 5nm could

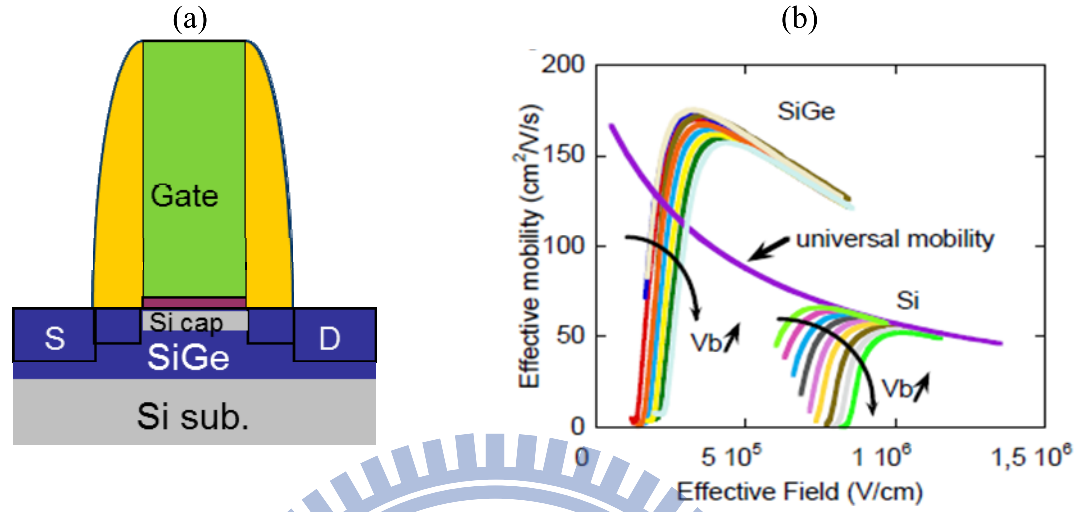

Figure 5.2.1 (a) the schematic structure of the SiGe channel with a thin Si cap layer (b) SiGe channel shows high effective mobility than that of Si channel at the same effective field. (F. Andrieu, et. al. EDL, 2006)

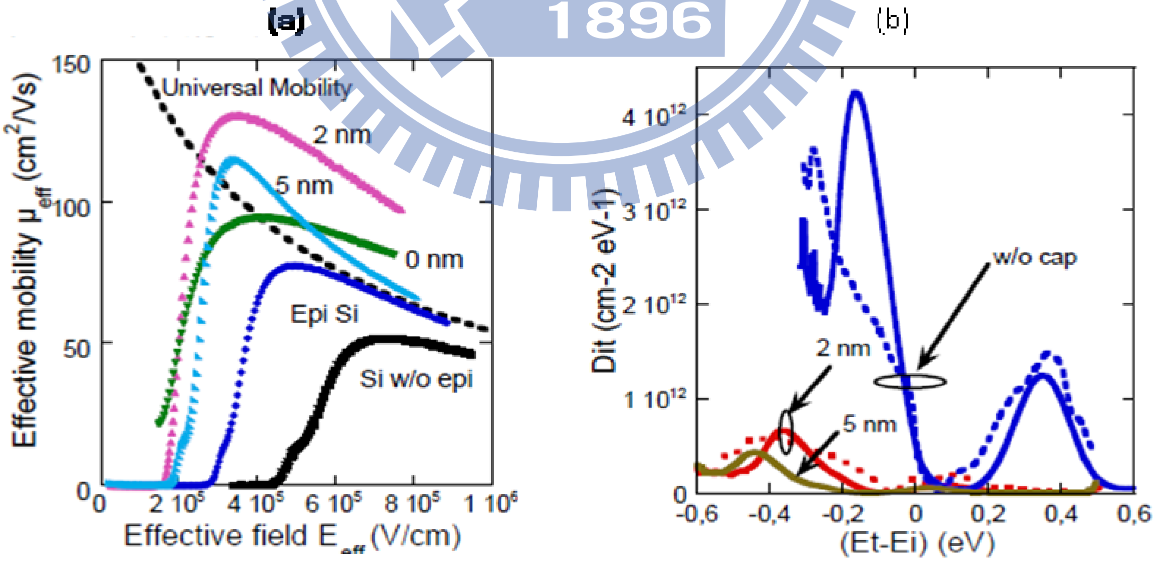

Figure 5.2.2 (a) effective mobility of SiGe channel is dependent on the thickness of thin Si cap (b) Dit is also dependent on the thickness of thin Si cap layer. (F. Andrieu, et. al. EDL, 2006)

demonstrate as low interfacial defect (Dit) as Si channel as shown in Fig.5.2.2. But it would attribute to dual channel profile that carriers transport in the Si and SiGe layers degrading carrier mobility. The optimized Si capping layer is about 1~2nm to provide better carrier mobility and low interfacial defects. Such a thin Si cap layer near 1~2nm is very difficult to control for mass production and one also need to consider the post SiGe-channel thermal induced dislocation resulting in gate leakage and device performance degradation. In all, an inevitable epitaxial Si cap layer to provide gate oxide integrity and subsequent thermal budget control to avoid onset of threading dislocations from SiGe channel become the major barriers of technology implementation [11-16].

In this work, we demonstrate a novel embedded SiGe channel (ESC) structure composed of strained SiGe channels without extra Si surface passivation to show potentially superior hole mobility and superior gate oxide integrity. It is believed that ESC structure is a very promising candidate in nano device era with the beautiful essence of low cost and standard pMOSFETs process compatibility.

5.3 Experiments

A series of pFETs with STI and well implantation to control Vt in the embedded SiGe channel (ESC) devices, in which SiGe has smaller energy gap (Eg) than Si substrate were fabricated on 300 mm [110]/(001) Si wafers. Following 1.5nm-thick SiON with 10%~15% of nitrogen concentration was formed by rapid thermal process (RTP) and decoupling plasma nitridation (DPN). 30nm gate length of poly-crystal was defined and the poly-crystal line was normal to channel direction [110] shown as in the Fig.5.3.1. Channel direction was switched to boost PMOSFET device performance from 65nm technology. Then 15nm nitride spacer critical dimension (CD) was conducted. A conventional reactive ion etching process (RIE), named as dry etch-1 (Fig.5,3.2), created a recessed region of 60 nm in depth with sidewall Si lattice plane (110) and bottom Si lattice plane (100).

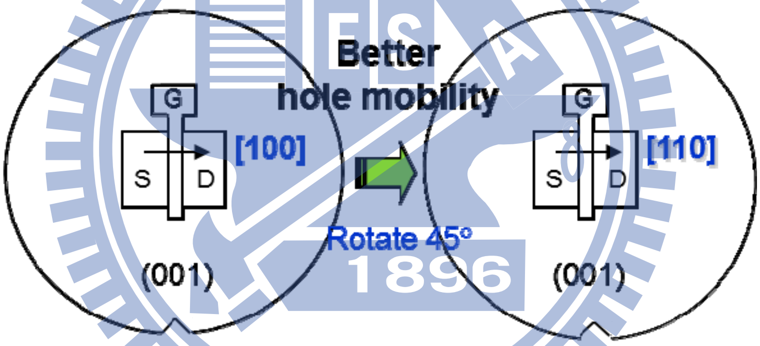

Figure 5.3.1 The channel direction was changed from [100] to [110] for pMOSFET device performance boosting

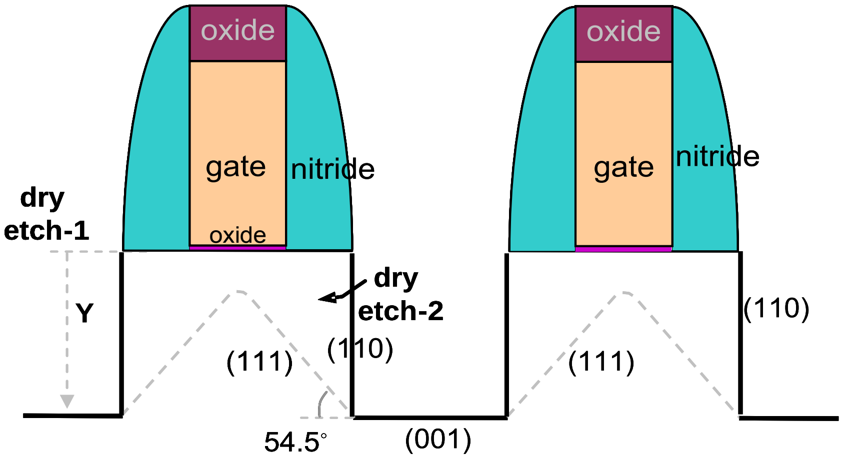

Figure 5.3.2 A conventional reactive ion etching process (RIE), named as dry etch-1 and (110) lattice plane of sidewall appeared.

Plane	Ea (eV)	Lattice plane
<100>	2.37	Existed
<110>	1.81	Disappeared
<111>	2.32	Existed

Table 5.3.1 The activation energy of etching away [110] is the lowest among [100] and [111] lattice planes

Subsequently the samples were put into the reduced pressure chemical vapor deposition (RPCVD) chamber at 700°C for the novel technique of the dry etch, named as dry etch-2, which is an in-situ etch process of Cl_2 or HCl gas to etch away silicon along (111) plane with 54.5° to create suspending gate stack (Fig.5.3.3)). The activation energy of etching away [110] is the lowest among [100] and [111] lattice planes as shown in table 5.3.1. One could use the difference of etching activation energy to make [110] plane disappeared and kept [100] and [111] plane. At the same time, the in-situ etching gas in the epitaxial chamber did not damage with silicon nitride (Si_3N_4) and gate oxide (SiO_2) at 700℃ and the chemical equations for describing the formation of the embedded SiGe channel (ESC) structure are expressed as below:

$$2Cl_{2(g)} + Si_{(s)} \rightarrow SiCl_{4(g)} \qquad T=700^{\circ}C, \qquad (1)$$

$$4HCl_{(g)} + Si_{(s)} \rightarrow SiCl_{4(g)} + 4H_{(g)} \qquad T=700^{\circ}C, \qquad (2)$$

$$4HCl_{(g)} + SiO_{2(s)} \rightarrow SiCl_{4(g)} + 2H_{2(g)} + O_{2(g)} \qquad T>1800^{\circ}C, \qquad (3)$$

$$12HCl_{(g)} + Si_3N_{4(s)} \rightarrow 3SiCl_{4(g)} + 4\,NH_{3(g)} \qquad T>1800^{\circ}C. \qquad (4)$$

By well-designed depth of dry etch-1 over 40nm and the lattice crystalline characteristic of dry etch-2 along (111) plane under gate length of 30nm and silicon nitride of 15nm, we can perform calculations involving trigonometric functions to obtain a suspending gate stack of poly-silicon as shown in Eq. (5.3.1.) and Fig.5.3.4. The process was very healthy and channel depth is well-controlled because [111] is the highest packing plane and etching would stop while [111] appears. Because the high modulus of silicon material at gate region, it is not so easy to break down while the substrate is empty. Therefore, we could obtain the depth of SiGe channel we want in the device design.

$$Z = Y - [(0.5\ Lg + X\ ]\tan(54.5^{\circ}) \qquad (5.3.1)$$

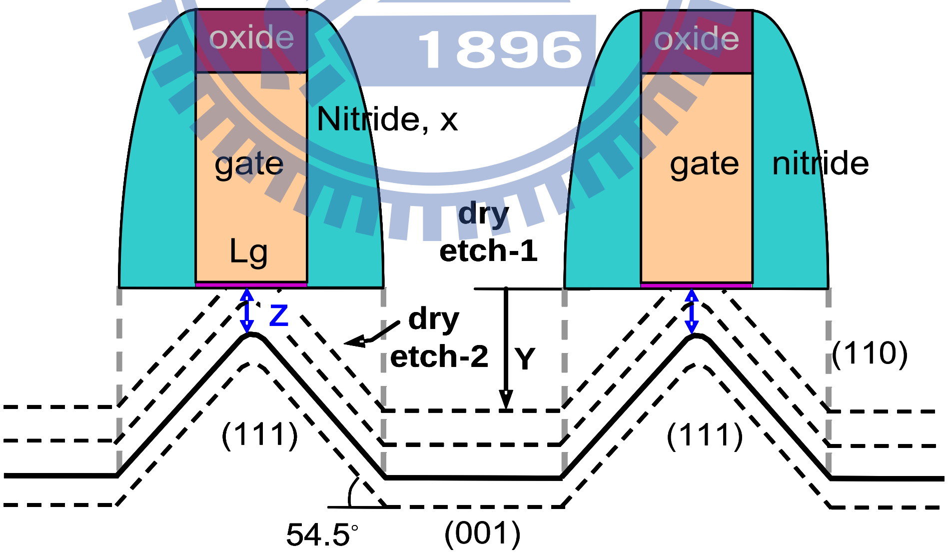

Figure 5.3.3 It illustrates the design of the embedded SiGe channel by defining the various depth of dry etch-1, Y, then obtaining the corresponding SiGe channel depth, Z.

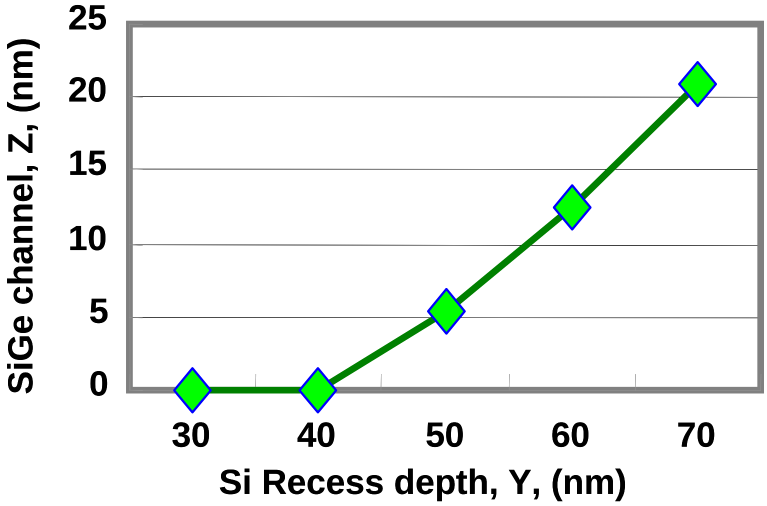

Figure 5.3.4 The suspending SiGe channel depth, Z versus S/D Si recess depth, Y.

An undoped SiGe epitaxial layer (Ge~40 at. %) to fill up channel and a doped SiGe SiGe layer to fill up source/drain was deposited at 700°C without the necessity of a thin Si surface passivation layer in the same RPCVD chamber. The epitaxial SiGe layer was conjointly formed in compressive mode at channel as well as the LDD and S/D region (Fig.5.3.5) and Fig.5.3.6). The transmission electron microscopy (TEM) image of the almost dislocation-free ESC showed the good crystalline embedded SiGe channel between the gate oxide and under-layered Si substrate, as shown in Fig.5.3.7. The good crystallinity of ESC layer on blanket wafer was characterized by X-ray diffraction spectrum (XRD) as shown in Fig.5.3.7.

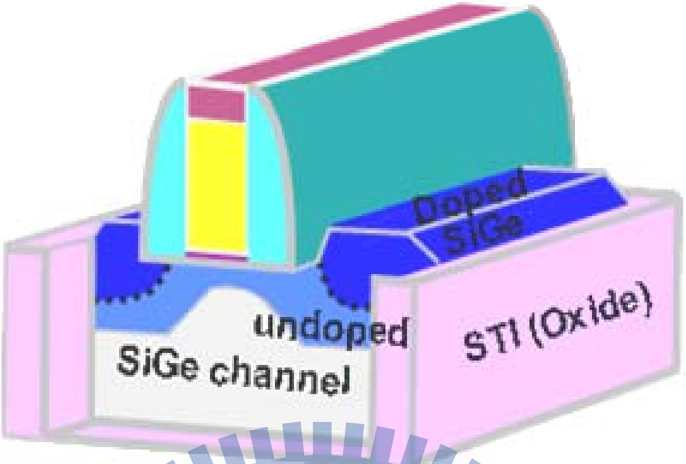

Figure 5.3.5 It shows the profile of embedded SiGe channel and S/D SiGe

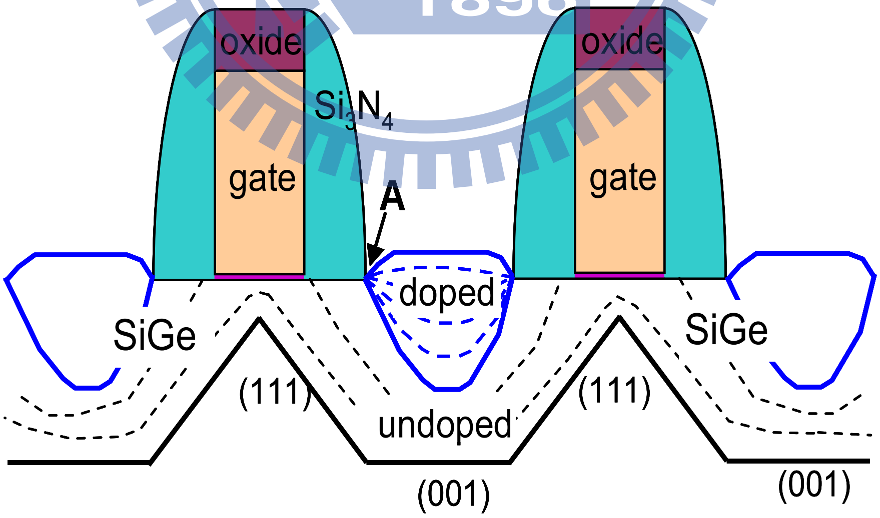

Figure 5.3.6 It shows the profile of embedded SiGe channel and S/D SiGe

Figure 5.3.7 TEM picture shows the embedded SiGe channel (ESC) structure

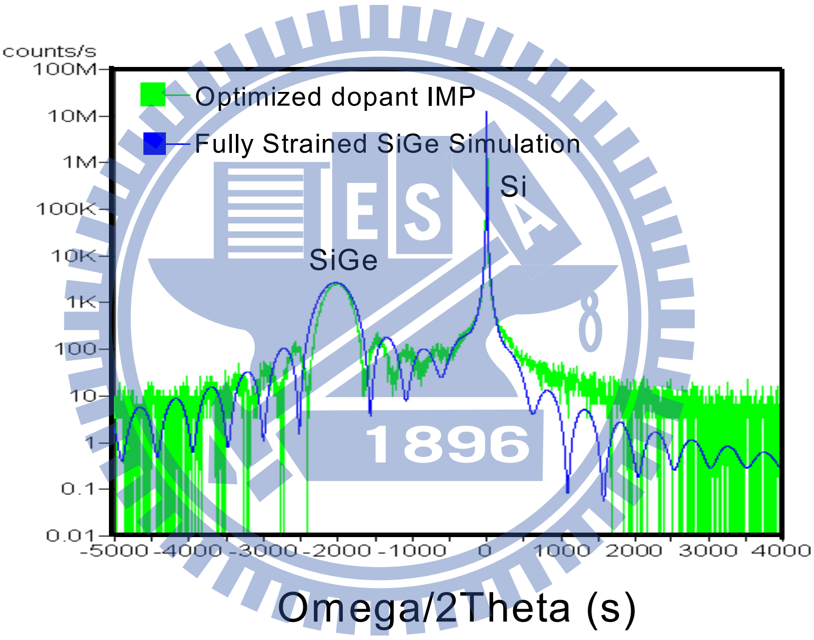

Figure 5.3.8 The good crystallinity of ESC layer on blanket wafer was characterized by X-ray diffraction spectrum (XRD)

The Arsenic (As) pocket implant was conducted after silicon nitride was removed shown as in Fig. 5.3.9 and another silicon nitride was deposited again for silicidation after the ESC formation shown as in Fig.5.3.10. Subsequent processes were carried out to fabricate the 28 nm pMOSFETs. The TEM image of the ESC showed the good crystalline embedded SiGe channel between the gate oxide and under-layered Si substrate. The ESC devices are compared to the referred Si pFETs with S/D strained SiGe.

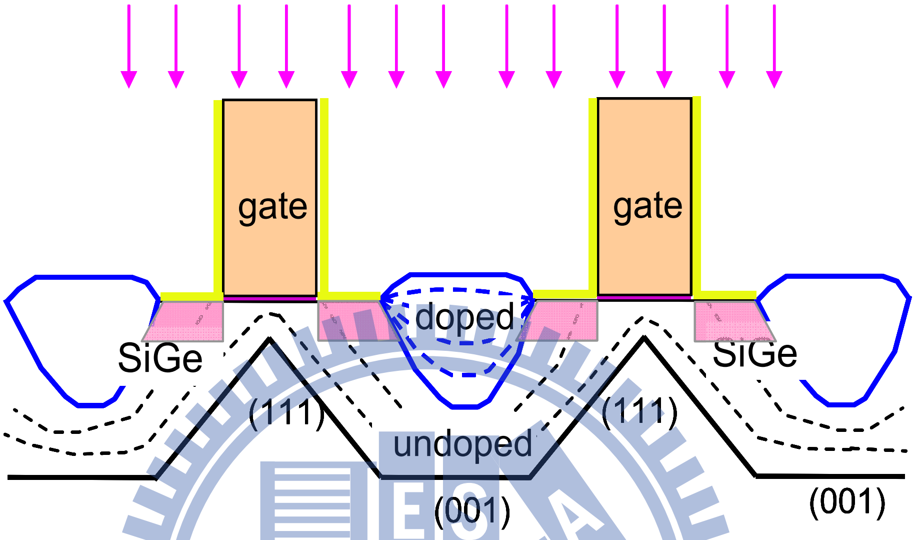

Figure 5.3.9 The following nitride removal and LDD implant on the ESC structure

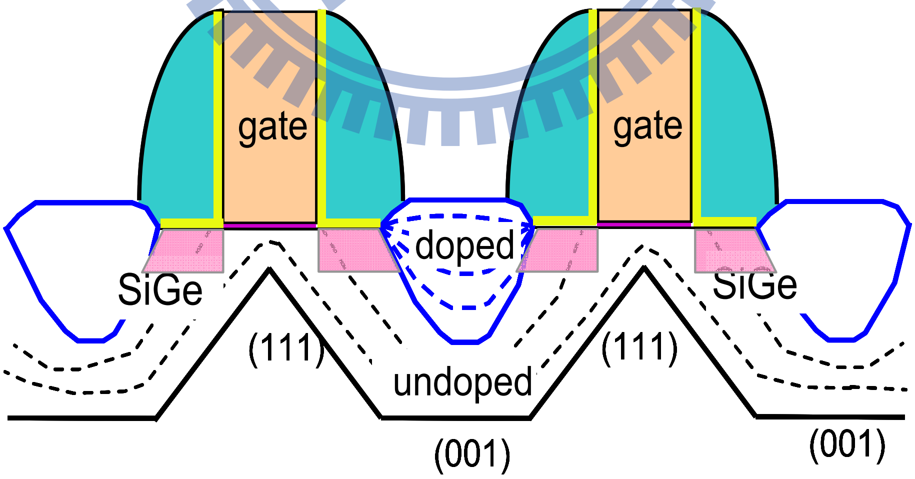

Figure 5.3.10 The following main nitride spacer was conducted on the ESC structure as well as S/D implant.

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5.4. Results and Discussion

5.4.1. Method of Electrical Parameter Extraction

In the thesis, the electrical characteristics of devices were measured by HP 4156C semiconductor parameter analyzer. Extraction methods of all the electrical parameters mentioned in this thesis, including the threshold voltage (V_{th}), subthreshold swing (S.S.), maximum on-current (I_{on}), minimum off-current (I_{off}), channel resistance and effective gate length (L_{eff}), are introduced.

Threshold Voltage (V_{th})

The method to determine the threshold voltage in this thesis is the constant drain current method, that is, defined as the gate voltage required to achieve a normalized drain current of $I_D = (W/L)\times 10^{-8}$ A at $|V_{DS}| = 0.1$V.

Transconductance (Gm)

The field effect mobility is extracted from the maximum transconductance in the linear region of I_{DS}-V_{GS} characteristics at $|V_{DS}| = 0.1$V using the formula:

$$\mu^* = \frac{g_m}{C_{ox}(\frac{W}{L})V_{DS}} (@V_{DS} = 0.1V) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5.4.1.)$$

, where C_{ox} is the gate oxide capacitance per unit area, and the transconductance (g_m) is defined as:

$$g_m = \frac{\partial I_D}{\partial V_g}\Big|_{V_{DS}=0.1V} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(5.4.2.)$$

Transconductance is an important parameter for carrier transport; it describes how strong the motion of an electron or hole is influenced by the applied electric field.

Subthreshold swing (S.S.)

Substhreshold swing (SS) is defined as:

$$\mathrm{SS} = \min\left(\frac{\partial \log(I_D)}{\partial V_G}\right)^{-1} @V_{DS} = 0.1V \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots(5.4.3.)$$

It is a typical parameter to describe the control ability of gate toward channel.

Maximum on-current and Maximum leakage-current

In this chapter, on-current is defined as the drain current measured at V_{GS}= 3V, V_{DS}= 1V. Maximum leakage current is defined as the drain current measured at V_{GS} = -3V, V_{DS} = 1V.

On/off current ratio

The on/off current ratio is defined as the ratio of maximum drain current over minimum drain current at $|V_{DS}|$ = 1 V.

A high performance poly-Si TFT should not only provides high on-state driving current but low off-state leakage current. High on-state driving current means the transistor capacitances could be turned on more efficiently. Sufficiently low off-state leakage current represents the low leakage current and low power consumption.

Channel resistance and effective gate length

Simple current-voltage relationship for the drain current in the linear region was expressed as

$$I_d = \frac{W}{L_{eff}} \mu C_o (V_{gs} - V_t) V_{ds}$$

Where W is the channel width, Co is the oxide capacitance per unit area, μ is the effective free-carrier mobility, V is the threshold voltage, and Vgs and Vds are the intrinsic gate-source and drain-source voltage, respectively. The intrinsic voltages can be related to the external gate-source and drain-source

$$V_{gs} = V_g - V_d R_s$$

$$V_{ds} = V_d - I_d (R_s + R_d)$$

Combining equations ( ) and ( ), the total channel resistance, Rm can be expressed by:

$$R_m = \frac{V_d}{I_d} = R_{ds} + \frac{(L_m - \Delta L_{eff})}{\mu C_0 W (V_{gs} - V_t)} \quad \text{.......(5.4.4)}$$

Then, according to equation (5.4.4.), the plot of Rm versus Lmask is a straight line for given (Vgs-Vt), and the unique intersection of all the straignt lines for different (Vg-Vt) yields Leff on the Lmask axis and Rsd on the Rm axis. Therefore, effective gate length can be extracted that was shown in reference [17].

5.4.2. Electrical Characteristics of Embedded SiGe Channel

- **Boron diffusion in ESC device**

Fig.5.4.1 shows implanted Boron diffusion length in Si and SiGe. It has been reported that Boron out-diffusion from lightly doped regions (LDD) region causes the worse short channel control in the conventional strained Si pFETs. The epitaxial SiGe layer of the ESC structure in the LDD region can retard the out-diffusion of Boron and has the better short channel control. As shown in the Fig.5.4.1, blanket SiGe layer exhibits a smaller Boron out-diffused length around 3.5nm than that in Si substrate. The reason why Boron out-diffusion was retard has been reported [18]. Under compressive strain, interstitial sites in lattice were reduced as shown in Fig. 5.4.2 and in general, Boron was an interstitial diffuser. Therefore, Boron diffusion was retarded under compressive strain of epitaxial SiGe layer as shown in Fig.5.4.3.

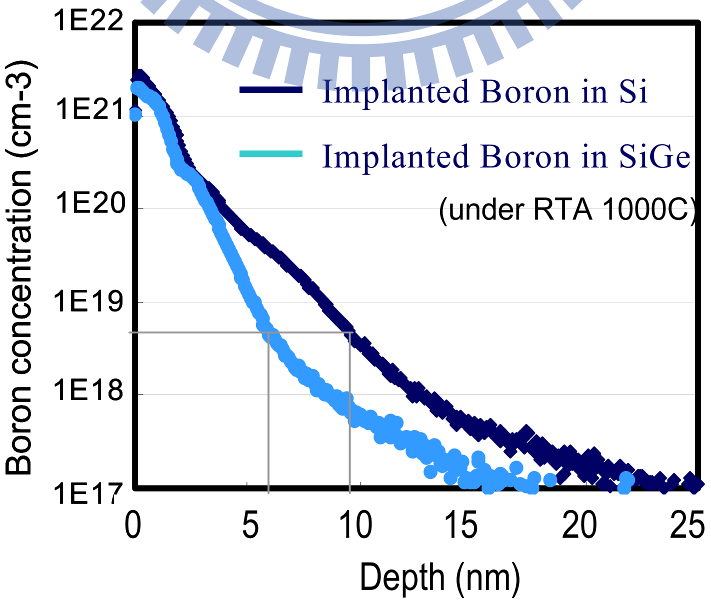

Figure 5.4.1 blanket-SiGe layer exhibits a smaller Boron out-diffused length around 3.5nm than that in Si substrate

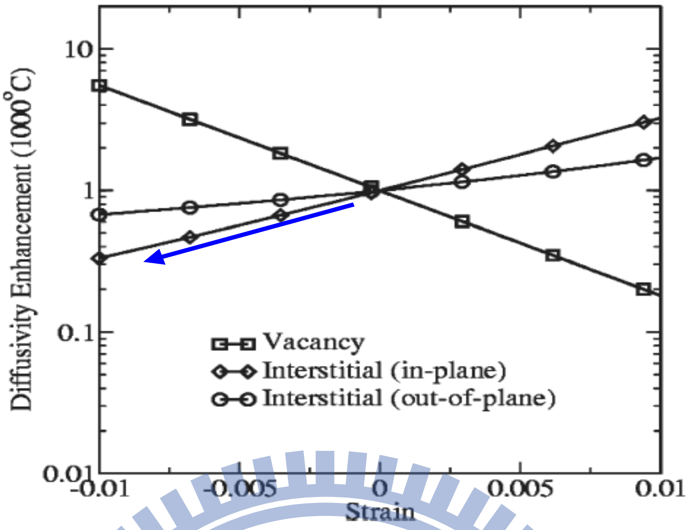

Figure 5.4.2 Under compressive strain, interstitial sites in lattice were reduced, and vacancy sites were increased. (P.R. Chidambaram, et. al, TED, 2006)

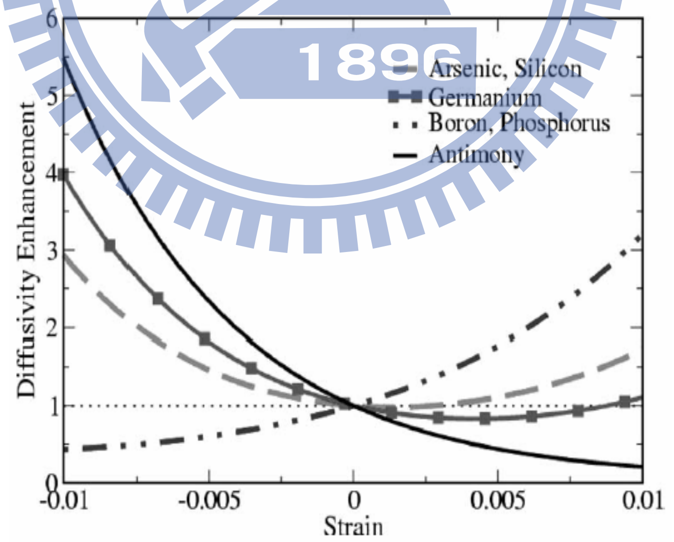

Figure 5.4.3 Boron was an interstitial diffuser then Boron diffusion was retarded under compressive strain of epitaxial SiGe layer. (P.R. Chidambaram, et. al, TED, 2006)

- **Transconductance and Total Resistance performance of ESC devices**

Fig. 5.4.4 and Fig. 5.4.5 show the Vt roll off and Gm improvement on the embedded SiGe channel (ESC) pFETs and conventional strained Si pFETs (S/D SiGe pFETs), respectively. Because LDD implanted Boron was retarded to show less diffusion length and the optimized well implant and As pocket implant, a better Vt curve of ESC devices can be obtained as well as better drain induced barrier lowering (DIBL). Due to the higher hole mobility in SiGe than it in Si channel, Fig. 5.4.5 demonstrates that the ESC p-FETs show 26% Gm performance enhancement higher than that of the strained Si pFETs with the S/D SiGe under the comparable position of threshold voltage (Vth).

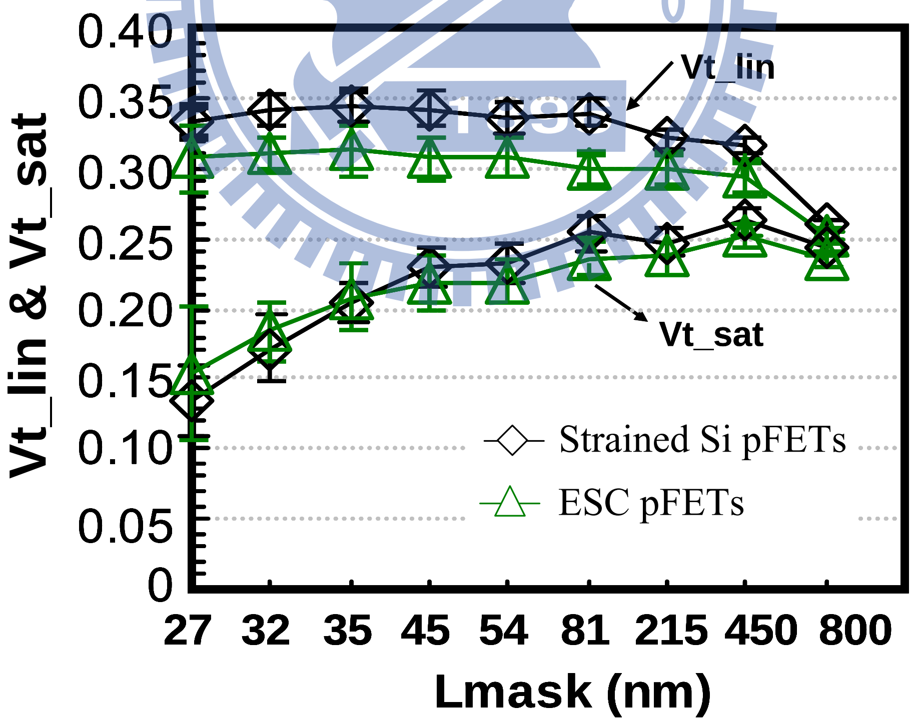

Figure 5.4.4 The ESC device demonstrates slightly better or comparable Vth to that of the conventional strained Si pFETs with the Source/Drain (S/D) SiGe devices.

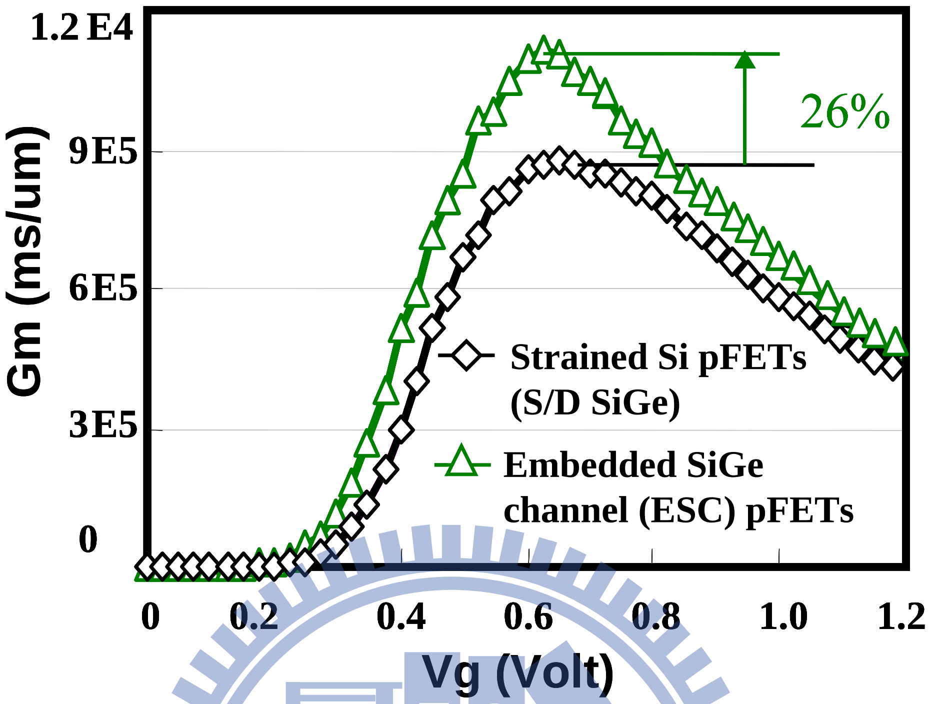

Figure 5.4.5 The ESC device shows 26% pFET Gm gain higher than that of the conventional strained Si pFETs with the Source/Drain (S/D) SiGe devices.

Higher hole mobility and Gm improvement can lead to the better device performance in the strained SiGe channel of the ESC pFETs than the strained Si pFETs. Fig. 5.4.6 shows a clear difference in the slop between the control (strained Si with S/D SiGe device) and the ESC PFET device in the R_{lin} (Resistance in the linear region of I-V curve) versus Lg, mask (gate length by mask) plot [19]. This obvious difference in slopes result from a 26% enhancement in transconductance gain by the higher carrier transport mobility for the ESC PFETs than for the control wafer under the comparable effective gate length, Lg,eff, which was electrically extracted by Terada method in the linear region of current-voltage relationship.

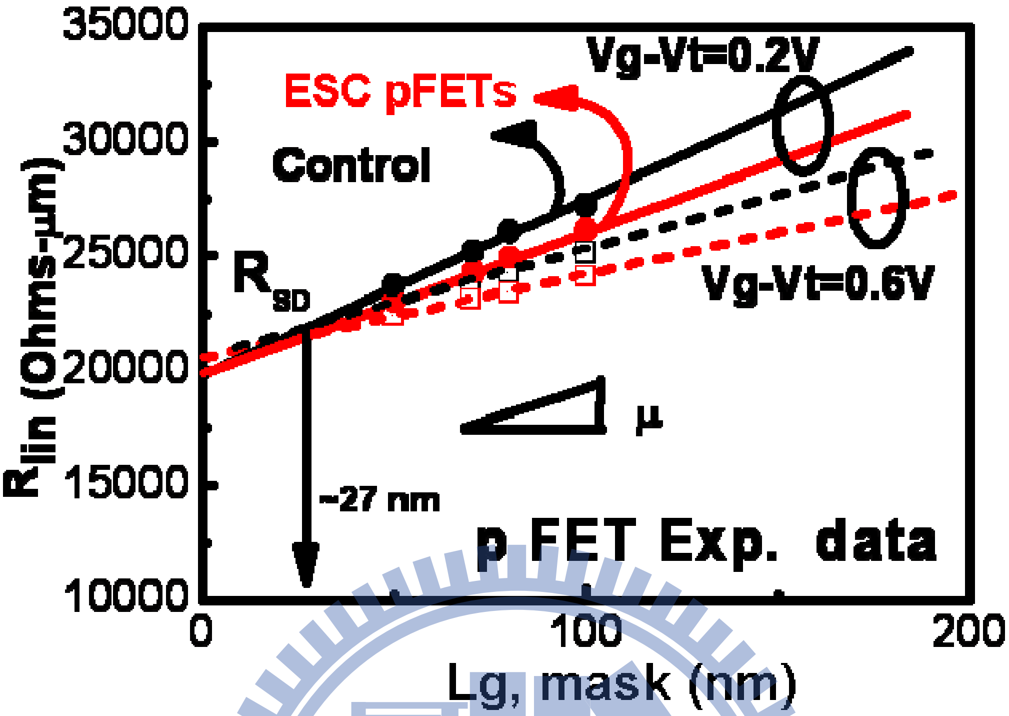

Figure 5.4.6 R_{lin} as a function of gate length showing mobility enhancement for ESC pFETs device.

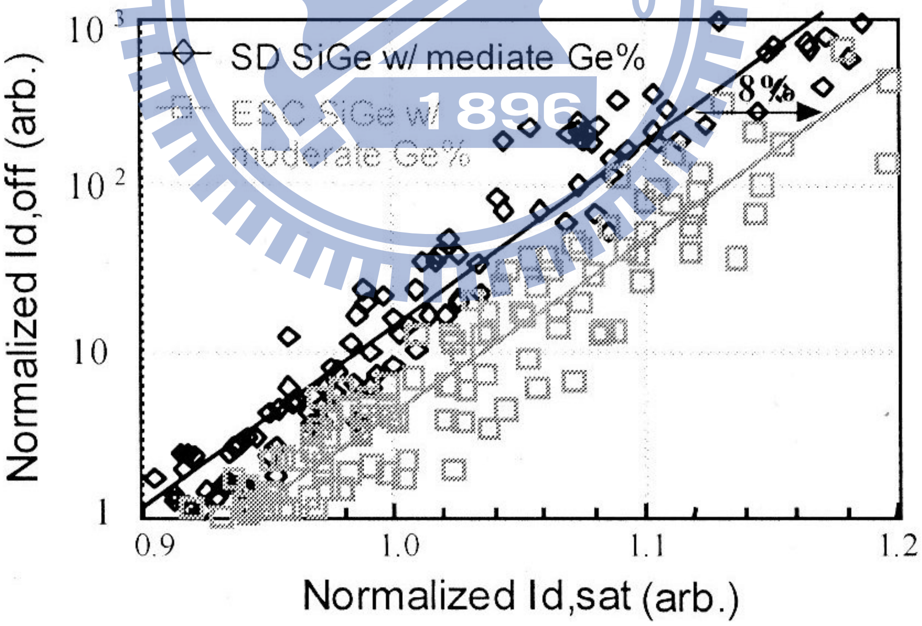

Figure 5.4.7 Ion-Ioff characteristic of PFET devices showing a performance improvement gain of 8% for ESC wafers. No other strain element such as compressive stressed nitride liner was used in either the control or the ESC devices.

In fact, the effect of this increased mobility can be seen in the Ion-Ioff characteristics shown in Fig. 5.4.7. In order to isolate the higher mobility effect of embedded SiGe channel alone, no other strain element such as compressive stressed nitride liner was incorporated in either the control or the ESC PFET devices. Vt roll-off and overlap capacitance were well matched. At a fixed Ioff value, the drive current gain of ESC PFETs with moderate Ge content is ~8% higher than that of the control devices. On the other hand, because long channel Si region can't be etched away by the etch-2 process, a partial SiGe channel is formed at the long channel device for SPICE model.

- **Id_Vgs and Id_Vds characterization of ESC devices**

As shown in Fig. 5.4.8, Id-Vgs plot shows higher Ion drive current for ESC devices than for the control of strained Si with S/D SiGe devices. At the same time, one can see that better swing slope of ESC device than that of control device due to higher carrier mobility in the SiGe material. On the other way, SiGe channel devices, in general, would show higher Ioff current than strained Si devices due to the small band-gap of SiGe material. Therefore, we use the additional Arsenic well implant about 2E12/cm2 to suppress Ioff in our embedded SiGe channel devices (ESC) the same as control strained Si devices and then do the clear deice performance comparison. Fig. 5.4.9 shows the Id_Vds characteristics of the control and ESC PFET. ESC device showed higher drive current at both linear region and saturation region than that of control device.

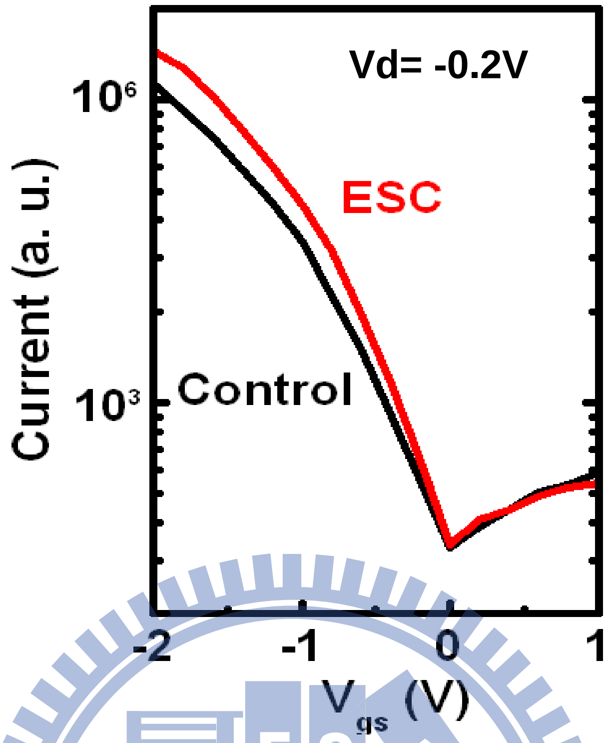

Figure 5.4.8 Ids-Vgs characteristic of 28nm Lg PFET with the control wafer and the ESC device.

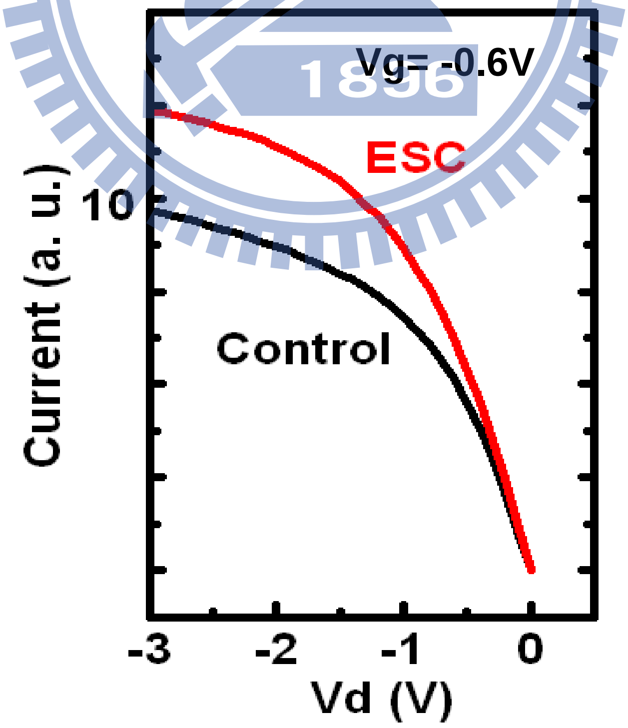

Figure 5.4.9 Ids-Vds characteristic of 28nm Lg PFET with the control wafer and the ESC device.

5.4.3. Embedded SiGe Channel (ESC) simulation

Fig.5.4.10 simulates the hole mobility in the ESC structure and the strained Si structure with the S/D SiGe. We calculate the hole mobility by the change of effective mass and carrier scattering with the stress treatment and different Ge concentration in the SiGe channel. The stress distribution is simulated by ANSYS simulation tool firstly and the SiGe effective mass, the change of scattering rate, corresponding hole mobility with stress is calculated by the 6x6 k.p model. Both SiGe material in the channel and compressive stress in the channel benefit the higher hole transport mobility. On the other hand, we also can observe that when the epitaxial SiGe layer shares more Si substrate region in the hole conduction channel, which means the proximity of the intra-recess spacing, X becomes smaller, the hole mobility in the strained Si can be further enhanced. Hence, the average hole mobility in the device increases with decreasing Si region X. The hole mobility of the ESC structure is enhanced to a highest value as the epitaxial SiGe layer filled up all the channel region. Based on the simulation, ESC structure has the hole mobility about 56% higher than that of the S/D SiGe structure. However, only 26% Gm gain enhancement of ESC pFETs devices is observed in our experiment. It is conjectured to existence of the channel resistance and S/D contact resistance [20]. The superior p-FETs performance of the ESC structure is considered as a highly potential candidate in the future nano-pMOSFETs node and FinFETs. Fig.5.4.11 shows the remaining Si region, X, by etch-2 related to channel Si stress enhancement. By growing a

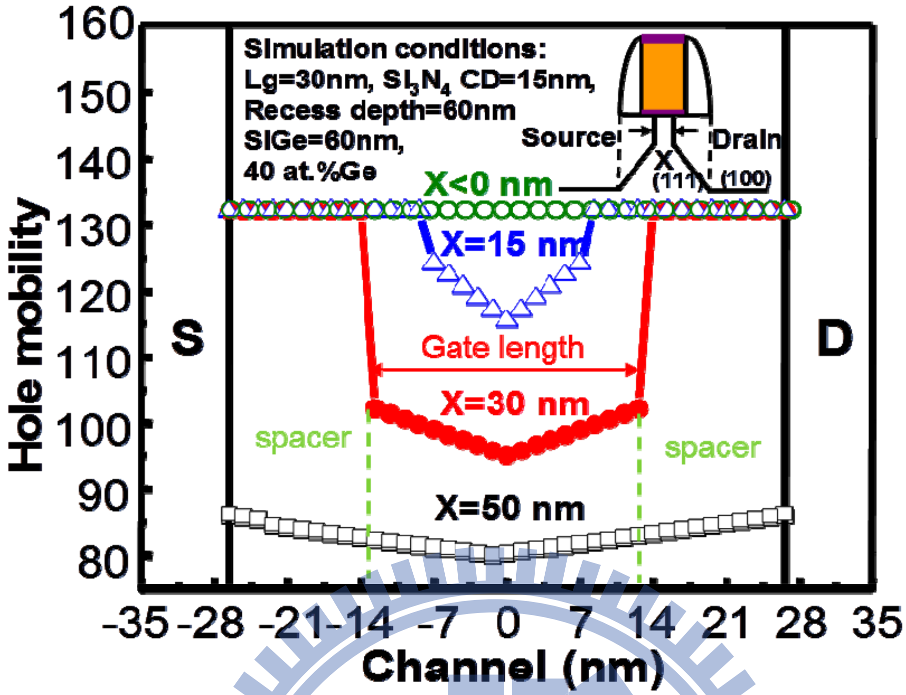

Figure 5.4.10 Simulates the hole mobility of the ESC structure and S/D SiGe structure. The epitaxial SiGe layer sharing more Si channel shows higher channel Si stress induced mobility enhancement.

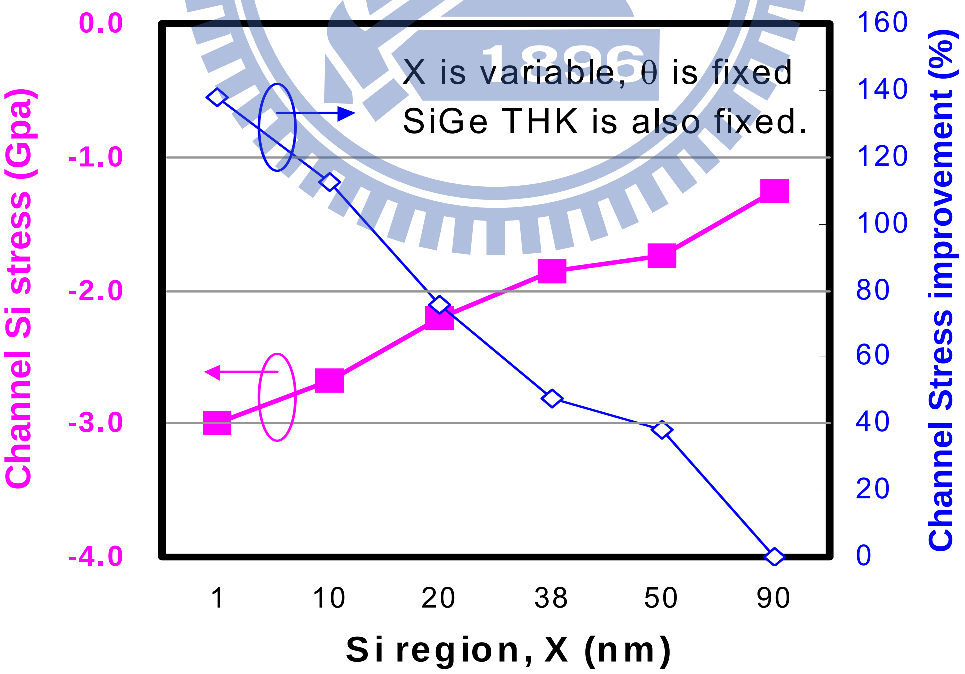

Figure 5.4.11 The channel stress is dependent of Si region, X, intra-spacing of source to drain recess, created by Si lateral etch-2

compressive SiGe layer to fill up the channel region, the ESC structure also enabled to exhibit compressive stress for carrier mobility enhancement. Combined high mobility and compressive stress, ESC device could show better device performance.

5.4.4. Gate oxide integrity of ESC devices

Fig. 5.4.12 shows the XPS analysis data and indicates that only the Si-O bonding is observed in our ESC devices. No Ge-O bonding observed for the grown SiGe layer on the SiO_2 reflects that the in-situ etch does not damage the gate oxide of the SiO_2 at 700˚C and the epitaxial SiGe deposition does not react with the suspending stacked gate dielectric of the SiO_2 to form GeO_X at the deposition temperature of 700˚C. The chemical equations for describing the formation of the embedded SiGe channel (ESC) structure are expressed as below:

$$2Cl_{2(g)} + Si_{(s)} \rightarrow SiCl_{4(g)} \qquad T=700^{\circ}C, \qquad (1)$$

$$4HCl_{(g)} + Si_{(s)} \rightarrow SiCl_{4(g)} + 4H_{(g)} \qquad T=700^{\circ}C, \qquad (2)$$

$$4HCl_{(g)} + SiO_{2(s)} \rightarrow SiCl_{4(g)} + 2H_{2(g)} + O_{2(g)} \qquad T>1800^{\circ}C, \qquad (3)$$

$$12HCl_{(g)} + Si_3N_{4(s)} \rightarrow 3SiCl_{4(g)} + 4\ NH_{3(g)} \qquad T>1800^{\circ}C, \qquad (4)$$

$$GeH_{4(g)} + SiO_{2(s)} \rightarrow SiH_{4(g)} + 2GeO_{2(s)} \qquad T>1800^{\circ}C. \qquad (5)$$

In the literature, the conventional SiGe channel without Si surface passivation formed the gate dielectric with the interface composed of GeO_X/SiGe, which caused numerous interfacial defects and became one of the most crucial issues in the SiGe channel pMOSFETs [21-22]. Then, Si surface passivation is necessary to avoid GeO_X formation and a thin Si passivation layer about 1nm with good uniformity is very difficult for mass production. Therefore, this approach of the ESC structure can achieve the benefit of the SiGe channel without Si passivation to obtain the superior interface quality in addition to the higher channel mobility in SiGe.

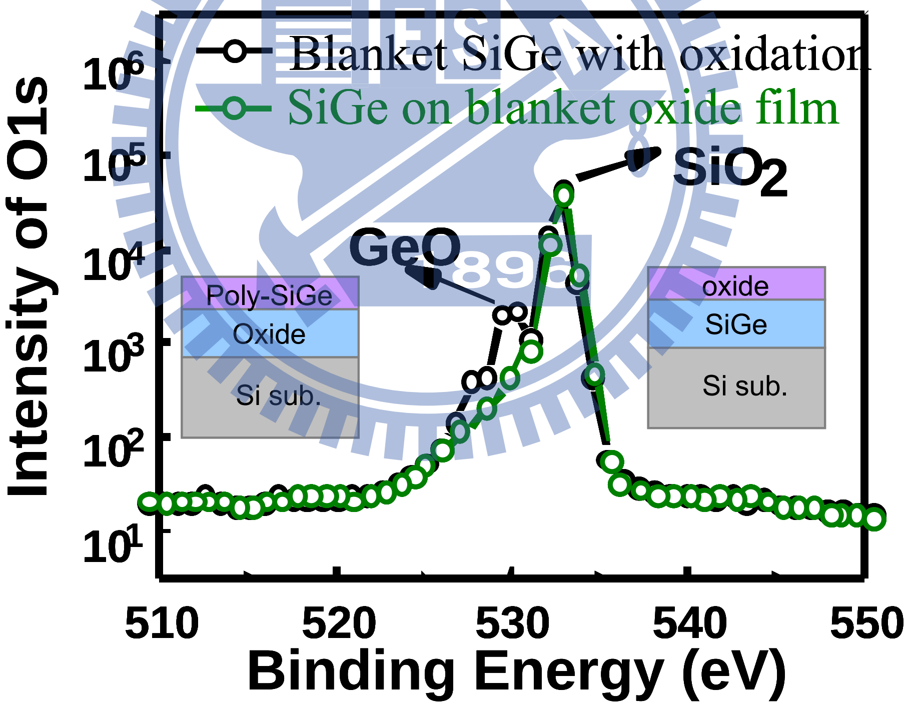

Figure 5.4.12 It shows the XPS analysis data and indicates no Ge-O bonding observed for the grown SiGe layer on the SiO_2, which means only the Si-O bonding is observed in our ESC device.

5.4.5. Leakage current performance of ESC devices

Fig. 5.4.13 compares the gate leakage current between ESC device and control strained Si devices with S/D SiGe. The comparable value between these two devices demonstrates that the insulator layer and the interface between SiO_2 and semiconductor surface is good with the only Si-O bonding, no Ge-O bonding observed in ECS device. Due to the process design of the embedded SiGe channel, it can not demonstrate full SiGe channel for large gate length (Lg), such as MOS capacitor. Therefore, we can not extract interfacial defect (Dit) as an index to evaluate the integrity of the gate oxide, instead, we use gate leakage current as an indicator for the integrity of the gate oxide of the ESC device.

In addition to the check of the gate oxide quality, Fig.5.4.14 shows the reliability of the voltage shift for our ESC devices. It is also comparable to the control strained Si pFETs for the long time constant voltage stress. As could be seen from XPS data as mentioned above, the comparable reliability of the ESC to strained Si ones could be also ascribed to the superior gate oxide integrity. Even though there is no Ge-O bonding formation of the ESC structure in our D-C electrical characterization, a more precise method to detect if on not GeO_x formation exists in the ESC devices is to use SRAM yield analysis, which enables to characterize millions of devices. We hope the promising ESC structure can provide an applicable SiGe channel for the next generation and beyond.

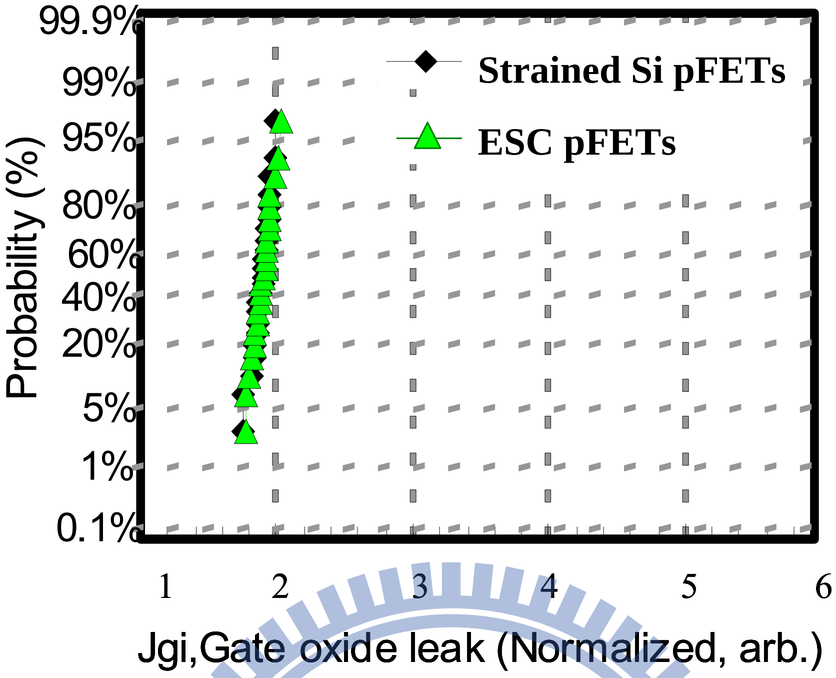

Figure 5.4.13 ESC device shows comparable Gate oxide leakage performance with the strained Si pFETs because there is no GeO_x composition during SiGe deposition according to the XPS analysis.

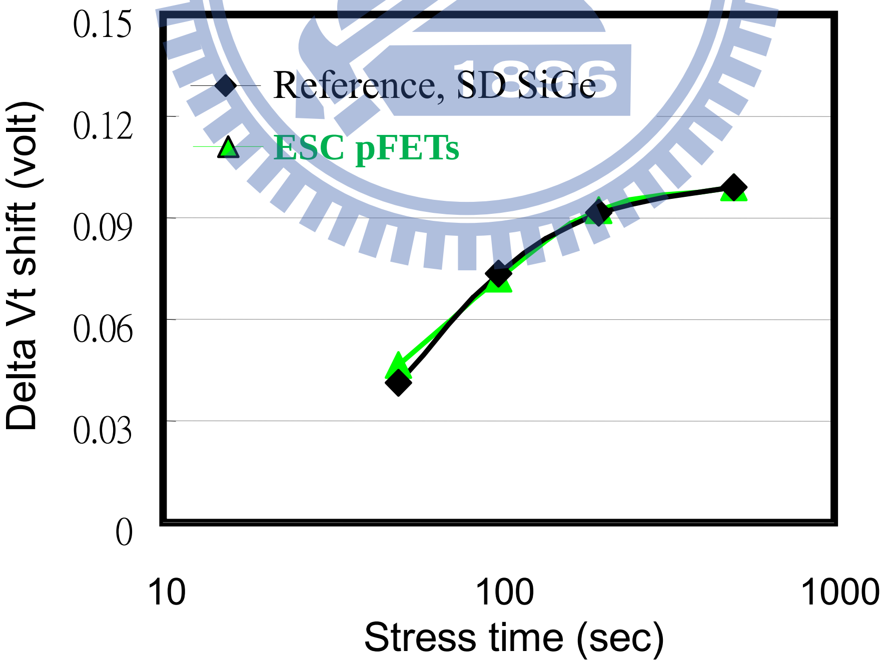

Figure 5.4.14 The constant voltage stress of the ESC device shows the same delta Vth shift with the strained Si pFETs with the S/D SiGe. No GeOx induced further Dit increment for ESC pFETs.

5.5 Summary

A novel technique of creating an embedded SiGe channel (ESC) structure without Si surface passivation shows a pFETs Gm gain of 26% higher than that of the conventional strained Si pFETs with the source/drain (S/D) SiGe for the 28 nm pMOSFETs. Better Rsd and device gain of 8% in the Ion-Ioff plot and improved swing slop in the Id-Vgs characteristics all indicate enhanced hole mobility in the ESC PFETs than the control wafer. According to the XPS analysis, the gate oxide leakage and the reliability of the constant voltage stress were also examined to recognize the superior SiGe/SiO2 interface with the Si-O bonding, no Ge-O bonding. The novel etch process to create the ESC structure is considered as a very promising technique for the 28 nm pMOSFETs and future N/P SiGe channel in FinFETs.

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Chapter 6

Summary and Conclusions

The degree of strained-SiGe relaxation remarkably affected the channel stress and the formation of the defects in the underlying Si substrate as well as the wafer bending while the MSA was applied to the S/D strained-SiGe in 28nm PMOSFET devices. Low-energy As implantation to cause shallower Rp in the strained-SiGe surface induced low-level 11% of relaxation and did not generate defects in the underlying Si, because the remaining strained-SiGe was sufficiently thick to resist wafer bending by the tensile stress associated with MSA thermal treatment. However, moderate relaxation 51% of the strained-SiGe by medium-energy As implantation revealed the partly relaxed SiGe with lower shear stress of yielding deformation was unable to withstand the significantly compressive stress of the surface expansion to form defects in the underlying Si substrate during MSA heating and more surface contraction of high CTE of SiGe to cause over-bending in the tensile state during MSA cooling. In addition, the 75% relaxation of the SiGe layer by high-energy implantation would for lots of interfacial misfit dislocations and low-density of coherent bonding with Si substrate. The highly relaxed strained-SiGe film is then deformed freely along with the externally thermal stress direction and would not cause any residual strain to the underlying Si substrate during the MSA thermal cycle. Therefore, proper implantation conditions were chosen to provide a relaxation-less strained-SiGe and boost the channel stress, achieving a 10% current gain. The defect-free underlying Si in millisecond-annealed 28 nm PMOSFETs devices exhibits a decrease in the junction leakage current by four orders of magnitude.

We have concluded that the degree of strained-SiGe relaxation significantly caused the wafer bending as well as the defect formation in the underlying Si substrate when MSA was applied to the relaxed strained-SiGe wafers. In either cases of post-SiGe implant or post-SiGe soak annealing or in-situ Ge at.% resulting in the relaxation of strained SiGe, low relaxation less than 10% did not cause large SiGe wafer bending during the MSA. Upon the MSA, the medium relaxation level indeed caused significant SiGe wafer bow height from the compressive to tensile state as well as the defect formation in the underlying Si substrate.

A design rule of S/D SiGe with different active area sizes to form the defects in the underlying Si substrate during MSA has been also proposed for the 28nm PMOSFETs. As the ratio of total SiGe area to whole wafer was less than 10%, the wafer bow height was less than 100 um after the MSA and it was acceptable for the following lithographic limitation. Therefore, a well-designed ratio of global SiGe area to whole wafer area is critical to prevent the large wafer warpage in the integration of SiGe and MSA and get rid of the lithographic limitation. We also came out the critical SiGe area to avoid defect formation in the underlying

Si substrate during the MSA. With the local SiGe area size smaller than 0.2um^2, upon the MSA, the defect formation in the underlying Si and the junction leakage of SiGe to the substrate could be controlled as low as those for non-MSA process. Therefore, a well-designed rule of global SiGe area ratio to whole wafer and local SiGe area size were proposed to avoid defect formation in the underlying Si substrate and junction leakage for 28nm CMOSFETs volume production.

A novel technique of creating an embedded SiGe channel (ESC) structure without Si surface passivation shows a pFETs Gm gain of 26% as well as Ion_Ioff performance gain of 8% higher than those of conventional strained Si pFETs with the source/drain (S/D) SiGe for the 28 nm pMOSFETs. Better S/D resistance (Rsd) in the resistance versus gate length plot and improved swing slop of Id_Vgs plot indicate the higher mobility in the ESC devices. According to the XPS analysis, the gate oxide leakage and the reliability of the constant voltage stress were also examined to recognize the superior SiGe/SiO2 interface with only the Si-O bonding and no Ge-O bonding. The novel etch process to create the ESC structure is thus considered as a very promising technique for the 28 nm pMOSFETs and future N/P SiGe channel in FinFETs.

Chapter 7

Future Prospects

There are some interesting and important topics that are valuable for the future further research about the strained-SiGe relaxation induced defect formation in the underlying silicon substrate and a significant wafer bending during the millisecond annealing (MSA) process for 28 nm node PMOSFETs and beyond.

(1) To figure out if or not there is process window for the MSA temperature independency to show defect-free in the underlying Si substrate whiles the S/D SiGe and MSA were combined in the integrated process of CMOS and beyond. Lowering MSA temperature would provide a small thermal stress to avoid defect formation in the underlying silicon substrate and wafer bending.

(2) Further thinking about the studying if there is orientation dependency with MSA (Flash anneal or Laser scanning anneal (LSA)), varying LSA scanning direction on relaxed strained-SiGe to come out defect-free in the underlying Si and result in better junction leakage. As we knew that different SiGe lattice orientation to LSA scan direction would show different immunity to MSA induced wafer warpage, which can widen LSA temperature window. In general, (100) lattice plane displays high immunity to strain deformation than that of (110)

lattice plane. Therefore, by good LSA scanning direction we also can obtain defect-free and small wafer bending for S/D SiGe and MSA process.

(3) Although the post-SiGe implantation and soak anneal would cause strained-SiGe relaxation and defect formation, one can study the possibility of non-implant and non-thermal process or low thermal flow after S/D strained SiGe (due to high-k/metal-gate last process) for CMOS device.

(4) To investigate a well-designed film scheme of SiGe multi-layer with higher Ge content that enables to resist post-soak anneal induced strained-SiGe relaxation and defect formation in the underlying Si substrate. Designing a grading Ge content film structure would provide a better immunity to form in-situ dislocation in the S/D SiGe and prevent the relaxation by the post-SiGe thermal process.

To further boost and enhance the performance of p-MOSFETs and beyond by implementing the embedded SiGe channel without silicon surface passivation possessing gate oxide integrity:

(5) To investigate how a high Ge content SiGe layer with dislocation-free could be achieved to provide the better device performance and lower junction leakage in the embedded SiGe channel structure.

(6) To fabricate embedded SiGe channel at FinFET structure, which is a promising structure

for the 22nm, and 14nm CMOSFETs as well as beyond. The novel technique of fabricate embedded SiGe channel is a good candidate for the 3-D transistors because it shows a simple process flow of integrating SiGe channel without gate oxidation concern in the CMOSFET.

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簡歷

姓名: 游明華

性別: 男

出生年月日: 民國六十二年三月三十日

籍貫: 台灣省宜蘭縣

地址: 宜蘭縣宜蘭市力行街 125 號

學歷: 清華大學材料工程系

(80 年 9 月～84 年 6 月)

國立交通大學材料工程研究所碩士班

(84 年 9 月～86 年 6 月)

國立交通大學電子工程研究所博士班

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Study on the Electrical Characteristics of the PMOSFETs with the Strained SiGe S/D and Embedded SiGe Channel for the 28 nm Node and Beyond