國 立 交 通 大 學

電子物理學系

碩士論文

氨電漿對下閘極多晶矽薄膜電晶體之影響

Effects of NH_3 Plasma Treatment on Bottom Gate Poly-Silicon Thin-Film Transistors

研 究 生：陳儀儒

指導教授：趙天生 博士

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指導教授：趙天生 博士　　Advisor : Dr. Tien-Sheng Chao

研 究 生：陳儀儒　　Student : Yi-Ju Chen

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A Thesis

Submitted to Department of Electrophysics

College of Science

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of Master of Science

in Electrophysics

July 2013

Hsinchu, Taiwan, Republic of China.

中華民國 一百零二 年 七 月

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摘要

首先，本研究深入探討氨電漿對於下閘極多晶矽薄膜電晶體鈍化效應之影響。這些元件經過數種條件的氨電漿製程，包括不同階段、不同製程時間長度，以及不同功率的電漿製程。

相較於沒有經過電漿製程的元件，pre-SPC-treatment 會使元件電性變差，而 post-SPC-treatment 及 after-AA-treatment 會提升元件電性。經過 pre-SPC-treatment 的元件有最差的電性表現，而經過 after-AA-treatment 的元件則有最好的電性表現。雖然 after-AA-treatment 是鈍化缺陷最有效率的方式，但是相較於 post-SPC-treatment，經過 after-AA-treatment 的元件也受到最嚴重的離子轟擊傷害。此外，較長時間或是較高功率的電漿製程，可以較有效地提升元件電性、抑制電流突增效應(Kink Effect)。較高功率的電漿製程也可以較有效地提升閘極氧化層的品質。

隨後，本研究探討退火製程對於已接受過電漿製程之多晶矽薄膜電晶體的影響。我們推測在氮氣的環境之下，退火或許可以消除乾蝕刻期間，在閘極氧化層中產生的電洞缺陷。此外，經過退火的元件，其電性表現主要受到幾個機制影響，分別是： (1)退火消除閘極氧化層中的電洞缺陷、(2)退火製程期間，氮自由基及氫自由基被釋出，並喪失鈍化效應、(3)退火製程後，殘餘的鈍化效應、(4)氨電漿製程中所造成的電漿傷害。

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Advisor : Dr. Tien-Sheng Chao **Student : Yi-Ju Chen**

Department of Electrophysics

National Chiao Tung University

Abstract

First, the passivation effect of NH_3 plasma treatment on bottom gate poly-Si TFTs is thoroughly discussed. The poly-Si TFTs are exposed to NH_3 plasma with several conditions, including diverse stages, various plasma treatment time, and different plasma power.

Compared with the sample without any plasma treatment, pre-SPC-treatment degrades device performance; however, post-SPC-treatment and after-AA-treatment improve device performance. The poly-Si TFTs with pre-SPC-treatment exhibit the worst performance, and those with after-AA-treatment ones exhibit the best performance than the counterparts. Although after-AA-treatment is the most efficient technique to passivate traps, the poly-Si TFTs with after-AA-treatment suffer from the heaviest ion bombardment damage than those with post-SPC-treatment ones. In addition, longer plasma treatment time or higher plasma power will enhance performance and alleviate kink effect more effectively. The plasma treatment with higher plasma power will also strengthen the bulk oxide quality more significantly.

Second, the impacts of post-metal-annealing on plasma-treated poly-Si TFTs are systematically investigated. We hypothesize that PMA in N_2 ambient is a method to annihilate the hole traps in the gate oxide generated by plasma dry etching. Moreover,

the performance of the poly-Si TFTs with PMA are mainly attributed to the combination of following mechanisms: 1) the elimination of the hole traps in the gate oxide by PMA, 2) the out-diffusion of nitrogen and hydrogen radicals during PMA processing, 3) the remaining passivation effect by NH_3 plasma, and 4) the plasma-induced damage by NH_3 plasma.

誌謝

Time goes fast ~ 轉眼間，碩班生涯即將結束了。碩班的兩年期間，很幸運的遇到許多貴人，也受到許多人的幫助。首先要感謝指導老師—趙天生老師。無論是做研究的態度，或者是待人處事的學問，老師都是我的模範。謝謝老師提供良好的研究環境，讓學生有許多學習、成長的機會，並且在研究遇到瓶頸時，給予學生方向。能夠當您的學生真的很幸運，謝謝您！

感謝廖家駿學長以及劉劭軒學長的指導。謝謝家駿學長即使在工作了，仍然在下班後專程回學校指導我。你總是很有耐心指導我許多理論及嚴謹的研究方法，並且鼓勵我閱讀各領域的文獻，讓我知道應該要時時充實自己，提升自己的視野。你對自己的高標準，以及實踐目標的能力，一直都是我的榜樣。沒有你的教導及督促，我不可能這麼順利的完成碩士學業，真的很謝謝你。感謝劭軒學長當初很有幹勁的完成這批元件，讓我可以在沒有壓力的情況下量測元件，完成碩論。謝謝你一大早陪我進NDL做實驗，以及在課業上給予協助，雖然有幾次我翹掉小咪，但我會一直記得你是一個熱心又很棒的學長！

謝謝郭柏儀學長在實驗上的幫助，讓我學習到嚴謹的實驗態度。謝謝陳昱璇學姊總是很有耐心的替我解答疑惑，熱心的借給學弟妹們妳的精美筆記，並且給予我許多實驗及課業上的幫助。感謝林哲緯學長、呂侑倫學長、呂宜憲學長、吳翊鴻學長、嚴立丞學長、張添舜學長、林哲毅學長、卓大鈞學長、郭柔含學姊、唐明慈學姊、偉斌、阿孔、小小、樂樂、小崴、可立、品烝及方晴的陪伴，讓我的碩班回憶增添不少色彩。

此外，謝謝十幾年的老友期蘭，細心的幫我修改論文文法，並時時給我鼓勵與支持，一起分享生活中的酸甜苦辣。感謝室友柔儀，幫我找了許多如何寫論文的資料，並且幫我修正文法。謝謝大學直屬學姊曼麗，到了碩班還是這麼的照顧我，認識妳真好。還要謝謝那些一路陪伴在我身邊的朋友們，因為有你們的陪伴，當我遇到挫折時，才有力量再站起來！

最後，我要感謝我的父母—陳正昌先生與林素秋女士。謝謝你們給我一個無憂無慮的成長環境，給我很多自由，一路以來支持我所做的任何決定，讓我有機會去嘗試許多挑戰，並且在我低潮時，給我許多建議及陪伴。因為有你們如此堅強的後盾，我才可以心無旁騖的完成學業，邁入人生的下一段旅程。

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Chapter 1

Introduction

1.1 Background

1.1.1 Poly-Si TFTs

Ongoing researches for polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted intense attention recently, due to their advantages over amorphous silicon thin-film transistors (a-Si TFTs), such as higher carrier mobility, lower leakage, and higher drive current. Thus, poly-Si TFTs have been widely used in large-area flat panel displays, for example, active-matrix liquid crystal displays (AMLCDs) and active matrix organic light-emitting displays (AMOLEDs) [1.1]-[1.2].

However, the grain boundaries and intra-grain defects degrade carrier transport [1.3]; therefore, they exert a profound influence on the device performance. For this reason, reducing defects inside the poly-Si layer plays a crucial role in optimizing the performance of poly-Si TFTs. It has been reported that poly-Si, formed by the crystallization of a-Si, results in larger grain size and better electronic properties than as-deposited poly-Si [1.4]. In order to improve the characteristics of poly-Si TFTs, there are various techniques in the fabrication which are aimed at two characteristics: 1) enlargement of grain size, and 2) removal of defects in poly-Si films.

Various techniques have been used to crystallize the a-Si into the poly-Si, for instance, solid phase crystallization (SPC), rapid thermal annealing (RTA), excimer laser crystallization (ELC), and metal-induced lateral crystallization (MILC). For SPC process, although it usually takes a long crystallization time of about 20-60 hours at 600℃, its advantages, such as low cost and superior uniformity, make it a commonly used technique [1.5]. RTA is a high temperature (>600℃) process that can complete

crystallization in a short period of time, but this results in films with high defect density [1.6]-[1.7]. Compared with SPC and RTA, ELC can be considered a low temperature process. Even though it is capable of producing poly-Si films with low defect density, it suffers from high initial setup cost, high process complexity and poor uniformity [1.8]. Furthermore, MILC has the problem with metal residues which lead to unacceptable leakage current [1.9]-[1.10].

To passivate the grain boundaries and intra-grain defects, various passivation methods such as hydrogen plasma treatment, hydrogen implantation, and hydrogen-containing nitride film deposition have been applied [1.11]-[1.13]. Although hydrogen passivation eliminates defects and improves the performance of poly-Si TFTs effectively, the poly-Si TFTs after hydrogen passivation suffer from hot-carrier, which might degrade the reliability [1.14]. Because the formation of weak Si–H bonds after hydrogen passivation are easily-broken under hot-carrier stress, F, N_2, NH_3 plasma treatment are used to obtain a better hot-carrier reliability than H_2 plasma treatment [1.14]-[1.16].

1.1.2 Plasma Treatment

Poly-Si thin film consists of different oriented grains, containing many grain boundaries and intra-grain defects. These defects act as trap centers and degrade carrier transport, resulting in unacceptable characteristics of poly-Si TFTs [1.17]. The deep states, which originate from the dangling bonds at grain boundaries, have a faster response to hydrogenation. These deep states degrade the threshold voltage and the subthreshold swing. The tail states, which originate from the strain-bond-related intra-grain defects, respond slower to hydrogenation with an onset period of 4 to 12 hours depending on the grain size. And these tail states degrade the field-effect mobility and minimum leakage current [1.3]. In order to obtain superior

characteristics of poly-Si TFTs, numerous techniques have been used to enhance the device performance by reducing the trap density or increasing the grain size of the polysilicon [1.4].

H_2 plasma treatment, also called hydrogenation, is an effective method to passivate defects and improve the performance of poly-Si TFTs. Unfortunately, poly-Si TFTs after hydrogen passivation suffer from hot-carrier issue because the formation of weak Si–H bonds are easily-broken during hot-carrier stressing [1.15]. Also, poly-Si TFTs with H_2 plasma treatment loss their passivation effect after subjecting to high temperature (>500℃) annealing [1.16].

N_2 plasma treatment can effectively improve device characteristics, such as field-effect mobility, subthreshold swing, minimum leakage current, and on/off current ratio [1.14]. Furthermore, N_2 plasma treatment has been proposed to attenuate hot-carrier degradation. Poly-Si TFTs with N_2 plasma treatment have better hot-carrier reliability than using H_2 plasma treatment, due to strong Si–N bonds with higher bonding energy that would replace the weak Si–H bonds.

Because of the passivation effect of nitrogen and hydrogen radicals, NH_3 plasma treatment has also been studied. Similar to N_2 plasma treatment, NH_3 plasma treatment can passivate defects, improve the performance and the hot-carrier reliability of poly-Si TFTs [1.18]-[1.19]. Besides, it is found that NH_3 plasma pretreatment before SPC annealing significantly shortens the a-Si film crystallization time and simultaneously improves device performance and hot-carrier reliability [1.20]. These improvements can be attributed to the combination of following mechanisms: 1) hydrogen radicals that enhance the formation of seed nuclei which reduces crystallization time, and 2) nitrogen and hydrogen radicals pile-up at SiO_2/poly-Si interface and terminate the dangling bonds at the grain boundaries, leading to improved performance.

1.1.3 Bottom Gate TFT Structure

Bottom gate TFTs as shown in Fig. 1-1(a), have been widely used because of good match with process integration of conventional SRAMs. Their channel areas are good isolated from parasitic electric field caused by under layers [1.21]. Also, bottom gate TFTs are commonly used as the switching elements in AMLCDs fabrication. It has been reported that bottom gate TFTs can be easily fabricated by the laser annealing of a-Si film for the active layer [1.22], allowing higher circuit density and improving topography compared with top gate devices [1.23]. In addition, because the gate electrode is located under gate insulator for bottom gate structure, the channel is not damaged by the plasma radiation during gate insulator deposition. Therefore, bottom gate TFTs have larger on-state current (I_{ON}) than the top gate TFTs [1.24].

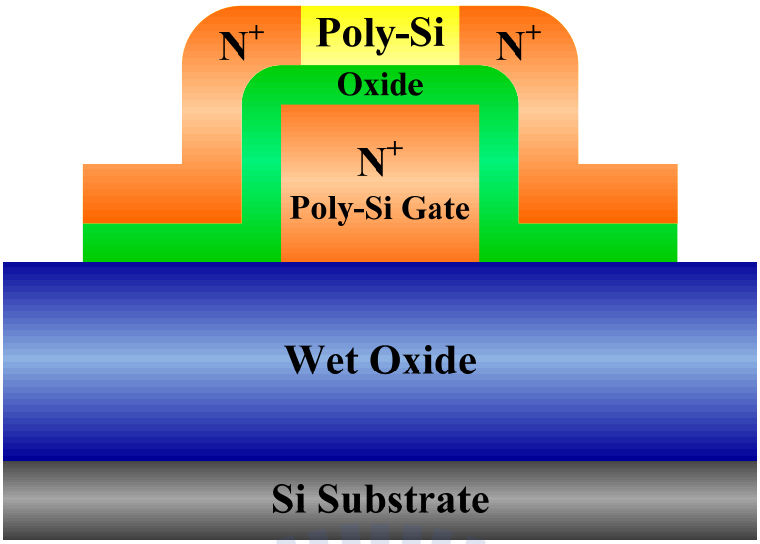
Unfortunately, compared with top gate devices as shown in Fig. 1-1(b), smaller grain size and irregular grains of the poly-Si channel result in unacceptable characteristics of bottom gate TFTs [1.25]. Besides, because the gate is located under the active layer, it is difficult to fabricate a bottom gate TFT with its gate edges self-aligned to its source/drain. Thus, bottom gate TFTs suffer from significant performance variation, large parasitic capacitance and poor scalability owing to the misalignment effect [1.23]. Although some self-aligned bottom gate TFTs processes have been proposed, the device processes were too complicated to be utilized [1.26].

1.2 Motivation

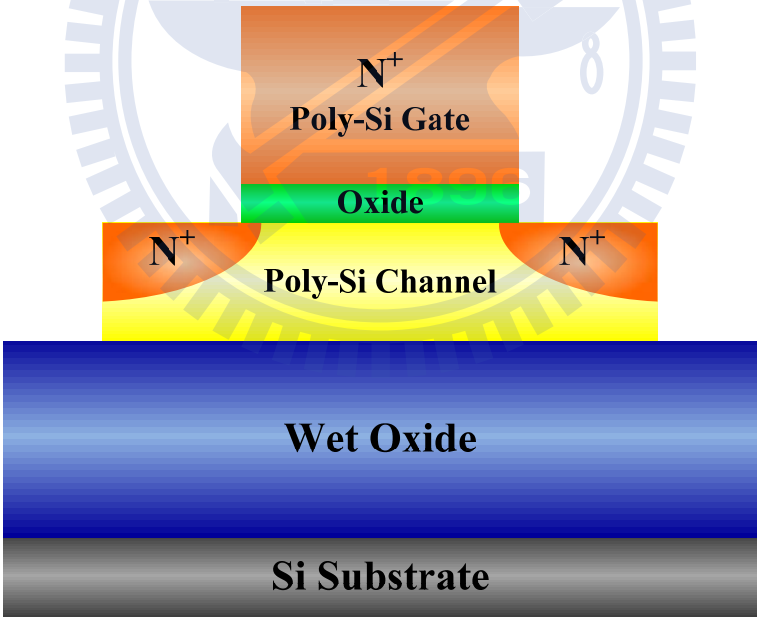
It is known that NH_3 plasma treatment is an effective method to passivate defects that will improve the performance and the hot-carrier reliability of poly-Si TFTs. Moreover, it has been proposed that NH_3 plasma pretreatment before SPC annealing not only shortens the a-Si film crystallization time significantly, but also improves device performance and hot-carrier reliability simultaneously. In fact, hydrogen

radicals enhance the formation of seed nuclei, which reduces crystallization time. Meanwhile, nitrogen and hydrogen radicals terminate the dangling bonds at the grain boundaries. It is because of these two events that strong Si–N bonds are formed and then the trap density is decreased.

Although there are several literatures discussing the passivation effect of NH_3 plasma treatment for top gate devices, there are few for bottom gate poly-Si TFTs. In addition, because the channel is located over the gate electrode for bottom gate structure, the poly-Si channel is directly exposed to NH_3 plasma. The passivation effect of bottom gate structure may be different to top gate structure. Thus, the passivation effect of NH_3 plasma treatment for bottom gate poly-Si TFTs will be thoroughly studied in this study. The poly-Si TFTs will be exposed to NH_3 plasma with several conditions, including diverse stages, various plasma treatment time, and different plasma power. The influences of NH_3 plasma with different conditions on bottom gate poly-Si TFTs will also be systematically investigated.



(a)



(b)

Fig. 1-1 (a) Bottom gate TFTs. (b) Top gate TFTs.

Chapter 2

Device Fabrication and Experimental Setup

2.1 Introduction

The process flow, experimental procedure, measurement, and equipment setup will be introduced in detail. In addition, the methods to extract the important electrical parameters will also be proposed.

2.2 Experimental Procedure

Fig. 2-1 shows the process flow of the poly-Si TFTs in this study, and the fabrication processes are shown in Fig. 2-2 (a)-(e). It is important to emphasize that each wafer was exposed to NH_3 plasma only once. The NH_3 plasma treatments were performed by plasma-enhanced chemical vapor deposition (PECVD), using pure NH_3 gas of 200 sccm, substrate temperature of 300℃, RF power of 50 W or 200 W, and the plasma treatment time varied from 15 to 120 min.

First, the thermal oxide of 5000 Å was grown on the 6 inch silicon wafer by horizontal furnace. The poly-Si film of 1500 Å was deposited as the gate electrode by low-pressure chemical vapor deposition (LPCVD) and implanted with phosphorous (50 keV at 5×10^{15} cm^{-2}) (Fig. 2-2 (a)). After gate electrode patterning, a 200 Å thick tetraethyl orthosilicate (TEOS) oxide was deposited as the gate insulator. Then, the a-Si film of 500 Å was deposited. Some wafers were exposed to NH_3 plasma, which was defined as “pre-SPC-treatment”, and the other wafers were skipped in this step (Fig. 2-2 (b)).

The a-Si was crystallized by solid phase crystallization (SPC) at 600℃ for 24 hr to transform the a-Si into poly-Si. The source/drain were implanted with phosphorous

(15 keV at 5×10^{15} cm^{-2}) and activated by annealing at 600℃ for 24 hr in N_2 ambient. Some wafers were exposed to NH_3 plasma, which was defined as "post-SPC-treatment", and the other wafers were skipped in this step (Fig. 2-2 (c)).

After defining the active area, some wafers were exposed to NH_3 plasma, which was defined as "after-AA-treatment", and the other wafers were skipped in this step (Fig. 2-2 (d)). Then, the 5000 Å thick SiO_2 by PECVD was deposited as the passivation layer. After patterning of the contact holes, the 6000 Å thick Al-Si-Cu pad was deposited by physical vapor deposition (PVD) and patterned to finish the processes of poly-Si TFTs fabrication (Fig. 2-2 (e)). All process splits are illustrated in Fig. 2-3. The poly-Si TFTs were exposed to NH_3 plasma with several conditions, including diverse stages, various plasma treatment time, and different plasma power.

2.3 Measurement and Equipment Setup

Measurement setup of the poly-Si TFTs is presented in Fig. 2-4, including semiconductor characterization system (KEITHLEY 4200), pulse pattern generator (Agilent 81110A), low leakage current switch mainframe (KEITHLEY 708A), and probe station.

KEITHLEY 4200 is equipped with programmable source-monitor units (SMU) which provides high resolution to measure DC I-V, pulse characterization and reliability testing of semiconductor devices.

Agilent 81110A with two pulse channels supplies high timing resolution pulse. When the devise is measured in probe station, KEITHLEY 708A, which is configured a 10-input × 12-output switching matrix, switching the signals from KEITHLEY 4200 and Agilent 81110A. Moreover, the C^{++} language is used for controlling the devise measurement instruments.

2.3 Extraction Methods of Device Parameters

The extraction methods of electrical parameters, including threshold voltage (V_{TH}) and transconductance (G_m), will be introduced in the following sections.

2.3.1 Threshold Voltage

In this thesis, threshold voltage (V_{TH}) is determined by constant drain current method. V_{TH} is defined as the gate voltage that yields a drain current (I_{DS}) of 100 nA , where I_{DS} = 100 nA × (W/L). W and L are channel width and channel length, respectively. This method is utilized in most of the studies of TFTs.

2.3.2 Transconductance

Transconductance (G_m) is the guide to extract the field-effect mobility (μ_{FE}). Field-effect mobility is calculated from the maximum transconductance (G_{m_max}) at low drain bias (V_{DS} = 0.1 V). The drain current in linear region ($V_{DS} < V_{GS} - V_{TH}$) can be approximated as

$$I_{DS} = \mu_{FE} C_{OX} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^{2}\right] \quad \text{(2-1)}$$

where C_{OX} is the gate oxide capacitance per unit area and V_{DS} is the drain-source voltage. The transconductance (in linear region) is defined as

$$G_{m\_max} \equiv \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{EF} C_{OX} (\frac{W}{L}) V_{DS} \quad \text{(2-2)}$$

However, KEITHLEY 4200 is automatic to extract G_{m_max} from the transfer characteristics (I_{DS}–V_{GS}). By finding out the G_{m_max}, we can calculate the field-effect mobility of all samples.

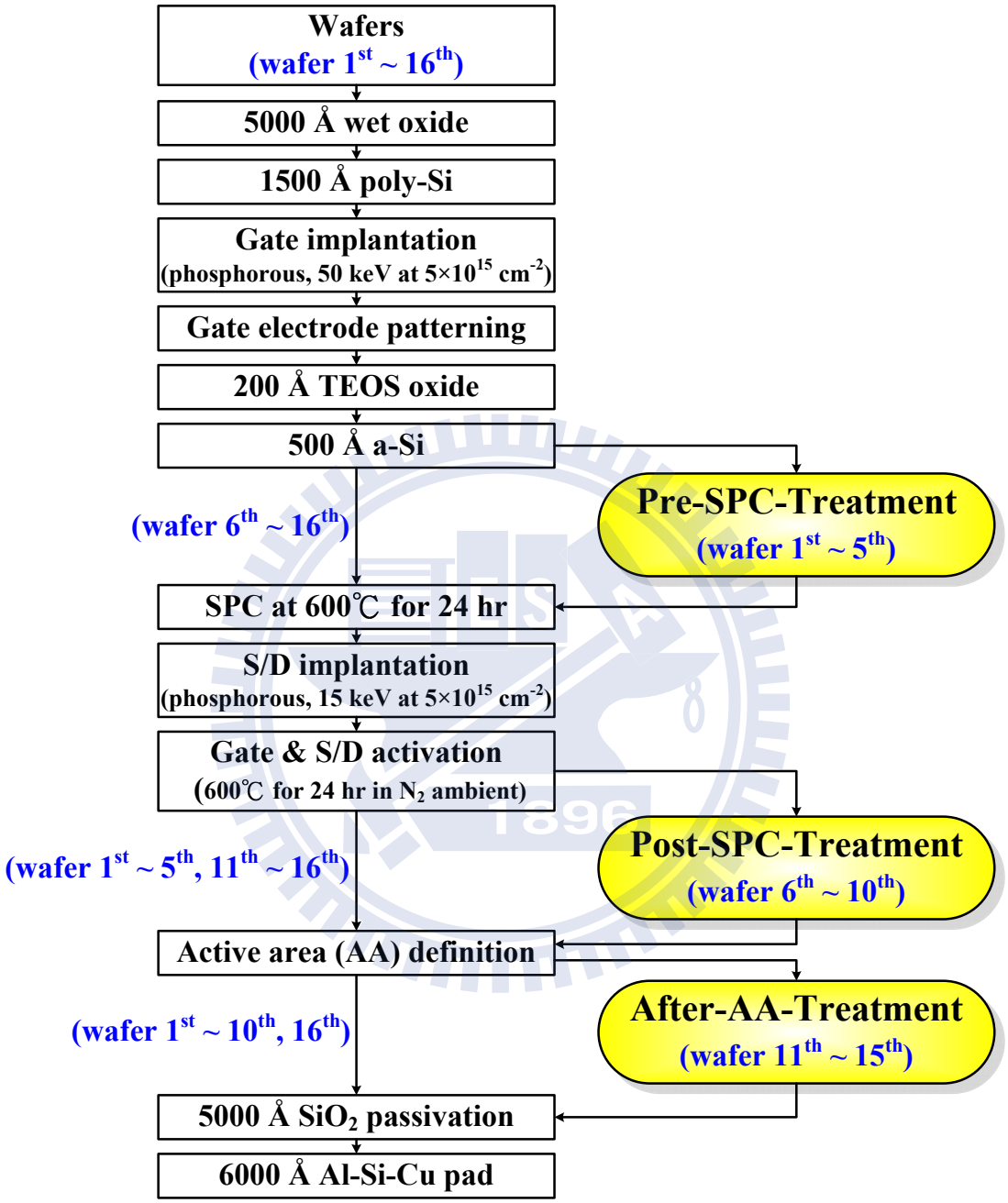
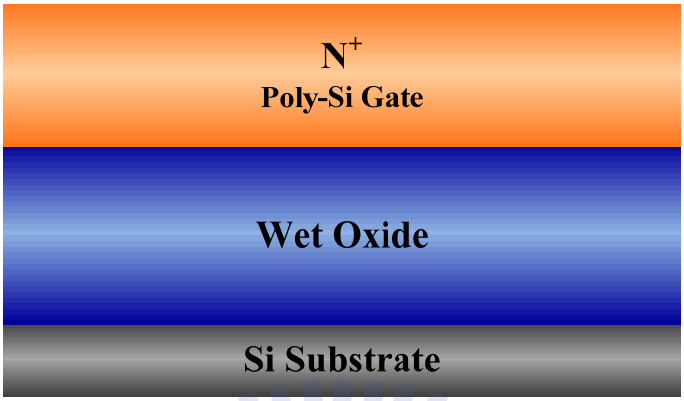
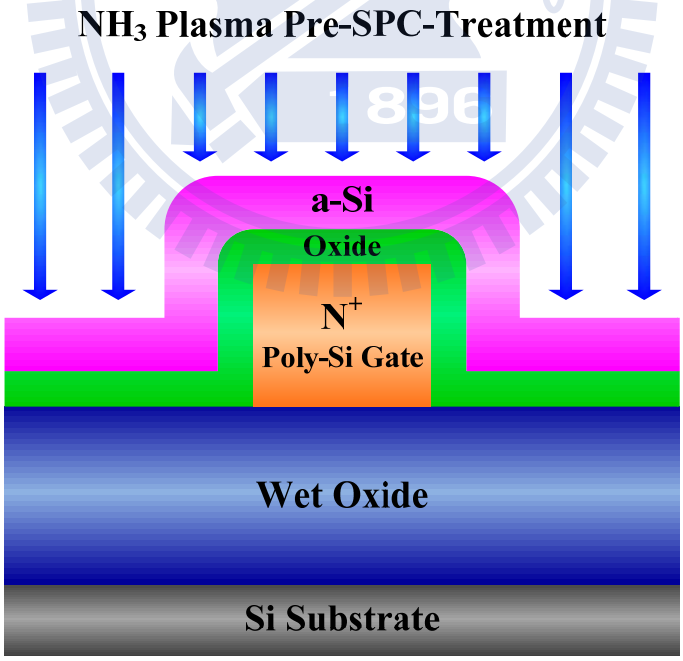


Fig. 2-1 The process flow of the poly-Si TFTs.

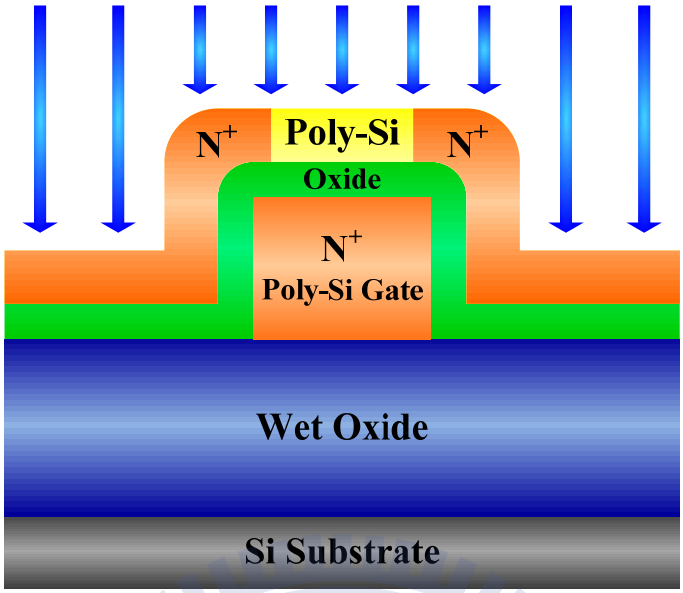


(a) The thermal oxide of 5000 Å was grown. The poly-Si film of 1500 Å was deposited and implanted with phosphorous (50 keV at 5×10^{15} cm^{-2}).



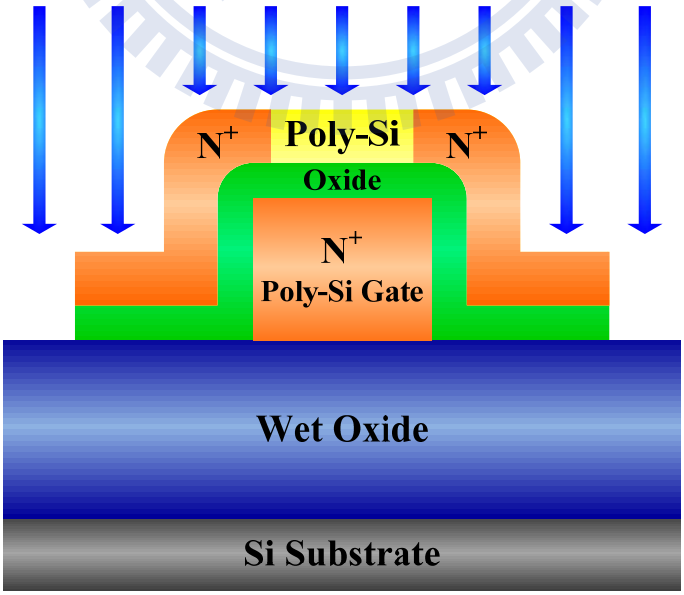
(b) After gate electrode patterning, a 200 Å thick TEOS oxide was deposited as the gate insulator. Then, the a-Si film of 500 Å was deposited. Some wafers were exposed to NH_3 plasma, which was defined as “pre-SPC-treatment”.

NH_3 Plasma Post-SPC-Treatment

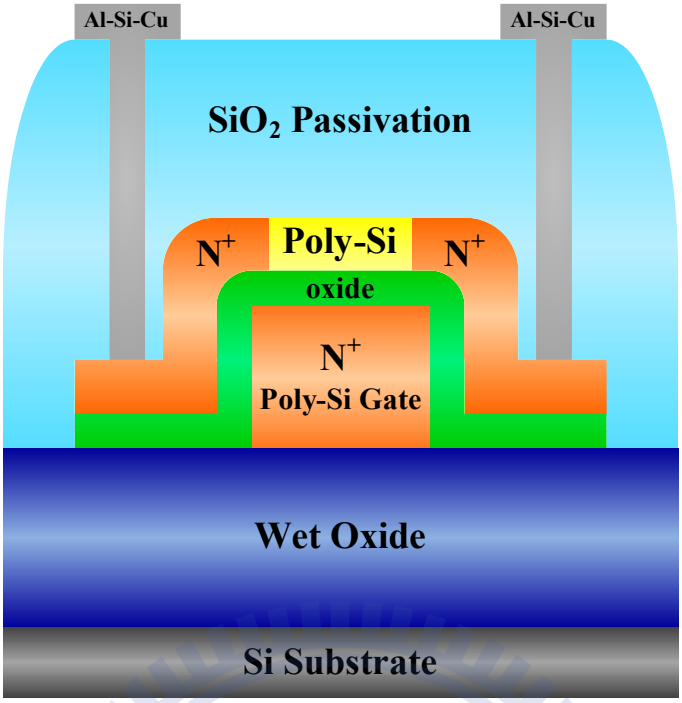


(c) SPC at 600℃ for 24 hr to transform the a-Si into poly-Si. The S/D were implanted with phosphorous (15 keV at 5×10^{15} cm^{-2}) and activated by annealing at 600℃ for 24 hr in N_2 ambient. Some wafers were exposed to NH_3 plasma, which was defined as "post-SPC-treatment".

NH_3 Plasma After-AA-Treatment



(d) After defining the active area, some wafers were exposed to NH_3 plasma, which was defined as "after-AA-treatment".



(e) The 5000 Å thick SiO_2 was deposited as the passivation layer. After patterning of the contact holes, the 6000 Å thick Al-Si-Cu pad was deposited and patterned to finish the process of poly-Si TFTs fabrication.

Fig. 2-2 Schematic of the fabrication processes for bottom gate poly-Si TFTs.

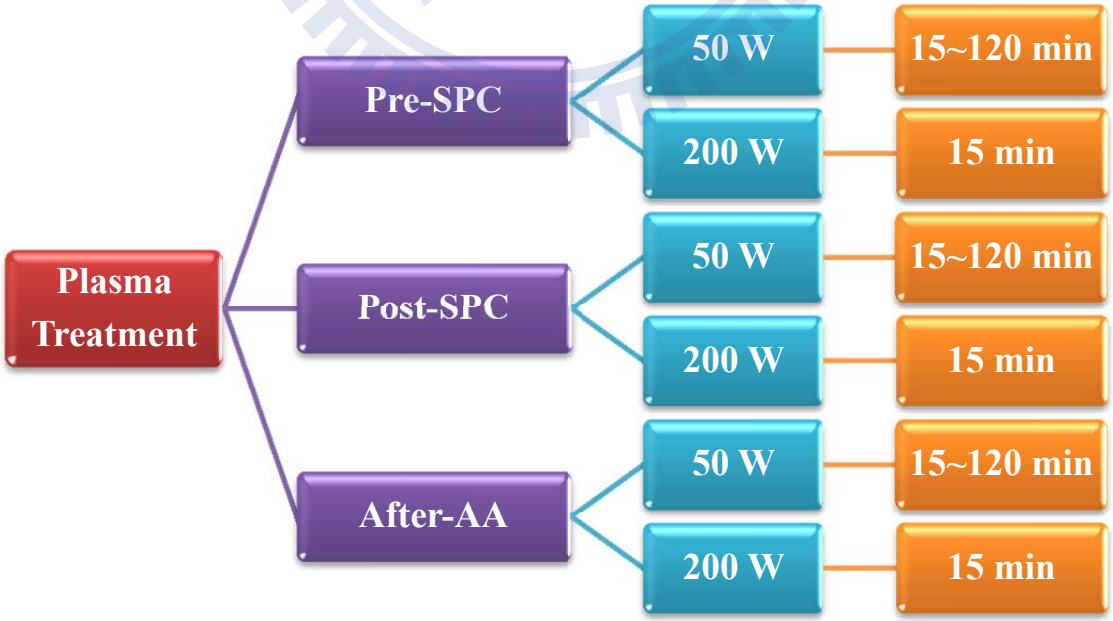


Fig. 2-3 The process splits for the poly-Si TFTs.

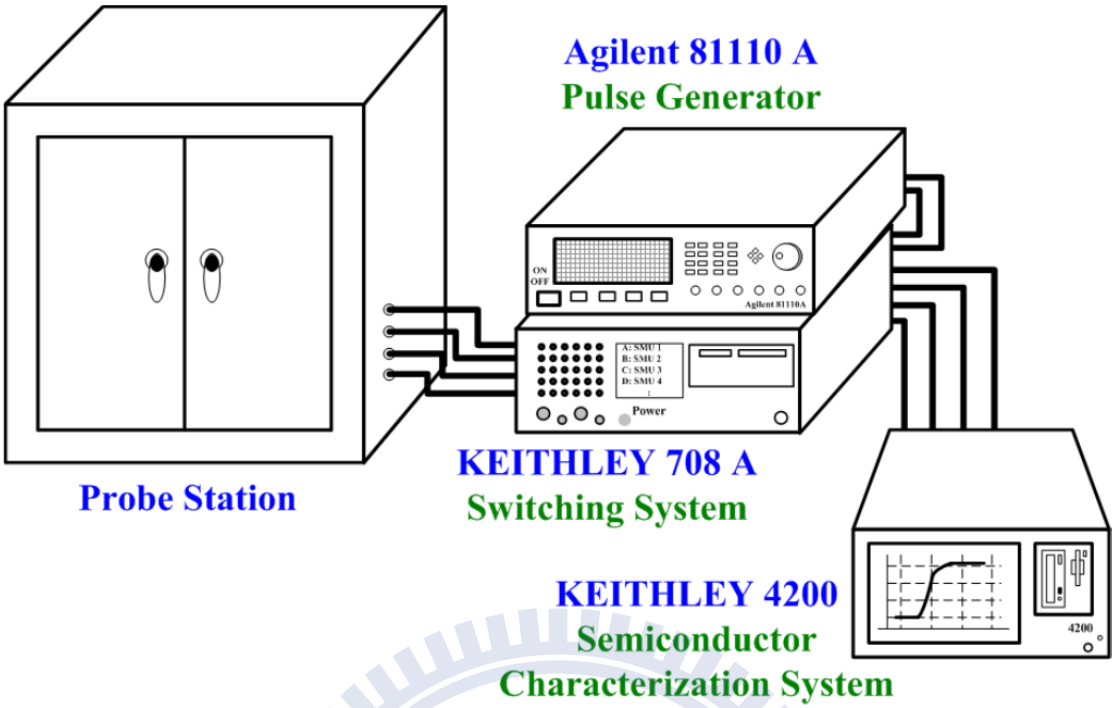


Fig. 2-4 The experimental setup of each apparatus.

Chapter 3

Effects of NH_3 Plasma Treatment on Bottom Gate Poly-Si TFTs

3.1 Introduction

NH_3 plasma treatment is an effective method to passivate defects that will improve the performance and the hot-carrier reliability of poly-Si TFTs [3.1]-[3.2]. During NH_3 plasma treatment, radicals pile-up at SiO_2/poly-Si interface and passivate the dangling bonds at grain boundaries (deep states) as well as the intra-grain traps (tail states), leading to improved performance. [3.3]. In this chapter, the passivation effect of NH_3 plasma treatment on bottom gate poly-Si TFTs will be thoroughly studied. First, the influences of different NH_3 plasma treatment time will be discussed. Second, the influences of different NH_3 plasma power will also be systematically investigated.

3.2 Plasma Treatment Time Dependence

Fig. 3-1 – Fig. 3-3 illustrate I_{DS}–V_{GS} and G_m–V_{GS} characteristics of n-channel poly-Si TFTs for control sample and the samples with NH_3 plasma pre-SPC-treatment, post-SPC-treatment, and after-AA-treatment at V_{DS} of 0.1 V, respectively. These poly-Si TFTs were exposed to NH_3 plasma with power of 50 W, and the plasma treatment time varied from 15 min to 120 min. The subthreshold double-hump phenomenon has been measured in these poly-Si TFTs. The subthreshold double-hump phenomenon indicates that there are two conduction paths for the device [3.4]. During plasma dry etching processing, especially in active area patterning, high energy photons may cause various types of damage, such as a shift in the threshold

voltage and the formation of crystalline defects [3.5]-[3.8]. It has been reported that plasma-induced charging stress produces the generation of hole traps and interface states in the gate oxide. The generation of hole traps will lead to negative V_{TH} shift [3.9]-[3.10]. The top-view of bottom gate poly-Si TFTs with different channel width are shown in Fig. 3-4 (a) and (b). For the poly-Si TFT in the width direction, the equivalent channel width can be divided into the flat plate and corner edge portions. During active area patterning, plasma may cause damage on the sidewall of the oxide, and the plasma-induced charging will generate new hole traps at the corner edge portions. These hole traps in the gate oxide lead to negative V_{TH} shift at the corner edge portions, and the corner edge portions will have lower V_{TH} than the flat plate portion. As shown in Fig. 3-5, this transistor can be equivalent to flat plate transistor and corner edge transistor in parallel. At low V_{GS} region, corner edge transistor which has low V_{TH} will be turned on first, then the flat plate transistor which has high V_{TH} will be turned on as V_{GS} is further increased [3.11]. Moreover, the non-uniform V_{TH} exhibits the early turn-on phenomena.

Once the channel width decreases from 10 μm to 2 μm, the corner edge portions will gradually dominate the device characteristics as shown in Fig. 3-4 (b). The I_{DS}–V_{GS} characteristics for the samples with 2 μm channel width are shown in Fig. 3-6 and Fig. 3-7. The poly-Si TFTs with 2 μm channel width have large off-state leakage current (I_{OFF}) due to the impacts of the corner edge portions. The hole traps generated by plasma dry etching at the corner edge portions construct a leakage path and lead to a large I_{OFF}. In addition, for the poly-Si TFTs with NH_3 plasma after-AA-treatment as shown in Fig. 3-7, the I_{OFF} become smaller with longer NH_3 plasma treatment time. We hypothesize NH_3 plasma after-AA-treatment may eliminate some of the hole traps generated by active area patterning, and after-AA-treatment may decrease the I_{OFF}.

Threshold voltage (V_{TH}), and maximum transconductance (G_{m_max}) as a function

of plasma treatment time are shown in Fig. 3-8 – Fig. 3-9. V_{TH} is defined as the gate voltage that yields a drain current (I_{DS}) of 100 nA , where I_{DS} = 100 nA × (W/L). As shown in Fig. 3-8, the poly-Si TFTs with NH_3 plasma pre-SPC-treatment have the largest V_{TH} and the lowest G_{m_max}. Besides, the poly-Si TFTs with NH_3 plasma pre-SPC-treatment have even larger V_{TH} and lower G_{m_max} than control sample without any NH_3 plasma treatment. It has been revealed that although NH_3 plasma pre-SPC-treatment before SPC annealing significantly shortens the a-Si film crystallization time, the average grain size of the device with NH_3 plasma pre-SPC-treatment is smaller than that of the device without any plasma treatment [3.3]. In general, the smaller grain size usually leads to the worse device performance because of the larger amount of grain boundaries defects. Furthermore, even though some nitrogen and hydrogen radicals terminate the dangling bonds at the grain boundaries during plasma pre-SPC-treatment processing, the following SPC annealing at high temperature (600℃) will lead to the out-diffusion of nitrogen and hydrogen radicals. The passivation effect breaks since the nitrogen and hydrogen radicals release from the defect sites [3.1]. Hence, due to 1) the smaller grain size of the device with NH_3 plasma pre-SPC-treatment, and 2) the out-diffusion of nitrogen and hydrogen radicals during high temperature SPC annealing, the poly-Si TFTs with NH_3 plasma pre-SPC-treatment will have worse performance than control sample without any NH_3 plasma treatment.

Moreover, the poly-Si TFTs with post-SPC-treatment or after-AA-treatment have substantial improvements of performance compared with control sample. The poly-Si TFTs have the smallest V_{TH} with NH_3 plasma after-AA-treatment. In addition, the poly-Si TFTs with NH_3 plasma after-AA-treatment have higher G_{m_max} than those with post-SPC-treatment ones for plasma treatment time ≤ 30 min. I. W. Wu et al. demonstrated that the deep states, which originate from the dangling bonds at grain

boundaries, degrade the threshold voltage and the subthreshold swing. The tail states, which originate from the strain-bond-related intra-grain defects, degrade the field-effect mobility and minimum leakage current [3.12]. According to the literature, we presume the improvements, including smaller V_{TH} and higher G_{m_max} of the poly-Si TFTs come from the passivation effect by after-AA-treatment. Moreover, it has been revealed that gate oxide is the major diffusion path for plasma radicals, because radicals diffuse rapidly in SiO_2. In contrast to SiO_2, for the poly-Si thin film, Si dangling bonds in the gain boundaries act as traps rather than as paths of enhanced diffusion [3.13]. Even though the cross-sectional area of the SiO_2 is small, radicals are directly guided along the SiO_2 to the SiO_2/poly-Si interface. By diffusing laterally within the SiO_2, radicals effectively passivate the traps in the middle of the channel. Therefore, after-AA-treatment passivates channel traps not only by radicals diffusing vertically through the poly-Si channel, but also by radicals diffusing laterally through the gate oxide as shown in Fig. 3-10. Because After-AA-treatment additionally passivates traps by radicals diffusing laterally through the gate oxide, it has higher passivation efficiency than post-SPC-treatment. As a result, NH_3 plasma after-AA-treatment is indeed a technique to effectively passivate the dangling bonds at grain boundaries (deep states) as well as the intra-grain traps (tail states).

For plasma treatment time > 30 min, the poly-Si TFTs with NH_3 after-AA-treatment have smaller V_{TH} but lower G_{m_max} compared with the samples with post-SPC-treatment. The degraded G_{m_max} may be attributed to the following mechanisms. Although after-AA-treatment passivates traps much more efficiently than post-SPC-treatment, the poly-Si TFTs with NH_3 plasma after-AA-treatment suffer from heavier ion bombardment damage. During plasma treatment processing, bombardment by energetic ions may cause breakage of chemical bonds and damage the poly-Si channel [3.8]. Furthermore, ion bombardment may also lead to the

generation of interface traps, degrade carrier transport and decrease the G_{m_max}. Due to the extra damage on the sidewall of the channel as shown in Fig. 3-11, after-AA-treatment results in heavier damage than post-SPC-treatment. Therefore, for plasma treatment time > 30 min, ion bombardment damage becomes the non-negligible mechanism for performance degradation for the samples with after-AA-treatment. For these reasons, the poly-Si TFTs with after-AA-treatment have lower G_{m_max} than those with post-SPC-treatment ones for plasma treatment time > 30 min. Since the poly-Si TFTs with NH_3 plasma pre-SPC-treatment have even worse performance than control sample without any NH_3 plasma treatment, we do not take results of the poly-Si TFTs with pre-SPC-treatment into account in the following discussions.

Fig. 3-12 and Fig. 3-13 illustrate I_{DS}–V_{DS} characteristics of n-channel poly-Si TFTs for control sample and the samples with NH_3 plasma post-SPC-treatment, and after-AA-treatment, respectively. At low V_{DS} region, both of the poly-Si TFTs with post-SPC-treatment and after-AA-treatment exhibit better performance than control sample. As V_{DS} is further increased, the kink effect has been measured in these poly-Si TFTs, and the kink effect is more significant for control sample than the samples with NH_3 plasma post-SPC-treatment or after-AA-treatment. The slopes of I_{DS}–V_{DS} characteristics for V_{DS} from 3 V to 6 V are shown in Fig. 3-14 and Fig. 3-15. The steeper slope indicates the kink effect more obviously. According to these results, the longer NH_3 plasma treatment time can alleviate kink effect more effectively. Hence, we hypothesize that kink effect can be suppressed by NH_3 plasma treatment because of the reduction of traps. There are several explanations for kink effect, which is related to traps, have been reported. M. Hack et al. claimed that it is the presence of grain boundaries or traps in the poly-Si that causes kink effect to be much more significant than in comparable single-crystal silicon counterparts [3.14]. A. K. K.

P. et al. demonstrated that due to grain boundaries, the local electric field near the irregular surface might be appreciably greater than the average electric field, which might initiate additional impact ionization [3.15]. Besides, B. Kim et al. indicated that the kink effect exists at the non-treated poly-Si TFTs do not appear at the surface-treated ones because the kink effect has been known to depend on the nature of surface states [3.16]. Thus, the reduction of traps by NH_3 plasma treatment is a reasonable explanation for the suppression of the kink effect.

During processing of plasma, such as thin film deposition, plasma etching and plasma treatment, gate oxides are also subjected to plasma-induced damage. Due to the electron, ion and particle bombardment, the gate oxide may be weakened by plasma related processes [3.17]. On the contrary, H. C. Cheng et al. claimed that after NH_3 plasma treatment, the oxide quality is improved because the nitrogen and hydrogen radicals in the oxide may strengthen the strained bonds and passivate the trap-states [3.2]. Nevertheless, the samples of the above-mentioned literatures were top gate structure, not bottom gate structure. In order to clarify the influences on bulk oxide quality for bottom gate poly-Si TFTs by NH_3 plasma treatment, Fig. 3-16 and Fig. 3-17 show gate-leakage current characteristics of poly-Si TFTs. All samples with different plasma treatment time exhibit comparable gate-leakage current characteristics, which indicate the bulk oxide quality for bottom gate poly-Si TFTs are insensitive to NH_3 plasma treatment with plasma power of 50 W.

3.3 Plasma Power Dependence

Fig. 3-18 – Fig. 3-20 illustrate I_{DS}–V_{GS} and G_m–V_{GS} characteristics of n-channel poly-Si TFTs for control sample and the samples with NH_3 plasma pre-SPC-treatment, post-SPC-treatment, and after-AA-treatment at V_{DS} of 0.1 V, respectively. These poly-Si TFTs were exposed to NH_3 plasma with power of 50 W or 200 W, and the

plasma treatment time was 15 min. Threshold voltage (V_{TH}) and maximum transconductance (G_{m_max}) as a function of plasma power are shown in Fig. 3-21 and Fig. 3-22. Compared with plasma power of 50 W, the poly-Si TFTs with plasma power of 200 W have lower V_{TH} and higher G_{m_max}. The higher the plasma power, the better the performance of these poly-Si TFTs. Because nitrogen and hydrogen radicals have higher kinetic energy with plasma power of 200 W than those with 50 W ones, they reach poly-Si/SiO_2 interface more easily. Consequently, plasma treatment with higher power passivates traps more efficiently compared with the lower one. Moreover, the poly-Si TFTs with NH_3 plasma pre-SPC-treatment for both power of 50 W and 200 W have even worse performance than control sample. For plasma power of 50 W, due to higher passivation efficiency of after-AA-treatment, the poly-Si TFT with NH_3 plasma after-AA-treatment has smaller V_{TH} and higher G_{m_max} than that with post-SPC-treatment one. However, for plasma power of 200 W, the performance of the poly-Si TFTs are exactly the opposite to plasma power of 50 W ones. For plasma power of 200 W, although after-AA-treatment passivates traps much more efficiently than post-SPC-treatment, the poly-Si TFT with NH_3 plasma after-AA-treatment suffers from heavier ion bombardment damage. Furthermore, ion bombardment damage becomes the non-negligible mechanism for the sample with NH_3 plasma after-AA-treatment with plasma power of 200 W. Thus, for plasma power of 200 W, the poly-Si TFT with NH_3 plasma after-AA-treatment has worse performance than that with post-SPC-treatment one.

Fig. 3-23 and Fig. 3-24 illustrate I_{DS}–V_{DS} characteristics of n-channel poly-Si TFTs for control sample and the samples with NH_3 plasma post-SPC-treatment, and after-AA-treatment, respectively. Both of the poly-Si TFTs with post-SPC-treatment and after-AA-treatment exhibit better performance than control sample at low V_{DS} region. And the poly-Si TFTs with plasma power of 200 W have better performance

than those with 50 W ones. The kink effect has been measured in these poly-Si TFTs as V_{DS} is further increased. The slopes of I_{DS}–V_{DS} characteristics for V_{DS} from 3 V to 6 V are shown in Fig. 3-25 and Fig. 3-26. The steeper slope indicates the kink effect more obviously. According to these results, the higher NH_3 plasma power can alleviate kink effect more effectively. The suppression of the kink effect is more efficient for the samples with plasma power of 200 W than those with 50 W ones because of the reduction of traps.

Fig. 3-27 and Fig. 3-28 show the gate-leakage current characteristics of n-channel poly-Si TFTs for control sample and the samples with NH_3 plasma post-SPC-treatment, and after-AA-treatment, respectively. The poly-Si TFTs with plasma power of 200 W have lower gate-leakage compared with those with plasma of 50 W ones. Because radicals have higher kinetic energy with plasma power of 200 W than those with 50 W ones, they reach SiO_2 and passivate traps more easily. In consequence, better bulk oxide quality for bottom gate poly-Si TFTs can be obtained by NH_3 plasma treatment with higher plasma power. In other words, NH_3 plasma treatment with plasma power of 200 W is a method to improve bulk oxide quality more effectively than the plasma treatment with power of 50 W.

3.4 Summary

In this chapter, the passivation effect of NH_3 plasma treatment for bottom gate poly-Si TFTs is thoroughly studied. In section 3.2, the influences of different NH_3 plasma treatment time are discussed. Compared with the control sample without any plasma treatment, pre-SPC-treatment degrades device performance; however, post-SPC-treatment and after-AA-treatment improve device performance. The poly-Si TFTs with NH_3 plasma pre-SPC-treatment have even worse performance than control sample owing to the smaller grain size and the out-diffusion of radicals during high

temperature SPC annealing. On the other hand, the poly-Si TFTs with after-AA-treatment ones exhibit the best performance than the counterparts. After-AA-treatment is the most efficient technique to passivate traps since after-AA-treatment additionally passivates traps by radicals diffusing laterally through the gate oxide. Unfortunately, the poly-Si TFTs with after-AA-treatment suffer from the heaviest ion bombardment damage than those with post-SPC-treatment ones. Thus, for plasma treatment time > 30 min, the samples with after-AA-treatment have lower G_{m_max} compared with the samples with post-SPC-treatment. In addition, longer plasma treatment time enhance performance and alleviate kink effect more effectively. And the bulk oxide quality is insensitive to the plasma with power of 50 W, because all samples with different plasma treatment time exhibit comparable gate-leakage current.

In section 3.3, the influences of different NH_3 plasma power are systematically investigated. The higher the plasma power, the better the performance of these poly-Si TFTs. Higher plasma power enhance performance and alleviate kink effect more effectively. Because nitrogen and hydrogen radicals have higher kinetic energy with plasma power of 200 W than those with 50 W ones, they reach poly-Si/SiO_2 interface more easily. However, plasma treatment with power of 200 W results in heavier ion bombardment damage than 50 W one. Thus, for plasma power of 200 W, the sample with after-AA-treatment has lower G_{m_max} than the sample with post-SPC-treatment. Moreover, the bulk oxide quality for the sample with plasma power of 200 W is better than the sample with 50 W based on the gate-leakage comparison.

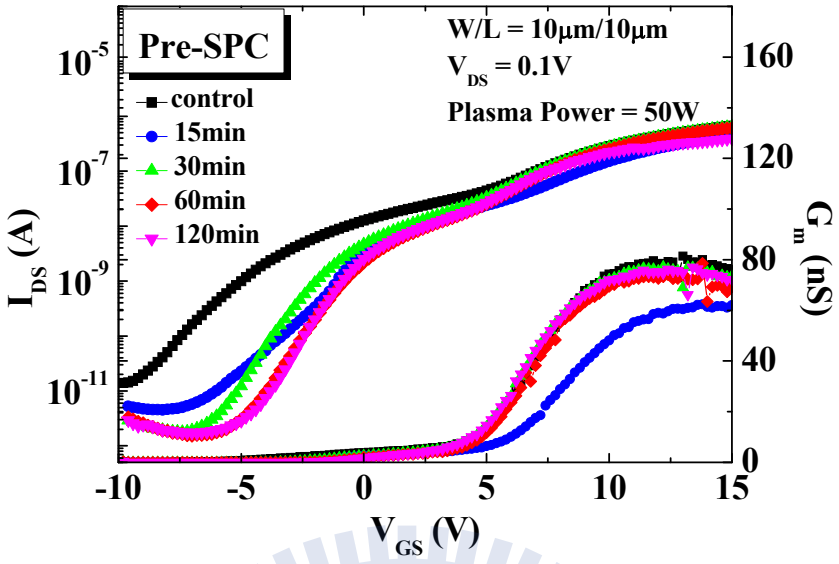


Fig. 3-1 I_{DS}–V_{GS} and G_m–V_{GS} characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma pre-SPC-treatment (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

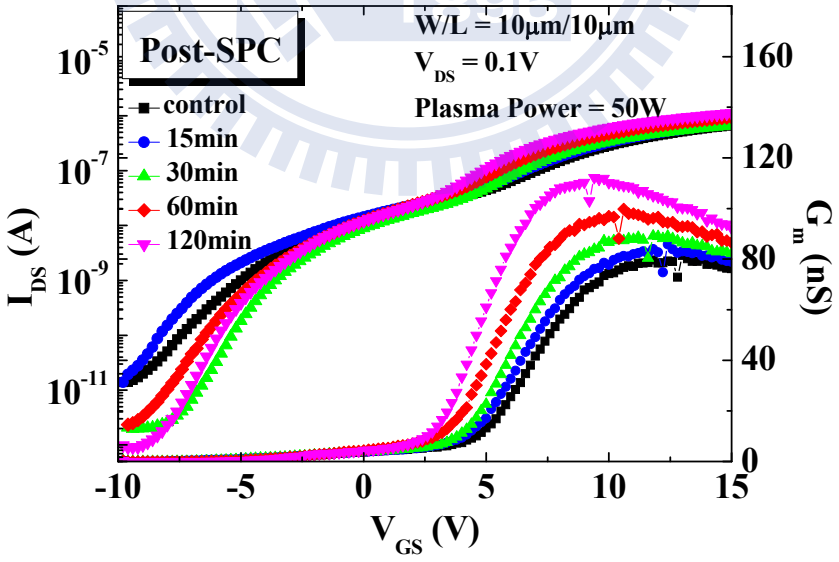


Fig. 3-2 I_{DS}–V_{GS} and G_m–V_{GS} characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma post-SPC-treatment (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

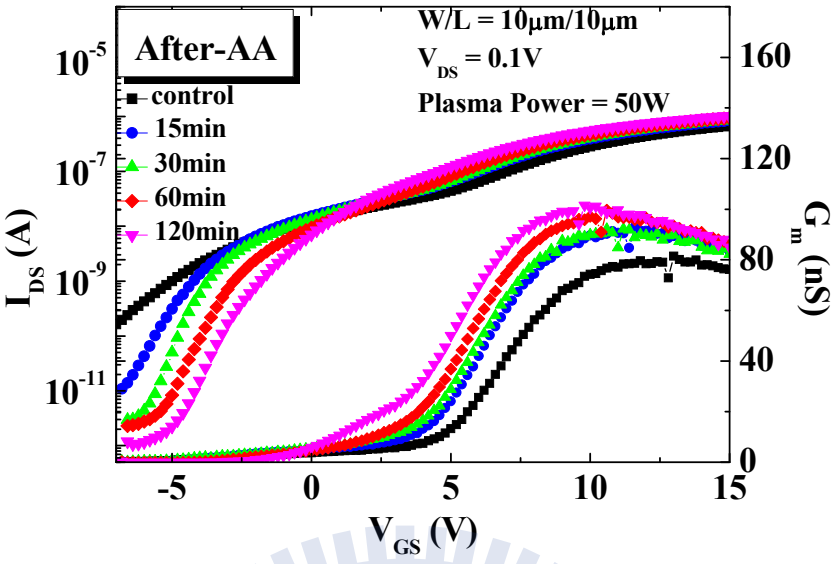
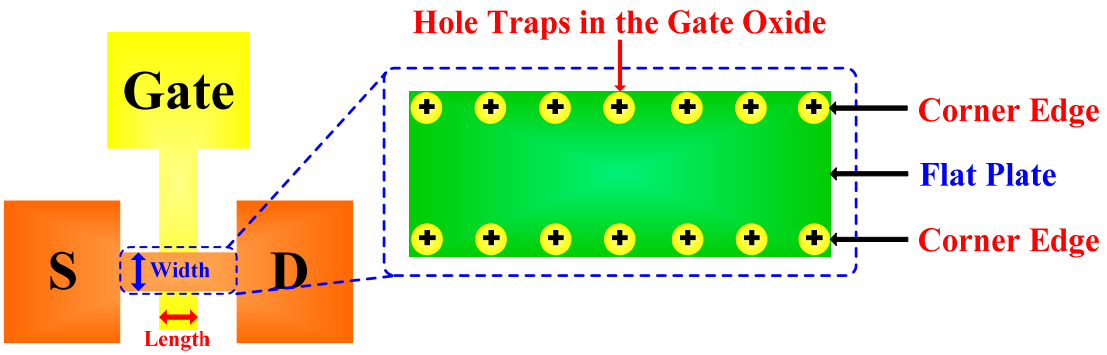
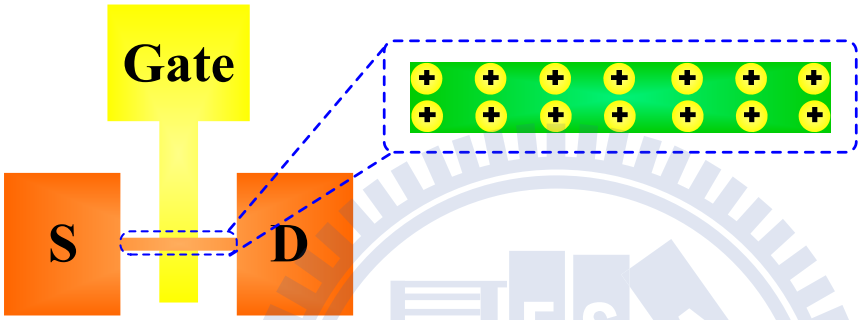


Fig. 3-3 I_{DS}–V_{GS} and G_m–V_{GS} characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma after-AA-treatment (plasma power = 50 W, plasma treatment time = 15 min to 120 min).



(a)



(b)

Fig. 3-4 Top-view of bottom gate poly-Si TFTs with plasma-induced hole traps in the gate oxide at the corner edge portions with (a) wide channel width and (b) narrow channel width.

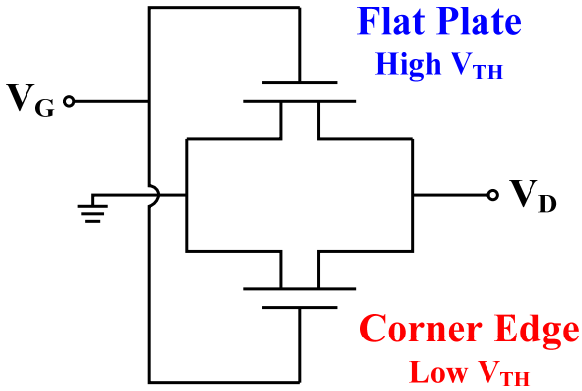


Fig. 3-5 The transistor can be equivalent to flat plate transistor and corner edge transistor in parallel.

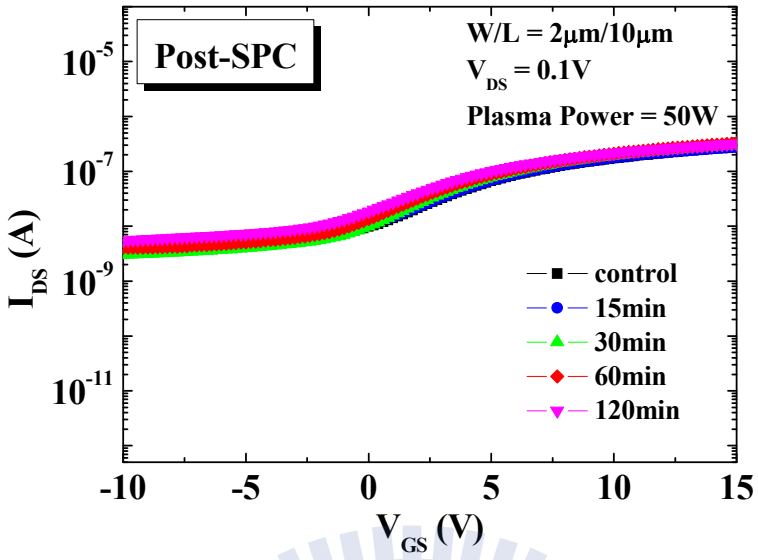


Fig. 3-6 I_{DS}–V_{GS} characteristics of poly-Si TFTs for the samples with 2 μm channel width with NH_3 plasma post-SPC-treatment (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

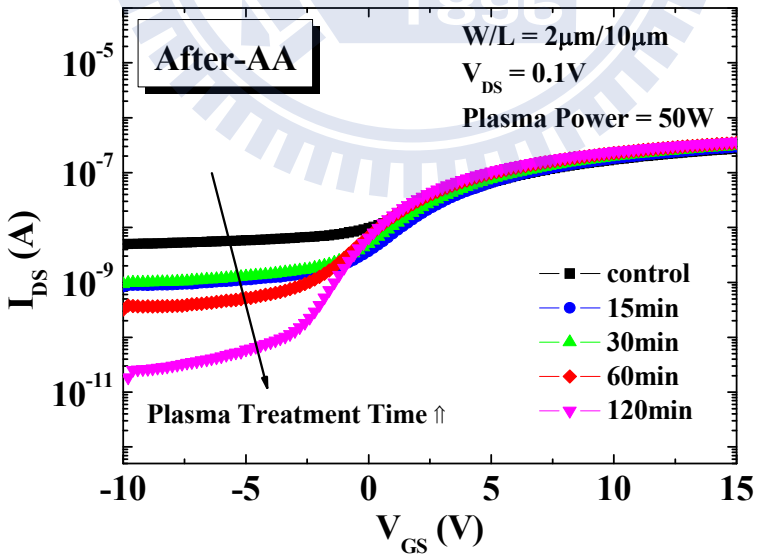


Fig. 3-7 I_{DS}–V_{GS} characteristics of poly-Si TFTs for the samples with 2 μm channel width with NH_3 plasma after-AA-treatment (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

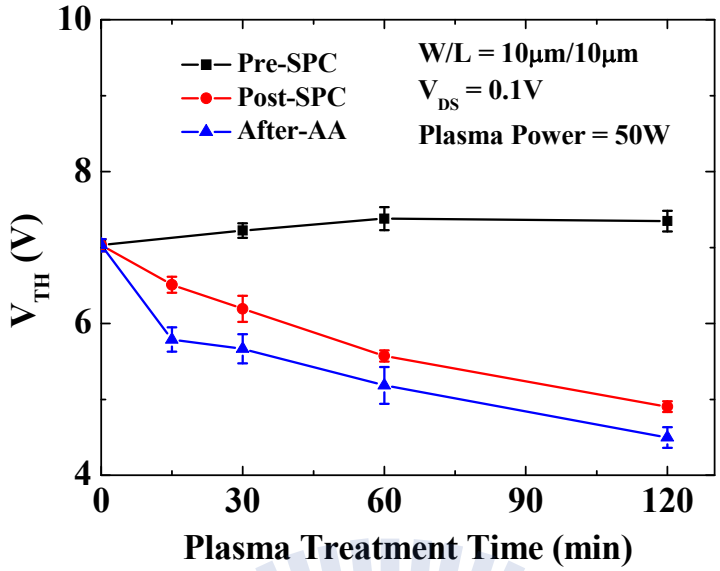


Fig. 3-8 Threshold voltage (V_{TH}) as a function of plasma treatment time.

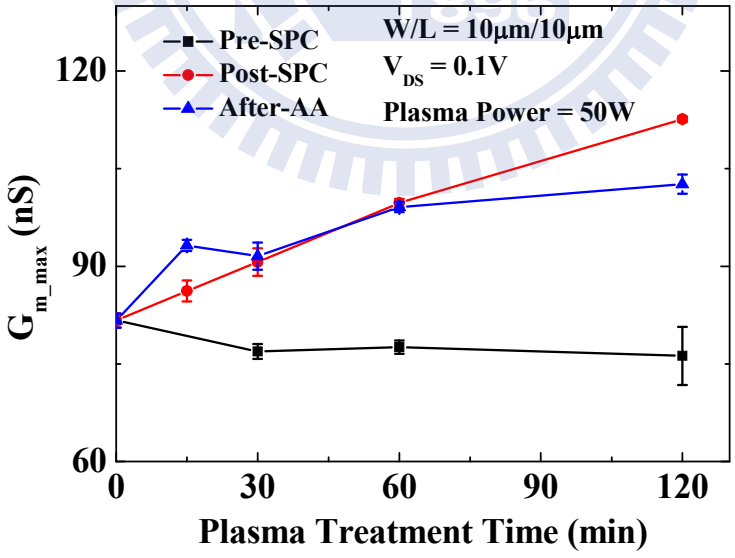


Fig. 3-9 Maximum transconductance (G_{m_max}) as a function of plasma treatment time.

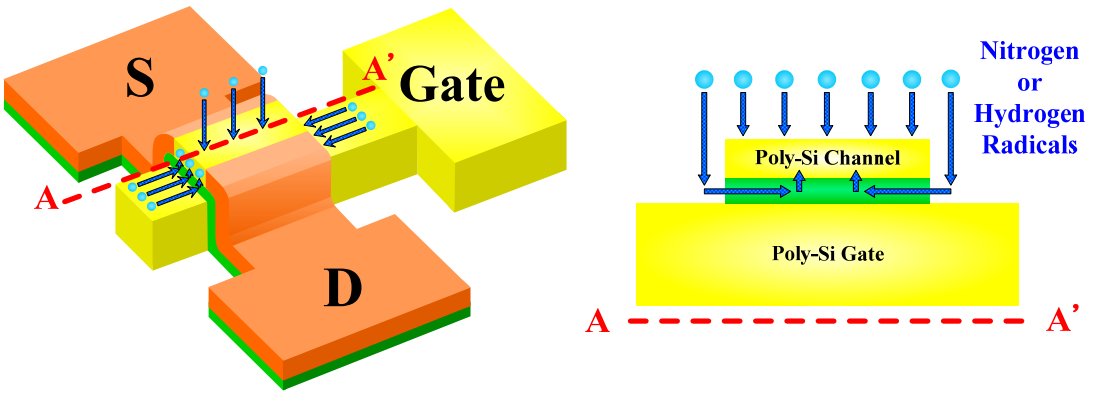


Fig. 3-10 NH_3 plasma after-AA-treatment passivates channel traps not only by radicals diffusing vertically through the poly-Si channel, but also by radicals diffusing laterally through the gate oxide.

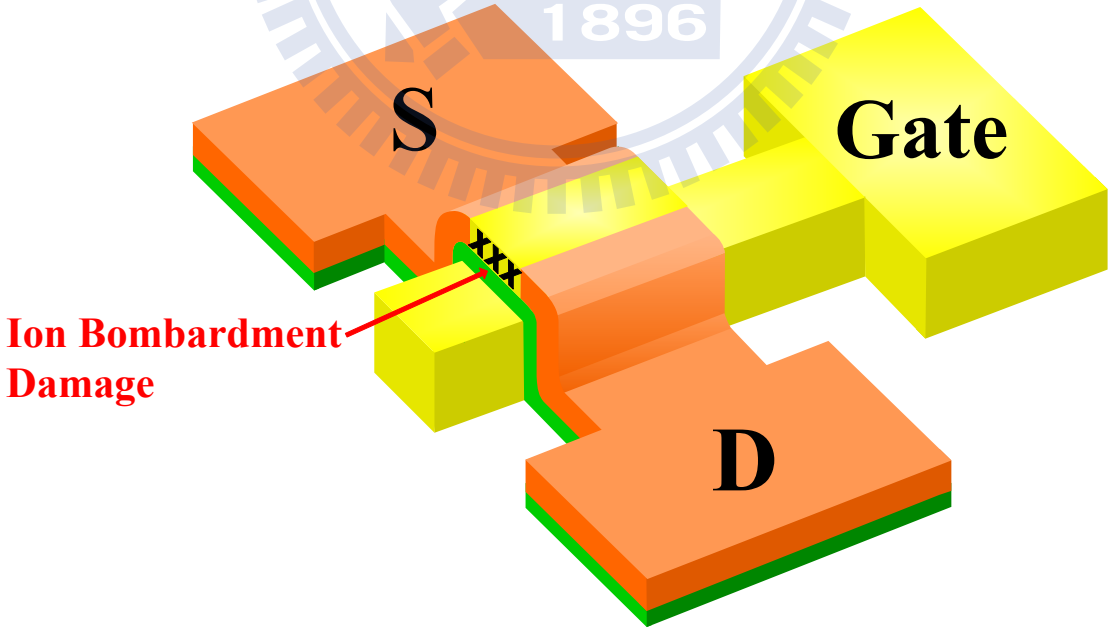


Fig. 3-11 The extra damage on the sidewall of the channel for the poly-Si TFTs with NH_3 plasma after-AA-treatment.

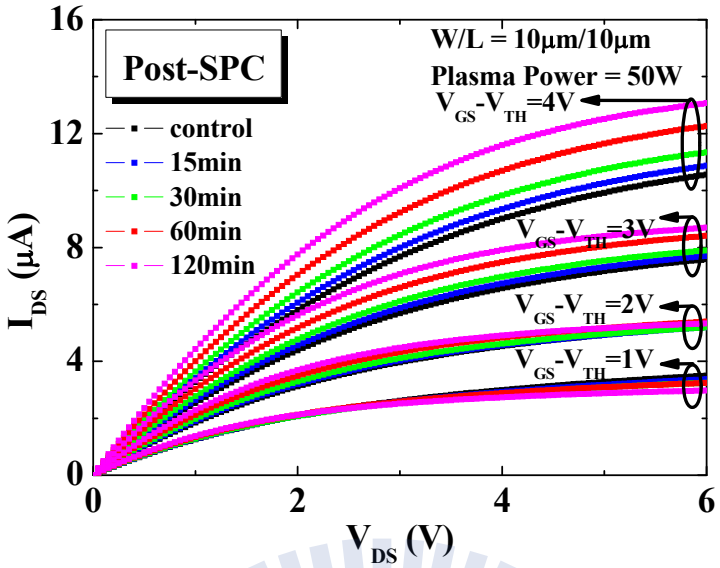


Fig. 3-12 I_{DS}–V_{DS} characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma post-SPC-treatment (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

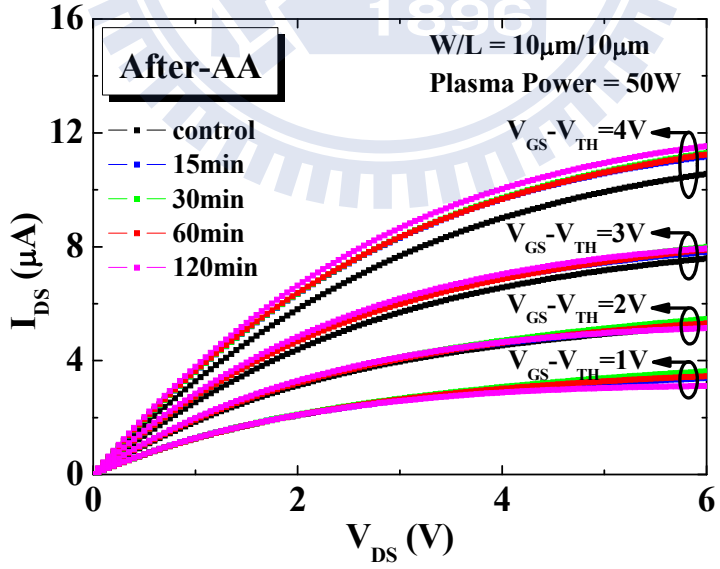


Fig. 3-13 I_{DS}–V_{DS} characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma after-AA-treatment (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

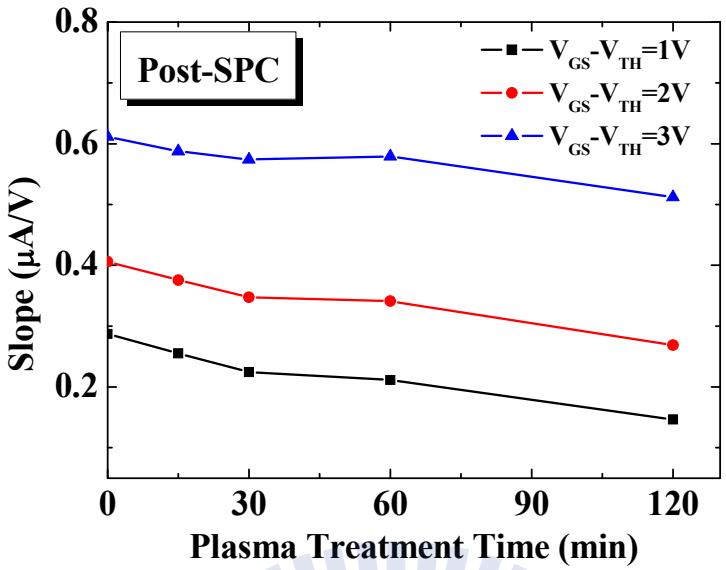


Fig. 3-14 Slopes of I_{DS}–V_{DS} characteristics (post-SPC-treatment) as a function of plasma treatment time (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

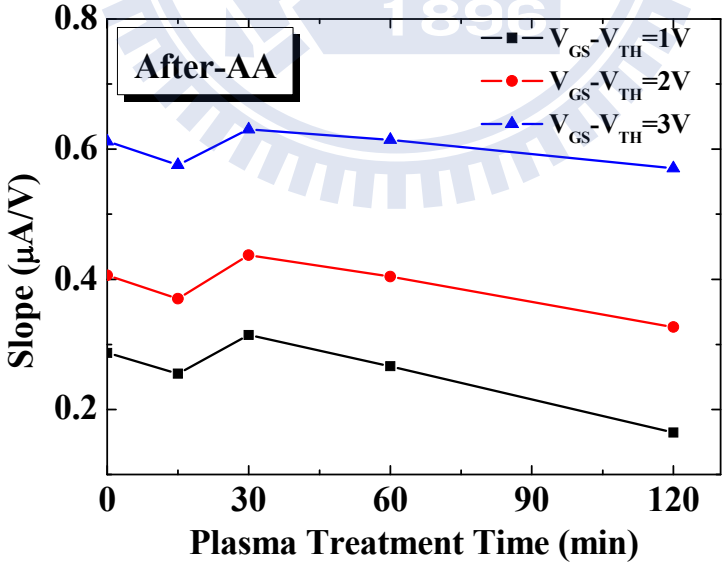


Fig. 3-15 Slopes of I_{DS}–V_{DS} characteristics (after-AA-treatment) as a function of plasma treatment time (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

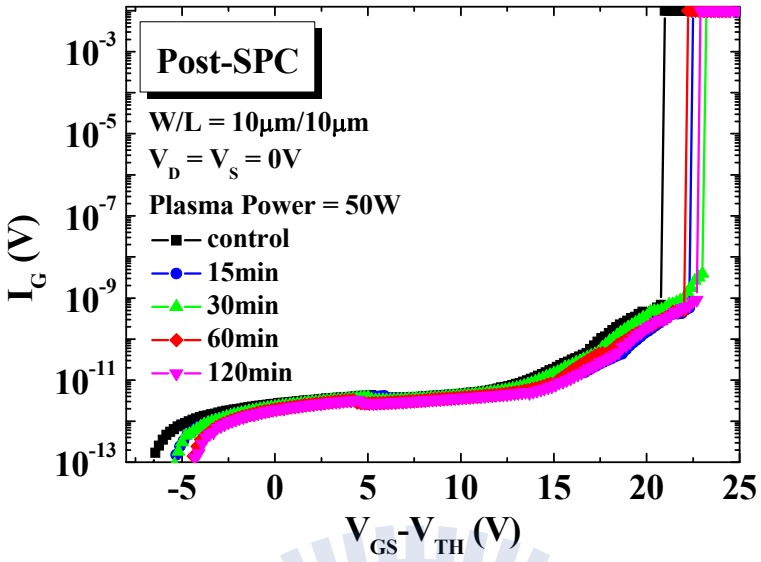


Fig. 3-16 Gate-leakage current characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma post-SPC-treatment (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

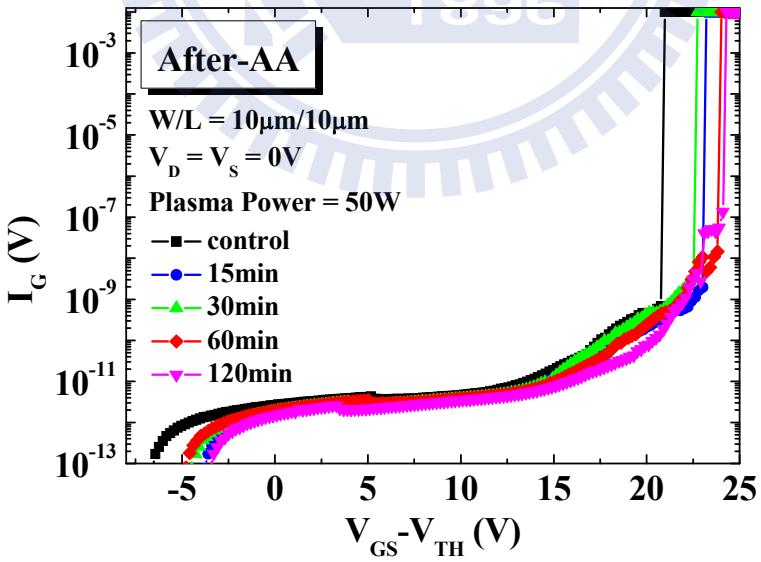


Fig. 3-17 Gate-leakage current characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma after-AA-treatment (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

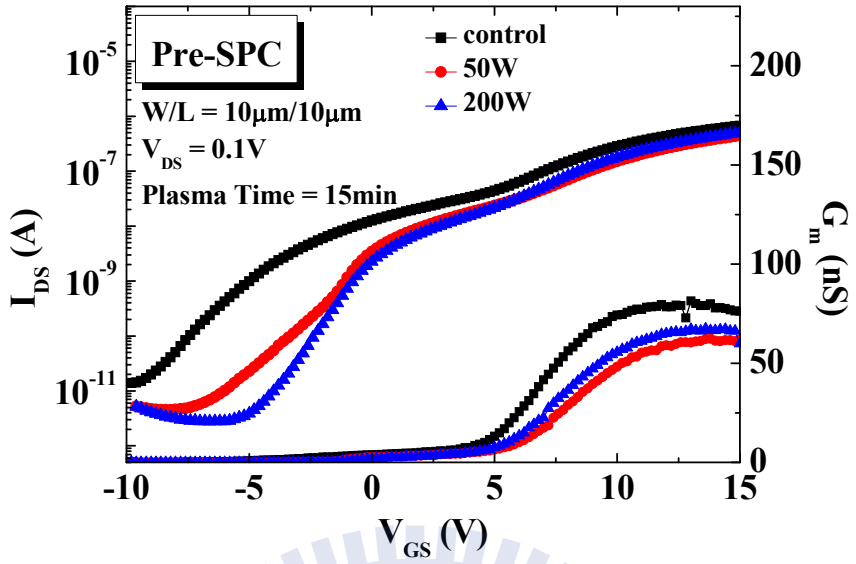


Fig. 3-18 I_{DS}–V_{GS} and G_m–V_{GS} characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma pre-SPC-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

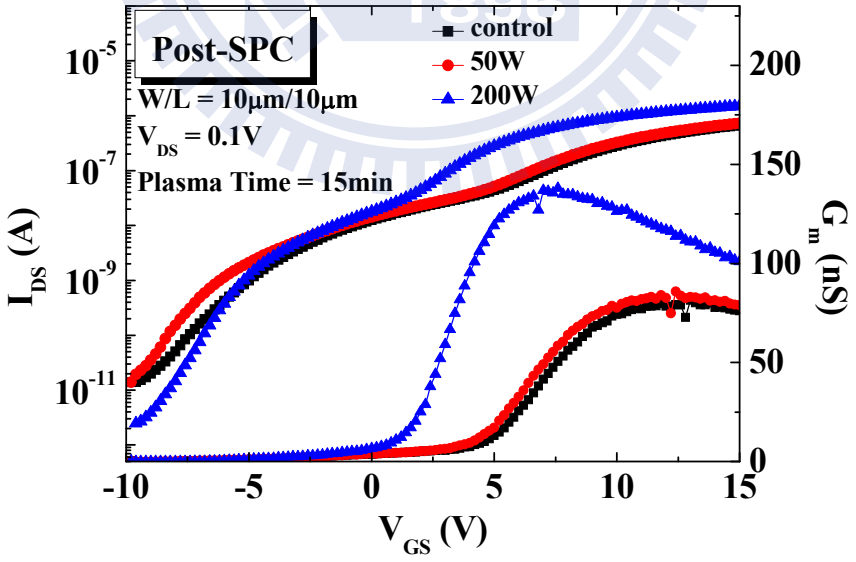


Fig. 3-19 I_{DS}–V_{GS} and G_m–V_{GS} characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma post-SPC-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

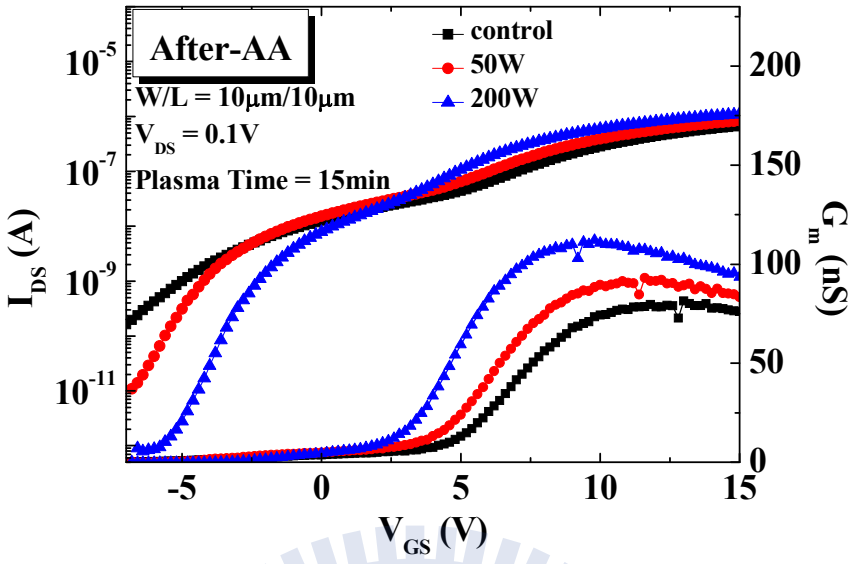


Fig. 3-20 I_{DS}–V_{GS} and G_m–V_{GS} characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma after-AA-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

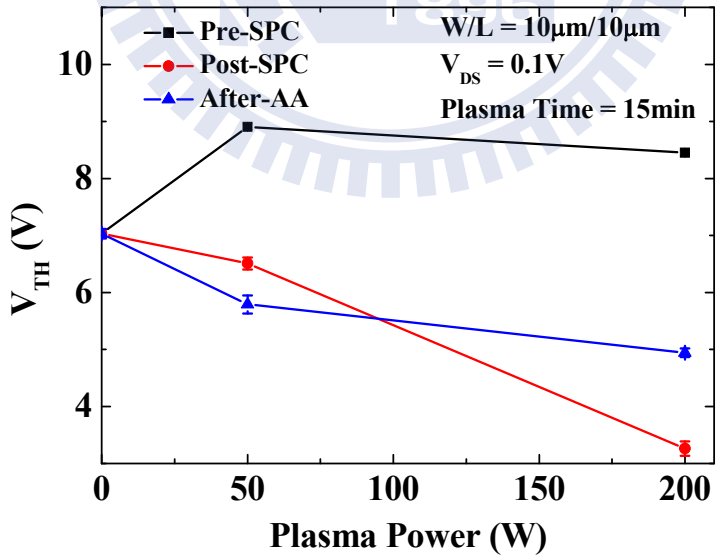


Fig. 3-21 Threshold voltage (V_{TH}) as a function of plasma power.

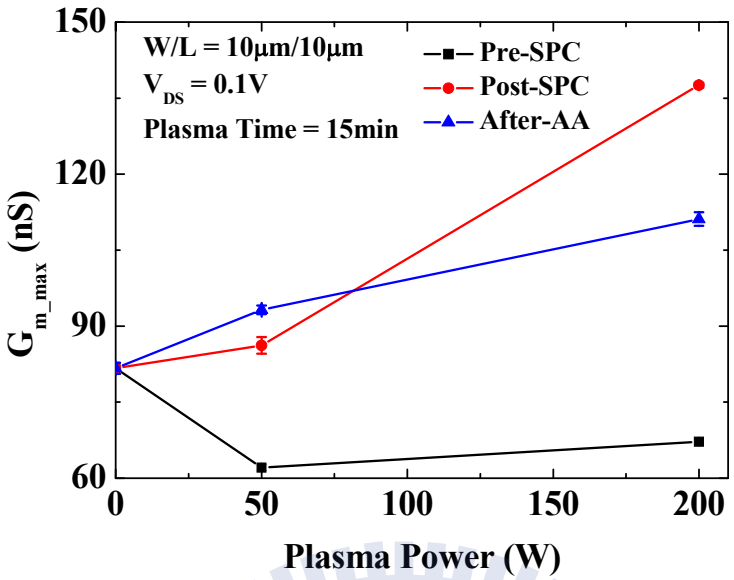


Fig. 3-22 Maximum transconductance (G_{m_max}) as a function of plasma power.

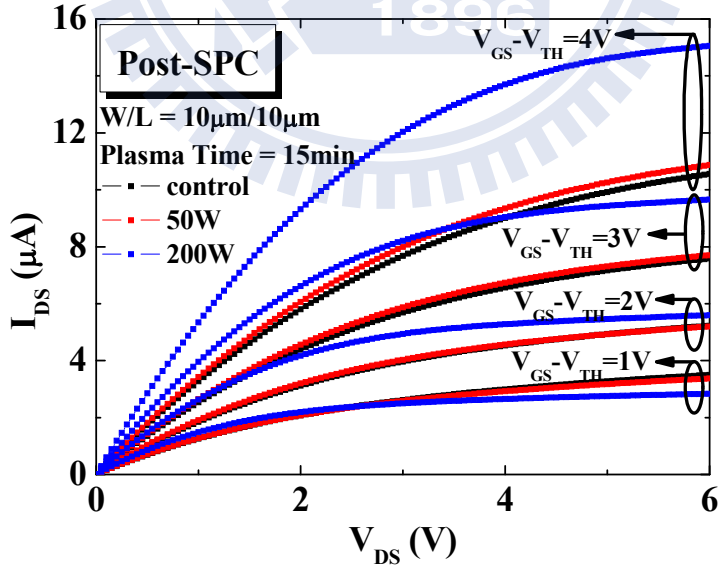


Fig. 3-23 I_{DS}–V_{DS} characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma post-SPC-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

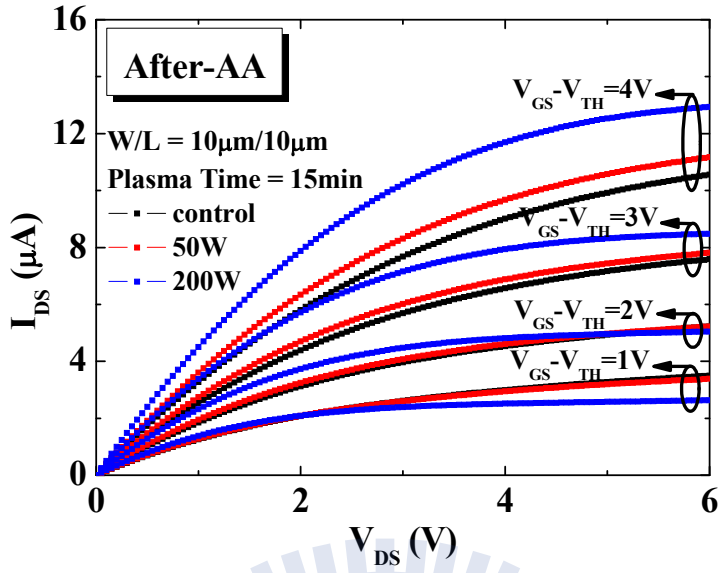


Fig. 3-24 I_{DS}–V_{DS} characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma after-AA-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

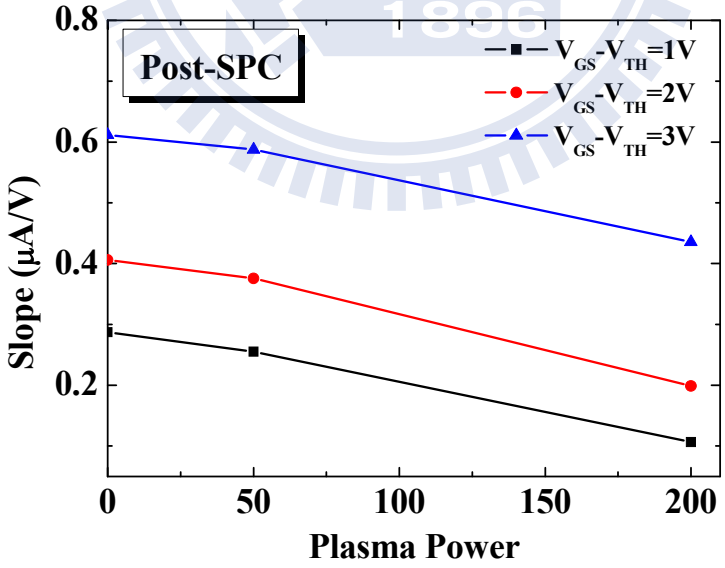


Fig. 3-25 Slopes of I_{DS}–V_{DS} characteristics (post-SPC-treatment) as a function of plasma treatment time (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

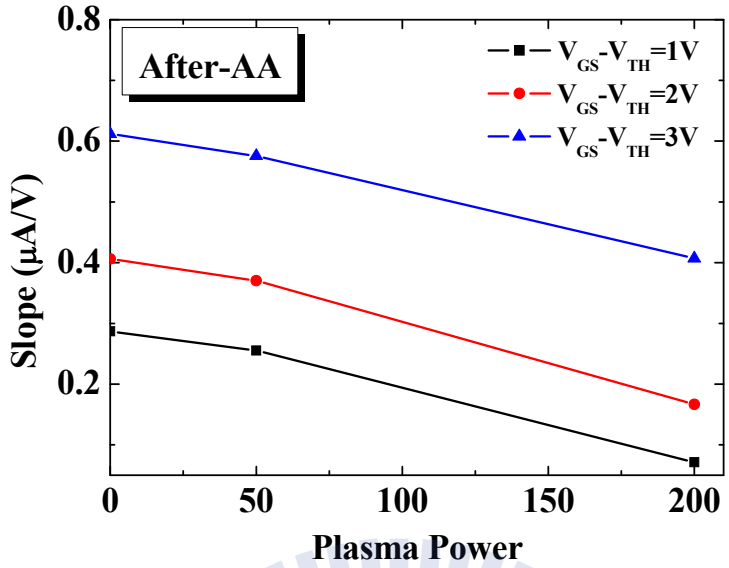


Fig. 3-26 Slopes of I_{DS}–V_{DS} characteristics (after-AA-treatment) as a function of plasma treatment time (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

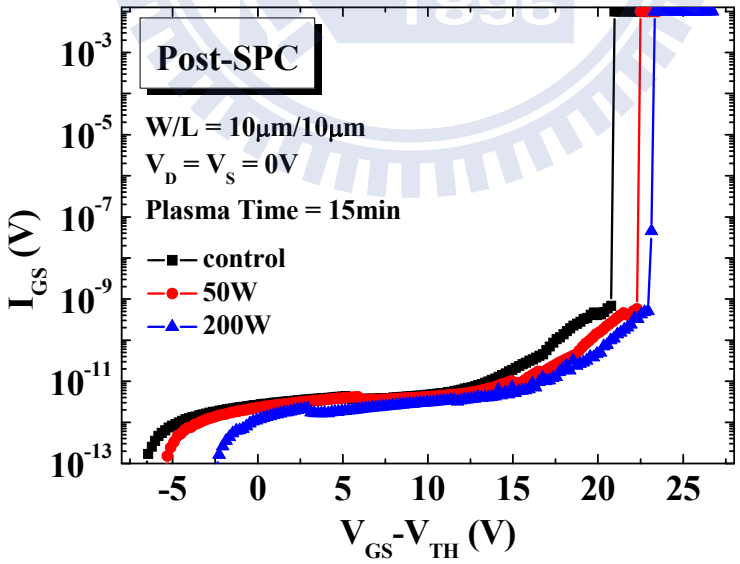


Fig. 3-27 Gate-leakage current characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma post-SPC-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

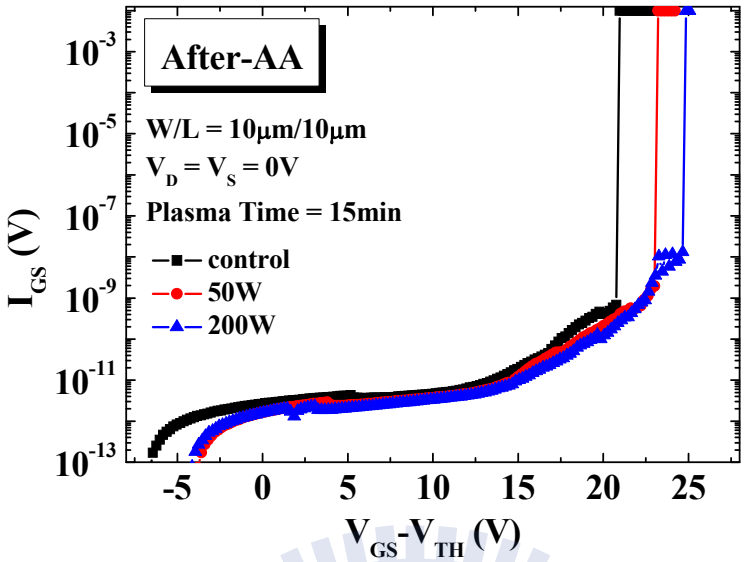


Fig. 3-28 Gate-leakage current characteristics of poly-Si TFTs for control sample and the samples with NH_3 plasma after-AA-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

Chapter 4

Impacts of Post-Metal-Annealing on Plasma-Treated Bottom Gate Poly-Si TFTs

4.1 Introduction

Due to the passivation effect of hydrogen and nitrogen radicals, NH_3 plasma treatment has been widely used to improve the performance and the hot-carrier reliability of poly-Si TFTs [4.1]-[4.2]. However, poly-Si TFTs with plasma treatment may lose their passivation effect after subjecting to high temperature annealing [4.2]-[4.3]. In this chapter, the impacts of post-metal-annealing on plasma-treated bottom gate poly-Si TFTs will be thoroughly studied.

4.2 Plasma Treatment Time Dependence

The comparisons of I_{DS}–V_{GS} and G_m–V_{GS} characteristics between the poly-Si TFTs with and without post-metal-annealing (PMA) are shown in Fig. 4-1 – Fig. 4-3. The samples with PMA were annealed at 400℃ for 30 minutes in N_2 ambient. The subthreshold double-hump phenomenon has been completely eliminated by PMA. In chapter 3, we hypothesized the subthreshold double-hump phenomenon was caused by the hole traps in the gate oxide at the corner edge portions, which were generated by plasma dry etching [4.4]-[4.5]. As a result, the elimination of the subthreshold double-hump phenomenon comes from the elimination of the hole traps in the gate oxide. Moreover, as shown in Fig. 4-1 (a) (curve: W/ PMA), because the hole traps in the gate oxide at the corner edge portions have been eliminated, the flat plate transistor with high V_{TH} dominates the I_{DS}–V_{GS} characteristics. PMA in N_2 ambient may be a method to annihilate the hole traps generated by plasma dry etching. In

addition, the I_{DS}–V_{GS} characteristics for the samples with 2 μm channel width are shown in Fig. 4-4 and Fig. 4-5. In chapter 3, we hypothesized the hole traps at the corner edge portions may construct a leakage path and lead to a large I_{OFF}. Nevertheless, after PMA, the I_{OFF} of all samples decrease significantly because PMA can eliminate the leakage path constructed by the hole traps.

Maximum transconductance (G_{m_max}) as a function of plasma treatment time for the samples with and without PMA are shown in Fig. 4-6. Substantial improvements of G_{m_max} for the poly-Si TFTs (pre-SPC-treatment) with PMA are measured. Surprisingly, control sample without any NH_3 plasma treatment has a large improvement of G_{m_max} with PMA. These improvements of G_{m_max} for the poly-Si TFTs with PMA are possibly due to the elimination of the hole traps in the gate oxide. Besides, the amounts of the improvements of G_{m_max} for each sample with different NH_3 plasma treatment time are almost the same.

However, for the poly-Si TFTs with NH_3 plasma post-SPC-treatment as shown in Fig. 4-7, the saturation phenomena of G_{m_max} for the samples with PMA have been measured. Without PMA, G_{m_max} become higher as plasma treatment time increases because more nitrogen and hydrogen radicals passivate the intra-grain defects. On the other hand, with PMA, the samples with and without NH_3 plasma have the G_{m_max} saturation value of about 113 nS. Even though longer NH_3 plasma treatment time yields better passivation effect, some nitrogen and hydrogen radicals release from the defect sites during high temperature PMA processing [4.2]-[4.3]. Therefore, the saturation phenomena of G_{m_max} can be attributed to the combination of following mechanisms: 1) the elimination of the hole traps in the gate oxide by PMA, 2) the out-diffusion of nitrogen and hydrogen radicals during PMA processing, and 3) the remaining passivation effect by NH_3 plasma.

Nevertheless, for the samples with NH_3 plasma after-AA-treatment as shown in

Fig. 4-8, although G_{m_max} saturates to 113 nS for plasma treatment of 60 min, it decreases from 113 nS to 105 nS as plasma time increases from 60 min to 120 min owing to heavier ion bombardment as plasma treatment time is further increased. Hence, the results of the G_{m_max} are attributed to the combination of following mechanisms: 1) the elimination of the hole traps in the gate oxide by PMA, 2) the out-diffusion of nitrogen and hydrogen radicals during PMA processing, 3) the remaining passivation effect by NH_3 plasma, and 4) the plasma-induced damage by NH_3 plasma.

4.3 Plasma Power Dependence

Fig. 4-9 – Fig. 4-11 illustrate the comparisons of I_{DS}–V_{GS} and G_m–V_{GS} characteristics between the poly-Si TFTs with and without PMA. Also, the subthreshold double-hump phenomenon has been completely suppressed because of the elimination of the hole traps in the gate oxide by PMA.

Maximum transconductance (G_{m_max}) as a function of plasma power for the samples with and without PMA are shown in Fig. 4-12 – Fig. 4-14. As shown in Fig. 4-12, for the poly-Si TFTs with NH_3 plasma pre-SPC-treatment, substantial improvements of G_{m_max} for the samples with PMA process have been measured due to the elimination of the hole traps in the gate oxide. Moreover, after PMA, the extent of the improvements of G_{m_max} for each sample with different NH_3 plasma power is almost the same.

The saturation phenomena of G_{m_max} for the samples (post-SPC-treatment) with PMA have been measured as shown in Fig. 4-13 because of 1) the elimination of the hole traps, 2) the out-diffusion of radicals, and 3) the remaining passivation effect. Meanwhile, with plasma power of 200 W, the samples without PMA have higher G_{m_max} than those with PMA ones since the out-diffusion of radicals during PMA

leads to the lost passivation effect.

Furthermore, as shown in Fig. 4-14, the sample with after-AA-treatment for 120 min has lower G_{m_max} than the sample with plasma treatment time of 60 min due to heavier ion bombardment as plasma treatment time is further increased. Thus, the results of the G_{m_max} are attributed to 1) the elimination of the hole traps, 2) the out-diffusion of radicals, 3) the remaining passivation effect, and 4) the plasma-induced damage.

4.4 Post-Metal-Annealing Time Dependence

4.4.1 Plasma Treatment Time Dependence

In order to clarify the influences of PMA, maximum transconductance (G_{m_max}) as a function of PMA time for the samples with different plasma treatment time are shown in Fig. 4-15 – Fig. 4-17. During PMA processing, some nitrogen and hydrogen radicals might release from the defect sites. By checking the G_{m_max} as a function of PMA time, we will know whether the poly-Si TFTs with after-AA-treatment do suffer from heavier ion bombardment damage or not.

As illustrated in Fig. 4-15, substantial improvements of G_{m_max} of the poly-Si TFTs after PMA for 30 min have been measured. As PMA time is further increased, G_{m_max} are almost the same. Therefore, we can presume that for the samples with pre-SPC-treatment, PMA for 30min might be sufficient to enhance G_{m_max}. Furthermore, the samples with NH_3 plasma pre-SPC-treatment have lower G_{m_max} than control sample without any plasma treatment owing to the smaller grain size and the out-diffusion of nitrogen and hydrogen radicals during high temperature SPC annealing.

In contrast, as shown in Fig. 4-16, G_{m_max} of the sample with post-SPC-treatment

for 120 min is not improved by PMA. Because G_{m_max} of the sample with post-SPC-treatment for 120 min before PMA is already high enough, the improvements by PMA (the elimination of the hole traps) are compensated by the out-diffusion of the radicals during PMA processing. These result in the saturation phenomena of G_{m_max}. Post-SPC-treatment for 120 min is the best way to obtain the highest G_{m_max} no matter the samples have been subjected to the PMA.

Interestingly, as presented in Fig. 4-17, before PMA, the sample with after-AA-treatment for 120 min has higher G_{m_max} than the counterparts because of higher passivation efficiency. On the contrary, after PMA, G_{m_max} of the samples with after-AA-treatment for 120 min have even lower G_{m_max} than the counterparts. Because after subjecting to PMA, the out-diffusion of radicals will lead to the lost passivation effect. Hence, it is noted that the ion bombardment becomes more serious for long plasma treatment time, leading to lower G_{m_max} compared with short plasma treatment time. We can hypothesize that for the sample with after-AA-treatment for 120 min, ion bombardment damage is indeed a non-negligible mechanism. And by the comparison with the samples with post-SPC-treatment, the samples with after-AA-treatment do suffer from heavier ion bombardment.

4.4.2 Plasma Power Dependence

Maximum transconductance (G_{m_max}) as a function of PMA time for the samples with different plasma power are shown in Fig. 4-18 – Fig. 4-20.

As shown in Fig. 4-18, substantial improvements of G_{m_max} of the poly-Si TFTs after PMA for 30min have been measured. Besides, G_{m_max} saturates to about 100 nS with PMA for 30 min. Therefore, PMA for only 30min is sufficient to enhance G_{m_max}. Moreover, the samples with NH_3 plasma pre-SPC-treatment have lower G_{m_max} than control sample without any plasma treatment because of the smaller grain size and the

out-diffusion of radicals during SPC annealing.

On the other hand, it is surprised to reveal that G_{m_max} of the sample with post-SPC-treatment power of 200 W is degraded by PMA as shown in Fig. 4-19. The reduction of G_{m_max} comes from the out-diffusion of the radicals during PMA processing. For the sample with post-SPC-treatment power of 200 W, the performance degradation induced by thermal instability is a critical issue.

As presented in Fig. 4-20, before PMA, the sample with after-AA-treatment power of 200 W has higher G_{m_max} than the counterparts because radicals have high kinetic energy and passivate traps more efficiently. Oppositely, after PMA, G_{m_max} of the samples with after-AA-treatment power of 200 W have even lower G_{m_max} than the counterparts, because these samples lose their passivation effect after subjecting to PMA. Furthermore, by the comparison with the samples with plasma power of 50 W, the fact becomes obvious that samples with power of 200 W suffer from heavier ion bombardment.

4.5 Summary

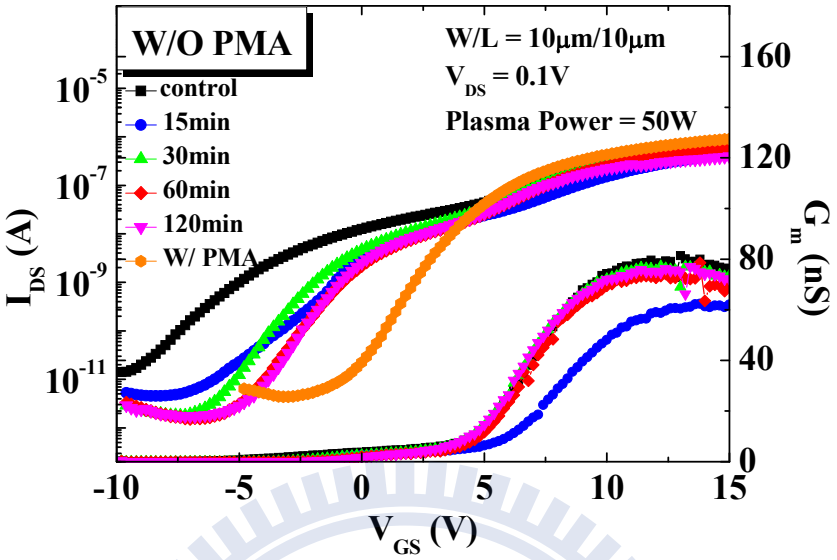
In this chapter, the impacts of post-metal-annealing on plasma-treated bottom gate poly-Si TFTs is thoroughly studied.

The subthreshold double-hump phenomenon has been completely eliminated by PMA owing to the elimination of the hole traps in the gate oxide. After PMA, the results of the G_{m_max} as a function of plasma treatment time are attributed to the combination of following mechanisms: 1) the elimination of the hole traps in the gate oxide by PMA, 2) the out-diffusion of nitrogen and hydrogen radicals during PMA processing, 3) the remaining passivation effect by NH_3 plasma, and 4) the plasma-induced damage by NH_3 plasma.

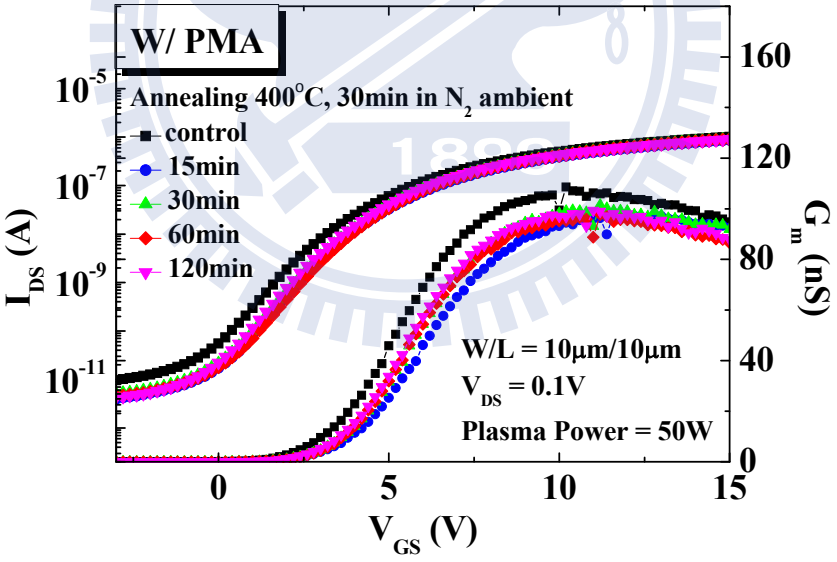
In addition, by checking the G_{m_max} as a function of PMA time, the samples with

after-AA-treatment do suffer from heavier ion bombardment than those with post-SPC-treatment ones.

Pre-SPC-treatment



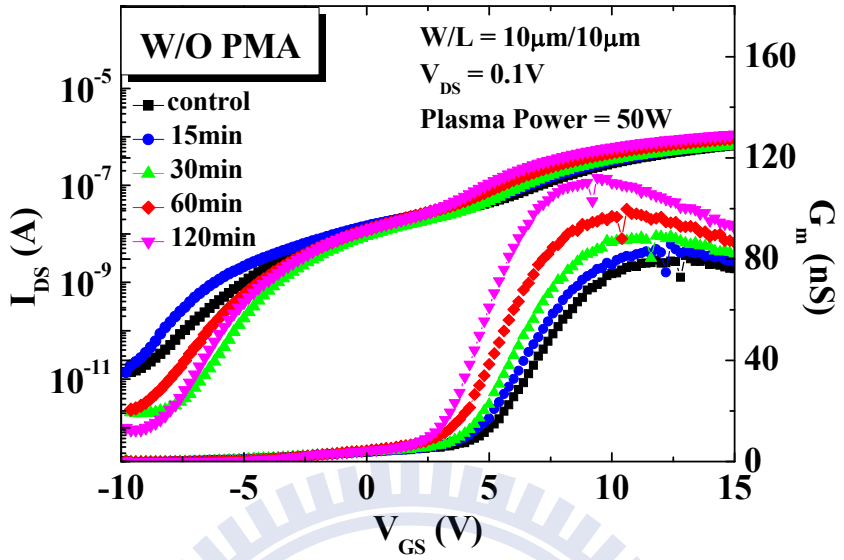
(a)



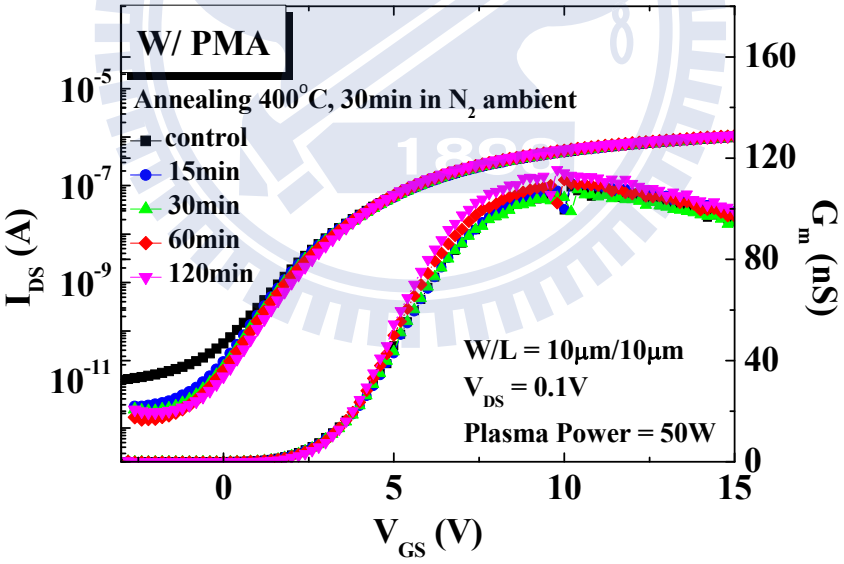
(b)

Fig. 4-1 I_{DS}–V_{GS} and G_m–V_{GS} characteristics of poly-Si TFTs (pre-SPC-treatment) (a) with and (b) without PMA (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

Post-SPC-treatment



(a)



(b)

Fig. 4-2 I_{DS}–V_{GS} and G_m–V_{GS} characteristics of poly-Si TFTs (post-SPC-treatment) (a) with and (b) without PMA (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

After-AA-treatment

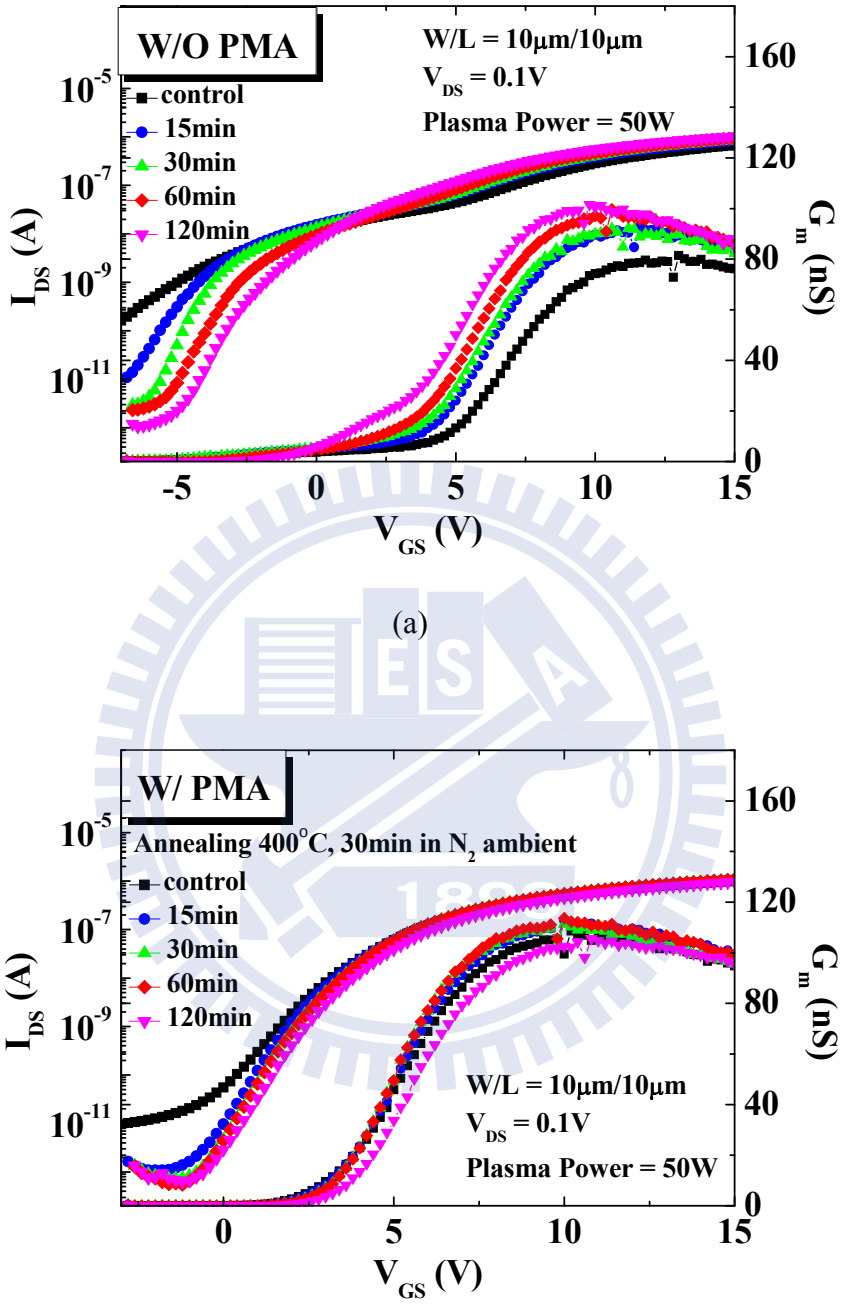


Fig. 4-3 I_{DS}–V_{GS} and G_m–V_{GS} characteristics of poly-Si TFTs (after-AA-treatment) (a) with and (b) without PMA (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

Post-SPC-treatment

(channel width = 2 μm)

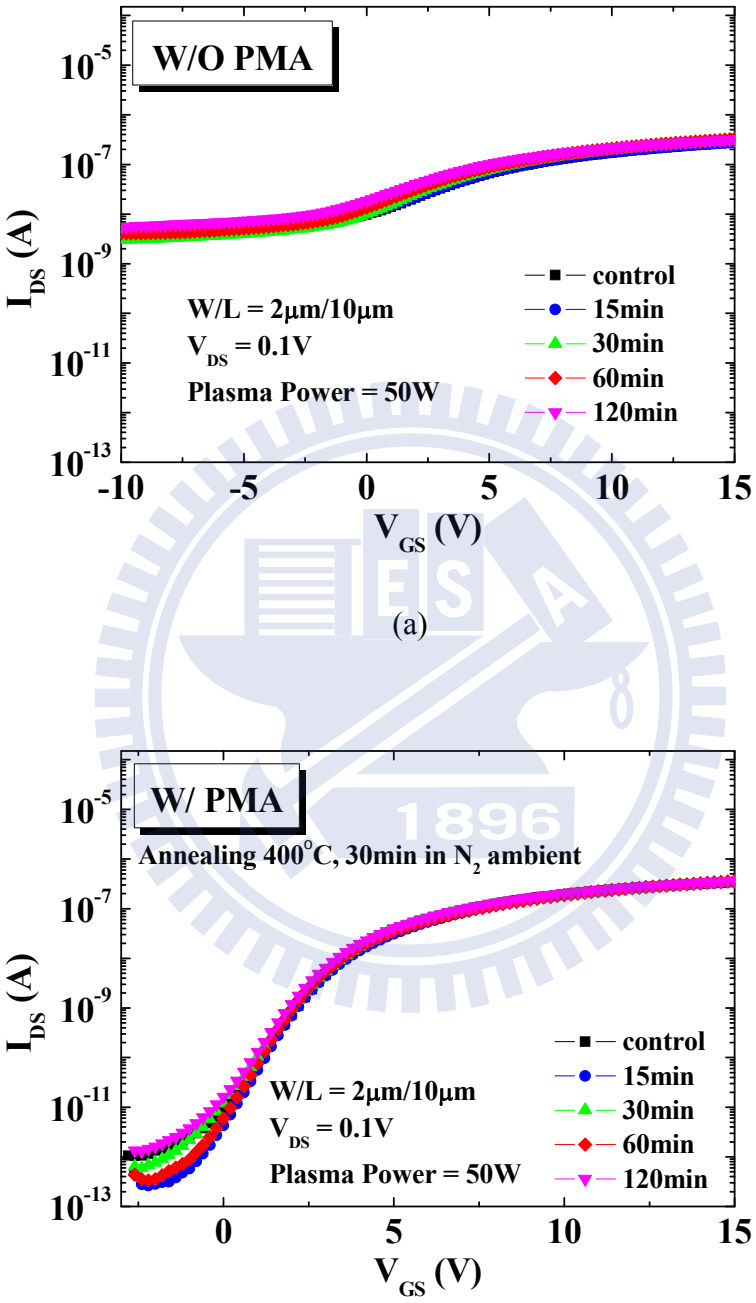
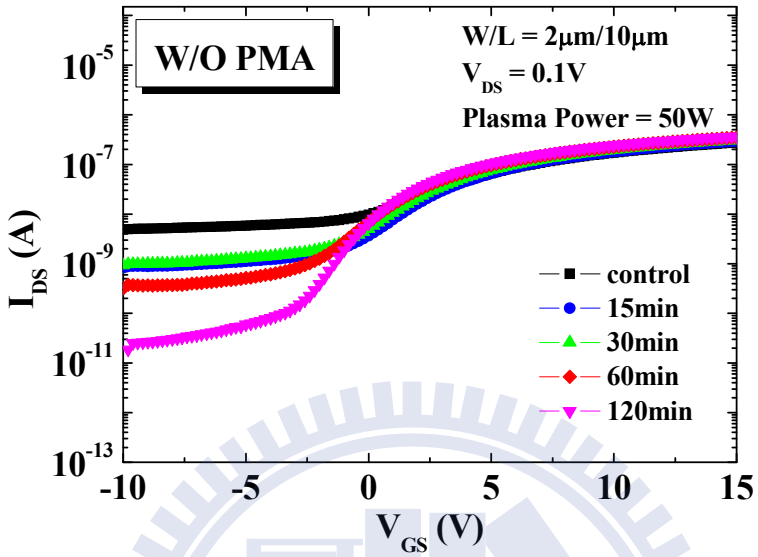


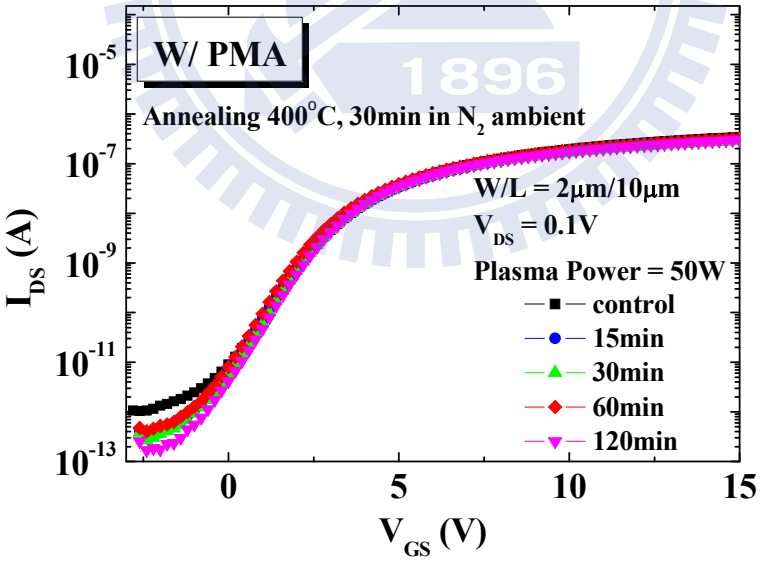
Fig. 4-4 I_{DS}–V_{GS} characteristics of poly-Si TFTs with 2 μm channel width (post-SPC-treatment) (a) with and (b) without PMA (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

After-AA-treatment

(channel width = 2 μm)



(a)



(b)

Fig. 4-5 I_{DS}–V_{GS} characteristics of poly-Si TFTs with 2 μm channel width (after-AA-treatment) (a) with and (b) without PMA (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

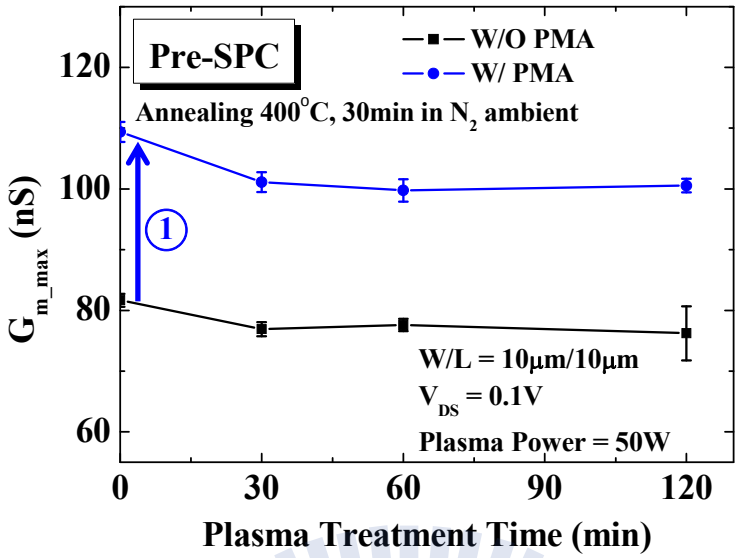


Fig. 4-6 Maximum transconductance (G_{m_max}) as a function of plasma treatment time for poly-Si TFTs with NH_3 plasma pre-SPC-treatment (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

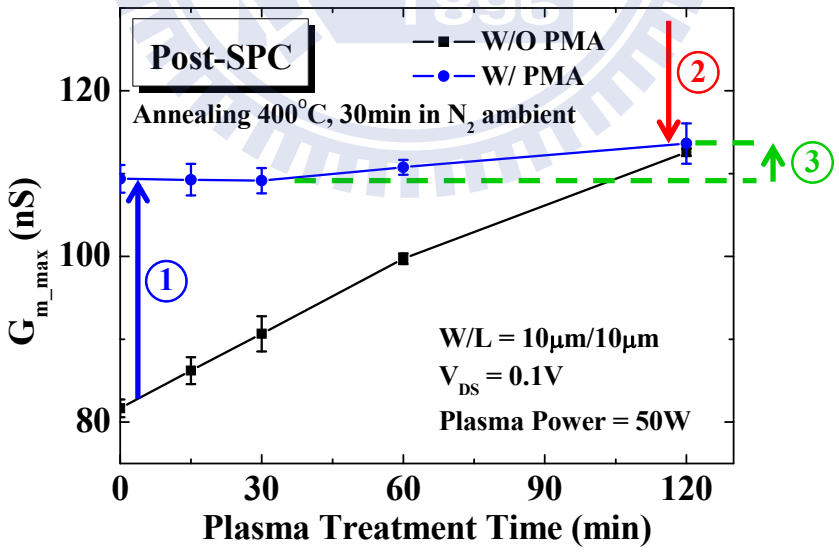


Fig. 4-7 Maximum transconductance (G_{m_max}) as a function of plasma treatment time for poly-Si TFTs with NH_3 plasma post-SPC-treatment (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

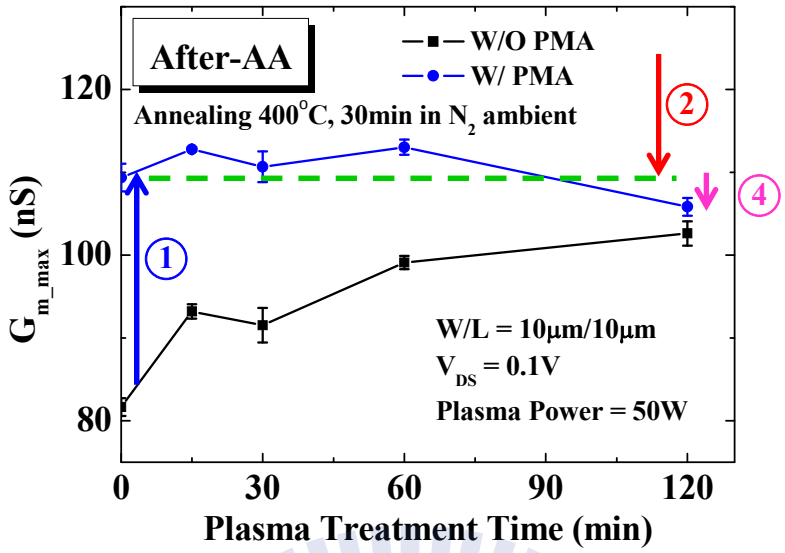


Fig. 4-8 Maximum transconductance (G_{m_max}) as a function of plasma treatment time for poly-Si TFTs with NH_3 plasma after-AA-treatment (plasma power = 50 W, plasma treatment time = 15 min to 120 min).

Pre-SPC-treatment

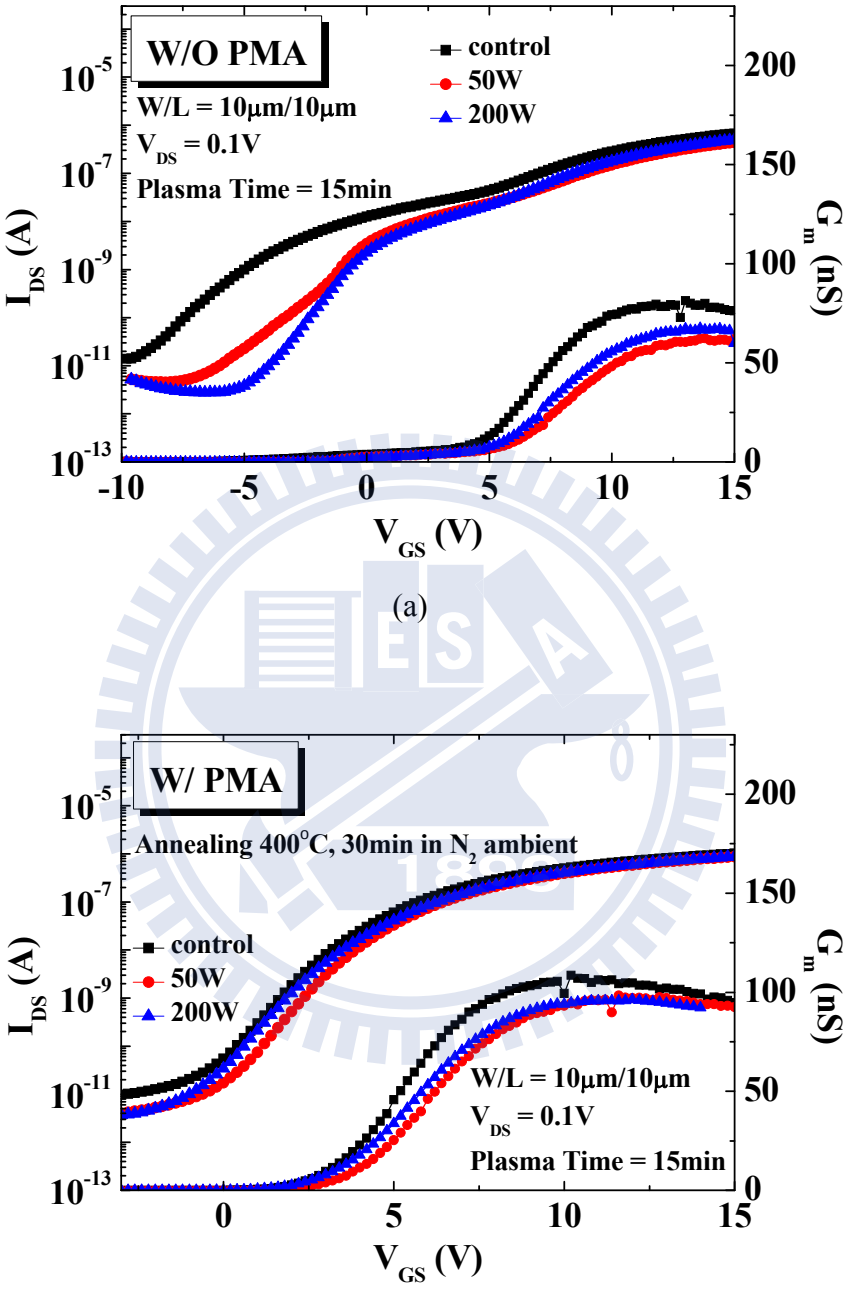
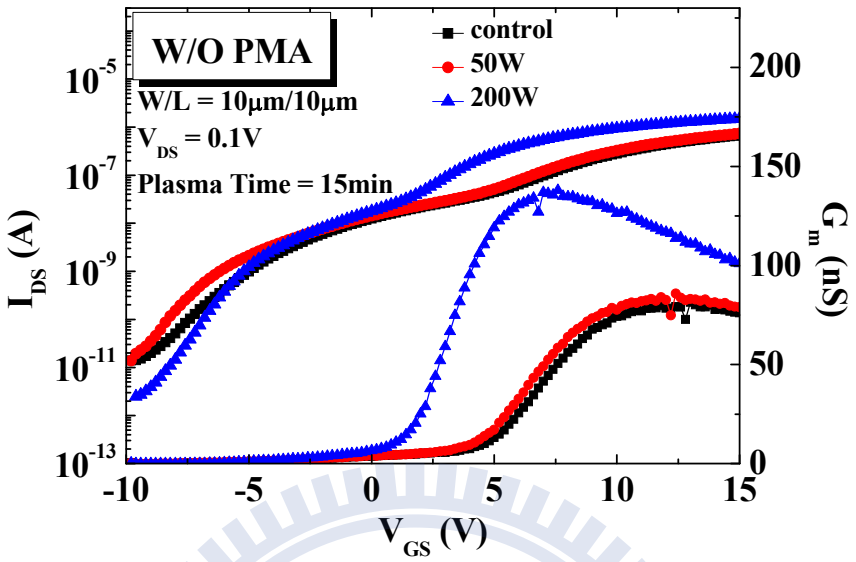
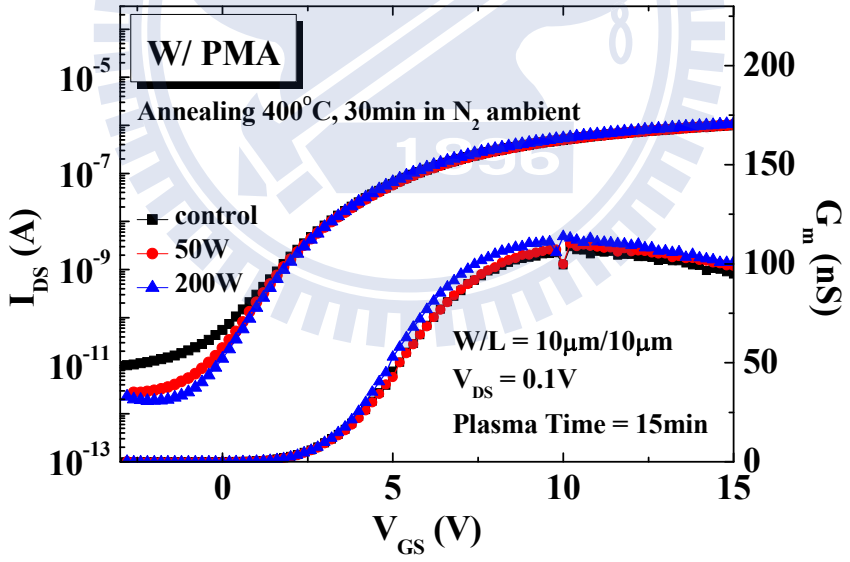


Fig. 4-9 I_{DS}–V_{GS} and G_m–V_{GS} characteristics of poly-Si TFTs (pre-SPC-treatment) (a) with and (b) without PMA (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

Post-SPC-treatment



(a)



(b)

Fig. 4-10 I_{DS}–V_{GS} and G_m–V_{GS} characteristics of poly-Si TFTs (post-SPC-treatment) (a) with and (b) without PMA (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

After-AA-treatment

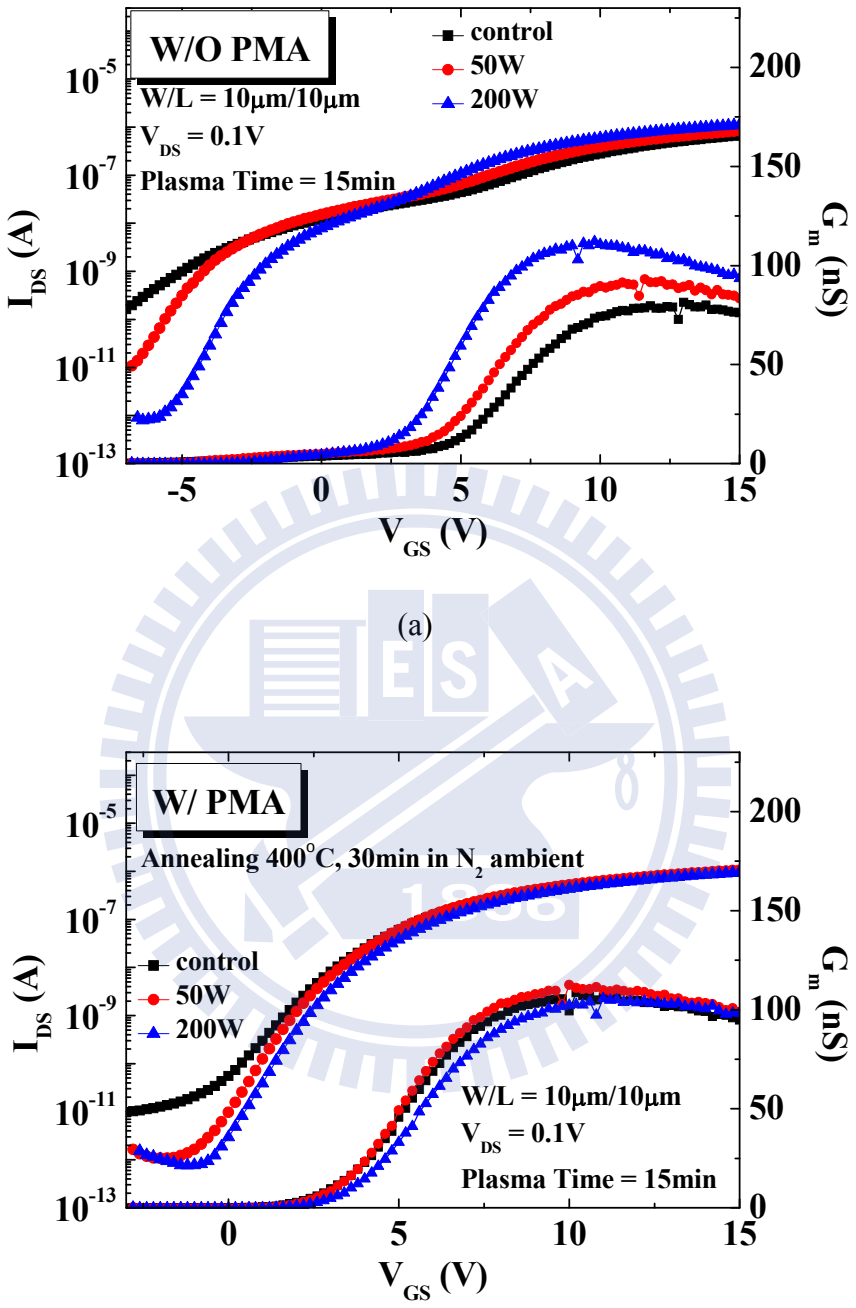


Fig. 4-11 I_{DS}–V_{GS} and G_m–V_{GS} characteristics of poly-Si TFTs (after-AA-treatment) (a) with and (b) without PMA (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

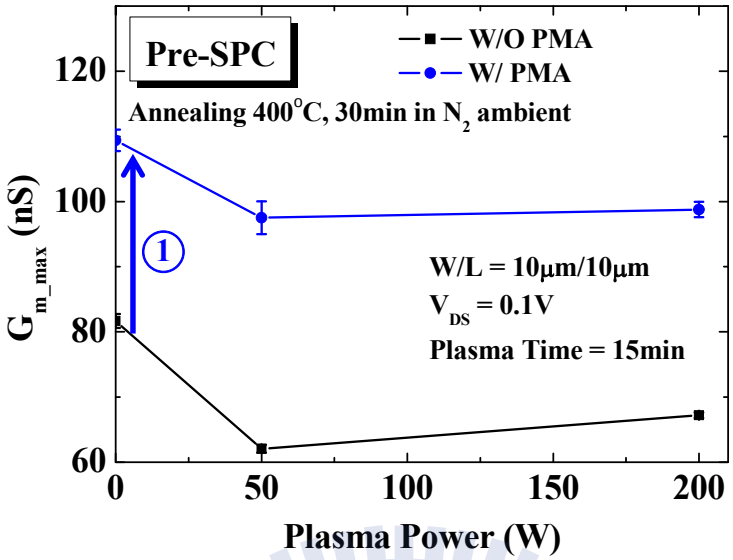


Fig. 4-12 Maximum transconductance (G_{m_max}) as a function of plasma power for poly-Si TFTs with NH_3 plasma pre-SPC-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

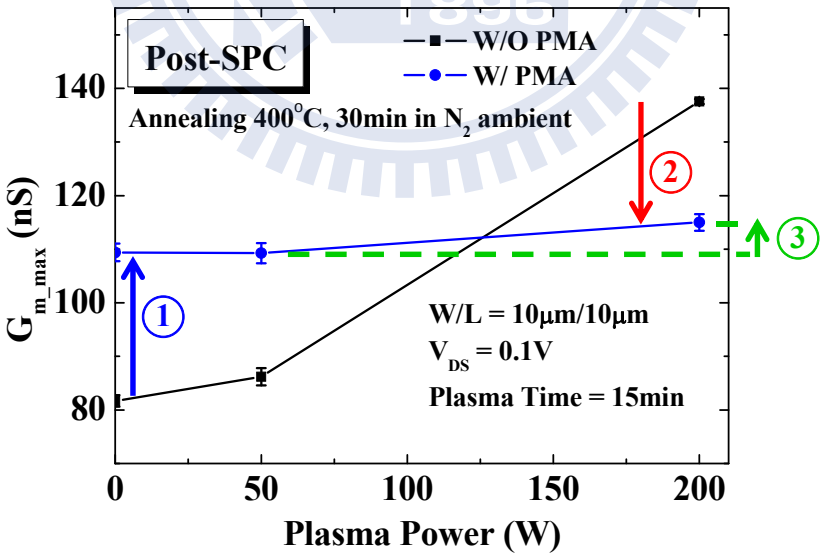


Fig. 4-13 Maximum transconductance (G_{m_max}) as a function of plasma power for poly-Si TFTs with NH_3 plasma post-SPC-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

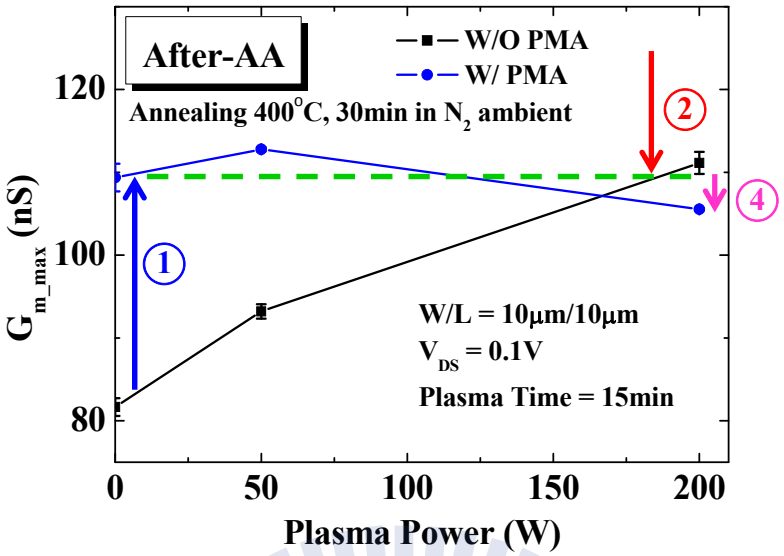


Fig. 4-14 Maximum transconductance (G_{m_max}) as a function of plasma power for poly-Si TFTs with NH_3 plasma after-AA-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

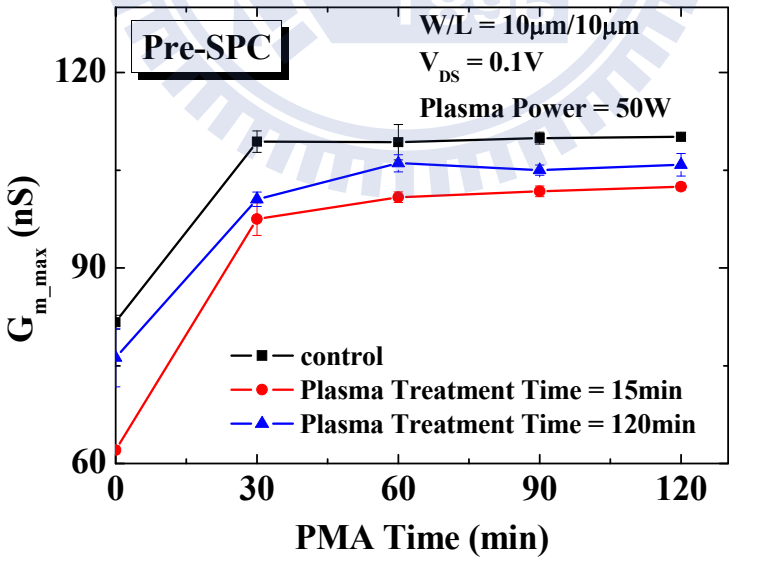


Fig. 4-15 Maximum transconductance (G_{m_max}) as a function of PMA time for poly-Si TFTs with NH_3 plasma pre-SPC-treatment (plasma power = 50 W, plasma treatment time = 15 min or 120 min).

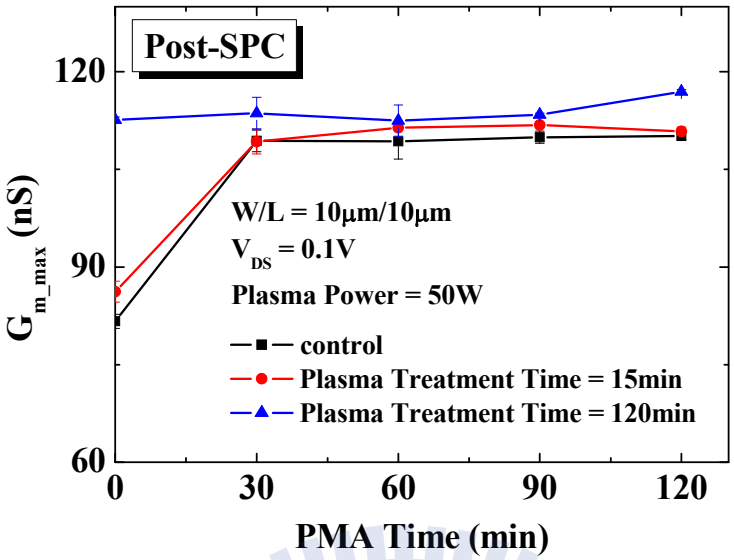


Fig. 4-16 Maximum transconductance (G_{m_max}) as a function of PMA time for poly-Si TFTs with NH_3 plasma post-SPC-treatment (plasma power = 50 W, plasma treatment time = 15 min or 120 min).

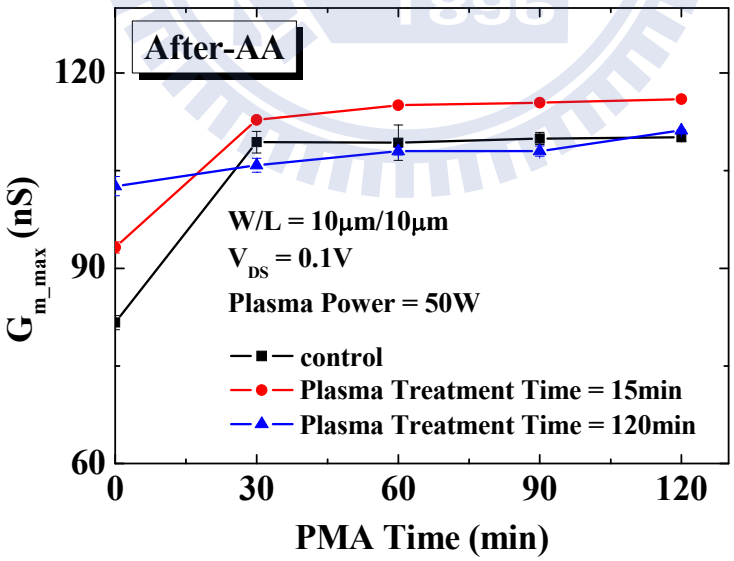


Fig. 4-17 Maximum transconductance (G_{m_max}) as a function of PMA time for poly-Si TFTs with NH_3 plasma after-AA-treatment (plasma power = 50 W, plasma treatment time = 15 min or 120 min).

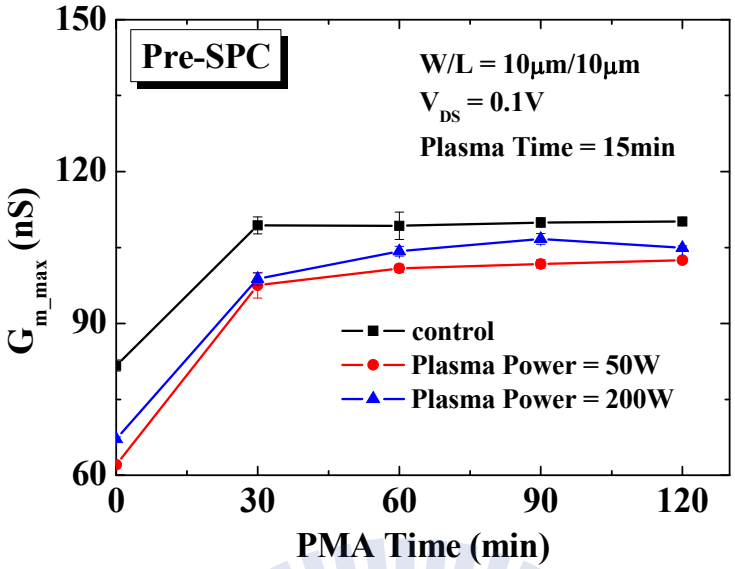


Fig. 4-18 Maximum transconductance (G_{m_max}) as a function of PMA time for poly-Si TFTs with NH_3 plasma pre-SPC-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

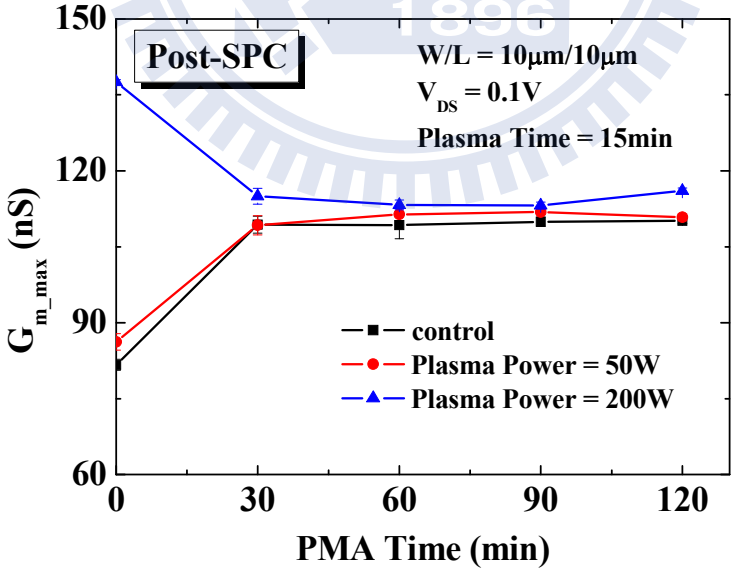


Fig. 4-19 Maximum transconductance (G_{m_max}) as a function of PMA time for poly-Si TFTs with NH_3 plasma post-SPC-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

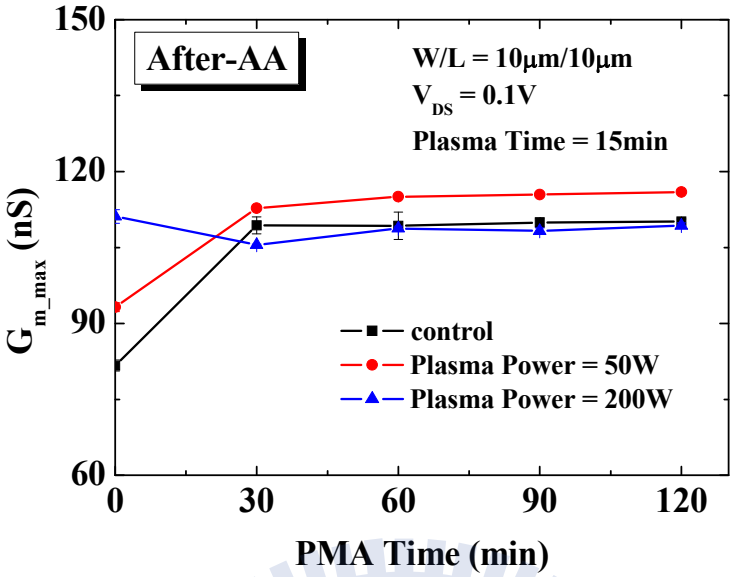


Fig. 4-20 Maximum transconductance (G_{m_max}) as a function of PMA time for poly-Si TFTs with NH_3 plasma after-AA-treatment (plasma power = 50 W or 200 W, plasma treatment time = 15 min).

Chapter 5

Conclusion and Implications for Future Research

5.1 Conclusion

In this study, the passivation effect of NH_3 plasma treatment on bottom gate poly-Si TFTs is thoroughly discussed. The poly-Si TFTs were exposed to NH_3 plasma with several conditions, including diverse stages, various plasma treatment time, and different plasma power.

Compared with the control sample without any plasma treatment, pre-SPC-treatment degrades device performance; however, post-SPC-treatment and after-AA-treatment improve device performance. The poly-Si TFTs with pre-SPC-treatment exhibit the worst performance owing to the smaller grain size and the out-diffusion of radicals during high temperature SPC annealing. On the contrary, the poly-Si TFTs with after-AA-treatment exhibit the best performance than the counterparts. After-AA-treatment is the most efficient technique to passivate traps since after-AA-treatment additionally passivates traps by radicals diffusing laterally through the gate oxide. Although after-AA-treatment passivates traps the most effectively, the poly-Si TFTs with after-AA-treatment suffer from the heaviest ion bombardment damage than those with post-SPC-treatment ones.

Moreover, longer plasma treatment time or higher plasma power enhance performance and alleviate kink effect more effectively. There are more radicals reach the SiO_2/poly-Si interface and passivate the traps with longer plasma treatment time or higher plasma power, leading to higher passivation efficiency. The bulk oxide quality is insensitive to the plasma with power of 50 W, because all samples with different plasma treatment time exhibit comparable gate-leakage current. On the other

hand, the plasma treatment with higher plasma power will strengthen the bulk oxide quality more significantly (Table. 5-1 and Table. 5-2).

Furthermore, the impacts of post-metal-annealing on plasma-treated poly-Si TFTs are systematically investigated. The plasma-treated poly-Si TFTs were subjected to PMA with annealing time varied from 30 min to 120 min. The subthreshold double-hump phenomenon has been completely eliminated by PMA. It is noted the subthreshold double-hump phenomenon is caused by the hole traps in the gate oxide, which is generated by plasma dry etching. Based on our results, PMA in N_2 ambient may be a method to eliminate the hole traps.

In addition, the performance of the poly-Si TFTs with PMA are mainly attributed to the combination of following mechanisms: 1) the elimination of the hole traps in the gate oxide by PMA, 2) the out-diffusion of nitrogen and hydrogen radicals during PMA processing, 3) the remaining passivation effect by NH_3 plasma, and 4) the plasma-induced damage by NH_3 plasma. By checking the G_{m_max} as a function of PMA time, the poly-Si TFTs with after-AA-treatment do suffer from heavier ion bombardment than those with post-SPC-treatment ones.

5.2 Implications for Future Research

We had clarified the passivation effect of NH_3 plasma treatment on bottom gate poly-Si TFTs in this study. However, we do not compare the passivation effect on bottom gate poly-Si TFTs with top gate ones. In order to know whether the structure of TFTs affect the passivation effect, the comparison between bottom gate and top gate is necessary.

It is known that NH_3 plasma treatment improves not only the electrical performance but also the hot-carrier reliability of poly-Si TFTs. The strong Si–N bonds with higher bonding energy will replace the weak Si–H bonds and lead to

excellent hot-carrier reliability. Therefore, investigating the hot-carrier reliability of these poly-Si TFTs may be interesting.

Although NH_3 plasma treatment is a technique to passivate traps, the ion bombardment damage is a non-negligible mechanism which degrades the performance and reliability of poly-Si TFTs. Hence, the technique that has the passivation effect and has no ion bombardment issue, such as hydrogen-containing nitride film deposition, may improve device performance more obviously than NH_3 plasma treatment. Besides, since radicals can terminate traps and improve performance of poly-Si TFTs, the performance of memory devices may also be improved by radicals. Thus, the passivation effect on memory and transistor by capping hydrogen-containing nitride layer will be systematically investigated.

Table 5-1 The comparison of different plasma treatment time.

	V_{TH}				G_{m_max}			
	15 min	30 min	60 min	120 min	15 min	30 min	60 min	120 min
Post-SPC-treatment							○	○
After-AA-treatment	○	○	○	○	○	○		

Table 5-2 The comparison of different plasma power.

	V_{TH}		G_{m_max}		Bulk Oxide Quality	
	50 W	200 W	50 W	200 W	50 W	200 W
Post-SPC-treatment		○		○		
After-AA-treatment	○		○		○	○

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簡歷 (Vita)

姓　名：陳儀儒

性　別：女

出生日：1989 年 2 月 3 日

籍　貫：臺灣 新北市

出生地：臺灣 新北市

學　歷：

國立屏東女子高級中學

2004 年 9 月~2007 年 6 月

國立彰化師範大學物理學系 學士班

2007 年 9 月~2011 年 6 月

國立交通大學電子物理學系 碩士班

2011 年 9 月~2013 年 6 月

碩士論文題目：

氨電漿對下閘極多晶矽薄膜電晶體之影響

Effects of NH_3 Plasma Treatment on Bottom Gate

Poly-Silicon Thin-Film Transistors