A 1.9mW Portable ADPLL-based Frequency Synthesizer for High Speed Clock Generation

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***Abstract*—An ADPLL-based frequency synthesizer has been designed and implemented with TSMC 130nm technology model. The cores of it are digital controlled oscillator (DCO) and phase frequency detector (PFD). A modified digitally controlled delay element (DCDE) with characteristics of its monotonicity and insensitivity to PVT variations is presented for the DCO design. A new PFD architecture that can finish phase and frequency comparison and adjustment in one reference cycle is presented. This frequency synthesizer can operate from 300MHz to 1GHz, and achieve frequency acquisition in fifteen reference clock cycles (worst case scenario). The peak-to-peak jitter of the output clock is less than 120ps at 300MHz. Furthermore, the design has been ported to TSMC 100nm process as a reusable IP block verification. The total power dissipation of the ADPLL-based frequency synthesizer is 1.9mW (TSMC 100nm technology) at 1GHz with a 1.2V power supply. With such specifications, it is suitable for high speed clock generation in system-on-a-chip (SoC) applications.**

I. Introduction

The phase-locked loop (PLL) has been designed for application and integration on high speed microprocessors. In traditional mixed-signal system, PLL is usually implemented by analog building block. However, owing to desirable characteristics relating to system integration in state-of-the-art complex SoC environment, all digital phase-locked loop (ADPLL) is currently chosen for system frequency synthesis applications. Not only insensibility to process variations but also portability to each new technology is preferred by SoC applications.

It is too hard to use the same analog PLL design in different process [1], [2]. On the other hand, ADPLL is much easier to fabricate without targeting a specific technology. Their area would also scale down quickly as the technology shrinks if only active components are used. Examples of ADPLLs are described in [3]-[5]. Although LC tank digitally controlled oscillator which is compose of passive components achieves very fine frequency resolution (23kHz) [6], this DCO simultaneously suffers the finest pMOS varactor is 38 attofarads. Such passive component lies on advanced lithography technology and intensive circuit layout that substantially decrease the design cycle efficiency. Not only portability but also area-effective low-power capability would be emphasized in this paper.

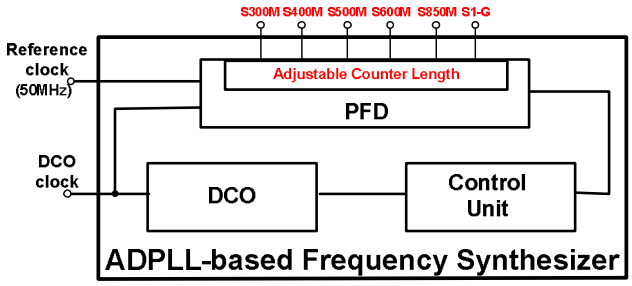

Figure 1. ADPLL-based frequency synthesizer block diagram.

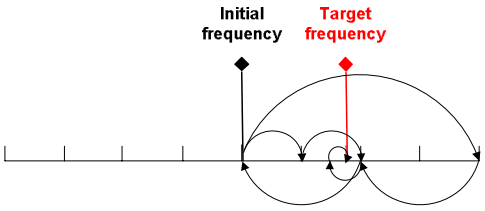

Figure 2. Modified binary search algorithm.

The rest of this paper is organized as follows: Section II describes the architecture and lock procedure of the ADPLL. The proposed modified DCDE and PFD circuit designs which are used in the ADPLL are shown in Section III. Section IV is the implementation of an ADPLL-based frequency synthesizer of high speed clock generation. The implementation has been done with both TSMC 130nm and 100nm technology model to verify its portability. Section V shows the simulation result and layout view. Finally, some conclusions are given in section VI.

II. Architecture and Lock Procedure of ADPLL

The block diagram of the ADPLL is depicted in Fig. 1. There are three major building blocks in the proposed ADPLL; they are phase frequency detector (PFD), digitally

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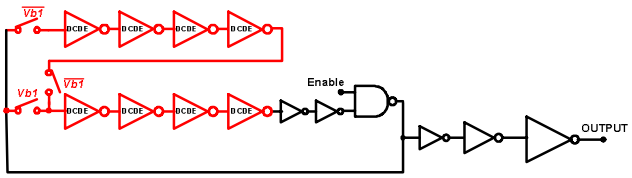

Figure 3. Digitally controlled oscillator (DCO).

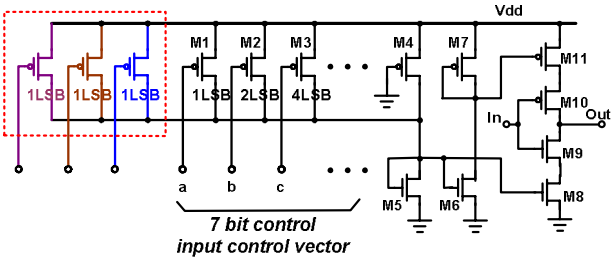

Figure 4. Modified digitally controlled delay element (DCDE).

controlled oscillator (DCO), and control unit (CU). The conventional ADPLL uses four modes of operation: frequency acquisition, phase acquisition, frequency maintenance, and phase maintenance. First, frequency acquisition mode adopted binary search algorithm to sweep all the available frequency output of DCO. This mode is trying to match the reference clock. Second, the algorithm changes DCO control word based on the output signals of the PFD to ensure phase acquisition mode completed. Finally, both frequency and phase maintenance modes are executed to keep ADPLL locked. Each mode is like a "search" algorithm with different scheme. This paper uses a modified binary search algorithm [4] to find the target frequency. The algorithm reduces the frequency gain by a factor of two when the search direction has been changed. The details are shown in Fig. 2.

III. CIRCUITS DESIGN OF ADPLL

A. *Digitally Controlled Oscillator*

The architecture of DCO is presented in Fig. 3. The proposed DCO circuit has 11-bit resolution, including coarse tune (1-bit) and fine tune (7-bit + 3-bit) parts. In coarse tune part, the number of delay element is chosen to cover different frequency band. The number of delay element will increase rapidly, thus, the circuit will consume much more power. Furthermore, the cover band between bands to bands will also decrease the operation frequency range. In a nutshell, only 1-bit control word has been used as a path selector.

In fine tune part, the new digitally controlled delay element (DCDE) [7], [8] is adopted with 7-bit resolution in consideration of linearity. The delay of the DCDE changes monotonically with respect to the digital input vector. The main idea of the DCDE is to adjust the delay difference by using current-mirror-based circuit in binary-weighted fashion.

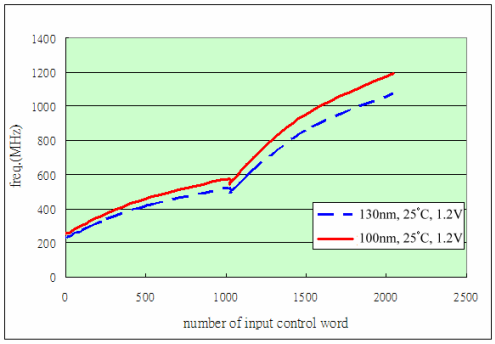

Figure 5. DCO frequency versus number of the input vector.

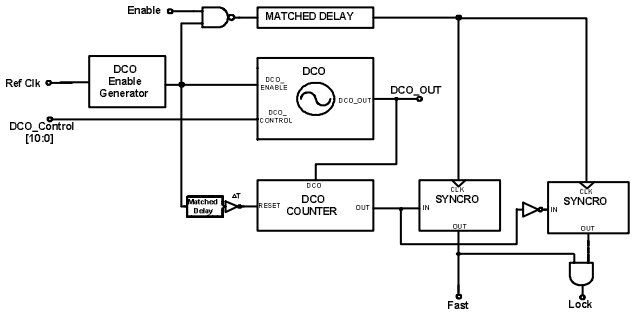

Figure 6. Phase/Frequency detector (PFD).

The most significant advantages of such delay element are its monotonicity and PVT variations immunity.

The minimum delay difference caused by an LSB, however, would increase in proportional to the increase of delay element. Based on that, a modified DCDE is presented, shown in Fig. 4. Initially, every two DCDEs have been taken as a group and chosen one of them to add a minimum delay difference PMOS. In other words, it is equivalently increase 1-bit resolution of proposed DCO circuit. Both simulation results (TSMC 130nm and 100nm technology) are shown in Fig. 5. The operation frequency range is in 224MHz – 1.06GHz, and the LSB resolution is 0.4 – 20ps. Power consumption is 0.9mW at 1GHz. Meanwhile, exact same design has been ported to TSMC 100nm technology. It has similar behavior (250MHz – 1.15GHz, 0.68mW at 1GHz).

B. *Phase Frequency Detector*

In conventional ADPLL design, PFD is composed of frequency comparator (FC) and phase detector (PD). The FC accepts the reference clock and DCO output as its inputs. By these two signals, the FC generates FAST, SLOW, and ENABLE output signals for the DCO. The ENABLE signal forces the reference clock edge and the DCO output edge to align in phase. Then, the PD also uses the same two signals to generate AHEAD or BEHIND output signals.

The proposed PFD, shown in Fig. 6, would enable DCO and start count the DCO output cycle at the rising edge of the reference clock. The falling edge of the reference clock

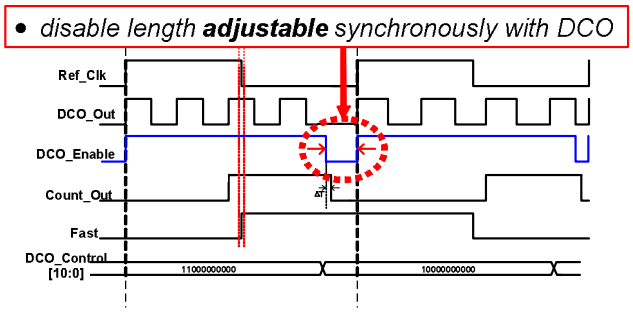

Figure 7. Timing diagram of PFD *(divider ratio = 2)*.

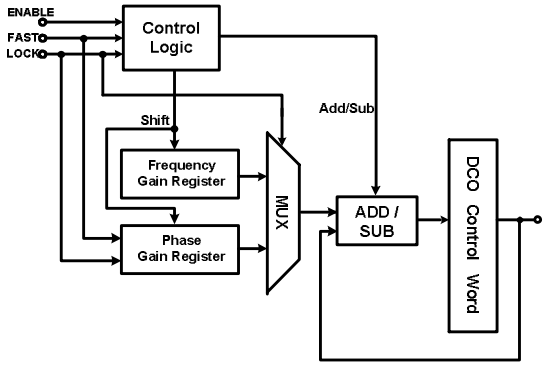

Figure 8. Block diagram of the control unit.

Figure 9. The strategy to adjust the phase gain register

captures the output and the inversion of the DCO counter which are the input to the synchronizer. If the output of the DCO counter arrives before the falling edge of the reference clock, the output of DCO divider is defined as FAST. The fast signal will be pulled up. Otherwise, it will be defined as SLOW, and the fast signal will be pulled down. Only when both the two synchronizers' output are high, the lock signal will be high. Meanwhile, the ADPLL will enter the lock state.

The conventional FC circuit takes one half reference cycles for synchronization before asserting SLOW or FAST. In the rest clock, the DCO is disabled. That would need two reference clock cycles to finish a full FC iteration. To settle such difficulty, a dual-mode one-cycle PFD is proposed.

The detailed timing diagram is shown in Fig. 7. First, the frequency and phase detection point is set at the falling edge of the reference clock. Second, a new flag signal is generated by DCO enable generator circuit. The signal will only disable the DCO before the rising edge of next reference clock cycle. It will last half DCO output cycle to synchronize with the reference clock. Consequently, PFD

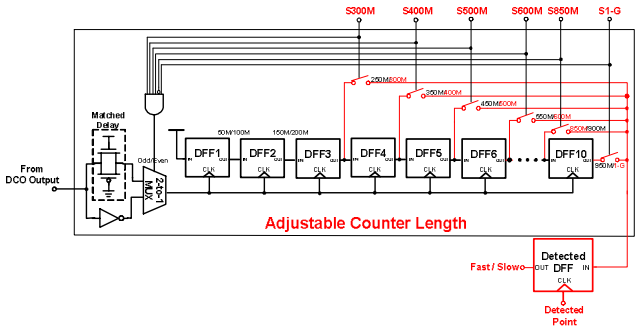

Figure 10. Adjustable length of the DCO counter.

TABLE I. Frequency of the output clock and input control signal

input control signal	output clock frequency
S300M=1, others=0	300MHz
S400M=1, others=0	400MHz
S500M=1, others=0	500MHz
S600M=1, others=0	600MHz
S850M=1, others=0	850MHz
S1-G=1, others=0	1-GHz

could finish frequency and phase comparison in only one reference clock cycle.

C. *Control Unit*

Control unit (CU) will adjust the DCO control word to change DCO output frequency according to the fast signal and lock signal received from PFD. The architecture of control unit is shown in Fig. 8, and it is based on the modified binary search algorithm. First, CU will decide if it needs to shift the frequency gain register to the right one bit by telling if the fast signal changed. Then, the control word will be added to value in the gain register if the fast signal is low, and vice versa.

After the ADPLL is locked, the reference clock or DCO output would still be changed by the PVT variations. Frequency gain register is replaced by phase gain register to let the ADPLL switch to maintenance mode. It can make sure of the phase error being minimized. Fig. 9 is used as an example of the procedure of gain value adjustment. The step 1 is set the initial value of the 4-bit phase gain register as 0001. The register will be shifted 1-bit to the left when PFD detects the fast signal remains the same for eight reference cycles. The register will be shifted 1-bit to the right, otherwise, as the fast signal changed. The gain register can only be 0001, 0010, 0100, and 1000.

IV. ADPLL-BASED FREQUNECY SYNTHESIZER

The proposed ADPLL-based frequency synthesizer is based on tunable counter length mechanism, as shown in Fig. 10. If 500MHz clock output, for example, is desired, the

TABLE II. Performance summary of the portable frequency synthesizer

ADPLL-based Frequency Synthesizer	
Reference clock	50MHz
Output Clock Freq.	300MHz - 1GHz (6 frequencies)
Jitter (p-p)	48.5ps at 1GHz (best case) 120ps at 300MHz (worst case)
Locked time	no more than 15 input cycles
Power consumption	2.9mW at 1GHz (130nm process) 1.9mW at 1GHz (100nm process)
Area	100um x 120um (130nm process)
Supply voltage	1.2V
DCO	
Frequency Range	224MHz~1.06GHz
Resolution	11bits (0.4ps ~ 20ps / LSB)
Power consumption	0.9mW at 1GHz (130nm process) 0.68mW at 1GHz (100nm process)

S500M signal will be set as 1. The fifth D Flip-Flop output signal would be selected to compare with matched delay reference clock. Finally, the ADPLL will generate 500MHz clock output when the state is lock. The relationship between control signal and output frequency is shown in Table I. Also, entire system has been simulated under different temperature and supply voltage value. The results are shown in Fig. 11.

V. Implementation and Simulation Results

The layout of the ADPLL-based frequency synthesizer is shown in Fig. 12. The area is 100um x 120um in TSMC 130nm CMOS technology. The frequency synthesizer runs up to 1GHz (50MHz x 20) with supply voltage 1.2V, and the resolution is 11 bits. The total power consumption of ADPLL-based frequency synthesizer is 2.9mW, and the jitter is 48.5ps at DCO output frequency 1GHz. The locking process takes at most 15 cycles of the reference clock. Performance summary of the proposed frequency synthesizer is shown in Table II.

VI. Conclusions

In this paper, a 1.9mW portable ADPLL-based frequency synthesizer with wide frequency range, low jitter, and short lock cycle is proposed.

A DCO with features of wide frequency range, and low power consumption is proposed. By using the modified DCDEs, the DCO also has better linearity and PVT variation immunity than the conventional DCO. In addition, a dual-mode one-cycle PFD is also presented to reduce the lock cycle time.

In conclusion, with such specifications, the proposed ADPLL-based frequency synthesizer is suitable for high speed clock generation in SoC applications.

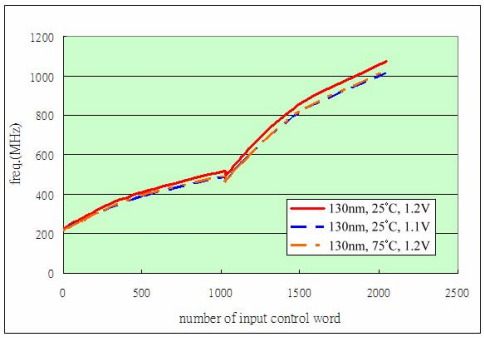

Figure 11. Frequency output in different temperature and voltage value

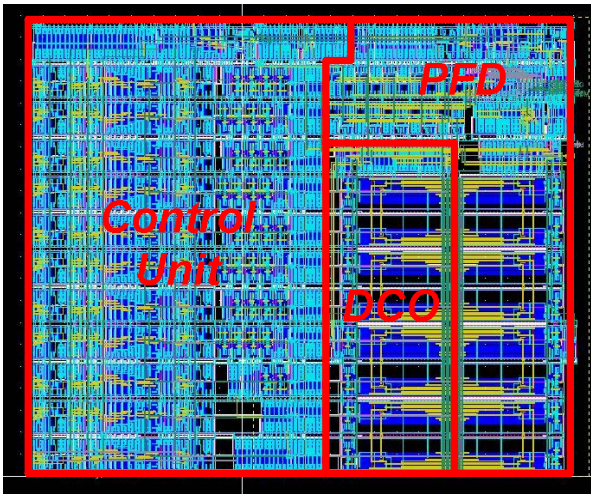

Figure 12. Layout floorplan.

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