國立交通大學

電子工程學系　電子研究所

博士論文

應用於離散時間三角積分調變器之校正技術

Calibration Techniques for Discrete-Time Delta-Sigma Modulators

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摘要

本論文發展應用於離散時間三角積分調變器的校正技術，藉此恢復調變器的雜訊形變能力，完成高速高解析度的類比數位轉換。校正技術能在背景執行，不影響三角積分調變器的正常運作。所發展的校正技術大幅放寬離散時間調變器對運算放大器電壓增益的要求，還可以放寬串疊式調變器對濾波器匹配的要求。

寬頻的離散時間三角積分調變器,其採用的放大器必須犧牲電壓增益，以達到高速的要求。如此導致積分器漏損的問題發生。使得三角積分調變器的解析度下降。本論文提出解決此問題的積分器漏損校正技術。積分器的漏損在數位端檢測，並在積分器類比端進行補償。此技術適用於任何有積分器漏損問題的離散時間三角積分調變器。因為運算放大器電壓增益的要求被大幅放寬，我們提出的積分器漏損校正技術，能在高解析度的前提下，讓離散時間調變器突破速度上限，達到高速的目標。

串疊式三角積分調變器的類比濾波器和數位雜訊消除器無法完全匹配，其訊雜比會因為雜訊漏損問題而嚴重下滑。本論文提出只需簡單電路便可解決此問題的雜訊漏損校正技術。利用頻寬外的測試訊號，檢測雜訊漏損發生與否，並調整數位雜訊消除器的增益，消彌雜訊漏損。此技術放寬在串疊式調變器所需的匹配規格，讓調變器完成高階雜訊形變。

一個以六十五奈米金屬氧化物半導體製程實現的 2-2 串疊式三角積分調變器，被用來驗證所提出的校正方法。這調變器的每一級都由兩個含有低增益高速運算放大器的積分器所構成。首先，積分器漏損校正技術會減少第一級的積分器漏損量，接著，雜訊漏損校正技術會匹配類比濾波器和數位雜訊消除器。因為這兩技術的作用，調變器得以完成高速高解析度的數位類比轉換。

實作出之串疊式調變器有效面積 0.58x0.33 平方釐米，調變器採用開路增益只有十倍的運算放大器，使調變器能以每秒十一億次的時脈工作。調變器的過取樣比率為三十三,輸入訊號頻寬為一千六百六十七萬赫茲，供應電壓一伏特，消耗功率九十四毫瓦。校正啟動前，訊雜比是 54dB ，而動態範圍是 60dB 。校正啟動後，訊雜比變成 74dB ，而動態範圍提升到 81dB 。該三角積分調變器的效能指標為 163.5dB 。

Calibration Techniques for Discrete-Time Delta-Sigma Modulators

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Abstract

This thesis presents background calibration techniques to reshape the capability of noise shaping of discrete-time (DT) Delta-Sigma modulators (DSMs). The calibration can operate in the background without interrupting the normal operation of the DSM. The proposed scheme relaxes the requirement of opamp DC gain in a DT DSM. and relaxes the matching requirement in a cascaded-DSM.

The opamp in a DT DSM is requested to sacrifice the DC gain for wide-band applications. This induces the issue of integrator-leakage and a degraded signal-to-noise-and-distortion ratio (SNDR). We develops an integrator-leakage calibration technique for a DT DSM. In the calibration of an integrator, its integration leakage is determined in the digital domain, and the leakage compensation is applied to the same integrator in the analog domain. The proposed scheme can be used to calibrate all of the integrators in a DT DSM of any form. The developed scheme can relax the requirement of opamp DC gain in the high-speed high-resolution DT DSMs.

A cascaded DSM without the perfect matching between analog loop filters and digital noise cancellation filters exhibits a degraded SNDR due to noise leakage. We develops an noise-leakage calibration technique with low-complex circuits. The noise leakage is determined by injecting an out-of-band signal, and the leakage is eliminated by merely adjusting the gain of digital filter. The developed scheme can relax the matching requirement in the cascaded DSMs and accomplish the higher-order noise shaping.

A 2-2 cascaded discrete-time DSM is fabricated in a 65 nm CMOS technology. Each stage of DSM consists of two integrators realized the low gain high speed opamp. The integrator leakage originated in the first stage is reduced by integrator leakage calibration at first. Then, the mismatch between the analog loop filter and the digital noise cancellation filter is cured by noise leakage calibration. The proposed calibrations enable the modulator to perform the high-speed high-resolution analog-to-digital conversion.

The active area of the fabricated DSM is 0.58×0.33 mm^2. This cascaded DSM with open-loop opamp gain of 20 dB is operating at 1.1 GHz clock rate. Its OSR is 33 and its bandwidth is 16.67 MHz. The DSM consumes 94mW from 1.0 V power supply. Before activating the calibrations, the SNDR is 54 dB and the dynamic range (DR) is 60 dB. After activating the integrator leakage calibration and the noise leakage calibration, the SNDR becomes 74 dB and the DR becomes 81 dB. The figure-of-merit of the DSM is 163.5 dB.

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吳書豪

國立交通大學

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Chapter 1

Introduction

1.1 Motivation

The developments of anlog-to-digital converters (ADCs) are driven by the increasing demand for signal bandwidth and dynamic range in applications such as wireline and wireless communications, medical imaging and high-definition video processing. Several communication systems and multi-channel applications, such as digital FM and LTE-advanced, need medium resolution ADCs with bandwidths in the tens of MHz range. Table 1.1 lists the requirements of ADC in receivers for various mobile communication. To achieve high data rates, these applications rely on advanced digital modulation techniques that can be advantageously implemented in nanometer-CMOS, which motivates the development of suitable ADCs in these technologies. This combination of resolution and bandwidth were considered the exclusive forte of pipelined ADCs. Delta-Sigma modulators (DSMs) are now being seen as attractive alternatives to pipelined converters in such applications.

1.2 Design Challenges

The noise-shaping function of a DSM can effectively suppress quantization noise when it is operated with oversampling, thus a DSM can achieve higher dynamic range than other ADC types. Oversampling ADCs that use DSMs require faster analog circuits

Specification	Standard	Bandwidth (MHz)	Dynamic range (bits)
WCDMA	3G Telecom	3.84,4	9-12
HSDPA	3.5G Telecom	5	9-13
Zigbee	IEEE 802.15	5	12
HipeLAN	European IEEE 802.11	6	14
Wifi	IEEE 802.11, WLAN	11,20,22	8-14
WiMax	IEEE 802.16, WMAN	5,10,20	7-11
LTE	3.9G Telecom	5,10,20	10-13
LTE-advanced	4G Telecom	20	12

Table 1.1: Baseband requirements of ADCs for various wireless standards.

than Nyquist-rate ADCs. Consider a discrete-time (DT) DSM that comprises a cascade of switched-capacitor (SC) integrators. Each integrator contains an opamp. The open-loop unity-gain frequency and slew rate of the opamp determine the speed of the integrator, while the dc voltage gain of the opamp dictates the quality of the integration function. Meanwhile, the integrator transfer function is also more sensitive to process-voltage-temperature (PVT) variations. An SC integrator realized with a low-gain opamp is lossy, meaning that it exhibits integrator-leakage. If the integrators in a DSM are lossy, then the noise-shaping capability of the DSM is weakened, degrading the signal-to-quantization-noise ratio (SQNR).

As CMOS technologies advance, MOSFETs become smaller and faster, but their intrinsic voltage gain, g_m/g_{ds}, also decreases. [1]. Consider a standard 32 nm CMOS. A minimum-channel-length MOSFET has a maximum transit frequency ,f_T, of over 400 GHz but it has an intrinsic gain g_m/g_{ds} of only about six [2, 3].

Although some circuit level techniques have been proposed to raise the dc gain of opamps, such as multi-stage amplifiers [4], gain-compensated integrators [5,6], correlated double sampling [7, 8], and correlated level shifting [9]. These existing solutions can restore SNQR of DSMs, but may be inappropriate in deep-submicron technology since low intrinsic gain and limited supply headroom. Moreover, all sacrifice the speed.

The performance of a wide-band DT DSM is usually limited by its internal opamps that realize the integrator function. For an input bandwidth of 20 MHz and an over-sampling ratio (OSR) of 32, the corresponding sampling rate is $f_s = 1.28$ GHz, and the

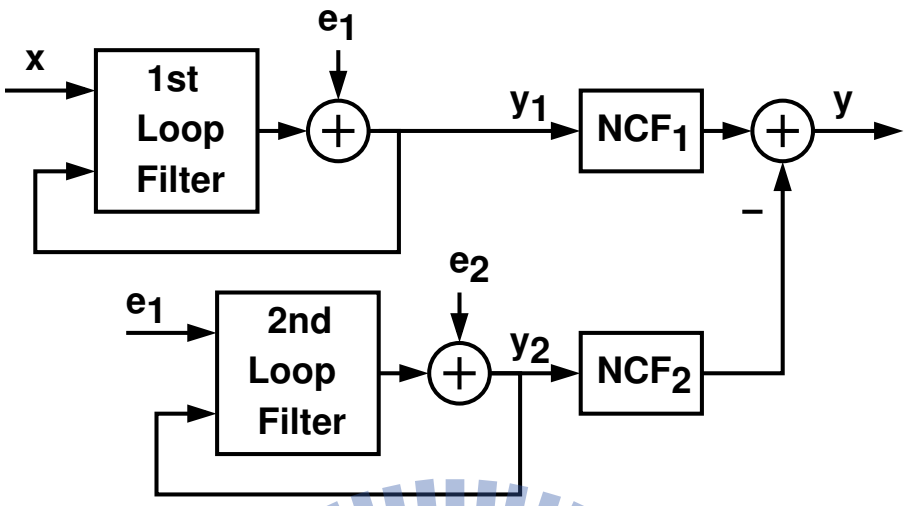


Figure 1.1: Traditional dual-stage $\Delta\Sigma$ modulator structure.

required opamp unity-gain frequency is about $5f_s = 6.4$ GHz. It is difficult for an opamp with such a speed to have a decent dc gain.

There are calibration techniques that can improve the frequency accuracy of the noise-shaping functions of the DSMs [10–13]. They all assume that the opamps have sufficiently large dc gain. There are DSM calibration techniques that try to correct the errors caused by non-ideal integrators that exhibit integration leakage as well as distortion [14, 15]. However, the required processing circuits are cumbersome.

The accuracy requirement for the SC integrators can be relaxed by increasing the order of the DSM loop, or by employing the multi-stage noise-shaping (MASH) structure [16–19]. A higher-order DSM may require more quantization levels from its internal analog-to-digital converter (ADC) and digital-to-analog (DAC) to stabilize the loop [20], yielding complex circuits. Thus a cascaded DSM which can avoid stability problem is relatively attractive.

A conventional dual-stage cascaded DSM is shown in Figure 1.1. There are two DSMs followed by the responsing noise cancellation filter (NCF). Idealistically, NCFs eliminate the first stage quantization noise completely, and shape the second stage quantization noise once more. However, the mismatch between analog loop filter and digital cancellation filter is unavoidable. This leads the first stage quantization noise leaks into the signal bandwidth and degrades the overall SQNR of DSM. Too often, the quantization noise

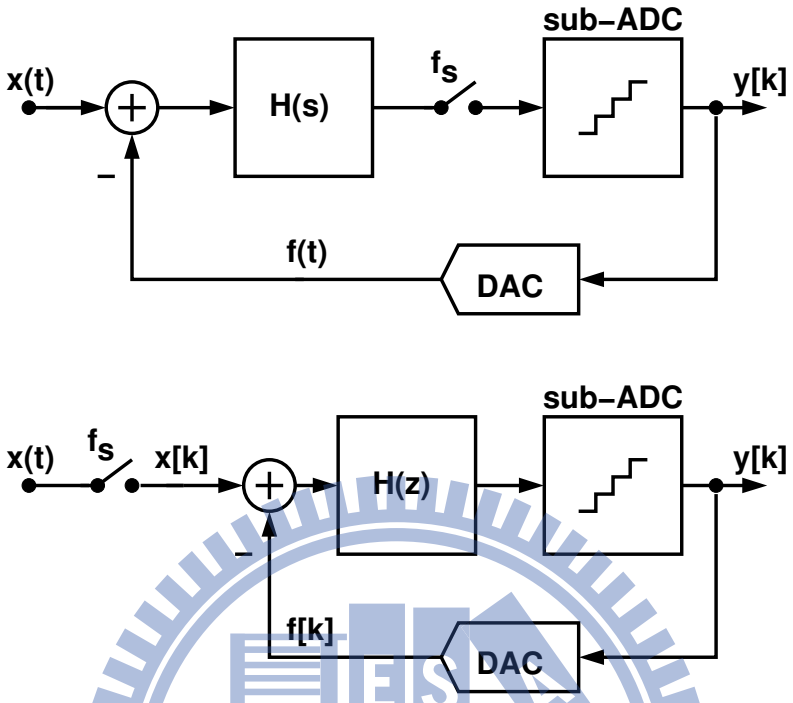


Figure 1.2: Continuous-time $\Delta\Sigma$ modulator and discrete-time $\Delta\Sigma$ modulator.

leakage is the major cause in the drop of DSM performance. This undesired effect typically requires high accuracy analog components to lessen. Circuit level techniques used to enhance the accuracy of SC integrators can also be applied to improve qualities of analog loop filter. Similarly, all lead analog loop filters of slow speed and large power consumption. Thus the feasibility of cascaded DSMs with the advanced CMOS technologies is limited.

There is an alternative cascaded DSM structure, sturdy MASH [21], can mitigate the matching requirements [21]. Although the demand on DAC performance gets more pressing. Using the adaptive NCF to alleviate the noise leakage in background are developed [22, 23]. However, it is difficult to obtain the required parameters from the DSM digital output alone.

Comparing to DT DSMs, the continuous-time (CT) DSMs can use opamps of less speed [24–29]. However, the time constant of a CT integrator is not as robust as that of a DT integrator. This disadvantage will become even more pronounced as technology will scale further [30]. Time-constant calibration is required in most CT DSM designs. In

addition, the excess loop delay in a CT DSM requires compensation to avoid instability or the degradation of the in-band noise suppression. This compensation needs to cover the PVT variations. The internal DACs in the CT DSMs are crucial. In additional to the static conversion errors, the jitter and dynamic distortion of those DACs also degrade the DSM performance. More quantization levels for the DAC may be needed. Those DACs may require calibration [29]. The CT DSMs are more sensitive to the clock jitter, especially when the OSR is low [31].

1.3 Contributions

To take advantage of advanced nano-scale CMOS technologies, this thesis proposes the use of opamps with a simple circuit configuration and minimum-length MOSFETs. The resulting SC integrators are high-speed and low-power but they are also lossy. A background calibration is then carried out to compensate for the integration leakage of the integrator and recover the noise-shaping capability of the DSM.

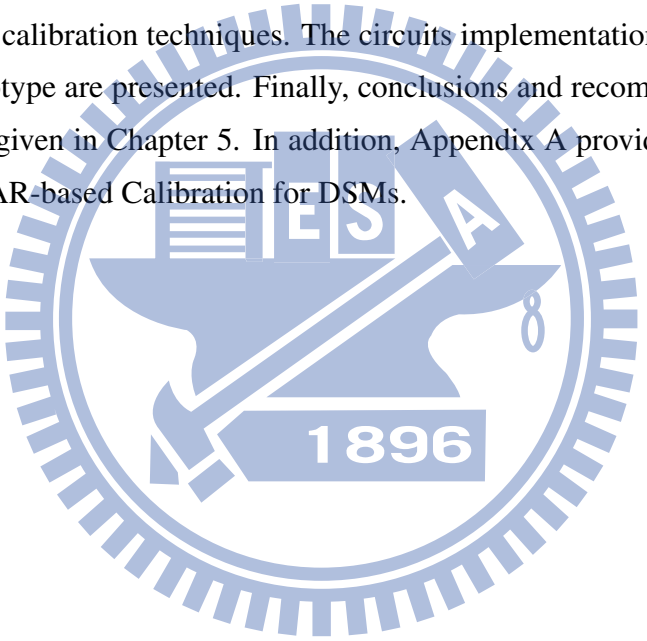
Moreover, to achieve wide bandwidth and large dynamic range for a cascaded DSM, this thesis proposes the use of combing low-complexity circuits and digital calibrations. The resulting analog loop filters are high-speed and low-power but also inaccurate. Two different types of digital calibrations are applied. We first employ the integrator leakage calibration to correct the poles of the integrators. We then use the noise leakage calibration to minimize the quantization noise from the first loop leaking to the DSM combined output. As a result, the cascaded DSM preforms higher-order noise shaping and SQNR is restored. And the noise leakage calibration can relaxe the component matching requirements of the cascaded DSMs.

Since each calibration adjusts only one parameter, it is robust. All calibrations can proceed in the background without interrupting the normal DSM operation. The calibration processors are simple digital circuits. They do not include any complex filter. A 2-2 cascaded DSM was fabricated using a 65 nm CMOS technology to verify our scheme. It has a sampling rate of 1.1 GHz and an input bandwidth of 16.67 MHz with an oversampling ratio (OSR) of 33. The measured signal-to-noise-and-distortion ratio (SNDR) and dynamic range (DR) are 74.32 dB and 81 dB respectively. The chip consumes 94 mW

from a 1 V supply.

1.4 Organization

This thesis is organized as follows. Chapter 2 discusses the integration leakage of DSMs, and introduces the integrator leakage calibration. Various design cases and its design consideration are included. Chapter 3 discusses the noise leakage of cascaded DSMs, and introduces the noise leakage calibration. A 2-2 cascaded DSM are instantiated for demonstration. Chapter 4 illustrates a 81 dB dynamic range 16.67MHz bandwidth DSM using the proposed calibration techniques. The circuits implementation and experimental results of this prototype are presented. Finally, conclusions and recommendations for future works will be given in Chapter 5. In addition, Appendix A provides a mathematical treatment of the AAR-based Calibration for DSMs.



Chapter 2

Integrator Leakage Calibration for DSMs

Switched-capacitor (SC) integrators realized with low-gain opamps are lossy. Lossy integrators in a delta-sigma modulator (DSM) degrade the signal-to-quantization-noise ratio (SQNR) of the DSM. In this chapter, we propose an integration-leakage calibration technique for the integrators in a SC DSM. To calibrate an integrator, its integration leakage is detected in the digital domain, while the leakage compensation is added to the same integrator in the analog domain. The leakage compensation signal path adds little noise and loading to the original integrator. To detect the integration leakage of an integrator, an out-of-band square wave is injected into the DSM, which can be easily removed by the decimation filter following the DSM. The integration-leakage detector is a simple digital circuit that performs the accumulation-and-reset (AAR) operation. The proposed scheme can calibrate all integrators in a DSM of any form. It calibrates one integrator at a time. It can proceed in the background without interrupting the normal DSM operation. Once all integrators are calibrated, the noise-shaping capability of the DSM is recovered, and the SQNR performance of the DSM is restored. Since each integrator is calibrated separately, the design parameters of the corresponding calibration signal and calibration processor (CP) can be easily optimized.

The rest of this paper is organized as follows. Section 2.1 discusses the effect of integration leakage on the SQNR performance of DSMs. Section 2.2 introduces the SC

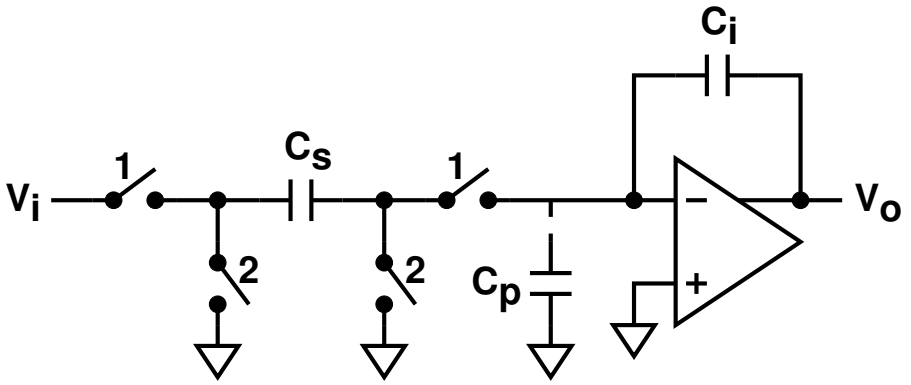


Figure 2.1: A conventional switched-capacitor (SC) integrator.

integrators with leakage compensation. Section 2.3 introduces the proposed calibration technique with a 1st-order DSM design case. Design considerations are outlined. Section 2.4 applies the calibration technique to a 2nd-order DSM design case. Section 2.5 applied the techniques to high-order DSMs. A 3rd-order DSM design case is demonstrated. Finally, Section 2.6 draws conclusions. In addition, the stochastic analysis of the calibration algorithm is addressed in Chapter A.

2.1 Integration Leakage and Its Effect

Consider a conventional SC integrator shown in Figure 2.1. Its z-domain transfer function is

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{\alpha}{1 - \beta z^{-1}} \tag{2.1}$$

with

$$\alpha = \frac{-\frac{C_s}{C_i}}{1 + \frac{1}{A_0} \cdot \frac{C_i + C_s + C_p}{C_i}} \qquad \beta = \frac{1 + \frac{1}{A_0} \cdot \frac{C_i + C_p}{C_i}}{1 + \frac{1}{A_0} \cdot \frac{C_i + C_s + C_p}{C_i}} \tag{2.2}$$

where A_0 is the dc voltage gain of the opamp and C_p is the total parasitic capacitance associated with the negative terminal of the opamp. If the opamp is ideal with $A_0 = \infty$, then $\alpha = -C_s/C_i$ and $\beta = 1$. Figure 2.2 illustrates the integrator time-domain output response, in which $V_i[k] = 0$ for $k > 0$. If $\beta = 1$, then $V_o[k]$ maintains its $V_o[0]$ value for

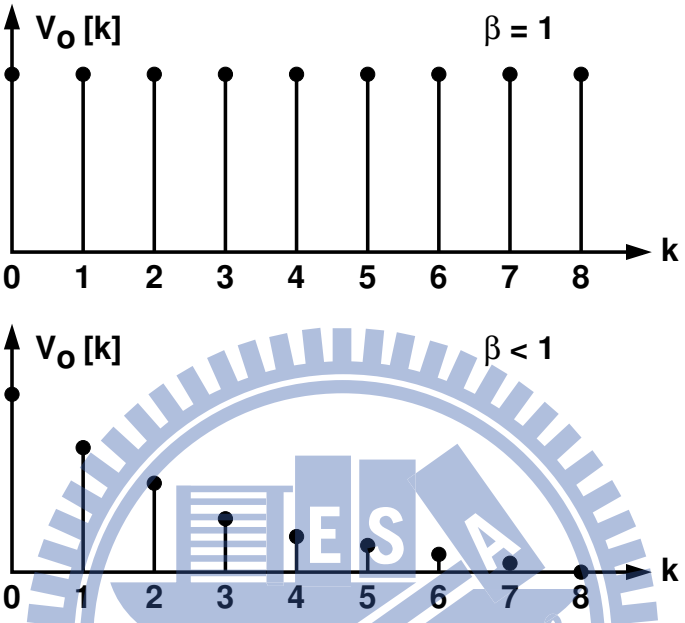


Figure 2.2: Integrator time-domain output response. $V_i[k] = 0$ for $k > 0$.

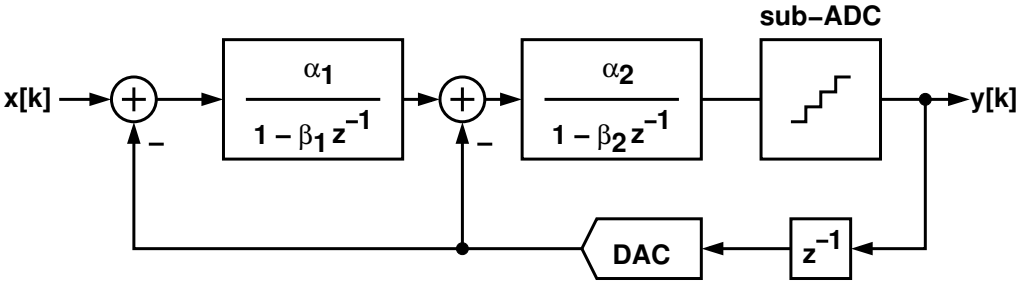


Figure 2.3: A delta-sigma modulator with lossy integrators.

$k > 0$. If $\beta < 1$, then the charge on capacitor C_i leaks and $V_o[k]$ decreases as k progresses. An integrator with $\beta < 1$ is an lossy integrator.

Figure 2.3 shows a delta-sigma modulator (DSM) that employs the lossy integrators. Although the coefficient α for the integrator of Figure 2.1 is negative, the coefficients α_1 and α_2 in Figure 2.3 are positive for simplicity. Their polarities can be easily changed in a fully differential circuit configuration. Assume the digital-to-analog converter (DAC) is ideal. The difference between the sampled analog input $x[k]$ and DAC output is integrated by two lossy integrators and then quantized by a sub-ADC. The sub-ADC introduces quantization errors, $e[k]$. The sub-ADC digital output $y[k]$ can be expressed as

$$Y(z) = \mathrm{STF}(z) \cdot X(z) + \mathrm{NTF}(z) \cdot E(z) \tag{2.3}$$

where $\mathrm{STF}(z)$ is the signal transfer function and $\mathrm{NTF}(z)$ is the noise transfer function. They are

$$\mathrm{STF}(z) = \frac{\alpha_1 \alpha_2}{D(z)} \qquad \mathrm{NTF}(z) = \frac{\left(1 - \beta_1 z^{-1}\right)\left(1 - \beta_2 z^{-1}\right)}{D(z)} \tag{2.4}$$

where

$$D(z) = 1 + \left(\alpha_1 \alpha_2 + \alpha_2 - \beta_1 - \beta_2\right) z^{-1} + \beta_1 \left(\beta_2 - \alpha_2\right) z^{-2} \tag{2.5}$$

If the integrators are lossy, i.e., $\beta_1 < 1$ and $\beta_2 < 1$, then the zeros of the NTF deviate from the unit circle in the z-plane, diminishing the the DSM's ability of suppressing the sub-ADC quantization errors.

Consider a M-th order DSM with M lossy integrators. Its NTF is expressed as

$$\mathrm{NTF} = \left(1 - \beta z^{-1}\right)^M \tag{2.6}$$

The β coefficients are assumed to be identical for simplicity. If the sub-ADC in the DSM has B-bit resolution, then the DSM's maximum signal-to-quantization-noise ratio (SQNR) is

$$\mathrm{SQNR(dB)} = 1.76 + 6.02 \times B + \mathrm{SQNR}_{\mathrm{NTF}} \tag{2.7}$$

$\mathrm{SQNR}_{\mathrm{NTF}}$ is the SQNR enhancement by the NTF.

To derives the SQNR enhancement, SQNR_{NTF} of (2.7). Let $\omega = 2\pi f/f_s$ be the normalized angular frequency, where f_s is the sampling frequency. If the input bandwidth is f_B, then the normalized input bandwidth is $\omega_b = 2\pi f_B/f_s = \pi/\text{OSR}$, where $\text{OSR} = f_s/(2f_B)$ is the oversampling ratio. Assume the noise shaping function of a M-th-order DSM is $\text{NTF}(z) = \left(1-\beta z^{-1}\right)^M$. All zeros deviate from 1 to β. Assume the quantization noise introduced by the sub-ADC is white and has a total power of P_e. The total in-band noise power after noise shaping is

$$P_{e,sh} = \frac{P_e}{2\pi}\int_{-\omega_b}^{+\omega_b} \left|\text{NTF}(e^{j\omega})\right|^2 d\omega \tag{2.8}$$

If $\text{OSR} \gg \pi$, then, for $|\omega| < \omega_b$, $\cos(\omega) \approx 1-\omega^2/2$. Using the binomial theorem [32], we have

$$\begin{aligned}\left|\text{NTF}(e^{j\omega})\right|^2 &= \left[1+\beta^2-2\beta\cos(\omega)\right]^M \\ &\approx \left[(1-\beta)^2+\beta\omega^2\right]^M \\ &\approx \sum_{n=0}^{M}\frac{M!}{n!(M-n)!}(1-\beta)^{2n}\beta^{M-n}\cdot\omega^{2M-2n}\end{aligned} \tag{2.9}$$

and

$$\begin{aligned}&\int_{-\omega_b}^{+\omega_b}\left|\text{NTF}(e^{j\omega})\right|^2 d\omega \\ &= \sum_{n=0}^{M}\frac{M!}{n!(M-n)!}(1-\beta)^{2n}\beta^{M-n}\frac{\omega^{2M-2n+1}}{2M-2n+1} \\ &= \frac{\omega^{2M+1}}{2M+1}\sum_{n=0}^{M}\frac{M!}{n!(M-n)!}\left(\frac{1-\beta}{\omega}\right)^{2n}\beta^{M-n}\frac{2M+1}{2M-2n+1}\end{aligned} \tag{2.10}$$

From (2.8) and (2.10), the SQNR enhancement by the NTF is

$$\text{SQNR}_{\text{NTF}} = \frac{P_e}{P_{e,sh}} = \frac{2M+1}{\theta\cdot\pi^{2M}}\times\text{OSR}^{2M+1} \tag{2.11}$$

where

$$\theta = \sum_{n=0}^{M}\frac{M!}{n!(M-n)!}\frac{(2M+1)\beta^{M-n}}{2M-2n+1}\left[\frac{\text{OSR}(1-\beta)}{\pi}\right]^{2n} \tag{2.12}$$

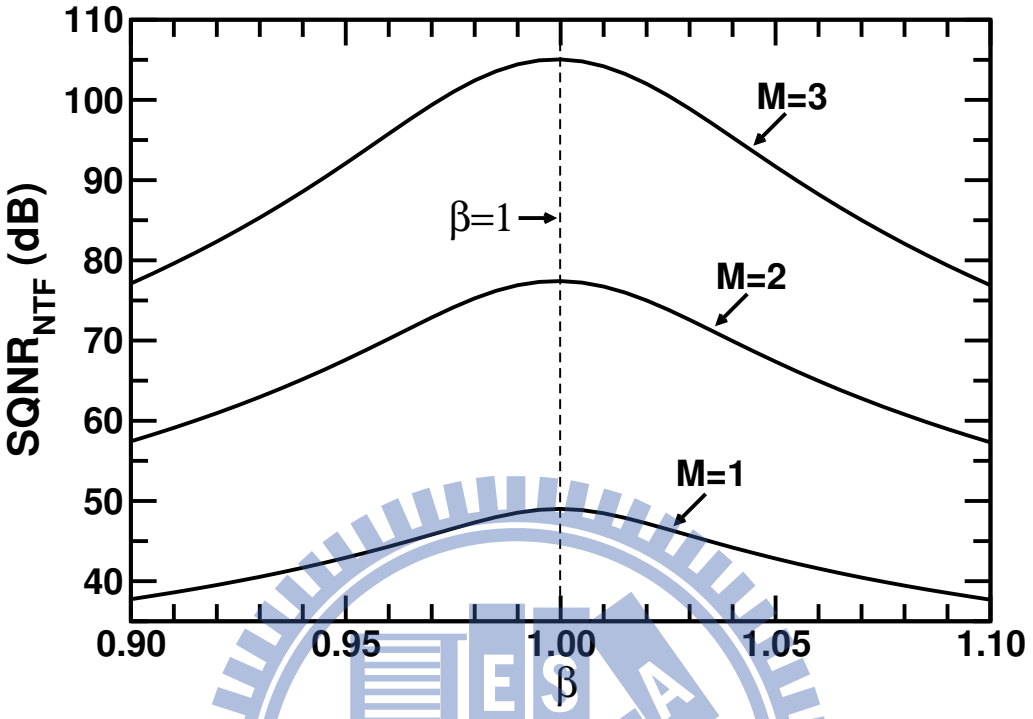


Figure 2.4: DSM SQNR enhancement versus β. OSR = 64. For a 1st-order DSM, $M = 1$. For a 2nd-order DSM, $M = 2$. For a 3rd-order DSM, $M = 3$.

Expressing (2.11) in decibel scale leads to (2.7). Reference to (2.12), in which θ is the ratio of in-band noise power with NTF $= \left(1 - z^{-1}\right)^M$ to the in-band noise power with NTF $= \left(1 - \beta z^{-1}\right)^M$. If $\beta = 1$, then $\theta = 1$. If $\beta \neq 1$, then $\theta > 1$ and SQNR_{NTF} decreases.

If $\beta = 1$, each term of (2.12) is zero except $n = 0$, then $\theta = 1$. If $\beta \neq 1$, then $\theta > 1$, yielding larger in-band quantization noise power.

Figure 2.4 shows the effects of β on SQNR_{NTF} when OSR = 64. Consider an ideal 3rd-order DSM with $\beta = 1$. It can offer a SQNR_{NTF} of 105 dB. However, if $\beta = 0.9$, the resulting SQNR_{NTF} is degraded to 77 dB. Figure 2.5 shows the effects of β on SQNR_{NTF} when OSR increases. For an ideal M-order DSM, the SQNR_{NTF} is improved by $6M+3$ dB when the OSR is doubled. If $\beta < 1$, then it becomes less effective for the DSM to improve SQNR_{NTF} by increasing OSR. Although above conclusions are established on assuming that all NTF's zeros are localed at β for simplicity, similar results are obtained even NTF's zeros are separated.

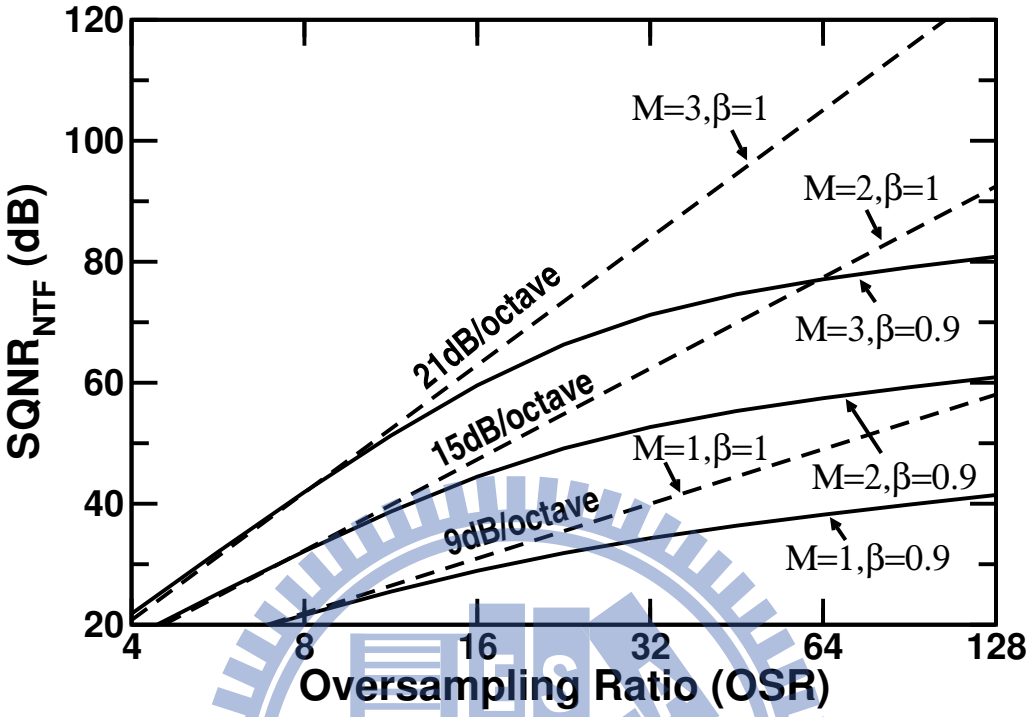


Figure 2.5: DSM SQNR enhancement versus oversampling ratio (OSR).

2.2 Integrator with Leakage Compensation

Consider the integrator shown in Figure 2.1 and its time-domain output response shown in Figure 2.2. If $\beta < 1$ for the integrator, its output loses an amount of $\Delta V_o = (1-\beta)V_o[k-1]$, as clock progresses from cycle $k-1$ to cycle k. The integrator is lossy and exhibits integration leakage. Figure 2.6 shows the proposed SC integrator to compensate this leakage. The capacitor C_f is added to sample V_o. The sampled V_0 is added to the integrator in the next clock cycle. If C_f has the right capacitance, the integrator becomes lossless. Similar integrator can be found in [33], which is used to reduce idle-channel tones.

The z-domain transfer function of the proposed integrator is (2.1) with

$$\beta = \frac{1 + \frac{C_f}{C_i} + \frac{1}{A_0}\frac{C_i+C_p}{C_i}}{1 + \frac{1}{A_0}\frac{C_i+C_s+C_f+C_p}{C_i}} \tag{2.13}$$

The proposed integrator requires a correct C_f to make $\beta = 1$. Regardless of C_p, to make

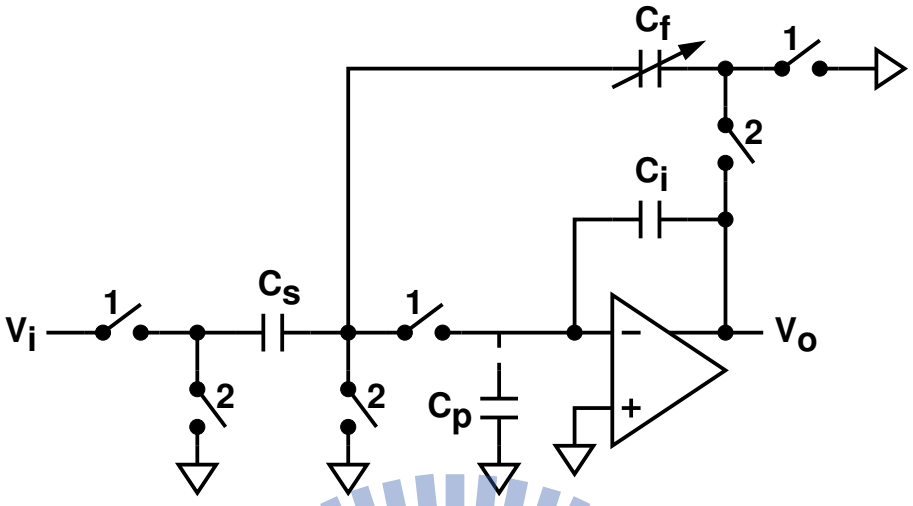


Figure 2.6: Proposed switched-capacitor (SC) integrator with leakage compensation.

$\beta = 1$, we want

$$C_f = \frac{C_s}{A_0 - 1} \tag{2.14}$$

Comparing to C_s, C_f is relatively small. The C_f capacitor itself and its associated switches add minuscule loading and noise to the integrator.

Figure 2.7 shows the proposed non-inverting SC integrator with integration leakage compensation. Its β can also be expressed as (2.13).

Both the integrators of Figure 2.6 and Figure 2.7 require constant calibration to adjust C_f against process-voltage-temperature (PVT) variations. In our proposed scheme, C_f is controlled by a digital signal $T[k] \in \{0, \pm 1, \pm 2, \cdots\}$, such that

$$C_f = C_{f0} + \Delta C_f \times T[k] \tag{2.15}$$

where ΔC_f is the C_f digital control step size and C_{f0} is the C_f capacitance when $T[k] = 0$. The corresponding β is

$$\beta = \beta_0 + \Delta\beta \times T[k] \tag{2.16}$$

where

$$\Delta\beta \approx \frac{1 + \frac{1}{A_0}\frac{C_s + C_p}{C_i}}{1 + \frac{2}{A_0}\frac{C_i + C_s + C_{f0} + C_p}{C_i}} \times \frac{\Delta C_f}{C_i} \tag{2.17}$$

In our calibration scheme, $\Delta\beta$ determines how close the β can be adjusted to approach 1. Referring to Figure 2.4, smaller $\Delta\beta$ makes β closer to 1, resulting in better SQNR_{NTF}.

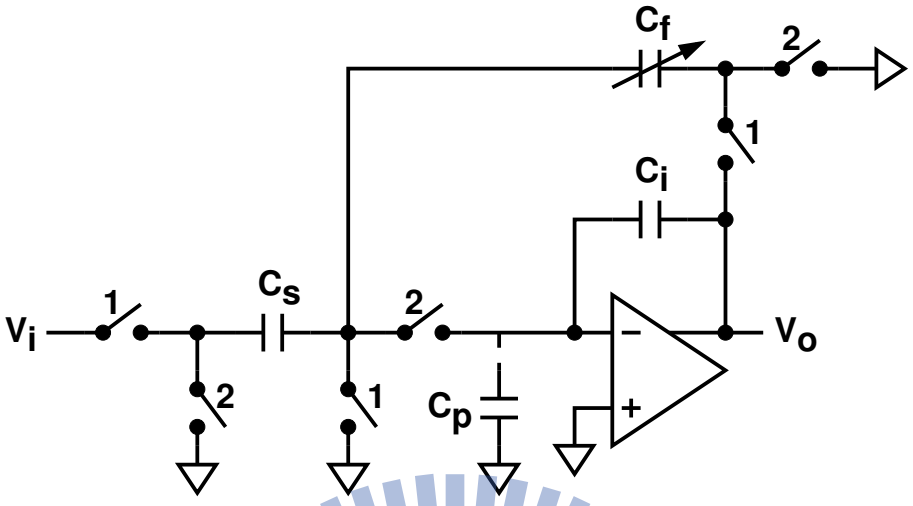


Figure 2.7: Proposed non-inverting switched-capacitor (SC) integrator with leakage compensation.

2.3 First-Order DSM Design Case

Figure 2.8 shows a 1st-order DSM using the integrator of Figure 2.6. The integrator's transfer function is expressed as (2.1). Although the integrator shown in Figure 2.6 has a negative α coefficient. The α coefficient in Figure 2.8 is positive. If $C_s = C_i$ and $A_0 = 8$, then $\alpha = 0.8$ and $\beta = 0.9$. This DSM includes a background calibration mechanism that automatically adjusts the C_f capacitor in the integrator to maximize SQNR.

In Figure 2.8, the sub-DAC has N levels and covers an output range of ± 1. The least-significant-bit (LSB) size is

$$\Delta = \frac{2}{N-1} \tag{2.18}$$

The DSM output is $y[k]$. If N is odd, $y[k]$ has its value among $\{0, \pm 1, \pm 2, \cdots, \pm(N-1)/2\}$. If N is even, $y[k]$ has its value among $\{\pm 0.5, \pm 1.5, \cdots, \pm(N/2 - 0.5)\}$, The DAC output is $V_{da}[k] = \Delta \times y[k-1]$. We assume the sub-ADC is a flash ADC, whose input thresholds correspond to the middle of adjacent DAC outputs. There are $N-1$ sub-ADC thresholds. The sub-ADC LSB size is the same as (2.18). If the sub-ADC is ideal, its input range is $\pm(1 + \Delta/2)$. The quantization errors $e[k]$ introduced by the sub-ADC have values between $-\Delta/2$ and $+\Delta/2$. The transfer curve of sub-ADC and sub-DAC are sketch in Figure 2.9.

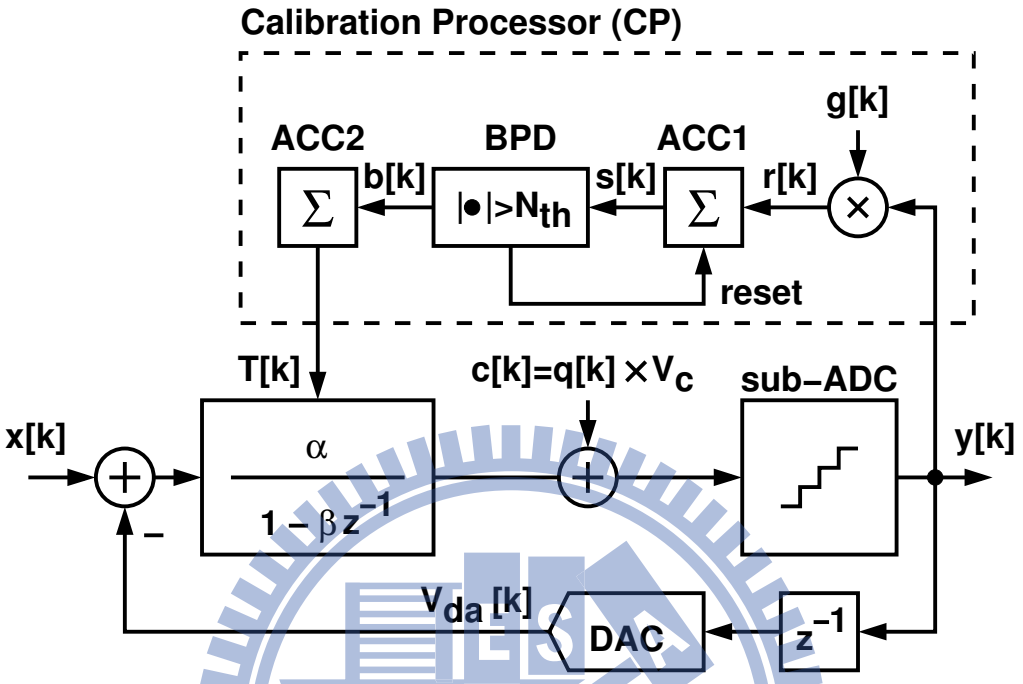


Figure 2.8: A 1st-order DSM with the proposed calibration scheme.

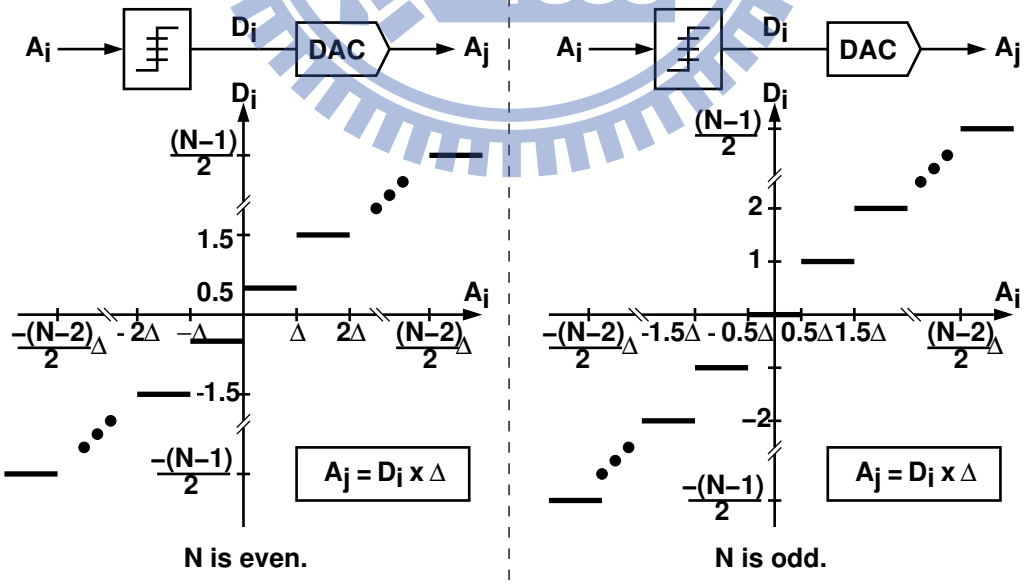


Figure 2.9: Transfer curve of sub-ADC and sub-DAC.

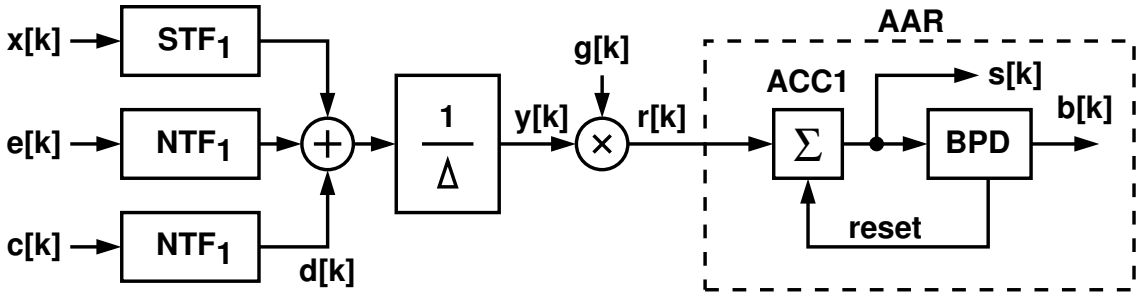


Figure 2.10: Calibration signal flow diagram.

The DSM has a sampling rate of f_s and a signal bandwidth of f_B. Its over-sampling ratio is OSR $= f_s/(2f_B)$. The modulator digital output $y[k]$ is

$$\Delta \times Y(z) = \mathrm{STF}_1(z) \cdot X(z) + \mathrm{NTF}_1(z) \cdot E(z) \tag{2.19}$$

where

$$\mathrm{STF}_1(z) = \frac{H(z)}{1 + z^{-1}H(z)} \quad \mathrm{NTF}_1(z) = \frac{1}{1 + z^{-1}H(z)} \tag{2.20}$$

and $H(z)$ is the transfer function of the integrator expressed in (2.1). As proposed in Section 2.2, the β of the integrator is adjustable. It is adjusted automatically by the calibration processor (CP) shown in Figure 2.8. To facilitate calibration, a periodic square wave $c[k] = q[k] \times V_c$ is added to the sub-ADC input. The CP detects the calibrating signal embedded in $y[k]$, generates a control signal $T[k]$, and adjusts β to approximate β to 1.

Figure 2.10 shows a signal flow diagram of the calibration. The modulator input $x[k]$ and sub-ADC quantization errors $e[k]$ are shaped by STF_1 and NTF_1 respectively. The calibrating signal $c[k]$ is shaped by NTF_1, yielding $d[k]$. The summation of the above three signals is converted to $y[k]$ with a conversion gain of $1/\Delta$. The calibrating signal $c[k]$ is expressed as a periodic binary square wave $q[k] \in \{-1, +1\}$ multiplied by an amplitude of V_c. Thus, embedded in $y[k]$, $d[k]$ is the step response of NTF_1 triggered by $c[k]$. Figure 2.11 shows the $d[k]$ waveform. The step response has an initial value of

$$V_{ci} = V_c \times \frac{2\alpha + 1 - \beta}{\alpha + 1 - \beta} \tag{2.21}$$

It settles toward a final value of

$$V_{cf} = V_c \times \frac{1 - \beta}{\alpha + 1 - \beta} \tag{2.22}$$

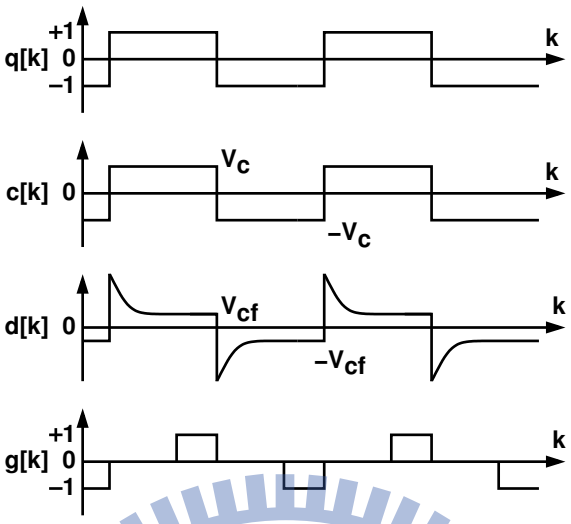


Figure 2.11: Calibration signal waveforms.

Since V_{cf} is proportional to $1-\beta$, it is used to detect β.

Figure 2.10 also shows the CP operation. The CP correlates the DSM output $y[k]$ with a triple-valued sequence $g[k] \in \{-1, 0, +1\}$. The $g[k]$ waveform is illustrated in Figure 2.11. It has the same polarity as $q[k]$, but its value is set to 0 during the initial transition phase of $d[k]$. Thus, the resulting product $r[k]$ contains only the valid V_{cf} information. Following $r[k]$ is an accumulator (ACC1) followed by a binary peak detector (BPD). Together they perform the accumulation-and-reset (AAR) operation [34, 35] to extract V_{cf} from $r[k]$ while removing the perturbations caused by $x[k]$ and $e[k]$. The AAR operation is described as follows. Accumulator ACC1 accumulates the $r[k]$ sequence. Its output $s[k]$ is monitored by a BPD with a threshold $N_{th} > 0$. Whenever $s[k]$ reaches either $+N_{th}$ or $-N_{th}$, the BPD issues an output $b[k] = +1$ or $b[k] = -1$ for one clock cycle respectively and reset $s[k]$ to 0. The BPD output $b[k]$ remains at 0 when no reset occurs. The BPD output $b[k]$ is an estimate of the $1-\beta$ polarity. The CP uses it to adjust the β of the integrator. As shown in Figure 2.8, following $b[k]$ is another accumulator, ACC2, that accumulates the $b[k]$ sequence. Its output $T[k]$ controls the β according to (2.16).

Figure 2.12 illustrates the time-domain waveform of the ACC1 output s, and the waveform of the resulting β. When β approaches 1, both $|1-\beta|$ and V_{cf} become smaller, and it takes a longer time to activate the BPD.

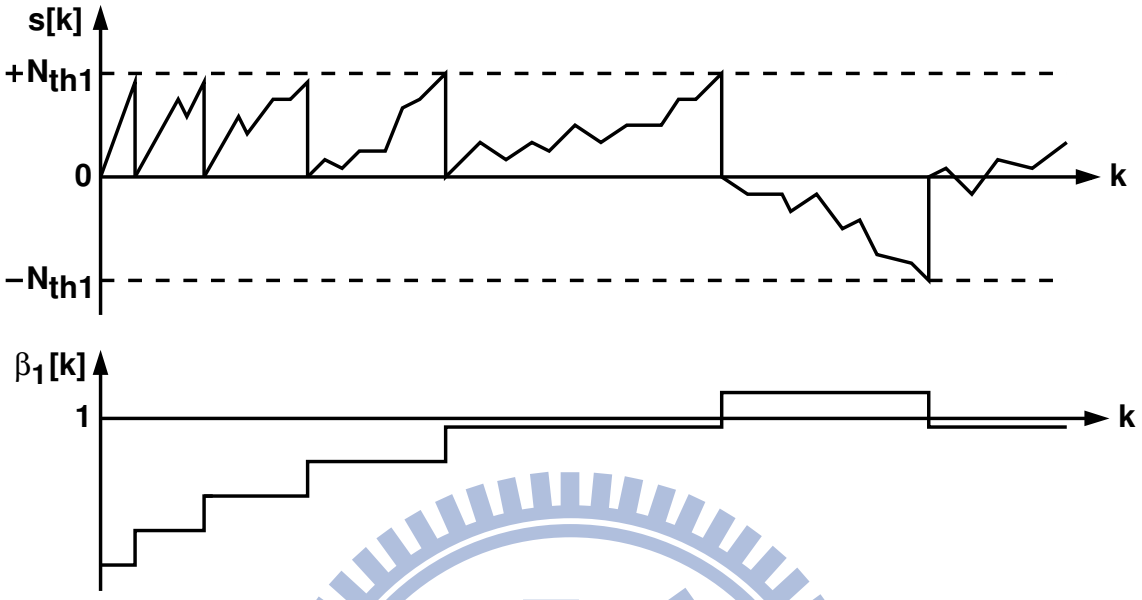


Figure 2.12: Accumulation-and-reset (AAR) operation.

The calibration has five design parameters, including the $c[k]$ amplitude V_c, the $c[k]$ frequency f_q, the $g[k]$ duty ratio D_g, the BPD threshold N_{th}, and the $T[k]$ control step size $\Delta\beta$. Referring to Figure 2.11, the duty ratio D_g is defined as the ratio of the time for $g[k] = +1$ to the time for $q[k] = +1$. The duty ratio for $g[k] = -1$ and $q[k] = -1$ is assumed to be the same as D_g.

In the following subsections, we use the aforementioned 1st-order DSM design case to illustrate the design considerations for the proposed calibration scheme. The DSM block diagram is shown in Figure 2.8. Its sub-ADC and DAC have $N = 16$ quantization steps. The corresponding quantization step size is $\Delta = 2/(N-1)$. It has a sampling frequency of f_s and a corresponding sampling period of $T_s = 1/f_s$. The integrator in Figure 2.8 is realized using the SC integrator of Figure 2.6 with a transfer function of (2.1). If the opamp has a dc gain of $A_0 = 8$, then $\alpha = 0.8$ and $\beta = 0.9$. Assume the DSM is used with an over-sampling ratio of OSR $= 64$. The theoretical maximum SQNR is 74 dB if $A_0 = \infty$. We will apply the proposed calibration to recover SQNR.

2.3.1 Design of $c[k]$ and $g[k]$

As shown in Figure 2.8, the calibration square wave $c[k] = q[k] \times V_c$ is added to the

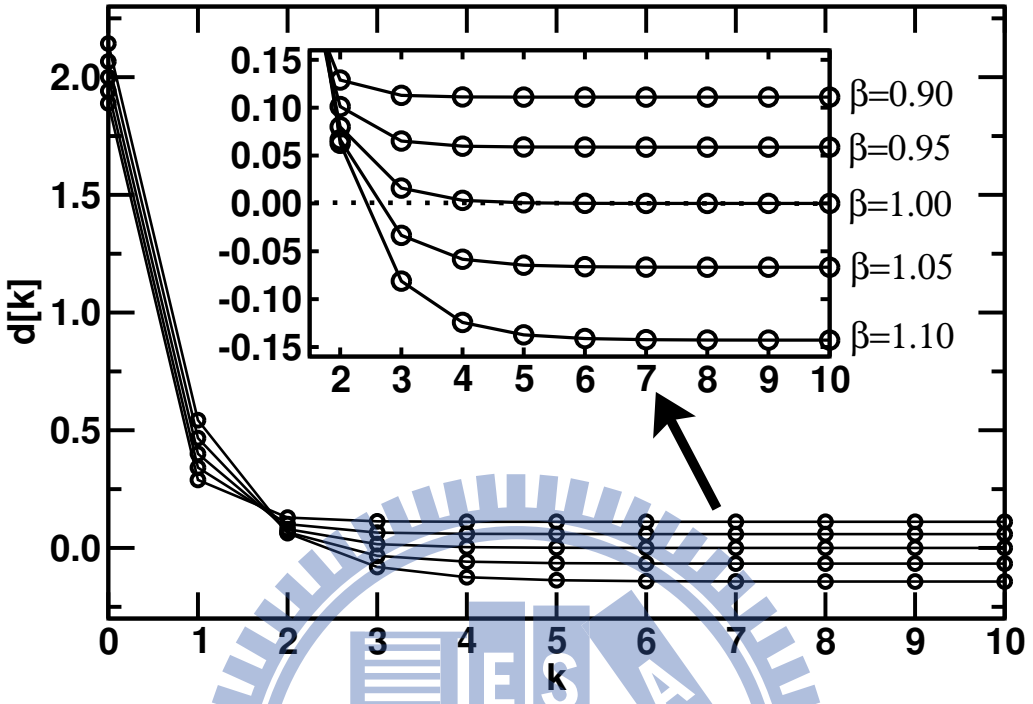


Figure 2.13: The transient response of $d[k]$ with different β.

sub-ADC input. Let $c[k]$ have a frequency of f_q, a corresponding period of $T_q = 1/f_q$, and a duty cycle of 50%. The resulting $d[k]$, as shown in Figure 2.11, is embedded in the sub-ADC output $y[k]$. In each f_q cycle, the transient response of $d[k]$ is a step response of NTF_1 triggered by $c[k]$. It can be expressed as

$$d[k] = V_c \times \frac{2\alpha(\beta-\alpha)^k + (1-\beta)}{\alpha+1-\beta} \tag{2.23}$$

This step response has an initial value of V_{ci} of (2.21) and then settles toward the V_{cf} of (2.22). Figure 2.13 shows several $d[k]$ waveforms with different β. The $d[k]$ waveforms have settled near V_{cf} for $k > 5$. We choose $T_q = 16T_s$ and $D_g = 1/4$, so that, in each $d[k]$ transient, $d[k]$ has a period of 6 clock cycles to settle before $g[k]$ is activated for 2 clock cycles. The frequency of the inject signal $c[k]$ is $f_q = f_s/16$. As long as OSR > 8, the frequency components of $d[k]$ in $y[k]$ is outside the signal band. It can be easily removed by the decimation filter following the DSM.

The injection of the calibration signal $c[k]$ degrades the DSM's maximum SQNR, since $c[k]$ increases the signal range of the signal at the sub-ADC input. The SQNR degradation is a function of the $c[k]$ amplitude V_c. Figure 2.14 shows the simulated SQNR

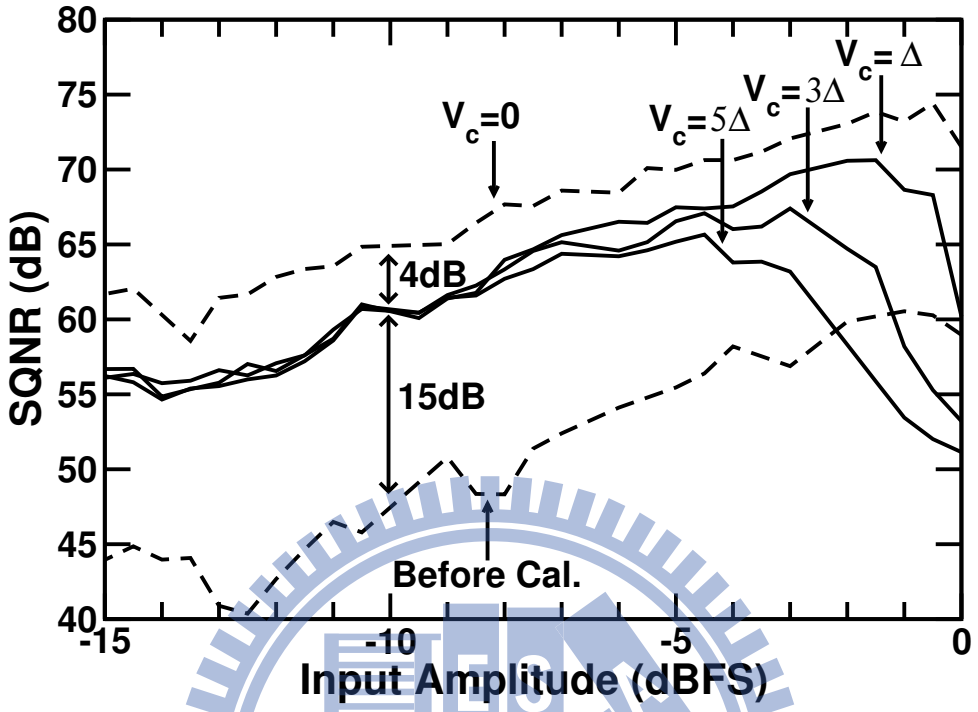


Figure 2.14: SQNR of the 1st-order DSM design case with different V_c. The opamp in the DSM is ideal.

of the DSM design case. Its internal integrator is assumed to be ideal with $\alpha = 1$ and $\beta = 1$. The injected $c[k]$ has a frequency $f_q = f_s/16$. In Figure 2.14, SQNR is plotted against $x[k]$ input amplitude at different V_c. The $x[k]$ frequency is $f_{in} = (41/2^{16})f_s$. If $V_c = 1\Delta = 2/15$, the maximum SQNR is 71 dB at -1.5 dBFS. If $V_c = 3\Delta = 6/15$, the maximum SQNR is 67 dB at -4.5 dBFS. If $V_c = 5\Delta = 10/15$, the maximum SQNR is 66 dB at -4.5 dBFS. In this design example, we choose $V_c = 1\Delta$.

2.3.2 Design of N_{th} and $\Delta\beta$

Figure 2.12 illustrates the transient response of β_1 during the calibration. Consider the DSM shown in Figure 2.8. The averaged variation of $s[k]$ for one clock cycle is $\Delta s = D_g V_{cf}/\Delta$. It takes $N_{th}/\Delta s$ cycles for $s[k]$ to accumulate from 0 to $+N_{th}$ (or $-N_{th}$) so that $T[k]$ is changed by 1 and β is changed by $\Delta\beta$. Thus, we have

$$\frac{d\beta}{dk} = \frac{\Delta\beta}{N_{th}/\Delta s} = \frac{\Delta\beta D_g V_c}{N_{th}\Delta}\frac{1-\beta}{1-\beta+\alpha} \approx \frac{\Delta\beta D_g V_c}{N_{th}\Delta\alpha}(1-\beta) \tag{2.24}$$

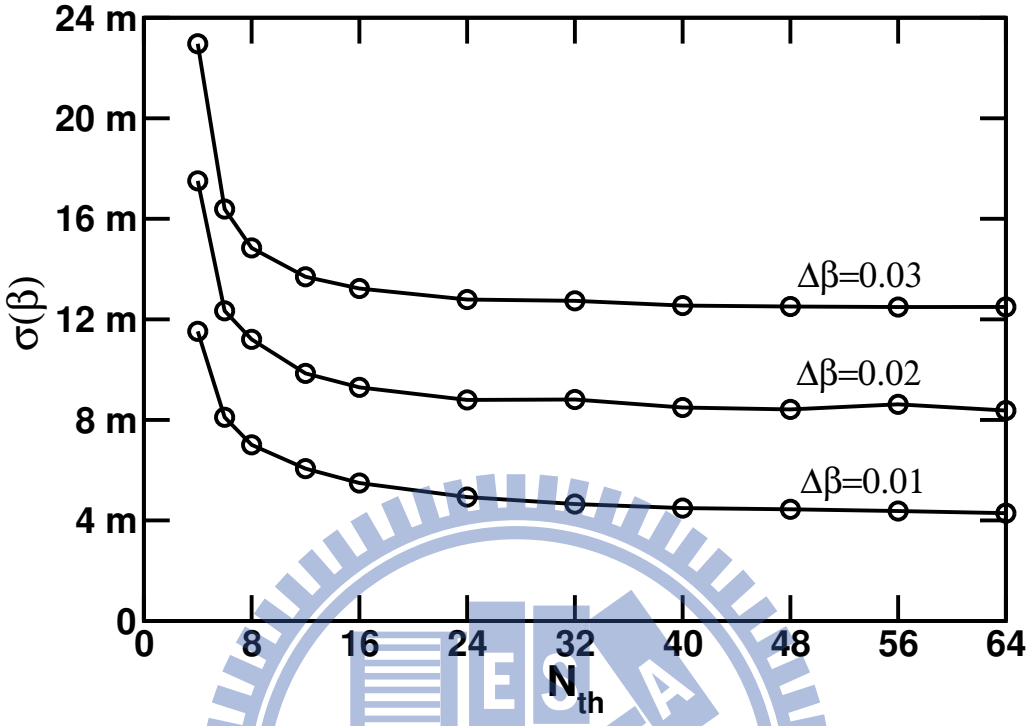


Figure 2.15: $\sigma(\beta)$ versus N_{th} with different $\Delta\beta$.

The calibration loop can be modeled as a single-pole feedback system. The transient response of β can be expressed as

$$\beta[k] = 1 - (1 - \beta[0]) \times e^{-k/\tau} \tag{2.25}$$

The time constant τ is

$$\tau = \frac{N_{th}}{D_g} \cdot \frac{\Delta}{V_c} \cdot \frac{\alpha}{\Delta\beta} \tag{2.26}$$

From (2.26), a smaller N_{th} and a larger $\Delta\beta$ lead to a smaller τ, yielding a faster calibration speed. However, as the calibration process converges, the behavior of $\beta[k]$ becomes a discrete random fluctuation around 1 [34]. Referring to Figure 2.10, both $x[k]$ and $e[k]$ induce this fluctuation. Their effects are diminished by the AAR operation. A larger N_{th} and a smaller $\Delta\beta$ lead to a smaller fluctuation in β, yielding the better SNDR performance for the DSM.

Figure 2.15 shows the standard deviation of the $\beta[k]$ fluctuation from the system simulation of the DSM design case. The standard deviation $\sigma(\beta)$ increases drastically for

$N_{th} < 8$. As N_{th} increases, the standard deviation of β fluctuation, $\sigma(\beta)$, converges to an averaged value.

When the H_1 calibration process converges, the behavior of β_1 becomes a discrete random fluctuation around 1. If $N_{th} = \infty$, β_1 alternates between only two values, which are $\beta_a = 1 - x\Delta\beta$ and $\beta_b = 1 + (1-x)\Delta\beta$, where $0 \le x \le 1$ depending on β_0. Define the probability for $\beta = \beta_a$ as P_a, and the probability for $\beta = \beta_b$ as P_b. Since the expected value of β is 1, i.e., $\beta_a P_a + \beta_b P_b = 1$, we have $P_a = 1 - x$ and $P_b = x$. If x is given, define the standard deviation of β_1 as

$$\sigma(\beta[x]) = \sqrt{(\beta_a - 1)^2 P_a + (\beta_b - 1)^2 P_b} = \Delta\beta\sqrt{x(1-x)} \tag{2.27}$$

If x is uniformly distributed from 0 to 1, the standard deviation of β is

$$\sigma(\beta) = \sqrt{\int_0^1 \sigma(\beta[x])^2 dx} = \frac{\Delta\beta}{\sqrt{6}} = 0.408 \times \Delta\beta \tag{2.28}$$

Chapter A contains a more detail of the above equation.

From Figure 2.4 and seeking the loss of SQNR_{NTF} by less than 1 dB, we want $3\sigma(\beta) < 0.015$, yielding $\Delta\beta < 0.0122$. In this design case, we choose $\Delta\beta = 0.01$ and $N_{th} = 24$.

2.3.3 Simulation Results

This 1st-order DSM design case is verified by using time-domain simulation. Calibration design parameters are $f_q = f_s/16$, $D_g = 0.25$, $V_c = 1\Delta$, $\Delta\beta = 0.01$, and $N_{th} = 24$. The resulting time constant $\tau = 7680$. Figure 2.16 shows the calibration transient response. The solid line is the $\beta[k]$ transient response from simulation and the smooth dashed line is the calculation using (2.25). It takes a calibration time of 3τ for β to converge from 0.9 to 0.995, where the SQNR degradation due to a non-ideal β is less than 1 dB. Assume the DSM input bandwidth is 2 MHz and the sampling frequency is $f_s = 256$ MHz, yielding an oversampling ratio OSR = 64. Then a calibration time of 3τ is 0.09 msec. Figure 2.17 shows the DSM output spectra before and after calibration. The input is a sine wave with a frequency of $(41/2^{16})f_s$ and an amplitude of -2 dBFS. The resulting SQNR is 58 dB before calibration, and is improved to 70 dB after calibration. The frequency components of $c[k]$ are visible in Figure 2.17. They are far away from the signal band.

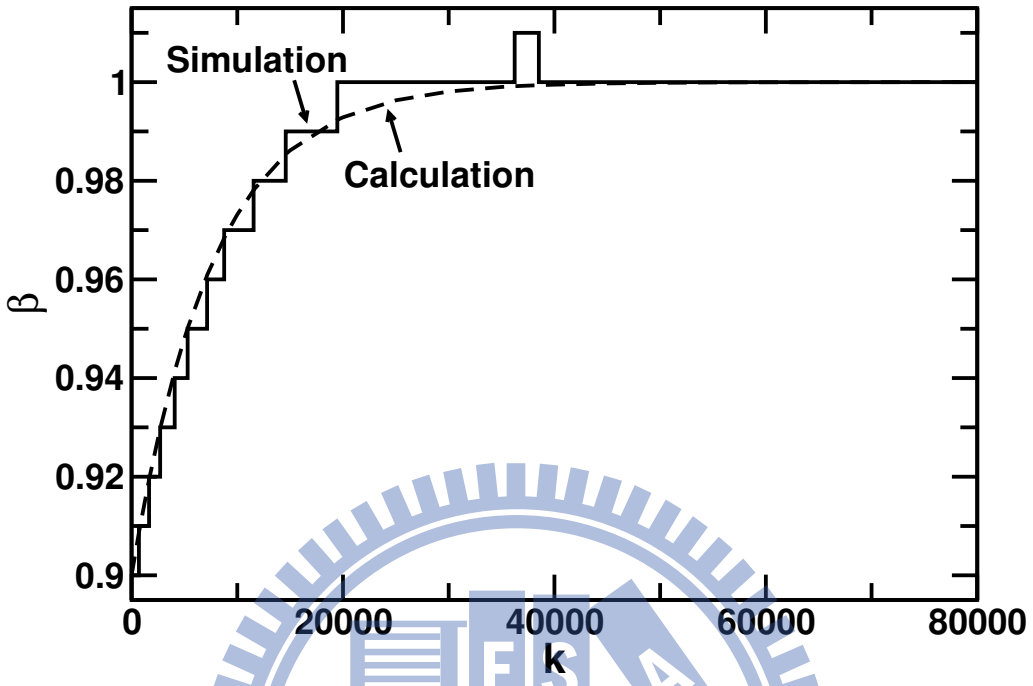


Figure 2.16: $\beta[k]$ transient response of the 1st-order DSM design case.

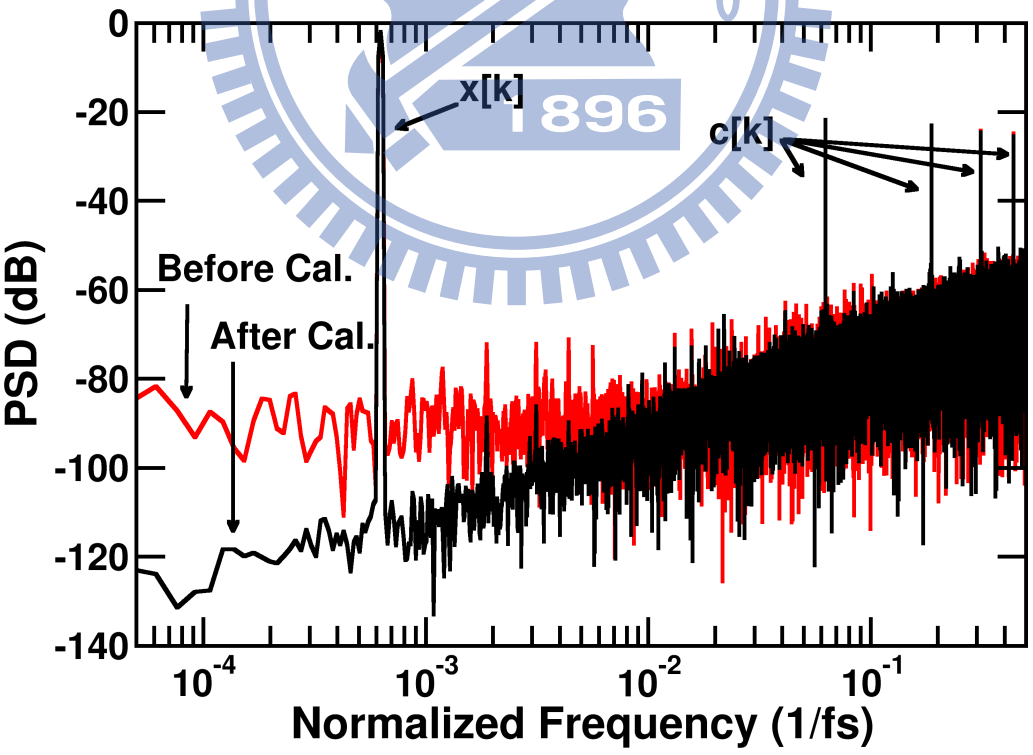


Figure 2.17: Output spectra of the 1st-order DSM design case.

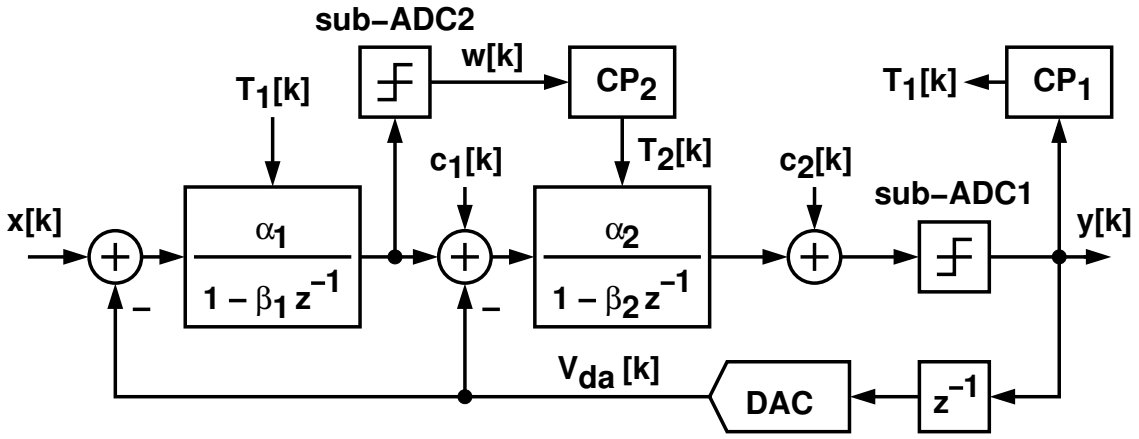


Figure 2.18: A 2nd-order DSM with the proposed calibration scheme.

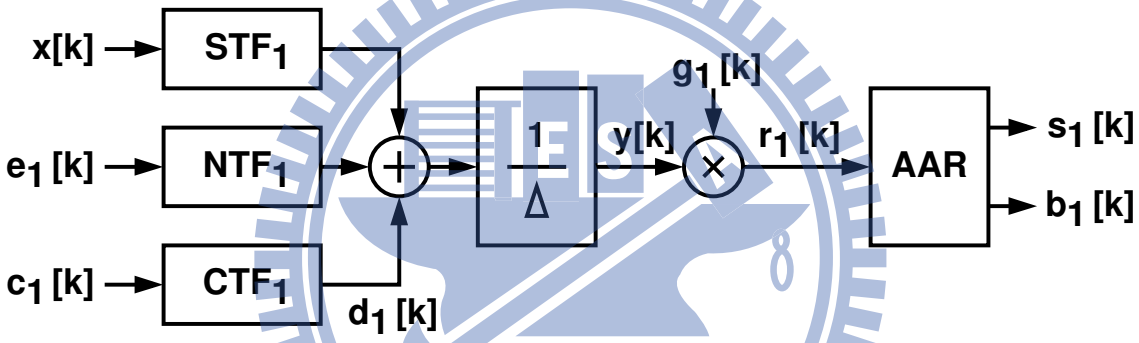


Figure 2.19: Calibration signal flow diagram for β_1 calibration.

2.4 Second-Order DSM Design Case

Figure 2.18 shows a 2nd-order DSM. It includes two integrators with their transfer functions expressed as

$$H_1(z) = \frac{\alpha_1}{1-\beta_1 z^{-1}} \qquad H_2(z) = \frac{\alpha_2}{1-\beta_2 z^{-1}} \tag{2.29}$$

The internal opamps of the integrators have a dc gain of 8.2 and 7.7 respectively, yielding $\alpha_1 = 0.804$, $\beta_1 = 0.902$, $\alpha_2 = 0.794$, and $\beta_2 = 0.897$. The regular sub-ADC1 following the 2nd integrator is single comparator. Thus, for this 2nd-order DSM, $N = 2$ and $\Delta = 2$. If the integrators are ideal and OSR = 64, the theoretical maximum SQNR is 79 dB for this DSM.

The proposed calibration scheme adjusts β_1 and β_2 separately. Integrators with adjustable β are described in Section 2.2. To calibrate β_1, a calibration signal $c_1[k] =$

$q_1[k]\times V_{c1}$ is injected to the input of the 2nd integrator. A calibration processor, CP1, takes the sub-ADC1 output $y[k]$ and generates a control signal $T_1[k]$ to adjust β_1 of the 1st integrator. The calibration signal $c_1[k]$ is a square wave with f_{q1} frequency, V_{c1} amplitude, and 50% duty cycle. Calibration processor CP1 is identical to the CP shown in Figure 2.10. In the CP1, its $g_1[k]$ signal has a duty ratio of D_{g1} and its BPD has a threshold of N_{th1}. Its output $T_1[k]$ controls the β_1 of the first integrator such that $\beta_1[k] = \beta_{0,1} + \Delta\beta_1 \times T_1[k]$. Figure 2.19 shows the calibration signal flow diagram, where $e_1[k]$ is the quantization noise of sub-ADC1. We have

$$\Delta \cdot Y(z) = \mathrm{STF}_1(z)X(z) + \mathrm{NTF}_1(z)E_1(z) + \mathrm{CTF}_1 C_1(z) \tag{2.30}$$

$$\mathrm{STF}_1(z) = \frac{H_1(z)H_2(z)}{1 + z^{-1}H_2(z) + z^{-1}H_1(z)H_2(z)} \tag{2.31}$$

$$\mathrm{NTF}_1(z) = \frac{1}{1 + z^{-1}H_2(z) + z^{-1}H_1(z)H_2(z)} \tag{2.32}$$

$$\mathrm{CTF}_1(z) = \frac{H_2(z)}{1 + z^{-1}H_2(z) + z^{-1}H_1(z)H_2(z)} \tag{2.33}$$

The sub-ADC1 output $y[k]$ is a summation of the input $x[k]$ shaped by the signal transfer function STF_1, the sub-ADC1 quantization $e_1[k]$ shaped by the noise transfer function NTF_1, and the calibration signal $c_1[k]$ shaped by CTF_1. The sub-ADC1 has a conversion gain of $1/\Delta$. The calibration signal $c_1[k]$ go through the CTF_1 filter, yielding $d_1[k]$. Thus, embedded in $y[k]$, $d_1[k]$ is the step response of CTF_1 triggered by $c_1[k]$. This step response settles toward a final value of

$$V_{cf1} = V_{c1} \times \mathrm{CTF}_1(1) \approx V_{c1} \times \frac{1-\beta_1}{\alpha_1} \tag{2.34}$$

The V_{cf1} value is used to detect β_1. The calibration processor CP1 masks $y[k]$ with $g_1[k]$ to extract only the valid V_{cf1} information. It then uses the AAR processing to diminish the calibration fluctuation caused by $x[k]$ and $e_1[k]$. The CP operation is identical to those described in Section 2.3. Following the design considerations outlined in Section 2.3, we choose $f_{q1} = f_s/32$, $D_{g1} = 7/16$, $V_{c1} = 0.1\Delta$, $\Delta\beta_1 = 0.01$, and $N_{th1} = 96$. The resulting time constant is $\tau_1 = 176421$.

To calibrate β_2, a calibration signal $c_2[k] = q_2[k] \times V_{c2}$ is injected to the input of sub-ADC1. The output of the 1st integrator is digitized by an extra ADC, sub-ADC2, yielding $w[k]$. For this design case, sub-ADC2 is a single comparator. A calibration

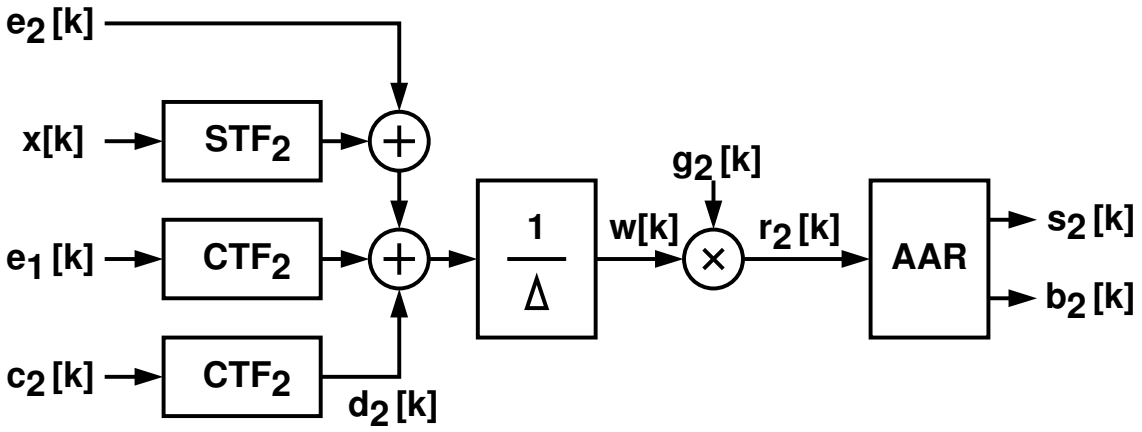


Figure 2.20: Calibration signal flow diagram for β_2 calibration.

processor, CP2, takes $w[k]$ and generates control signal $T_2[k]$ to adjust β_2 of the 2nd integrator. Design parameters are the calibration signal frequency f_{q2}, the calibration signal amplitude V_{c2}, the $g_2[k]$ signal duty ratio D_{g2}, the BPD threshold N_{th2}, and the β_2 control step size $\Delta\beta_2$. Figure 3.7 shows the calibration signal flow diagram, where $e_1[k]$ is the quantization noise of sub-ADC1 and $e_2[k]$ is the quantization noise of sub-ADC2. We have

$$\Delta \cdot W(z) = E_2(z) + \mathrm{STF}_2(z)X(z) + \mathrm{CTF}_2(z)\,[E_1(z) + C_2(z)] \tag{2.35}$$

$$\mathrm{STF}_2(z) = \frac{H_1(z) + z^{-1}H_1(z)H_2(z)}{1 + z^{-1}H_2(z) + z^{-1}H_1(z)H_2(z)} \tag{2.36}$$

$$\mathrm{CTF}_2(z) = \frac{-z^{-1}H_1(z)}{1 + z^{-1}H_2(z) + z^{-1}H_1(z)H_2(z)} \tag{2.37}$$

The sub-ADC2 output $w[k]$ is a summation of the input $x[k]$ shaped by the signal transfer function STF_2, the sub-ADC1 quantization $e_1[k]$ shaped by CTF_2, the sub-ADC2 quantization $e_2[k]$, and the calibration signal $c_2[k]$ shaped by CTF_2. The sub-ADC2 has a conversion gain of $1/\Delta$. The calibration signal $c_2[k]$ go through the CTF_2 filter, yielding $d_2[k]$. Thus, embedded in $w[k]$, $d_2[k]$ is the step response of CTF_2 triggered by $c_2[k]$. This step response settles toward a final value of

$$V_{cf2} = V_{c2} \times \mathrm{CTF}_2(1) \approx V_{c2} \times -\frac{1-\beta_2}{\alpha_2} \tag{2.38}$$

The V_{cf2} value can be used to detect β_2. The CP2 operation is similar to the CP1 operation. Note that V_{cf2} is negative, while V_{cf1} is positive. Thus, referring to Figure 2.11, the

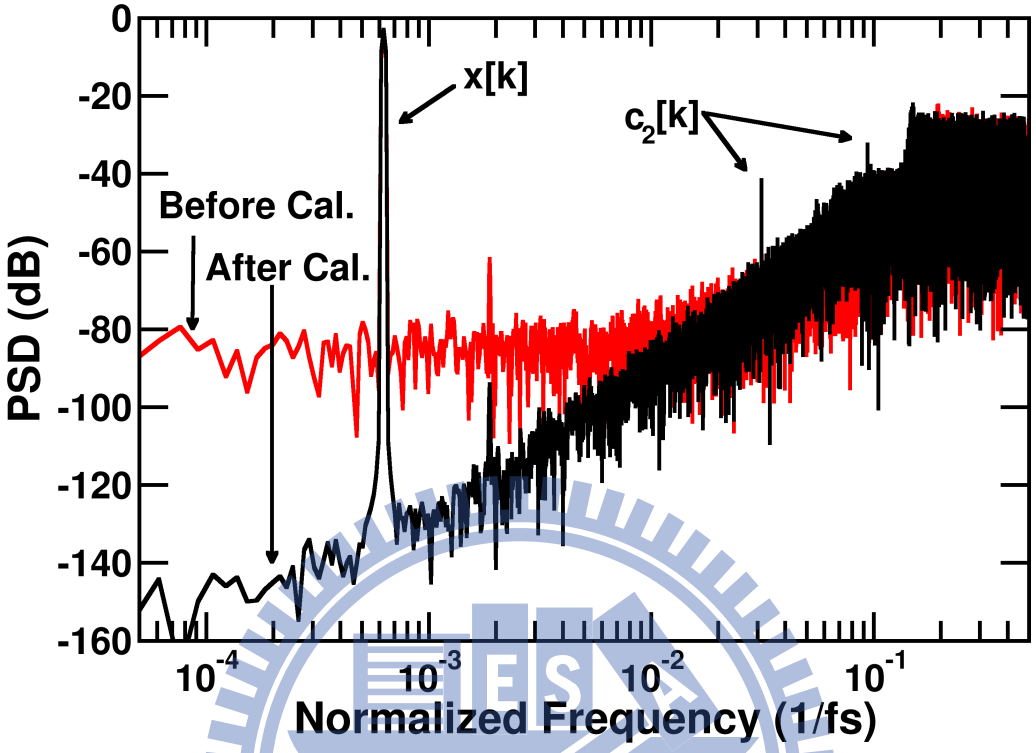


Figure 2.21: Output spectra of the 2nd-order DSM design case.

polarity of $g_2[k]$ is inverted. To simplify design, $c_2[k]$ is identical to $c_1[k]$ and CP2 is identical to CP1. The design parameters f_{q2}, D_{g2}, V_{c2}, $\Delta\beta_2$, and N_{th2} are identical those for $c_1[k]$ and CP1.

Figure 2.21 shows the DSM output spectra before and after calibration. The input is a sine wave with a frequency of $(41/2^{16})f_s$ and an amplitude of -3 dBFS. Assuming an OSR of 64, the resulting SQNR is 52 dB before calibration, and is improved to 72 dB after calibration. Assume the DSM input bandwidth is 2 MHz and the sampling frequency is $f_s = 256$ MHz, yielding an oversampling ratio OSR $= 64$. Then a calibration time of $2 \times 3\tau_1 = 4.1$ msec is required for both β_1 and β_2 to converge from 0.9 to 0.995. Besides this, the SFDR grows from 57.71 dB to 87.25 dB.

The injected calibration signals increase the swing of the internal nodes in the loop filter. As V_{cj} grows, j is 1 or 2, not only a rise of the output swing of integrators, but also a rise of the quantization noise power caused by the overload of the internal quantizer are discovered. Therefore, the amplitude of V_{cj} is restricted and the bounds are decided from

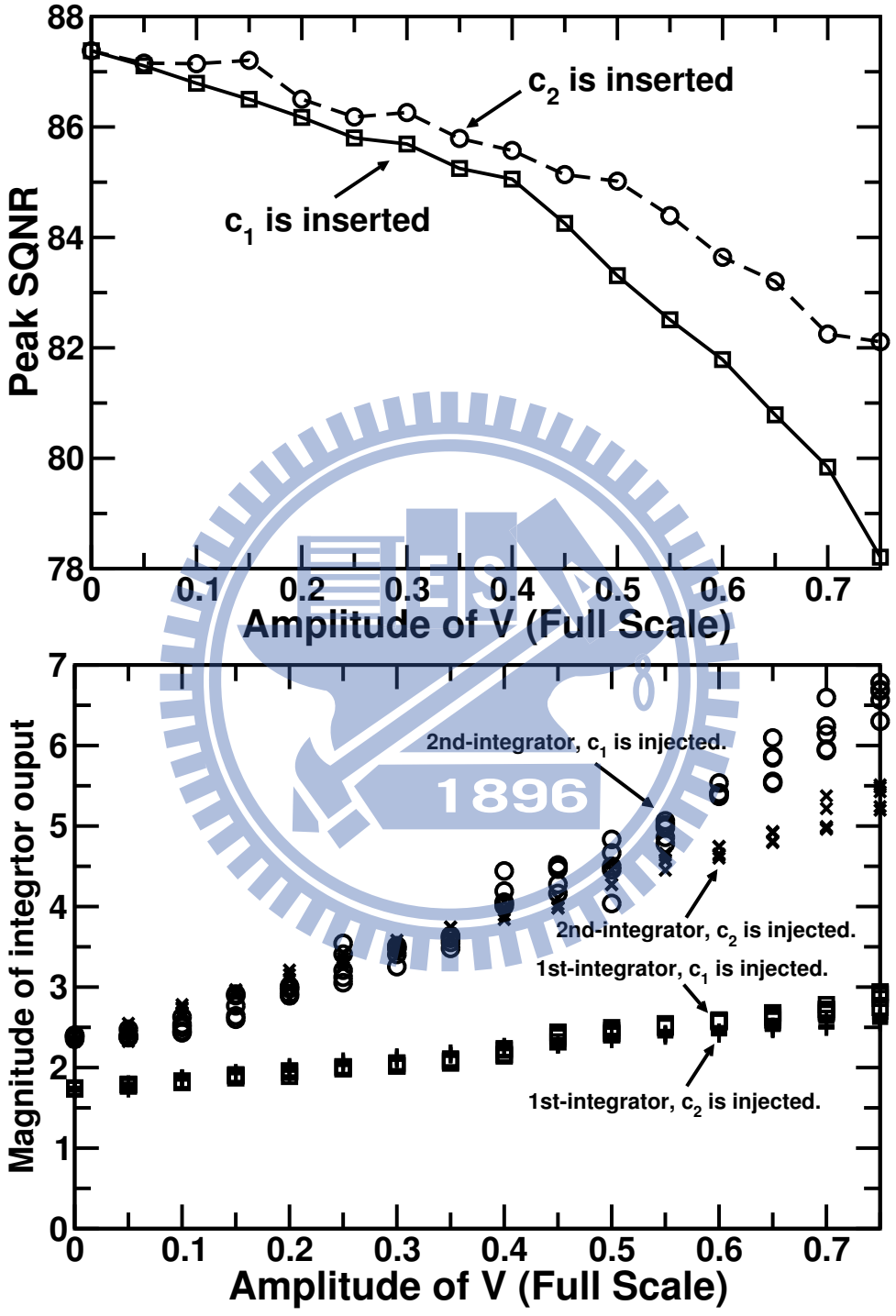


Figure 2.22: The amplitude of V_{cj} vs. peak SQNR as well as the magnitude of integrator output.

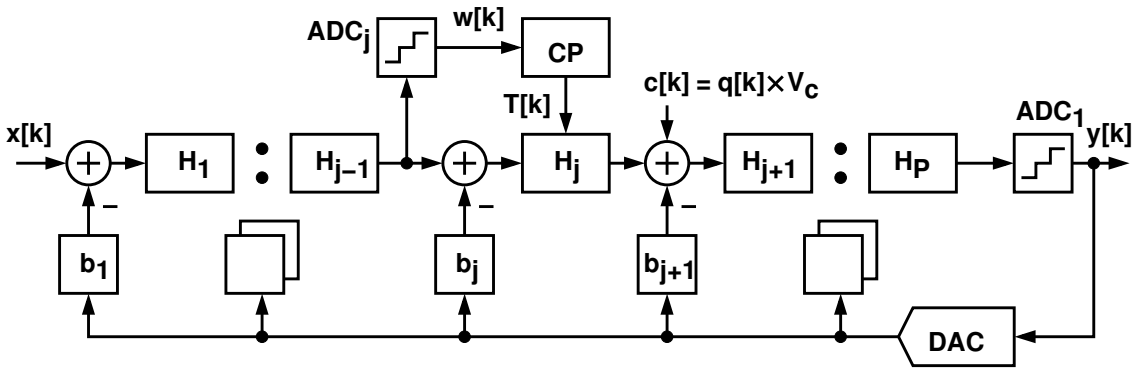


Figure 2.23: Calibration of a CIFB DSM.

simulations, such as peak SQNR and the magnitude of integrator output. For the second-order one-bit DSM demonstrated earlier, these two kinds of simulations are plotted in Figure 2.22. Along as V_{cj} is smaller than 0.4, the decrease of SQNR is no more than 2dB. If $V_{cj} > 0.4$, V_{c1} especially, a noticeable loss of peak SQNR will happen. As regards the magnitude of integrator output, the higher amplitude of V_{cj} is, the lagger magnitude of integrator output will be.

2.5 High-Order DSM Design Case

The proposed calibration can be applied to DSMs of any structure. Figure 2.23 is a DSM containing P cascaded integrators with distributed feedback (CIFB). The transfer functions of the integrators are $H_1(z)$, ..., $H_P(z)$. The j-th integrator, where $j = 1, \cdots, P$, is modeled as

$$H_j(z) = \frac{\alpha_j}{1-\beta_j z^{-1}} \quad \text{or} \quad \frac{\alpha_j z^{-1}}{1-\beta_j z^{-1}} \tag{2.39}$$

The calibration corrects the β of the integrators one at a time. To calibrate the j-th integrator, $H_j(z)$, a calibration signal $c[k]$ is injected at the input of the $(j+1)$-th integrator, while the output of the $(j-1)$-th integrator is digitized as $w[k]$ and send to the calibration processor (CP). The CP output $T[k]$ adjusts the β of the j-th integrator.

Figure 2.24 shows the $c[k]$-to-$w[k]$ signal flow, in which $x[k]$ and the quantization errors generated by the sub-ADCs are neglected. The function $F(z)$ is the transfer function

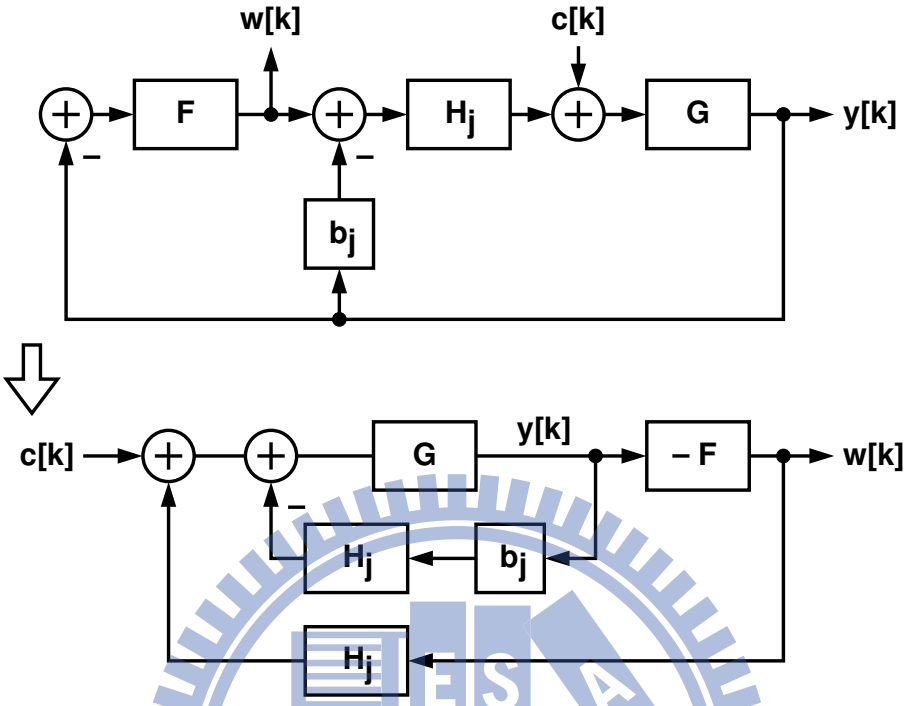


Figure 2.24: $c[k]$-to-$w[k]$ signal flow in a CIFB DSM.

from $y[k]$ to $w[k]$. It involves integrators from H_1 to H_{j-1}. The function $G(z)$ is the transfer function from $c[k]$ to $y[k]$. It involves integrators from H_{j+1} to H_P but without the contribution from $H_j(z)$. In the bottom half of Figure 2.24, the signal flow is redrawn so that $F(z)$ and $G(z)$ are in the forward signal path and $H_j(z)$ and $b_j H_j(z)$ are the feedback paths. The $c[k]$-to-$w[k]$ transfer function is

$$\mathrm{CTF}_j(z) = \frac{W(z)}{C(z)} = \frac{-F(z)G(z)}{H_j(z)F(z)G(z) + b_j H_j(z)G(z) + 1} \tag{2.40}$$

The dc gain of $\mathrm{CTF}_j(z)$ is $\mathrm{CTF}_j(0)$. Since the signal structure of $F(z)$ is a cascade of integrators, we have $F(0) \gg 1$ and

$$\mathrm{CTF}_j(0) \approx \frac{-F(0)G(0)}{H_j(0)F(0)G(0)} = -\frac{1}{H_j(0)} = -\frac{1-\beta_j}{\alpha_j} \tag{2.41}$$

We design $c[k]$ as a square wave with an amplitude of V_c. In each $c[k]$ cycle, the step response of $\mathrm{CTF}_j(z)$ is embedded in $w[k]$. We design the $c[k]$ period to be long enough so that the step response can settle toward its final value, which is $V_{cf,j} = V_c \times -(1-\beta_j)/\alpha_j$. The CP extracts $V_{cf,j}$ to determine the polarity of $1-\beta_j$, and then adjusts β_j to make it approaches 1.

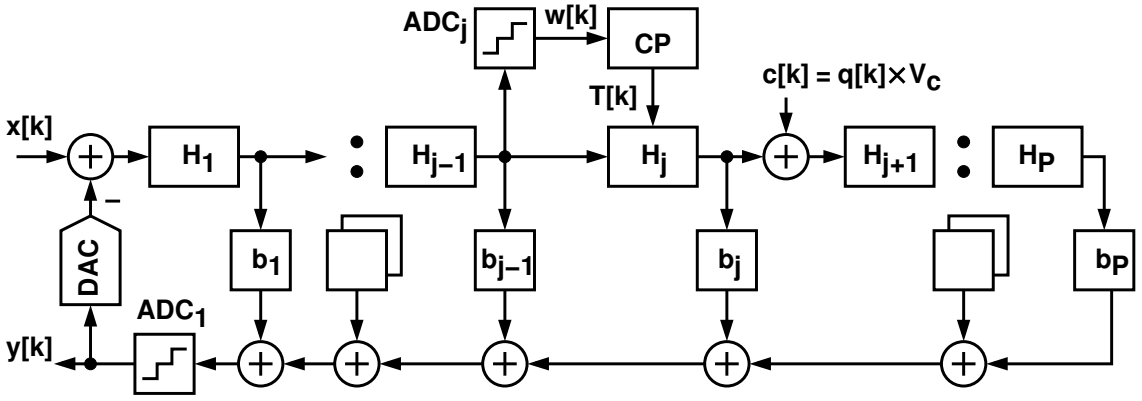


Figure 2.25: Calibration of a CIFF DSM.

To calibrate the 1st integrator, $H_1(z)$, the calibration signal $c[k]$ is injected to the input of the 2nd integrator and the DSM regular digital output $y[k]$ is used as the CP input. The corresponding $c[k]$-to-$y[k]$ signal flow is similar to those shown in Figure 2.24, but without the $-F(z)$ block and the outer H_j feedback path. The $c[k]$-to-$y[k]$ transfer function is

$$\mathrm{CTF}_1(z) = \frac{Y(z)}{C(z)} = \frac{G(z)}{1 + b_1 H_1(z) G(z)} \tag{2.42}$$

Since $b_1 H_1(0) G(0) \gg 1$, the dc gain of $\mathrm{CTF}_1(z)$ can be approximated by

$$\mathrm{CTF}_1(0) \approx \frac{G(0)}{b_1 H_j(0) G(0)} = \frac{1}{b_1 H_j(0)} = \frac{1 - \beta_1}{b_1 \alpha_1} \tag{2.43}$$

When $c[k]$ is applied, the final value of the $\mathrm{CTF}_1(z)$ step response is $V_{cf,1} \approx +V_c(1 - \beta_1)/(b_1\alpha_1)$. The polarity of $V_{cf,1}$ is different from that of $V_{cf,j}$ where $j \neq 1$.

Figure 2.25 is a DSM containing P cascaded integrators with distributed feedforward summation (CIFF). Similar to the CIFB DSM shown in Figure 2.23, to calibrate the j-th integrator, $H_j(z)$, a calibration signal $c[k]$ is injected at the input of the $(j+1)$-th integrator, while the output of the $(j-1)$-th integrator is digitized as $w[k]$ and send to the calibration processor (CP). The CP output $T[k]$ adjusts the β of the j-th integrator. Figure 2.26 shows the $c[k]$-to-$w[k]$ signal flow, where

$$\begin{aligned} F_1(z) &= H_1(z) \times H_2(z) \times \cdots \times H_{j-1}(z) \\ F_2(z) &= b_1 H_1(z) \times b_2 H_2(z) \times \cdots \times b_{j-1} H_{j-1}(z) \\ G(z) &= b_{j+1} H_{j+1}(z) \times b_{j+2} H_{j+2}(z) \times \cdots \times b_P H_P(z) \end{aligned} \tag{2.44}$$

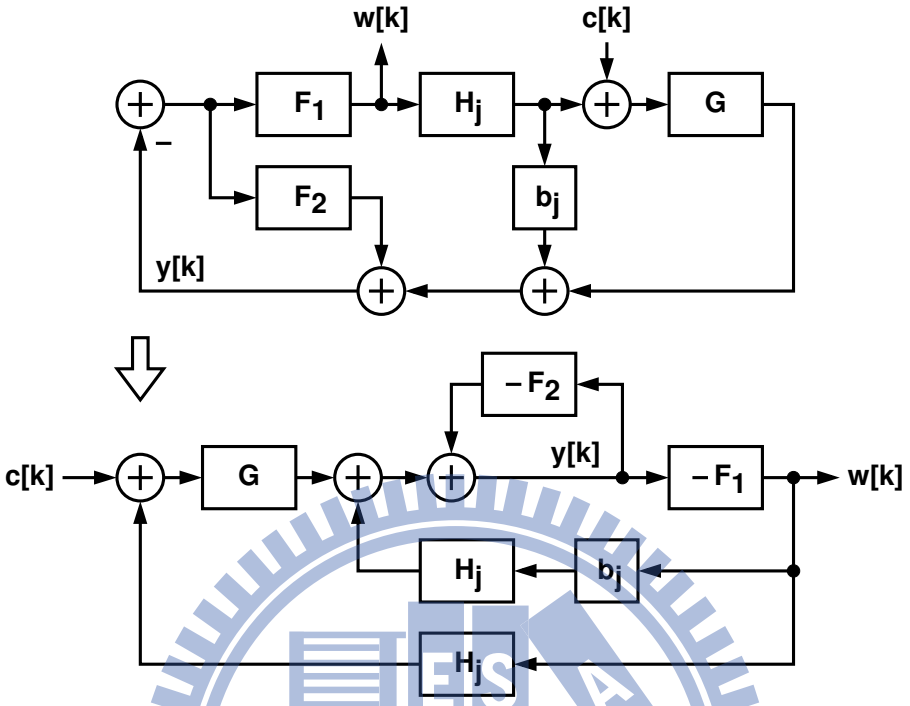


Figure 2.26: $c[k]$-to-$w[k]$ signal flow in a CIFF DSM.

From Figure 2.26, it can be shown that $\mathrm{CTF}_j(0) \approx -1/H_j(0)$ for $j \geq 2$ and $\mathrm{CTF}_1(0) \approx +1/H_1(0)$.

The proposed calibration technique can correct the β of all integrators in a DSM. It calibrates each individual integrator one at a time. Although a square wave is injected into the DSM for calibration, its effect on the DSM is minuscule. The calibration itself is robust. It can easily converge as long as the amplitude of the square-wave calibration signal $c[k]$ is sufficiently large. It does not require high-precision analog circuitry. It can tolerate the non-linearity of the sub-ADCs. The design procedures for the proposed calibration scheme are similar to those described in Section 2.3 and Section 2.4.

2.5.1 A Third-Order CRFB DSM

Figure 2.27 shows a 3rd-order DSM design case. It employs the cascade of resonators with distributed feedback (CRFB) structure [20]. Its NTF has three zeros, i.e.,

$$z_1 = \beta_1 \quad z_{2,3} = \sqrt{\beta_2 \beta_3} \times e^{\pm j\rho} \tag{2.45}$$

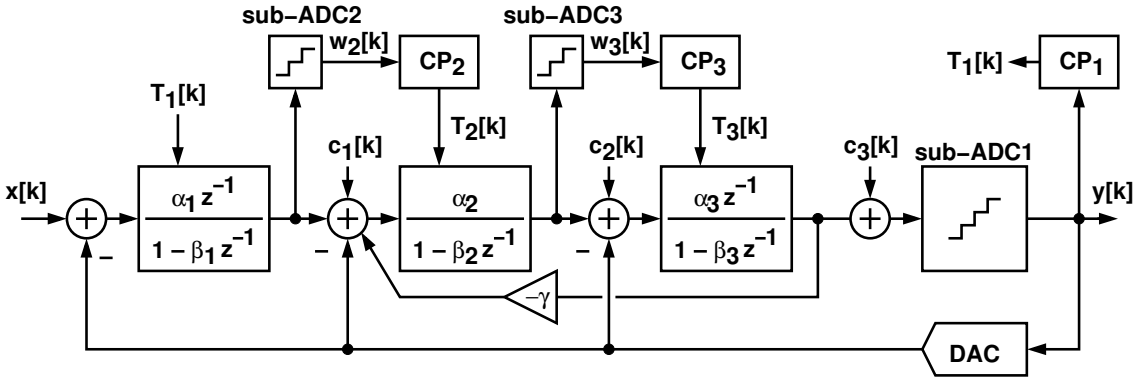


Figure 2.27: A 3rd-order DSM with the proposed calibration scheme.

where

$$\rho = \tan^{-1}\left(\sqrt{\frac{4\beta_2\beta_3}{(\beta_2+\beta_3-\gamma\alpha_2\alpha_3)^2}-1}\right) \tag{2.46}$$

For an ideal case, $\gamma = 0.0064$, $\alpha_1 = 0.145$, $\alpha_2 = 0.474$, $\alpha_3 = 0.789$, and all $\beta = 1$, yielding $z_1 = 1$ and $z_{2,3} = e^{\pm j2\pi/128}$. All zeros are located on the z-plane unit circle. Their frequencies are 0 and $f_s/128$ respectively. Assume the DSM operates at an oversampling ratio OSR = 64, and its sub-ADC1 and DAC have $N = 3$ quantization levels. Then, the DSM can achieve a theoretical maximum SQNR of 90 dB.

From (2.45) and (2.46), if $\beta < 1$, then the zeros are moved inside the z-plane unit circle, degrading the NTF's noise suppression capability in the signal band. Consider a non-ideal case, in which $\gamma = 0.0064$, $\alpha_1 = 0.146$, $\alpha_2 = 0.478$, $\alpha_3 = 0.80$, $\beta_1 = 0.982$, $\beta_2 = 0.940$, and $\beta_3 = 0.9$. This DSM can only achieve a theoretical maximum SQNR of 66 dB with a −5 dBFS input.

As shown in Figure 2.27, the proposed calibration scheme is added to this DSM. The regular sub-ADC and its corresponding DAC have $N = 3$ quantization levels, yielding $\Delta = 2/(N-1) = 1$. All calibration signals, $c_1[k]$, $c_2[k]$, and $c_3[k]$, are identical. They have a frequency $f_q = f_s/64$ and an amplitude $V_c = 0.1\Delta$. For CP1, $D_{g1} = 0.125$, $N_{th1} = 96$, and $\Delta\beta_1 = 0.005$, yielding $\tau_1 = 223488$. To reduce the analog overhead of the calibration, sub-ADC2 and sub-ADC3 are realized with a single comparator. For CP2 and CP3, $D_{g2} = D_{g3} = 0.125$, $N_{th2} = N_{th3} = 96$, and $\Delta\beta_2 = \Delta\beta_3 = 0.005$, yielding $\tau_2 = 733594$ and $\tau_3 = 1228800$. Assume the DSM's sampling rate is $f_s = 256$ MHz

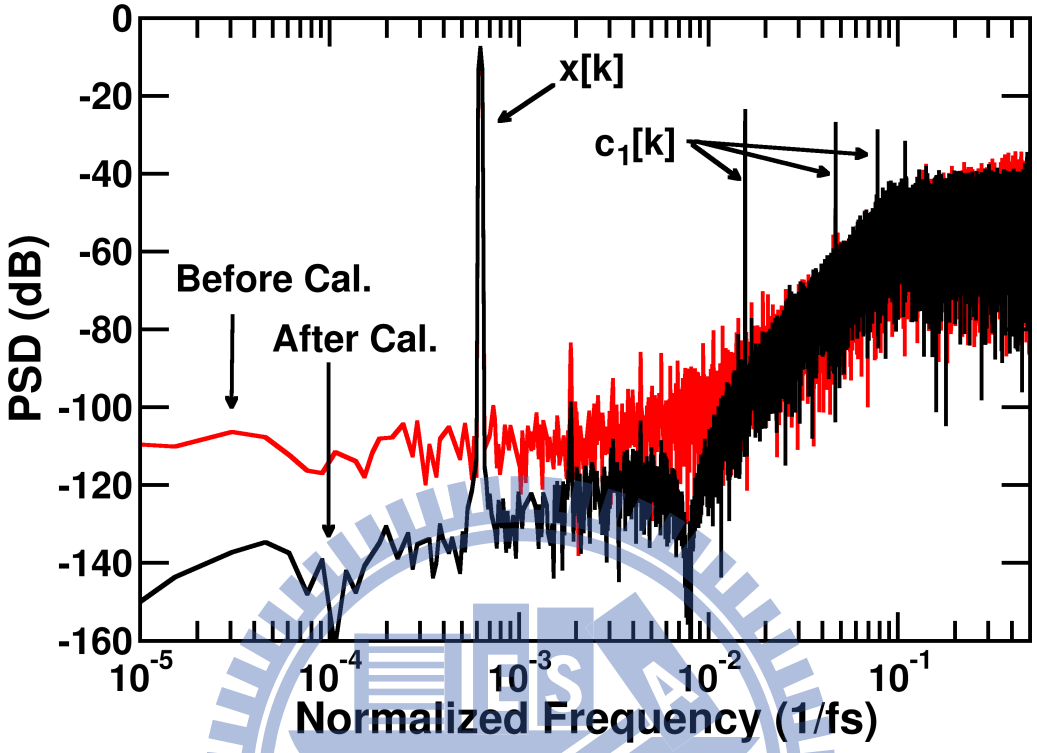


Figure 2.28: Output spectra of the 3rd-order CIFB DSM design case.

and the same amount of time is allocated for each CP to operate. Then, the worst-case calibration time is $3 \times 3\tau_3 = 43$ msec for β_3 to converge from 0.9 to 0.995.

Figure 2.28 shows the output spectra of this DSM design case before and after the calibration. The input is a sine wave with a frequency of $(41/2^{16})f_s$ and an amplitude of -5 dBFS. If OSR $= 64$, then the SQNR is 66 dB before calibration, and is improved to 84 dB after calibration. Note that a notch at $f_s/128$ appears only after the calibration. The notch is desirable in the original DSM design. This illustrates that the proposed calibration can also correct the NTF zeros not at dc.

For the above 3rd-order DSM design case, the input signal bandwidth is from 0 to $f_s/128$, while the frequency of the calibration signal $c_j[k]$ is $f_s/64$, Figure 2.29 shows the output spectra of the DSM after its output passing through a $sinc^4$ decimation filter. The $c_j[k]$-related signal is completely eliminated, since its frequency components are located at the notches of the decimation filter.

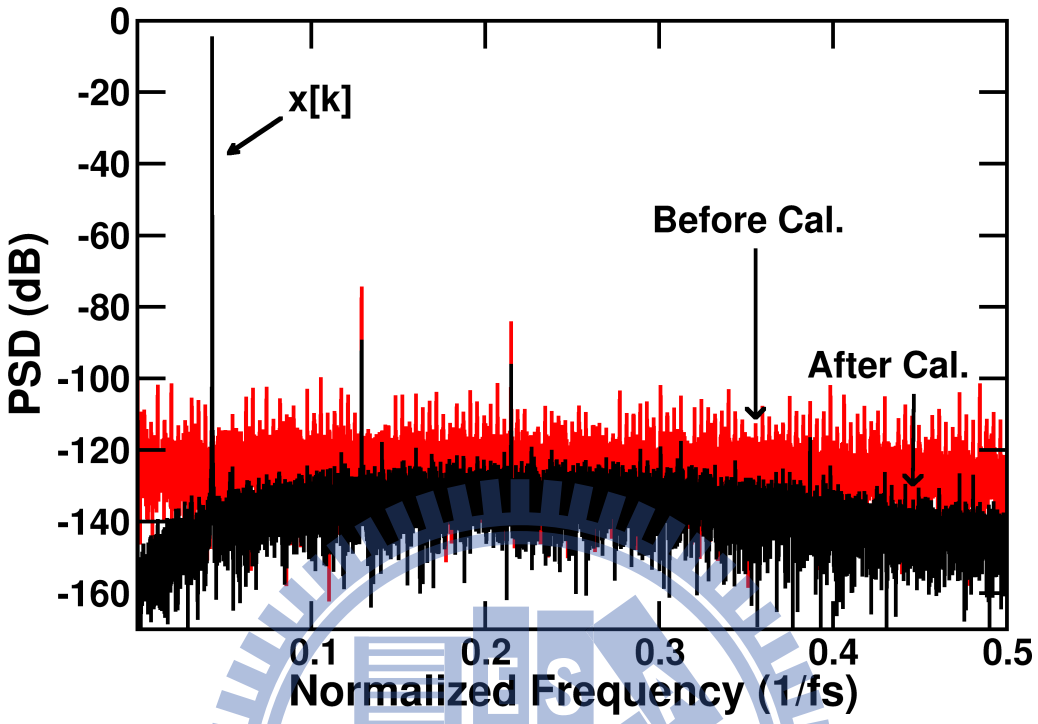


Figure 2.29: Filtered output spectra of the 3rd-order DSM design case by a sinc^4 decimation filter.

2.5.2 A Third-Order CIFF DSM

A 3^{rd}-order CIFF DSM is simulated to demonstrate the proposed scheme. Figure 2.30 shows the DSM, which is designed in a 65 nm CMOS technology with a 1 V supply voltage. The entire circuit is fully differential. The input and output are x and y, respectively. ADC1 and DAC are 2-bit to increase system stability. Three comparators comprise ADC1 with the thresholds of $\{0, \pm 2/9\text{V}\}$. The output swing of DAC is ± 1 V. Signal scaling and feed-forward paths are used to relax the linearity requirements of integrators. A passive SC adder preceding ADC1 combines the feed-forward paths. All of the integrators adopt single-stage inverter-based opamps [36]. Figure 2.31 shows the opamp schematic. The channel lengths of the MOSFETs are chosen to be 60 nm. The resulting dc gain is 8.4 and the gain-bandwidth is 3.9 GHz with a capacitive load of 4 pF. The capacitances are C_{s1}=3.981 pF, C_{i1}=10.179 pF, C_{s2}=976 fF, C_{i2}=595 fF, C_{s3}=354 fF, C_{i3}=1013 fF, C_g=16 fF, C_{u1}=140 fF, C_{u2}=90 fF and C_{u3}=80 fF. The DSM is operated at 640 MHz with OSR=32.

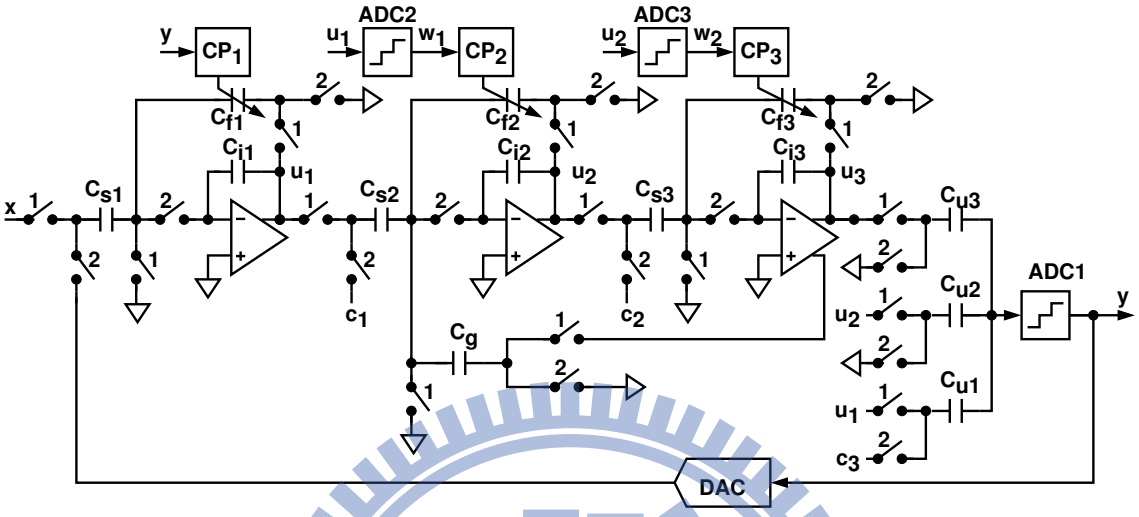


Figure 2.30: A 3^{rd}-order CIFF DSM with local resonator feedback.

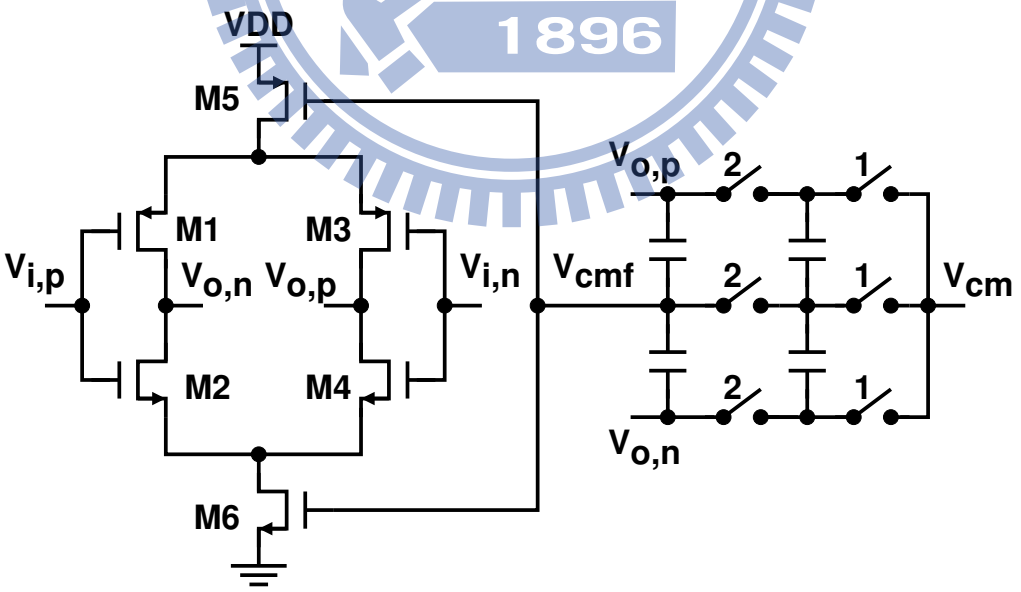


Figure 2.31: Inverter-based opamp with common-mode feedback.

To calibrate the first integrator H_1, the calibration signal c_1 is injected into to the second integrator H_2, and CP_1 receives the data stream y from ADC1. To calibrate H_2, c_2 is injected to the input of the third integrator H_3, and the output u_1 from H_1 is quantized by ADC2 and sent to CP_2. To calibrate H_3, c_3 is injected to the input of ADC1, and the output u_2 from H_2 is quantized by ADC3 and sent to CP_3. ADC2 and ADC3 are 2-bit. The calibrations are performed sequentially and run in the background during the DSM operation. Three calibration signals c1, c2, and c3 are identical, with a frequency of 11.43 MHz and an amplitude of 0.01 V. The compensation capacitor C_{f1} comprising a 5-bit capacitor bank can vary from 0 fF to 837 fF. C_{f2} comprising a 4-bit capacitor bank can vary from 0 fF to 240 fF. C_{f3} comprising a 4-bit capacitor bank can vary from 0 fF to 90 fF.

Figure 2.32 shows the output spectra of the DSM from the Spectre® circuit simulator. The bandwidth is 10 MHz. The input is a sine wave with a frequency of 1.035 MHz and an amplitude of 0.625 V. Every standard variation of the integrator output is around 0.1 V. Before calibration, the quantization noise leaks into the bandwidth and the SNDR is 73 dB. After calibration, the noise floor drops and a notch appears at 8 MHz. The SNDR is increased to 87.3 dB and the SNR is 88.7 dB. The power consumption of this DSM excluding CPs is 21 mW. Among that, the integrators consume 14.7 mW; ADC1, DAC and the adder consume 4.1 mW; ADC2 and ADC3 consume 2.2 mW. All CPs have $D_g = 2/7$ and $N_{th} = 96$. The calibration time, for each β to converge, is around 15 msec. This design reveals that the developed method can correct the NTF whether their zeros are placed at dc or not. The calibration is robust. It can tolerate the non-linearity of the sub-ADCs. As long as the amplitude of the square-wave calibration signal is large enough, the calibration can easily converge. Although a calibration signal is injected into the DSM, its effect on the DSM is tiny. The calibration does not require highly precise analog circuitry, and does not require cumbersome digital circuits such as narrow band filters.

2.6 Summary

Lossy integrators in a delta-sigma modulator (DSM) degrade the signal-to-quantization-

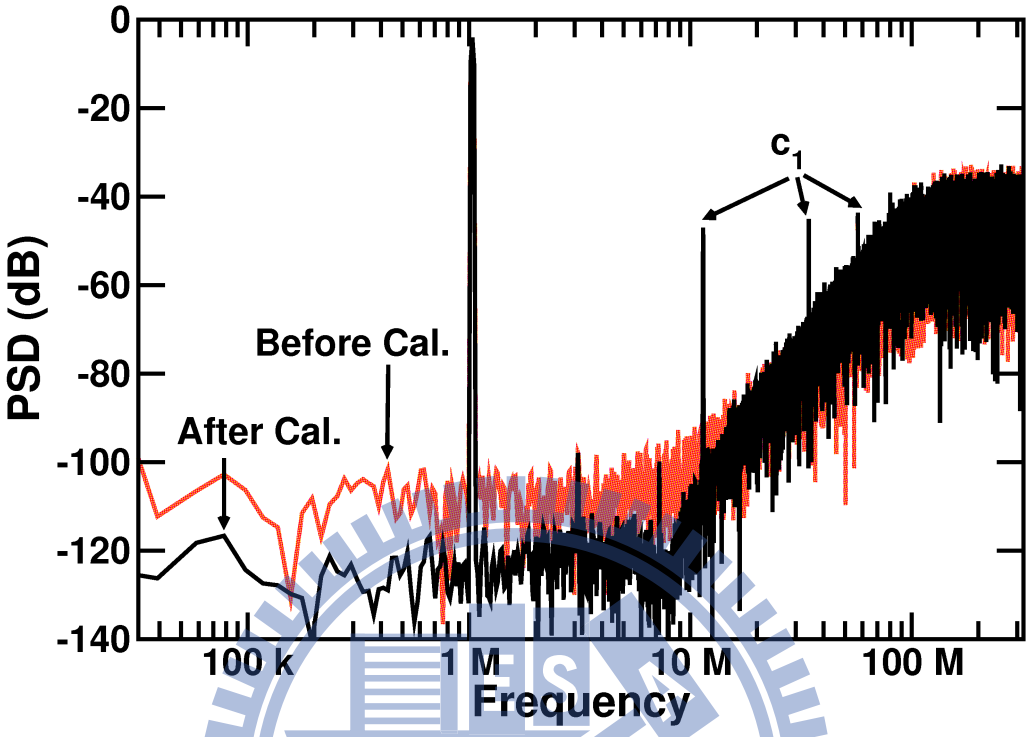


Figure 2.32: Output spectra of the 3^{rd}-order CIFF DSM design case.

noise ratio (SQNR) of the DSM. This paper proposes a calibration technique to correct the integration leakage of switched-capacitor integrators. Although the integrators are embedded in a DSM, they can be calibrated one at a time without interrupting the normal DSM operation. Since each integrator is calibrated separately, the design parameters of the corresponding calibration signal and calibration processor can be easily optimized. The proposed scheme can calibrate all integrators in a DSM of any form.

The proposed calibration technique enables the use of low-gain opamps in high-resolution DSMs. It is specially useful for designing DSMs in advanced nano-scale CMOS technologies, which offer MOSFETs of large g_m/C_{gs} but small dc gain g_m/g_{ds}. The effect of opamp's non-linearity on DSMs is not pursued in this paper. The nonlinear effects can be mitigated by reducing the output signal range of the integrators or by using DSM configurations with input feed-forward path [37].

Besides the latest research reveals that the non-linear error can be treated by the adaptive filter in the digital domain [14]. Therefore, we proposed a calibration that attempts to further diminish the DC gain in company with the scaled-down process. The analysis in

this paper is based on the linear opamp, however, the SQNR enhancement of a calibrated DSM remains even the opamp is non-linear.

Chapter 3

Noise Leakage Calibration for Cascaded DSMs

The quantization noise leakage limits the performance of a cascaded DSM. In this chapter, the noise leakage is addressed in Section 3.1 at first. Then our novel solution based on AAR-calibration is disclosed by a 2-2 cascaded DSM design case in Section 3.2. The procedure of calibration techniques is also present.

3.1 Noise leakage Issue

A conventional dual-stage cascaded DSM is shown in Figure 3.1. There are two DSMs followed by the responsing noise cancellation filter (NCF). Idealistically, NCFs eliminate the first stage quantization noise completely, and shape the second stage quantization noise once more. However, the mismatch between analog loop filter and digital cancellation filter is unavoidable. This leads the first stage quantization noise leaks into the signal bandwidth and degrades the overall SQNR of DSM. Too often, the quantization noise leakage is the major cause in the drop of DSM performance. This undesired effect typically requires high accuracy analog components to lessen. Such demand limits the feasibility of cascaded DSMs with the advanced CMOS technologies. For example, a standard 32 nmm CMOS technology exhibits a maximum transition frequency f_t up to 400 GHz but its intrinsic voltage gain is only about 6 [2, 3]. Therefor, the CMOS tech-

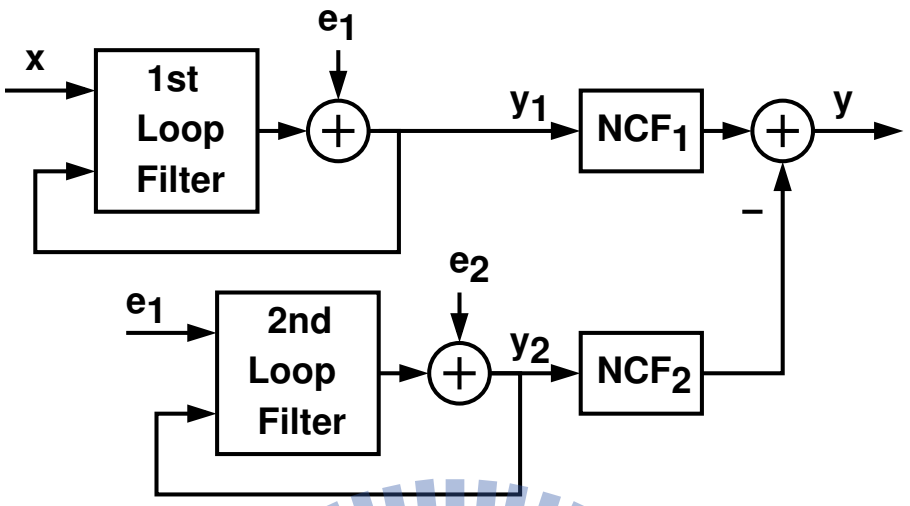


Figure 3.1: Traditional dual-stage $\Delta\Sigma$ modulator structure.

nology scaling even speeds up the clock frequency, the low intrinsic gain dramatically exacerbate analog circuits performance than before. One disaster after another, the low voltage supply is an obstacle to design an high speed opamp with a good DC gain.

Consider a typical dual-stage cascaded DSM in Figure 3.1. The first stage converters the analog input x into digital output y_1. The internal quantization noise of DSM_1 is e_1. Then e_1 is feed into the second stage to generate another digital output y_2. The internal quantization noise of DSM_2 is e_2. The digital output $y1$ and $y2$ is processed by NCF_1 and NCF_2 respectively. And the resulting is summed up as the cascaded DSM final digital output y, which can be found as

$$\begin{aligned} Y =& \mathrm{STF}_1\mathrm{NCF}_1 \cdot X - \mathrm{NTF}_2\mathrm{NCF}_2 \cdot E_2 + \\ & (\mathrm{NTF}_1\mathrm{NCF}_1 - \mathrm{STF}_2\mathrm{NCF}_2)\, E_1 \\ =& \mathbf{STF} \cdot X + \mathbf{NTF} \cdot E_2 + \mathbf{NLF} \cdot E_1 \end{aligned} \tag{3.1}$$

where STF_i is the signal transfer function, NTF_i is the noise transfer function and NLF is the noise leakage transfer function. Choosing

$$\mathrm{NCF}_2 = \frac{\mathrm{NTF}_1\mathrm{NCF}_1}{\mathrm{STF}_2} \tag{3.2}$$

will remove $e1$ completely and shape e_2 further. But finite opamp DC gain and the capacitor mismatch lead to imperfect analog filters, precise noise cancel filters in digital domain

become impossible. When poor analog performance caused device scaling is concerned, trimming NCF_2 is more preferable and provides opportunities to relax analog requirement as well as save power dissipation. A popular implementation of NCF_2 is an adaptive finite-impulse-response (FIR) filter based on least-mean-square (LMS) algorithm. Depending on the cascaded DSM architecture, infinite-impulse-response IIR to FIR approximation is needed occasionally. A simplified cascaded DSM architecture was introduced in [38]. Its first stage is a feed-forward low-distortion topology, and the second stage is characterized by $STF_2 = 1$. Then the second integrator's output is coupled to the second stage rather than e_1. The main advantage of this modification is that, the FIR tap number is reduced as the IIR to FIR approximation is unnecessary.

A 2-2 MASH originated from this concept and its linear model are depict in Figure 3.2. Where the i-th integrator outputs u_i and its z-domain transfer function is H_i. In addition, NCF_1 is decided as z^{-2}. The NLF is

$$NLF = NTF_1 \times (NCF_1 - H_1H_2NCF_2) \tag{3.3}$$

now. Since two paths of e_1 exist, matching NCF_1 with $H_1H_2NCF_2$ will dismiss the quantization noise leakage. An adaptive FIR is born for this. As long as injecting a test signal into the first stage, the noise leakage could be traced. However, (1) the correction terms of adaptive FIR is prescribed to three for compensating imperfect analog circuits; (2) these terms are difficult to perceive directly through a unique test signal; (3) the limit of adaptive NCF_2 cause the quantization noise remain within the signal band. All leave room to improve the calibration of a cascaded DSM.

3.2 A Design Case of 2-2 Cascaded DSM

We propose a cascaded DSM, which apply not only quantization noise leakage calibration but also integrator calibration. Figure 3.3 is a 2-2 MASH based on this novel structure, and the linear model is shown too. For attenuation of quantization noise leakage, two events are encouraged. One is depressing noise via the noise shaping of the first stage NTF_1, another is seeking $NCF_2 = z^{-2}/(H_1H_2)$. The integrator leakage calibration suppresses noise power at first. Two tunable integrators of the first stage are healed

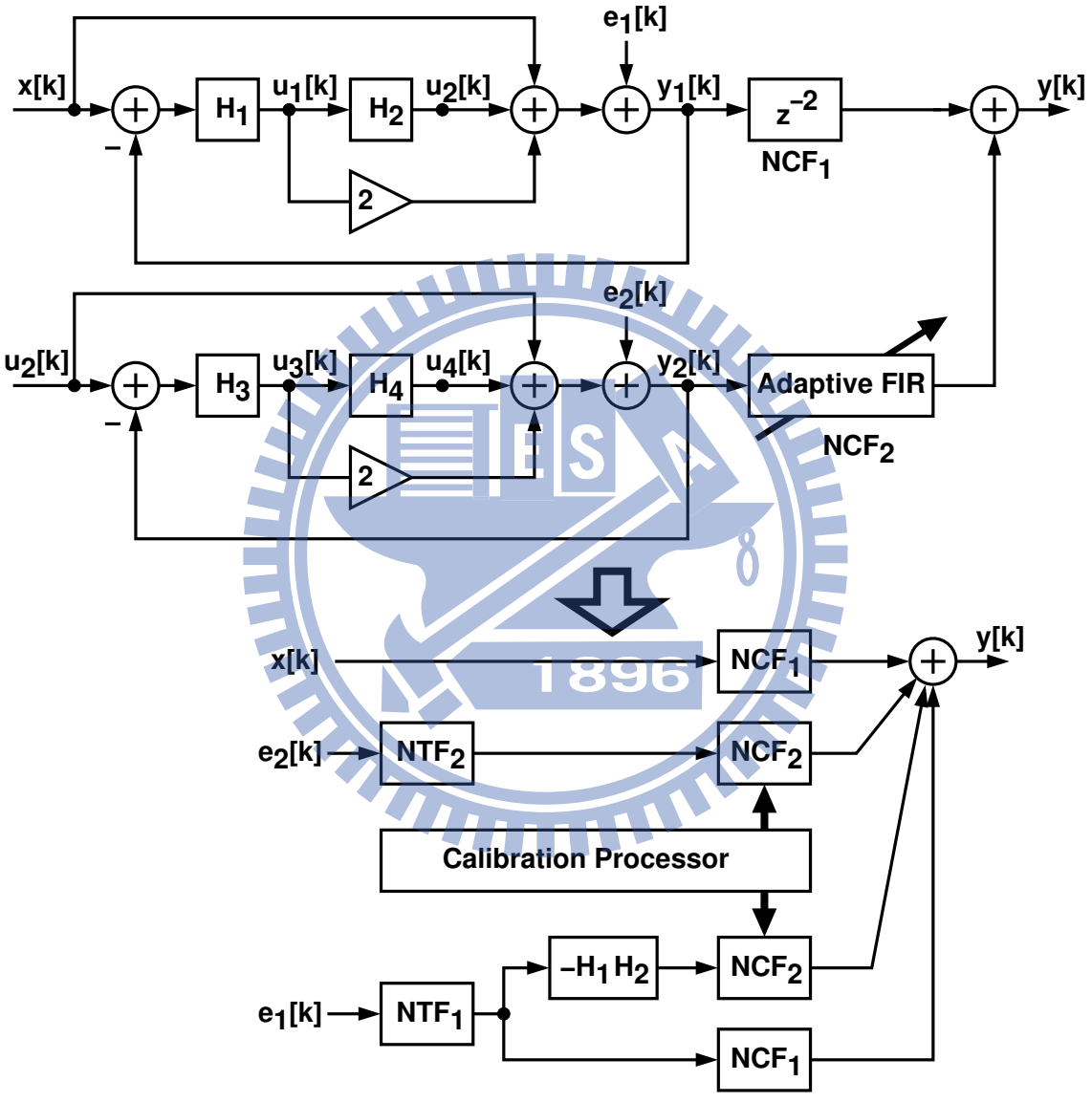


Figure 3.2: A 2-2 $\Delta\Sigma$ architecture with adaptive noise cancelantion fillter.

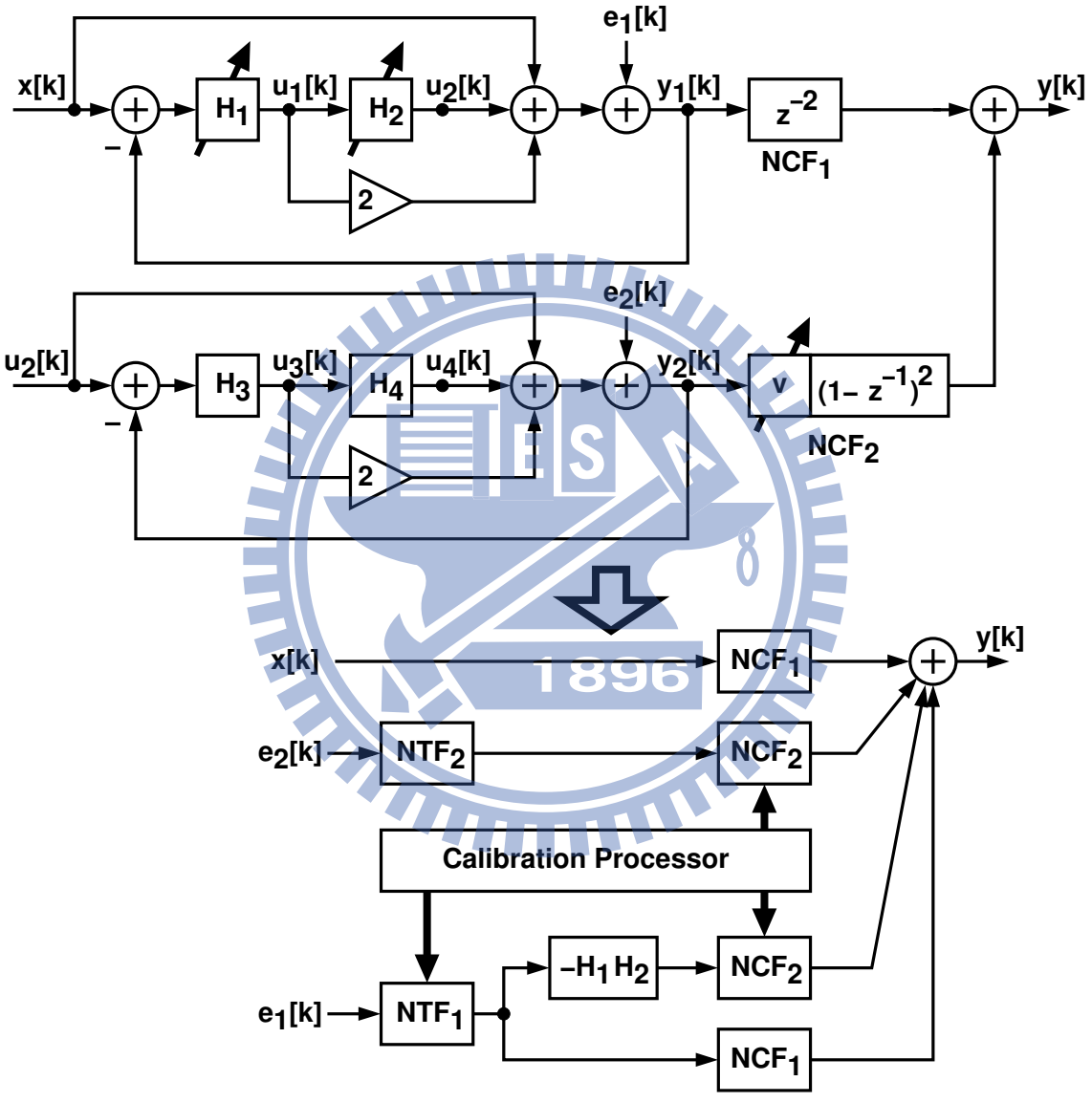


Figure 3.3: Proposed 2-2 $\Delta\Sigma$ architecture with leakage calibration.

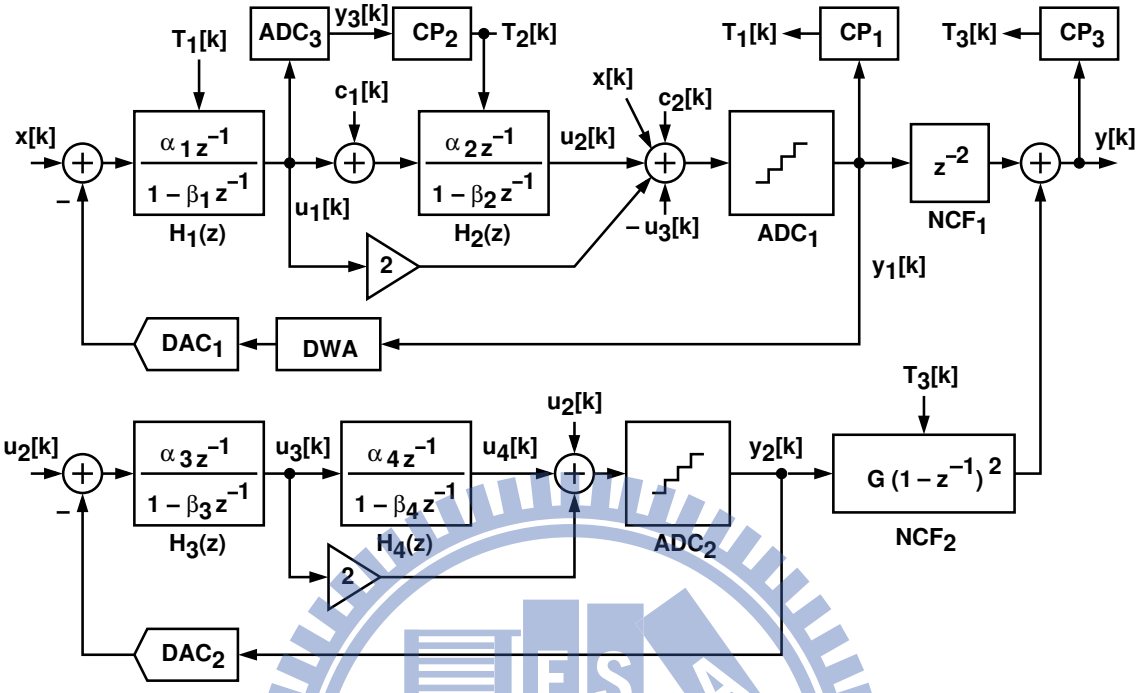


Figure 3.4: Proposed 2-2 $\Delta\Sigma$ modulator with calibration techniques.

separately in analog domain. The detail is addressed in Section 3.2.1. Then, the quantization noise leakage calibration is operated in digital domain to match between analog and digital noise transfer function. Thanks to calibrated integrators, NCF_2 becomes a basic second-order differentiator i.e. $\left(1-z^{-1}\right)^2$ with one gain coefficient. There is only one coefficient should be corrected, thus the implementation of adaptive NCF_2 is simplified amazingly. How to tune this parameter is discussed in Section 3.2.2. When all calibration schemes are accomplished, the minimization of NLF is done and then the SQNR of calibrated DSM is restore. It is particular noteworthy that, the developed modification allows the employment of low-gain high-speed opamps without paying the penalty of a extract NCF_2. It will be a great benefit to the DSM in nanometer CMOS technologies. Besides, each terms under calibrated is perceived directly through a responding test signal. It make the calibration is more efficient than previous works.

A 2-2 cascaded DSM design case shown in Figure 3.4 is demonstrated here to explain our calibration scheme, which combines quantization noise leakage calibration and integrator calibration. This DSM consists of two feedforwad form loop filter with STF = 1.

ADC_1 and ADC_2 is the sub quantizor of the first and the second stage respectively. Similarly, DAC_1 and DAC_2 is the sub digital-to-analog converter (DAC) of the first and the second stage respectively. The j-th integrator is modeled as $H_j(z) = \alpha_j z^{-1} / \left(1 - \beta_j z^{-1}\right)$, $j \in \{1, 2, 3, 4\}$. For the linearization of DAC_1, a type of dynamic element matching skill called DWA is adopted. There are three calibration processors (CPs), CP_1 and CP_2 are used to calibrate the integrators of the fist stage. And CP_3 is use to trim NCF_2 for minimization of noise leakage. One out-of-band calibration signal c_1 is inserted before H_2 to check the first integrator. CP_1 process the first stage output y_1 and generate control signal T_1 to correct H_1. Another out-of-band calibration signal c_2 is added into the adder for two purposes; checking the second integrator and checking the noise leakage. ADC_3 converts the first stage output u_1 into a digital signal as CP_2 input. CP_2 then generates control signal T_2 to correct H_2. CP_3 process the cascaded DSM output y and generate control signal T_3 to correct NCF_2.

3.2.1 Integrator leakage Calibration

The first stage of Figure 3.4 is a second-order DSM. It includes two integrators with their poles at β_1 and β_2. Restoring the noise shaping capability of NTF_1 is the object here according to previous discussion. In another word, the noise leakage of a cascaded DSM could be reduced by adjusting β_1 and β_2 to the ideal placement 1. To treat the integrator leakage without interrupting the normal operation of DSM, we develop a calibration technique. This technique can detect the deviation of each integrator separately, and then correct the phase error by tunable SC integrators as Figure 2.6. In our scheme, the compensation feedback capacitance C_f is controlled by a digital signal $T[k]$, and consists of several unit step size capacitance ΔC_f. Such that,

$$C_{f1} = C_{f1,0} + \Delta C_{f1} \times T_1 \tag{3.4}$$

where T_1 is an integer, ΔC_{f1} is the C_f digital control step size and $C_{f1,0}$ is the C_f capacitance when $T_1 = 0$. From (2.13), the corresponding β_1 of H_1 is approximated by

$$\beta_1 = \beta_{1,0} + \Delta\beta_1 \times T_1 \tag{3.5}$$

where $\Delta\beta_1 \approx \Delta C_{f1}/C_{i1}$.

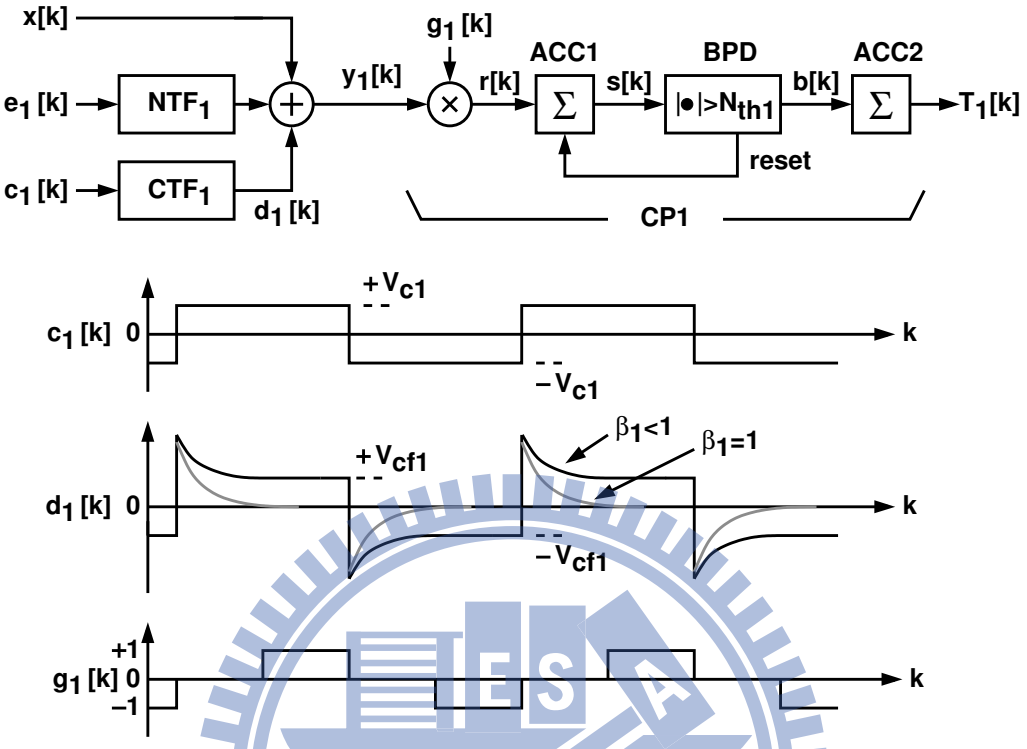


Figure 3.5: The first integrator calibration block diagram.

To calibrate β_1, a calibration signal c_1 is injected to the input of the 2nd integrator. A calibration processor, CP1, takes the ADC1 output y_1 and generates a control signal T_1 to adjust β_1 of the 1st integrator. The calibration signal c_1 is a square wave with f_{q1} frequency, V_{c1} amplitude, and duty cycle of D_{c1}. Calibration processor CP1 is shown in Figure 3.5, including a signal flow diagram of the fist integrator leakage calibration. At the CP_1 input, the digital stream y_1 is a summation of (1) the input x, (2) the ADC_1 quantization noise e_1 shaped by the noise transfer function NTF_1, and (3) the calibration signal c_1 shaped by the calibration-signal transfer function CTF_1, which is defined as $\mathrm{CTF}_1 = Y_1/C_1$.

The calibration signal $c_1[k]$ go through the CTF_1 filter, yielding $d_1[k]$. Thus, embedded in y, d_1 is the step response of CTF_1 triggered by $c_1[k]$. This step response settles toward a final value of

$$V_{cf1} = V_{c1} \times \mathrm{CTF}_1(1) \approx V_{c1} \times \frac{1-\beta_1}{\alpha_1} \tag{3.6}$$

V_{cf1} shows the same polarity as $1-\beta_1$. Thus, CP_1 can determine if β_1 is above or below

1 by detecting the polarity of V_{cf1}.

The CP1 correlates $y_1[k]$ with a triple-valued sequence $g_1[k] \in \{-1, 0, +1\}$. The $g_1[k]$ waveform is also illustrated in Figure 3.5. It has the same polarity as $c_1[k]$, but its value is set to 0 during the initial transition phase of c_1. Thus, the resulting product r contains only the valid V_{cf1} information. Following r is an accumulator (ACC1) followed by a BPD. Together they perform the AAR operation to extract V_{cf1} from r while removing the perturbations caused by x and e.

The above calibration scheme involves signal correlation and AAR operation. For this calibration to be effective, it requires that the calibration signal c_1 has no correlation with other signals in y_1, including the input x and the quantization noise e_1. Since c_1 is out of the signal band of x, there is no correlation between c_1 and x. Assume e_1 is a white noise. There are frequency components in e_1 that can have correlation with c_1. However, this correlation is weak since those frequency components have randomly varying phases. The effect of this correlation can be overcome by choosing a large BPD threshold N_{th1}.

The frequency of c_1 is determined out-of the signal bandwidth. Thus it would not disturb the normal operation of DSM during calibration process. Besides, $c_1[k]$ could be filtered by the following decimation filter. The triple-level $g_1]$ containing a null timing gap reduces the mistake of integrator leakage detection. A little digital circuits allow g_1 to be realized without an extra narrow band filter in previous works.

The standard deviation of β_1, $\sigma(\beta_1)$, is the evidence of how well the calibration information is acquired and how well the overall calibration performs. Figure 3.6 shows $\sigma(\beta_1)$ from simulations, where calibration design parameters of CP_1 are adopted. As N_{th1} increases, the disturbance caused by x and e_1 is reduced, yielding smaller $\sigma(\beta_1)$.

Since e_1 is shaped by NTF_1, it has larger frequency components at higher frequencies. Thus, a c_1 with a higher frequency has a stronger correlation with e_1, thus, requiring a larger N_{th1} to ensure an effective calibration. This is one reason we choose the c_1 frequency f_{c1} to be as low as possible. The other reason is to allow the transient response of d_1 to settle and allocate enough time for d_1-g_1 correlation.

To calibrate the 2nd integrator leakage, i.e. β_2, a calibration signal $c_2[k]$ is injected to the input of ADC1. The output of the 1st integrator u_1 is digitized by an extra ADC, ADC_3, and is converted into a digital stream y_3. ADC_3 yields the input of a calibration

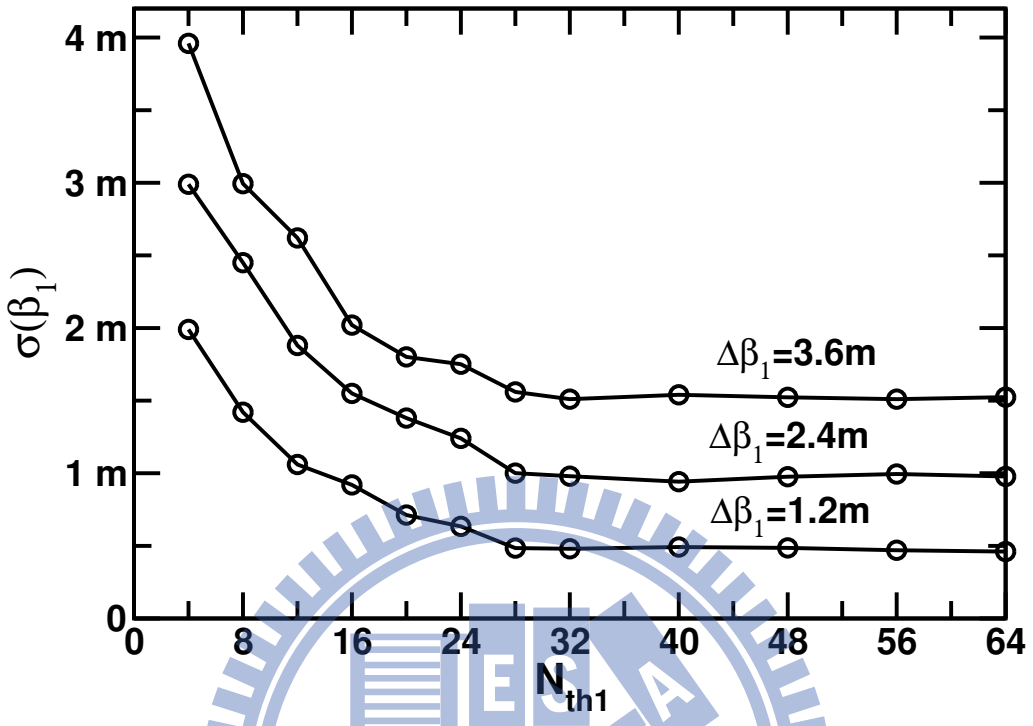


Figure 3.6: $\sigma(\beta_1)$ versus N_{th1} with different $\Delta\beta_1$.

processor CP2. CP_2 generates control signal T_2 to adjust β_2 of the 2nd integrator.

Figure 3.7 shows the calibration signal flow diagram. The ADC_3 output y_3 comprises (1) the ADC_3 quantization noise e_3, (2) the ADC_1 quantization noise e_1 shaped by CTF_2, and (3) the calibration signal c_2 shaped by CTF_2, where $CTF_2 = U_1/C_2$ is the transfer function from c_2 to u_1.

The calibration signal c_2 go through the CTF_2 filter, yielding d_2. Thus, embedded in w, d_2 is the step response of CTF_2 triggered by c_2. This step response settles toward a

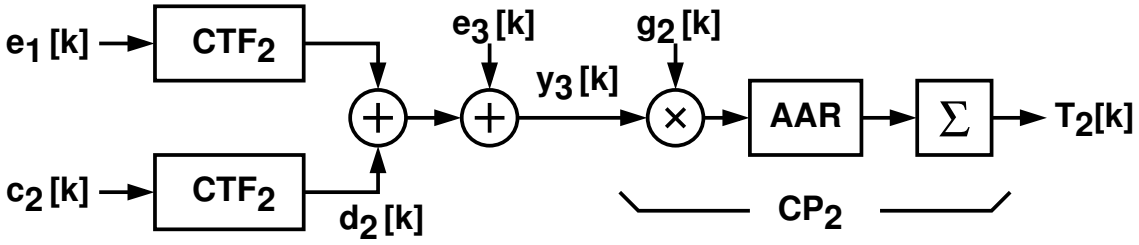


Figure 3.7: Signal flow diagram of the second integrator calibration.

final value of

$$V_{cf2} = V_{c2} \times \mathrm{CTF}_2(1) \approx V_{c2} \times -\frac{1-\beta_2}{\alpha_2} \tag{3.7}$$

The V_{cf2} value can be used to detect β_2. The CP2 operation is similar to the CP1 operation. Note that V_{cf2} is negative, while V_{cf1} is positive. Thus, referring to Figure 3.5, the polarity of g_2 is inverted.

In conclusion, the injecting scheme of $c_i[k]$ as well as the accessing scheme of β_i are the features of the proposed calibration scheme. This enables each integrator is corrected separately to optimize the capability of noise shaping. Furthermore, the compensation scheme is based on the polarity of $(1-\beta_j)$ instead of an extensive sweep or a blind trimming.

3.2.2 Noise leakage Calibration

Not only integration leakage calibration is necessary, the quantization noise leakage calibration is also necessary to maximize the SQNR of cascaded DSM. The noise leakage calibration processor CP_3 in Figure 3.4 controls T_3 to minimize the NTF in (3.3). Once $\mathrm{NCF}_1 = z^{-2}$ and NCF_2 are decided, as well as $\beta_1 = \beta_2 = 1$ is assumed, NLF becomes as

$$\mathrm{NLF} \approx \mathrm{NTF}_1 \cdot z^{-2} \cdot (1 - \alpha_1\alpha_2 \cdot G) \tag{3.8}$$

where α_j is the gain of j-th integrator, G is the gain factor. This equation indicates that, the minor $(1-\alpha_1\alpha_2 \cdot T_3)$ is, the minor noise leakage. We want $G \approx 1/(\alpha_1\alpha_2)$ to minimize NLF. As shown in Figure 3.4, the gain factor G is adjusted by a digital control T_3, such that

$$G = G_0 + \Delta G \times T_3 \tag{3.9}$$

where T_3 is an integer, ΔG is the control step size, and G_0 is the value of G when $T_3 = 0$. The control T_3 is generated from the calibration processor CP_3.

To calibrate T_3, the calibration signal c_2 is injected to the input of the ADC2 just likes the 2nd integrator leakage calibration. CP3 takes the DSM regular output y and generates a control signal T_3 to adjust the coefficient of NCF_2. Although such detect method is

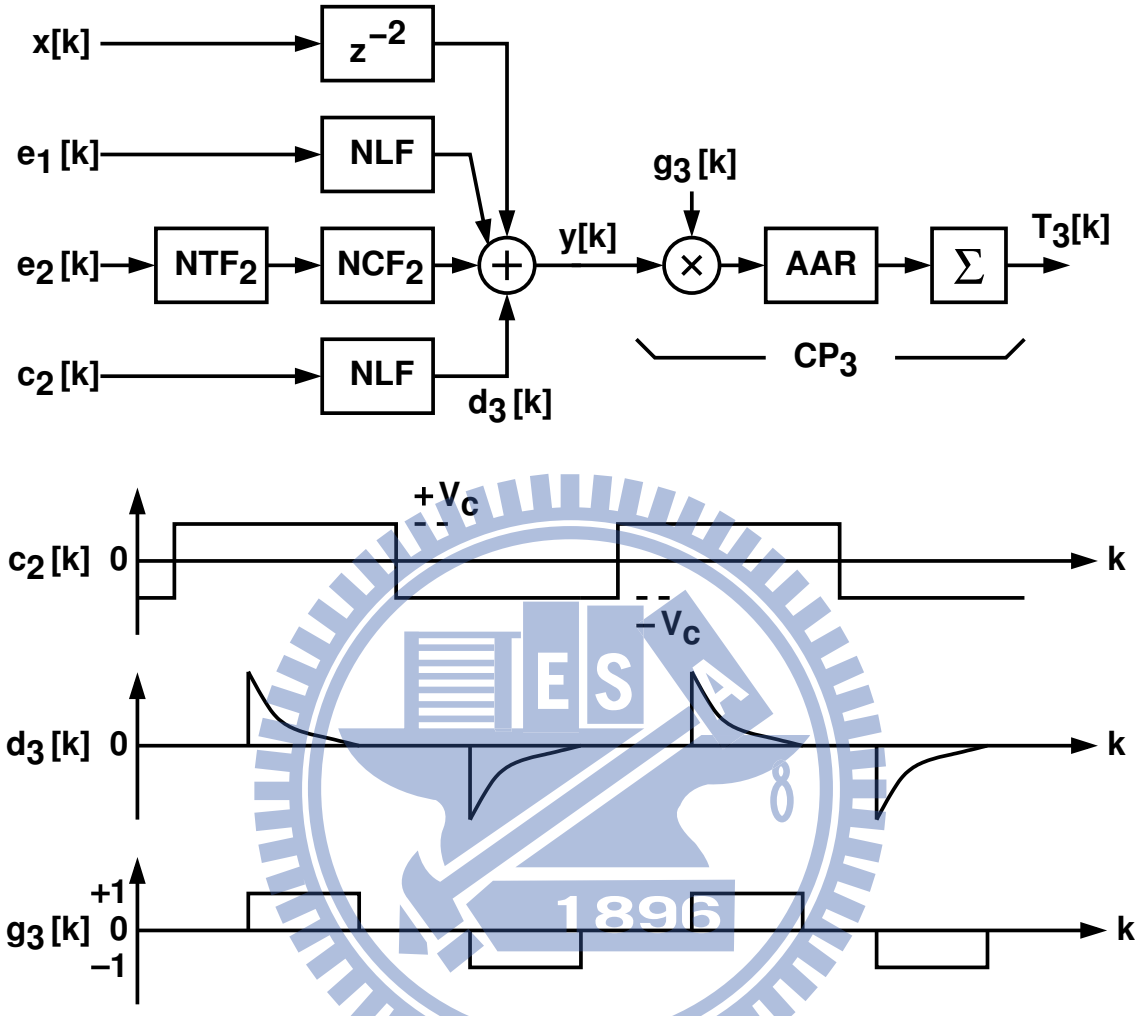


Figure 3.8: The noise leakage calibration block diagram.

widely used in the cascaded DSM, two major differences between previous works and this work. First, CP3 is based on AAR algorithm described in Section 3.2.1 rather than LMS algorithm. Second, only one coefficient is trimmed, which shorten the calibration time and reduce the calibration hardware.

Figure 3.8 shows the CP_3 block diagram and its input components. The DSM output y contains (1) the input x delayed by the filter $NCF_1 = z^{-2}$, (2) the quantization noise e_1 shaped by NLF, (3) the quantization noise e_2 shaped by $NTF_2 \times NCF_2$, and (4) the calibration signal c_2 shaped by NLF.

The calibration square wave c_2 excites the NLF filter, yielding d_3. Thus, embedded in

y, d_3 is the step response of NLF triggered by c_2. As expressed in (3.2), the NLF filter is a NTF_1 filter with a time delay of two clock cycles and a gain factor of $1-\alpha_1\alpha_2 G$. The NTF_1 filter is a high-pass filter with two zeros close to dc. Thus, the time-domain step response of NLF is a spike and settles toward zero. CP_3 detects the energy of those spikes and then adjusts G to eliminate the spikes. The operation of CP_3 is similar to those of CP_1 and CP_2. A triple-level sequence, $g_3 \in \{-1, 0, +1\}$ with a duty cycle of D_{g3}, is used to catch this spike before the CP3. Comparison with the integrator leakage calibration, the g_3 is valid at the middle segment of c_3 rather than at the end. Exactly speaking, the active region of g_3 overlaps the major area of the spikes. Then CP3 based on AAR algorithm extracts the polarity of $(1-\alpha_1\alpha_2 \cdot G)$, and controls T_3 to adjusts G as expressed in (3.9). The AAR in CP3 eliminates the perturbation caused by e_1, e_2, and x. The AAR has a BPD threshold of N_{th3}.

However, the amplitude of d_3 embedded in y is inconspicuous since the attenuation of NTF_1. This gives rise that, the quantization noise calibration takes 30X times more than the integrator leakage calibration. Fortunately, a predetermined T_3 could accelerate the quantization noise calibration. This is achieved by estimating $1/\alpha_1\alpha_2$ during the integrator leakage calibration. As the $T_1[k]$ and $T_2[k]$ hint the opamp dc gain, then α_1 and α_2 are predictable through the predetermined capacitance ratio. Recall the tunable SC integrator in Figure 2.6, if C_{s_j} denotes the sampling capacitance of j-th integrator, C_{i_j} denotes the integrating capacitance of j-th integrator, $C_{f_j} = T_j \cdot \Delta C_f$ denotes the compensation capacitance of j-th integrator, and $j \in 1, 2$.

We choose a G_0 that is close to $1/(\alpha_1\alpha_2)$, which can be calculated as

$$G_0 = \frac{C_{i1}}{C_{s1}}\frac{C_{i2}}{C_{s2}}\left(1+\frac{C_{f1}}{C_{s1}+C_{f1}}+\frac{C_{f1}}{C_{i1}}\right)\left(1+\frac{C_{f2}}{C_{s2}+C_{f2}}+\frac{C_{f2}}{C_{i2}}\right) \tag{3.10}$$

where C_{i1}, C_{s1}, and C_{f1} are the capacitors in the integrator H_1, and C_{i2}, C_{s2}, and C_{f2} are the capacitors in the integrator H_2. Capacitors C_{f1} and C_{f2} are functions of control signals T_1 and T_2 respectively.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Chapter 4

A 81 dB DR 16.67 MHz BW Cascaded DSM

This chapter describes a DT DSM that combines low-complexity circuits and digital calibration to achieve wide bandwidth and large dynamic range. It is a MASH modulator consisting of two cascaded second-order loops. The number of the quantization levels of its internal ADCs and DACs is only 4. The internal integrators are realized with high-speed opamps with a dc gain of only 10. Two different types of digital calibrations are applied. We first employ the integrator leakage calibration to correct the poles of the integrators. We then use the noise leakage calibration to minimize the quantization noise from the first loop leaking to the DSM combined output. The noise leakage calibration also relaxes the component matching requirements for the MASH structure. Since each calibration adjusts only one parameter, it is robust. All calibration can proceed in the background without interrupting the normal DSM operation. The calibration processors are simple digital circuits. They do not include any complex filter. The modulator was fabricated using a 65 nm CMOS technology. It has a sampling rate of 1.1 GHz and an input bandwidth of 16.67 MHz with an oversampling ratio (OSR) of 33. The measured signal-to-noise-and-distortion ratio (SNDR) and dynamic range (DR) are 74.32 dB and 81 dB respectively. The chip consumes 94 mW from a 1 V supply. The active area is 0.33×0.58 mm^2.

The rest of this chapter is organized as follows. Section 4.1 describes the DSM ar-

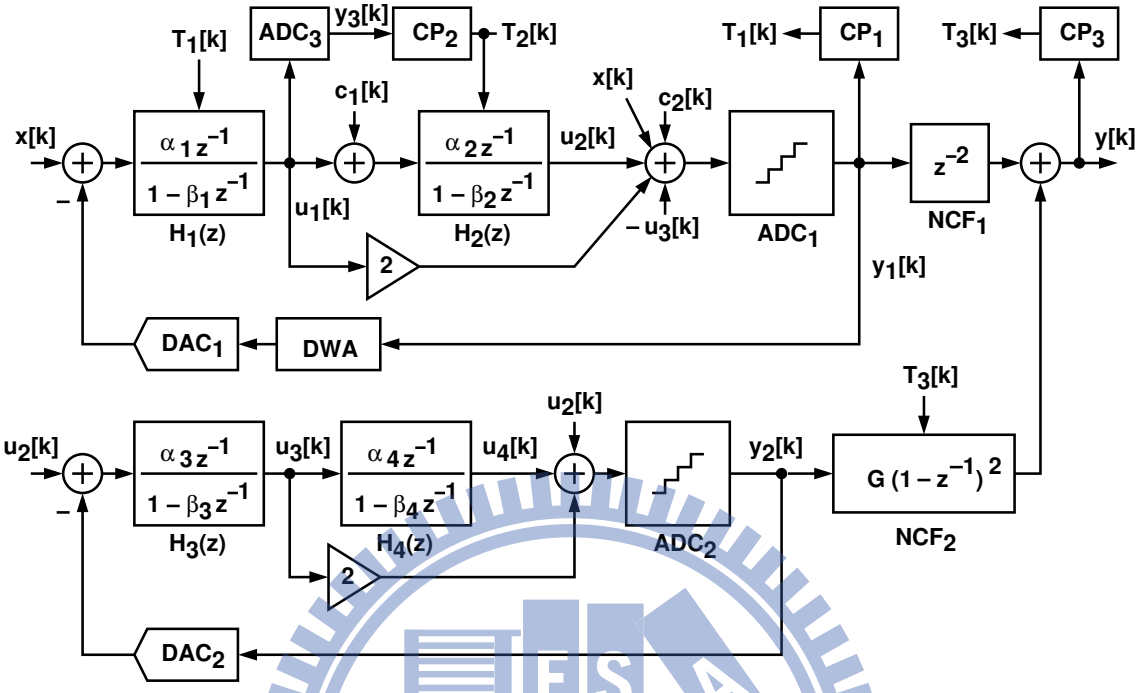

Figure 4.1: A 4th-order MASH DSM with digital calibrations.

Table 4.1: Integrator variations due to opamp dc gain A_0.

A_0	α_1	α_2	α_3	α_4	β_1	β_2	β_3	β_4
∞	0.410	0.455	1	1	1	1	1	1
10	0.359	0.396	0.833	0.833	0.964	0.957	0.917	0.917

chitecture and its design parameters. The integrator leakage calibration and quantization noise leakage calibration are also included. Section 4.2 describes the design of the crucial circuits. Section 4.3 shows the experimental results. Section 4.4 draws conclusions.

4.1 DSM Architecture

Figure 4.1 shows the reported 4th-order DT DSM architecture. In its core is a MASH modulator consisting of two stages of second-order modulation loops. There are 4 integrators, H_1 to H_4. Each integrator is modeled with a gain factor α and a pole β. Table 4.1 shows the design values for α and β. For an ideal integrator with an opamp dc

gain $A_0 = \infty$, $\beta = 1$. There are two analog-to-digital converters (digitizers), ADC_1 and ADC_2. Each one is a 2-bit flash ADC comprising 3 comparators. There are two corresponding digital-to-analog converters, DAC_1 and DAC_2. DAC_1 covers an output range of $\pm V_R$, while DAC_2 covers an output range of $\pm(1/2)V_R$. The adders preceding the two ADCs are passive switched-capacitor circuits. In the first loop, a data-weighted averaging (DWA) dynamic element matching logic [39] is added before DAC_1 to mitigate its conversion errors. DAC_1 has 4 analog output levels at $\{\pm(1/3)V_R, \pm V_R\}$ covering an output range of $2V_R$. DAC_2 has 4 output levels at $\{\pm(1/6)V_R, \pm(1/2)V_R\}$, covering an output range of V_R. The thresholds of ADC_1 are $\{0, \pm(2/3)V_R\}$. The thresholds of ADC_2 are $\{0, \pm(1/3)V_R\}$. A full-scale sine-wave input is defined as $V_R \sin \omega_i t$, which has a signal power of $P_S = (1/2)V_R^2$. In our design, $V_R = 1$ V. The use of multi-bit ADCs leads to smaller quantization errors and stability improvement. The combination of filter feedforward and multi-bit ADCs relaxes the linearity and voltage swing requirements for the analog circuitry [40].

As shown in Figure 4.1, the raw digital outputs from the two modulation loops are y_1 and y_2 respectively. Due to the use of feedforward, both loops have a signal transfer function (STF) of 1, i.e, $\text{STF}_1 = Y_1/X = 1$ and $\text{STF}_2 = Y_2/U_2 = 1$. The two digitizers ADC_1 and ADC_2 introduce quantization noises, denoted as e_1 and e_2 respectively. The two noise transfer functions are defined as $\text{NTF}_1 = Y_1/E_1$ and $\text{NTF}_2 = Y_2/E_2$. NTF_1 is a function of H_1 and H_2, while NTF_2 is a function of H_3 and H_4. Applying the α and β parameters listed in Table 4.1 with an opamp dc gain $A_0 = \infty$, the resulting noise transfer functions are $\text{NTF}_1 = \left(1 - z^{-1}\right)^2 / \left(1 - 1.18z^{-1} + 0.37z^{-2}\right)$ and $\text{NTF}_2 = \left(1 - z^{-1}\right)^2$. Two digital noise cancellation filters, NCF_1 and NCF_2, combine the two outputs y_1 and y_2 to generate the final DSM output y, which can be expressed as

$$Y = X \times \text{NCF}_1 + E_1 \times \text{NLF} + E_2 \times \text{NTF}_2 \cdot \text{NCF}_2 \tag{4.1}$$

where the noise leakage transfer function NLF is defined as

$$\text{NLF} = \frac{Y}{E_1} = \text{NTF}_1 \times (\text{NCF}_1 - H_1 \cdot H_2 \cdot \text{NCF}_2) \tag{4.2}$$

If we choose the digital filters $\text{NCF}_1 = z^{-2}$ and $\text{NCF}_2 = G\left(1 - z^{-1}\right)^2$ with $G = 1/(\alpha_1\alpha_2) \approx 5.36$, then, in the DSM combined output y, e_1 is completely eliminated, and e_2 is shaped by a 4th-order function $\left(1 - z^{-1}\right)^4$.

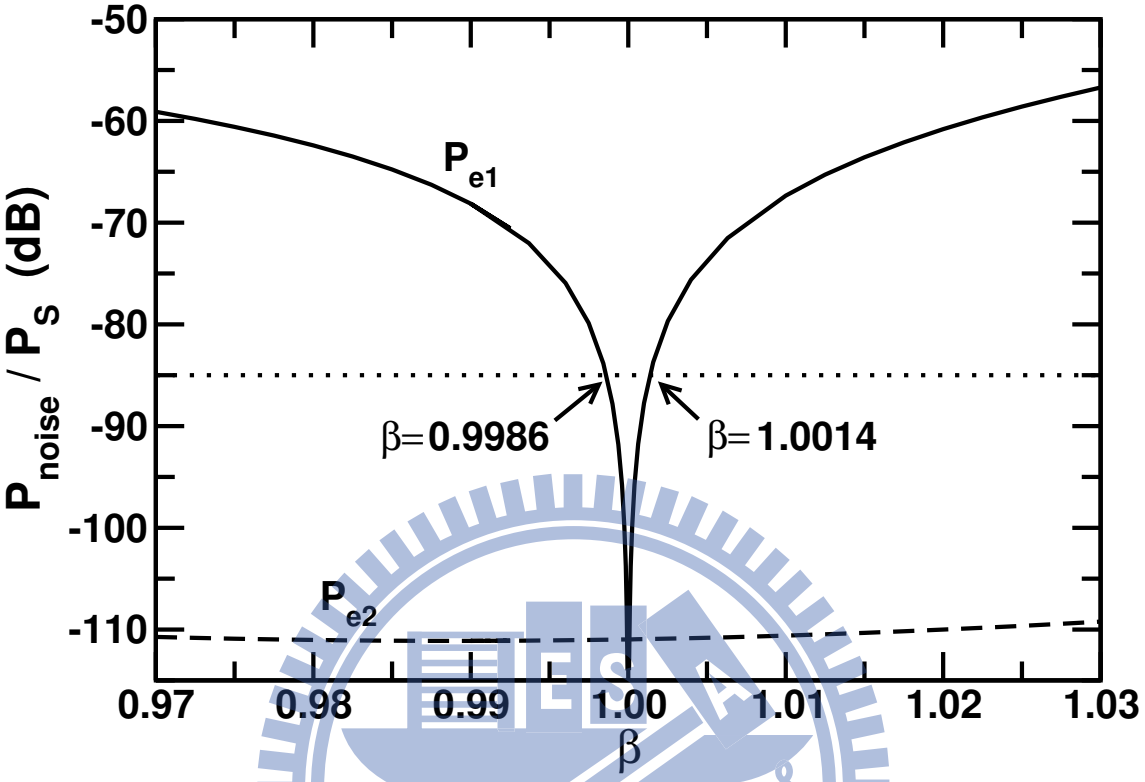

Figure 4.2: Effect of integrator pole β on the noises e_1 and e_2 in the DSM output.

In the wide-bandwidth applications, the DSM uses high-speed opamps to implement the integrators. In our design, the opamps in the integrator configuration have an unity-frequency of 6 GHz, but have a dc gain A_0 of only 10. Table 4.1 shows the effect of A_0 on the integrators. Their gain factors α change and their poles β become less than 1. When placing these integrators in the DSM, the corresponding NTF exhibits a degraded capability of suppressing quantization noise in the signal band. Besides the A_0 effect on α and β, the capacitor mismatch in an integrator also causes a change in α. Both the α and the β variations yield NLF $\neq 0$. This phenomenon is called noise leakage, when portion of e_1 leaks out to the DSM output y.

Figure 4.2 shows the effect of β on the noises e_1 and e_2 appearing in the output y. It plots the ratio of noise power to the signal power of a full-scale sine-wave input, $P_S = 0.5V_R^2$. The noise power includes only the frequency components within the signal band. An OSR of 33 is assumed. P_{e1} is the noise power of e_1 in y and P_{e2} is the noise power of e_2 in y. It is assumed all integrators have the same β. In our design, P_{e2} is a weak function

of β. It can be neglected if the expected signal-to-noise ratio (SNR) of the entire DSM is 80 dB. On the other hand, P_{e1} is a strong function of β. It requires $|1-\beta| < 1.4 \times 10^{-3}$, so that P_{e1} is 85 dB below P_S.

From (4.1) and (4.2), and since $\mathrm{NCF}_1 = z^{-2}$ is a simple delay, the digital filter NCF_2 must match the analog integrators H_1 and H_2 to reduce P_{e1}. The filter NCF_2 can become adaptive to accommodate the variations in H_1 and H_2 [38]. However, if the β parameters in H_1 and H_2 are away from 1, the calibration for NCF_2 are complex. In our design, we first calibrate integrators H_1 and H_2 to simplify the requirement for NCF_2. We then calibrate NCF_2 to minimize the NLF of (4.2). We apply the integrator leakage calibration described in Section 3.2.1 to integrators H_1 and H_2 to recover their capability of noise suppression and make their β approximate 1. We simplify the second noise cancellation filter as $\mathrm{NCF}_2 = G\left(1-z^{-1}\right)^2$, which has only one adaptive parameter G. We then apply the noise leakage calibration described in Section 3.2.2 to find G. All calibrations are operated in the background without interrupting the normal DSM function.

4.1.1 Dithering

The ADC_1 quantization noise e_1 may contain harmonic tones or idle tones. These tones may show up in the signal band of the DSM output y. The dithering can effectively decorrelate and white the quantization error, because the power of spurs caused by harmonics and idle tones are spread over the whole spectrum. Generally speaking, a second-order or higher-order DSM do not sound tonal because the small thermal noise are enough to randomize the quantization noise. But these tones may correlate with the calibration signals introduced by the aforementioned calibrations, corrupting the calibration process. For the accuracy of calibration, the first stage DSM is dithered to randomize e_1.

The drawback of dithering a single stage DSM is the increment of in-band noise power. A shaped dithering or a subtractive dithering is preferable to lessen the cost. A cascaded DSM, however, bears a dithered first stage due to noise cancellation. If the second stage adopts the feedforward structure likes Figure 4.1, wherein the third integrator output $-u_3$ is a first-order shaped random noise source inherently. So the injecting $-u_3$ into the ADC1 accomplishes the dithering of first stage without an extra pseudo random number genera-

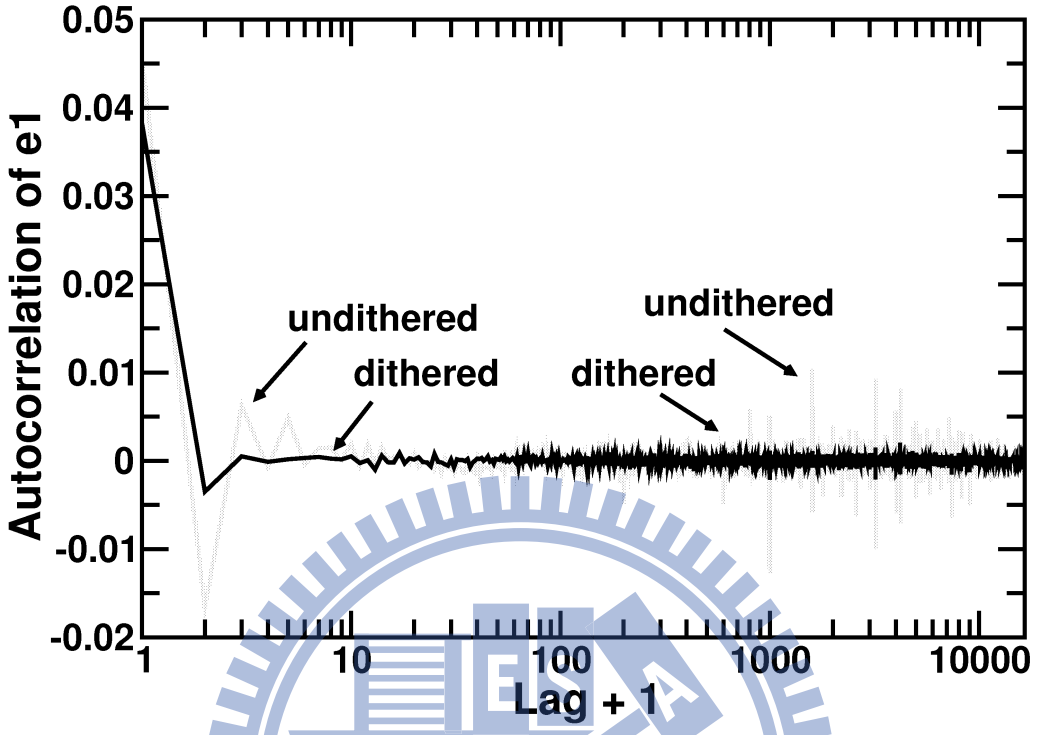

Figure 4.3: Autocorrelatoin of the first stage quantization noise.

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The figure Figure 4.3 shows the auto correlation of the e_1. Without dithering, the auto correlation ripples at the low lag, and appears several spurs at the high lag. With dithering, the auto correlation resembles a delta function which is the statistical character of a white noise. In addition, because the first stage of Figure 4.1 is feedforward. The first integrator output u_1 contains shaped e_1 only. As long as $e1$ is input-independent by dithering, the requirement of integrator linearity relax further. The spectrum of u_1 whether dithering is enabled or not are shown in Figure 4.4.

The dithering signal is not included in the following analyses since its effect is minuscule.

4.1.2 Calibration of Integrator Leakage

As shown in Figure 4.1, the integrator leakage calibration is applied to the integrators H_1 and H_2 of the first modulation loop. Consider the calibration of the first integrator

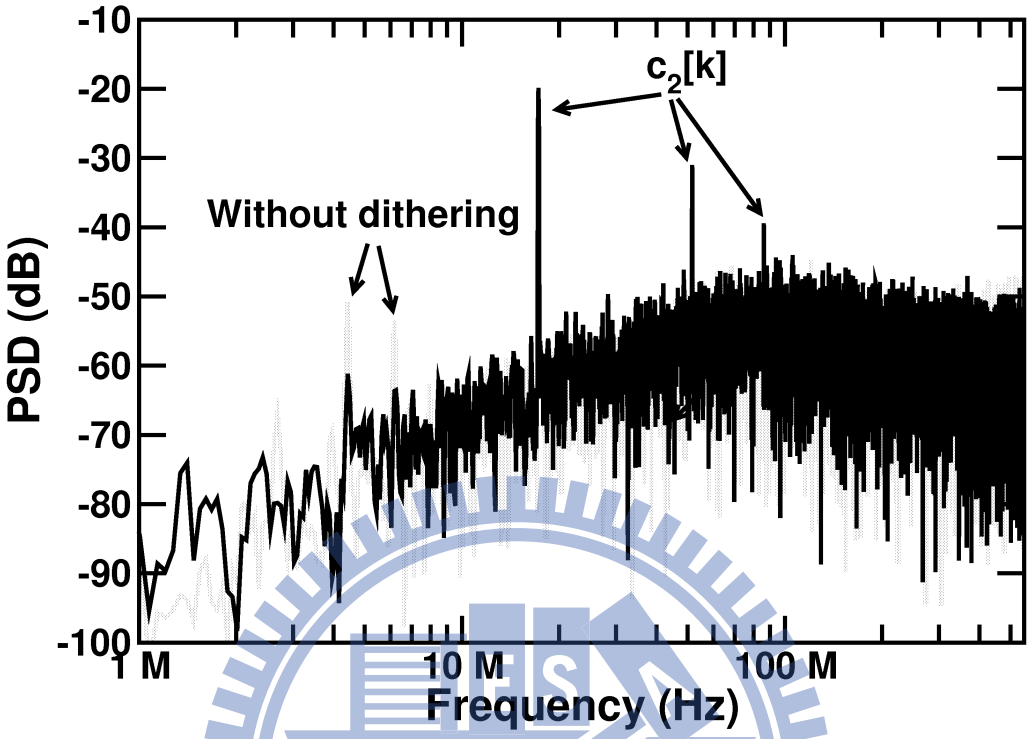


Figure 4.4: Spectra of the first integrator output.

H_1. The C_f capacitor in H_1 is controlled by a digital signal T_1. The control signal T_1 is generated from a calibration processor, CP_1. To calibrate H_1, a calibration signal c_1 is added to the input of the second integrator H_2. CP_1 receives the ADC_1 output y_1, and detects the β_1 of H_1 from the c_1-related signal embedded in y_1. It then adjusts T_1 to make β_1 approximate 1.

As described in Section 3.2.1, the calibration square wave c_1 triggers a step response d_1. Let c_1 have a frequency of f_{c1}, a corresponding period of $T_{c1} = 1/f_{c1}$, and a duty cycle of 50%. We want f_{c1} to be larger the signal bandwidth so that it can be removed by the decimation filter following the DSM. We also want $T_{c1}/2$ to be longer than the time required for d_1 to settle so that its final value V_{cf1} can be extracted by correlating d_1 with g_1. In our design, $T_{c1} = 64T_s$ and $D_g = 1/2$, so that, in each d_1 transient, d_1 has a period of 16 clock cycles to settle before g_1 is activated for 16 clock cycles. The frequency of c_1 is $f_{c1} = f_s/64$. As long as OSR > 32, the frequency components of d_1 is outside the signal band.

The injection of c_1 increases the signal ranges of the integrators' outputs, u_1 and u_2.

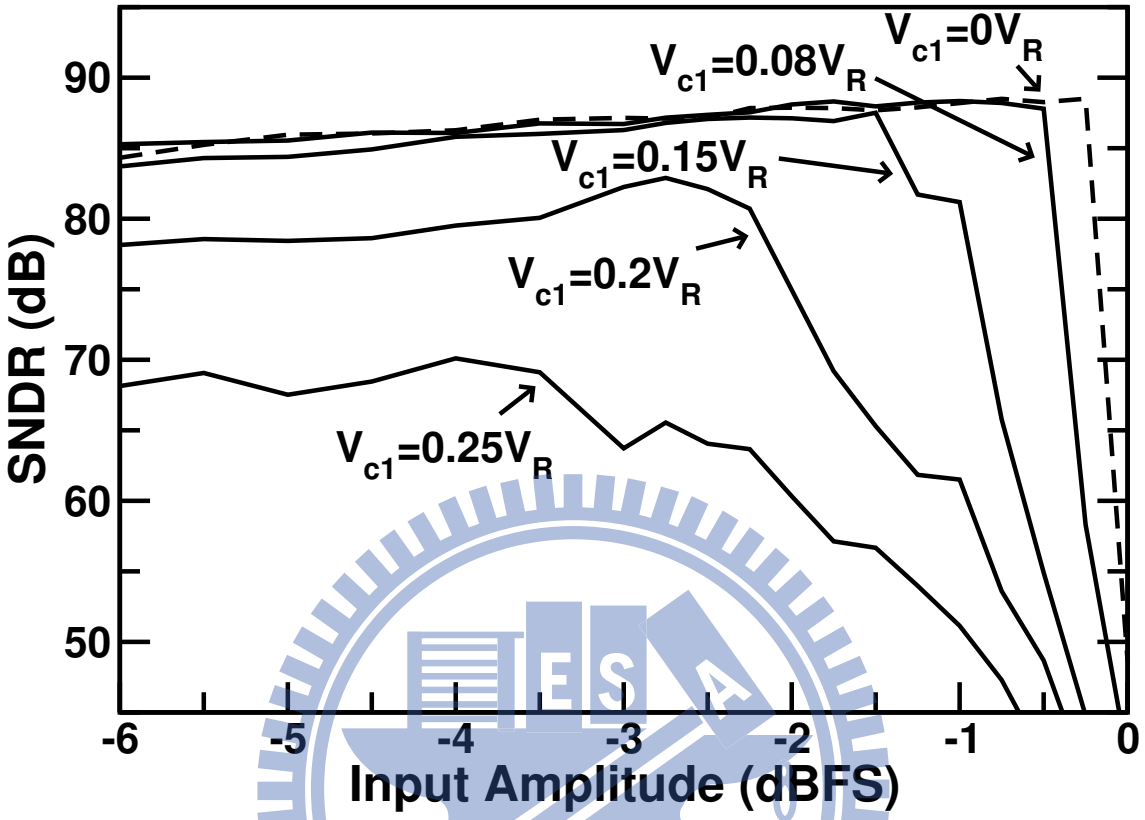


Figure 4.5: DSM SNDR versus input level at various V_{c1} values.

A larger u_1 and lager u_2 raise the nonlinearity effect of the integrators. A large u_2 may even overload the second modulation loop, yielding large e_2. Thus, an increase in the c_1 amplitude, V_{c1}, degrades the SNDR of the DSM. On the other hand, from (3.6), if V_{c1} is too small, the corresponding V_{cf1} is too small to ensure a robust calibration.

We choose V_{c1} by using simulations. Figure 4.5 shows the resulting SNDR of the MASH DSM versus the input amplitude at different V_{c1} values. In the simulations, all integrators are assumed to have a pole at $\beta = 1$. Without the injection of c_1, the peak SNDR of the entire DSM is 88.5 dB occurring at an input level of -0.25 dBFS. The peak SNDR is degraded by more than 6 dB if $V_{c1} > 0.2V_R$. For our design, we choose $V_{c1} = 0.08V_R$. The resulting peak SNDR is maintained at 88 dB. Without c_1, the signal standard deviation for u_1 and u_2 are $\sigma(u_1) = 0.085V_R$ and $\sigma(u_2) = 0.075V_R$ respectively. When c_1 with $V_{c1} = 0.08V_R$ is injected, $\sigma(u_1)$ and $\sigma(u_2)$ become $0.115V_R$ and $0.160V_R$ respectively.

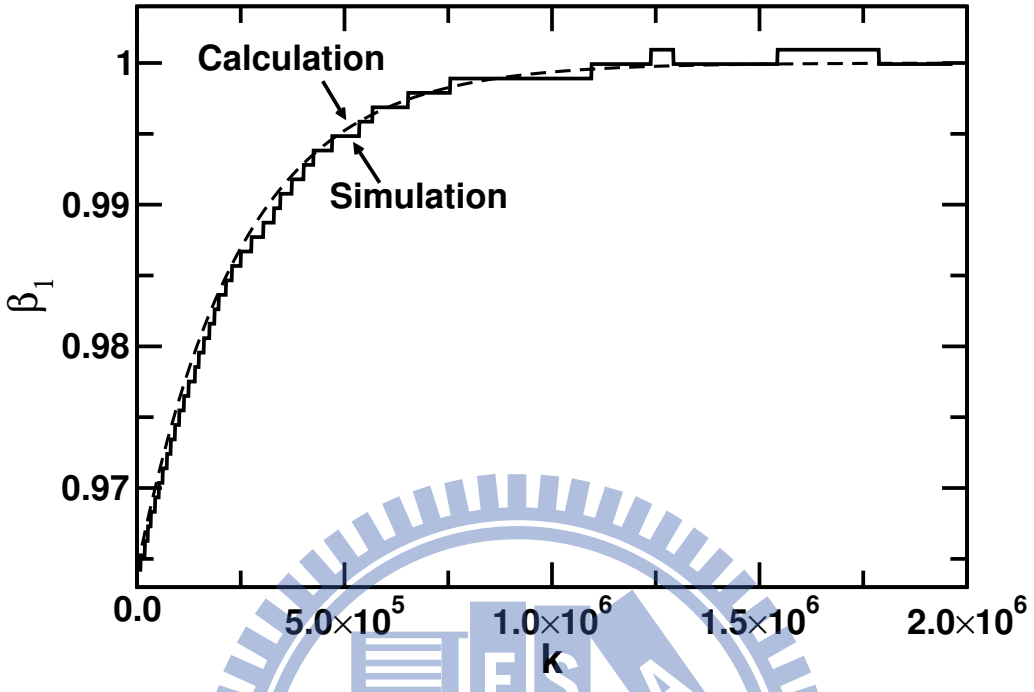


Figure 4.6: $\beta_1[k]$ transient response.

As shown in Figure 4.2, the deviation of β from 1 increase the noise power P_{e1}. we want $3\sigma(\beta) < 1.4 \times 10^{-3}$ so that P_{e1} is 85 dB below P_S. In this design, we choose $\Delta\beta_1 = 1.126 \times 10^{-3}$ and $N_{th1} = 32$, yielding a time constant $\tau_1 = 2.481 \times 10^5$. If the clock rate $f_s = 1/T_s = 1$ GHz, the physical time constant is $\tau \times T_s = 248.1$ μsec. The transient response of H_1 calibration is shown in Figure 4.6.

Referring to Figure 4.1, to calibrate the second integrator H_2, a calibration square wave c_2 is added to the input of ADC_1. An additional digitizer ADC_3 is added to convert u_1, the output of the first integrator H_1, into a digital stream y_3. ADC3 is also a flash ADC, comprising 3 comparators with thresholds at $\{0, \pm(1/9)V_R\}$. The calibration processor CP_2 receives y_3, and generates T_2 to adjust the β_2 of H_2. The control signal T_2 adjusts β_2 by controlling the C_f capacitor in H_2. The control mechanism is similar to (3.4) and (3.5).

The calibration signal c_2 is a square wave with f_{c2} frequency, V_{c2} amplitude, and 50% duty cycle. The V_{cf2} expressed in (3.7) is extracted by CP_2 to detect the polarity $1-\beta_2$. The operation of CP_2 is identical to that of CP_1. For our design, c_2 has a period of $T_{c2} = 64T_s$ and an amplitude of $V_{c2} = 0.11V_R$. The duty ratio of g_2 is $D_{g2} = 1/2$. The BPD threshold

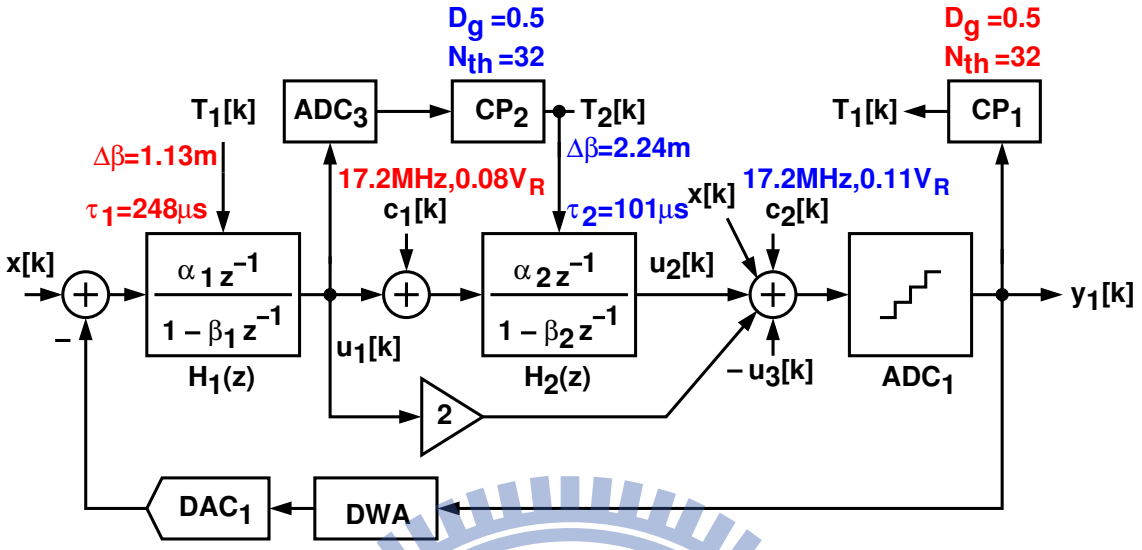


Figure 4.7: The integrator-leakage calibration of the first loop in the DSM.

for the AAR is $N_{th2} = 32$. The β_2 control step size is $\Delta\beta_2 = 2.24\times10^{-3}$. The above design parameters result in a calibration time constant of $\tau_2 = 1.013\times10^5$ or $\tau_2 \times T_s = 101.3$ μsec with a 1 GHz clock. When the calibration signal c_2 is injected into the DSM, the signal standard deviation for u_1 and u_2, are $\sigma(u_1) = 0.095V_R$ and $\sigma(u_2) = 0.120V_R$ respectively.

The H_1 calibration and the H_2 calibration are executed sequentially, and are summarized as Figure 4.7. They do not interfere with each other. The operations are robust. The calibration signals c_1 and c_2 are easy to generate. The calibration processors CP_1 and CP_2 can be realized with simple digital circuits. They use the masking signals g_1 and g_2 to extract the calibration data. Complex filter is not needed.

4.1.3 Calibration of Noise Leakage

During the integrator leakage calibration of H_2, a calibration square wave c_2 is added to the input of ADC_1. Similar to the ADC_1 quantization noise e_1, c_2 passes through NLF and appears in the DSM combined output y. Thus, CP_3 can observe y, extract the c_2-related signal in y, and then adjust G through T_3 to make c_2 disappear from y.

As described in Section 3.2.2, CP_3 detects the energy of those residue spikes and then adjusts G to eliminate the spikes. The operation of CP_3 is similar to those of CP_1 and CP_2. For our design, the duty ratio of g_3 is $D_{g3} = 0.25$. The BPD threshold for the AAR is

$N_{th3} = 96$. The G control step size is $\Delta G = 0.25$. The above design parameters result in a calibration time constant of $\tau_3 = 6.514 \times 10^5$ or $\tau_3 \times T_s = 651.4$ μsec with a 1 GHz clock. This time constant is larger than the time constants for the integrator leakage calibration, τ_1 and τ_2.

During the power-on phase, CP_3 is reset and $T_3 = 0$ and $G = G_0$. To reduce the initial calibration convergence time, we choose a G_0 that is close to $1/(\alpha_1\alpha_2)$, which can be calculated as (3.10). The power-on sequence for calibration is described as follows. The DSM first executes the H_1 calibration for $4\tau_1 T_s \approx 1$ msec, and then the H_2 calibration for $4\tau_2 T_s \approx 0.4$ msec. Afterward, the DSM uses the values of T_1 and T_2 from the above calibrations to estimate C_{f1} and C_{f2}, and applies (3.10) to calculate G_0. The DSM then activates CP3 every time when the H_2 calibration is in progress.

4.2 Circuit Design

This section describes the circuit design to implement the DSM of Figure 4.1. The DSM is to be fabricated using a 65 nm CMOS technology. The supply voltage is 1 V. The DSM is expected to achieve a sampling rate higher than 1 GS/s and a dynamic range larger than 80 dB.

4.2.1 Operational Amplifiers

Figure 4.8 shows the schematic of the opamps used in the integrators. It is a two-stage class-AB amplifier without frequency compensation [41]. All MOSFETs are sized with the minimum channel length of 60 nm. The amplifier has a dc voltage gain of 10. Its dominant poles are located at the output nodes $V_{o,p}$ and $V_{o,n}$. When configured as an integrator, the opamp achieves an unity-gain frequency of 6 GHz and a phase margin of 63 degrees. The voltages V_{CMF1} and V_{CMF2} are generated by two separate continuous-time common-mode feedback (CMFB) circuits. The complementary CMFB circuits are shown in Figure 4.9 and are suitable for low-voltage high-swing application [42]. Each CMFB contains additional voltage amplification to increase the loop gain and improve the common-mode rejection against power-line fluctuation. The push-pull output stage also

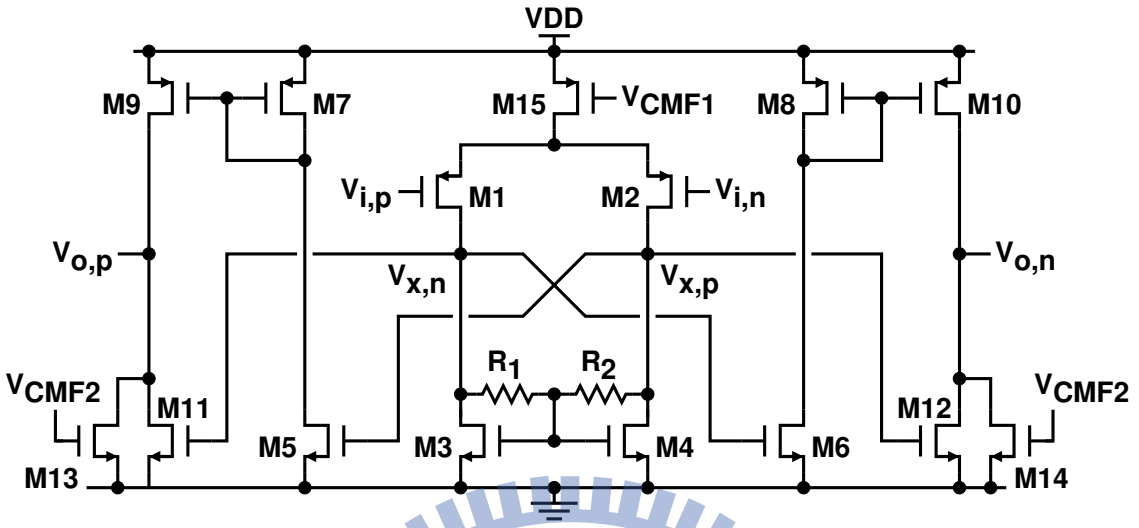


Figure 4.8: Operational amplifier schematic.

provides additional common-mode rejection.

4.2.2 Integrators

The opamp is used to realize the fully-differential version of the integrator shown in Figure 4.10. The input common-mode voltage of the opamp is set to $V_{DD}/4$. The analog switches connected to the opamp's inputs are nMOSFETs with boosting gate control [41] as shown in Figure 4.11. Consider the integrator H_1. Its ideal value of the gain factor α_1 is determined by the capacitor ratio C_{s1}/C_{i1}.

The control signal T_1 from the calibration processor CP_1 adjusts the pole β_1 of H_1 by varying the capacitor C_{f1}, as described by (2.13), (3.4), and (3.5).

In our design, the thermal noise from the first integrator H_1 is the dominant source of thermal noise. Its total noise power showing up in the signal band of the DSM output y is about $(14/3)(kT/C_{s1})$ [20]. We choose $C_{s1} = 1.9$ pF so that the power of this thermal noise in the signal band, P_θ, is 90 dB below the power of a full-scale sine-wave input, P_S. By using the periodic noise analysis of the circuit simulator, we estimate that the total P_θ of the entire DSM is 86 dB below P_S.

The control signal T_1 adjusts the capacitor C_{f1} in the integrator H_1 as described by (3.4), thus varying β_1 as described by (3.5). The capacitor step size ΔC_{f1} determines the

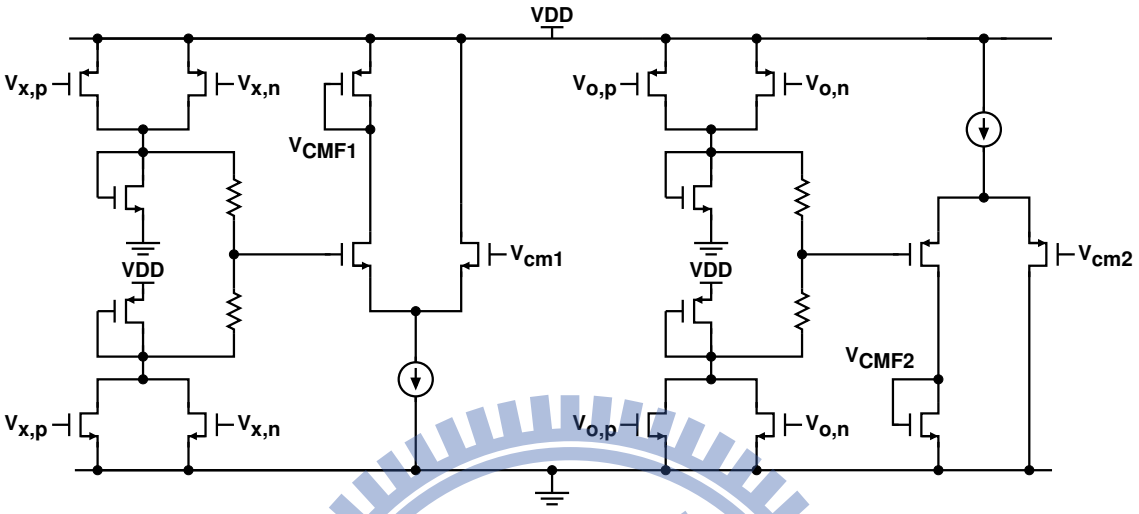


Figure 4.9: Common-mode feedback schematic.

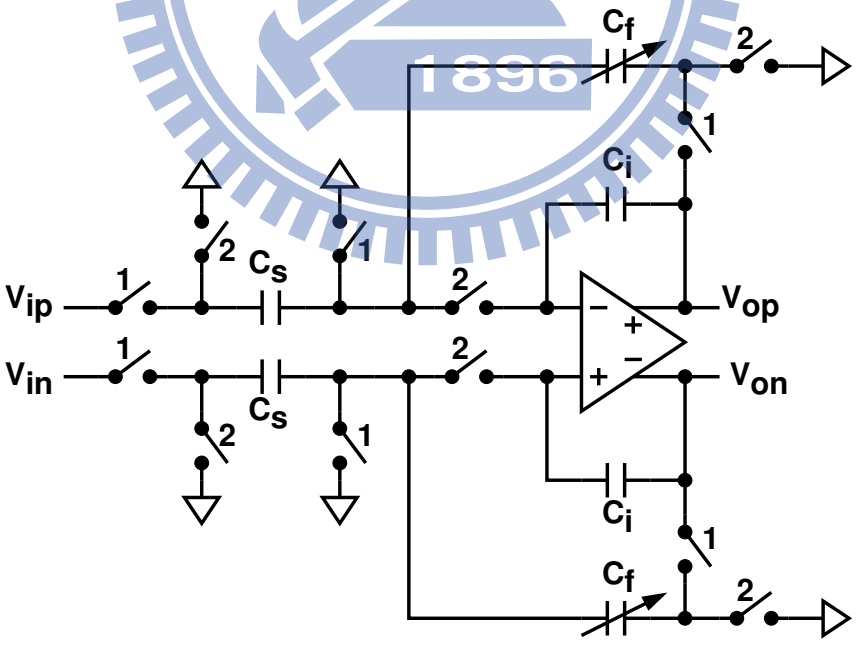


Figure 4.10: Differential schematic of the first integrator.

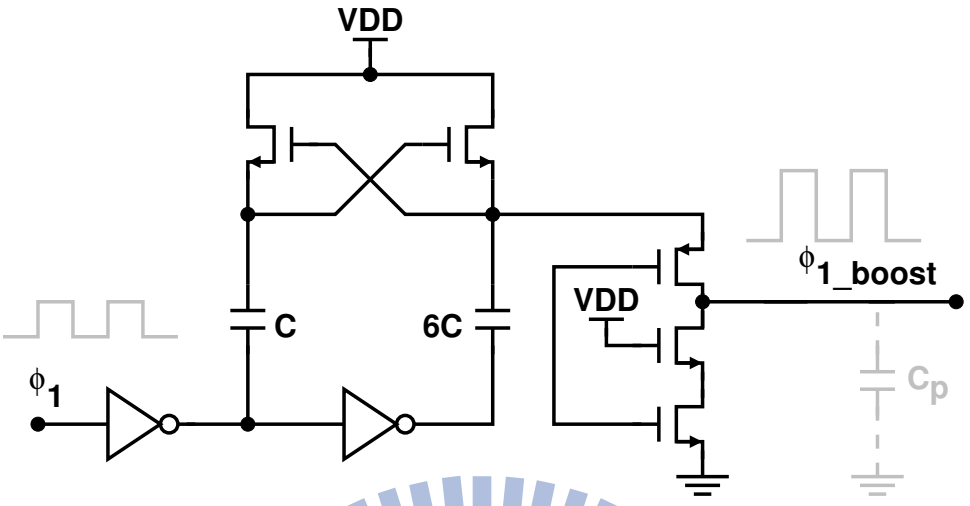


Figure 4.11: Schematic of clock boosting.

Table 4.2: Capacitor size of Integrators.

C_{s1}	C_{i1}	C_{s2}	C_{i2}	C_{s3}	C_{i3}	C_{s4}	C_{i4}
1928 fF	4707 fF	964 fF	2115 fF	294 fF	294 fF	294 fF	294 fF

step size $\Delta\beta_1$. From Section 3.2.1, we want $\Delta\beta_1 = 1.126\times10^{-3}$. In our design, T_1 is a 6-bit control signal, and C_{f1} can be varied from 0 fF to 378 fF with a step size $\Delta C_{f1} = 6$ fF. As a result, β_1 can be varied from 0.964 to 1.028 with a step size $\Delta\beta_1 \approx 1.13\times10^{-3}$. Similarly, the CP_2 output T_2 controls the capacitor C_{f2} in the integrator H_2. The signal T_2 is a 5-bit control signal, and C_{f2} can be varied from 0 fF to 186 fF with a step size $\Delta C_{f2} = 6$ fF. As a result, β_2 can be varied from 0.957 to 1.027 with a step size $\Delta\beta_2 \approx 2.24 \times 10^{-3}$.

Summarize above discussion and the coefficients shown in Table 4.1, the capcitance of each integrator are listed in Table 4.2. Every capacitors are realized by the MOM capacitor.

4.2.3 Adder and DAC

Figure 4.12 shows the schematic of DAC_1 and the adder preceding ADC_1 in the first modulation loop of the DSM. Only one side of the fully-differential circuit is depicted. The adder is a passive switched-capacitor circuit [43], comprising 3 capacitors C_{a1} to C_{a3}.

The capacitors have an identical capacitance of 60 fF. During $\phi_2 = 1$, the preamplifier in the comparator is reset with its input shorted to its output. Meanwhile, the inverse of u_1 from the integrator H_1, the output u_3 from the integrator H_3, and a comparator threshold voltage V_{th1} are sampled onto capacitors C_{a1}, C_{a2}, and C_{a3} respectively. The input offset of the preamplifier is also stored on the capacitors. During $\phi_1 = 1$, the output u_1 from H_1, the output u_2 from H_2, and the modulator input x are connected to the capacitors respectively, yielding a differential voltage $x + 2u1 + u2 - u3 - V_{th1}$ at the input of the preamplifier. Upon the falling edge of ϕ_1, the latch in the comparator compares $V_a = x + 2u1 + u2 - u3$ with the threshold V_{th1}, generating a single-bit digital output D_1. There are 3 comparators in ADC_1. They compare V_a with three different thresholds, which are $V_{th1} = -(2/3)V_R$, $V_{th2} = 0$, and $V_{th3} = +(2/3)V_R$.

All the integrators in this DSM sample their input during $\phi_1 = 1$ and perform the integration during $\phi_2 = 1$. As shown in Figure 4.12, the input sampling capacitor C_{s1} of the integrator H_1 is divided into 3 identical capacitors C_{s1a}, C_{s1b}, and C_{s1c} to implement the 2-bit equally-weighted DAC_1. During $\phi_1 = 1$, the input x is sampled onto all 3 capacitors. During $\phi_2 = 1$, the capacitors are connected to either V_R or 0, depending on the 3 binary signals B_1, B_2, and B_3 respectively. For capacitor C_{s1a}, it is connected to V_R if $B_1 = 1$ and is connected to ground if $B_1 = 0$.

The analog input of the DSM, $x(t)$, is sampled onto the capacitor C_{s1} in the first integrator H_1 and the capacitor C_{a3} in the passive adder simultaneously. The sampling switches connected to C_{s1a}, C_{s1b}, and C_{s1c} are boostrapped nMOSFET switches [44], which are shown in Figure 4.13. These switches need to meet the linearity requirement the DSM. The sampling switches connected to the C_{a3} capacitors are regular CMOS switches. The linearity requirement of these switches are less critical.

In Figure 4.12, the comparator output set $\mathbf{D} = [D_1, D_2, D_3]$ is a thermometer code. An encoder converts $\mathbf{D}$ into a 2-bit Gray-code y_1 rather than Binary-code. y_1 serves as the ADC_1 output. A data-weighted-averaging (DWA) rotator also receives $\mathbf{D}$ and generates the DAC_1 input set $\mathbf{B} = [B_1, B_2, B_3]$ to mitigate the mismatches among C_{s1a}, C_{s1b}, and C_{s1c}. The rotator shown in Figure 4.14 is a passive switch matrix controlled by a DWA pointer, which is a finite-state machine (FSM) as shown in Figure 4.15 [45].

In Figure 4.12, the critical path is from the latch in the comparator to the first in-

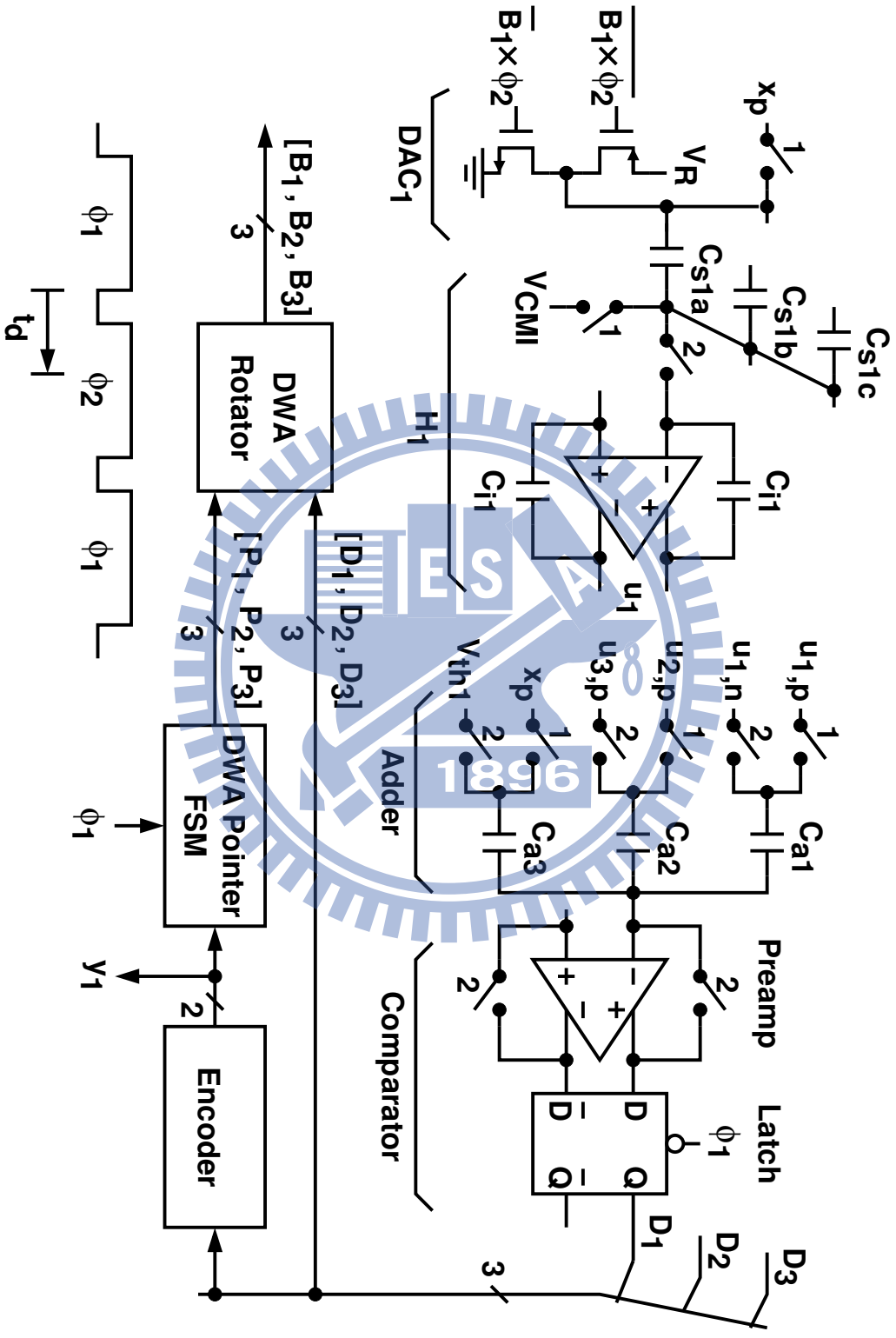


Figure 4.12: Schematic of the first loop in the DSM and its timing scheme.

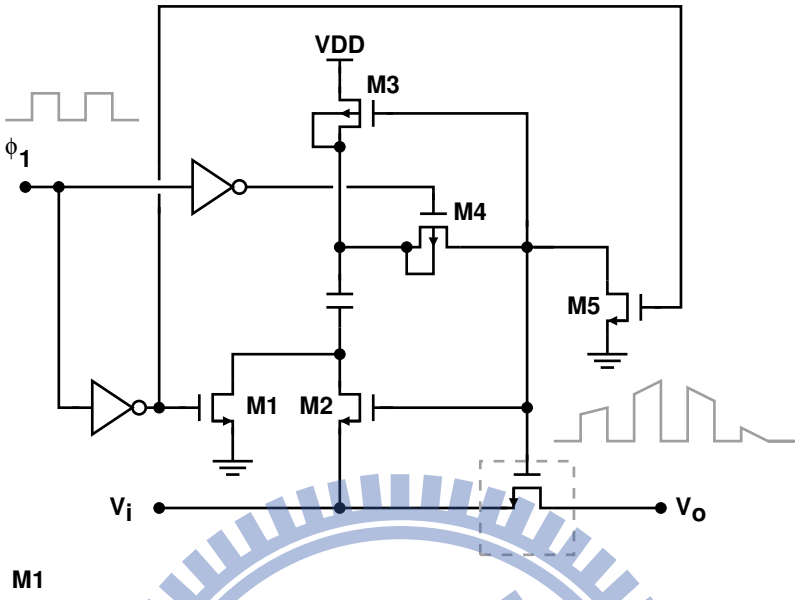


Figure 4.13: Schematic of Constant-V_{gs} boostrapped nMOSFET switch.

tegrator H_1. Upon the falling edge of ϕ_1, the latches in all three comparators begin the regeneration process to update $\mathbf{D} = [D_1, D_2, D_3]$. The change must propagate to the DAC_1 switches in time so that the integrator H_1 receives the correct DAC_1 output during $\phi_2 = 1$. The duration from the ϕ_1 falling edge that triggers the latches in the comparators to the ϕ_2 falling edge that ends the H_1 integration operation is only half of the clock period. If the sampling frequency of the DSM is 1 GHz, half of the clock period is 500 psec. We define the propagation delay from the latch in the comparator to the DAC_1 switches as t_d. It is critical to minimize t_d so that the integrator H_1 is given enough time to settle during $\phi_2 = 1$.

4.2.4 Comparator

Figure 4.16 shows the comparator preamplifier. It is a two-path amplifier that combines the high gain of a two-stage amplifier with the high-speed of a single-stage amplifier [27]. MOSFETs M1 and M2 are the input of the high-gain path. Its resistive loads are MOSFETs M5 to M8. The M7-M8 cross-coupled pair enhances the differential dc gain. MOSFETs M3 and M4 are the input of a direct feed-forward path to the output. The preamplifer has a dc gain of 22 dB. It achieves a unit-gain frequency of 16.5 GHz with a

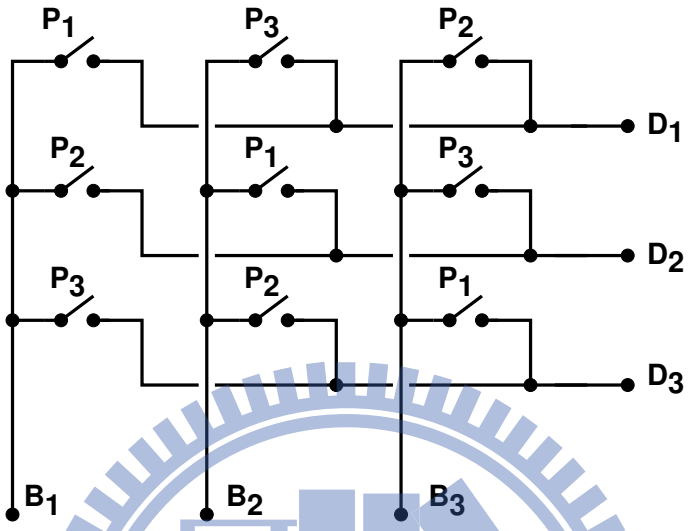
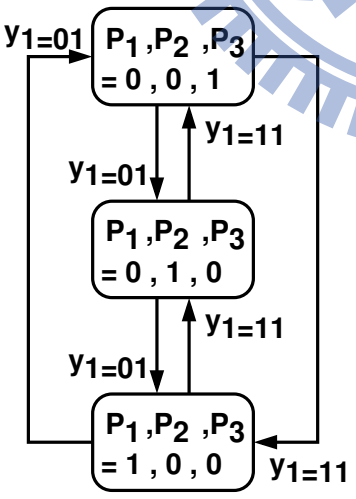


Figure 4.14: DWA rotator schematic.



D_1	D_2	D_3	y_1
0	0	0	0 0
0	0	1	0 1
0	1	1	1 1
1	1	1	1 0

Figure 4.15: DWA pointer and encoding.

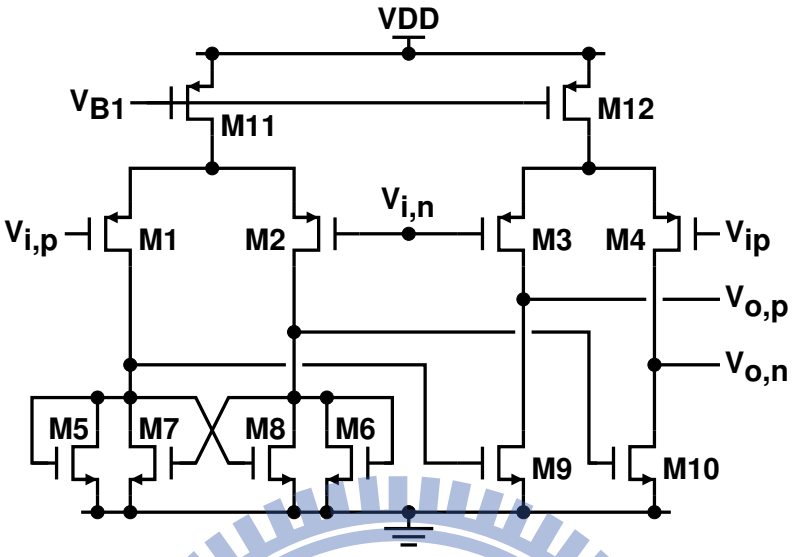


Figure 4.16: Comparator preamplifier schematic.

phase margin of 68 degree.

Noticeably, the preamplifier used in the comparator has more DC gain and wider bandwidth than the amplifiers in the loop filter. This is because that the preamplifier has a cross-coupled load, which provides large gain but is highly nonlinear. Meanwhile, the output capacitive loading of the preamplifier is minuscule.

With reference to Figure 4.17, the amplifier has smaller nominal DC gain than the preamplifier has. But the amplifier has less DC gain variation than the preamplifier has, i.e. the amplifier is more linear. This ensures that the non-linearity of integrators is attenuated for less distortions. When the output voltage is zero, the DC gain of the amplifier is 20 dB. When the output voltage changes to ±0.46 V, the DC gain of the amplifier is still 19 dB. In contrast, the linearity of preamplifier used in the comparator is unimportant. To detect zero crossing rapidly, the comparator seeks to have more DC gain and wider bandwidth. When the output voltage is zero, the DC gain of the preamplifier is 22 dB. When the output voltage changes to ±0.46 V, the DC gain of the preamplifier becomes 17.5 dB.

Figure 4.18 shows the schematic of the latch in the comparator. It is a cascade of a dynamic sense amplifier [46] and a static S-R latch [47]. The sense amplifier comprises a dynamic input stage followed by a dynamic latch. They are controlled by clocks ϕ_1 and

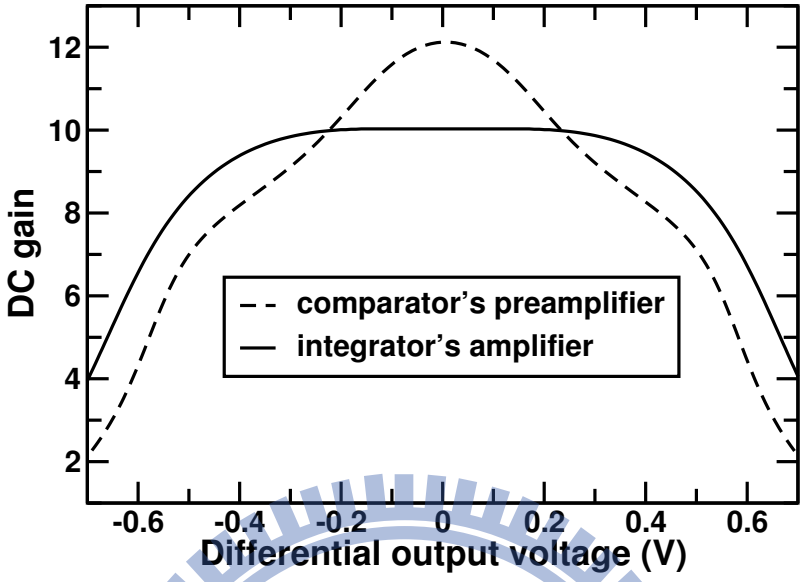


Figure 4.17: DC gain versus differential output voltage.

Table 4.3: S-R latch operation.

S	R	Q
0	0	forbidden
0	1	1
1	0	0
1	1	hold

$\overline{\phi_1}$ respectively. An inverter is used to generate $\overline{\phi_1}$ from ϕ_1. Thus, there is an inverter delay from ϕ_1 to $\overline{\phi_1}$. When $\phi_1 = 1$, the sense amplifier is reset, yield $S = V_{DD}$ and $R = V_{DD}$. When ϕ_1 changes to 0, the input stage is enabled before the dynamic latch is triggered. The comparison result of the sense amplifier is stored in the following S-R static latch. When $\phi_1 = 1$, both $S = V_{DD}$ and $R = V_{DD}$, causing the S-R latch to freeze its outputs. Table 4.3 presents the operation of S-R latch.

As illustrated in Figure 4.12, a comparator consists of a preamplifier followed by a latch. The preamplifier is a two-path amplifier that combines the high gain of a two-stage amplifier with the high-speed of a single-stage amplifier [27]. The latch is a cascade of a dynamic sense amplifier [46] and a static S-R latch [47]. The preamplifier has a dc gain of 22 dB. It achieves a unit-gain frequency of 16.5 GHz with a phase margin

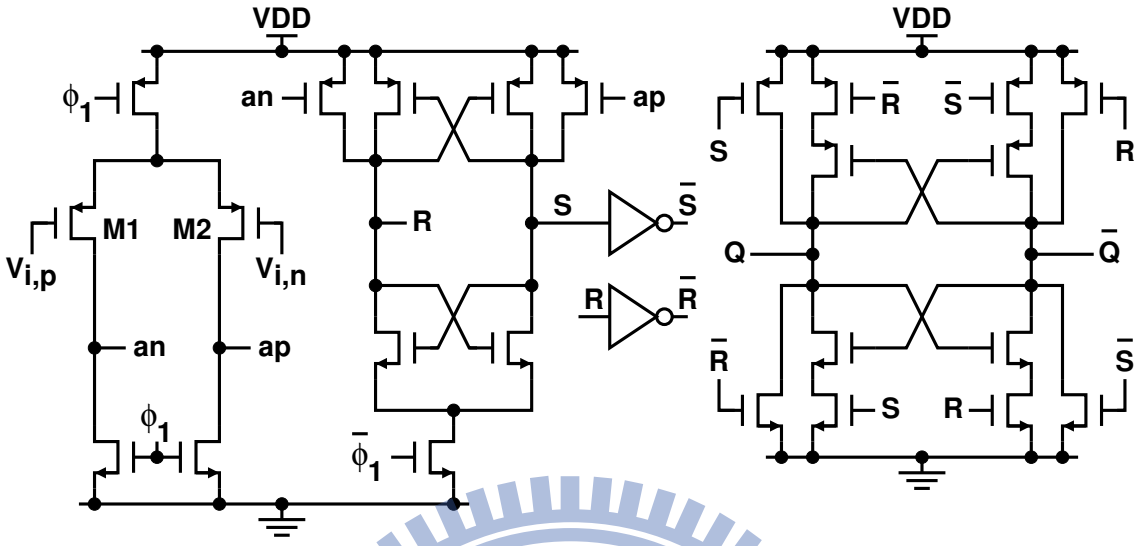


Figure 4.18: Comparator latch schematic.

of 68 degree. The propagation delay t_d defined in Figure 4.12 depends on the signal magnitude $|V_a - V_{th1}|$, where $V_a = x + 2u1 + u2 - u3$ is the comparator input and V_{th1} is the threshold of the comparator. As $|V_a - V_{th1}|$ decreases, it takes longer time for the latch to regenerate a valid output. In our design, $t_d = 125$ psec if $|V_a - V_{th1}| = 1$ mV. That leaves about 300 psec for the first integrator H_1 to settle during $\phi_2 = 1$, if the rise time, fall time, and non-overlapping time of the clocks are taken into account.

4.3 Chip Measurement

The DSM shown in Figure 4.1 was fabricated using a 65 nm CMOS technology. Figure 4.20 shows the chip micrograph. Its active area is 0.58×0.33 mm^2. The calibrations processors, CP_1, CP_2, and CP_3, and the noise cancellation filters, NCF_1 and NCF_2, are realized off-chip.

4.3.1 Setup

The DSM chip is mounted directly on a printed circuit board for measurement. Figure 4.22 shows the simplified block diagram of the instrumentation setup. The input signal is generated by HP ESG-D300A E4438C signal generator, and then it passes through

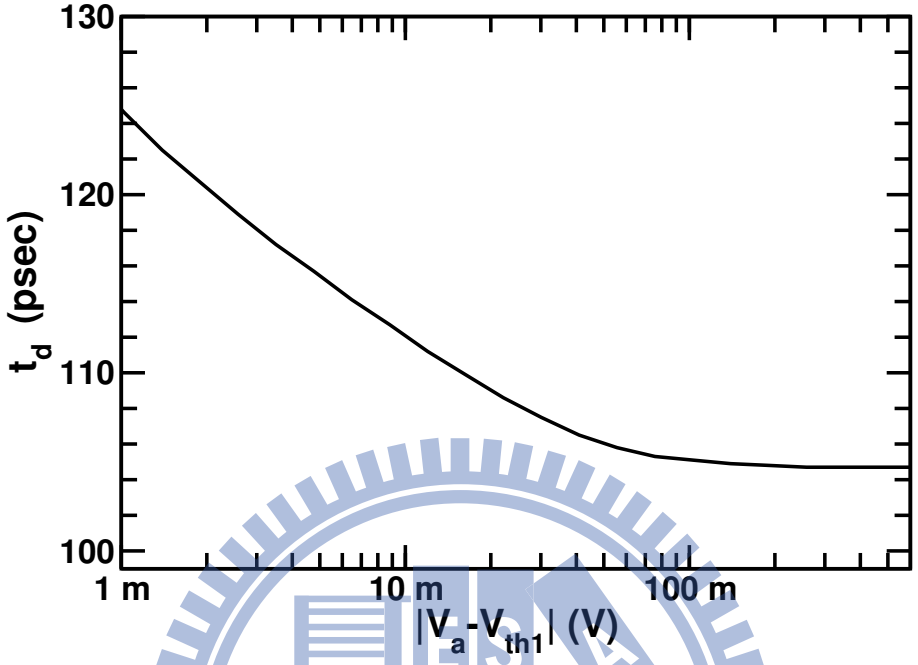


Figure 4.19: Propagation delay from the latch in the comparator to the DAC_1 switches.

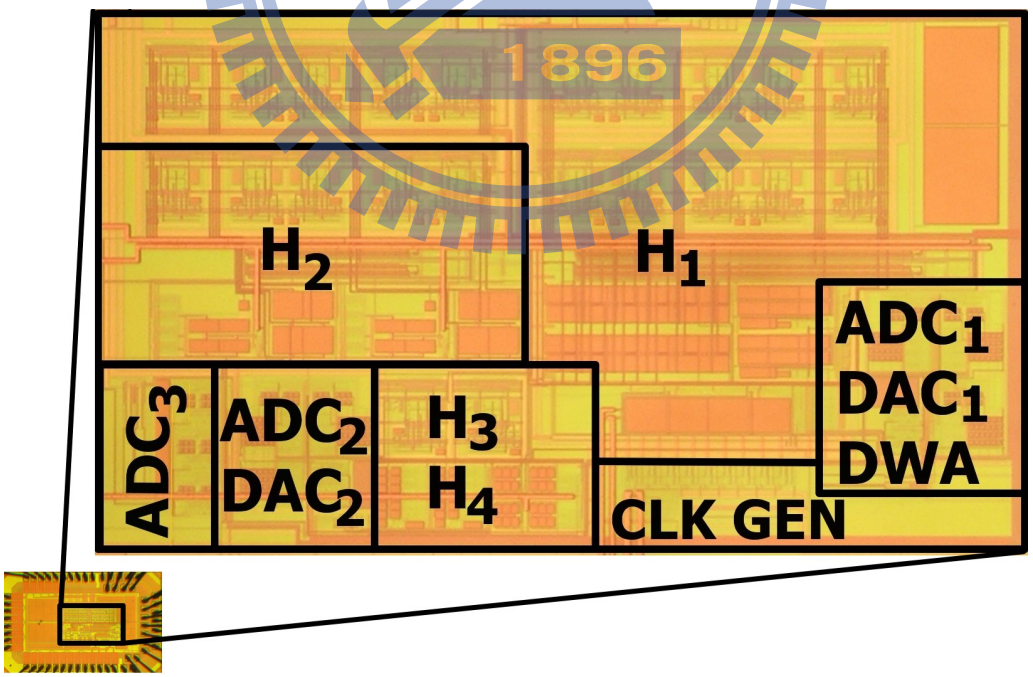


Figure 4.20: Modulator chip micrograph.

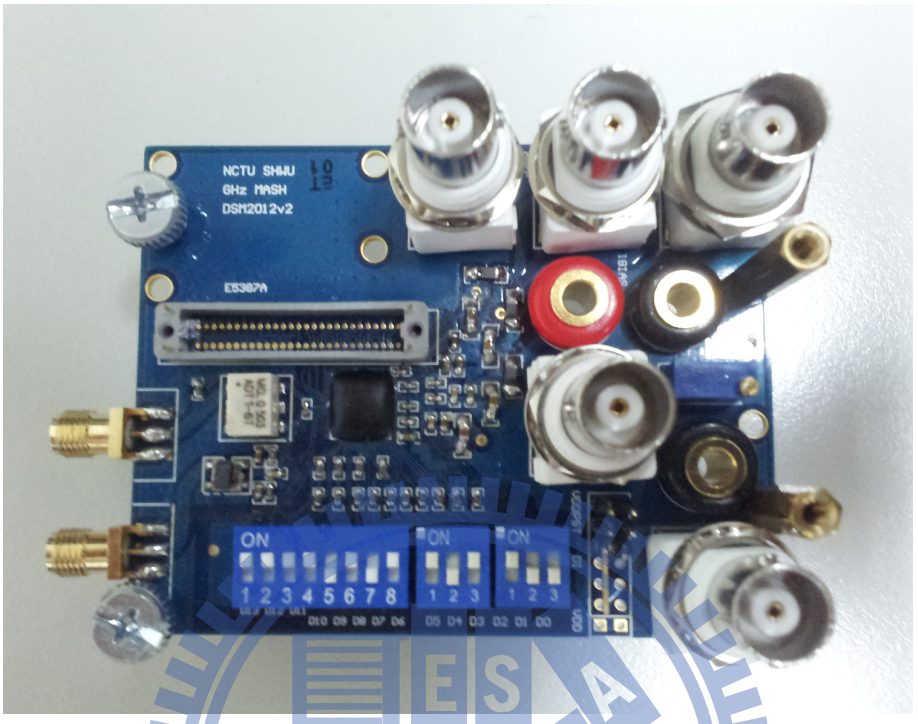


Figure 4.21: Photo of printed circuit board.

a band-pass filter (BPF). Next, a transformer ADT1-6T yeilds the diffrential input signals VIP and VIN to feed into the DSM chip. The clock source is originated from Agilent E4428C signal generator. Two RF transformers, including KRYTAR-3060200 and Mini-circuits TC1-1-13, creates the differential clock signals CLKP and CLKN with double DSM's sampling rate. These two clock signals are translated into digital clock signals by the built-in clock receiver. The power supplies are provided by Keithlay 2400 and Agilent E3631A. The reference V_R, analog V_{DD}, and digital V_{DD} are 1 V. The input common-mode voltage $V_{CMI} = (1/4)V_{DD}$, and the output common-mode voltage $V_{CMO} = (1/2)V_{DD}$. The differential full-scale input range is $\pm V_R$.

The calibration signals c_1 and c_2 are generated on chip. They can be enabled externally. The control signals T_1 and T_2 are generated externally and are fed to the chip to adjust integrators H_1 and H_2.

The DSM outputs, including y_1, y_2, and y_3, are taken off-chip through current-steering buffers with low-voltage-swing differential analog outputs, which is shown in Figure 4.23. Subsequently, Agilent logic analyzer with 16760A module captures the data, including y_1

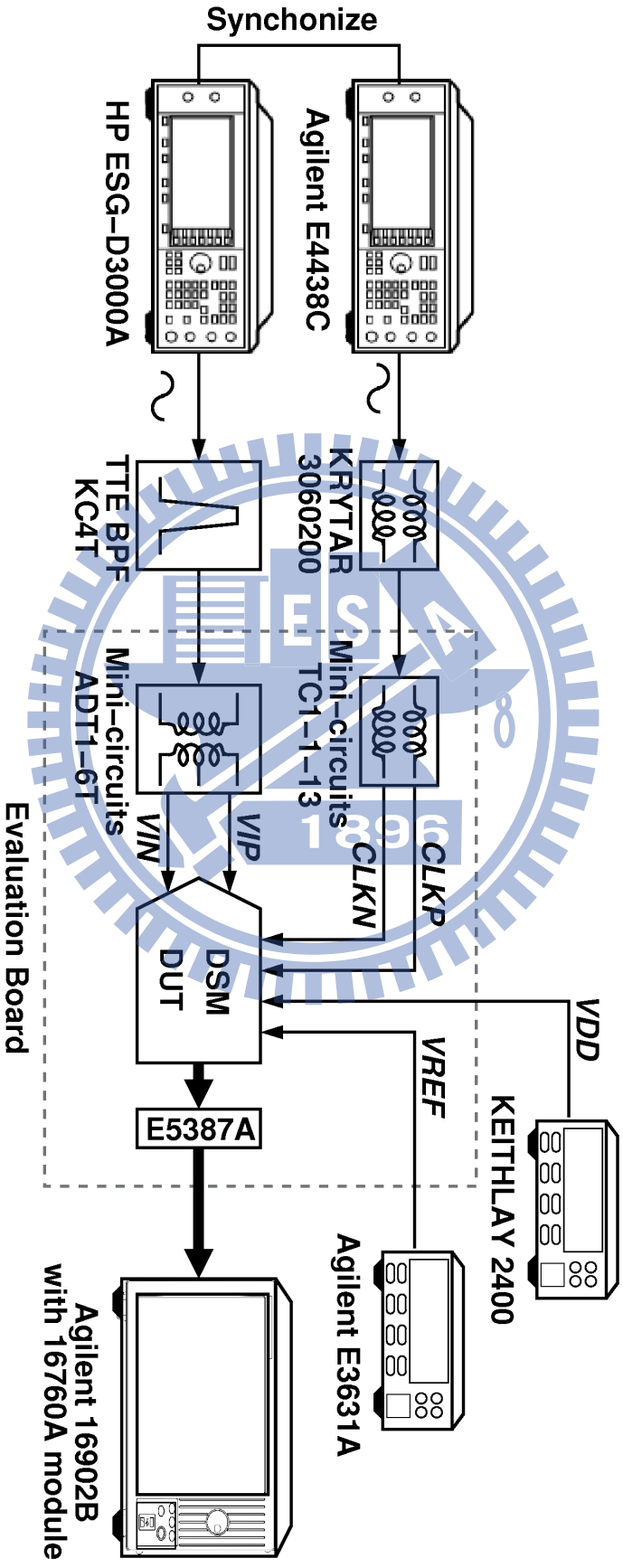


Figure 4.22: Measurement Setup.

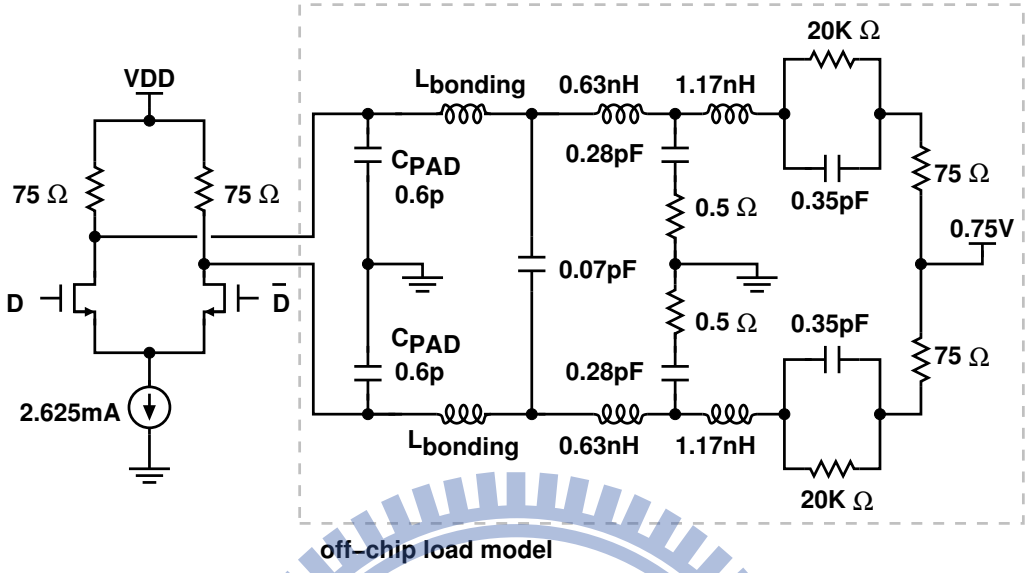


Figure 4.23: Current-steering buffers.

and y_2 as well as y_3, via the E5387A differential probe. Then the acquirement is post-processed by MATLAB. The Figure 4.24 shows the eye-diagrams of DSM output data.

4.3.2 Experimental Results

The DSM has a sampling rate of $f_s = 1.1$ GHz. Its signal bandwidth is 16.67 MHz if the oversampling ratio (OSR) is 33. Figure 4.25 is the measured DSM output spectra before and after the calibration. The input signal is a -3 dBFS 2 MHz sine wave. Without the calibration, the quantization noise of the first stage, e_1, dominates the low-frequency band and is shaped by a 40 dB/decade slope for frequencies above 10 MHz. The calibration signal c_2 is visible. It has a frequency of $f_s/64 = 17.19$ MHz. The measured signal-to-noise ratio (SNR) is 57 dB. The SNDR is 54 dB. After the calibration, the quantization noise e_1 is minimized. The noise floor drops and the noise at high frequency is shaped by a 80 dB/decade slope. The calibration signal c_2 is attenuated by 30 dB. The measured SNR and SNDR become 76 dB and 74 dB respectively. If the calibration signal c_1 is injected instead of c_2, the c_1 tones are -34 dB in the DSM output spectra. Figure 4.26 shows the passband details of the output spectra. Before the calibration, the 5th and 7th harmonics are the dominant tones. The spurious-free dynamic range (SFDR) is 58 dB.

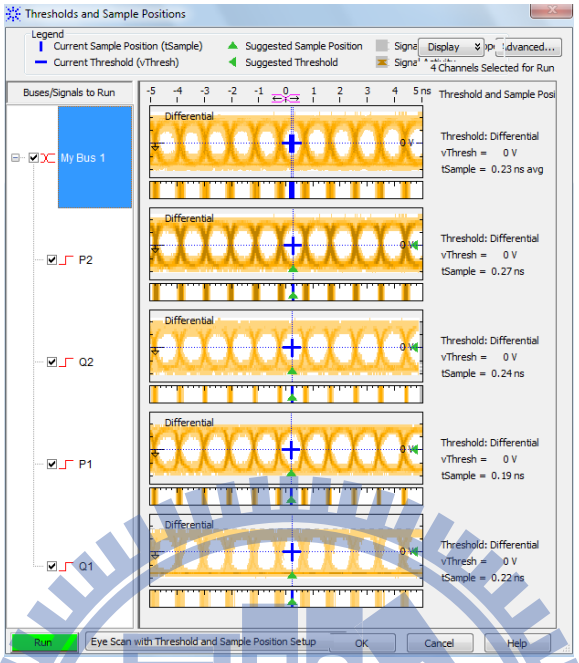


Figure 4.24: Eye-diagram of output data.

After the calibration, the 3rd harmonic becomes the dominant tone. The SFDR increases to 83 dB.

Figure 4.27 shows the measured SNR and SNDR versus the input signal level. The input is a 2-MHz sine wave. Before the calibration, the peak SNR and the peak SNDR are 57.42 dB and 54.23 dB respectively at −0.71 dBFS input level. The dynamic range (DR) is 62 dB. After the calibration, the peak SNR is 77.22 dB at −0.93 dBFS input level, and the peak SNDR is 74.32 dB at −3.85 dBFS input level. The DR increases to 81 dB. Note that, before the calibration, there is a visible difference between the SNR and the SNDR for the input level higher than −20 dBFS. This is because the quantization noise e_1 leaking to the DSM output contains input harmonics. After the calibration, the e_1 leakage is reduced, and the difference between SNR and SNDR is also decreased.

Operating at $f_s = 1.1$ GHz sampling rate, the chip consumes a total of 94 mW from a 1 V supply. The power and area of the circuit blocks are listed in Table 4.4.

In our design, the opamps employ the constant-current biasing scheme. Simulations show that the dc gain of the opamps varies from 10.74 to 8.76 if the temperature changes from 0°C to 80°C. Thus, after calibration, the SNR of the DSM will degrade by −3 dB if

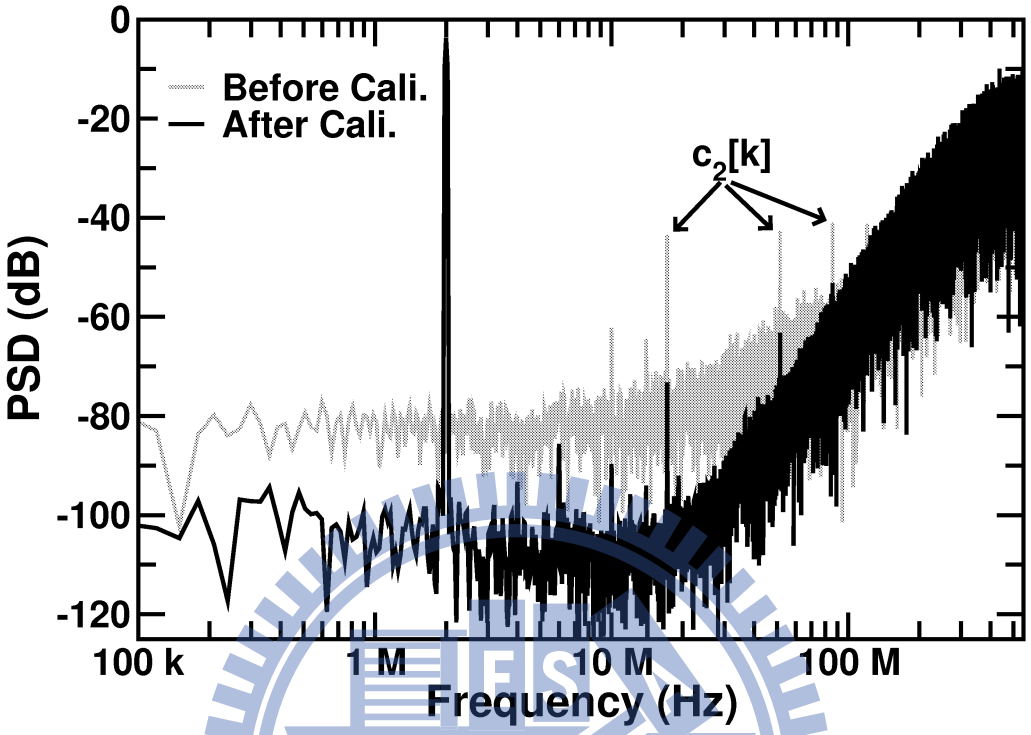


Figure 4.25: Measured output spectra of the DSM.

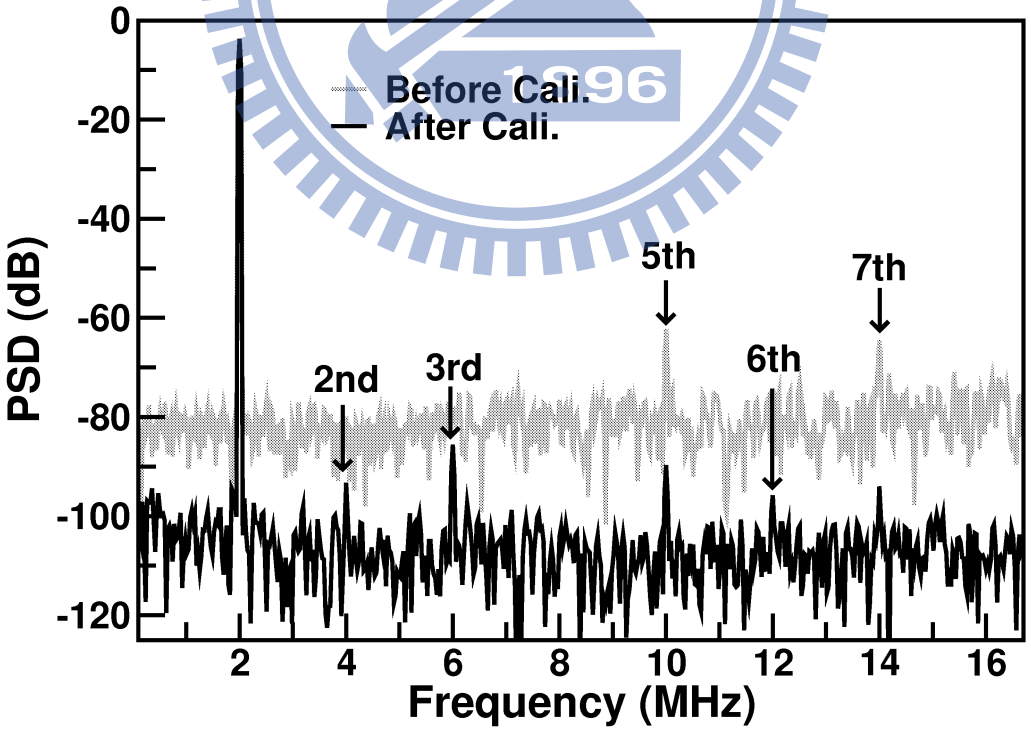


Figure 4.26: Measured in-band output spectra of the DSM.

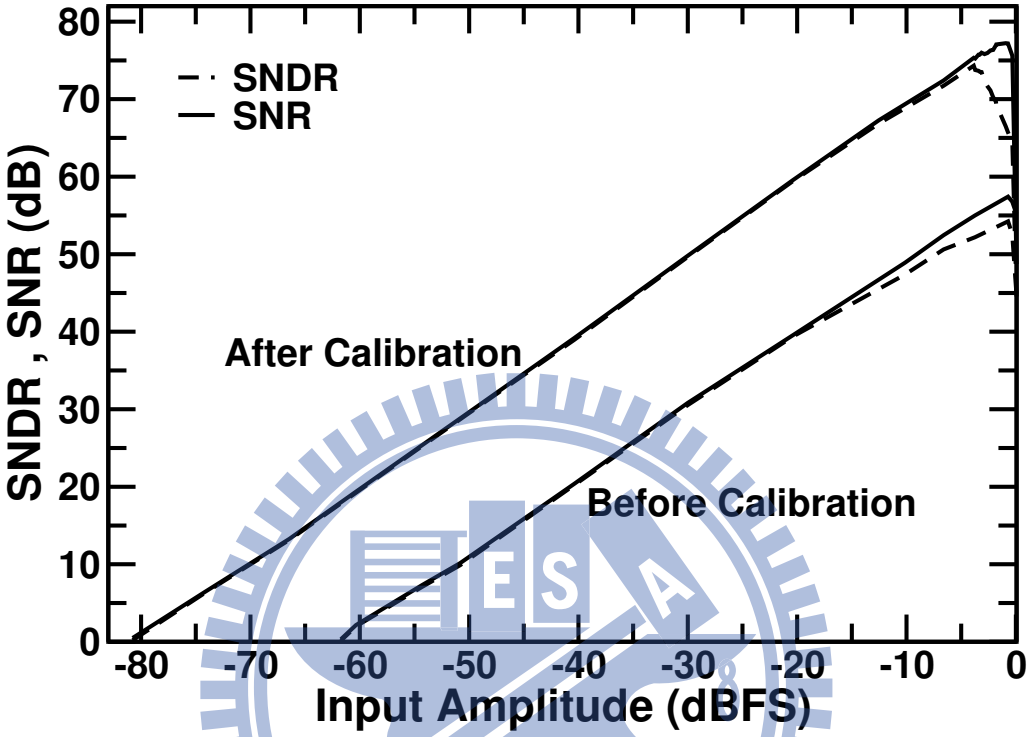


Figure 4.27: Measured dynamic performance of the DSM.

Table 4.4: Power and area of circuit blocks.

Block	Power (mW)	Power (%)	Area (%)
Integrator H_1	56.4	60	50
Integrator H_2	17.7	19	22
Integrator H_3	3.75	4	4.5
Integrator H_4	3.75	4	4.5
ADCs, DACs	12.4	13	19
Total	94	100	100

the temperature changes by 10°C. However, this degradation will not occur if the time for the temperature change is much longer than the calibration time constant. On the other hand, the dc gain of the opamp varies from 9.77 to 10.87 if the supply voltage changes from 0.9 V to 1.1 V. Thus, after calibration, the SNR degradation is less than −3 dB if the supply voltage variation is less than ±50 mV.

Table 4.5 summarizes the performance of this DSM chip and compares it with other wide-bandwidth DSMs. The figure of merit (FOM) are defined as follows [28]:

$$\text{FOMs} = \text{DR}_{\text{dB}} + 10\log_{10}\frac{\text{BW}}{\text{Power}} \qquad \text{FOMw} = \frac{\text{Power}}{2\text{BW} \times 2^{(\text{SNDR}-1.76)/6.02}} \tag{4.3}$$

The FOMs of this chip is 163.487 dB, and the FOMw is 660 fJ/level. Comparing to other discrete-time (DT) DSMs, this DSM has the highest sampling rate, operates under the lowest supply voltage, and achieves competitive FOMs and FOMw. In Table 4.5, the continuous-time (CT) DSMs show better FOMw performance. However, they require clocks of more stringent jitter performance. They are also more sensitive to PVT variations without on-chip calibration. One of them requires foreground calibration of DACs [29]. Some of them are based on voltage-controlled ring oscillaotrs (VCOs) and require non-linearity correction of phase noise [51, 52].

A plot of bandwidth versus DR according to [55] is shown in Figure 4.28 to contrast the performance of various ADCs. With conditions of above 10MHz bandwith and DSM type ADC, another plot of FOMw versus DR is shown in Figure 4.29. Among that, the excellent works are highlighted [50, 56–59].

4.4 Summary

A 4th-order discrete-time DSM was fabricated using a 65 nm CMOS technology. It has a sampling rate of 1.1 GHz and an input bandwidth of 16.67 MHz with an oversampling ratio (OSR) of 33. We use low-complexity circuits to achieve high speed. The opamps have a unity-frequency of 6 GHz in the integrator configuration, but have a dc gain of only 10. The low-gain opamps result in lossy integrators. We apply the integrator leakage calibration to adjust the leakage-compensating capacitors of the integrators to move their poles β back to 1. We use the noise leakage calibration to minimize the quan-

Table 4.5: Comparison of wide-bandwidth DSMs.

Publication	This work	[48]	[49]	[16]	[17]	[18]	[19]	[50]	[29]	[51]	[52]	[53]	[54]
Type	DT	DT	DT	DT	DT	DT	DT	CT	CT	CT	CT	CT	CT
Process (nm)	65	65	180	32	180	90	90	90	90	65	130	90	28
Supply (V)	1.0	1.25	1.8	1.05	1.8	1.2	1.4	1.2	1.2	1.2	1.5	1.4	1.5
Clock (MHz)	1100	240	160	400	80	420	330	3600	500	2400	900	600	640
OSR	33	8	8	10	8	10.5	8	50	10	64	22.5	30	17.8
BW (MHz)	16.67	15	20	20	10	20	20	36	25	18.8	20	10	18
DR (dB)	81	-	64	66	75.5	-	-	83	72	78	-	-	78
Peak SNR (dB)	77.22	-	63	-	74	72	67	76	69	76	81	83	-
Peak SNDR (dB)	74.32	67	63	63	74	70	63	71	68	74	78	78	73.6
Power (mW)	94	37	16	28	22	28	73	15	8.5	39	87	16	2.6
Die Size (mm^2)	0.19	0.28	0.36	0.13	0.62	1	1.3	0.12	0.23	0.075	0.45	0.36	0.08
FOMs (dB)	163.5	153*	155	155	162	161*	151*	176.8	167	165	165*	171*	175
FOMw (pJ/conv.)	0.66	0.67	0.35	0.61	0.27	0.27	1.5	0.07	0.09	0.25	0.33	0.12	0.028

* Assume DR equals to peak SNDR or peak SNR.

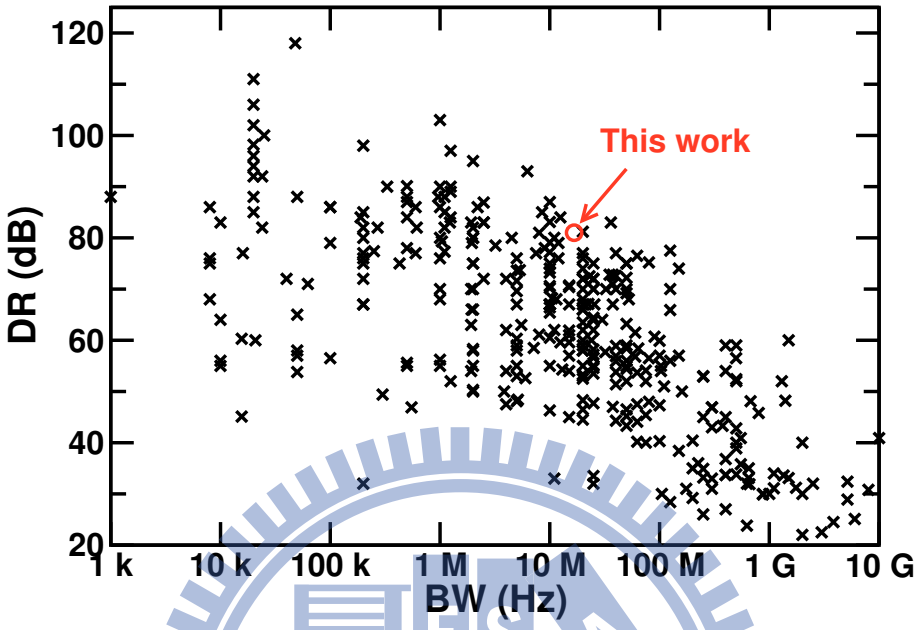


Figure 4.28: Comparison with various ADCs.

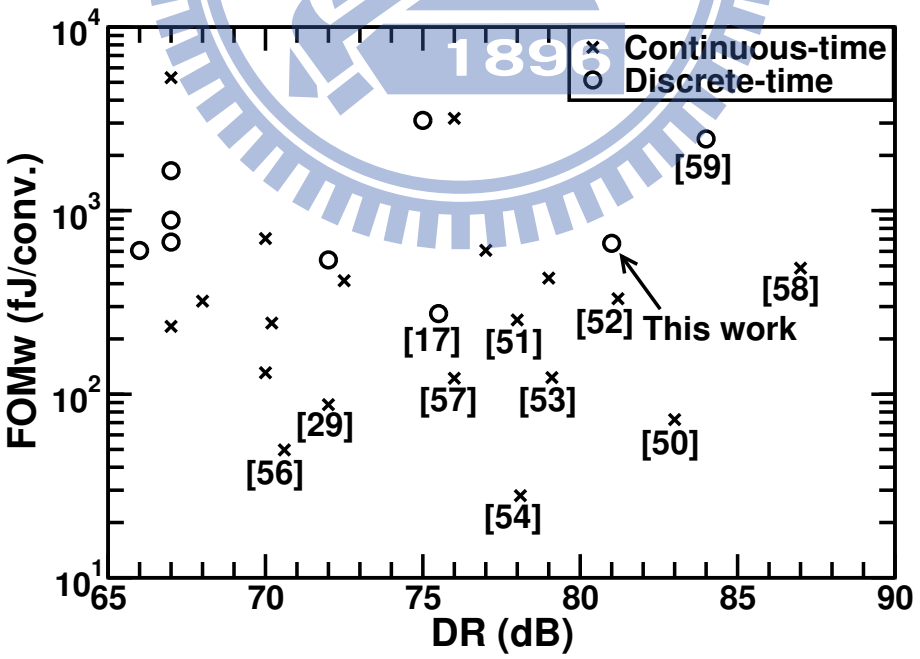


Figure 4.29: Comparison with various DSMs, whose bandwidth is above 10MHz.

tization noise of the first loop leaking to the DSM's combined output. The noise leakage calibration relaxes the matching requirement for the MASH structure. The calibration is simplified since it does not need to correct the β coefficients. Both digital calibrations can operate in the background without interrupting the normal DSM operation. The calibration processors are simple digital circuits. They do not have complex filters. The chip's measured signal-to-noise-and-distortion ratio (SNDR) and dynamic range (DR) are 74.32 dB and 81 dB respectively. The chip consumes 94 mW from a 1 V supply. The active area is 0.33×0.58 mm^2.

We demonstrate that the combination of low-complexity circuits and digital calibration can yield a high-speed high-performance DSM. The design technique is specially suitable for advanced nanoscale CMOS technologies.Besides, each terms under calibrated is perceived directly through a responding test signal. This makes the calibration procedure be more efficient than previous works.

Chapter 5

Conclusions and Future Works

5.1 Conclusions

The NTF zero deviation caused by the integrator leakage decreases the SQNR of the DSM. DSM designers traditionally improve the SQNR by increasing the OSR, using higher-order loop filters or more complex analog circuits. At a price, more complicated designs in system level also in circuit level. This thesis proposed a digital signal processing technique to correct NTF zeros without interrupting the normal DSM operation. The enabling technique injects out-of-band signals into different nodes of the loop filter, that have no influence on the SQNR, to detect every NTF zeros. Then the AAR-based CPs demodulate the chopped signals without cumbersome digital circuits like IIR filters or multipliers. Thus the information about the NTF zero deviation is observed quickly and is used to drive the tunable SC integrators we developed for correcting NTF zeros.

A cascaded DSM is suffered from the quantization noise leakage, which is originated by the mismatch between the analog loop filter and the digital noise cancellation filter. This makes circuits requirement of a cascaded DSM severe. This thesis presents a new calibration scheme to minimize the quantization noise leakage and relax the requirement of precise integrators that are needed in previous cascaded DSMs. The noise leakage calibrarion using the AAR-based calibration also can execute without interrupting the normal operation of DSM and be optimized according to the architecture of DSM.

A 2-2 cascaded Discrete-Time $\Delta\Sigma$ modulator is fabricated using a 65 nm CMOS

technology. It is operated at 1.1 GHz clock rate and achieves 81 dB dynamic rage over 16MHz bandwidth. The chip demonstrates our proposed background calibration techniques, including integrator leakage calibration and quantization noise calibration. The lossy integrators and inaccuracy NCF are detected separately by the novel scheme. Then compensation and trimming are applied on both analog and digital domain to minimize the cost of calibration, including chip area and power as well as circuit complexity. Both calibration techniques provide the utilizing of low gain high speed opamps for broadband $\Delta\Sigma$ data conversion, especially as CMOS technologies advance. Although the additional circuits and power consumption for calibration are necessary, but both should be negligible compares to the saving in the loop filter for restoring SQNR. Measurement results show the theory was truth and can be implemented in silicon.

5.2 Recommendations for Future Investigation

This section presents several suggestions for future investigations for DSMs using calibration techniques.

- To apply the calibration schemes, extra-ADCs are necessary. This costs the calibrated DSM chip area and power consumption. For saving power and area further, the calibrated DSM with only one extra-ADC is encouraged.
- The injected signal, which is used to detect the leakage in this thesis, is a square wave. Although it can be removed by the following decimation filter. Using a pseudo-random number sequence may provide an alternative for leakage detection.
- Improve SNDR beyond 80 dB.
- Improve power efficiency.

Appendix A

Stochastic Analysis of AAR-based Calibration

The purpose of this appendix is the deviation of (2.28).

A.0.1 The First-Order DSM

Briefly speaking, the CP monitors $s[k]$ to adjust β since $s[k]$ is the mapping of the NTF zero deviation. The approximation of $s[k]$ (i.e. $\dot{s}k$) reveals that the polarity of $s[k]$ is the same to the polarity of the NTF zero deviation. Hence the intuitive criterion for curing β is picking $N_{th} = 0$ in the AAP-based CP. But the input signal x and the quantization noise practically influence $s[k]$, thus the CP may mistakes the polarity of the NTF zero deviation. To improve the validity of the calibration, the CP is analyzed from the stochastic perspective to examine $s[k]$ in detail as well as to figure out the value of N_{th} and Δ.

According to Figure 2.10, there are three contributions to $s[k]$, one is $s_c[k]$ caused by $c[k]$, another is $s_x[k]$ caused by input $x[k]$, and the other is $s_e[k]$ caused by the quantization noise $e[k]$. $s[k]$ is the sum of them, i.e. $s[k] = s_c[k] + s_x[k] + s_e[k]$. Addition to this, the probability density function (PDF) of them is $f_{s_v}(x)$, $f_{s_x}(x)$ and $f_{s_e}(x)$ respectively. All above description could be summarized graphically in Figure A.2.

Since the signal path of $c[k]$ is deterministic, so $f_{s_c}(x)$ is intuitively found as

$$f_{s_c}(x) = \delta(x - \dot{s} \cdot k) \tag{A.1}$$

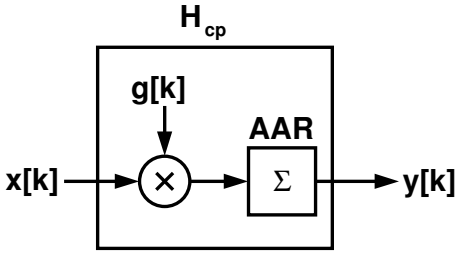


Figure A.1: Representation of the AAR-based CP whithout reset.

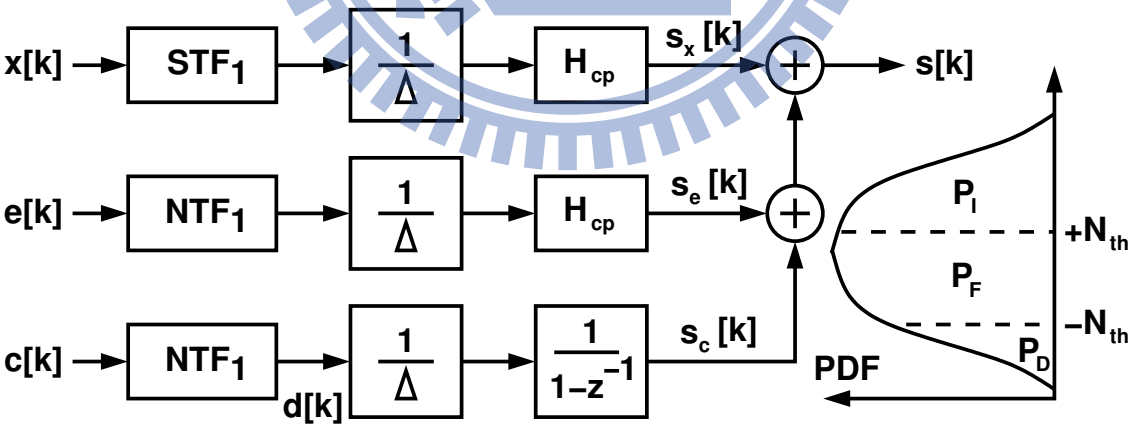


Figure A.2: The linear model of a DSM in cascade with an AAR-based CP.

In contrast, the DSM converts the $x[k]$ and brings the quantization noise $e[k]$ into the digital domain, furthermore the results is upset by the CP. Such that the actual evaluations of $f_{s_x}(x)$ and $f_{s_e}(x)$ are very tedious. However, this problem could be solved by thinking the AAR-based CP as a discrete-time system illustrated in Figure A.1. The input of the CP has to be multiplied first by $g[k]$ that is a square-wave sequence with dead time insertions, next feeding into the ACC where the accumulator is specified to be reset at $k = 0$. Then the difference equation of this process is expressed as

$$y[k] = \sum_{n=0}^{k} x[k-n]g[k-n] = \sum_{n=-\infty}^{\infty} x[k-n]h_{cp}[n] \tag{A.2}$$

So the impulse response of the CP, $h_{cp}[n]$, is

$$h_{cp}[n] = g[k-n] \cdot u[n] \cdot u[k-n] \tag{A.3}$$

Once $h_{cp}[n]$ is known, the complete characterization of a DSM in cascade with a AAR-based CP can be analytical evaluated. Return to Figure A.2, the input signal of the DSM is processed by $\mathrm{STF}_(e^{j\omega}) \cdot \frac{1}{\Delta} \cdot \mathrm{H_{cp}}(e^{j\omega})$. Since the frequency of the input is low with respect to f_s, in-band $\left|\mathrm{STF}_(e^{j\omega})\right|$ generally comes close to 1, as well as in-band $\left|\mathrm{H_{cp}}(e^{j\omega})\right|$ has the following relationship

$$\left|\mathrm{H_{cp}}(e^{j\omega})\right| \leq \left|\frac{D_g \cdot \frac{f_s}{f_q}}{1 + e^{\frac{-j\omega}{2f_q}}}\right| = \left|\frac{D_g \cdot \frac{f_s}{f_q}}{1 + e^{-j\pi\frac{f}{f_q}}}\right| \tag{A.4}$$

If input bandwidth is much lower than f_q, this equation can be derived further as $\frac{D_g f_s}{2f_q}$. Therefore, without knowing the distribution of input signal prior, we suppose $f_{s_x}(x)$ is a uniform distribution denoted as

$$f_{s_x}(x) = \mathcal{U}(\frac{-D_g f_s}{2\Delta f_q}, \frac{+D_g f_s}{2\Delta f_q}) \tag{A.5}$$

Apparently the result is complicated, but a special case is good for understanding, that a DC signal $\bar{x}$ is the input of the DSM and the quantization noise is ignored. Seeing Figure A.1, due to the modulation of the DSM and the multiplication of $g[k]$, $\bar{x}$ is transferred into a sequence which is like $[0, 0, 0, \frac{+\bar{x}}{\Delta}, \frac{+\bar{x}}{\Delta}, 0, 0, 0, \frac{-\bar{x}}{\Delta}, \frac{-\bar{x}}{\Delta}, \cdot\cdot]$. After accumulation, the output becomes $[0, 0, 0, \frac{\bar{x}}{\Delta}, \frac{2\bar{x}}{\Delta}, 0, 0, 0, \frac{\bar{x}}{\Delta}, 0, \cdot\cdot]$, namely the output is dispersed from 0 to

$\frac{D_g f_s}{2f_q}\frac{\bar{x}}{\Delta}$. Therefore, if we attempt to extend the preceding observation into a practical case that input is a slowly varying signal with range between -1 and 1, $f_{s_x}(x)$ can be surmised as (A.5) for simplicity.

In terms of $f_{s_e}(x)$, the procedure of analysis is similar. That is to say, the quantization noise is filtered by $\mathrm{NTF}_(e^{j\omega}) \cdot \frac{1}{\Delta} \cdot \mathrm{H_{cp}}(e^{j\omega})$. By assuming the quantization noise is white, the average power $s_e[k]$, $\sigma^2_{s_e}[k]$, can be estimated as

$$\begin{aligned}
\sigma^2_{s_e}[k] &= \frac{\sigma_n^2}{\Delta^2} \cdot \frac{1}{2\pi} \int_{-\pi}^{\pi} \left| \mathrm{NTF}_(e^{j\omega}) \cdot \mathrm{H_{cp}}(e^{j\omega}) \right|^2 d\omega \\
&= \frac{1}{12} \cdot \sum_{n=-\infty}^{\infty} \left| Z^{-1}\left\{ \mathrm{NTF}_(z) \right\} * h_{cp}[n] \right|^2 \\
&\approx \frac{1}{12} \cdot \sum_{n=0}^{\infty} \left| Z^{-1}\left\{ \sum_{m=0}^{\frac{D_g f_s}{2f_q}-1} z^{-m} \mathrm{NTF}_(z) \right\} \right|^2 \cdot \frac{k}{\frac{f_s}{2f_q}} \\
&= \sigma^2_{cp} \cdot \frac{k}{\frac{f_s}{2f_q}} = \sigma^2_{cp} \cdot \frac{2f_q}{f_s} k
\end{aligned} \tag{A.6}$$

where σ_n^2 is the quantization noise power in the analog domain as well as it is well-known as $\frac{\Delta^2}{12}$. Meanwhile, the σ^2_{cp} is defined as the noise power coefficient of the AAR-based CP. For better understanding, this equation can be modeled on a *one-dimensional random walk*, where every $\frac{f_s}{2f_q}$ samples is considered as one step which owns a finite variance σ^2_{cp}. After $\frac{2f_q}{f_s}k$ steps for accumulation, the variance of translation distance, $\sigma^2_{s_e}[k]$, is equal to $\sigma^2_{cp} \cdot \frac{2f_q}{f_s}k$. Then $f_{s_e}(x)$ is found to be a normal distribution denotated as

$$f_{s_e}(x) = \mathcal{N}(0, \sigma^2_{s_e}[k]) \tag{A.7}$$

In probability theory, the PDF of the sum of independent random variables involves the convolution of their PDF's [60]. Therefore the PDF of $s[k]$, $f_s(x)$, can be approximated to be a close-form expression by exploiting the Gauss error function as

$$\begin{aligned}
f_s(x) &= f_{s_c}(x) * f_{s_x}(x) * f_{s_e}(x) \\
&= \delta(x - c_1) * \mathcal{U}(-c_0, +c_0) * \mathcal{N}(0, c_2) \\
&= \frac{1}{4c_0} \left\{ \mathrm{erf}\left(\frac{x + c_0 - c_1}{\sqrt{2c_2}} \right) - \mathrm{erf}\left(\frac{x - c_0 - c_1}{\sqrt{2c_2}} \right) \right\}
\end{aligned} \tag{A.8}$$

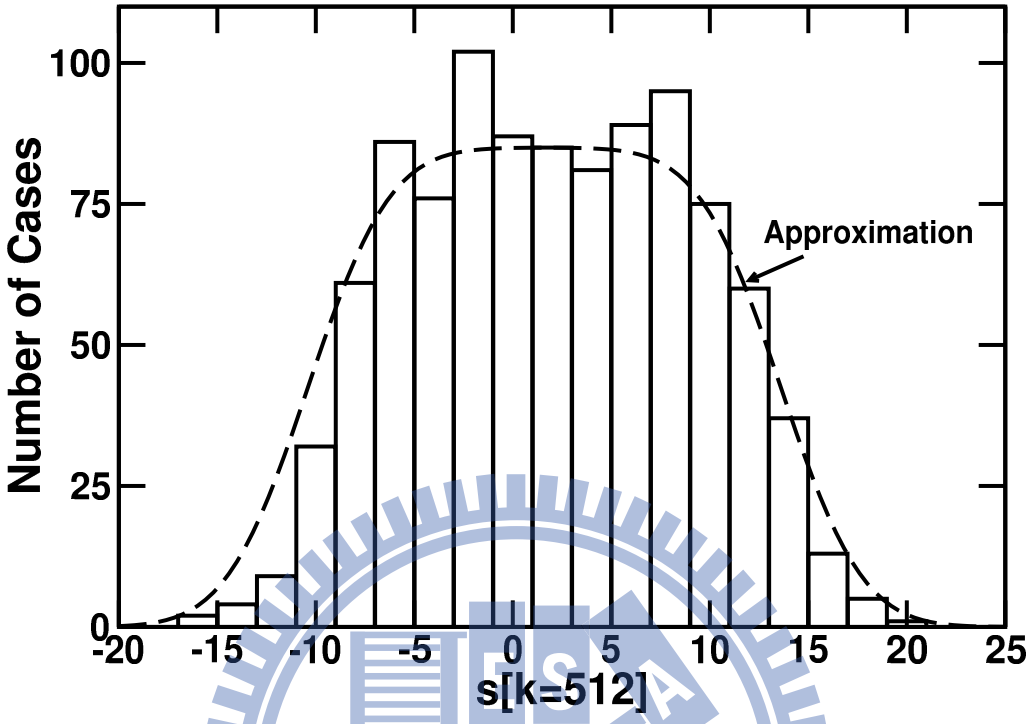


Figure A.3: Histogram of $s[k = 512]$ with 1000 Monte Carlo simulations for a 4-bit 1st-order DSM. $\beta = 0.99$, $V = \Delta$, $f_q = \frac{f_s}{16}$ and $D_g = 25\%$

where $c_0 = \frac{D_g f_s}{2\Delta f_q}$, $c_1 = \dot{s}k$ and $c_2 = \sigma^2_{s_e}[k]$. All above discussions could be verified by Monte Carlo simulations. A 4-bit 1st-order DSM with $\beta = 0.99$ is used to demonstrate here. The data were collected from 1000 Monte Carlo simulations when $k = 512$. The result, a histogram of $s[k]$ as Figure A.3, corresponds to the estimations of (A.8).

Owning to $f_s(x)$, the probability of states of $s[k]$ are available: (1) the probability of $s[k] > +N_{th}$ is P_I, which stems from the increase of β in the CP; (2) the probability of $s[k] < -N_{th}$ is P_D, which stems from the decrease of β; (3) the probability of $s[k]$ is P_F, which stems from the freeze of β. It is noticeable that $s[k]$ is among the three states, so

$$P_I + P_D + P_F = 1. \tag{A.9}$$

$$P_D = \int_{-\infty}^{-N_{th}} f_s(x)dx; P_F = \int_{-N_{th}}^{+N_{th}} f_s(x)dx; P_I = \int_{+N_{th}}^{+\infty} f_s(x)dx \tag{A.10}$$

A 1st-order 4-bit DSM with $\beta = 0.99$ was also simulated to show the transient responses of probabilities when $N_{th} = 16$. At the beginning, P_F is 1 nearly. As times goes by, P_F gradually decreases to 0, and P_I approaches to 1. And P_D is the smallest

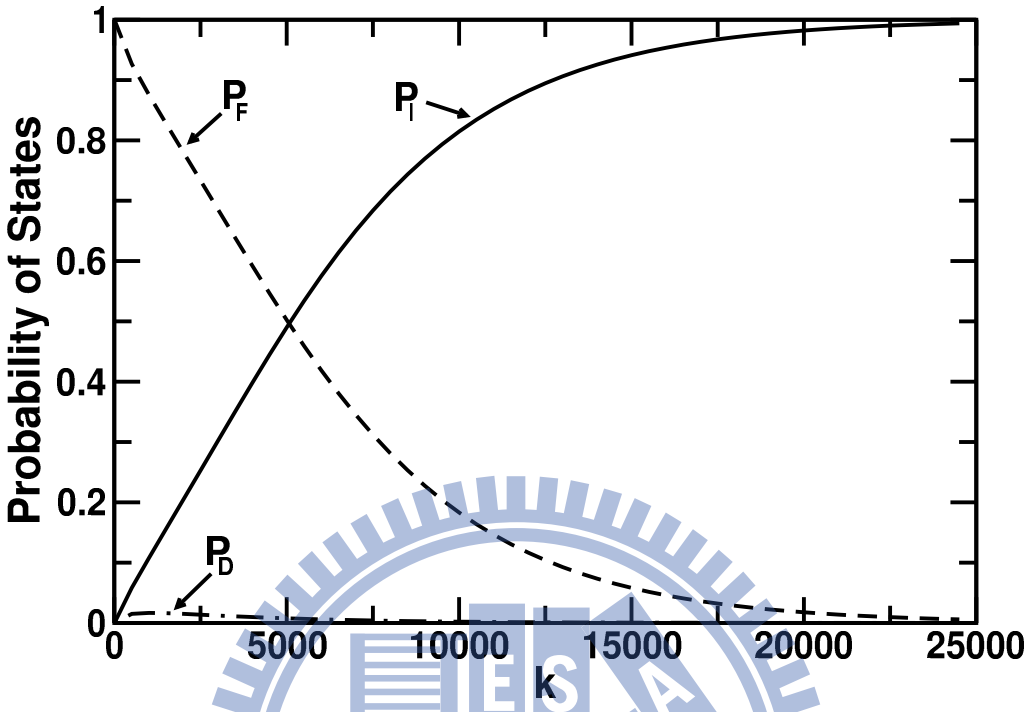


Figure A.4: Transient behaviors of P_F, P_D and P_I when $N_{th} = 16$. $\beta = 0.99, V = \Delta$, $f_q = \frac{f_s}{16}$ and $D_g = 25\%$.

one during the whole simulation time. To put it another way, the CP holds the β until it collects enough information of the polarity of the NTF zero deviation. Finally, the NTF zero deviation compels the CP to increase β rather decrease.

Figure A.5 provides a physical analogue to discover the idea behind the AAR-based CP whenever k is given. A ball with three forces to control its movement is in a bowl. Initially, the ball locates at the state of $\beta = 1 - \Delta\beta$. As long as a proper N_{th} is picked to create a negligible P_D all along, the ball hardly moves outside the bowl. Moreover, P_I grows gradually, thus the ball will move to the state of $\beta = 1$ by adding a step size $\Delta\beta$. Consequently, the ball will be corrected to the state of $\beta = 1$ by the AAR-based calibration.

When the calibration loop converges, the β fluctuates between a few of states, and the root-mean-square error $\sigma(\beta)$ can be applied to express the calibration precision. The $\sigma(\beta)$ depends on $\Delta\beta$ and N_{th}, and the trend is pictured in Figure 2.15. However, as N_{th} is big enough to avoid compensate β in the wrong direction, the $\sigma(\beta)$ will converge to σ_0. Most

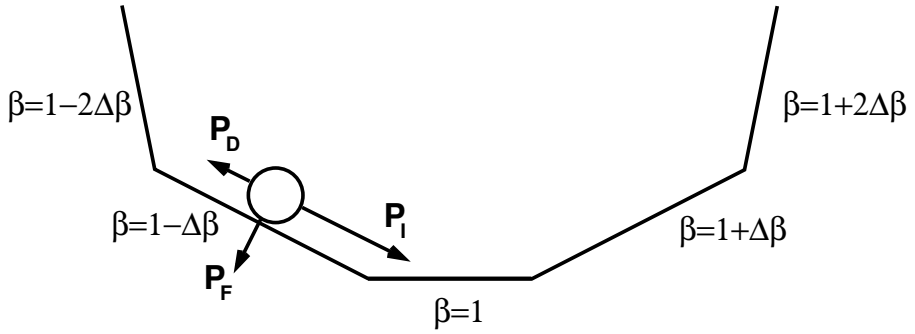


Figure A.5: A physical analogue of the AAR algorithm when k is given.

importantly, σ_0 depends on $\Delta\beta$ only and is used for selecting $\Delta\beta$.

To obtain the expression of σ_0, $\beta_n = 1 - \xi$ and $\beta_p = 1 - \xi + \Delta\beta$ with $0 < \xi < \Delta\beta$ are defined as the two states which are closest to 1. Because β is swapped either β_n or β_p, the average duration of β stays in both states are required to evaluate σ_0. The average duration can be given as

$$T(\beta) = -\int_0^\infty k \frac{dP_F(\beta)}{dk} dk \tag{A.11}$$

Let we name the average duration of β stays in β_n is T_n, and the average duration of β stays in β_p is T_p. Then we have

$$\frac{T_p}{T_n} \approx \frac{\beta_n}{\beta_p} = \frac{\xi}{\Delta\beta - \xi} \tag{A.12}$$

And the root-mean-square deviation when ξ is given is

$$\sigma_0 = \sqrt{\xi^2 \frac{T_n}{T_n + T_p} + (\xi - \Delta\beta)^2 \frac{T_p}{T_n + T_p}} = \sqrt{\xi(\Delta\beta - \xi)} \tag{A.13}$$

Furthermore, the root-mean-square error when ξ is uniformly distributed from 0 to $\Delta\beta$ is

$$\sigma_0 = \sqrt{\int_0^{\Delta\beta} \frac{1}{\Delta\beta} \xi(\Delta\beta - \xi) d\xi} = \frac{\Delta\beta}{\sqrt{6}} \tag{A.14}$$

This equation is repeated in (2.28) and matches the result of Figure 2.15.

A.0.2 The Second-Order DSM

The PDF of $s_j[k]$, $f_{s_j}(x)$, is necessary to decide N_{th_j} of CP_j. Since the stochastic behavior of a DSM in cascade with an AAR-based CP has been discussed adequately in previous

section as well as illustrated in Figure A.2. We need mention here only that, $f_{s_1}(x)$ is equal to (A.8) if we replace f_q and $\dot{s}$ with f_{q_1} and $\dot{s_1}$ respectively. However, the PDF of $s_2[k]$, $f_{s_2}(x)$, demands further discussion for deciding N_{th_2} of CP_2. Because the main difference between CP_1 in Figure 2.19 and CP_2 in Figure 3.7 is that, $x[k]$ is a narrow-band signal but $e_2[k]$ is a white noise. So the contribution of $e_2[k]$ should be combined with the contribution of $e_1[k]$, rather than be treated as (A.5). Repeating the deduction of (A.6), the noise power coefficient of CP_2 is expressed as

$$\begin{aligned}\sigma_{cp_2}^2 &= \frac{1}{12}\cdot\sum_{n=0}^{\infty}\left|Z^{-1}\left\{\sum_{m=0}^{\frac{D_{g_2}f_s}{2f_{q_2}}-1} z^{-m}\left[R+\mathrm{CTF}_2(z)\right]\right\}\right|^2 \\ &= \frac{\frac{D_{g_2}f_s}{2f_{q_2}}}{12}R+\frac{1}{12}\cdot\sum_{n=0}^{\infty}\left|Z^{-1}\left\{\sum_{m=0}^{\frac{D_{g_2}f_s}{2f_{q_2}}-1} z^{-m}\mathrm{CTF}_2(z)\right\}\right|^2\end{aligned} \tag{A.15}$$

where R is the ratio of the LSB of sub-ADC2 to the LSB of sub-ADC. Apply a random walk model on the CP_2. After $\frac{2f_{q_2}}{f_s}k$ steps for accumulation, $f_{s_2}(x)$ is found to be

$$\begin{aligned}f_{s_2}(x) &= \delta(x-\dot{s_2}k) * \mathcal{N}(0,\sigma_{cp_2}^2\cdot\frac{2f_{q_2}}{f_s}k) \\ &= \mathcal{N}(x-\dot{s_2}k,\sigma_{cp_2}^2\cdot\frac{2f_{q_2}}{f_s}k)\end{aligned} \tag{A.16}$$

Once $f_{s_1}(x)$ and $f_{s_2}(x)$ are available, the probability of different state of $s_j[k]$ can be calculated to ensure the relevant value of N_{th_j}.

Bibliography

[1] B. Murmann, P. Nikaeen, D. J. Connelly, and R. W. Dutton, "Impact of scaling on analog performance and associated modeling needs," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 2160–2167, Sept. 2006.

[2] I. A. Young, "Analog mixed-signal circuits in advanced nano-scale CMOS technology for microprocessors and SoCs," in *European Solid-State Circuits Conference (ESSCIRC)*, Sept. 2010, pp. 61–70.

[3] F. Ellinger, M. Claus, M. Schroter, and C. Carta, "Review of advanced and beyond CMOS FET technologies for radio frequency circuit design," in *SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference (IMOC 2011)*, Oct. 2011, pp. 347–351.

[4] X. Peng, W. Sansen, L. Hou, J. Wang, and W. Wu, "Impedance adapting compensation for low-power multistage amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 2, pp. 445–451, Feb. 2011.

[5] P. J. Hurst, R. A. Levinson, and D. J. Block, "A switched-capacitor delta-sigma modulator with reduced sensitivity to op-amp gain," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 6, pp. 691–696, June 1993.

[6] L. Fang and K. S. Chao, "A gain-compensated switched capacitor integrator," in *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 1998, pp. 229–232.

[7] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp

imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[8] H. Yoshizawa, T. Yabe, and G. C. Temes, "High-precision switched-capacitor integrator using low-gain opamp," *Electronics Letters*, vol. 47, no. 5, p. 315, Mar. 2011.

[9] T. Musah and U.-K. Moon, "Correlated level shifting integrator with reduced sensitivity to amplifier gain," *Electronics Letters*, vol. 47, no. 2, p. 91, Jan. 2011.

[10] H. Huang and E. K. F. Lee, "A 1.2V direct background digital tuned continuous-time bandpass sigma-delta modulator," in *European Solid-State Circuits Conference (ESSCIRC)*, Sept. 2001, pp. 526–529.

[11] C.-Y. Lu, J. F. Silva-Rivas, P. Kode, J. Silva-Martinez, and S. Hoyos, "A sixth-order 200 MHz IF bandpass sigma-delta modulator with over 68 dB SNDR in 10 MHz bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1122–1136, June 2010.

[12] Y.-S. Shu, B.-S. Song, and K. Bacrania, "A 65nm CMOS CT $\Delta\Sigma$ modulator with 81dB DR and 8MHz BW auto-tuned by pulse injection," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, Feb. 2008, pp. 500 –631.

[13] A. R. Duggal, S. Sonkusale, and J. Lachapelle, "Calibration of delta-sigma data converters in synchronous demodulation sensing applications," *IEEE Sensors Journal*, vol. 11, no. 1, pp. 16–22, June 2011.

[14] S.-C. Lee and Y. Chiu, "Digital calibration of nonlinear memory errors in sigma-delta modulators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 9, pp. 2462–2475, Nov. 2010.

[15] K. A. O'Donoghue, P. J. Hurst, and S. H. Lewis, "A digitally corrected 5-mW 2-MS/s SC $\Delta\Sigma$ ADC in 0.25- μm CMOS with 94-dB SFDR," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 11, pp. 2673–2684, Nov. 2011.

[16] B. Carlton, H. Lakdawala, E. Alpman, J. Rizk, Y. Li, B. Perez-Esparza, V. Rivera, C. Nieva, E. Gordon, P. Hackney, C.-H. Jan, I. Young, and K. Soumyanath, "A 32nm, 1.05V, BIST enabled, 10-40MHz, 11-9 bit, 0.13mm^2 digitized integrator MASH $\Delta\Sigma$ ADC," in *Symposium on VLSI Circuits*, June 2011, pp. 36–37.

[17] S. Lee, J. Chae, M. Aniya, S. Takeuchi, K. Hamashita, P. K. Hanumolu, and G. C. Temes, "A double-sampled low-distortion cascade $\Delta\Sigma$ modulator with an adder/integrator for WLAN application," in *IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2011, pp. 1–4.

[18] P. Malla, H. Lakdawala, K. Kornegay, and K. Soumyanath, "A 28mW spectrum-sensing reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT $\Delta\Sigma$ ADC for 802.11n/WiMAX receivers," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, Feb. 2008, pp. 496–631.

[19] J. Paramesh, R. Bishop, K. Soumyanath, and D. Allstot, "An 11-Bit 330MHz 8X OSR $\Sigma\Delta$ modulator for next-generation wlan," in *Symposium on VLSI Circuits*, June 2006, pp. 166 –167.

[20] R. Schreier and G. C. Temes, *Understanding delta-sigma data converters*. IEEE press Piscataway, NJ, 2005.

[21] N. Maghari, S. Kwon, and U.-K. Moon, "74 dB SNDR multi-loop sturdy-mash delta-sigma modulator using 35 dB open-loop opamp gain," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 8, pp. 2212–2221, Aug. 2009.

[22] J. Silva, X. Wang, P. Kiss, U. Moon, and G. C. Temes, "Digital techniques for improved $\Delta\Sigma$ data conversion," in *IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2002, pp. 183 – 190.

[23] Z. Zhang, J. Steensgaard, G. C. Temes, and J.-y. Wu, "A 14-bit dual-path 2-0 MASH ADC with dual digital error correction," *Analog Integrated Circuits and Signal Processing*, vol. 59, no. 2, pp. 143–150, May 2009.

[24] L. J. Breems, R. Rutten, and G. Wetzker, "A cascaded continuous-time $\Delta\Sigma$ modulator with 67-dB dynamic range in 10-MHz bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2152–2160, Dec. 2004.

[25] L. J. Breems, R. Rutten, R. H. M. van Veldhoven, and G. van der Weide, "A 56 mW continuous-time quadrature cascaded $\Sigma\Delta$ modulator with 77 dB DR in a near Zero-IF 20 MHz band," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2696–2705, Dec. 2007.

[26] Y.-S. Shu, J. Kamiishi, K. Tomioka, K. Hamashita, and B.-S. Song, "LMS-based noise leakage calibration of cascaded $\Delta\Sigma$ continuous-time modulators," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 2, pp. 368–379, Feb. 2010.

[27] M. Bolatkale, L. J. Breems, R. Rutten, and K. A. A. Makinwa, "A 4 GHz continuous-time $\Delta\Sigma$ ADC with 70 dB DR and 74 dBFS THD in 125 MHz BW," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 1–12, Dec. 2011.

[28] V. Singh, N. Krishnapura, S. Pavan, B. Vigraham, D. Behera, and N. Nigania, "A 16 MHz BW 75 dB DR CT $\Delta\Sigma$ ADC compensated for more than one cycle excess loop delay," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 8, pp. 1884–1895, Aug. 2012.

[29] P. Witte, J. G. Kauffman, J. Becker, Y. Manoli, and M. Ortmanns, "A 72dB-DR $\Delta\Sigma$ CT modulator using digitally estimated auxiliary DAC linearization achieving 88fJ/conv in a 25MHz BW," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, Feb. 2012, pp. 154–156.

[30] L. Bos, G. Vandersteen, P. Rombouts, A. Geis, A. Morgado, Y. Rolain, G. Van der Plas, and J. Ryckaert, "Multirate cascaded discrete-time low-pass $\Delta\Sigma$ modulator for GSM/Bluetooth/UMTS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1198–1208, June 2010.

[31] K. Reddy and S. Pavan, "Fundamental limitations of continuous-time delta-sigma modulators due to clock jitter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 10, pp. 2184–2194, Oct. 2007.

[32] S. Goldberg, *Probability: An Introduction*. Dover Publications, 1986.

[33] R. Schreier, "On the use of chaos to reduce idle-channel tones in delta-sigma modulators," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 41, no. 8, pp. 539–547, Aug. 1994.

[34] C.-C. Huang and J.-T. Wu, "A background comparator calibration technique for flash analog-to-digital converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 9, pp. 1732–1740, Nov. 2005.

[35] C.-C. Huang, C.-Y. Wang, and J.-T. Wu, "A CMOS 6-Bit 16-GS/s time-interleaved ADC using digital background calibration techniques," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 848–858, Apr. 2011.

[36] M. Figueiredo, R. Santos-Tavares, E. Santin, J. Ferreira, G. Evans, and J. Goes, "A two-stage fully differential inverter-based self-biased CMOS amplifier with high efficiency," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 7, pp. 1591–1603, July 2011.

[37] W. M. Koe, F. Maloberti, J. Hochschild, S. Karthikeyan, and Y.-K. Park, "Digital scheme for quantizer and integrator swing reduction in multibit sigma-delta modulator," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2006, pp. 2981–2984.

[38] J. Silva and G. C. Temes, "Low-distortion delta-sigma topologies for MASH architectures," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2004, pp. I–1144 – I–1147.

[39] R. Baird and T. Fiez, "Linearity enhancement of multibit $\Delta\Sigma$ A/D and D/A converters using data weighted averaging," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 753–762, Dec. 1995.

[40] J. Silva, U. Moon, J. Steensgaard, and G. C. Temes, "Wideband low-distortion delta-sigma ADC topology," *Electronics Letters*, vol. 37, no. 12, pp. 737–738, June 2001.

[41] S. Rabii and B. Wooley, "A 1.8-V digital-audio sigma-delta modulator in 0.8-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 6, pp. 783–796, June 1997.

[42] H. Maarefi, A. Parsa, H. Hatamkhani, and D. Shiri, "A wide swing 1.5 V fully differential op-amp using a rail-to-rail analog CMFB circuit," in *The 45th Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2002, pp. I–105–I–108.

[43] K. Nam, S.-M. Lee, D. Su, and B. Wooley, "A low-voltage low-power sigma-delta modulator for broadband analog-to-digital conversion," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1855–1864, Sept. 2005.

[44] H. Park, K. Nam, D. Su, K. Vleugels, and B. Wooley, "A 0.7-v 870-μw digital-audio cmos sigma-delta modulator," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1078–1088, Apr. 2009.

[45] S.-J. Huang and Y.-Y. Lin, "A 1.2V 2MHz BW 0.084mm^2 CT $\Delta\Sigma$ ADC with -97.7dBc THD and 80dB DR using low-latency DEM," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, Feb. 2009, pp. 172–173,173a.

[46] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, Feb. 2007, pp. 252–253.

[47] B. Nikolic, V. Oklobdzija, V. Stojanovic, and M. Ming-Tak Leung, "Improved sense-amplifier-based flip-flop: design and measurements," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 6, pp. 876–884, June 2000.

[48] S.-C. Lee, B. Elies, and Y. Chiu, "An 85dB SFDR 67dB SNDR 8OSR 240MS/s $\Delta\Sigma$ ADC with nonlinear memory error calibration," in *Symposium on VLSI Circuits*, June 2012, pp. 164–165.

[49] J. Chae, S. Lee, M. Aniya, S. Takeuchi, K. Hamashita, P. K. Hanumolu, and G. C. Temes, "A 63 dB 16 mW 20 MHz BW double-sampled $\Delta\Sigma$ analog-to-digital converter with an embedded-adder quantizer," in *IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2010, pp. 1–4.

[50] P. Shettigar and S. Pavan, "Design techniques for wideband single-bit continuous-time $\Delta\Sigma$ modulators with FIR feedback DACs," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2865–2879, Dec. 2012.

[51] G. Taylor and I. Galton, "A reconfigurable mostly-digital $\Delta\Sigma$ ADC with a worst-case FOM of 160dB," in *Symposium on VLSI Circuits*, June 2012, pp. 166–167.

[52] M. Park and M. H. Perrott, "A 78 dB SNDR 87 mW 20 MHz bandwidth continuous-time $\Delta\Sigma$ ADC with VCO-based integrator and quantizer implemented in 0.13 μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3344–3358, Dec. 2009.

[53] K. Reddy, S. Rao, R. Inti, B. Young, A. Elshazly, M. Talegaonkar, and P. K. Hanumolu, "A 16-mW 78-dB SNDR 10-MHz BW CT $\Delta\Sigma$ ADC using residue-cancelling VCO-based quantizer," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2916–2927, Dec. 2012.

[54] Y.-S. Shu, J.-Y. Tsai, T.-Y. L. Ping Chen, and P.-C. Chiu, "A 28fJ/conv-step CT $\Delta\Sigma$ modulator with 78dB DR and 18MHz BW in 28nm CMOS using a highly digital multibit quantizer," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, Feb. 2013, pp. 268–269.

[55] B. Murmann, "ADC performance survey 1997-2012 (ISSCC and VLSI Symposium)." [Online]. Available: http://www.stanford.edu/ murmann/adcsurvey.html

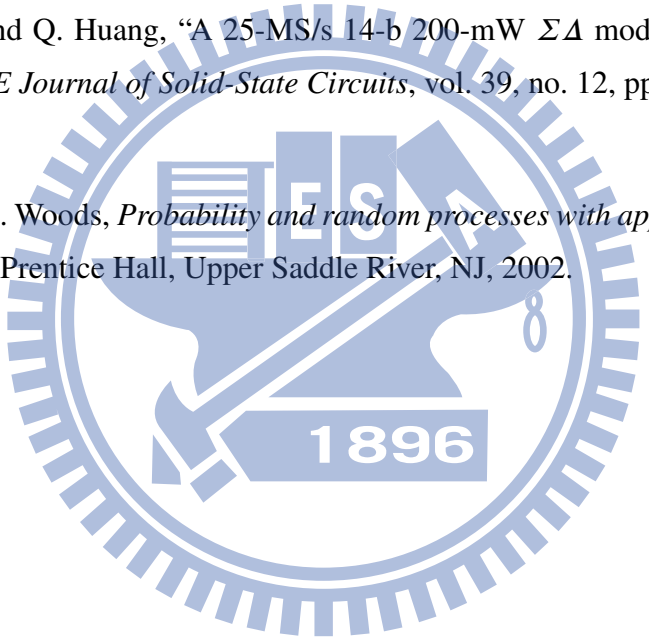
[56] K. Matsukawa, K. Obata, Y. Mitani, and S. Dosho, "A 10 MHz BW 50 fJ/conv. continuous time $\Delta\Sigma$ modulator with high-order single opamp integrator using optimization-based design method," in *Symposium on VLSI Circuits*. IEEE, June 2012, pp. 160–161.

[57] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani, "A 20-mW 640-MHz CMOS continuous-time $\Sigma\Delta$ adc with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2641–2649, Dec. 2006.

[58] W. Yang, W. Schofield, H. Shibata, S. Korrapati, A. Shaikh, N. Abaskharoun, and D. Ribner, "A 100mw 10mhz-bw ct $\Delta\Sigma$ modulator with 87dB DR and 91dBc IMD," in *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb. 2008, pp. 498–631.

[59] P. Balmelli and Q. Huang, "A 25-MS/s 14-b 200-mW $\Sigma\Delta$ modulator in 0.18- μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2161–2169, Dec. 2004.

[60] H. Stark and J. Woods, *Probability and random processes with applications to signal processing*. Prentice Hall, Upper Saddle River, NJ, 2002.



Vita

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Publication List

- Journal Paper:
  - **Su-Hao Wu** and Jieh-Tsorng Wu, " A 81-dB Dynamic Range 16-MHz Bandwidth $\Delta\Sigma$ Modulator Using Background Calibration," to be published in *IEEE Journal of Solid-State Circuits*, September, 2013.
- Conference Paper:
  - **Su-Hao Wu** and Jieh-Tsorng Wu, " Background Calibration of Integrator Leakage in Discrete-Time Delta-Sigma Modulators," *proceedings in 11th IEEE International New Circuits and Systems Conference (NEWCAS)*, Paris, France, 16-19 June, 2013.
- Patent:
  - **Su-Hao Wu** and Jieh-Tsorng Wu, "Background integration-leakage calibration technique for delta-sigma modulators," Taiwan patent pending.