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碩士論文

前表面場與氧化鋁鈍化對於交指背接觸電極矽晶太陽能電池之研究

A Study of Front Surface Field Passivation and Al_2O_3 Passivation on Interdigitated Back Contact Back Junction Silicon Solar Cell

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中華民國　一百零二　年　七　月

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摘要

近年來太陽能電池的研究正在如火如荼的進行中, 在眾多種太陽能電池中, 單晶矽太陽能電池的技術發展最為成熟, 在現階段也是最適合量產的太陽能電池, 目前以 PERL 結構製成的太陽能電池效率已經可以高達 25%, 。

交指背接觸電極矽晶太陽能電池則是被看好極具有成為高效能太陽能電池的潛力，且較易於模組化的特性則是非常適合大量生產與應用，基於上述原因，交指背接觸電極太陽能電池的研究也是相當熱門的課題。但是由於載子傳輸距離較傳統結構長的特性，表層鈍化即成為了最重要的研究方向。

在我們的研究之中分別對於前表面場的鈍化效果以及背面硼摻雜的射極區鈍化進行測試，在前表面場鈍化處理上，我們採用了不同溫度的磷擴散以及濕氧化處理時間還有磷玻璃的移除與否進行了探討，藉由少數載子存活時間量測找出最優化的處理。

背面硼摻雜射極區的鈍化探討中,則是討論了氧化鋁的使用，以及氧化鋁在不同溫度的退火後對於射極鈍化的影響,藉由少數載子存活時間量測找出最優化的條件。上述的條件皆實際採用在交指背接觸電極矽晶太陽能電池中，而所得到的最高效率為 7.59%，

A Study of Front Surface Field Passivation and Al_2O_3 Passivation on Interdigitated Back Contact Back Junction Silicon Solar Cell

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Abstract

In recent years, the study of solar cell is a big issue, in numerous species of solar cells, single crystalline silicon solar cell is well developed and is appropriate to mass production, the crystalline silicon solar cell made in PERL structure has already achieved 25%

Interdigitated back contact back junction silicon solar cell has potential to achieve high efficiency, and has benefits for mass production due to the feature of easily linking in module, for the reasons we mentioned above, interdigitated back contact back junction silicon solar cell is a popular research. However the longer transport distance for carriers makes surface passivation a crucial issue for interdigitated back contact back junction silicon solar cell.

In our research, front surface field and p^+ emitter passivation was investigated. For front surface field passivation, $POCl_3$ diffusion at different temperature with different wet oxide growing time and PSG

preservation were tested by lifetime measurement, the optimism condition was discovered

For p^+ emitter passivation, application of Al_2O_3 and annealing at different temperature was also investigated by lifetime measurement and the optimism is discovered

These treatments are applied to Interdigitated back contact back junction silicon solar cell in our experiment, the best efficiency is 7.57%.

誌謝

在求學的路上，最感謝的是家人們對我無條件的支持與付出，尤其感謝父親解定國以及母親楊繼芬從小對我的諄諄教誨與照顧。

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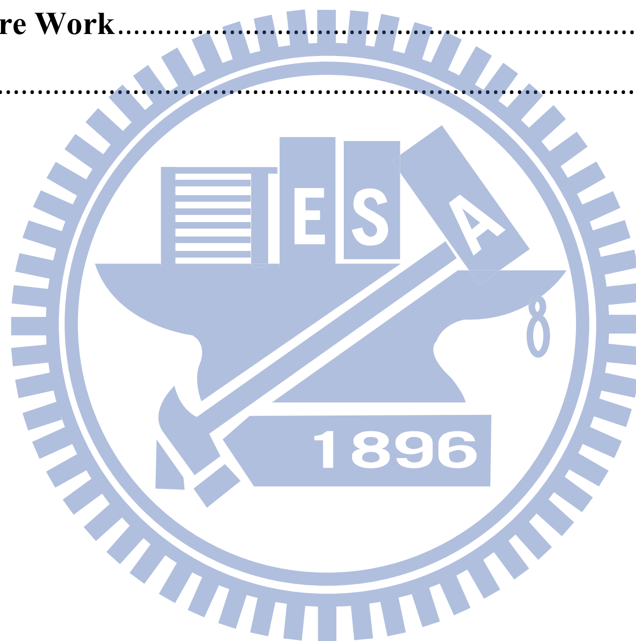

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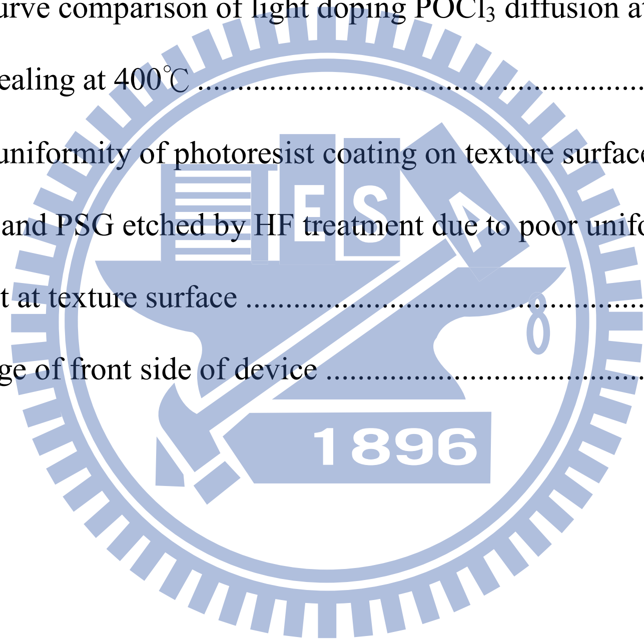

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Chapter 1

Introduction

1.1 Why solar cells?

Fossil has been used as energy resource since 18th.Until now, fossil is the crucial energy in modern world. However, the storage of fossil is not unlimited. Although limit has been modified year by year due to the technology of fossil exploitation is improved, development of substitutional energy is still necessary, it is also a big issue to discover a new type of energy that we would not concern about the influence to the environment and might be running out one day. In many of the candidates, solar power is attractive due to solar power that we could receive on earth is enormous, the annual mount of energy earth receives exceeds the power human beings consume per year, and we can keep using this kind of power until sun comes to its end no doubt. Direct use of solar power is appealing when the energy demand increasing year by year, and solar cell is exact the device that fits all requirements we need as substitutional energy.

Directional use of sun power, turning sun light into electricity, and less pollution for environment, solar cell is the candidate energy in the future according to the above advantages. In this way, plenty of materials have been researched for fabrication of solar cells.

For year 2012, the cumulative PV capacity exceeded 100-gigawatt(GW) installed electrical power mark, and save more than 50million tones of CO_2 each year, the capacity is equal to 16 coal power plants. In PV industry market, Europe remains the largest region in cumulative installed capacity, with more than 70GW in 2012, due to government subsidy policy, shown in Fig. 1.1 [1.1], other market such as China, America, APAC grows year by year. When the Europe market is near saturation, other place we mentioned above would play important roles in the future.

1.2 Classification of Solar Cell

We could classify solar cells into three parts, shown in Fig. 1.2 [1.2], there are silicon type, III-V type, and organic type, we will introduce them respectively, world record is shown in Fig. 1.3 [1.3].

Silicon is an attractive material for researching due to the fabrication

process is matched to traditional CMOS technology, and abundant of content on earth. According to all the reasons above, Silicon solar cell fabrication process is easier to be commercialized and the cost is lower than any other material.

III-V type solar cell could achieve high efficiency, and epitaxy technique is adopted to manufacture III-V type solar cell, many structure could be realized by epitaxy, such as muti-junction, hetero-junction, quantum well, quantum dot, super lattice….etc. It is proved that the only way to break through the limit of single junction material is multi-junction which is made by specific III-V compounds stacking on glass substrate as result of tandem cell. Due to the efficiency of single junction solar cell is limited in theory, multi-junction solar cell has been developed, photon with different energy can be absorbed by different band gap material separately, reducing the energy waste which would be released by phonon, however, tunneling mechanism is applied between different junction to collect photo-generation current, then the current flowed through every junction is required to be matched, otherwise efficiency loss would occur. We understand that the sunlight changes all the time for the same location on earth, hence the composition of sunlight

changes constantly, which results in different amount of photo-generation current for each junction of tandem cell, in addition to the above situation, III-V material is more expensive than silicon, therefore III-V is not appropriate to be commercialized temporarily.

Organic solar cell is under development nowadays, it is believed as a potential candidate of the future due to the convenience of large scale production, low cost and flexibility of application, the best record efficiency of organic solar cell has already broken through 10% by Mitsubishi Chemical, sub-model efficiency is about 7 % (15 series cell) [1.4]. The production ratio of organic solar cell is growing in the world photovoltaic market, it might become the major product in the future due to the advantages we mentioned above.

1.3 Development of Silicon Solar Cell

The first Si solar cell device was invented by Russell Ohl of Bell Laboratories at 1940-1950, adopted the band bending created by different impurity doping, efficiency is about 1 %,shown in Fig. 1.4 [1.5].

Silicon solar cell was developed rapidly at 1950s due to the space race between USA and Soviet Union. Space ship and satellite demand

long-term power supply, and sunlight is the reliable energy source in space, government also invested resources for solar cell research. Silicon solar cell for space industry had dominated the research of solar cell until 1970s.

In 1970s, terrestrial solar cell had been well developed. Metal fingers made by photolithography, heavy doped back surface field (BSF), pyramid-shaped texture was also introduced as a part of antireflection, silicon solar cell efficiency was increased obviously by the change we just mentioned above, shown in Fig. 1.5 [1.5], the best efficiency is 17% reported by Rittner and Arndt in 1976.

In 1980s, we started to focus on the recombination mechanism of the solar cell structure, for minimizing the high recombination velocity at the interface of silicon and metal, metal-insulator-NP (MINP) junction was invented, the carrier can be collected by metal finger according to tunneling mechanism, shown in Fig. 1.6 [1.5], the efficiency reached 18%.

Passivated emitter solar cell (PESC) was developed after MINP structure, the difference between PESC and MINP are simply front side texture and the opening at the front surface of metal and silicon oxide to

reduce the contact resistance, shown in Fig. 1.7 [1.5], the efficiency of PESC achieved 20.1% at 1985.

Passivated emitter and rear locally diffused (PERL) cells was invented by UNSW after PESC structure, this structure has an apparent change at rear surface, most of the rear surface is covered by oxide, point contact is adopted with heavy doped p^+ region to achieve superior back surface passivation than before, shown in Fig. 1.8 [1.5], PERL is still the best record for single crystalline silicon solar cell.

For nowadays, there are several points PV industry focuses on, which are improving efficiency, thinner substrate, efficiency stability under higher operating temperature and bifacial module. SANYO puts plenty of resources to research and develop a kind of solar cell which is called HIT solar cell matches the requirement of high efficiency, thinner substrate and bifacial module due to symmetrical structure. HIT solar cell adopts high quality but extra thin amorphous silicon (a-Si) layer to form hetero junction which is also applied for passivation at the interface of silicon substrate, for HIT solar cell, hetero junction treatment is the biggest issue which we put attention for optimization. The structure of HIT solar cell is shown in Fig. 1.9 [1.6], the substrate is covered by intrinsic amorphous

silicon at both side which is extremely thin, then p-type and n-type amorphous silicon is deposited at different side as emitter and back surface field (BSF), after TCO and metal electrode is formed at both front side and back side, HIT solar cell is completed. The standard HIT solar cell for large area (100 cm^2) has already reached 23% (V_{oc} > 700 mV, J_{sc}> 39 mA/cm^2, FF: 80 %), which has real potential for commercial production except for cost reason.

In recent years, n-type silicon substrate is suitable for IBC solar cells due to n-type silicon substrate has larger tolerance to common impurities such as Fe than p-type silicon substrate, and there is no light induced degradation at the same time. According to these two advantages, n-type silicon substrate has been adopted to achieve high efficiency solar cell.

1.4 Back contact and back junction solar cell

Back contact and back junction solar cell which is also called Interdigitated back contact (IBC) silicon solar cell is recognized as an option to achieved high efficiency. The structure is shown in Fig 1.10 [1.7].There are several advantages of IBC silicon solar cell, the major one is that there is no optical shading loss at the front side of IBC silicon solar

cell because of the absence of front metal finger which leads to a high photo-generated current, it also has benefit for optimizing front side surface passivation. In solar cell industry, photovoltaic module is the actual product for consumer instead of simply solar cell device. Photovoltaic module contains solar cell devices, electric circuit, epoxy board, glass, providing protection, self-cleaning ability for solar cell to extending the using lifetime. IBC solar cell is convenient to photovoltaic module owing to all the metal fingers are at the back side of the IBC solar cell. However, IBC solar cell structure is more complex than traditional silicon solar cell, involves multiple photolithography masking technology which is accompanied with higher costs and longer process time.

1.5 Motivation

Obviously, interdigitated back contact (IBC) silicon solar cell is one of the best choices for fitting in module, combining two demands of commercial PV device, which are high efficiency and low cost due to simplification of linking other device in the module, according to this reason, the principle of interdigitated back contact (IBC) silicon solar cell is worth-researching.

To realize the substitution of main energy generation methods by PV industry, the theory of solar cell operation must be well-understood, hence we decided to put attention on passivation research. Although the process we will show in the subsequent chapter adopts photolithography, which is almost eliminated in PV industry except for lab research. Some basic physical mechanism such as field effect passivation provided by different doping profile, or chemical passivation provided by Al_2O_3 and SiNx at the back side are what we want to figure out in our research, we hope this study would have contribution to PV industry in the future.

1.6 Organization of the thesis

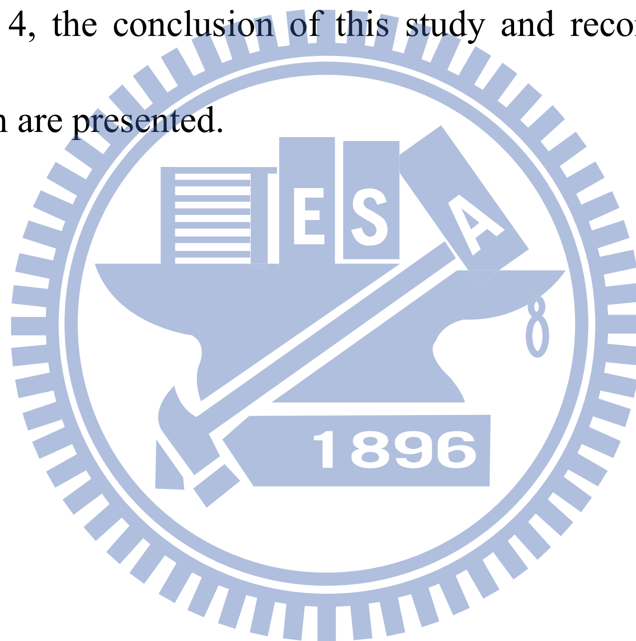
In Chapter 1, a quick introduction about the general background and the development of solar cell are described. Readers could have some initial understanding of the structure evolution of silicon solar cell (ex. black cell, MINP, PESC, PERL, MIS, HIT and IBC). At the end of Chapter 1, we would introduce the reason of our research.

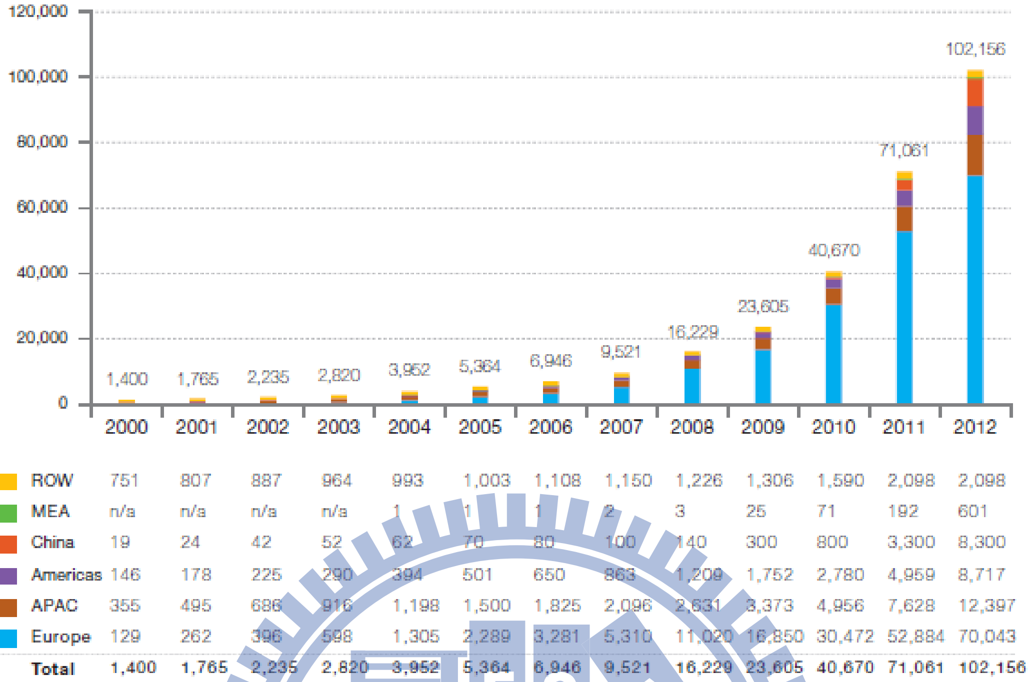
In Chapter 2, we report the basic principle of why solar cell would generate electricity and the significance of each parameter which appears regularly. In addition, the measuring equipment is also presented to let readers understand how we measure the device, at last, device fabrication

will be shown.

In Chapter 3, the detail study about interdigitated back contact (IBC) silicon solar cell with different $POCl_3$ temperature for forming front surface field (FSF), and different Al_2O_3 annealing temperature arepresented, we would discuss the impact of the changes we mentioned above by I-V curve, implied open circuit voltage.

In Chapter 4, the conclusion of this study and recommendation for further research are presented.





	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012
ROW	751	807	887	964	993	1,003	1,108	1,150	1,226	1,306	1,590	2,098	2,098
MEA	n/a	n/a	n/a	n/a	1	1	1	2	3	25	71	192	601
China	19	24	42	52	62	70	80	100	140	300	800	3,300	8,300
Americas	146	178	225	290	394	501	650	863	1,209	1,752	2,780	4,959	8,717
APAC	355	495	686	916	1,198	1,500	1,825	2,096	2,631	3,373	4,956	7,628	12,397
Europe	129	262	396	598	1,305	2,289	3,281	5,310	11,020	16,850	30,472	52,884	70,043
Total	1,400	1,765	2,235	2,820	3,952	5,364	6,946	9,521	16,229	23,605	40,670	71,061	102,156

Fig. 1.1 cumulative PV capacity for each year [1.1]

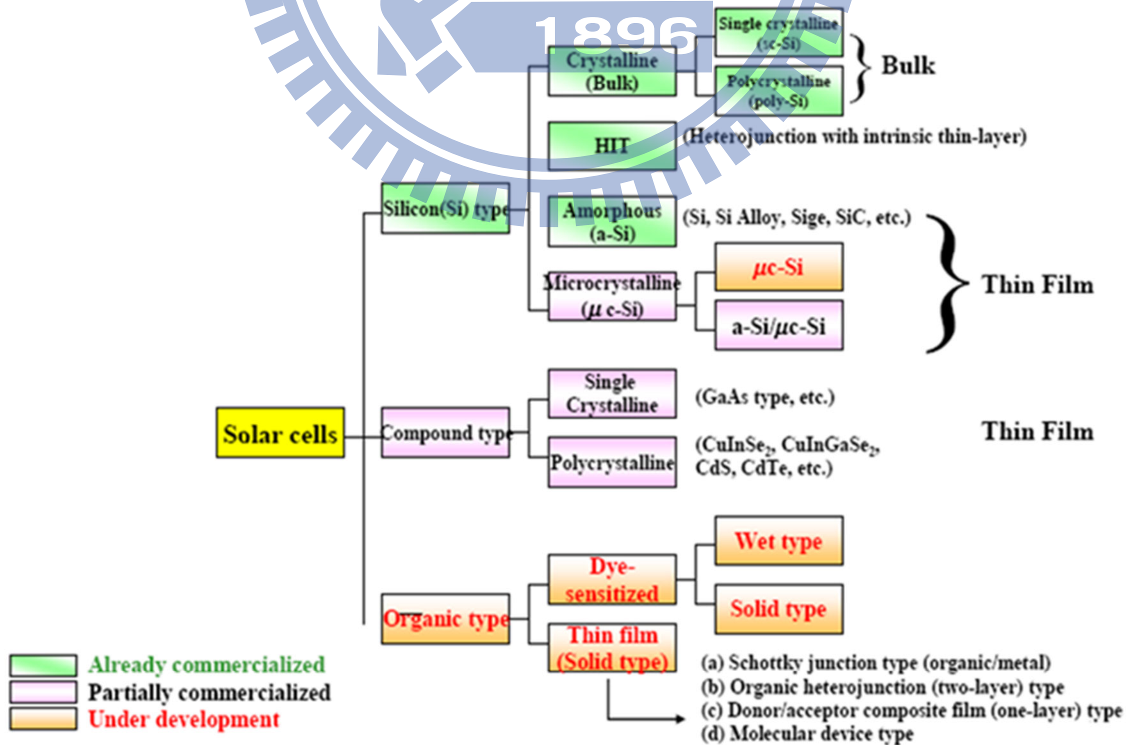


Fig. 1.2 classification of solar cell [1.2]

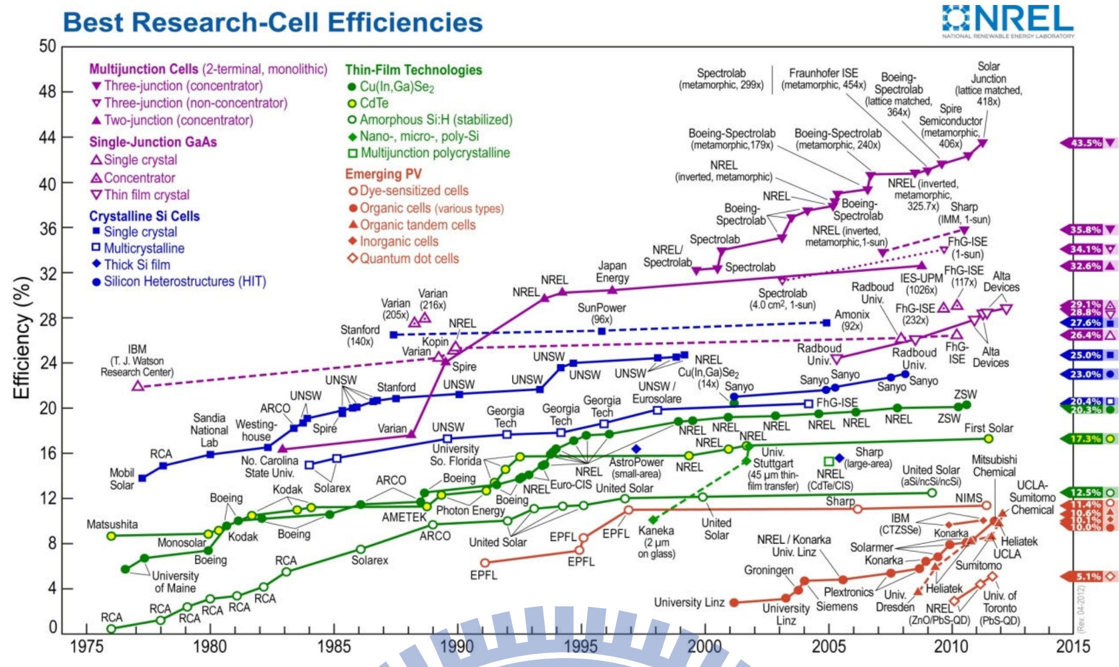


Fig. 1.3 world record for each type of solar cell [1.3]

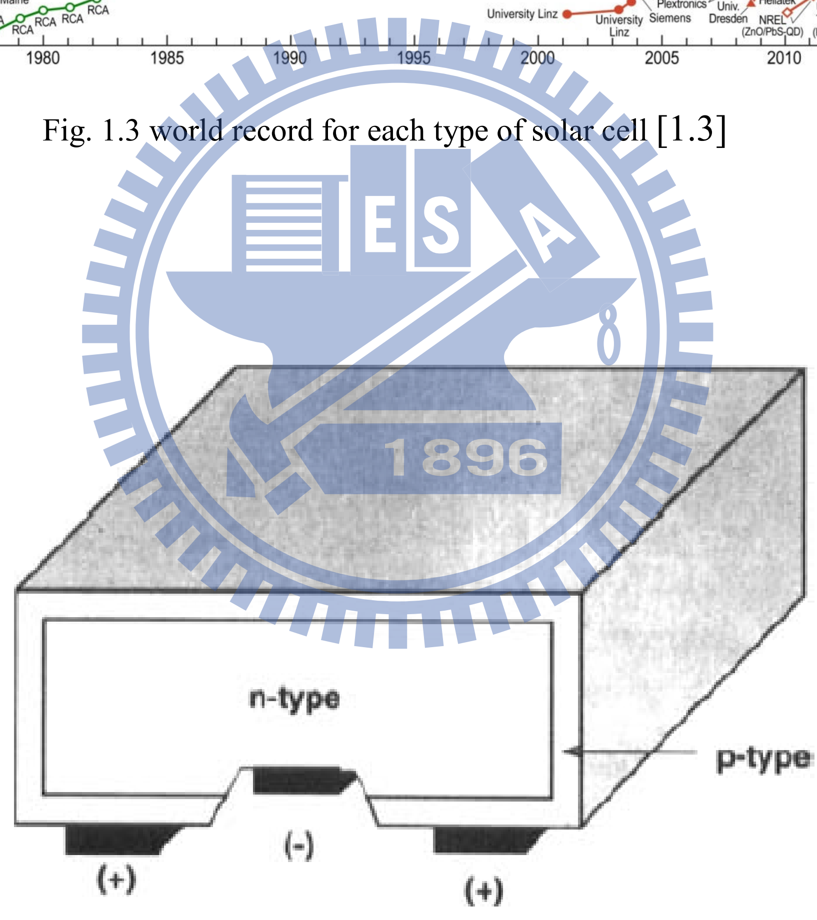


Fig. 1.4 first solar cell invented in Bell Lab [1.5]

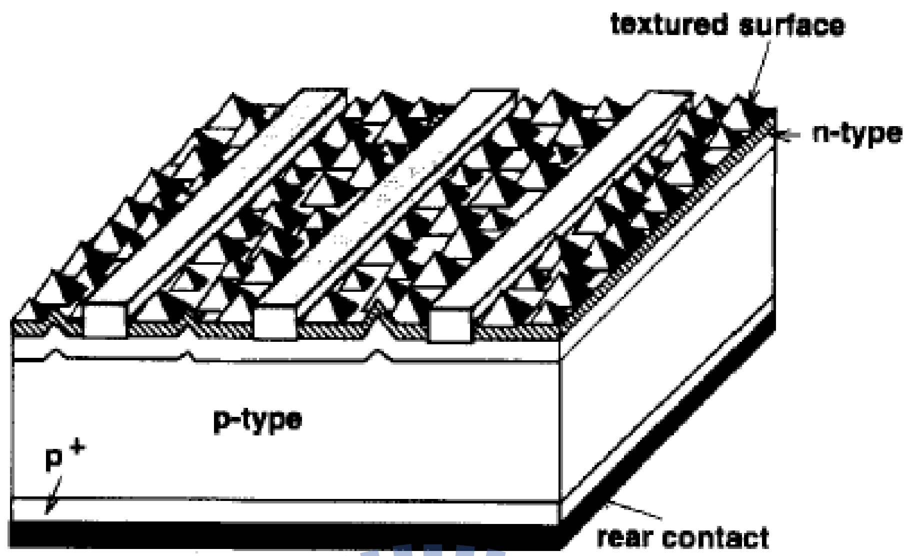


Fig. 1.5 terrestrial solar cell [1.5]

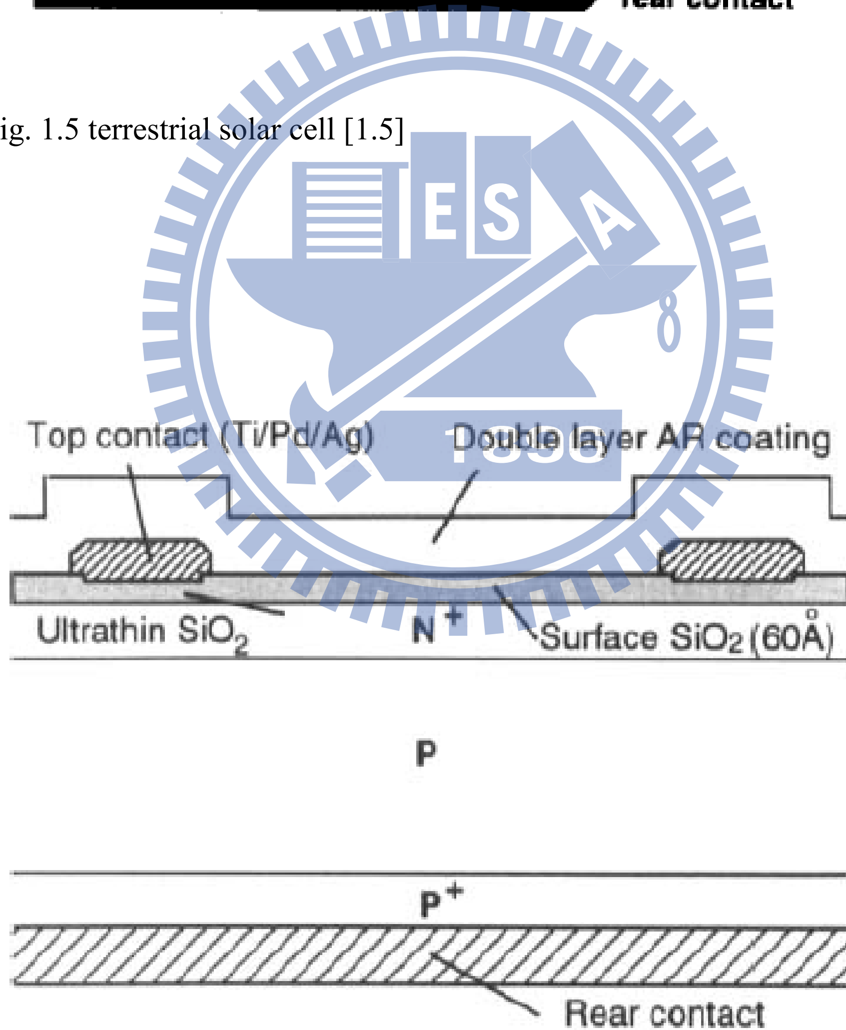


Fig. 1.6 MINP solar cell [1.5]

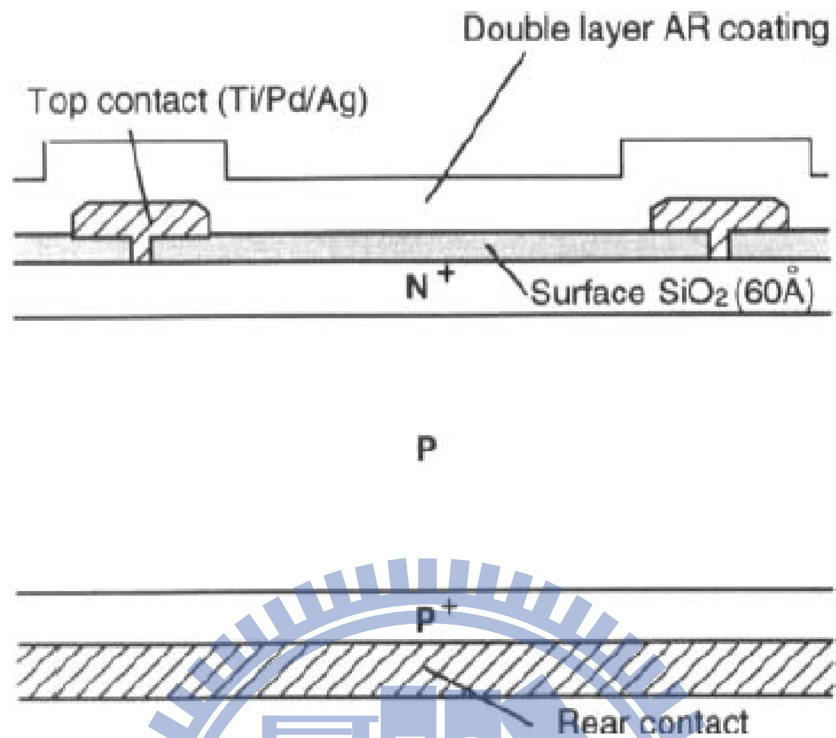


Fig. 1.7 PESC solar cell [1.5]

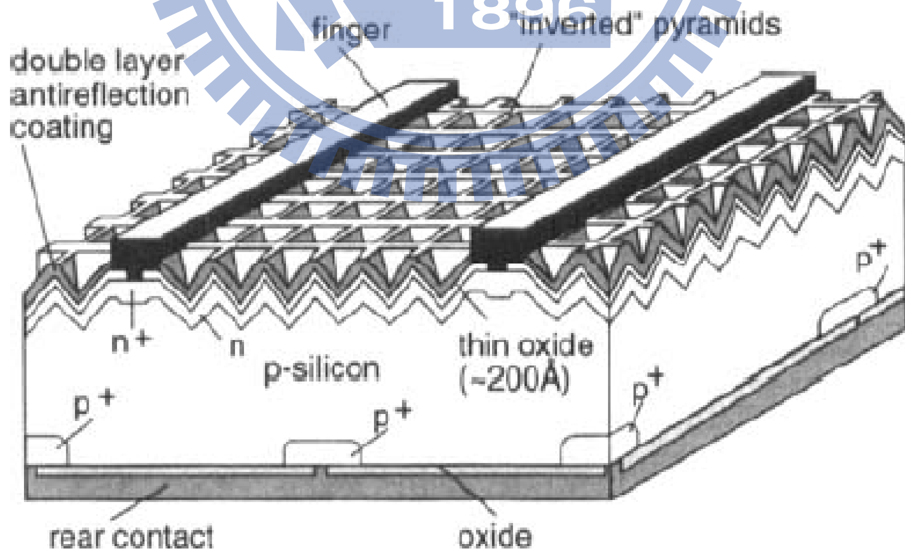


Fig. 1.8 PERL solar cell [1.6]

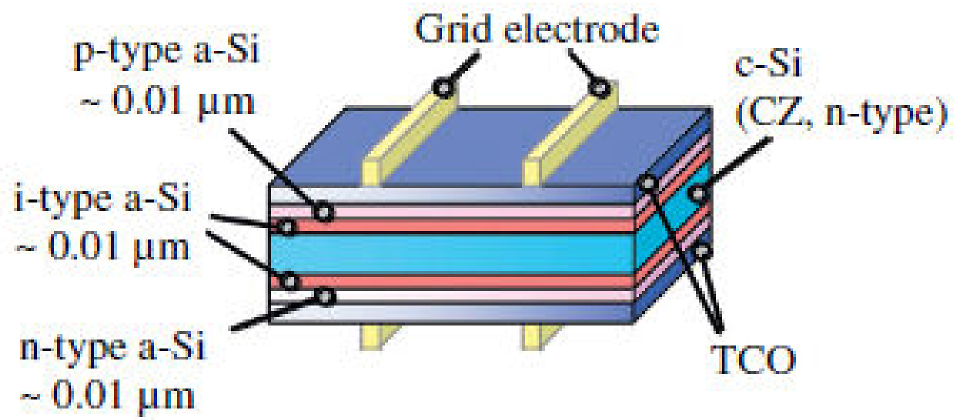


Fig. 1.9 HIT solar cell [1.7]

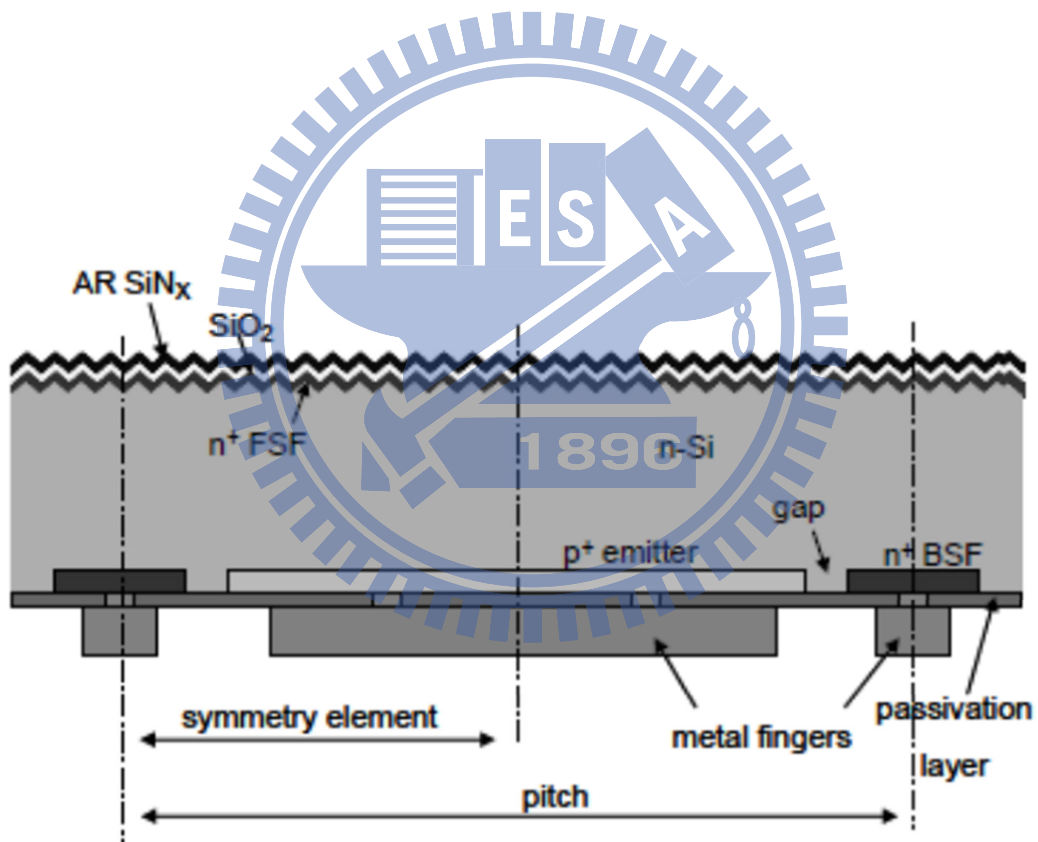


Fig. 1.10 IBC solar cell [1.8]

Chapter 2

Basic Principle of Silicon Solar Cell

2.1 Solar spectrum

Obviously, the output power of solar cell is dependent with the input light spectrum and light intensity, the same solar cell device provides different power according to location where device is installed on earth. Hence the understanding of solar spectrum is important to photovoltaic device researchers.

In general, we assume a plane is at the midpoint of the distance between atmosphere and sun, the direction of this plane is vertical to the sunlight and the emission power is a constant per unit area. We call this power intensity air mass zero (AM0). The definition of air mass is ratio of the actual distance and the shortest distance between sun and observer. As shown in Fig. 2.1 [2.1] and eq. 2-1.

$$AM = 1/\cos\theta \dots\dots\dots\dots\dots\dots\dots \text{(eq. 2-1)}$$

The emission of sunlight would decay by many reasons. For example, atmosphere would absorb specific spectrum of sunlight. AM 1.5 is the standard measurement condition we adopted to test the solar cell device,

shown in Fig. 2.2 [2.2].

2.2 p-n diode model

p-n junction diode is the basic structure for semiconductor device, the major product such as MOSFET, memory contain p-n junction, for photovoltaic device, p-n junction is applied to separate photo-generation electron-hole pair to prevent immediately carrier recombination, based on the above reasons, the mechanism of p-n junction must be well-understood.

P-n junction is made by n-type doping in p-type wafer or p-type doping in n-type wafer. In thermal equilibrium, band-bending and built-in electric field are formed at the interface because Fermi level must be equal in this condition, which block electrons flow from n-type region to p-type region and holes flow from p-type region to n-type region. For ordinary operation of p-n diode, positive voltage is applied to p-type region, and n-type region is grounded, therefore the Fermi level in p-type region is lower than n-type region, and potential barrier is reduced, electrons and holes would diffuse across depletion region, hence the current occurs. The equation which describes voltage-current relation of

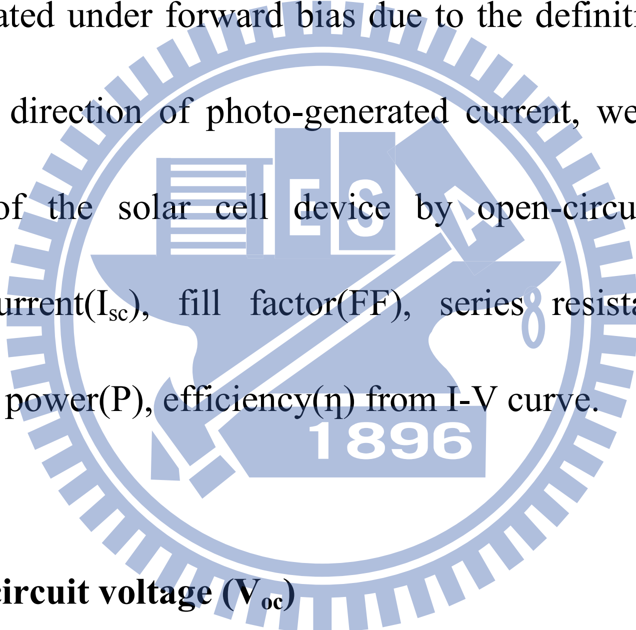
p-n diode is

$$I = I_0(\exp\left(\frac{qV}{kT}\right) - 1)\text{............}(eq.\ 2\text{-}2)$$

Where I_0 we called saturation current.

2.3 I-V curve of solar cell

I-V curve of solar cell is similar but still different from the normal p-n diode operated under forward bias due to the definition of solar cell model and the direction of photo-generated current, we could analysis characteristic of the solar cell device by open-circuit voltage(V_{oc}), short-circuit current(I_{sc}), fill factor(FF), series resistance(R_s), shunt resistance(R_{sh}), power(P), efficiency(η) from I-V curve.



2.3.1 open-circuit voltage (V_{oc})

The formula of the relationship of solar cell is

$$I = I_0(\exp\left(\frac{qV}{nkT} - 1\right) - I_L)\text{.......}(eq.\ 2\text{-}4)$$

I_L represents photo-generation current, I_0 means saturation current, we could realize the similarity of the equation for p-n diode and solar cell, except for photo-generation current, and the direction of photo-generation current is opposite to forward bias current of p-n diode. According to

definition, open circuit means there is no current in the circuit, then V_{oc} is the output voltage that solar cell supplies when the current is zero in the circuit under illumination.

$$V_{oc} = \frac{kT}{q}\ln(\frac{I_L}{I_0} + 1) \ldots\ldots\ldots\ldots\ldots\ldots (eq. 2-5)$$

or

$$V_{oc} = \frac{kT}{q}\ln[\frac{\Delta n(N_A+\Delta n)}{n_i^2}] \ldots\ldots\ldots\ldots\ldots (eq. 2-6)$$

Open circuit voltage also has something to do with band gap, we have already understood that n_i^2 is proportional to $\exp(\frac{-E_g}{kT})$, hence we choose large band gap material as the light absorption layer of solar cell, open circuit voltage would be increased in theory.

The limit of open circuit voltage is connected with recombination rate of electron hole pairs, for an ideal solar cell, there are two kinds of recombination mechanism exist, radiative recombination and Auger recombination. For silicon solar cell which is 150 μm thick, and base doping is $5e15cm^{-3}$, the limit of open circuit voltage is about 740 mV.

2.3.2 short-circuit current (I_{sc})

Short circuit means the supplied voltage of the circuit is zero, we could understand the ideal value of short circuit current must be the total

photo-generation current, hence I_{sc} is affected by photon flux of incident light, and the bang gap of material, the reason why band gap affects I_{sc} is that the production of electron-hole pair is determined by the photon which energy is larger than band gap for direct band gap material. For indirect band gap material, incident photon energy still dominates the generation of electron-hole pair although phonon participates one part of this process. Carrier recombination at the interface and bulk also cause I_{sc} loss. For silicon solar cell which is 150 μm thick, and base doping is 5e15cm^{-3}, the limit of open circuit voltage is about 44 mA under AM1.5G spectrum illumination

2.3.3 Series Resistance

Current flowing in the circuit accompanies with energy consumption due to series resistance. However, solar cell is a device of energy generation, unnecessary energy loss during carrier transport must be reduced. To satisfy this demand, we have to cut down series resistance as much as possible. The source of series resistance is contact resistance, bulk resistance, metal finger resistance. Circuit model is shown in Fig. 2.3.

The equation to describe the impact of series resistance for solar cell operation is

$$\mathrm{I} = I_L - I_0(\exp(\frac{qV+IR_s}{nkT})\text{.............(eq. 2-7)}$$

High series resistance influences fill factor, even short circuit current if series resistance is extremely high.

2.3.4 Shunt Resistance

The presence of low shunt resistance is due to the poor design of solar cell or mistake happens during manufacture, substitutional path is provided for photo-generation current would cause serious leakage during device operation and create power loss. The equation to describe the impact of shunt resistance for solar cell operation is

$$\mathrm{I} = I_L - I_0 \exp\left(\frac{qV}{nkT}\right) - \frac{V}{R_{sh}}\text{.......(eq. 2-8)}$$

Circuit model is shown in Fig. 2.4.

2.3.5 Fill Factor

Fill Factor is the relationship between ideal diode and actual diode, due to the effect of series resistance and shunt resistance, shown in Fig. 2.5. High series resistance and low shunt resistance lead to low Fill Factor,

which means how solar cell is far from the perfect p-n diode. In other words, Fill Factor is the ratio of max power ($V_{mp} \times I_{mp}$) and to $V_{oc} \times I_{sc}$, we define Fill Factor as

$$\mathrm{F.F} = \frac{V_{mp} - I_{mp}}{V_{oc} - I_{sc}} \ldots\ldots\ldots\ldots\ldots\ldots\text{(eq. 2-9)}$$

2.3.6 Efficiency

The definition of efficiency is the ratio of power that solar cell generates to the power of light that illuminates solar cell, the corresponding equation is

$$\eta = \frac{F.F \times V_{oc} \times I_{sc}}{P_{in}} \ldots\ldots\ldots\ldots\ldots\ldots\text{(eq. 2-10)}$$

2.4 Quantum Efficiency (QE)

Quantum efficiency is the relation of carriers collected by the solar cell device and incident photons, we analyze quantum efficiency by different wavelength to understand which part of wavelength is well absorbed by solar cell, if the solar cell absorbs all photons we provides and transform into electron-hole pairs, and all collected by the finger eventually, then quantum efficiency must be 100% for every wavelength, and the shape of the curve is rectangle, shown in Fig. 2.6. There are two

kind of Quantum efficiency, external quantum efficiency and internal quantum efficiency, external quantum efficiency contains the consideration of reflection and transmission, internal quantum efficiency shows the quantum efficiency after reflection and transmission, in other words, carrier recombination at the front, back interface and recombination in the bulk dominates the carrier collection inside the solar cell. We could calculate internal quantum efficiency from the data of external quantum efficiency and reflection and transmission.

2.5 Mechanism of Efficiency Loss

Solar cell efficiency is limited due to many reasons, it is a key point to figure out what loss mechanism limits the efficiency of solar cell, then research the way to improve the solar cell device, no matter what structure we adopted or what mechanism we apply to refine our solar cell device.

Sub band gap loss is one of the major loss-mechanism, for instance, band gap of single crystalline silicon is 1.12 e V, the incident light almost would not be able to be absorbed if the wavelength is longer than 1200nm, in this situation most of the long-wavelength light is wasted.

Lattice thermalisation loss is also an important loss mechanism, if the incident light energy is higher than the material band gap, the electron-hole pair which is generated by photon would carry high energy, the energy would be released as phonon until the electron falls to conduction band edge.

Junction loss describes the phenomenon which represents the energy loss when carriers pass through p-n junction, band bending of p-n junction band diagram is applied to separate electron-hole pair before recombination, however the energy level of p-type silicon and n-type material is different, energy loss of carrier is inevitable due to the application of p-n junction to separates carriers.

Conduction loss is caused by the resistance existed in several parts of solar cell, such as bulk resistance, contact resistance, resistance of metal finger…etc.

Recombination loss is the reaction of electron-hole pair recombination by many different mechanisms, like radiative recombination, Auger recombination, surface recombination and trap recombination. Due to silicon is an indirect band gap material, we focus on Auger recombination, surface recombination and trap recombination.

Auger recombination is just like the back reaction of impact ionization, Auger recombination dominates minority carrier lifetime at high level injection or heavy doping region. For the reason of low cost, solar cell device becomes thinner than before, hence the importance of surface passivation grows stronger than ever, there are some methods to decline surface recombination which are reducing the amount of interface traps quantity, and keeping minority carrier away from the surface. All the loss mechanisms are shown in Fig. 2.7.

Due to all the loss mechanism that mentioned above, the ideal efficiency of single crystalline silicon solar cell is about 28.8%, and the record of the practical single crystalline silicon solar cell is 25±0.5%, which is Passivated emitter and rear locally diffused (PERL) structure made by UNSW, and measured by Sandia.

2.6 Lifetime measurement

Lifetime is also a key factor for solar cell device, minority lifetime determines recombination rate of solar cell. There are two major methods to measure minority carrier lifetime, first one is transient measurements, another one is Quasi-Steady-State Lifetime Measurements.

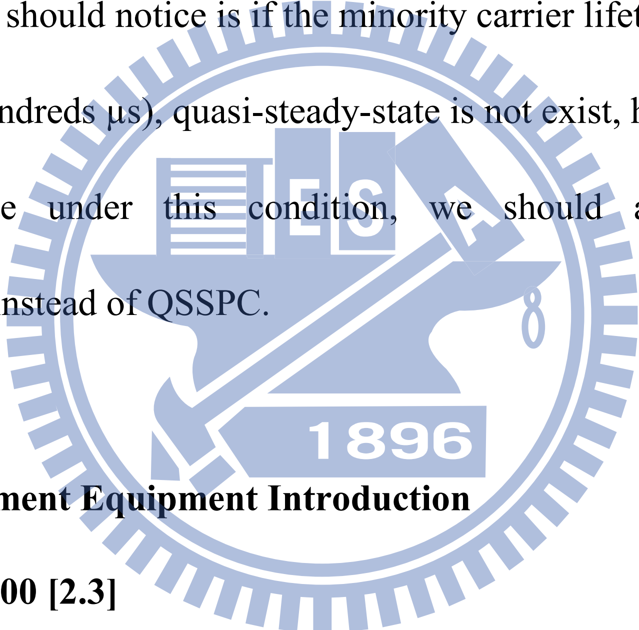
QSSPC (quasi-steady-state photoconductance) applies pulse light to sample, and electron-hole pairs would be generated, conductivity changes at the same time [2.3], the describing equation is

$$\Delta\sigma = q\Delta n(\mu_n + u_p)w \text{.........} \quad \text{(eq. 2-11)}$$

Where σ is conductivity, Δn is excess carrier concentration, w is wafer thickness, in steady state, carrier generation rate must be equal to recombination rate, photogenerated current could be expressed as

$$J_{ph} = \frac{\Delta nqw}{\tau_{eff}} \text{................} \quad \text{(eq. 2-12)}$$

by measuring and calculation, we could find out the value of τ_{eff}, but there is one thing we should notice is if the minority carrier lifetime is too large (higher than hundreds μs), quasi-steady-state is not exist, hence QSSPC is not appropriate under this condition, we should adopt transient measurements instead of QSSPC.



2.7 Measurement Equipment Introduction

2.7.1 QE-3000 [2.3]

Solar Cell Quantum Efficiency Measurement System (QE-3000) is the professional equipment for Quantum Efficiency test incident photo to electron conversion efficiency (IPCE) test, shown in Fig. 2.8. QE-3000 could measure photo-generation current under different wavelength of incident light, providing wavelength region is from 300nm to 2000nm, and QE-3000 is applied to detect internal quantum efficiency, external

quantum efficiency and reflectance in my experiment.

2.7.2 WCT-120 Offline Wafer Lifetime Measurement [2.4]

WCT-120 is an outstanding measurement which is designed to perform multiple measuring shown in Fig. 2.9, here we mention some of the principle functions such as quasi steady state photoconductance (QSSPC) lifetime measurement, transient lifetime measurement, generalized lifetime measurement, lifetime measurement range is from 10 ns to 10 ms, emitter saturation current density measurement. WCT-120 could help researchers to go deep into device operational mechanism.

2.8 Device Fabrication

The following description would show the fabrication process of our research. A 4-in (100) n-type silicon wafer which thickness is about 180 μm was used as bulk. First, native oxide is removed by DHF for 2 minutes, and then metal removal by HPM for 20 minutes at 80℃, after that native oxide is removed by DHF again, shown in Fig. 2.10 ,oxide was grown by HNO_3 for 5 minutes next, then wafer was dipped in KOH for 30minutes at 80℃ for texture, shown in Fig. 2.11, after ionic metal

removal by HPM for 20 minutes at 80℃, and native oxide removal by DHF, 36 nm Si_3N_4, was deposited at front side of wafer, shown in Fig. 2.12, then wafer was dipped in NaOH for 5 minutes for rear side polish, shown in Fig. 2.13, after all these treatment, Si_3N_4 was removed by BOE(buffer oxide etching) for 10 minutes, metal removal by HPM for 20 minutes at 80℃ and native oxide removal by DHF were performed, shown in Fig. 2.14. All process we have just mentioned was performed in ITRI, after that we adopted HDP-RIE and the first photolithography to etch silicon material at polish side to form align-key we needed for the following photolithography process. Next, blocking oxide 500 nm was deposited at polish side by PECVD, shown in Fig. 2.15, and then second photolithography was used to define p^+ emitter region, then the wafer was dipped in BOE solution to etch the oxide which covered the emitter region, then p^+ emitter was formed by ion implant(B^{11}, $5e^{15}$, 10 keV) , shown in Fig. 2.16, then wafer was dipped in BOE again to remove all oxide remained, shown in Fig. 2.17, after this blocking oxide 500 nm was deposited at polish side, shown in Fig. 2.18, n^+ BSF region was defined by third photolithography, after blocking oxide which covered n^+ region was removed by BOE and photoresist was removed, ion implant was

adopted to form n^+ BSF region(P^{31}, $5e^{15}$, 30 keV) , shown in Fig. 2.19, then the rest blocking oxide was removed by BOE, shown in Fig. 2.20, all photolithography process was performed in NFC. Then the dopant annealing was performed at 1000℃ for 1 minute in O_2, shown in Fig. 2.21. Then BOE was used again to remove oxide at both side, shown in Fig. 2.22, after that PECVD blocking oxide 500 nm was deposited at polish side, shown in Fig. 2.23, and we sent wafer for $POCl_3$ diffusion, we set 5 conditions for $POCl_3$ diffusion, 650℃ for 20 minutes, 675℃ for 20 minutes and 700℃ for 20 minutes, 850℃ for 20 minutes with drive in and wet oxide growing 10 minutes and 30 minutes, shown in Fig. 2.24, after this we did not remove PSG , instead, we directly deposited PECVD SiN_x 90 nm on PSG as anti-reflection layer, shown in Fig. 2.25, then removing blocking oxide at polish side by BOE, shown in Fig. 2.26. Next, 10 nm ALD Al_2O_3 deposition was adopted at polish side, then the device was dealt with annealing immediately, we still have 2 conditions for Al_2O_3 annealing(300℃, 400℃, 30 minutes in O_2 ambient) , shown in Fig. 2.27, then we deposited PECVD SiN_x 150 nm on Al_2O_3 layer, shown in Fig. 2.28. Fourth photolithography was used to define emitter passivation region, both SiN_x and Al_2O_3 at polish side was removed by

BOE except for the region protected by photoresist, shown in Fig. 2.29, then we used PECVD SiN_x deposition again to passivate undiffused region and n^+ region, thickness is 150 nm, shown in Fig. 2.30. Fifth photolithography was used after PECVD SiN_x deposition to define contact region, BOE was applied for contact etching, shown in Fig. 2.31, then the following process was metal deposition, we use Titanium and Aluminum stack for metal finger, deposited by E-gun, Ti thickness is 10 nm and Al thickness is 1000nm, shown in Fig. 2.32, Al deposition was applied at once after Ti deposition, there was no chamber vent between two process to avoid Ti oxidation. Sixth photolithography was applied for metal finger formation, shown in Fig. 2.33, then Al etching solution and BOE were used to remove Al an Ti that we did not wanted, sintering at 380℃, 20 minutes in N_2 ambient was assumed to improve contact of metal and silicon and fabrication process is completed. The SEM micrograph of random pyramids texture surface are shown in Fig. 2.34, Fig. 2.35 and the picture of device is shown in Fig. 2.36.

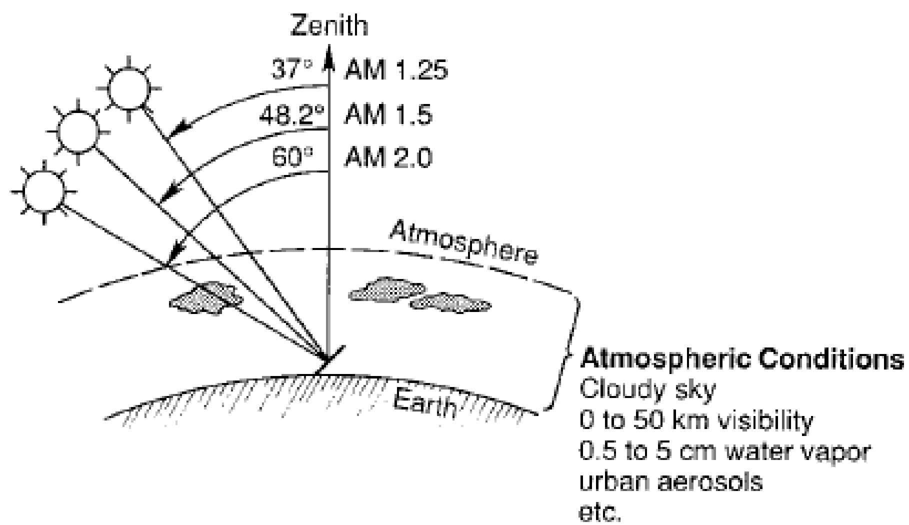


Fig. 2.1 Definition of Air Mass [2.1]

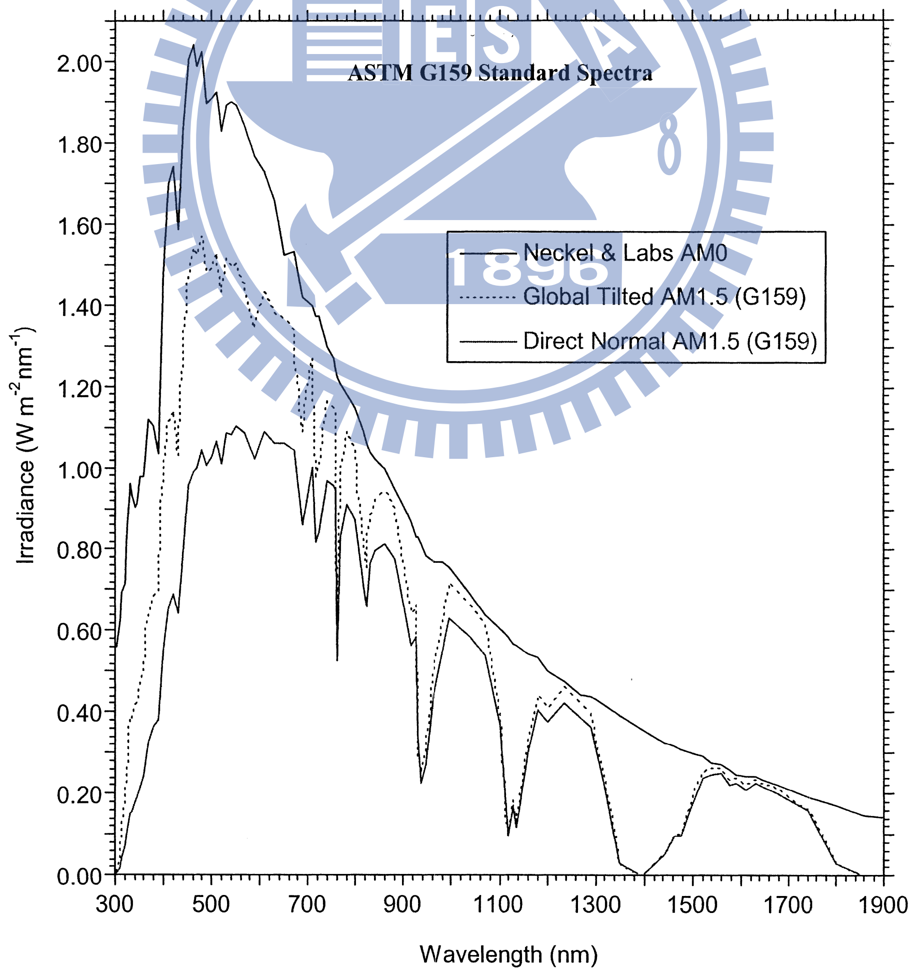


Fig. 2.2 AM1.5G solar spectrum [2.2]

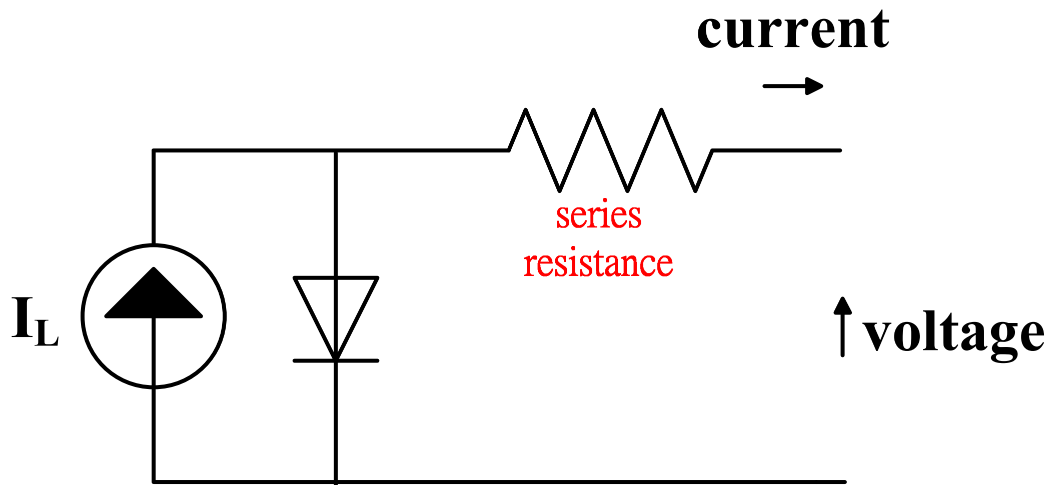


Fig. 2.3 Circuit model of series resistance

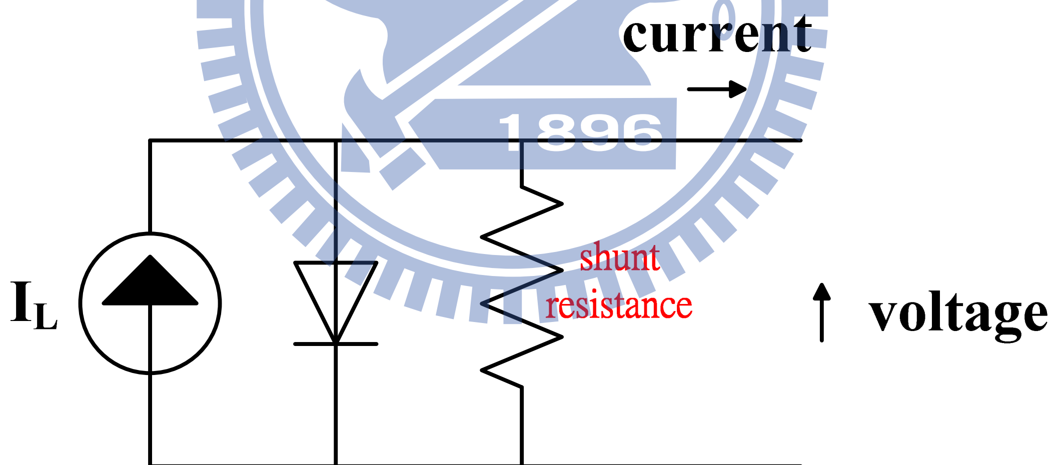


Fig.2.4. Circuit model of shunt resistance

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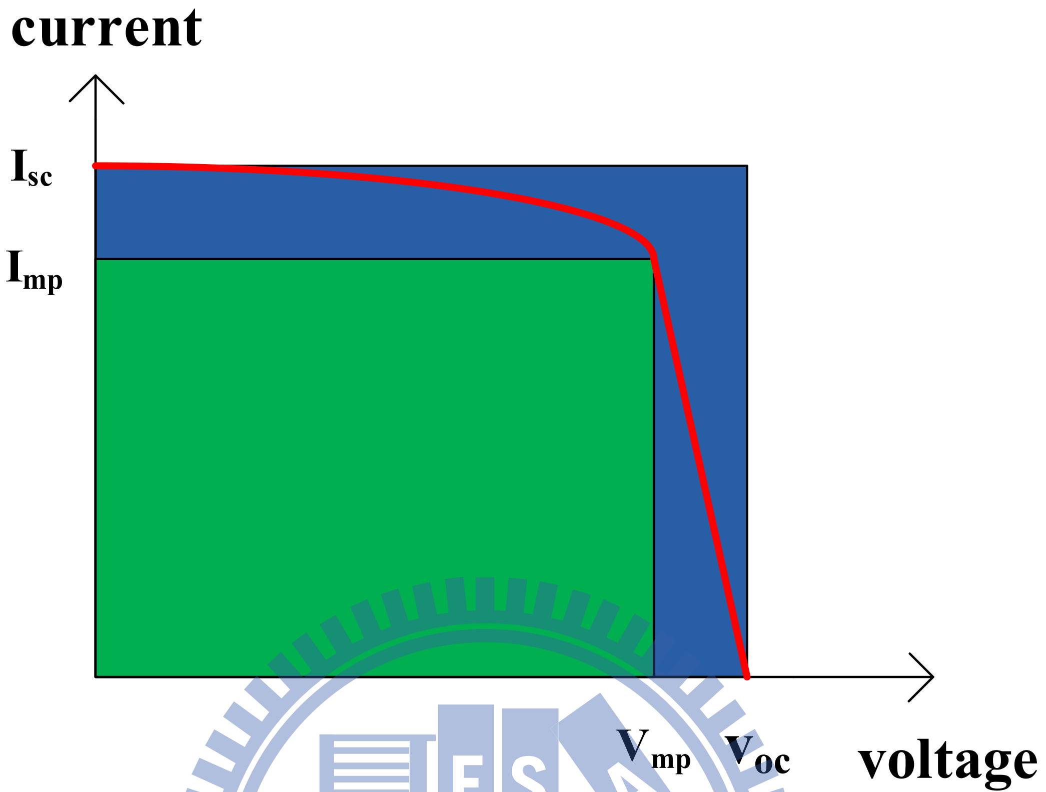

Fig. 2.5 explanation of Fill Factor

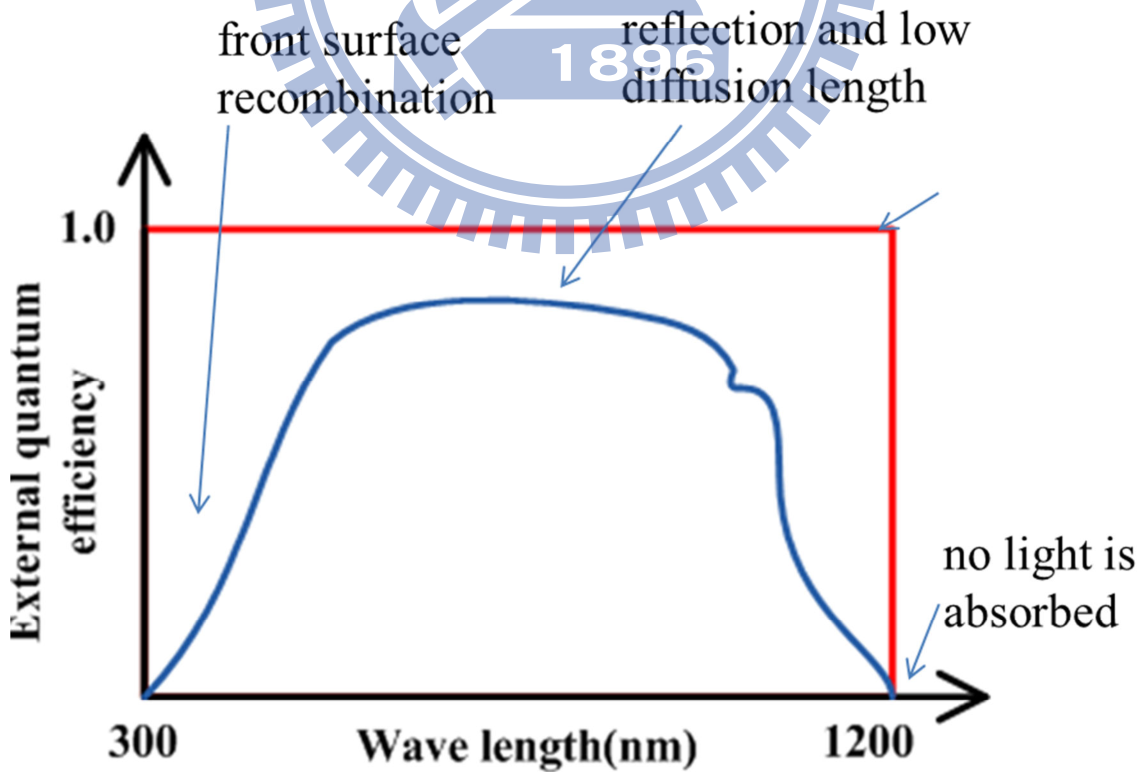

Fig. 2.6 explanation of External Quantum Efficiency

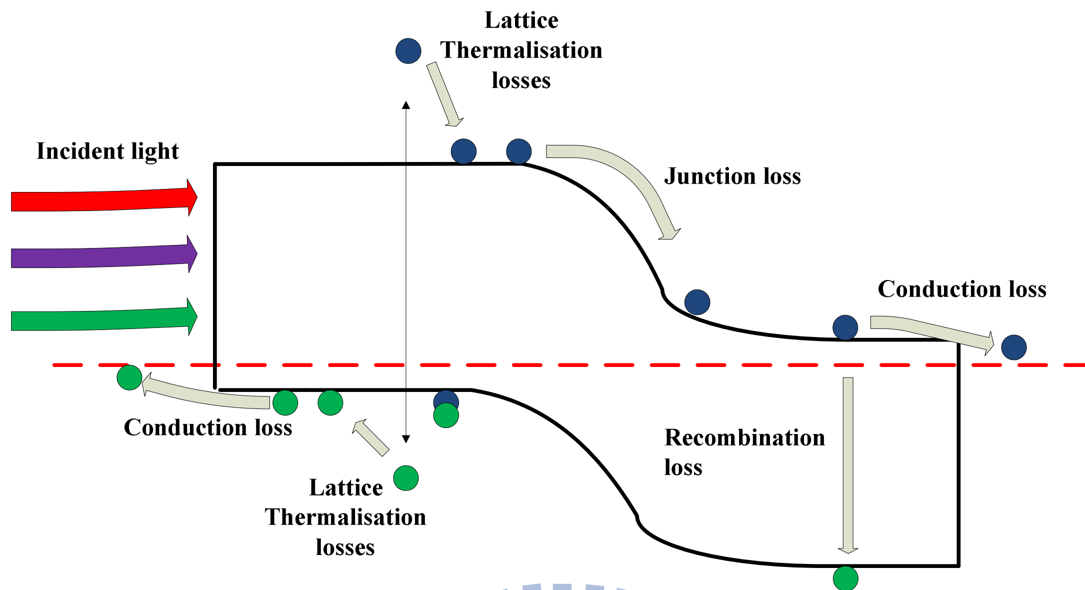

Fig. 2.7 Loss Mechanism

Fig. 2.8 QE3000 [2.3]

Fig. 2.9 WCT-120 [2.4]

n-type

Fig. 2.10 silicon bulk after clean treatment

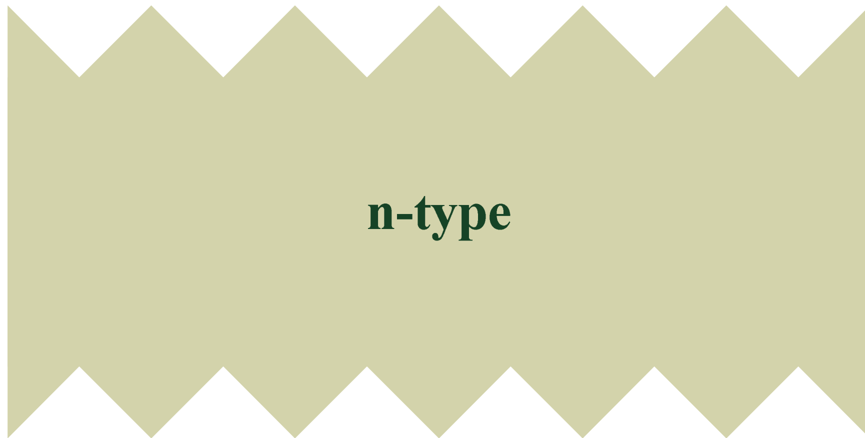

Fig. 2.11 KOH etching for texture formation

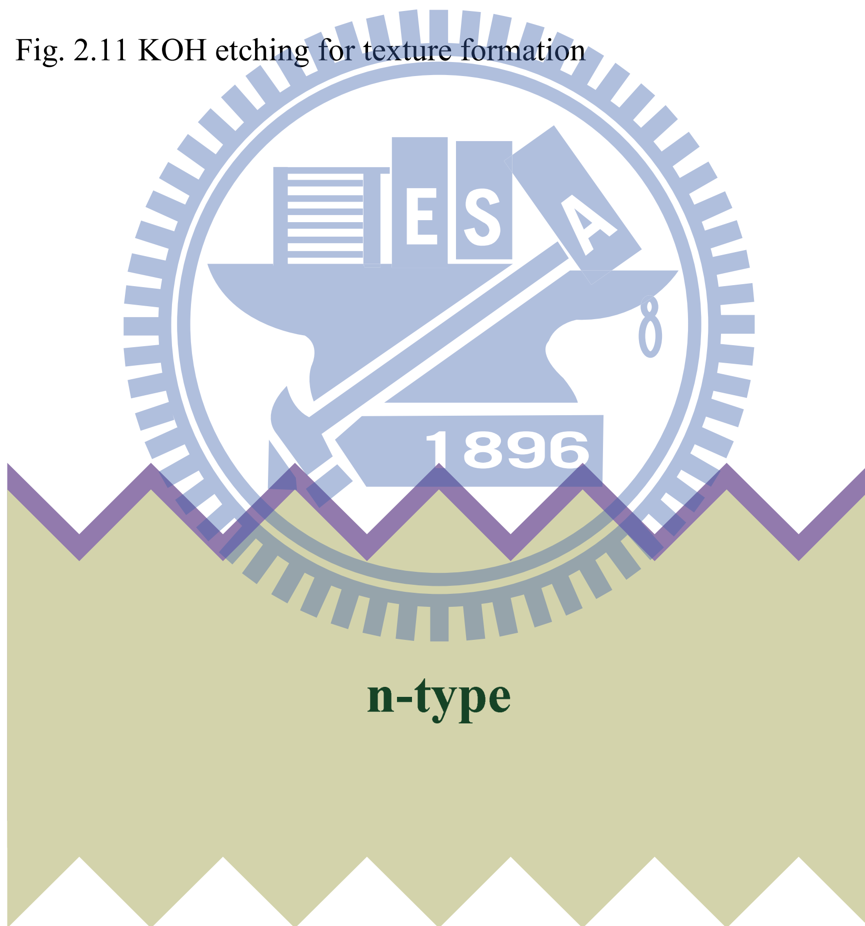

Fig. 2.12 SiNx deposition as protection layer

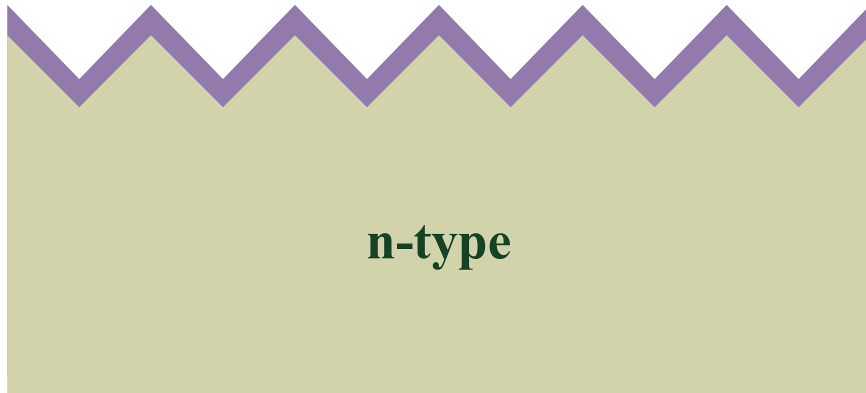

Fig. 2.13 rear side polished by NaOH etching

Fig. 2.14 SiNx removed by BOE etching and clean

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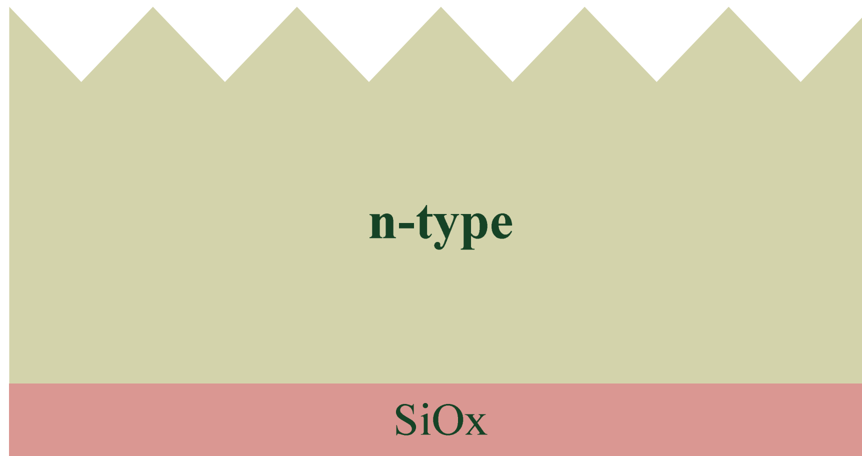

Fig. 2.15 blocking oxide deposition at rear side

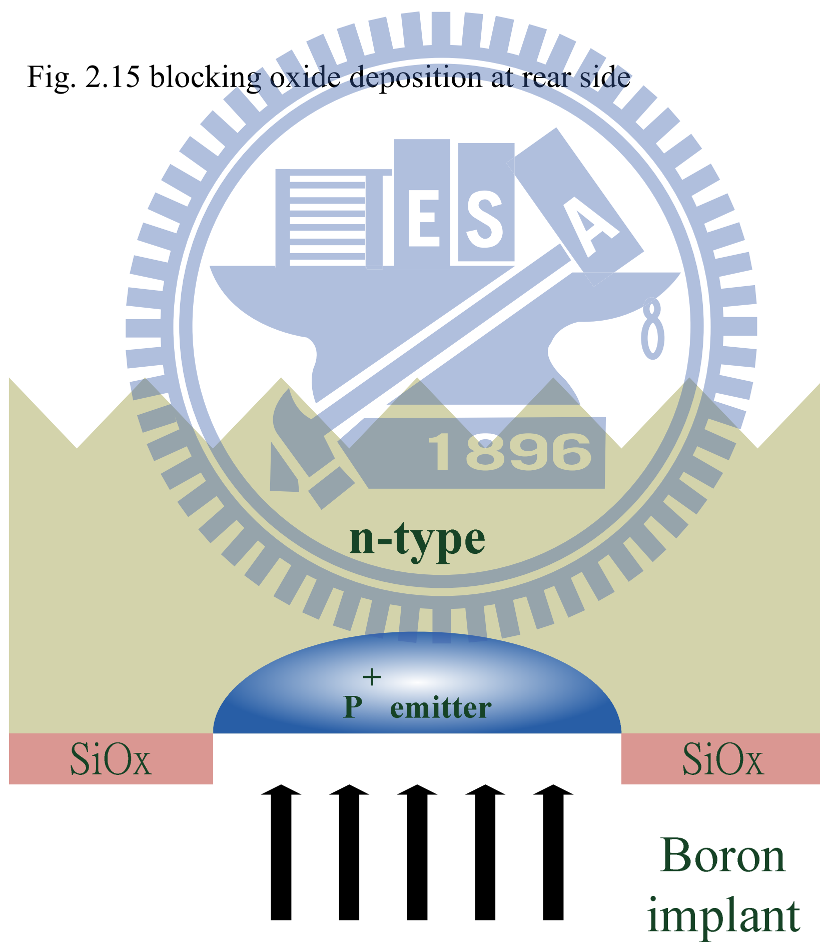

Fig. 2.16 emitter definition and Boron implantation

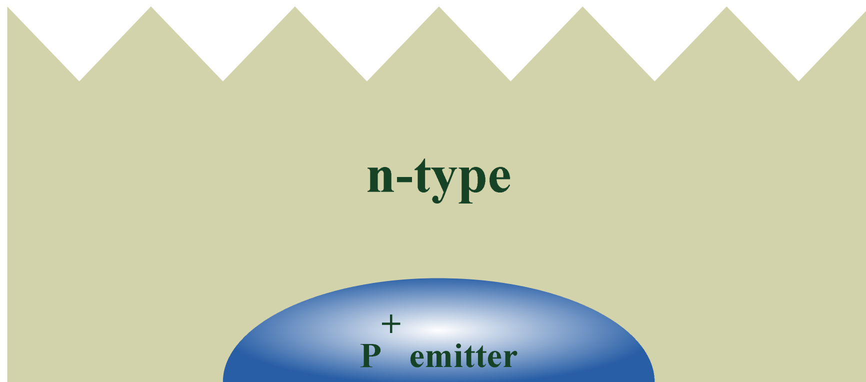

Fig. 2.17 blocking oxide removed by BOE etching

Fig. 2.18 blocking oxide deposition

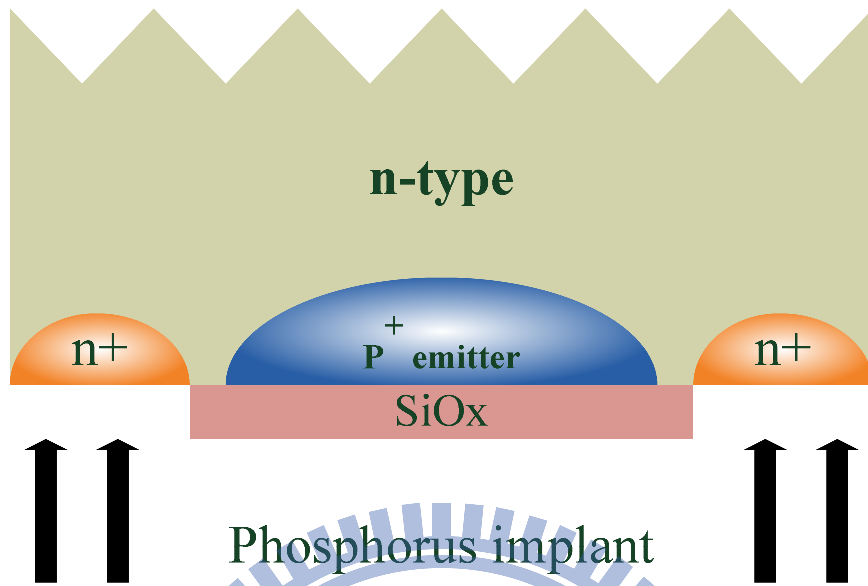

Fig. 2.19 back surface field definition and Phosphorus implantation

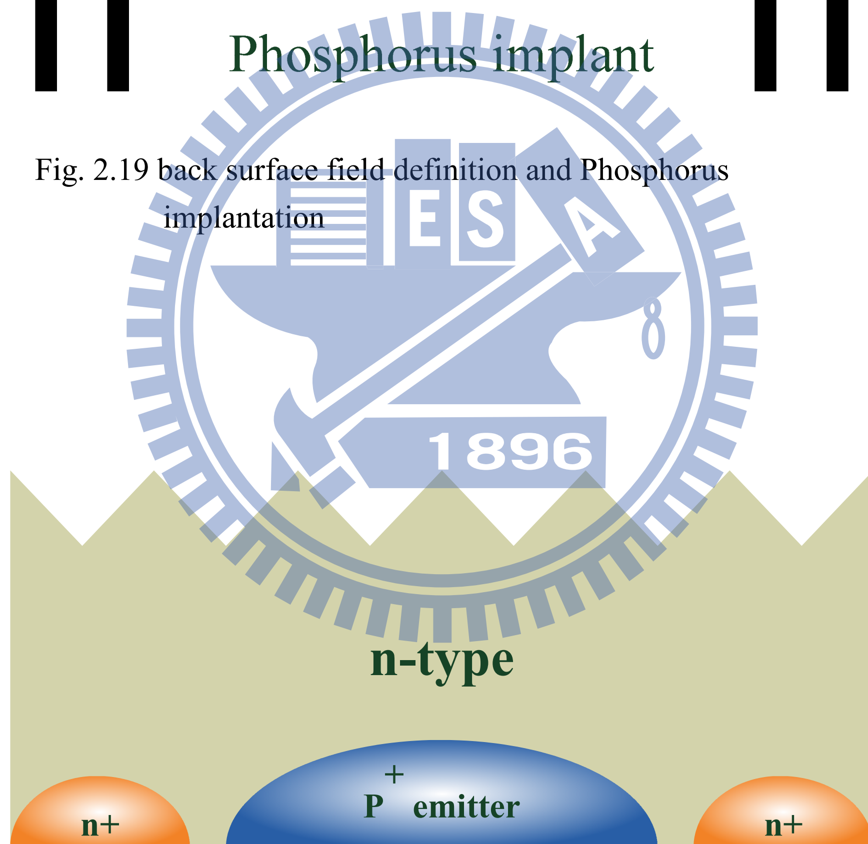

Fig. 2.20 blocking oxide removed by BOE etching

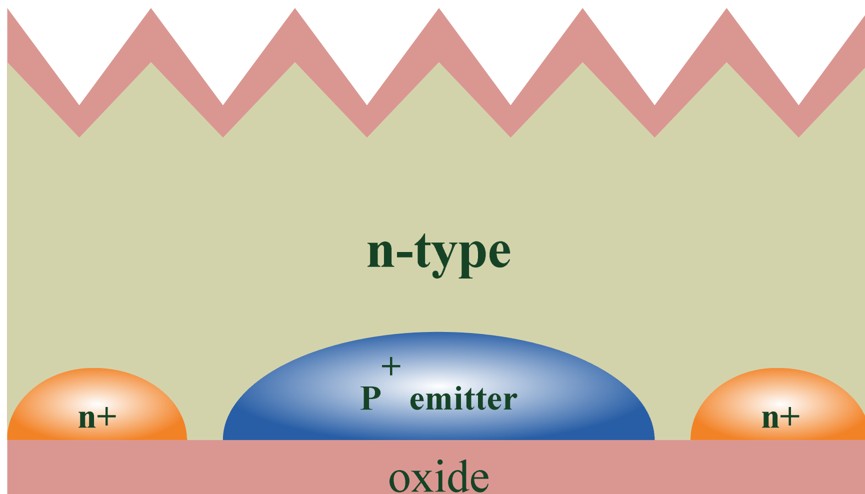

Fig. 2.21 annealing at 1000℃ for 1 minute in O_2 ambient

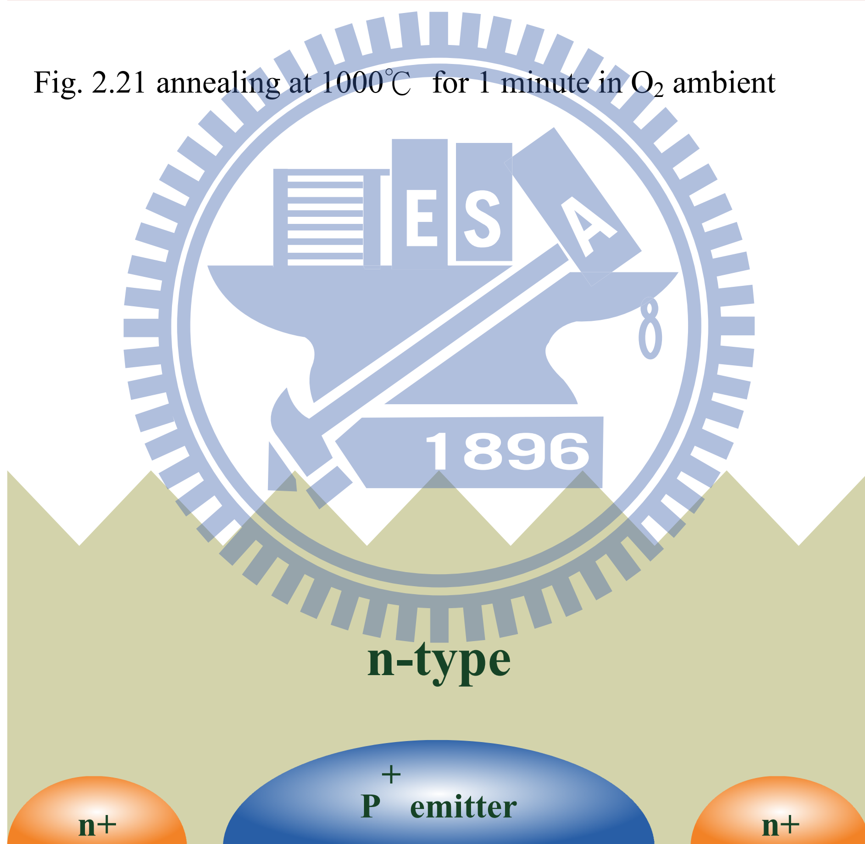

Fig. 2.22 oxide removed by BOE etching

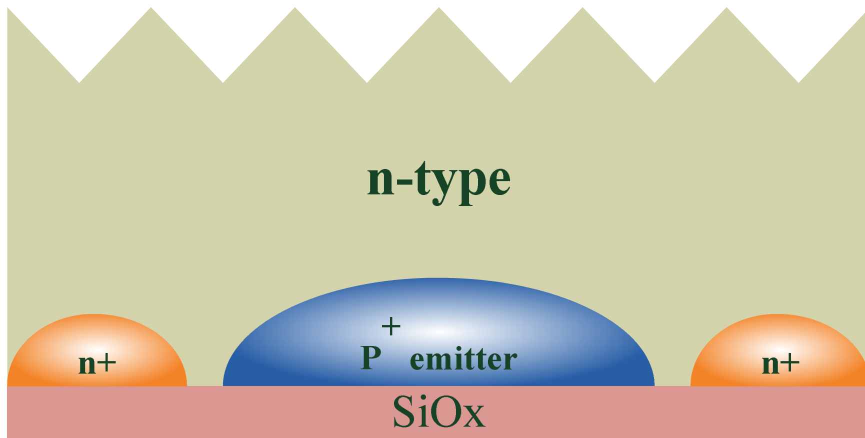

Fig. 2.23 blocking oxide deposition at rear side

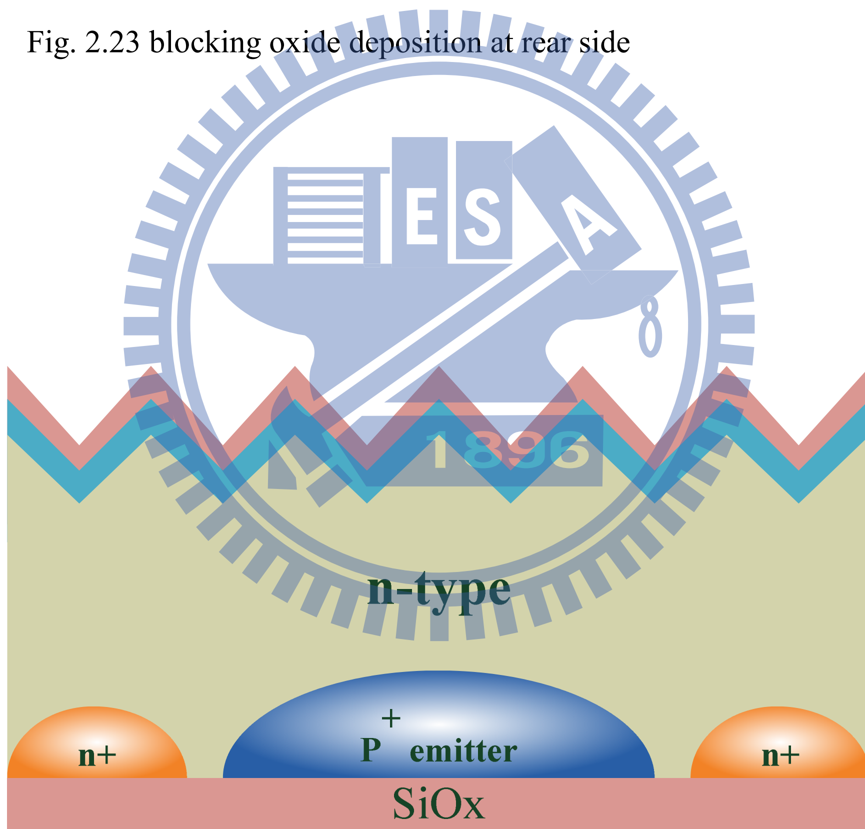

Fig. 2.24 $POCl_3$ diffusion at different temperature

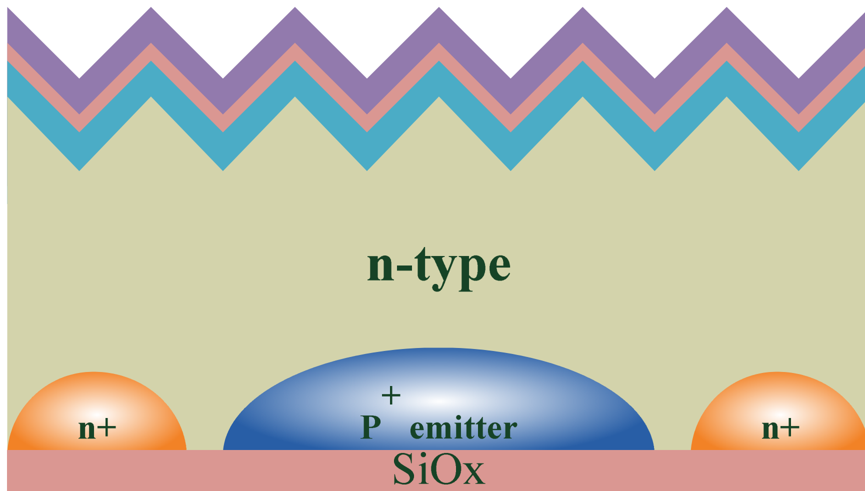

Fig. 2.25 SiNx deposition at front side as ARC

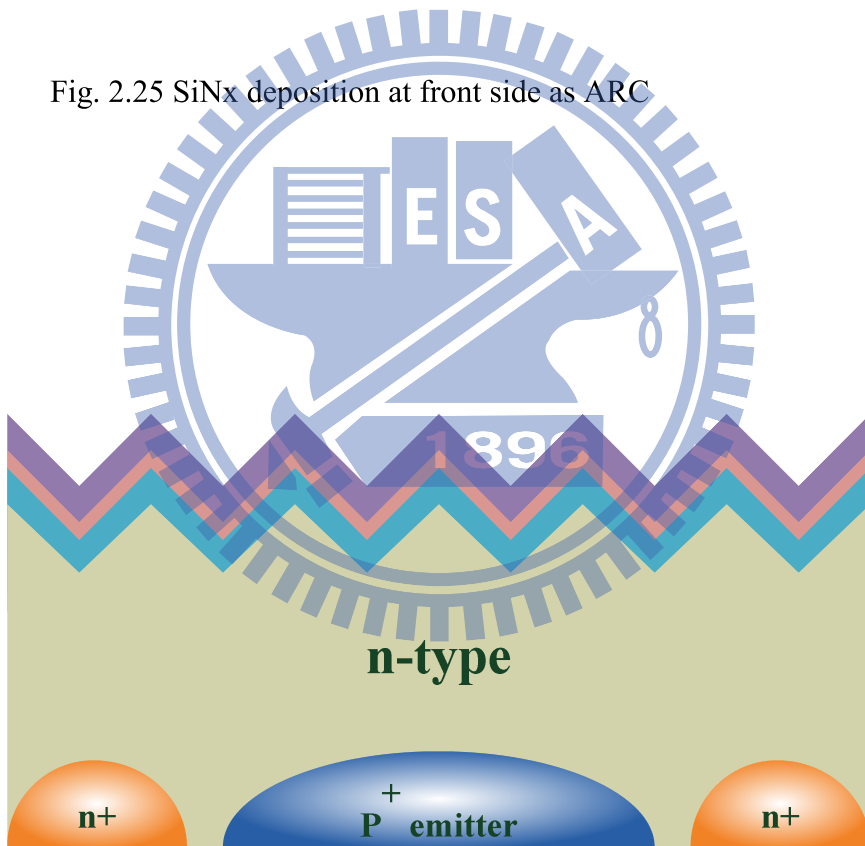

Fig. 2.26 blocking oxide removed by BOE etching

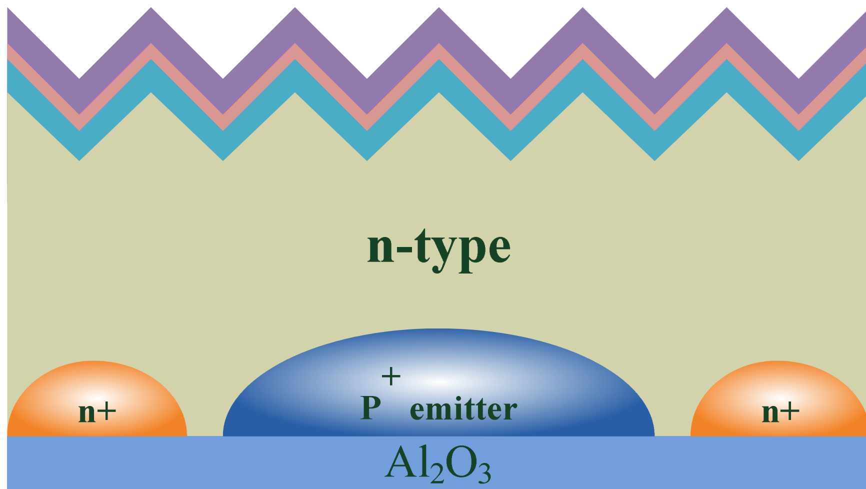

Fig. 2.27 ALD Al_2O_3 deposition at rear side

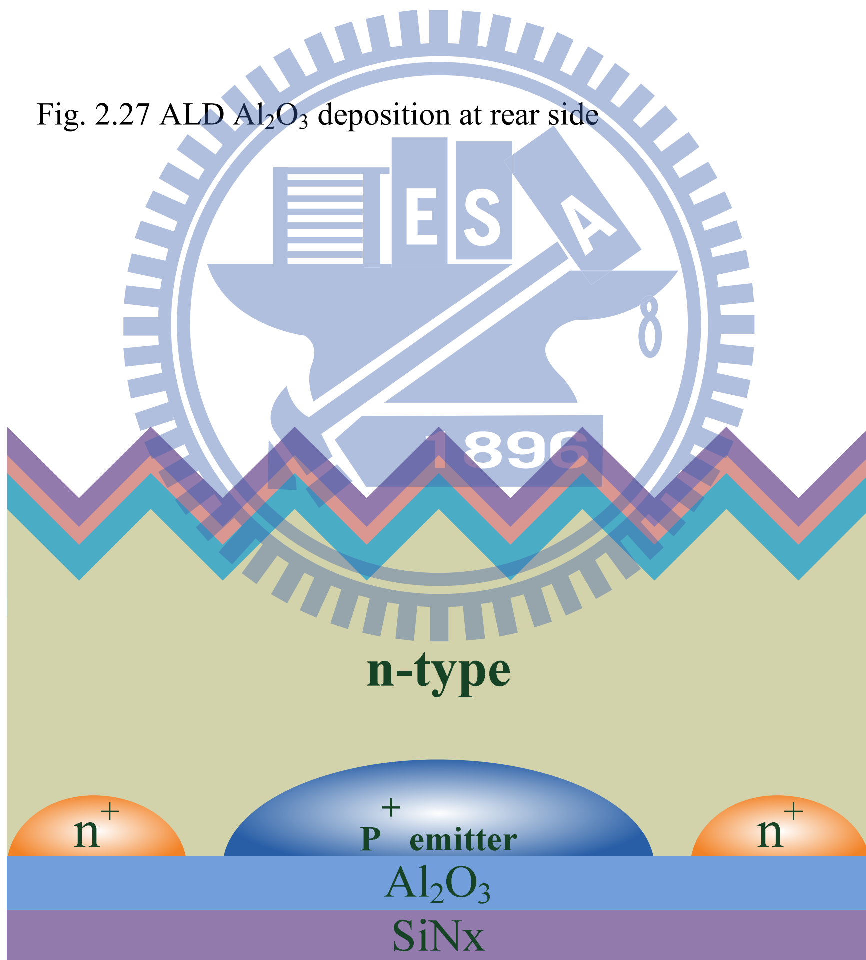

Fig. 2.28 SiNx capping layer deposition at rear side

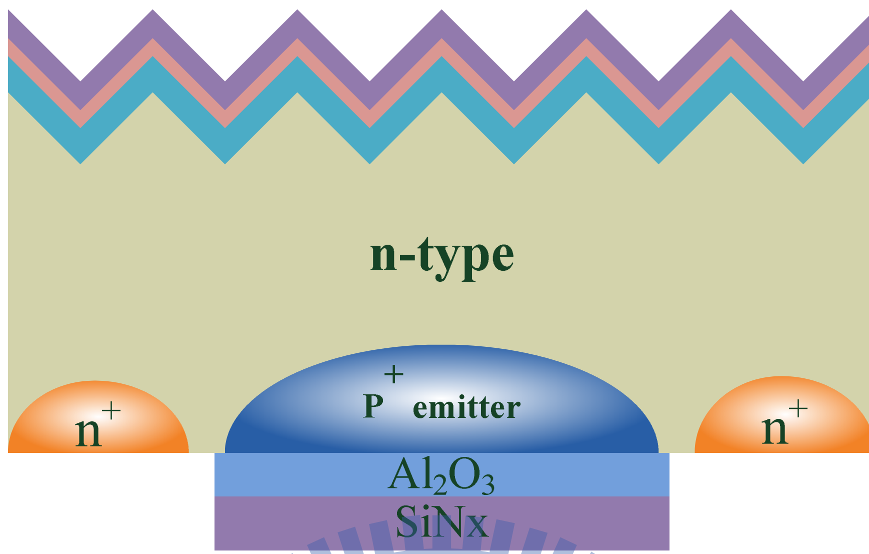

Fig. 2.29 emitter passivation definition with BOE etching

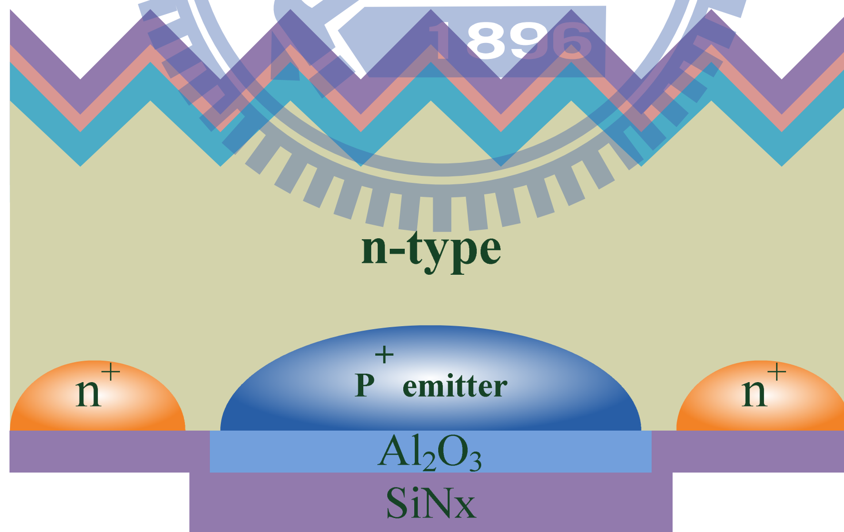

Fig. 2.30 SiNx passivation deposition

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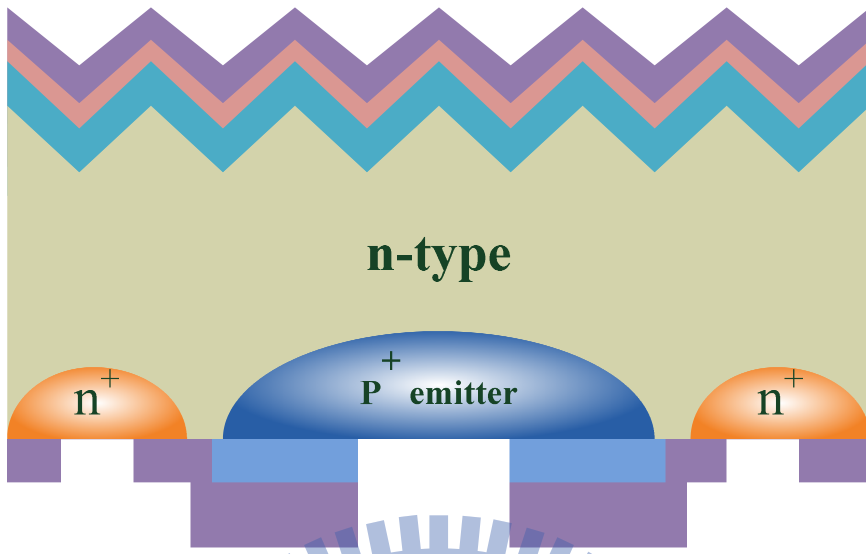

Fig. 2.31 contact definition

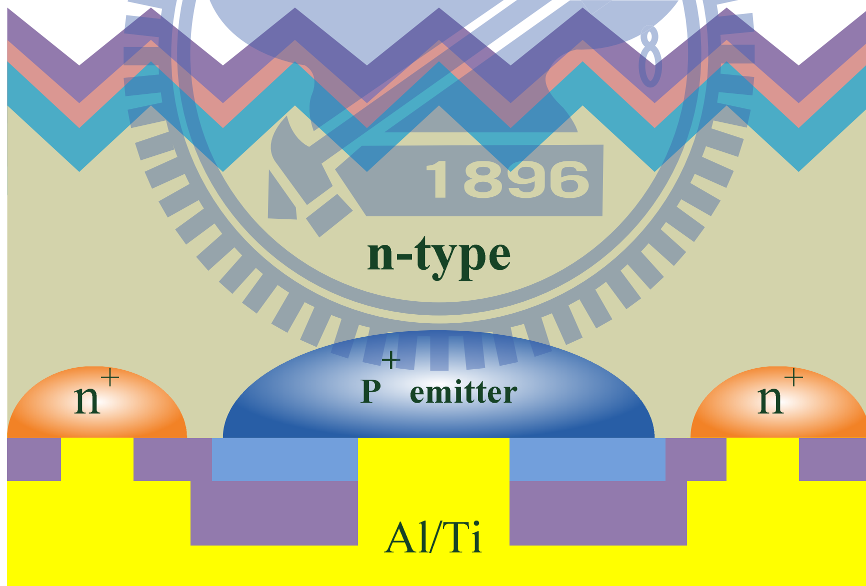

Fig. 2.32 metal deposition

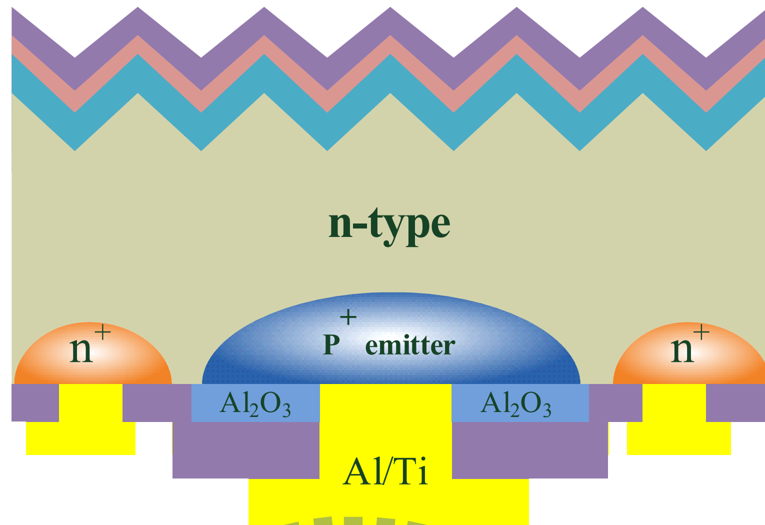

Fig. 2.33 metal finger definition

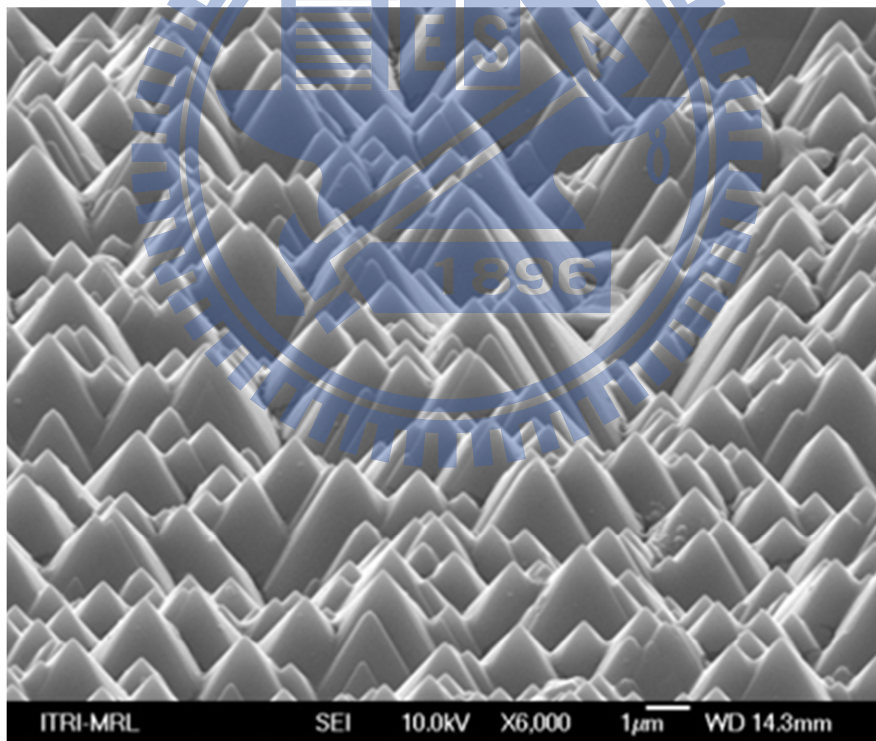

Fig. 2.34 scanning electron microscope (SEM) micrograph of random texture surface

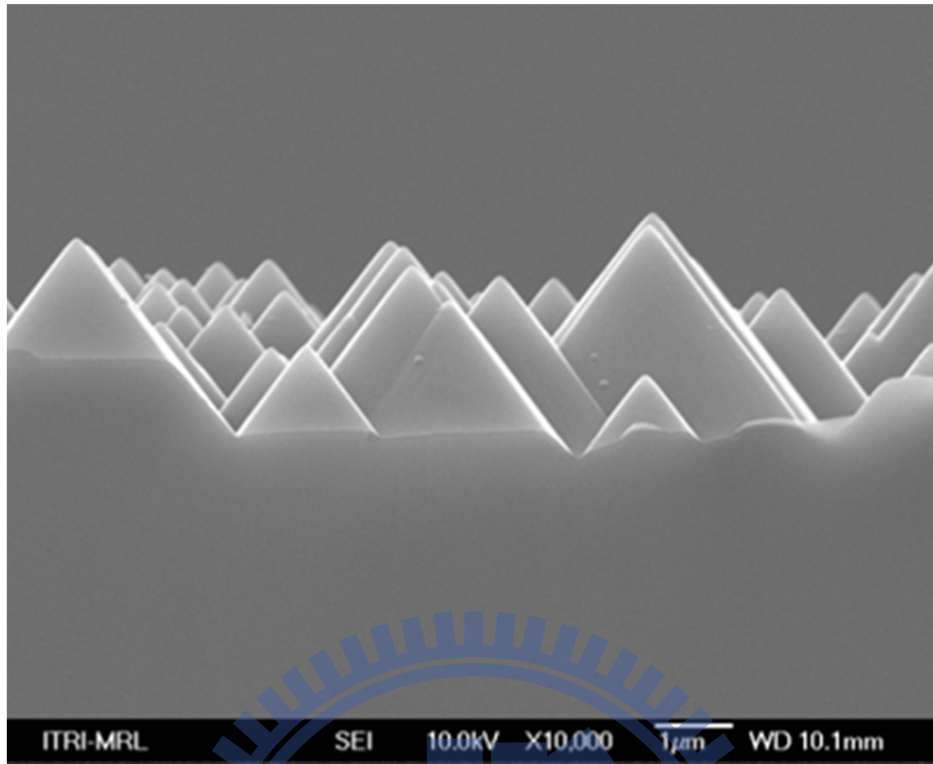

Fig. 2.35 scanning electron microscope (SEM) of texture surface cross section

Fig. 2.36 image of front side and back side of device

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Chapter 3

Result and Discussion

3.1 Introduction

For n-type IBC silicon solar cell, front surface field passivation is a key point for achieving higher efficiency, an appropriate front surface field with great passivation layer could provide some extra benefit, such as increasing the stability under UV light exposure [3.1], providing a low lateral series resistance way for majority carriers [3.2], keeping minority carriers away from front surface to decrease the opportunity of recombination, however the heavy doping profile for front surface field might cause serious recombination at the front interface. For the reason that is just mentioned above, front surface passivation is one of the issues we want to discuss in this chapter.

P-type emitter is also a crucial issue for n-type IBC silicon solar cell, emitter region is larger than spacer and back surface field region as design rule to increase the collection possibility of minority carriers, therefore the passivation of p^+ emitter region is worth researching to improve the efficiency of IBC silicon solar cell.

Undiffused gap, or we call it spacer is worth discussing for IBC solar cell, different spacer determines the lateral transport distance for minority carriers which are generated at the region far from emitter in 1-dimension [3.2], such as back surface field and undiffused gap, in this research, we design different spacer for IBC n-type silicon solar cell to make the relationship of carrier transport and undiffused gap clear.

3.2 Lifetime measurement

3.2.1. $POCl_3$ Diffusion Front Surface Field

First we adopt heavy doping $POCl_3$ diffusion and heavy doping $POCl_3$ diffusion with wet oxide growing and HF treatment to remove dead layer at the front surface for test structure, after samples covered by PECVD SiNx, we compare two processes by minority carrier lifetime measurement, implied open circuit voltage and saturation current density, as shown in Fig.3.1 to Fig. 3.4, we could realize that for minority carrier lifetime, and implied open circuit voltage at 1 sun, heavy doping with wet oxide growing and HF treatment are overwhelmingly higher than normal heavy doping process, and saturation current for heavy doping is extremely higher than heavy doping with wet oxide growing and HF

treatment, we attribute this result to doping concentration is reduced at the front side due to heavy doped silicon bulk is oxidized and then removed by HF treatment, therefore the diffusion length of minority carriers is enhanced significantly because of the lower defect density created by overdosing impurities which exceeds solid solubility. $POCl_3$ 850℃ with drive in 15min was adopted for heavy doping diffusion, and wet oxide was growing under the condition of 800℃ for 10 minutes.

Due to heavy doping $POCl_3$ diffusion leads to lifetime degradation and wet oxide growing with HF treatment need more time and thermal process, light doping $POCl_3$ diffusion profile is another way to achieve excellent front surface passivation. Next we comparing light doping diffusion profile with PSG remained or removed by HF treatment, the result of lifetime measurement, surface recombination velocity and implied open circuit voltage were tested after deposition of SiNx capping layer as anti-reflection layer, the results are shown in Fig.3.5 to Fig.3.7, the sample with light doping $POCl_3$ diffusion and PSG passivation shows higher minority carrier lifetime, implied open circuit voltage at one sun and lower surface recombination velocity due to the passivation provided by PSG, light doping $POCl_3$ diffusion profile is performed under the

condition of 20 minutes $POCl_3$ diffusion without drive in whether temperature does not exceed 700℃. We should notice that $POCl_3$ diffusion is adopted for front surface field and front surface passivation which is texture structure to reduce the reflection of incident light. The difference between $POCl_3$ diffusion applied for texture surface and polish surface is worth researching. For this purpose, $POCl_3$ diffusion 20 minutes without drive in at 650℃, 675℃ was applied for test structure for lifetime measurement , the result are shown in Fig.3.8, Fig.3.9, the minority carrier lifetime of polish sample is higher than texture sample, this phenomenon could be explained that the surface area of texture surface is about two-times larger than polish side, hence the heavy doping region is double, so is the quantity of defect [3.3]. For the purpose of finding out the optimism of light doping $POCl_3$ diffusion with PSG and PECVD SiNx as front surface passivation at relatively low process temperature (650℃ to 700℃), we set light doping $POCl_3$ diffusion at 650℃, 675℃, 700℃ for 20minutes as our experiment, the result of minority carrier lifetime measurement are shown in Fig.3.10, although the values are closed, but we could still identify light doping $POCl_3$ diffusion at 675℃ for 20 minutes is the optimism. Finally the comparison of

saturation current density of heavy doping with wet oxide growing 10 minutes at 700℃ with HF treatment and light doping $POCl_3$ diffusion with PSG at 650℃, 675℃, 700℃ is shown in Fig.3.11, we could realize light doping profile is superior for front surface field and front surface passivation.

3.2.2. Emitter Passivation By Atomic Layer Deposition (ALD) Al_2O_3

For n-type IBC silicon solar cell, we normally deposit SiO2 to cover p-type emitter region as passivation layer, however, the existence of positive fix charge at the interface of Si and SiO2 might cause negative effect for hole collection, recently Al_2O_3 has been researched as the substitution to be passivation layer of p-type emitter region. At the beginning, the development of Al_2O_3 deposition technique is for high k dielectric research due to the demand of MOSFET scaling down. The deposition methods often applied are PECVD, ALD and sputter, Al_2O_3 which is deposited by ALD has state-of-the-art quality, furthermore after annealing, high density negative fix charge would appear at the interface of Si substrate and Al_2O_3 layer with ultrathin SiOx which could enhance

field effect passivation at p-type emitter region Fig.3.12 [3.4], according to the research, the fixed charge density is up to 10^{12} ~10^{13} cm^{-2}, which is able to be achieved that many researchers have also reported [3.4] [3.5]. However, the optimism of passivation is existed for different annealing temperature due to two kinds of passivation mechanism which are chemical passivation and field effect passivation. The dangling bond at the interface is the origin of defect which would trap minority carriers then creating recombination, however dangling bond can be passivated by hydrogen [3.4].

There are other benefits for Al_2O_3 passivation. SiNx and SiO_2 show the degradation of effective lifetime after UV irradiation which means surface passivation goes worse than before, however Al_2O_3 appears improved effective lifetime after long term light illumination [3.6] [3.7], this is a significant phenomenon for solar cell. Moreover, Al_2O_3 grown by thermal ALD with PECVD SiNx capping layer is proved to own higher thermal stability and longer effective lifetime than single Al_2O_3 layer even for sample with capping layer without anneal for Al_2O_3 [3.8].

In our experiment, we test two kind of annealing temperature in O_2 for 30 minutes which are 300℃ and 400℃ to the same ALD Al_2O_3

thickness which is 10nm.

First, the result of minority carrier lifetime measurement, surface recombination velocity and implied open circuit voltage of single Al_2O_3 layer are shown in Fig.3.13 to Fig.3.15, sample with 400℃ annealing treatment presents better quality than sample with 300℃ annealing treatment, this result can be explained by the top view of the test sample from microscope as shown in Fig.3.16, Fig.3.17, the sample with 300℃ annealing treatment shows more blistering part of surface than sample with 400℃ annealing treatment, however, in our fabrication process, ultrathin Al2O3 layer is protected by SiNx capping layer which is deposited by PECVD, for this reason, the passivation of Al_2O_3/SiNx stacking layer is investigated, the sample with SiNx capping layer after Al_2O_3 annealing at different temperature have been tested, the result of minority carrier lifetime measurement, surface recombination velocity and implied open circuit voltage are shown in Fig.3.18 to Fig.3.20, we could clear understand the passivation of Al_2O_3 annealing at 300℃ with SiNx capping layer is better than sample at 400℃ annealing with SiNx capping layer, the comparison of surface recombination velocity of single Al_2O_3 layer and Al_2O_3 with SiNx capping layer at the same annealing

temperature is shown in Fig.3.21, Fig.3.22, the surface recombination velocity is improved for both of sample, this is due to the hydrogen from NH_3 passivates the interface and blistering area of sample, and Al_2O_3 layer with 300℃ annealing shows higher blistering area density, hence hydrogen passivation is more effectively for Al_2O_3 layer with 300℃ annealing.

3.3 Open Circuit Voltage Comparison

The conditions we mentioned above are all applied for IBC solar cell device, the device condition is shown in Table 3.1 All the discussion in section 3.2.1 and 3.2.2 is about minority carrier lifetime which would influence open circuit voltage seriously, so we start from open circuit voltage analysis.

Fist, the comparison of open circuit voltage and shunt resistance for the solar cell device which spacer is 50 um with the same heavy doping $POCl_3$ diffusion treatment (850℃,drive in 15 minutes), but different wet oxide growing time (10 minutes, 30 minutes) is shown in Fig.3.23, with longer wet oxide growing time, the device shows higher open circuit voltage and larger shunt resistance, the result can be speculated from

lifetime measurement we had already tested. Next, we compare the open circuit voltage and shunt resistance of device with different light doping $POCl_3$ diffusion, as shown in Fig.3.24 to Fig.3.29, we have already known light doping $POCl_3$ diffusion with 675℃ is the optimism on lifetime measurement, for solar cells with Al_2O_3 annealing at 400℃, devices with 675℃ light doping $POCl_3$ diffusion demonstrate higher open circuit voltage as we expected. However, for the device at 300℃ annealing condition, device with light doping $POCl_3$ diffusion shows poor open circuit voltage and low shunt resistance, this might be caused by the mistake in fabrication process, in fact, all devices with Al_2O_3 annealing at 300℃ and light doping $POCl_3$ at 675℃ demonstrate low open circuit voltage and low shunt resistance which means serious leakage mechanism is existed in our device.

The results of the open circuit voltage with different Al_2O_3 annealing temperature for light doping $POCl_3$ diffusion at 650℃, 675℃, 700℃ are shown in Fig.3.30 to Fig.3.38 for all the spacer conditions, the devices with Al_2O_3 annealing at 300℃ generally demonstrate higher open circuit voltage and larger shunt resistance, except for device with light doping $POCl_3$ at 675℃

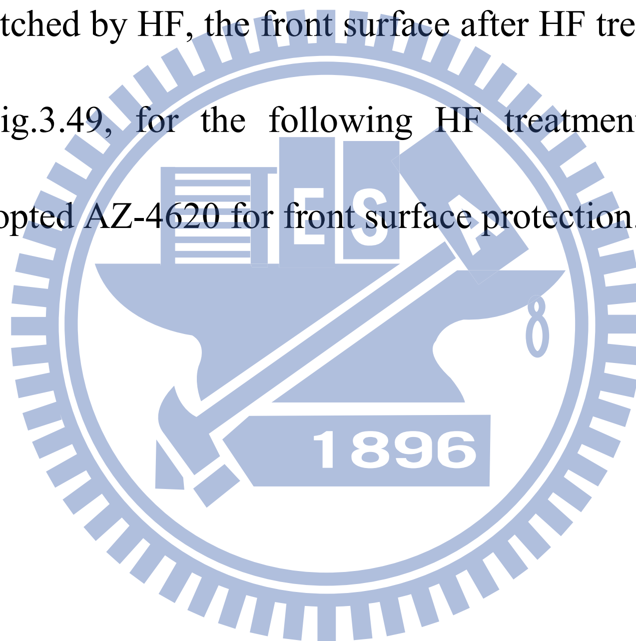
3.4 Short Circuit Current Density Comparison

The short circuit current has relation to the emitter fraction in solar cell [3.2], we design three kinds of spacer for solar cell device, which are 50um, 100um, 150um, the emitter fraction is increasing with smaller spacer, accompanying with lower series resistance, the relationship of spacer, short circuit current and series resistance is shown in Fig.3.39 to Fig.3.44.

3.5 I-V curve and efficiency

After the comparison of open circuit voltage and short circuit current, I-V curve and efficiency for the solar cell with heavy doping $POCl_3$ diffusion and the best result of light doping $POCl_3$ with Al_2O_3 passivation are shown in Fig.3.45 to Fig.3.47, Table.3.2, Table.3.3, we could clearly discover that for light doping $POCl_3$ diffusion with Al_2O_3 passivation condition, the best solar cell is for 675℃ $POCl_3$ diffusion with Al_2O_3 emitter passivation layer at 400℃ annealing 30 minutes in O_2 ambient, which efficiency could achieve 7.37%. However, the efficiency of the solar cell with heavy doping $POCl_3$ diffusion and Al_2O_3 passivation at

annealing temperature 400 ℃ could achieve 7.59%. This can be attributed to the accident during device fabrication, during the process the HF treatment before ALD Al_2O_3 deposition, photoresist is applied for texture surface to protect SiNx anti reflection layer and PSG passivation, the photoresist we adopted is FH-6400, the photoresist could not cover the texture surface completely during spin coating process, hence SiNx and PSG was etched by HF, the front surface after HF treatment is shown in Fig.3.48, Fig.3.49, for the following HF treatment in fabrication process, we adopted AZ-4620 for front surface protection.



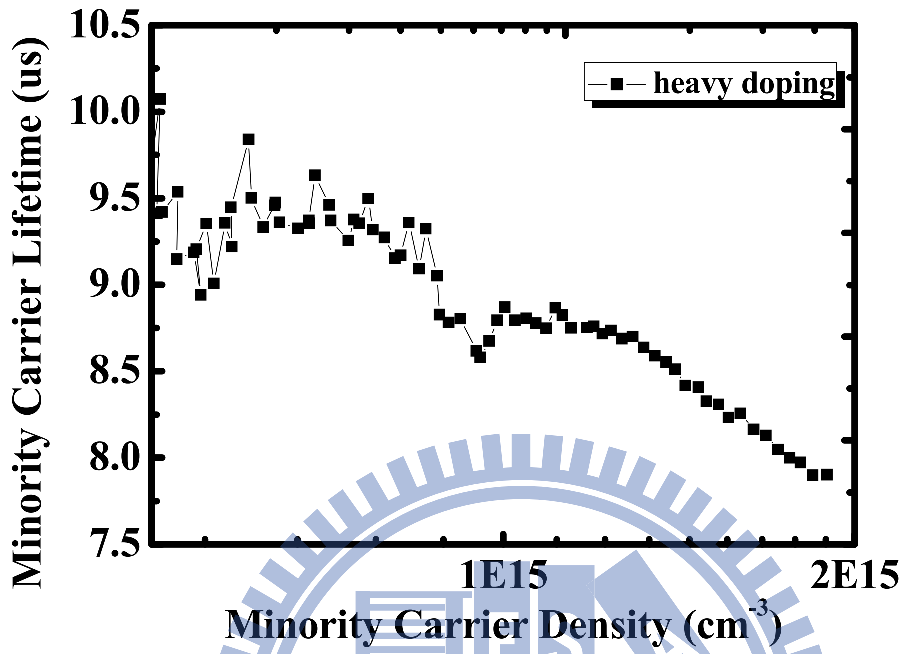


Fig. 3.1 lifetime of heavy doping $POCl_3$ diffusion

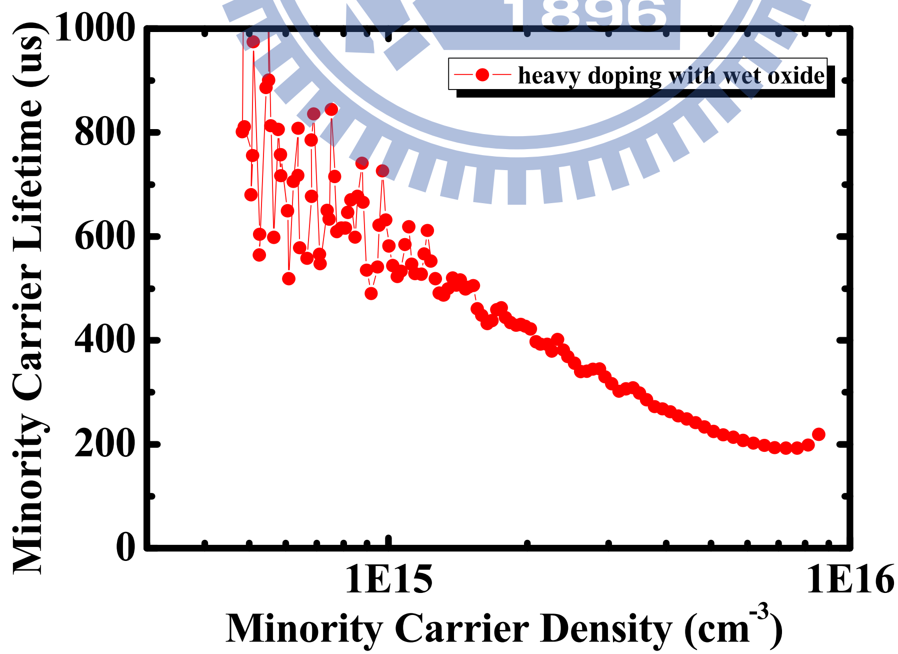


Fig. 3.2 lifetime of heavy doping $POCl_3$ diffusion with wet oxide growing

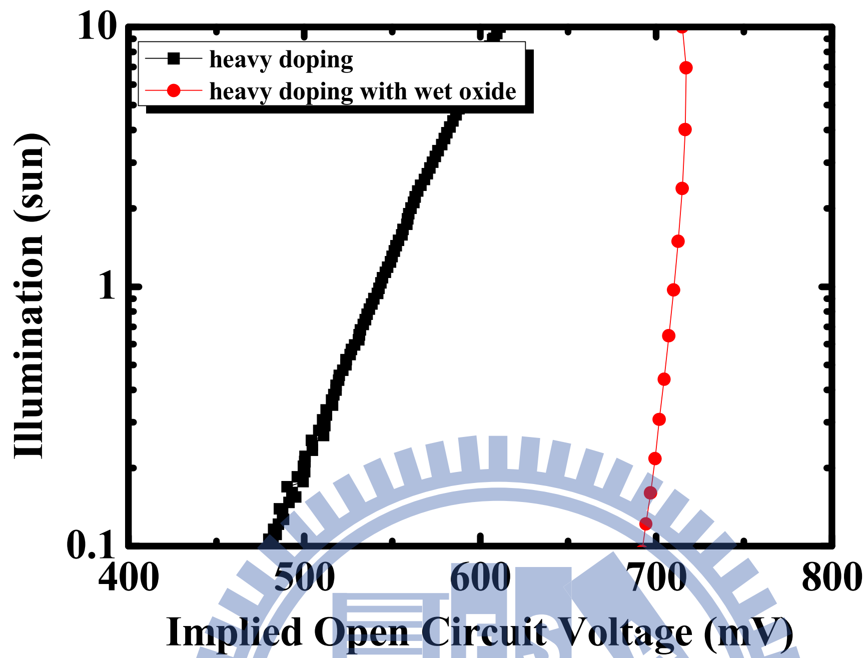


Fig. 3.3 implied open circuit voltage for heavy doping $POCl_3$ diffusion w/wo wet oxide growing

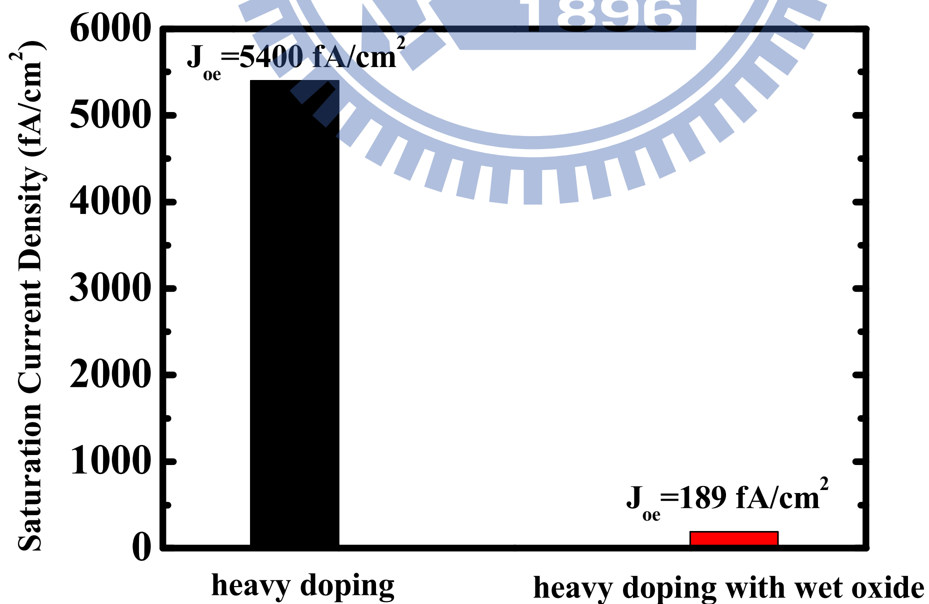


Fig. 3.4 saturation current density for heavy doping $POCl_3$ diffusion w/wo wet oxide growing

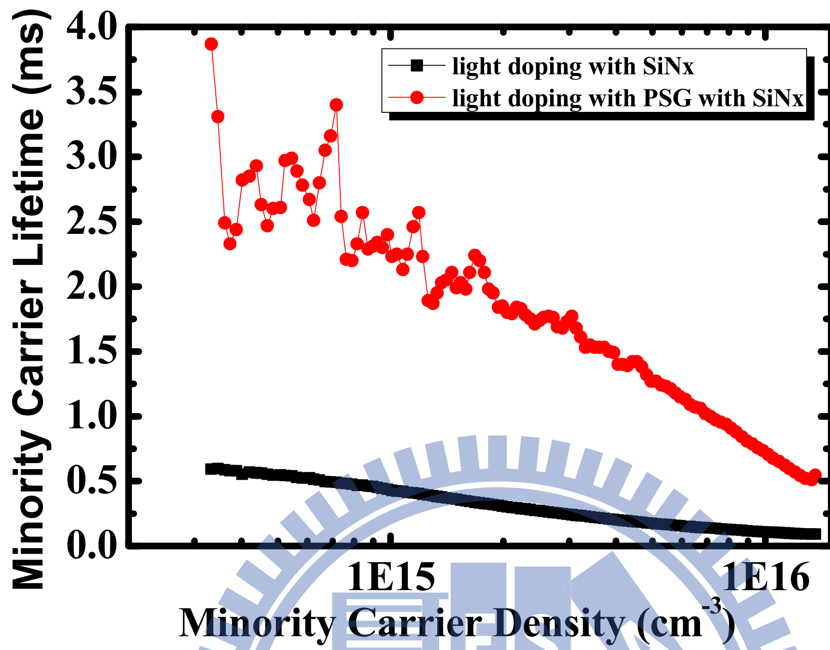


Fig. 3.5 lifetime of light doping w/wo PSG

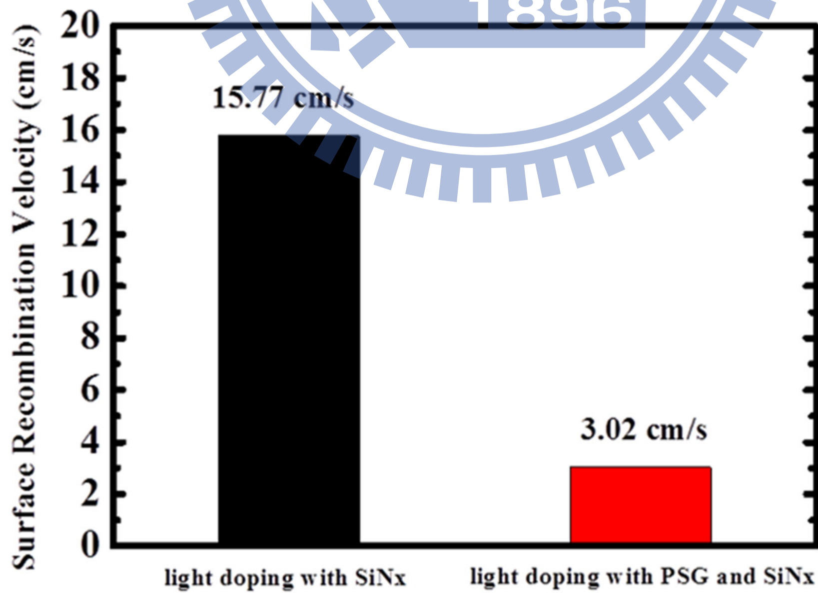


Fig. 3.6 SRV of light doping w/wo PSG

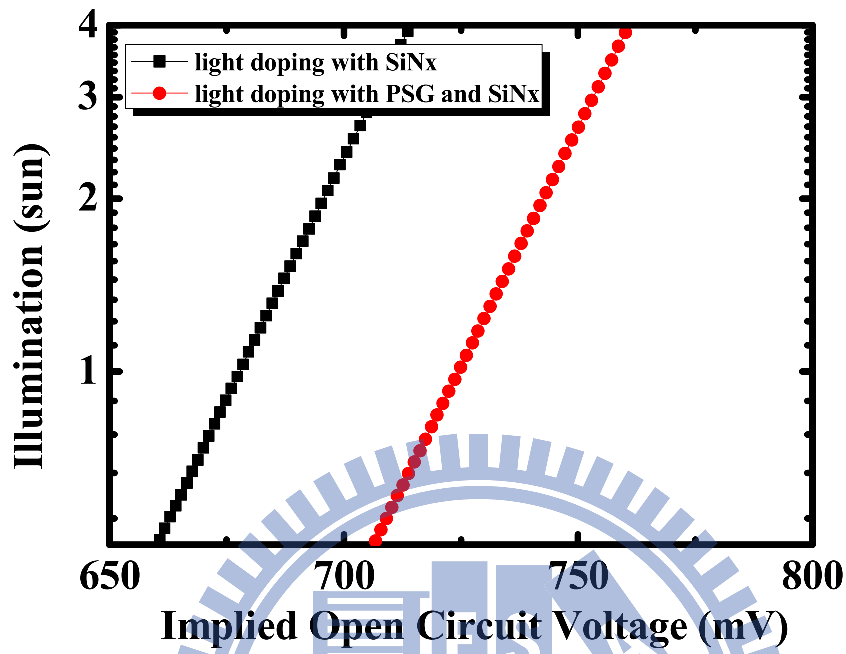


Fig. 3.7 implied open circuit voltage of light doping w/wo PSG

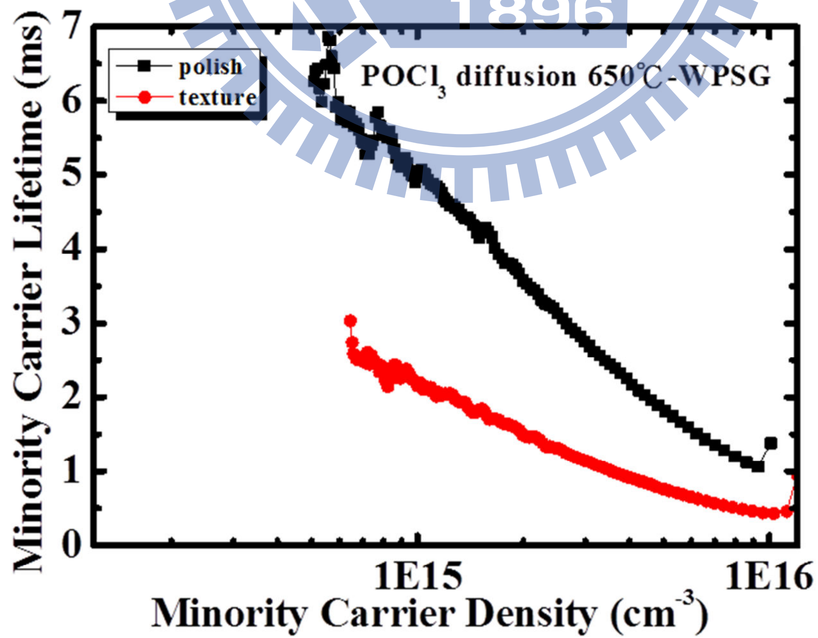


Fig. 3.8 lifetime of light doping at 650℃ on texture/polish surface

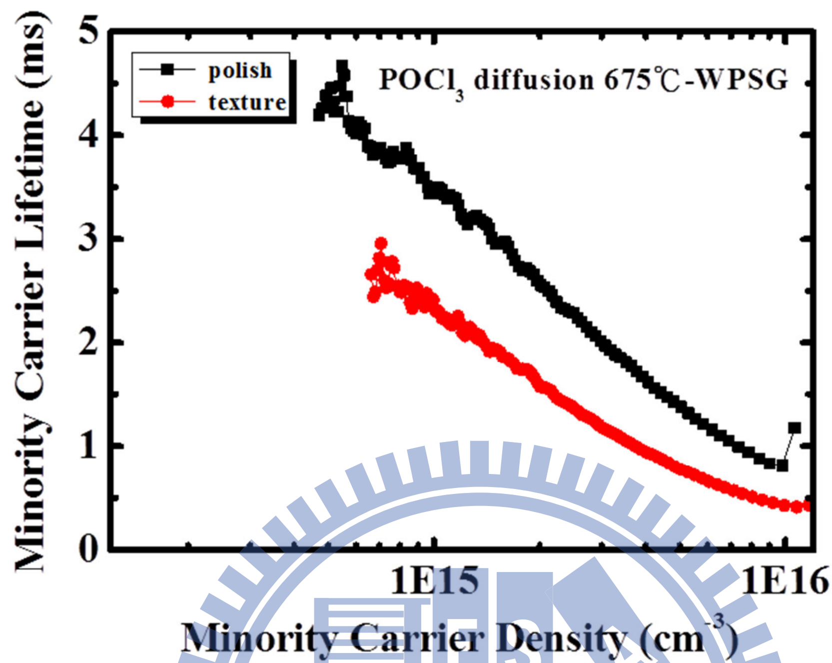


Fig. 3.9 lifetime of light doping at 675℃ on texture/polish surface

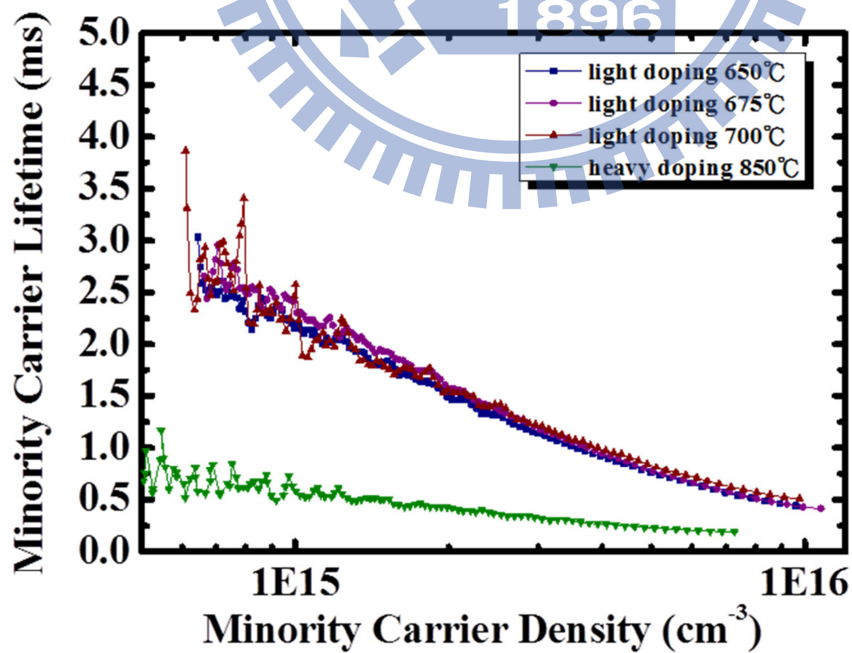


Fig. 3.10 lifetime of light doping at 650℃, 675℃, 700℃ and heavy doping 850℃

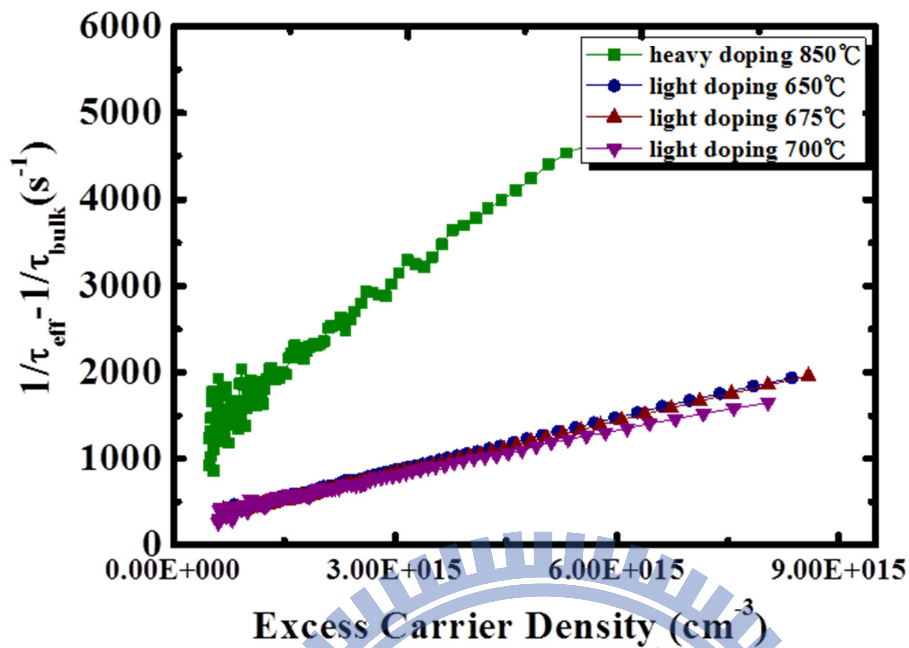


Fig. 3.11(a) saturation current for light doping with different temperature and heavy doping with wet oxide growing

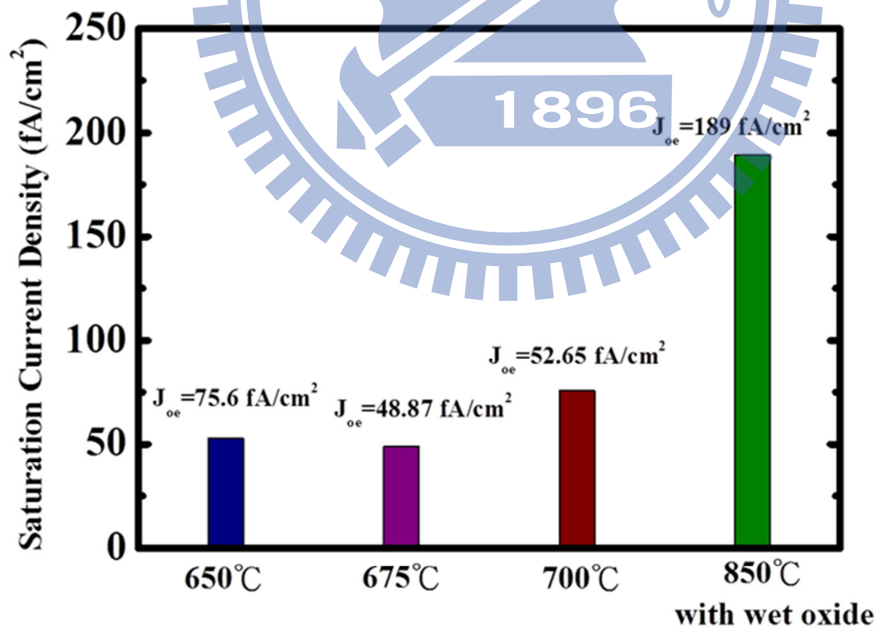


Fig. 3.11(b) saturation current for light doping with different temperature and heavy doping with wet oxide growing

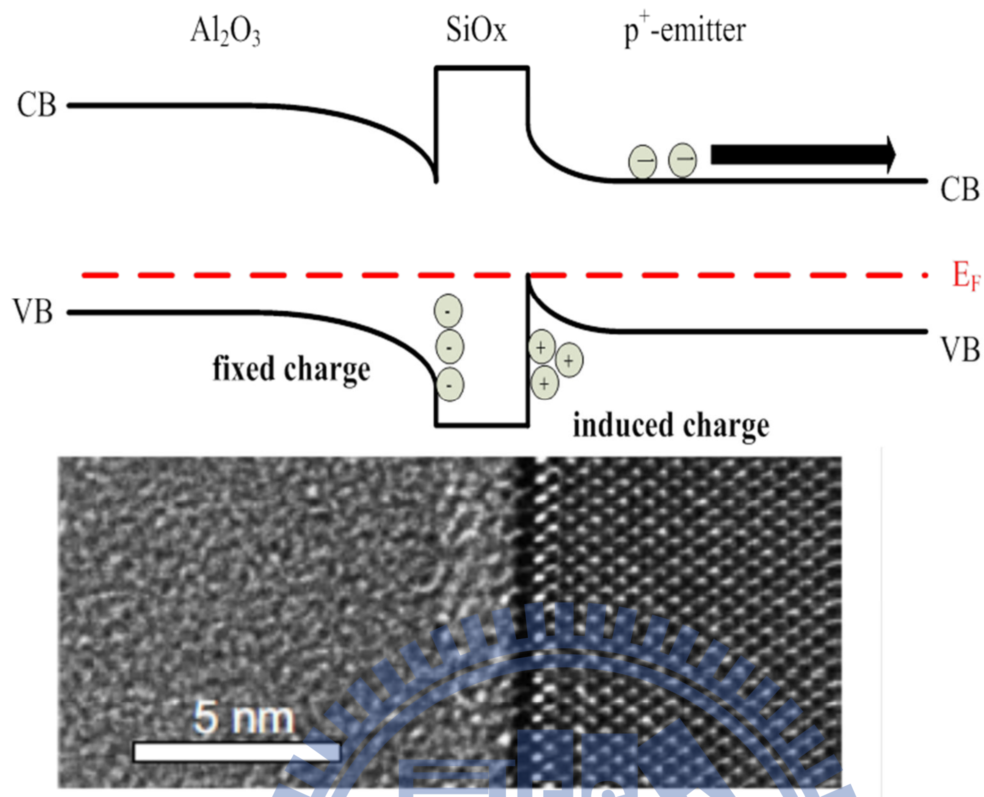


Fig. 3.12 interface band diagram and TEM image [3.4]

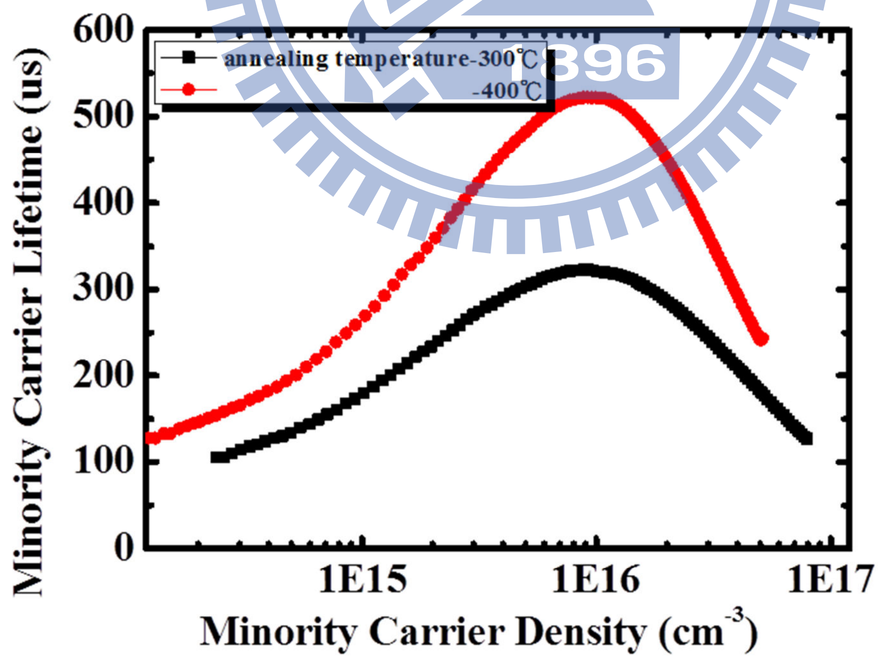


Fig. 3.13 lifetime of Al_2O_3 layer at different annealing temperature

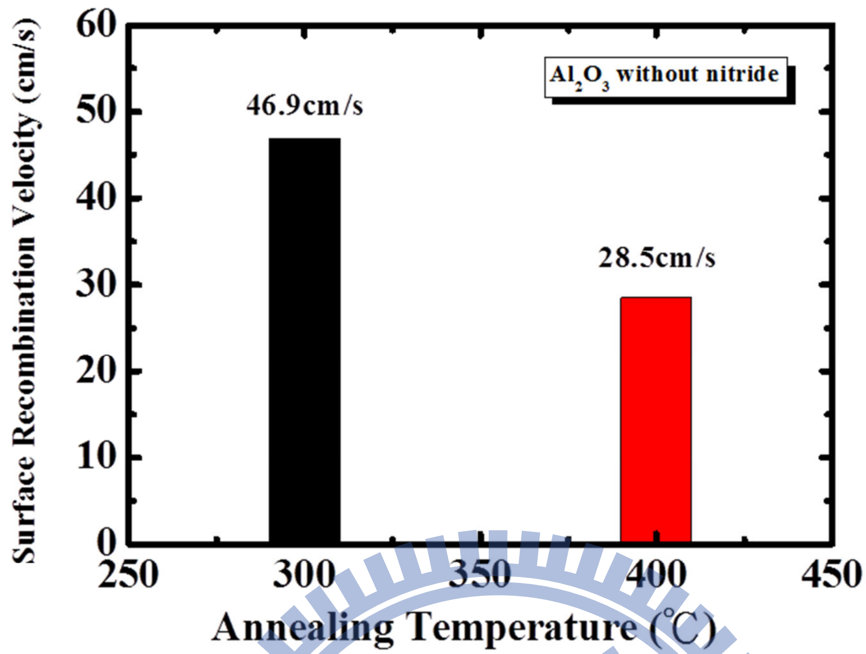


Fig. 3.14 SRV of Al_2O_3 layer at different annealing temperature

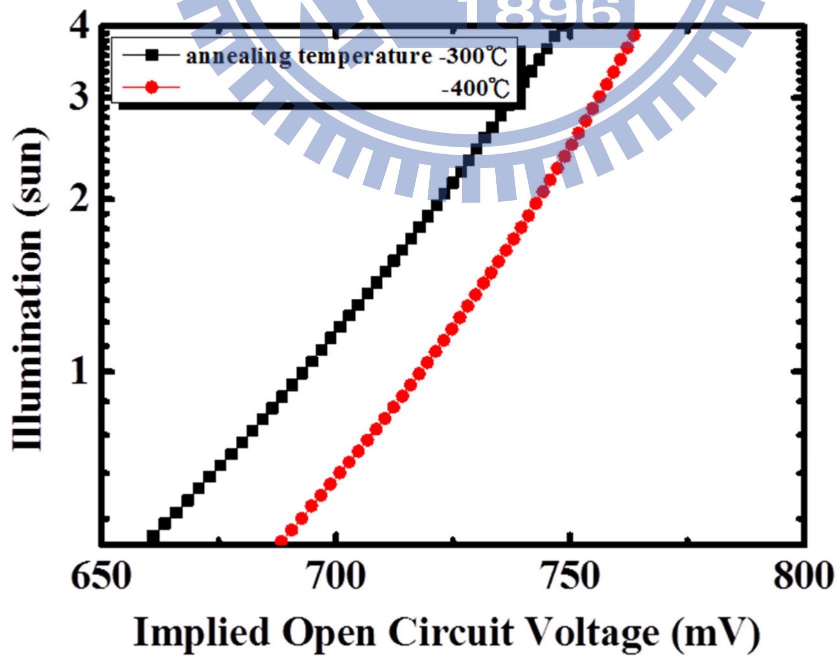


Fig. 3.15 implied open circuit voltage of Al_2O_3 layer at different annealing temperature

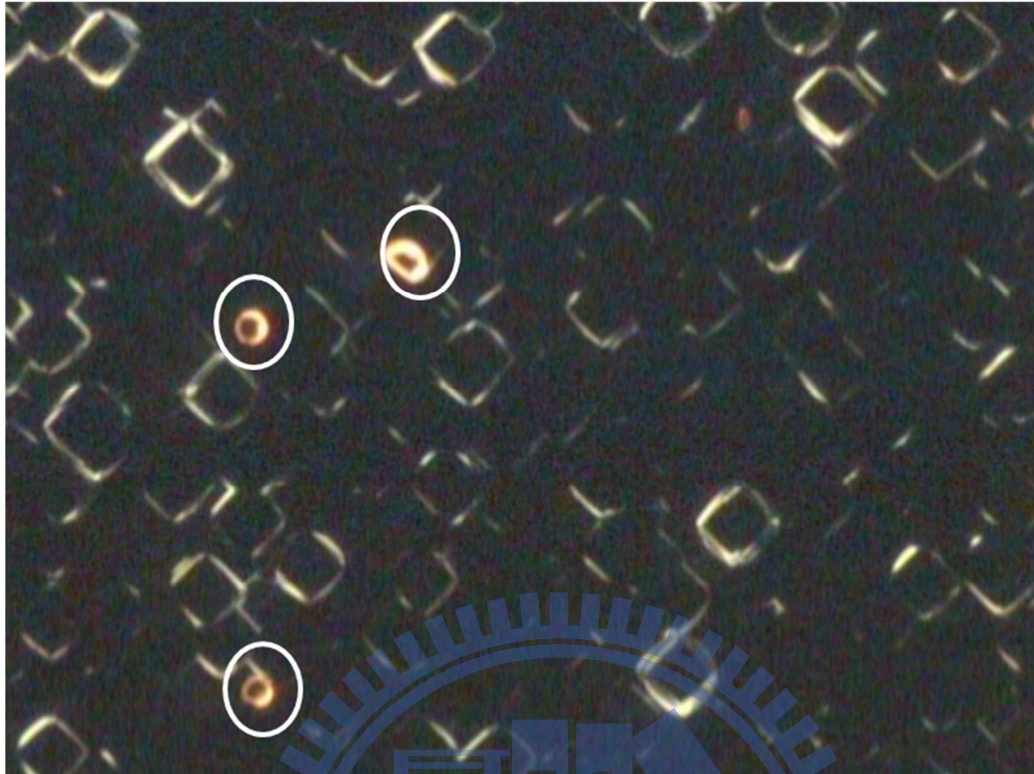


Fig. 3.16 OM image of Al_2O_3 layer at 300℃ annealing

Fig. 3.17 OM image of Al_2O_3 layer at 400℃ annealing

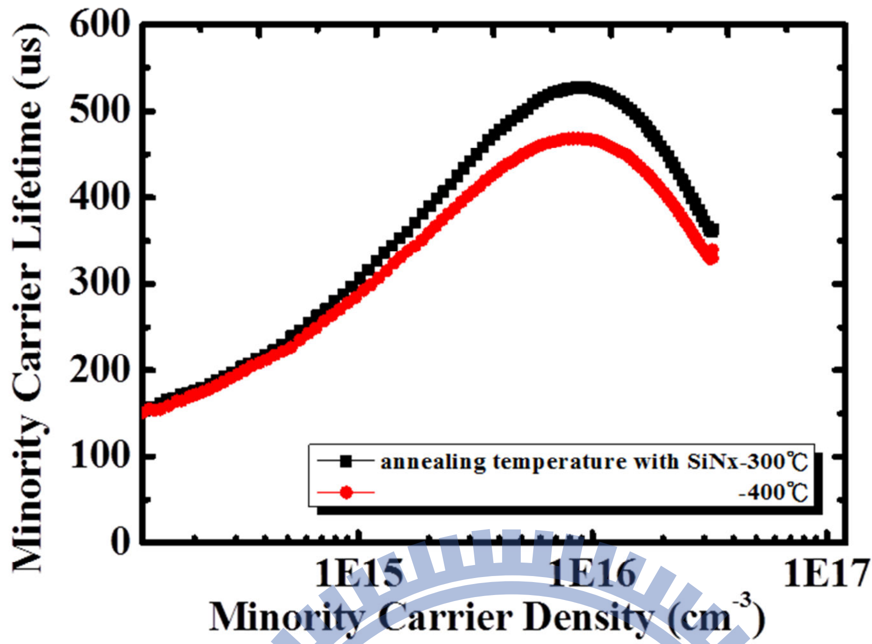


Fig. 3.18 lifetime of Al_2O_3 at different annealing temperature with SiNx capping layer

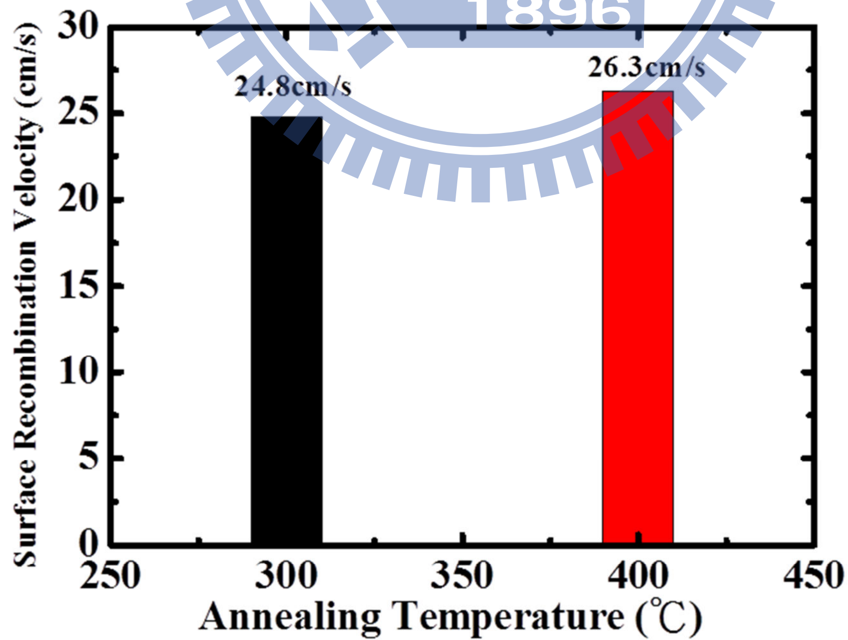


Fig. 3.19 SRV of Al_2O_3 at different annealing temperature with SiNx capping layer

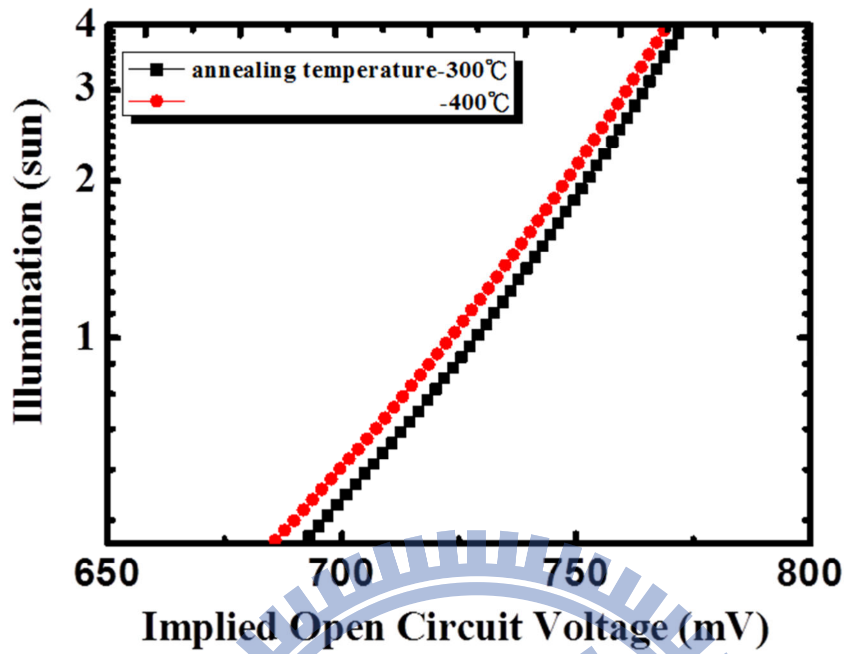


Fig. 3.20 implied open circuit voltage of Al_2O_3 at different annealing temperature with SiNx capping layer

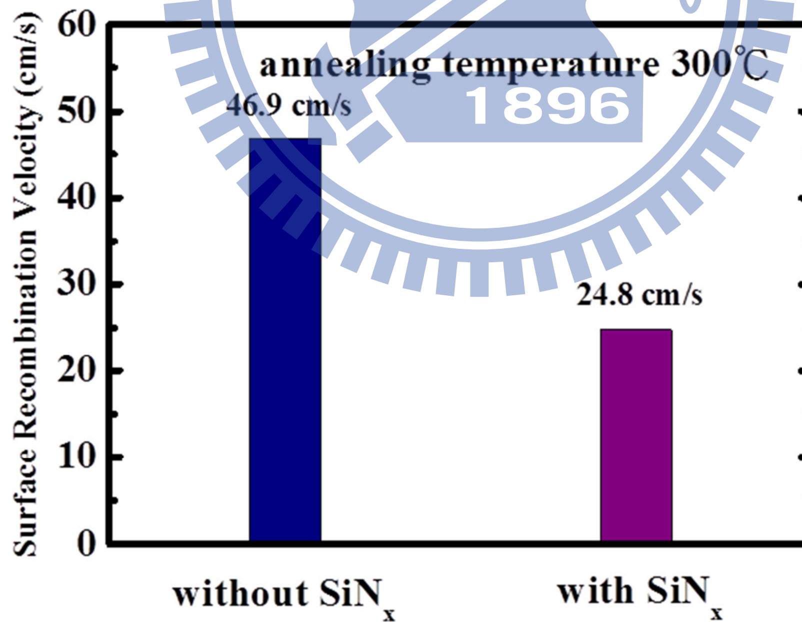


Fig. 3.21 SRV of Al_2O_3 at same 300℃ temperature w/wo SiNx capping layer

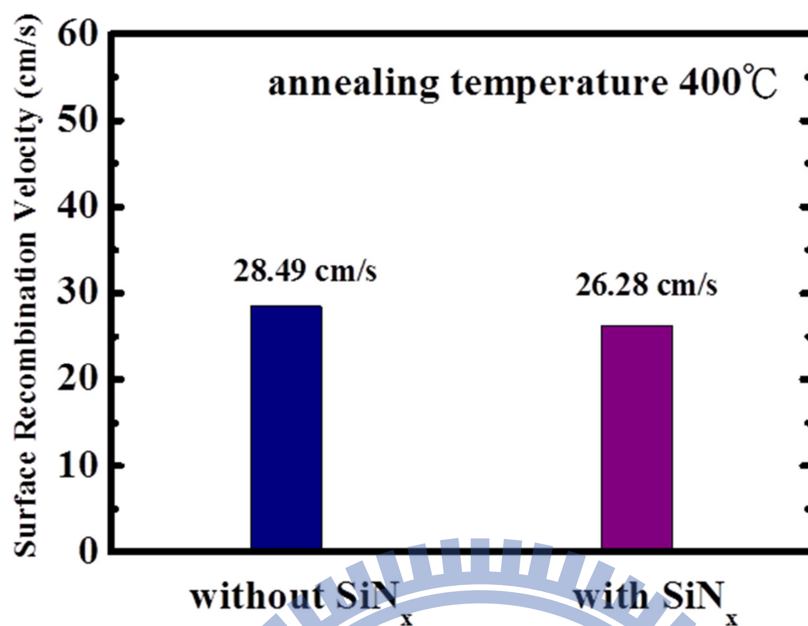


Fig. 3.22 SRV of Al_2O_3 at same 400℃ temperature w/wo SiNx capping layer

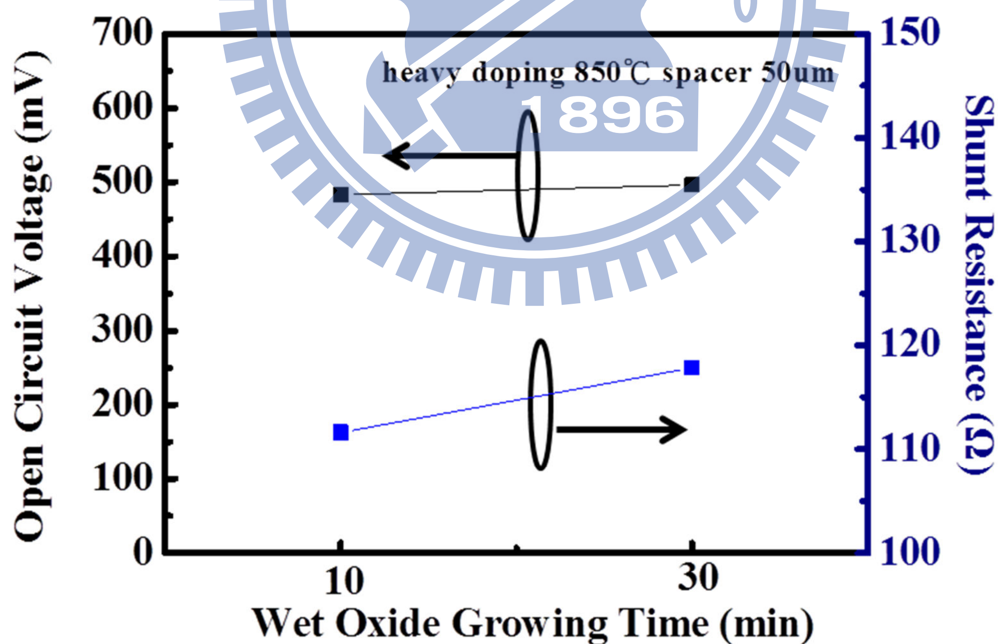


Fig. 3.23 open circuit voltage & shunt resistance comparison for heavy doping with different wet oxide growing time

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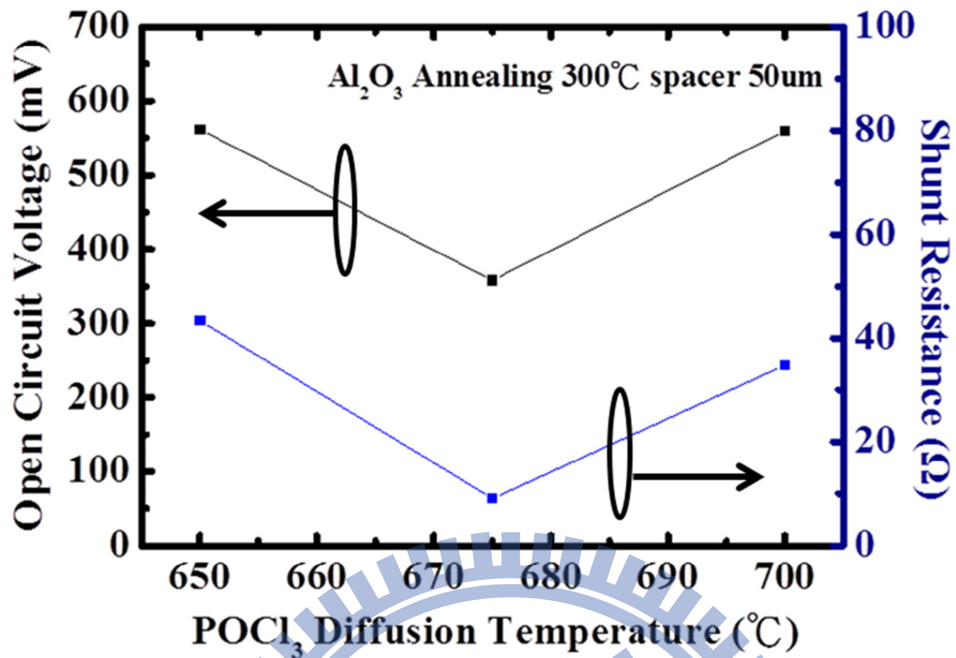


Fig. 3.24 open circuit voltage & shunt resistance comparison for light doping with different temperature, spacer 50um, annealing at 300℃

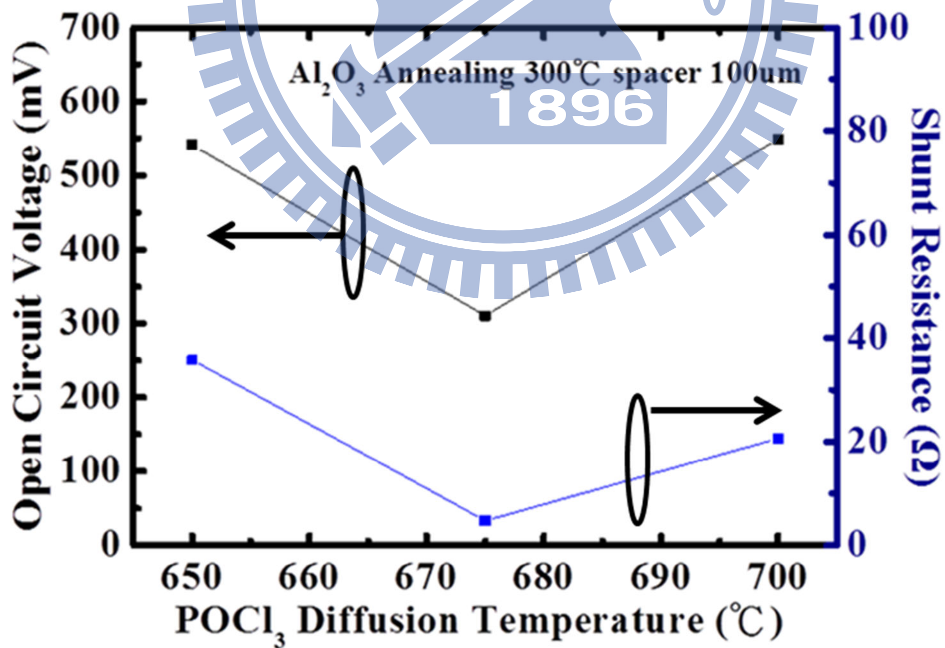


Fig. 3.25 open circuit voltage & shunt resistance comparison for light doping with different temperature, spacer 100um, annealing at 300℃

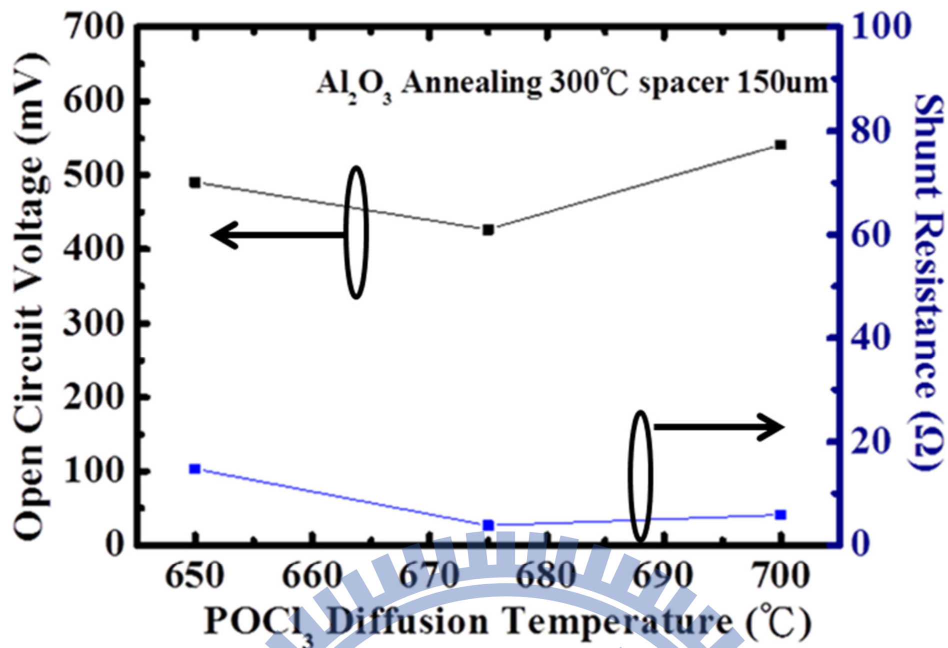


Fig. 3.26 open circuit voltage & shunt resistance comparison for light doping with different temperature, spacer 150um, annealing at 300℃

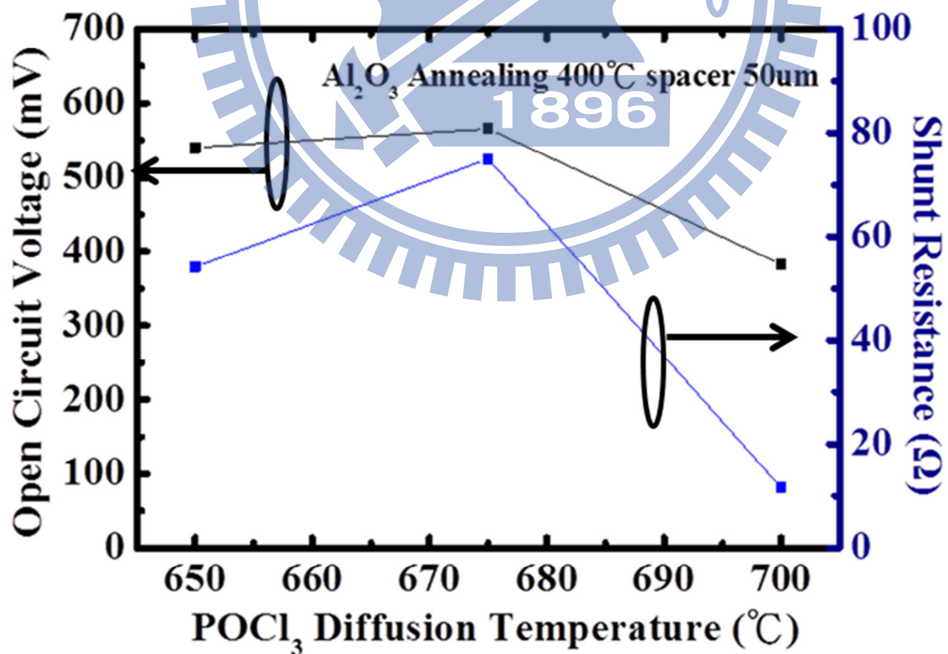


Fig. 3.27 open circuit voltage & shunt resistance comparison for light doping with different temperature, spacer 50um, annealing at 400℃

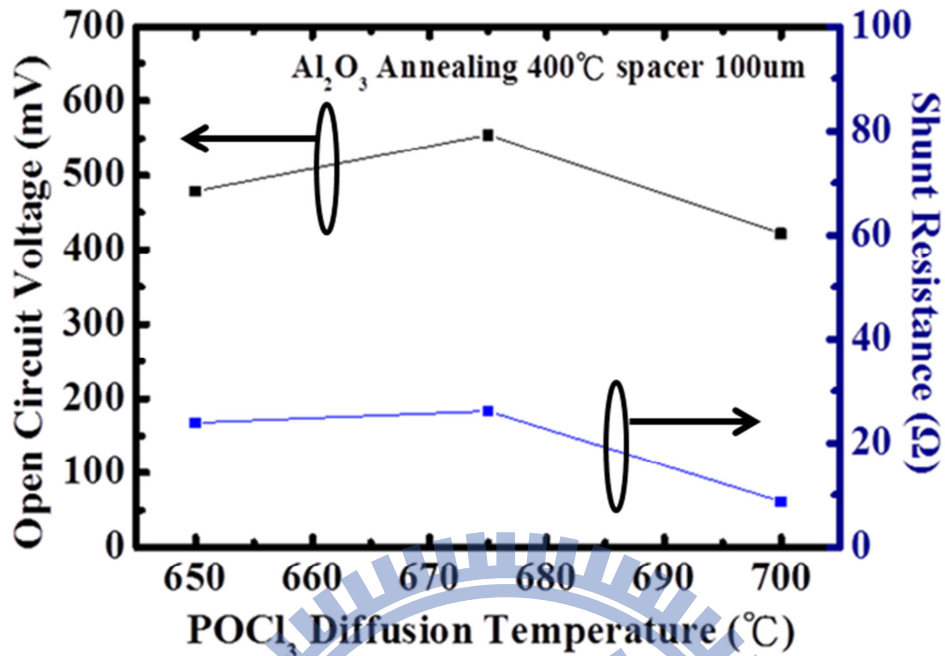


Fig. 3.28 open circuit voltage & shunt resistance comparison for light doping with different temperature, spacer 100um, annealing at 400℃

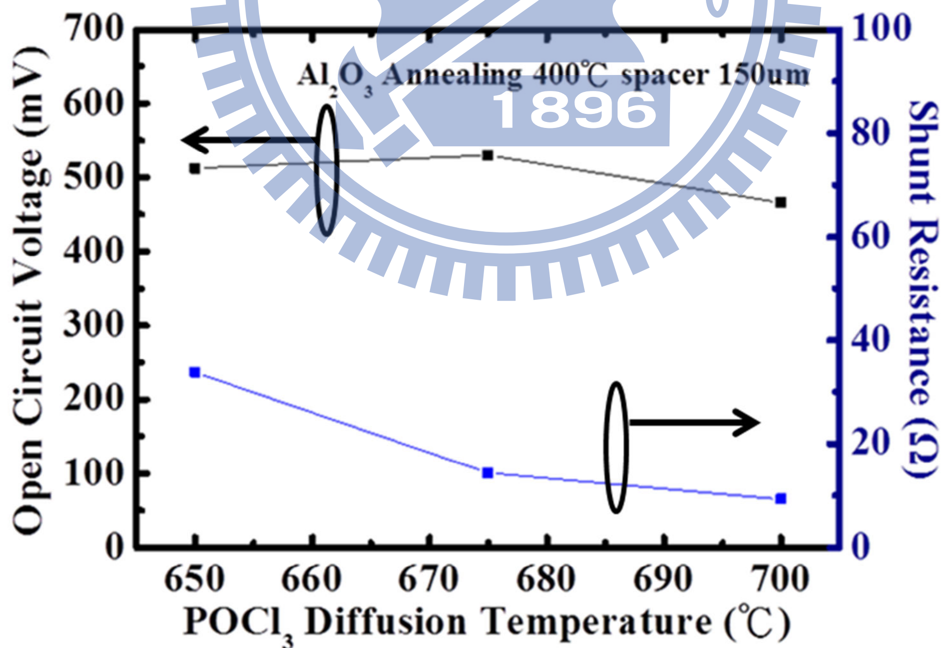


Fig. 3.29 open circuit voltage & shunt resistance comparison for light doping with different temperature, spacer 150um, annealing at 400℃

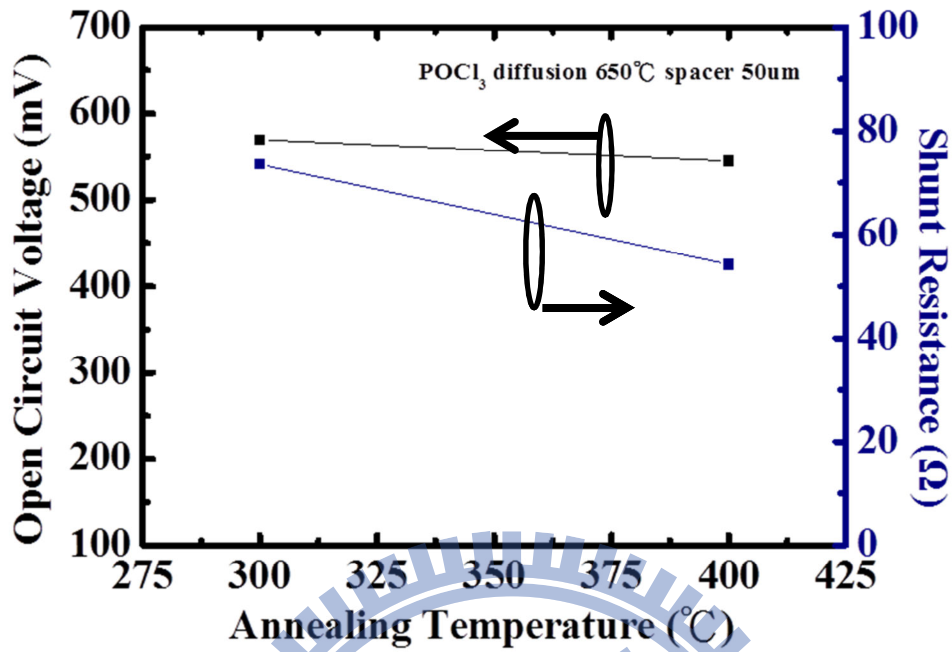


Fig. 3.30 open circuit voltage & shunt resistance comparison for annealing with different temperature, spacer 50um, $POCl_3$ diffusion 650℃

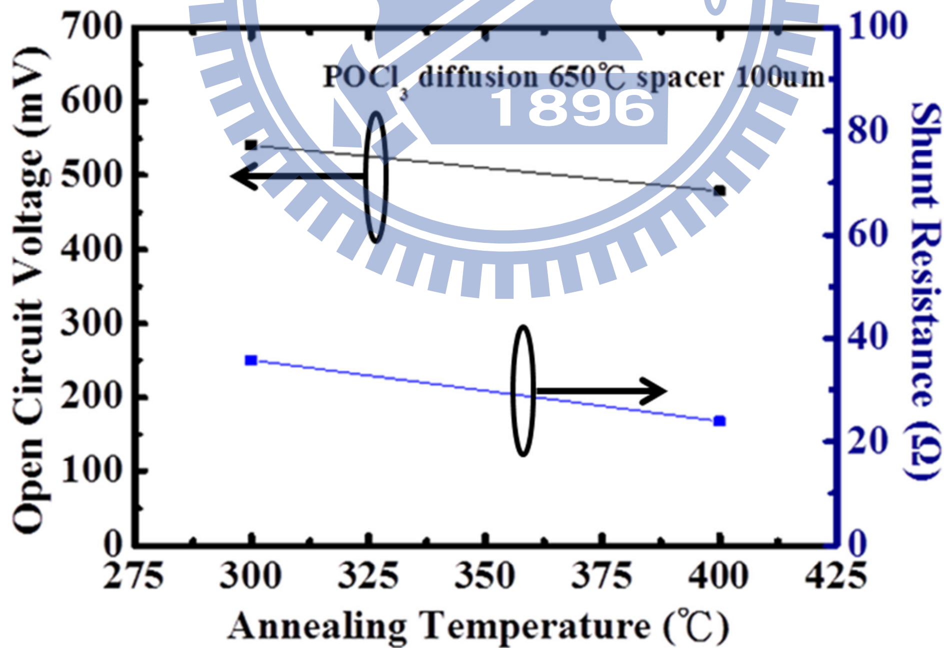


Fig. 3.31 open circuit voltage & shunt resistance comparison for annealing with different temperature, spacer 100um, $POCl_3$ diffusion 650℃

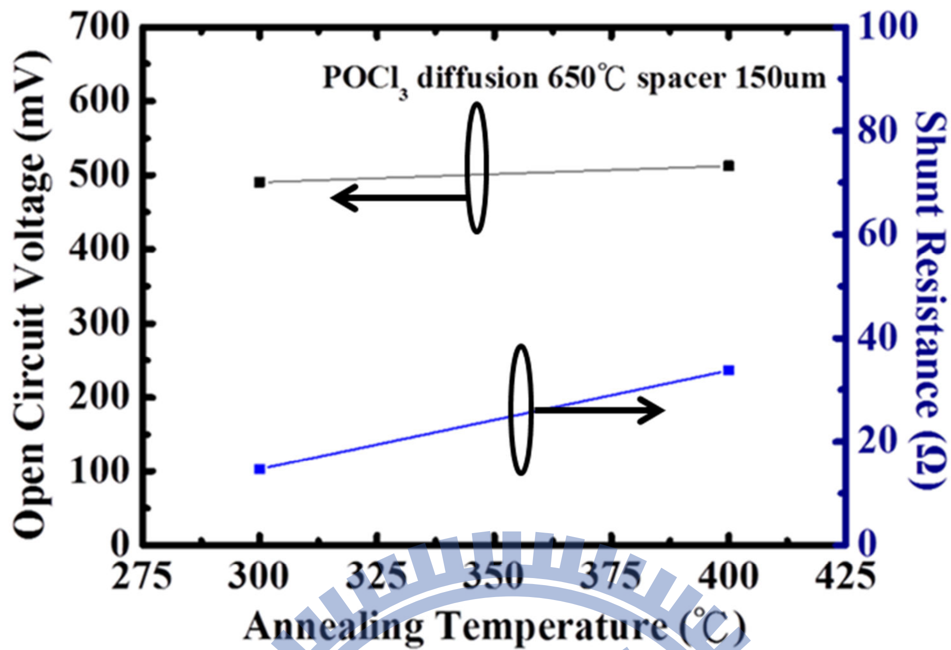


Fig. 3.32 open circuit voltage & shunt resistance comparison for annealing with different temperature, spacer 150um, $POCl_3$ diffusion 650℃

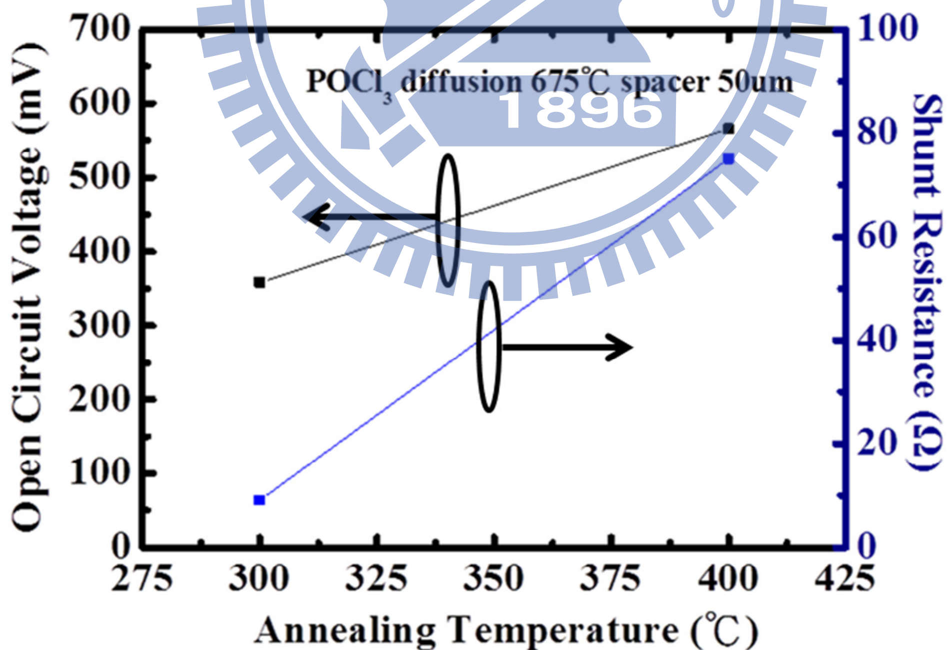


Fig. 3.33 open circuit voltage & shunt resistance comparison for annealing with different temperature, spacer 50um, $POCl_3$ diffusion 675℃

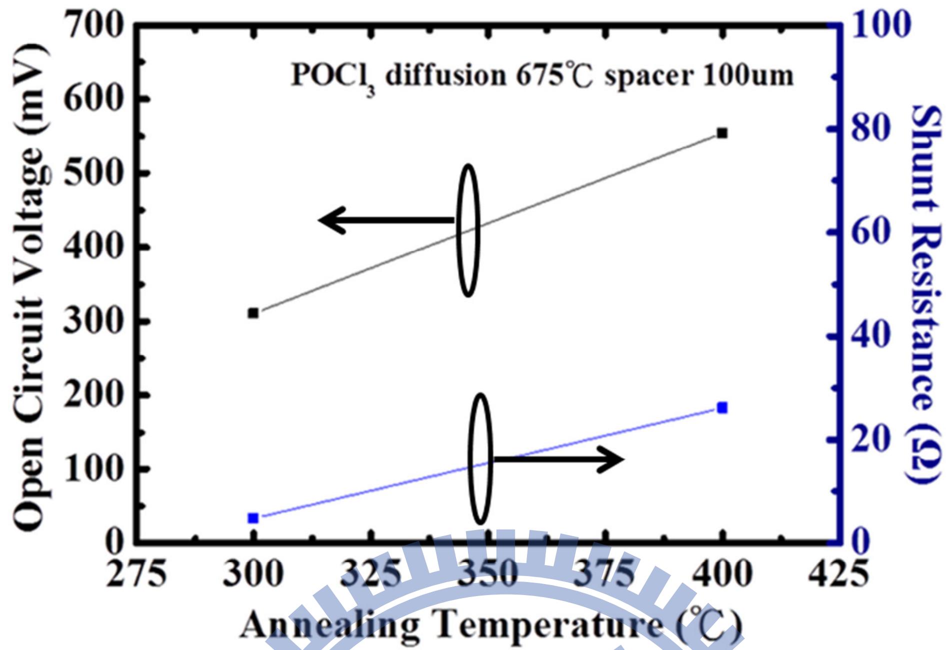


Fig. 3.34 open circuit voltage & shunt resistance comparison for annealing with different temperature, spacer 100um, $POCl_3$ diffusion 675℃

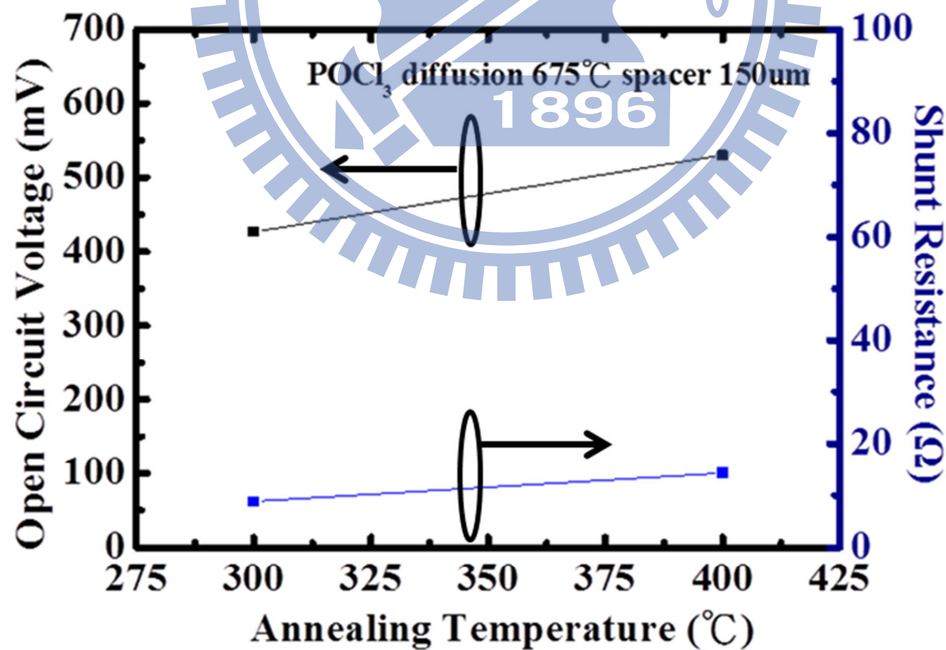


Fig. 3.35 open circuit voltage & shunt resistance comparison for annealing with different temperature, spacer 150um, $POCl_3$ diffusion 675℃

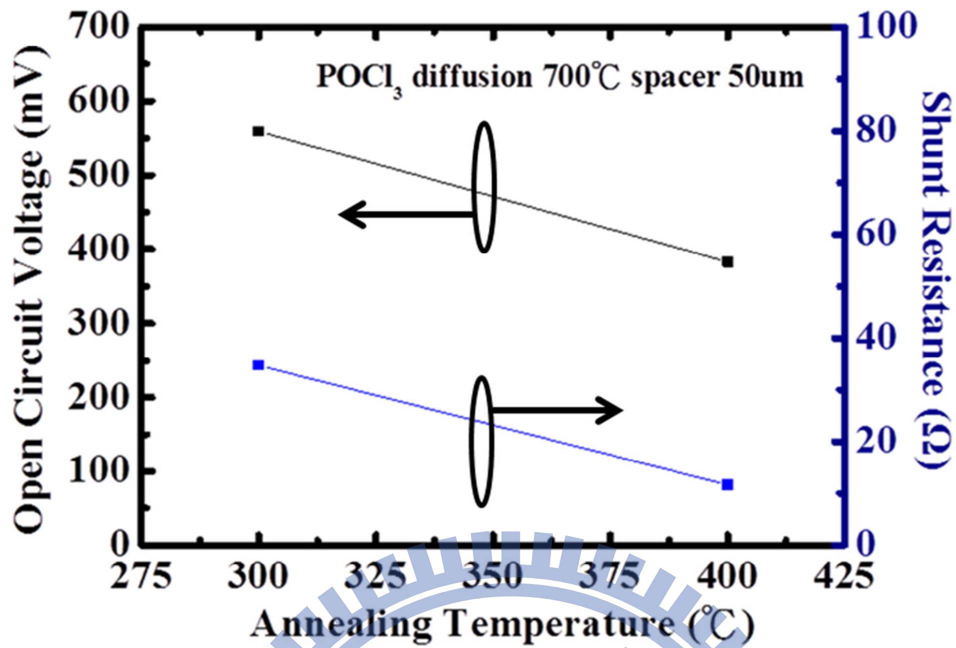


Fig. 3.36 open circuit voltage & shunt resistance comparison for annealing with different temperature, spacer 50um, $POCl_3$ diffusion 700℃

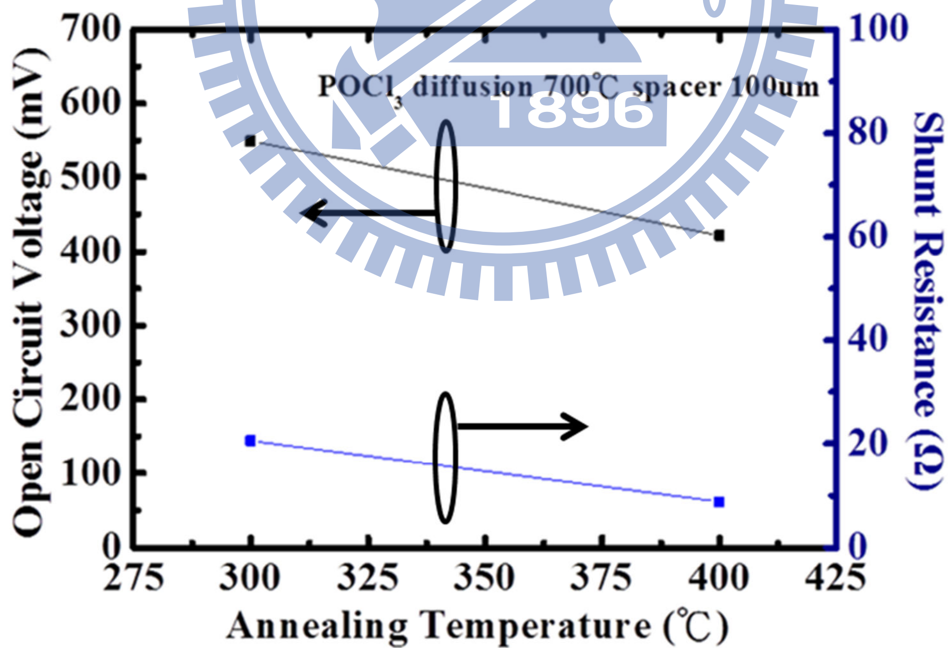


Fig. 3.37 open circuit voltage & shunt resistance comparison for annealing with different temperature, spacer 100um, $POCl_3$ diffusion 700℃

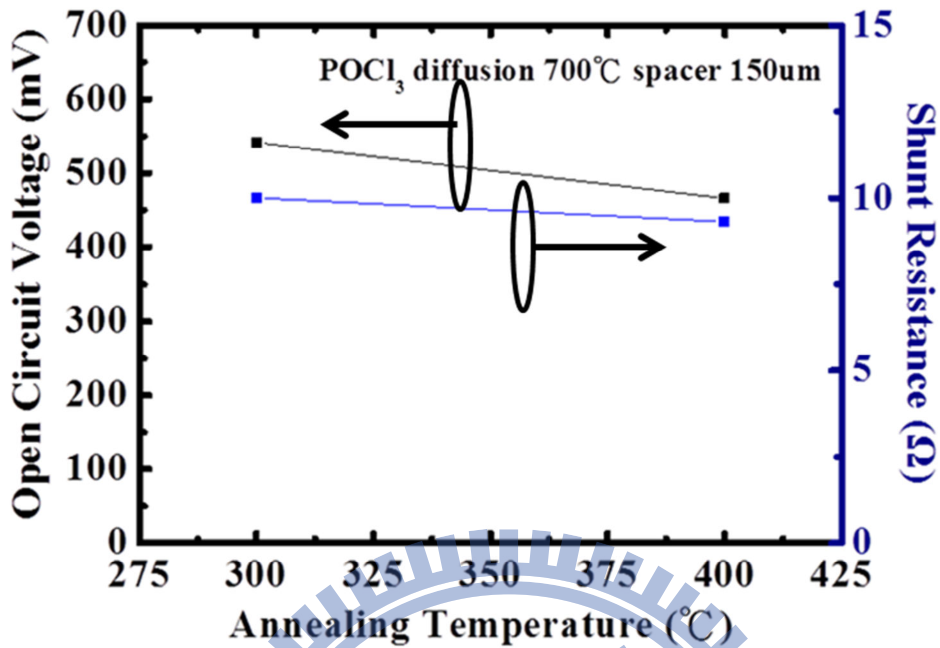


Fig. 3.38 open circuit voltage & shunt resistance comparison for annealing with different temperature, spacer 150um, $POCl_3$ diffusion 700℃

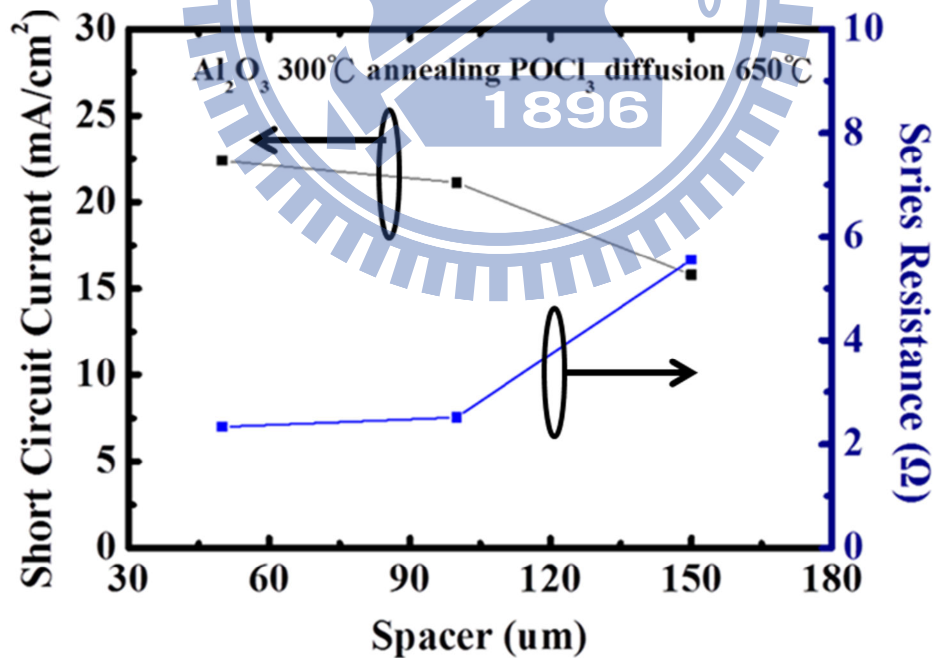


Fig. 3.39 short circuit current & series resistance comparison for different spacer, annealing 300℃, $POCl_3$ diffusion 650℃

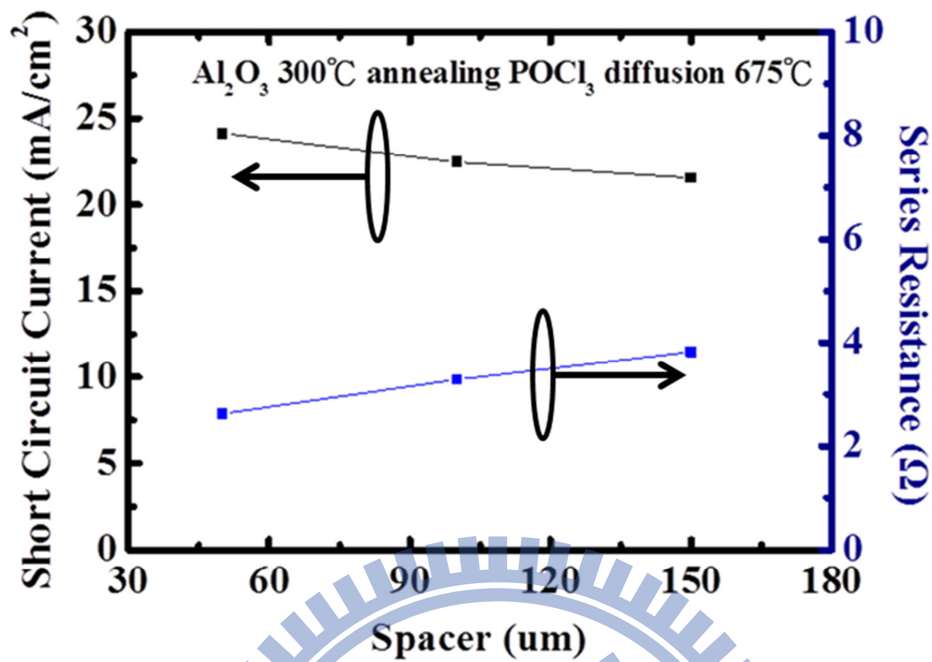


Fig. 3.40 short circuit current & series resistance comparison for different spacer, annealing 300℃, $POCl_3$ diffusion 675℃

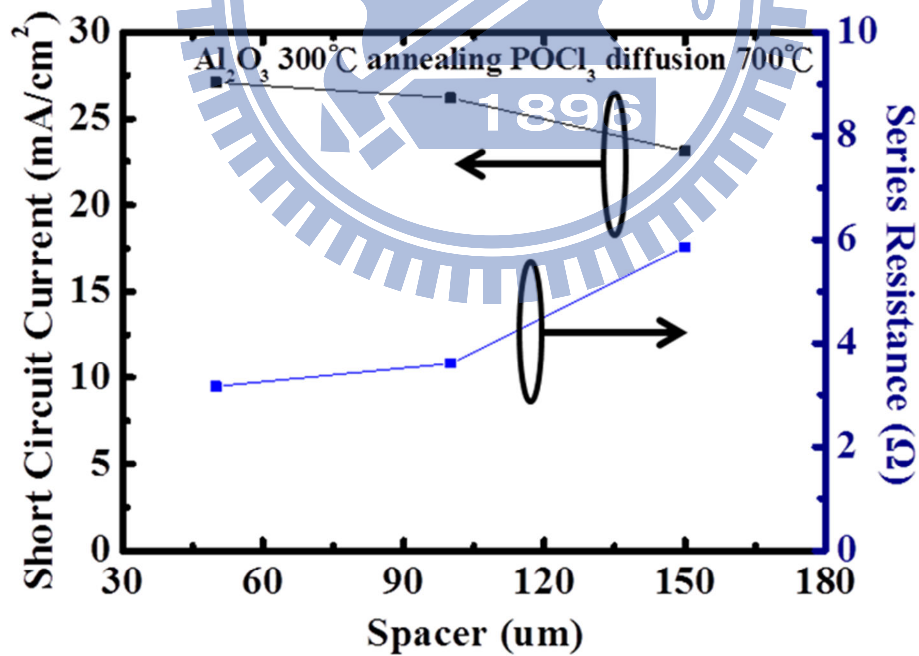


Fig. 3.41 short circuit current & series resistance comparison for different spacer, annealing 300℃, $POCl_3$ diffusion 700℃

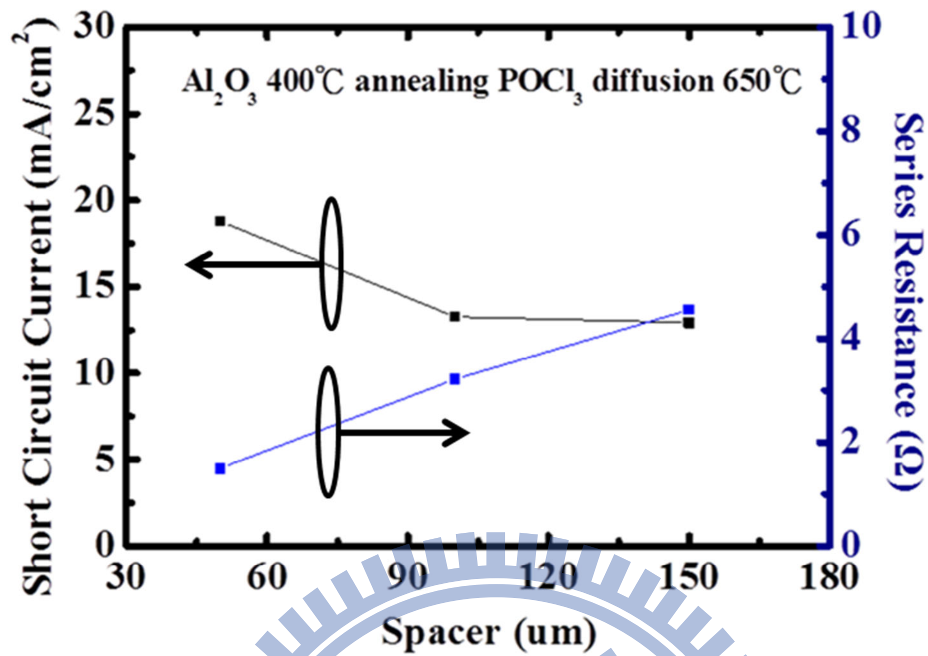


Fig. 3.42 short circuit current & series resistance comparison for different spacer, annealing 400℃, $POCl_3$ diffusion 650℃

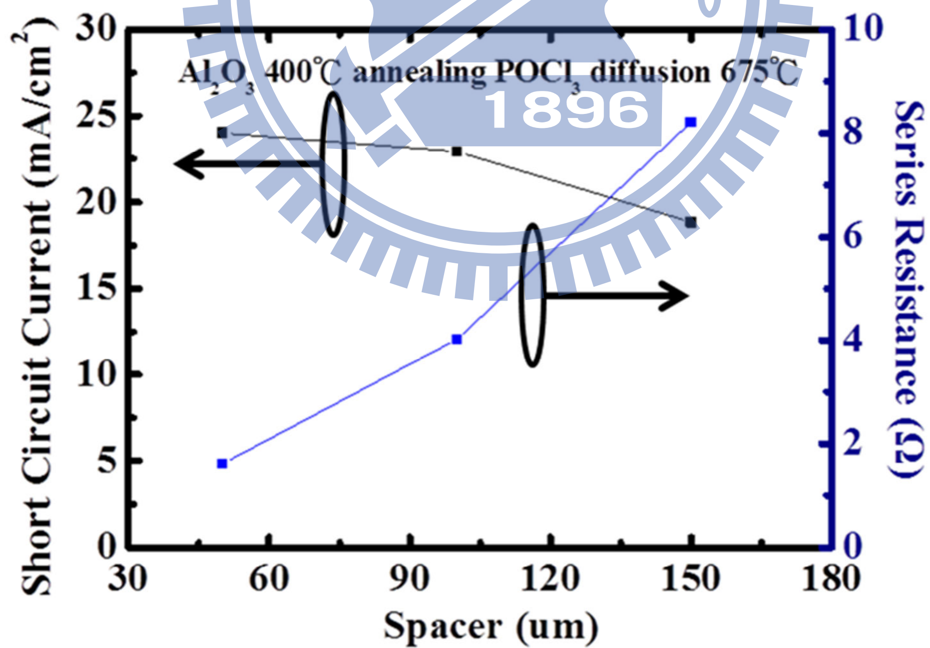


Fig. 3.43 short circuit current & series resistance comparison for different spacer, annealing 400℃, $POCl_3$ diffusion675℃

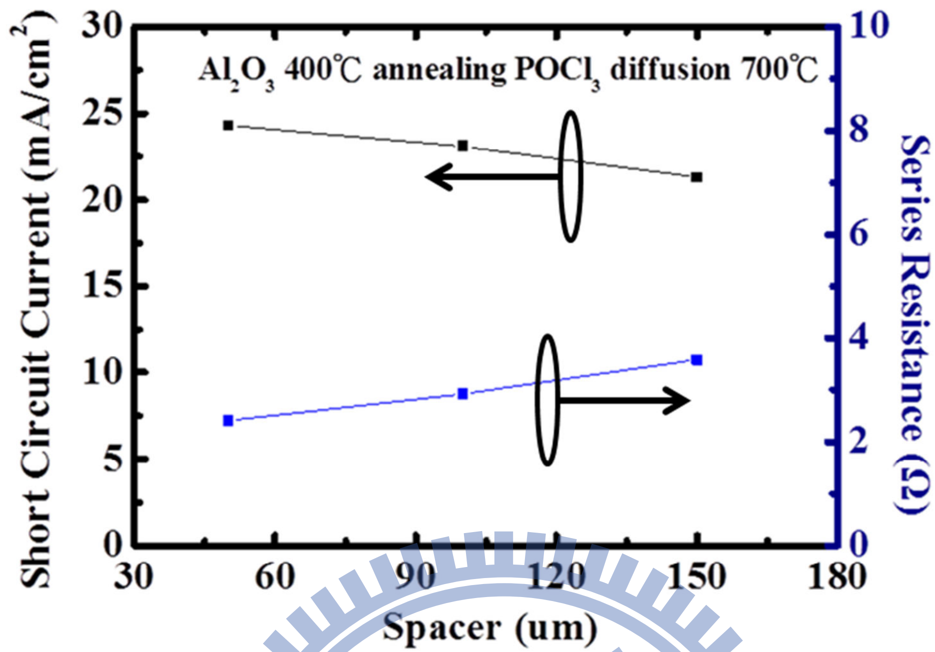


Fig. 3.44 short circuit current & series resistance comparison for different spacer, annealing 400℃, $POCl_3$ diffusion700℃

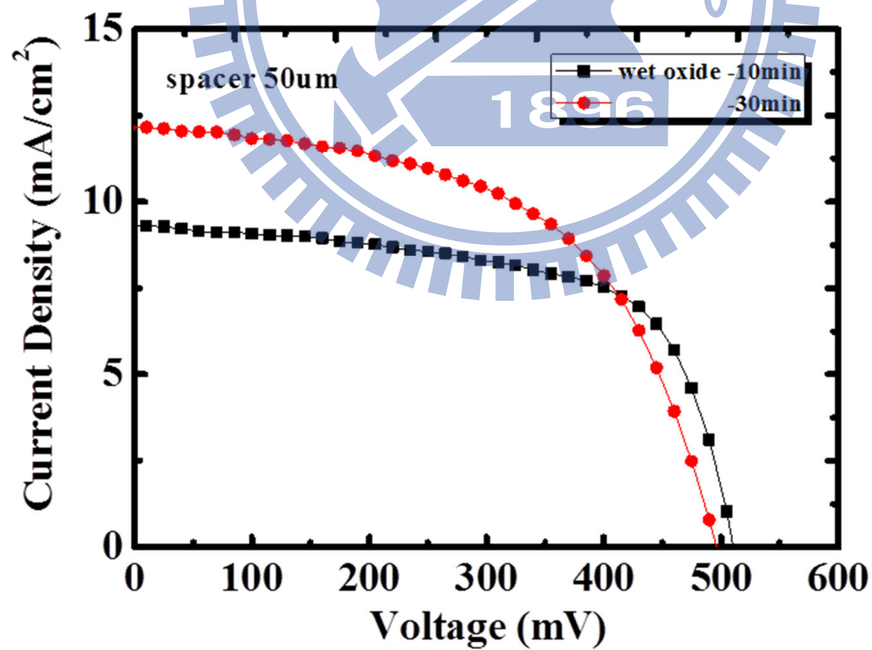


Fig. 3.45 I-V curve comparison of heavy doping with different wet oxide growing time, spacer 50um

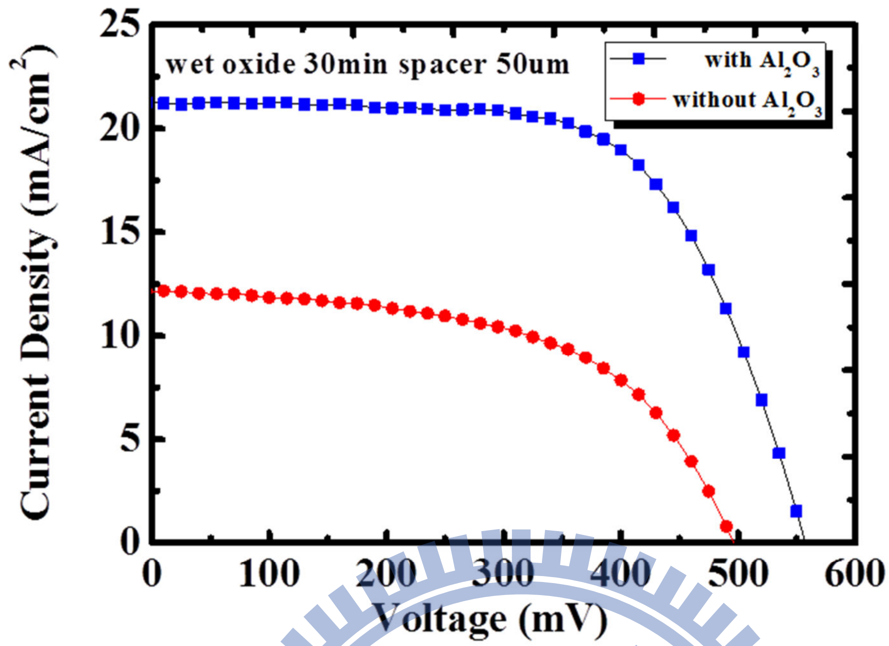


Fig. 3.46 I-V curve comparison of heavy doping w/wo Al_2O_3 passivation

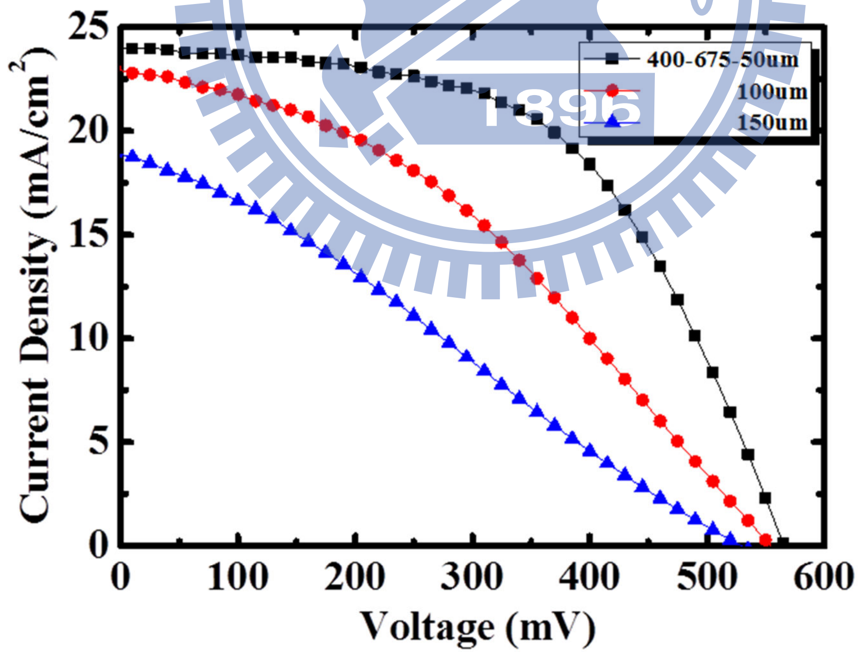


Fig. 3.47 I-V curve comparison of light doping $POCl_3$ diffusion at 675℃ and Al_2O_3 annealing at 400℃

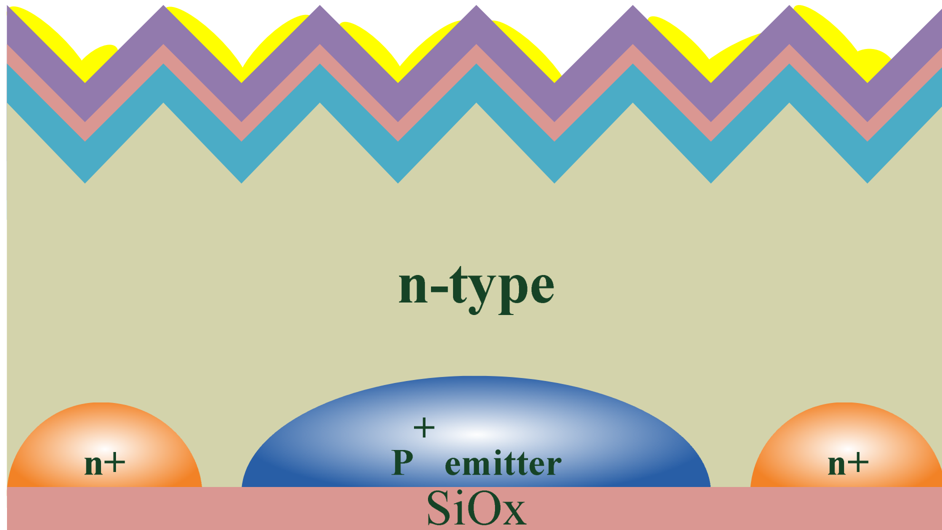


Fig. 3.48 poor uniformity of photoresist coating on texture surface

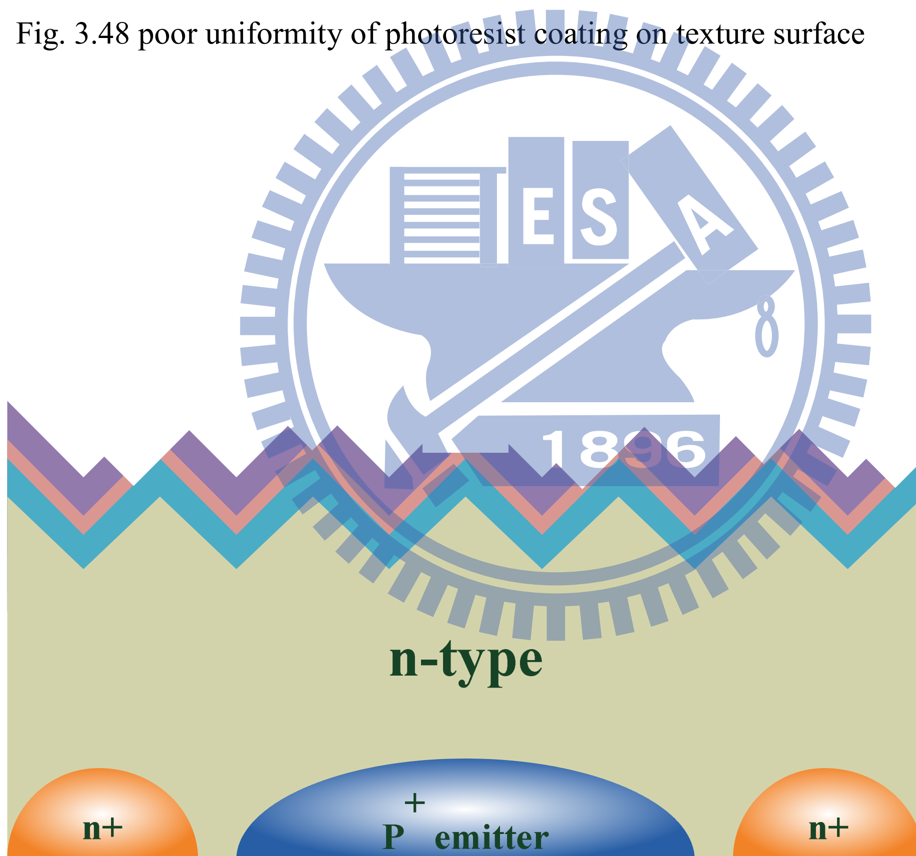


Fig. 3.49 SiNx and PSG etched by HF treatment due to poor uniformity of photoresist at texture surface

Fig. 3.50 damage of front side of device

	$POCl_3$ temperature(℃)	Al_2O_3 annealing temperature(℃)	Spacer width(um)
Sample A	850 with drive in an wet oxide growing 10min	No Al_2O_3	50
Sample B	850 with drive in an wet oxide growing 30min	No Al_2O_3	50
Sample C	850 with drive in an wet oxide growing 30min	400	50
Sample D	650	300	50, 100, 150
Sample E		400	50, 100,150
Sample F	675	300	50, 100, 150
Sample G		400	50, 100, 150
Sample H	700	300	50, 100, 150
Sample I		400	50, 100, 150

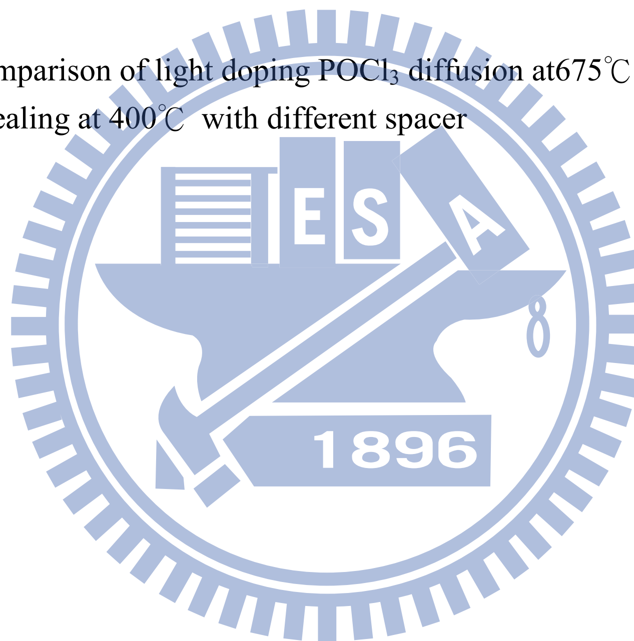
Table 3.1 split table of device fabrication

	Voc (mV)	Jsc (mA/cm^2)	F.F(%)	Efficiency(%)
Wet oxide 10min	483.37	11.46	52.79	2.92
Wet oxide 30min	496.31	12.14	55.1	3.32
Wet oxide 30min with Al_2O_3 passivation	557.54	21.25	60.1	7.59

Table 3.2 comparison of heavy doping device with different treatment

	Voc (mV)	Jsc (mA/cm^2)	F.F(%)	Efficiency (%)
400-675-50	565.8	24	54.3	7.37
400-675-100	554.6	22.9	37.7	4.79
400-675-150	530	18.9	27.8	2.77

Table 3.3 comparison of light doping $POCl_3$ diffusion at675℃ and Al_2O_3 annealing at 400℃ with different spacer



Chapter 4

Conclusion and Future Work

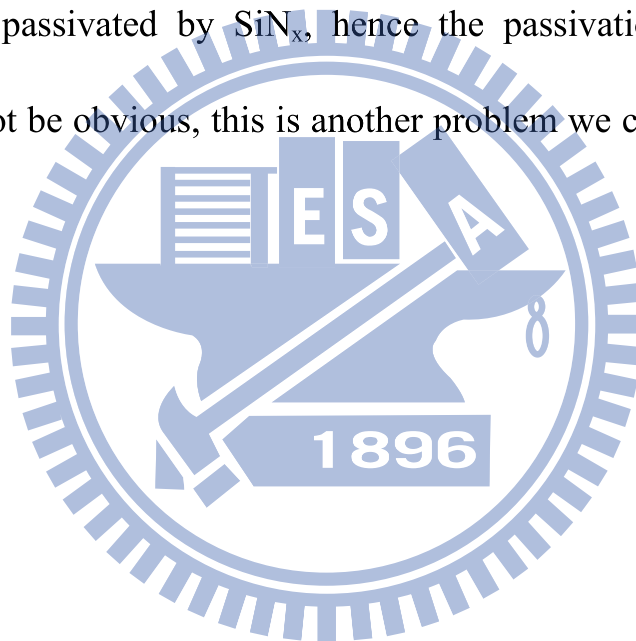
4.1 Conclusion

We have successfully proved light doping $POCl_3$ diffusion and PSG layer provide state-of-art passivation comparing to heavy doping $POCl_3$ diffusion from minority carrier lifetime measurement, and the effect Al_2O_3 layer passivation from test structure, although the result is not outstanding showing on the true IBC solar cell device due to some problems in the fabrication process, the reason of SiNx and PSG etched during HF dip treatment was explained at the end of Chapter 3, and the solution is adopted immediately for the following fabrication process, however the damage could not be recovered. as long as we improved the fabrication process, high efficiency IBC solar cell can be achieved

4.2 Future Work

For recent IBC silicon solar cell, point contact and metal finger which is made by Ti, Pt, Ag stack deposition are guaranteed to achieved better metal contact, reducing contact recombination and resistance

simultaneously. According to the reason we mentioned above, changing metal material and designing new mask for point contact are what we could research in the future, in addition to metal, Al_2O_3 is also a key issue we consider to researching deeply, different Al_2O_3 thickness, the effect of Al_2O_3 for n-type region are worth-attention. Except for all of these, based on mask design, the emitter area passivated by Al_2O_3 is almost equal to n-type region passivated by SiN_x, hence the passivation provided by Al_2O_3 might not be obvious, this is another problem we could improve in future study.



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