Ka/Ku-Band pHEMT Gilbert Mixers With Polyphase and Coupled-Line Quadrature Generators

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***Abstract*—In this paper, three kinds of Ka/Ku-band Gilbert mixers are demonstrated using 0.15-μm AlGaAs/InGaAs pseudomorphic high electron mobility transistor technology. Thanks to the semiinsulating GaAs substrate, microwave passive components have a low-loss feature, and polyphase filters work up to higher frequencies. Highly accurate tantalum–nitride thin-film resistors utilized in polyphase filters result in perfect quadrature operation. Therefore, our proposed single-sideband up-converter operates at 15 GHz with a 63-dB sideband rejection ratio, and another 34-GHz in-phase/quadrature (I/Q) subharmonic down-converter reaches $<$0.4-dB magnitude and $< 1^\circ$ phase errors. More than 50-dB local oscillator (LO) leakage suppression is achieved in the I/Q subharmonic mixer. On the other hand, a 40-GHz stacked-LO subharmonic mixer with a novel compensation technique is also proposed and demonstrated to improve LO speed and reduce the amount of transistors, as compared to previous work.**

***Index Terms*—Compensation, down-converter, polyphase filter, pseudomorphic HEMT (pHEMT), quadrature, single sideband (SSB), subharmonic, up-converter.**

I. Introduction

UNTIL NOW, HEMT technology has played a chief role in microwave and millimeter-wave circuits [1], [2]. The advantages of HEMT transistors, such as large transconductance, great power density, low noise figure (NF), and high breakdown voltage, as well as a semiinsulating GaAs substrate are favorable for circuits operating at high frequencies. Today, the HEMT technology retains the world record for the cutoff frequency and maximum operation frequency (about 500-GHz f_t and about 400-GHz $f_{\max}$) [3]. Obviously, HEMT-based low-noise amplifiers (LNAs) and power amplifiers (PAs) are superior to silicon-based circuits at microwave and millimeter-wave regimes in terms of gain, NF, and power performances [4]–[6]. Much effort has been expended to integrate silicon-based front-end circuits with CMOS analog and logic circuits. However, HEMT-based LNAs and PAs are not yet replaceable for better performance, especially at much higher frequencies. Connections between individual LNAs, PAs, and mixers using different technologies in a module suffer from large loss. It is preferable to implement the front-end circuits with the same process and on the same chip to reduce chip connections at high frequencies. Here, the HEMT technology is the best choice at high-frequency regimes [7].

In the past, different kinds of passive mixers, such as diode mixers and field-effect transistor (FET) resistive mixers, were discussed using the HEMT technology. The diode-based double-balanced mixers and sub-harmonically pumped FET-based resister mixers were realized in K-band and Ka-band frequencies using a GaAs process in commercial products [8]–[10]. These mixers have good linearity, but a larger conversion loss [8]–[12], whereas the traditional microwave passive components based on quarter-wavelength design concepts are not compact and consume the real estate in the integrated circuit (IC) technology [11], [12]. Therefore, analog circuit design concepts are adopted in this paper rather than implementing impedance-matching design approaches. The double-balanced Gilbert mixer is a popular topology for designing an active mixer due to the benefits of high conversion gain, compact size, and good isolation. Recently, increased attention has been paid to complex mixers in modern wireless systems. Many Gilbert complex mixers have been realized using CMOS and SiGe HBT technologies, mostly at low frequencies. Lately, advancements in silicon device scaling have made Gilbert mixers possible even at millimeter-wave frequencies [13], [14].

Complex mixers with both in-phase (I) and quadrature (Q) phase mixing are employed to image rejection mixers and single-sideband (SSB) up-converters. The resistor–capacitor (RC) capacitor–resistor (CR) polyphase filters [15]–[19] are used to generate the differential quadrature signals needed by complex mixers and subharmonic mixers. However, the RC–CR polyphase filters in CMOS and SiGe HBT technologies were realized below 2 GHz because it is difficult to fabricate accurate small resistors and capacitors at high frequencies due to the Si substrate parasitic effect [17]. Even with electronic tuning, the complex Gilbert mixers based on the silicon technology can function at up to 6 GHz and the uncalibrated sideband rejection of the SSB Gilbert mixer at 6 GHz is 48.2 dB [18], [19]. On the contrary, the GaAs-based technology has accurate thin-film resistors, metal–insulator–metal (MIM) capacitors and no parasitic substrate effect. Thus, the resistors and capacitors required for the polyphase filter can be implemented in a precise way. The high accuracy in GaAs-based thin-film resistors comes from the *in-situ* film thickness monitor during processing. A 5-GHz complex mixer with accurate RC–CR polyphase filters has been

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realized in GaInP/GaAs HBT technology, but the performance is limited by the GaInP/GaAs HBT device due to its low f_t [20]. At high operating frequencies, a quadrature coupler is another good choice for complex mixers. Nevertheless, the silicon-based coupler has a poor quality factor and bad magnitude balance at high frequencies. The 5.9-GHz CMOS I/Q subharmonic mixer with a quadrature coupler and transformers at the RF path reveals a large magnitude mismatch in the output waveforms [21].

The subharmonic Gilbert mixer also plays an important role because the local oscillator (LO) frequency of a subharmonic mixer is only half of the fundamental mixer's LO frequency. This can solve the problem associated with generating LO signals at high frequencies. However, at high LO frequencies, the transistor time delay destroys the frequency doubling mechanism in the LO stage so that the LO speed and the RF-to-IF isolation degrade [22]. Thus, a time-delay compensator is proposed at the stacked-LO stage to improve the performances of the subharmonic Gilbert mixer in this paper. This time-delay compensated subharmonic Gilbert mixer is reformed based on the previous work [22] to reduce the amount of transistors and to balance the current density of the transistors at the current commutating stages.

The low breakdown voltage in the advanced silicon technology makes the analog circuit design approach difficult. Thus, GaAs-based pseudomorphic HEMT (pHEMT) technology with a high cutoff frequency, high breakdown voltage, and semiinsulating substrate becomes the technological choice for high-frequency complex Gilbert mixers and subharmonic Gilbert mixers. Thus far, very few papers on Gilbert mixers incorporating HEMT technology have been published [23]–[26]. The 0.15-μm pHEMT technology employed has an 85-GHz f_t and 10-V breakdown voltage. The high-performance active devices and precise passive components are utilized to realize several typical pHEMT Gilbert up- and down-converters, which are fundamental, leveled-LO, and stacked-LO subharmonic Gilbert mixers. In Section II-A, Monte Carlo simulations are employed to verify that the polyphase filter on the GaAs substrate has better accuracy than that on the silicon substrate. In Section II-B, the S-matrices of the two types of differential quadrature coupled-line generators are analyzed for our Gilbert mixer at an RF port. In Section II-C, the novel time-delay compensator, which cancels the phase error, is explained. From the experimental results, polyphase filters and 90°/180° passive couplers used at the LO and RF stages are suitable for applications in the microwave and millimeter-wave regimes. A 15-GHz Ku-band pHEMT SSB complex Gilbert up-converter of 63-dB sideband rejection is realized in Section III-A. A 34-GHz quadrature RF subharmonic down-converter with I/Q outputs is successfully demonstrated in Section III-B, and a 40-GHz stacked-LO subharmonic mixer with a novel compensation technique is represented in Section III-C.

II. Component Design of Millimeter- Wave Gilbert Mixer With Quadrature Features

A. Polyphase Filter Design Using Monte Carlo Simulation for GaAs and CMOS Technologies

There are two common methods to design a quadrature generator—one is a polyphase filter and the other is a coupler. A

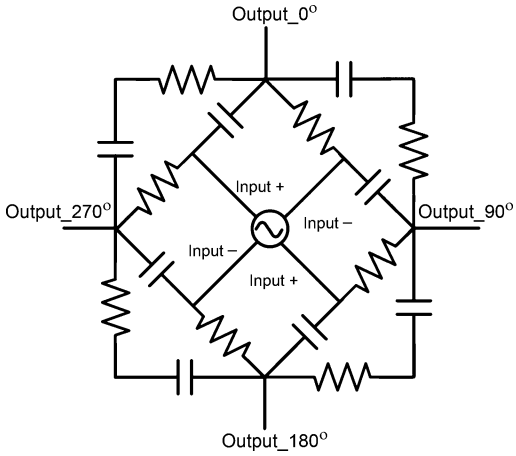

Fig. 1. Two-section RC–CR polyphase filter structure.

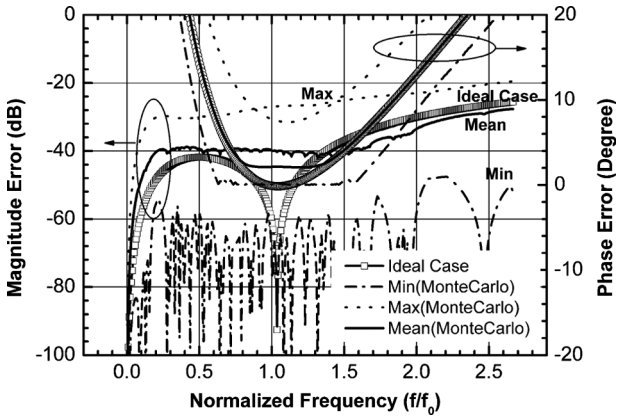

Fig. 2. Magnitude and phase errors of the two-section polyphase filter by Monte Carlo simulations with resistance and capacitance variations.

polyphase filter is composed of sequential R–C and C–R components. The one-stage RC–CR polyphase filter is only designed at a center frequency and usually many stages are cascaded to tolerate mismatch errors. A two-section polyphase filter is shown in Fig. 1. This topology can generate balanced quadrature signals with equal amplitude at 0°, 90°, 180°, and 270° when R and C values are designed at the desired frequency $\omega = 1/(\mathrm{RC})$. The two-stage polyphase filter has lower sensitivity to process variations than a one-stage. Thus, the two-stage polyphase filter is adopted in our mixer design to achieve optimum tradeoffs in terms of magnitude balance, phase error, loss, and layout size.

In the GaAs pHEMT technology, the tantalum–nitride (TaN) thin-film resistors and MIM capacitors possess a sheet resistance of $50\ \Omega/\mathrm{sq} \pm 2\%$ and a unit capacitance of $0.4\ \mathrm{fF}/\mu\mathrm{m}^2 \pm 10\%$ [7], respectively. On the other hand, the poly resistors and MIM capacitors in the TSMC 1P6M 0.18-μm CMOS technology have $7.58\ \Omega/\mathrm{sq} \pm 25\%$ and $1\ \mathrm{fF}/\mu\mathrm{m}^2 \pm 15\%$, respectively. Compared with the silicon-based technology, the semiinsulating GaAs-based HEMT process has better accuracy for passive components. The *in-situ* film thickness monitor in the thin-film resistor fabrication enhances resistance accuracy. According to Monte Carlo simulations with process variations, the maximum phase mismatch of 7° and magnitude error of −28 dB in a two-section GaAs-based polyphase filter for the worst case are shown at the desired frequency (f_0) in Fig. 2.

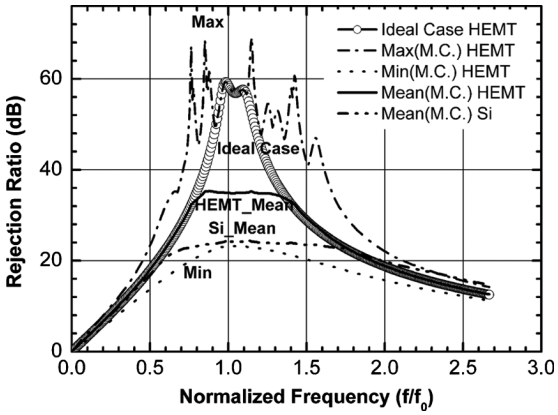

Fig. 3. Rejection ratio of Si- and GaAs-based polyphase filters by Monte Carlo simulations.

Fig. 3 describes the rejection ratio of the two-stage polyphase filters between the silicon- and GaAs-based technologies using Monte Carlo simulations with resistance and capacitance variations. The formula for the sideband and image rejection ratios is expressed as

$$\text{Rejection ratio (dB)} = 10\log\left\{\frac{(1+\chi)^2+2(1+\chi)\cos\theta+1}{(1+\chi)^2-2(1+\chi)\cos\theta+1}\right\} \quad (1)$$

with the function of amplitude (χ %) and phase (θ °) errors [7]. The mean rejection ratio of the GaAs-based polyphase filter reaches 34 dB, but there is only a 24-dB rejection ratio for the silicon-based counterpart. A 60-dB rejection ratio can be achieved in the ideal case.

B. Performance Analysis of Differential Quadrature Coupled-Line Generator

The passive RC–CR polyphase filter is more suitable for applications below 30 GHz, while a quadrature coupler consumes formidably large sizes at lower frequencies. However, as the operating frequency becomes higher and higher, the polyphase filters are not easily realized due to process limitations, interconnection delays and high driven power requirements so that a quadrature coupler becomes a preferable alternative. At 30 GHz, a quarter-wavelength coupled line is about 1000 μm. The layout size of a coupler can be further reduced by the spiral shape, and thus a coupler can be easily implemented in the ICs above 30 GHz.

There are two methods to generate differential quadrature signals based on microwave components. One is a quadrature coupler followed by two Marchand baluns and the other is a Marchand balun before two quadrature couplers, as illustrated in Fig. 4(a) and (b), respectively. All quadrature couplers are terminated with a 50-Ω resistor at the isolation port. Since the Marchand balun is composed of two back-to-back quadrature couplers, the first topology has five couplers, while the second counterpart has four couplers. These five-port scattering parameter matrices can be obtained by the heuristic derivation, as developed in [27]. The scattering parameter matrix for each differential quadrature generator is shown in (2) at the bottom of this page and (3), shown at the bottom of this page with the S-parameters (S_{11B}, S_{12B}, S_{22B}, and S_{23B}) of the Marchand balun, as defined in [27] and [28], and with the coupling coefficient (C_Q) and through coefficient (T_Q) of the quadrature coupler in possession of perfect matching and isolation. Obviously, these two combinations produce the same differential quadrature outputs. The input return loss of the first type is improved by the factor of $(T_Q^2+C_Q^2)$ in comparison with the second counterpart because the reflected power caused by the impedance mismatch between the coupler and balun can be absorbed totally at the isolation port of the coupler. Fig. 4(c) shows the input return loss of the two topologies of the differential quadrature generators with coupler factors, $\sqrt{1/2}$ and $\sqrt{1/3}$ for a coupler and a Marchand balun, respectively [27], [28]. There is more than 75% bandwidth expansion of 10-dB input return loss in the first structure. This design approach is commonly used in balanced amplifiers. In the first structure, the two Marchand baluns do not interfere with each other since $S_{24(42)}$, $S_{25(52)}$, $S_{34(43)}$, and $S_{35(53)}$ are equal to zero.

In this paper, the structure of the coupler followed by two Marchand baluns is employed at the RF input stage and connected with common-gate-configured transistors with 50-Ω input impedance. The ac grounded terminals in the Marchand

$$[S_a]=\begin{bmatrix} S_{11B}\left(T_Q^2+C_Q^2\right) & T_QS_{12B} & -T_QS_{12B} & C_QS_{12B} & -C_QS_{12B} \\ T_QS_{12B} & S_{22B} & S_{23B} & 0 & 0 \\ -T_QS_{12B} & S_{23B} & S_{22B} & 0 & 0 \\ C_QS_{12B} & 0 & 0 & S_{22B} & S_{23B} \\ -C_QS_{12B} & 0 & 0 & S_{23B} & S_{22B} \end{bmatrix} \quad (2)$$

$$[S_b]=\begin{bmatrix} S_{11B} & T_QS_{12B} & -T_QS_{12B} & C_QS_{12B} & -C_QS_{12B} \\ T_QS_{12B} & T_Q^2S_{22B} & T_Q^2S_{23B} & T_QC_QS_{22B} & T_QC_QS_{23B} \\ -T_QS_{12B} & T_Q^2S_{23B} & T_Q^2S_{22B} & T_QC_QS_{23B} & T_QC_QS_{22B} \\ C_QS_{12B} & T_QC_QS_{22B} & T_QC_QS_{23B} & C_Q^2S_{22B} & C_Q^2S_{23B} \\ -C_QS_{12B} & T_QC_QS_{23B} & T_QC_QS_{22B} & C_Q^2S_{23B} & C_Q^2S_{22B} \end{bmatrix} \quad (3)$$

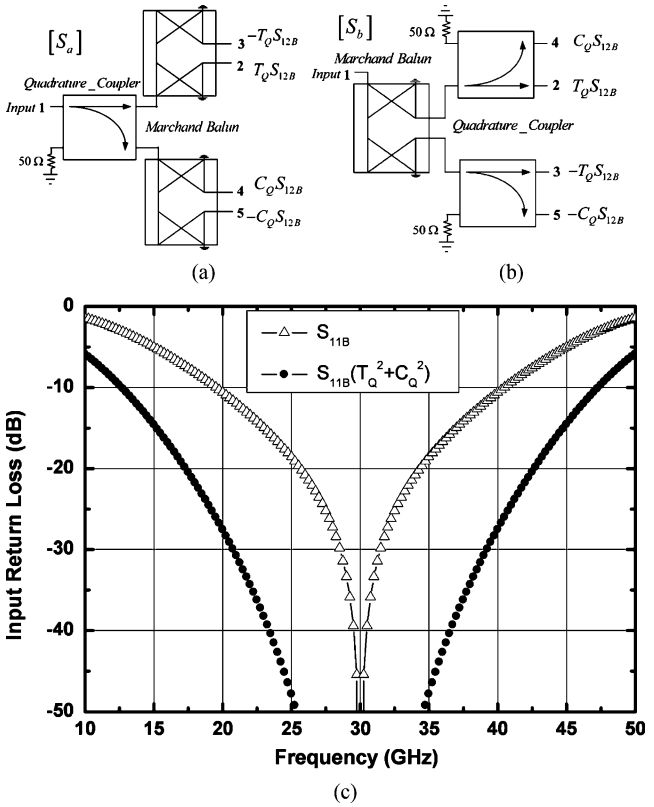

Fig. 4. Differential quadrature generator consists of: (a) one coupler with two baluns or (b) one balun with two couplers. (c) Simulated input return loss of (a) and (b) differential quadrature generators.

balun can be used as the dc grounds for the common-gate-configured transistors [29]. Thus, this structure does not need to add an auxiliary ac choke and an auxiliary dc blocking capacitor to separate the ac signal and dc bias of the mixers. The layout size can also be reduced by the first topology because of no extra biasing components.

C. Stacked-LO Subharmonic Gilbert Cell With Time-Delay Compensation

A transistor has a finite time delay between the output drain current and input gate voltage. The *I–V* transfer function of a transistor can be expressed by the gate–source voltage, the drain–source voltage, and the time delay τ. When the gate–source port of a transistor is fed by a step voltage function, the output drain shows up after the phenomenological time delay τ, which is generally one-third of the transistor transit-time delay. Thus, the adiabatic approximation for *I–V* characteristics is used when the operating frequency is much slower than the inversion of the time delay $\tau(\omega \ll 1/\tau)$ [15]. However, the time-delay problem cannot be ignored when a mixer operates at higher frequency.

A conventional stacked-LO subharmonic Gilbert mixer is shown in Fig. 5. The stacked-LO stage provides a frequency doubling mechanism when differential quadrature LO signals are applied. Thus, the mixer outputs are $2\cos(2\omega_{\rm LO}t)i_{\rm RF}$ and $-2\cos(2\omega_{\rm LO}t)i_{\rm RF}$ at nodes A and C, respectively. However, the finite transistor delay $\theta = \omega\tau$, which is pronounced at high frequencies, introduces the extra dc term $\sin(\theta)$ at nodes A and C. This dc offset problem makes the LO speed of a conventional stacked-LO subharmonic Gilbert mixer slow and degrades the RF-to-IF isolation. A novel time-delay compensated subharmonic Gilbert mixer is proposed and analyzed in Fig. 5. The time-delay compensator is employed at the stacked-LO stage to improve the LO speed and isolation of the subharmonic Gilbert mixer. The upper/lower LO stages of the conventional stacked-LO stage and compensator are fed with $(I+, I-)/(Q+, Q-)$ and $(Q+, Q-)/(I+, I-)$ signals, respectively. Nodes A and C of the conventional stacked-LO stage connect with nodes B and D of the compensator, respectively, and as a consequence, the component $(\pm 2i_{\rm RF}\sin(\theta))$ is cancelled. Only the $\pm 4\cos(2\omega_{\rm LO}t - \theta)i_{\rm RF}$ signal is available at the outputs. Further, for the purpose of enhancing the LO speed, the upper and lower LO stages can use the smallest transistors with a width of 2×15 μm, which is limited by air-bridge fabrication, to obtain the same high current density.

The time-delay compensated LO multiplier shown in Fig. 5 is an improved version of the first proposed one, as shown in Fig. 6 [22]. It is evident that both time-delay-compensated mixers have the identical mathematical functions. The mixer intrinsic response depends on the transistor cutoff frequency, which is determined by the current density. On the other hand, the mixer extrinsic response caused by the device capacitance is limited by the device size. The current density and device size are optimized for the improved version because the switching pairs of the lower and upper LO are identical, as shown in Fig. 5. Thus, the improved version has the advantages of higher speed, smaller size, and less power consumption.

III. Millimeter-Wave Up- and Down-Converter Designs and Measured Results

Fig. 7 shows the block diagram and frequency planning of a Ka-band system. The circuits in the shaded area are implemented in this paper. The polyphase filters needed for both transmitting and receiving are designed around 15 GHz thanks to the semi-insulating GaAs substrate. The received signal is amplified by an LNA and then sequentially down-converted to 200 MHz by the 34-GHz I/Q subharmonic mixer. The LO frequency works at only half an RF frequency for the subharmonic mixer to reduce the effects of dc offset and self-mixing. Dual conversion is employed in the transmitter chain. A quadrature IF input is first up-converted to 15 GHz by the 15-GHz SSB up-converter and subsequently up-converted to 30-GHz by a double balanced fundamental up-converter. The simple 30-GHz double balanced up-converter has equal LO and IF frequencies. Thus, the undesired sideband signal is around dc and can be eliminated by the front-end circuits and antenna [30]. The proposed frequency planning has its merit because all the mixers in Fig. 7 share the same voltage-controlled oscillator (VCO) of 15–17 GHz to reduce the complexity. In addition, the VCO operated at low frequency consumes less power than the one operated at high frequency.

As mentioned in Section II, the polyphase filter, quadrature coupler, and compensation technique have their own advantages in the up- and down-conversion mixers. In this section, all the implemented mixers adopt the two-section polyphase filter at the LO stages. The predictions of the RF output return loss of the

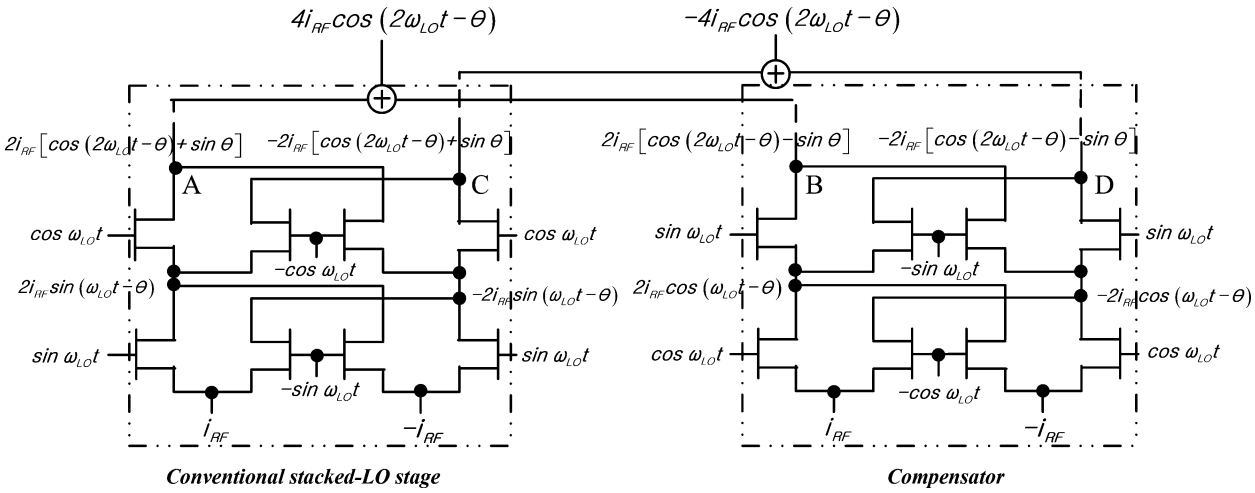

Fig. 5. Time-delay (θ) compensation analysis for the compensated stacked-LO subharmonic mixer.

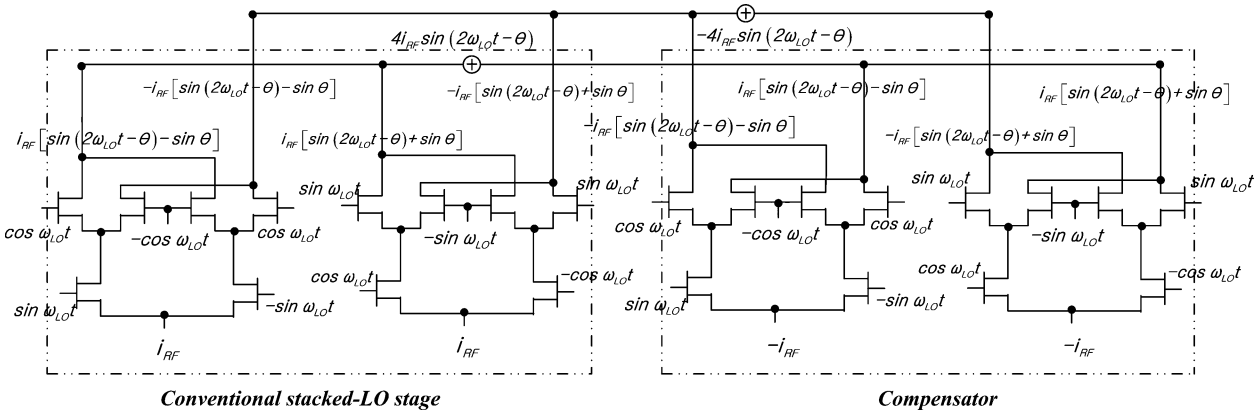

Fig. 6. Time-delay-compensated LO multipliers [22].

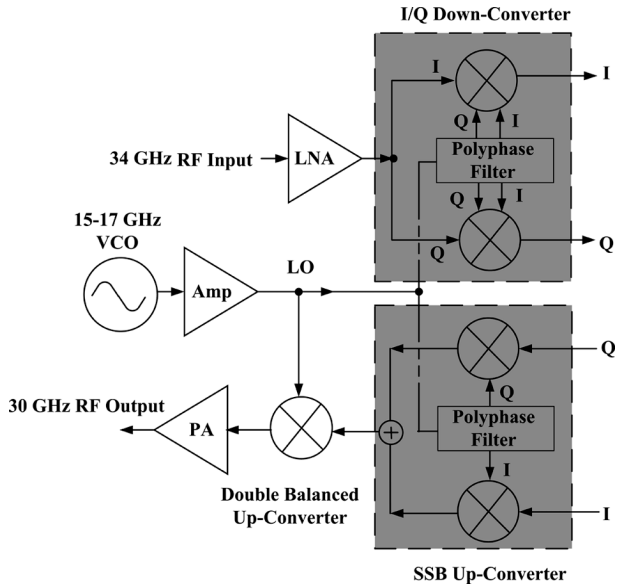

Fig. 7. Simple block diagram of a Ka-band system.

up-converter and the input RF return loss of the down-converter by simulations are accurate because precise passive components can be built on the semiinsulting GaAs substrate. A pHEMT device reaches the maximum transconductance when the fully transfer of electrons from the low-mobility donor layer to the high-mobility channel layer occurs. The gate terminal controls the 2-D electron gas (2-DEG) channel at the heterojunction interface when a more negative gate voltage is applied. The abrupt charge transfer renders the pHEMT device characteristics sensitive to the process variation and thus makes the circuit prediction from the given active device model inaccurate. Passive components and all of the high-frequency routings are simulated by an EM simulator. The distance between high-frequency routings is kept at least 25 μm to avoid line-to-line coupling effects. The symmetry in the circuit is well preserved in layouts by keeping the symmetrical paths equal length to suppress the phase mismatch. The sideband rejection in the SSB up-converter and I/Q IF waveforms in the I/Q down-converter are the best vehicles to verify the overall quadrature accuracy. 63-dB SSB rejection is achieved for the 15-GHz SSB up-converter. The leveled-LO subharmonic I/Q down-converter at 34 GHz has $<$0.4-dB magnitude and $< 1^\circ$ phase errors in the output waveform. The advantage of combination of analog and microwave circuit design methodology in HEMT technology is evident. The fabricated pHEMT mixers for high-frequency applications are measured by on-wafer testing.

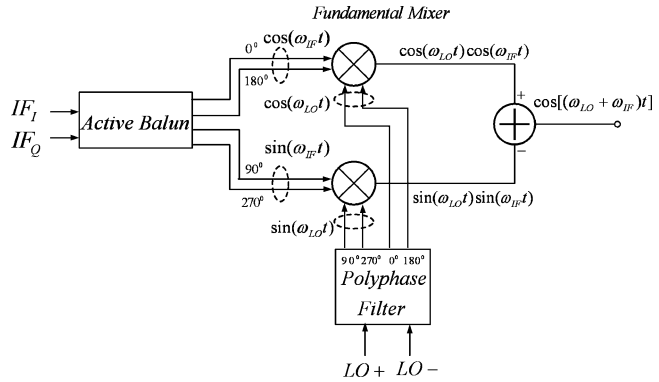

Fig. 8. Block diagram of an SSB up-converter.

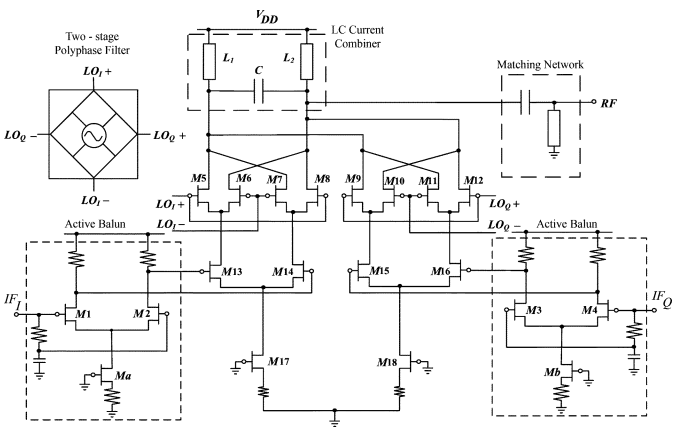

Fig. 9. Circuit topology of a 15-GHz SSB up-conversion mixer using depletion mode AlGaAs/InGaAs pHEMT technology.

A. 15-GHz Up-Conversion Mixer With 63-dB Sideband Rejection

Fig. 8 shows the functional block diagram of a double-quadrature SSB up-converter. The SSB output expression, i.e., $\cos(\omega_{\rm LO}t + \omega_{IF}t)$, is derived and explained straightforwardly in Fig. 8. Quadrature IF signals and quadrature LO signals are needed in the SSB up-converter. The SSB up-converter in Fig. 9 includes an LO polyphase filter, two fundamental analog multipliers, IF active baluns, and a current combiner with the matching network for the RF output. The two analog multipliers are two double-balanced Gilbert mixers, which are composed of Gilbert cells (M_5–M_8 and M_9–M_{12}), IF input stages (M_{13}–M_{16}) and current sources (M_{17} and M_{18}). The source resistors are used for self-biasing the current sources because only the depletion mode pHEMT devices are available. The self-biasing technique had been utilized in amplifiers [31]. The differential quadrature signals needed by the Gilbert cells are generated by applying the differential signals to the two-stage polyphase filter.

The input quadrature IF signals are transformed to the differential quadrature signals via the IF active baluns. These active baluns are employed to generate two IF signals with balanced magnitude and opposite phase. The IF active balun is intentionally designed with low gain in order to not limit the gain compression point. In addition, when compared with the passive baluns, the active baluns can save much valuable real estate in the IC technology at low IF frequencies.

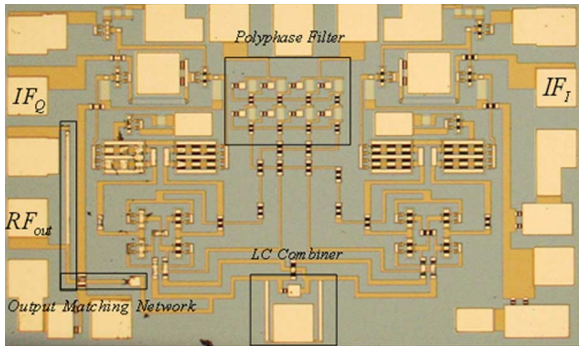

Fig. 10. Micrograph of a 15-GHz pHEMT SSB Gilbert up-converter.

Two inductors, L_1 and L_2, and a capacitor, C, form an LC passive current combiner designed at $\omega = \sqrt{1/(2L_{1,2}C)}$. The purpose of the LC current combiner is to transform the differential output of the Gilbert mixer into the single-ended output while doubling the current gain [32]. In general, the performance of a passive LC current combiner at higher frequencies is superior to an active current mirror load because an active current mirror has a limited output voltage swing and cannot respond rapidly at higher frequencies. Furthermore, a passive LC current combiner possesses higher linearity. The microstrip line inductor has a good quality factor because the GaAs-based technology owns the backside ground plane and semiinsulating substrate. On the other hand, the high-quality microstrip line inductor cannot be realized in the Si-based technology due to the lack of the backside ground plane and the lossy silicon substrate.

Fig. 10 displays the micrograph of the fabricated chip in Fig. 9. The layout is kept as symmetric as possible and the IF_I and IF_Q inputs are located on opposite sides for the sake of symmetrical considerations. A ground–signal–ground (GSG) IF_I input is on the right-hand side, a ground–signal–ground–signal–ground (GSGSG) LO pad is on the top, and an IF_Q input and RF output GSGSG pad is on the left-hand side. The chip size is 1.4×0.9 mm^2 including pads. The supply voltage and current for the mixer cores are 4.8 V and 18 mA, respectively.

When $\mathrm{IF} = 0.18$ GHz and $\mathrm{LO} = 15$ GHz, the conversion gain keeps a constant of 5 dB for LO input power from 10 to 20 dBm. The sideband rejection ratio of the SSB up-converter is shown in Fig. 11. The sideband rejection ratio is defined as the power ratio between the wanted and unwanted signals. We have achieved a 63-dB sideband rejection ratio in this study.

The simulation and measurement of the RF output return loss are shown in Fig. 12. The output return loss is determined by the LC current combiner and the output matching network because the impedance looking into the output of the commutating Gilbert mixer cell is high. The simulated curve of the RF output return loss is close to the measured curve. The RF output return loss is better than 10 dB from 12.8 to 17 GHz and 20 dB between 15.4 and 15.8 GHz. The measured conversion gain versus RF frequencies is also illustrated in Fig. 12. The experimental RF 3-dB bandwidth is about 1 GHz in the RF frequency range from 14.4 to 15.4 GHz and is limited by the LC current combiner and the associated output matching network. Meanwhile,

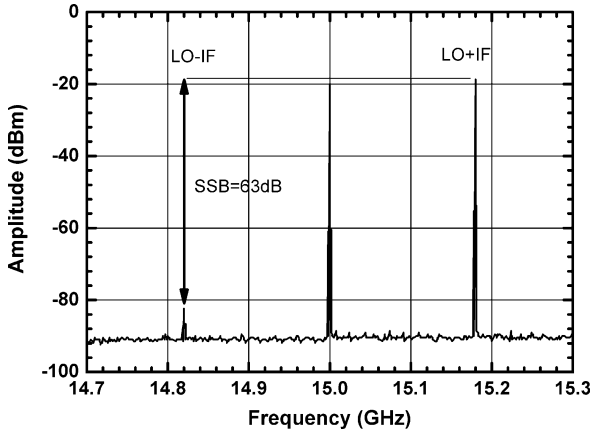

Fig. 11. SSB suppression performance of the pHEMT SSB Gilbert up-converter. 63-dB sideband rejection is achieved.

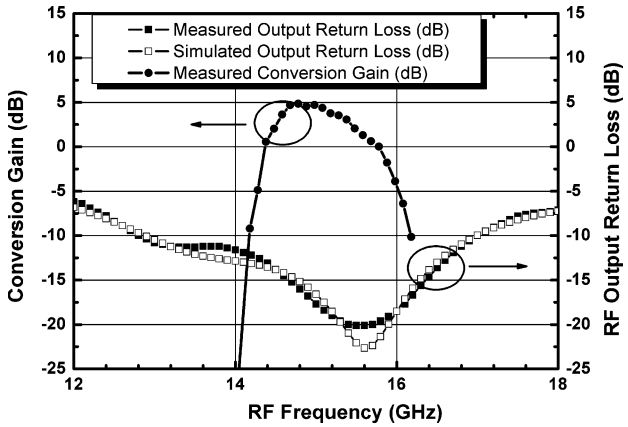

Fig. 12. Measured and simulated RF output return loss and measured conversion gain of the pHEMT SSB Gilbert up-converter.

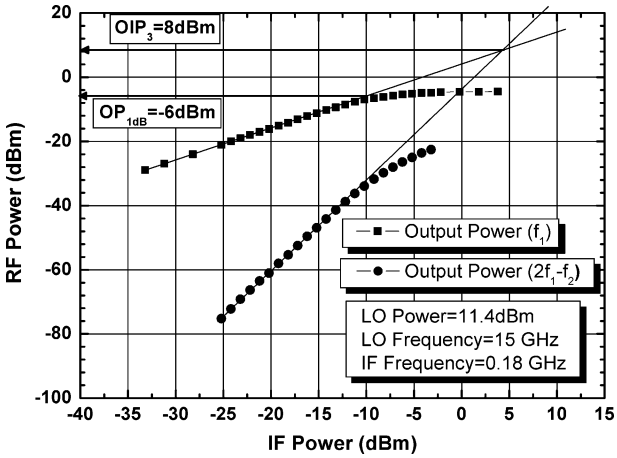

Fig. 13. Power performance of the pHEMT SSB Gilbert up-converter.

the LO-to-RF isolation is better than 31 dB for 14.7–15.2-GHz LO frequencies and the IF-to-RF isolation is above 50 dB for 0.1–0.4-GHz IF frequencies. The output power performances of an SSB up-converter are displayed in Fig. 13. The measured $\mathrm{OP}_{1\ \mathrm{dB}}$ equals -6 dBm and OIP_3 equals 8 dBm. The measured data reveal that the SSB up-converter has good linearity because the bandpass LC current combiner is utilized instead of an active low-pass current mirror.

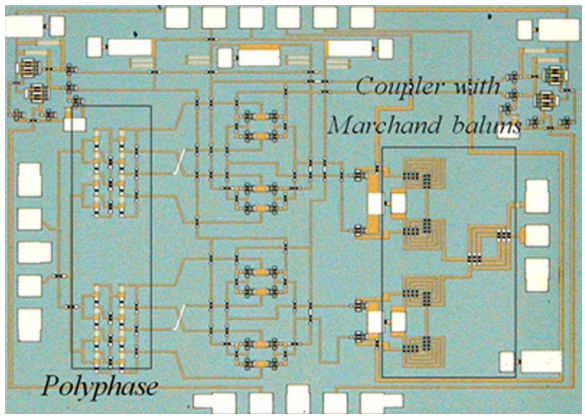

Fig. 14. Micrograph of the 34-GHz pHEMT double-quadrature subharmonic Gilbert mixer.

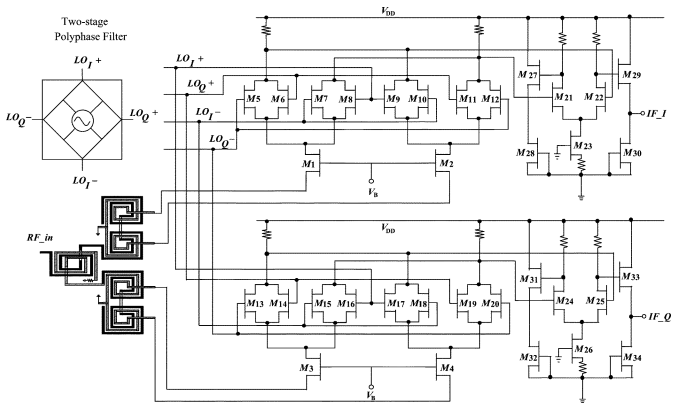

Fig. 15. Schematic of the 34-GHz I/Q subharmonic down-conversion mixer.

B. 34-GHz Double-Quadrature I/Q Subharmonic Down-Conversion Mixer

The micrograph of a 34-GHz double-quadrature I/Q subharmonic down-converter is shown in Fig. 14. The mixer utilizes an area of 2.35×1.85 mm^2. This proposed circuit of the leveled-LO I/Q subharmonic down-conversion mixer is employed with the quadrature LO and RF inputs. The quadrature LO signals and differential quadrature RF signals are generated by a two-section polyphase filter and one coupler followed by two Marchand baluns, respectively. The mixer core consists of a leveled-LO subharmonic Gilbert mixer to perform frequency translation, as shown in Fig. 15 [15]. The mixer core has 12 mA and the supply voltage is 8 V.

Fig. 16 displays the 200-MHz IF_I and IF_Q output waveforms when RF and LO input frequencies are 34.2 and 17 GHz, respectively. The measured performances have smaller than 1° phase error and 0.4-dB amplitude error limited by the measurement accuracy of $\pm 0.5^\circ$ phase and ± 0.1-dB amplitude errors. Fig. 17 shows the phase and magnitude errors as a function of frequencies and the I/Q phase error and the output mismatch from 32.5 to 34 GHz are less than 1° and 0.5 dB, respectively. The excellent I/Q performance reveals that the LO RC–CR polyphase filter, as well as the RF coupler and baluns can be implemented precisely on the semiinsulating GaAs substrate and operates well at high frequencies. The two-stage polyphase filter at the LO port has a wider balanced magnitude-and-phase bandwidth

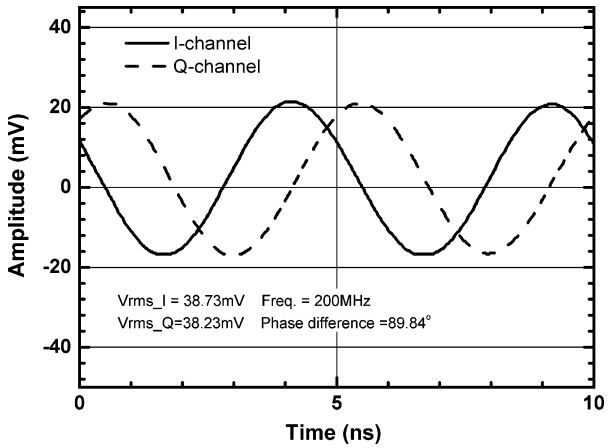

Fig. 16. IF output waveforms of the 34-GHz I/Q subharmonic down-converter.

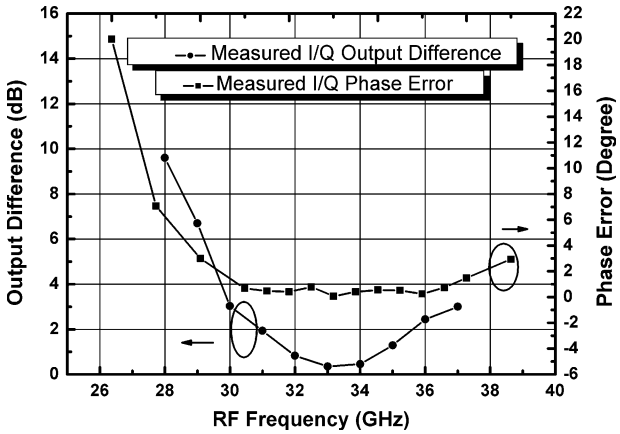

Fig. 17. Measured phase error and output difference of the 34-GHz I/Q subharmonic down-converter.

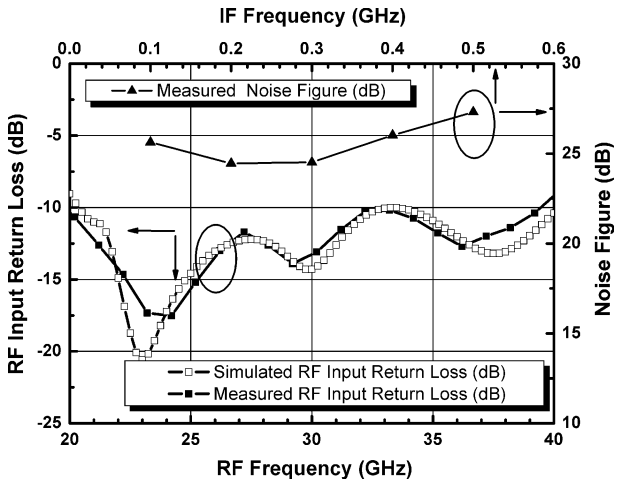

Fig. 18. Measured and simulated RF input return loss and measured NF of the 34-GHz pHEMT leveled-LO subharmonic Gilbert down-converter.

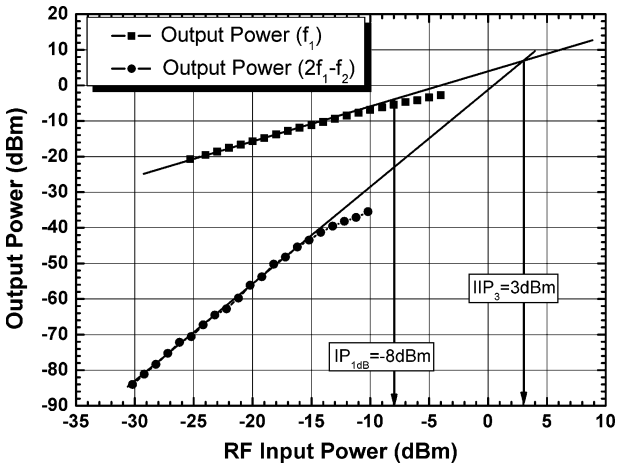

Fig. 19. Power performance of the I/Q subharmonic Gilbert down-converter.

than the coupled-line components at the RF port. The differential quadrature signal for feeding the RF port of the mixer is produced by the composite network, which consists of one quadrature coupler and two Marchand baluns. Since the Marchand balun has a wider balanced bandwidth than that of the coupler, the I/Q output difference in conversion gain is mainly affected by the quadrature coupler. The peak conversion gain reaches 4.5 dB for 14–15-dBm LO input power.

The RF input return loss is simulated and measured in Fig. 18 and the RF input return loss is better than 10 dB from 20 to 39.2 GHz. The input matching network of the subharmonic I/Q down-converter shown in Fig. 15 consists of a differential quadrature coupled-line coupler and source-port input impedance of the common-gate configuration. The common-gate input impedance is simply a reciprocal of the transconductance for the frequency up to the transistor cutoff frequency, 85 GHz in the employed pHEMT transistor. Thus, the simulated and measured data of the input return loss in the down-converter is very consistent. From 200 to 300 MHz, the measured NF is about 24.5 dB, as shown in Fig. 18. The 3-dB IF bandwidth is 500 MHz.

Fig. 19 depicts that the input 1-dB compression point $\mathrm{IP}_{1\ \mathrm{dB}}$ of the RF signal is -8 dBm, while the input third-order intercept point IIP_3 is 3 dBm. All port-to-port isolations regarding LO leakage are more than 50 dB for 15–18-GHz LO frequencies. Meanwhile, LO-to-RF and 2LO-to-RF [33] isolations exceed 60 dB. The outstanding isolations of the I/Q subharmonic down-converter prevent the self-mixing problem.

C. 40-GHz pHEMT Stacked-LO Subharmonic Gilbert Down-Conversion Mixer With Time-Delay Compensation

In order to cancel the dc offset resulting from the transistor delay, the highly symmetrical stacked-LO subharmonic Gilbert mixer is designed with a time-delay compensation technique. This structure not only improves the LO speed, but also largely reduces the amount of transistors required, as compared with previous work [22].

As shown in Fig. 20, the 20-GHz RC–CR polyphase filter is employed at the LO stage when the RF input stage is a common-gate-configured amplifier with a Marchand balun. Here, the common-gate-configured transistors provide an input impedance of 50 Ω for the Marchand balun, and hence, facilitate the input matching. The fabricated chip is shown in Fig. 21. The chip size is 2.4 mm $\times$ 1.9 mm. The microstrip lines connecting a polyphase filter with stacked-LO Gilbert cells are a critical issue, and these microstrip lines are meandered so as to remain equal in length for the phase error reduction of the

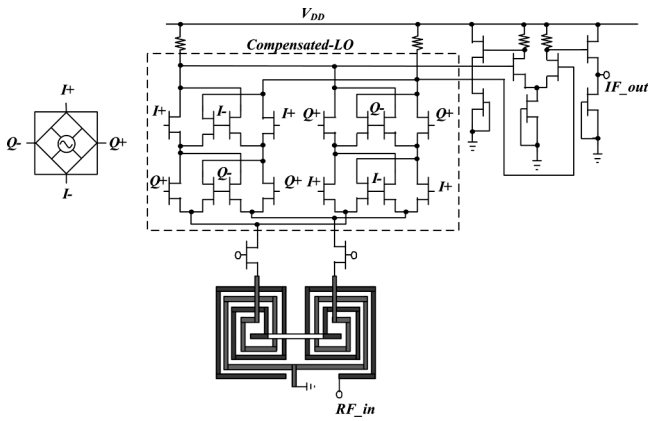

Fig. 20. Schematic of the 40-GHz pHEMT stacked-LO subharmonic Gilbert down-conversion mixer with a time-delay compensation technique.

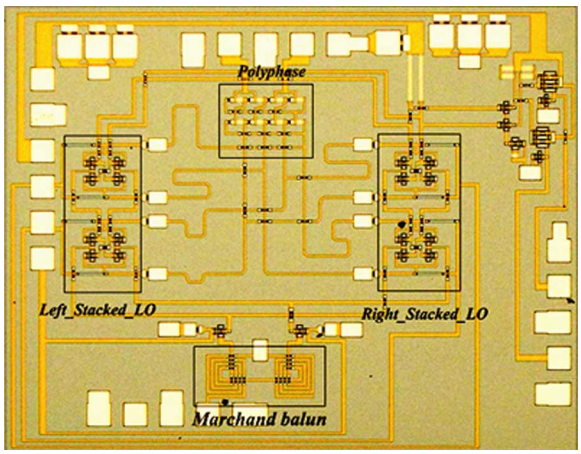

Fig. 21. Micrograph of the 40-GHz pHEMT compensated stacked-LO subharmonic Gilbert down-conversion mixer.

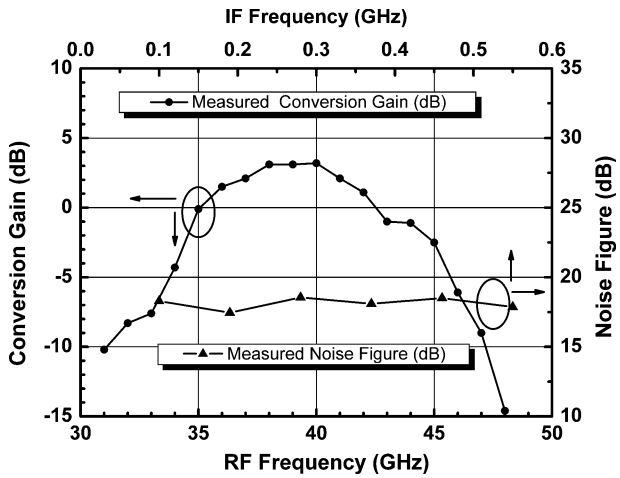

Fig. 22. Measured conversion gain and NF of the 40-GHz pHEMT stacked-LO subharmonic down-converter.

differential quadrature LO signals. The current consumption of the mixer core is 11 mA at the supply voltage of 8 V.

The maximum conversion gain of 3.1 dB is obtained from a single-ended IF output at the LO power of 10 dBm, as shown in Fig. 22. At the same time, the 3-dB RF bandwidth is about

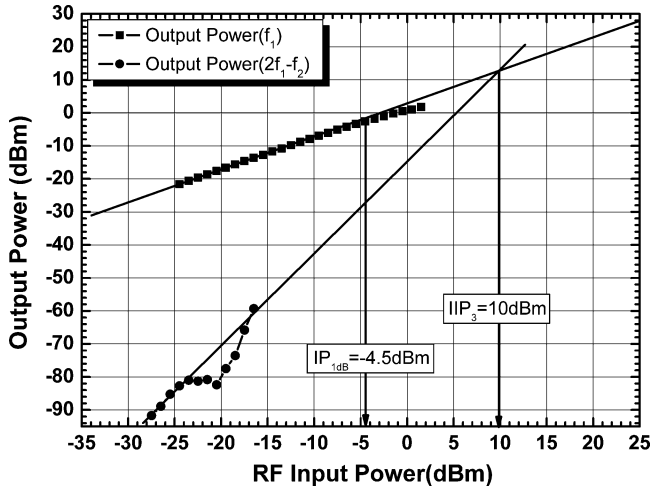

Fig. 23. Power performance of the 40-GHz compensated stacked-LO Gilbert down-converter.

4 GHz from 37 to 41 GHz. The measured NF of the 40-GHz stacked-LO subharmonic down-converter with the time-delay compensation is also shown in Fig. 22. The NF almost keeps a constant of 18 dB. The 3-dB IF bandwidth is 550 MHz. The LO-to-IF, 2LO-to-IF, LO-to-RF, and 2LO-to-RF [33] isolations are better than 30, 45, 40, and 50 dB, respectively. Further, the RF-to-IF isolation is better than 30 dB. The 1-dB gain compression occurs when the input RF power equals -4.5 dBm and the IIP_3 of 10 dBm is achieved, as shown in Fig. 23.

IV. Conclusion

The combination of analog and microwave circuit design approaches has been successfully demonstrated with Ka/Ku-band mixers using 0.15-μm AlGaAs/InGaAs pHEMT technology. The quadrature coupler based on the microwave design methodology is formidably large for operation frequencies below 30 GHz. Thus, the complex mixer can be feasible using the RC–CR polyphase differential quadrature generator. The excellent 63-dB sideband rejection ratio of the 15-GHz SSB up-conversion mixer, and the $<$ 0.4-dB magnitude and $< 1^\circ$ phase errors of the 34-GHz I/Q down-conversion mixer reveal that not only does the LO polyphase filter work accurately, but also the quadrature coupler has good quality on the semi-insulating GaAs-based substrate. Further, the novel time-delay compensator is employed at the stacked-LO subharmonic Gilbert cell to improve the current commutation speed and RF-to-IF isolation. The analog Gilbert mixer design can be further improved by employing mHEMT technology. The 0.15-μm mHEMT has an f_t of 110 GHz. On the other hand, passive mixers using the mHEMT and pHEMT technologies have the same conversion loss [12]. The results shed light on the HEMT analog circuit design approach in the millimeter-wave regime.

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