Discrete-Dopant-Induced Timing Fluctuation and Suppression in Nanoscale CMOS Circuit

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***Abstract*—As the dimensions of semiconductor devices continue to be reduced, device fluctuations have become critical to determining the accuracy of timing in circuits and systems. This brief studies the discrete-dopant-induced timing characteristic fluctuations in 16-nm-gate complementary metal–oxide–semiconductor (CMOS) circuits using a 3-D "atomistic" coupled device–circuit simulation. The accuracy of the simulation has been confirmed by using the experimentally calibrated transistor physical model. For a 16-nm-gate CMOS inverter, 3.5%, 2.4%, 18.3%, and 13.2% normalized fluctuations in the rise time, fall time, high-to-low delay time, and low-to-high delay time, respectively, are found. Random dopants may cause significant timing fluctuations in the studied circuits. Suppression approaches that are based on the circuit and device design viewpoints are implemented to examine the associated characteristic fluctuations. The use of shunted transistors in the circuit provides similar suppression to the use of a device with doubled width. However, both approaches increase the chip area. To eliminate the need to increase the chip area, channel engineering approaches (vertical and lateral) are proposed, and their effectiveness in reducing the timing fluctuation is demonstrated.**

***Index Terms*—Fluctuation suppression technique, modeling and simulation, nanometer-scale metal–oxide–semiconductor field-effect transistor (MOSFET) device and circuit, random dopant effect, timing fluctuation.**

I. Introduction

The GATE lengths of scaled metal–oxide–semiconductor field-effect transistors (MOSFETs) are under 30 nm in 45-nm-node high-performance circuits. Devices with sub-10-nm gate lengths have recently been studied. For state-of-the-art nanometer-scale (nanoscale) circuits and systems, intrinsic device parameter fluctuations that result from line-edge roughness [1], the granularity of the polysilicon gate [2], random discrete dopants [3]–[13], and other causes have substantially affected the signal system timing [10], [11] and high-frequency characteristics [12], [13]. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, fluctuations in process parameters, and other factors, are known as indispensable components of the circuit design procedure [14]–[17]. Among the aforementioned fluctuation sources, the random dopant effect is caused by the scaled device dimensions. The randomness of the dopant position and number in a device makes the fluctuation of device characteristics difficult to model and mitigate. Diverse approaches have recently been presented to investigate fluctuation-related issues in semiconductor devices [3]–[10] and circuits [10]–[13]. However, less attention has been paid to timing characteristic fluctuations of active devices caused by random dopants. Additionally, the randomness of dopant positions in devices makes the fluctuation of the gate capacitance of a device nonlinear and difficult to model using the present compact models [5]. Thus, this brief presents a large-scale statistically sound coupled device–circuit simulation approach to analyze the random dopant effect in nanoscale complementary metal–oxide–semiconductor (CMOS) circuits, concurrently capturing the fluctuations associated with the number and positions of discrete dopants. Various fluctuation suppression approaches have been proposed [6]–[9], [12], [13]. Unfortunately, the effect of such suppression techniques on transient timing fluctuations is not yet clear. To mitigate the impact of timing fluctuations on the circuit, four fluctuation suppression techniques from the circuit and device design viewpoints are proposed and implemented. Relationships between the suppression of dc and transient characteristic fluctuations are thus studied. The results of this brief elucidate the fluctuations in circuit characteristics and support the development of the next-generation of nanoelectronic circuits and systems.

This brief is organized as follows: Section II introduces the simulation technique for studying the effect of random dopants in nanoscale devices and circuits. Sections III and IV study the characteristic fluctuations and associated suppression techniques for 16-nm devices and circuits. Finally, conclusions are drawn, and future work is suggested.

II. Nano-MOSFET Circuit and Simulation

The nominal channel doping concentration of the explored device is 1.48×10^{18} cm^{-3}. They have a 16-nm gate, a gate oxide thickness of 1.2 nm, and a workfunction of 4.4 eV. The source/drain and background doping concentrations are 1.1×10^{20} and 1×10^{15} cm^{-3}, respectively. To study the effect of random fluctuations in the number and position of discrete dopants in the channel region, 758 dopants are randomly generated in an $(80\ \text{nm})^3$ cube, yielding an equivalent doping concentration of 1.48×10^{18} cm^{-3}, as shown in Fig. 1(a). The $(80\ \text{nm})^3$ cube is then partitioned into 125 subcubes of volume $(16\ \text{nm})^3$. The number of dopants varies from zero to 14, and the average number is six, as presented in Fig. 1(b), (c), and (f). These 125 subcubes are then mapped into the

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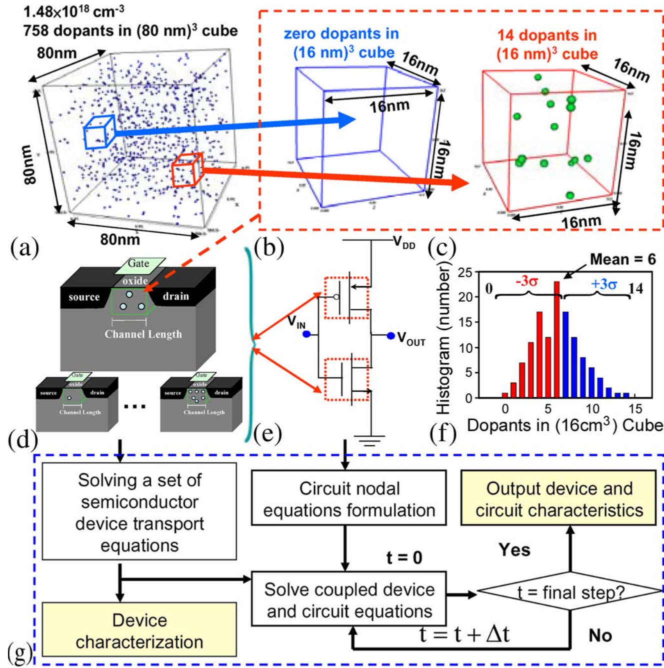


Fig. 1. (a) Discrete dopants randomly distributed in the $(80\ \text{nm})^3$ cube with the average concentration of $1.48 \times 10^{18}\ \text{cm}^{-3}$. (b)–(d) There are 758 dopants within the cube, but dopants vary from 0 to 14 (the average number is six) within its 125 subcubes of volume $(16\ \text{nm})^3$. (e) and (f) One hundred twenty-five subcubes are mapped into the channel region for dopant-position/number-sensitive device simulation and coupled device–circuit simulation. (g) Simulation flowchart for the coupled device–circuit approach.

channel region of the device for the 3-D "atomistic" device simulation, including discrete dopants, as shown in Fig. 1(d). The device is simulated by solving a set of 3-D density-gradient equations coupled with the Poisson equation and electron–hole current continuity equations [18]. In the "atomistic" device simulation, the resolution of individual charges within a conventional drift–diffusion simulation using a fine mesh creates problems associated with singularities in the Coulomb potential [3]. Thus, the density-gradient approximation is used to handle discrete charges by properly introducing the related quantum mechanical effects [18]. The inverter circuit, as displayed in Fig. 1(e), is used as a tested circuit to study the fluctuation of timing characteristics. Similarly, 125 cases of PMOSFETs with discrete dopants are generated according to Fig. 1(a)–(d). Then, 125 pairs of NMOSFETs and PMOSFETs are randomly selected and used to study the circuit characteristic fluctuations. To fairly compare the NMOSFET- and PMOSFET-induced characteristic fluctuations and eliminate the effect of the transistor size on the fluctuation, the dimensions of the PMOSFET were the same as those of the NMOSFET, and the absolute value of the nominal threshold voltages for both the NMOSFET and PMOSFET were both 140 mV. All statistically generated devices and circuits with discrete dopants, as shown in Fig. 1, are incorporated into the large-scale 3-D coupled device–circuit simulation, which is performed using a parallel computing system [19]. In estimating circuit characteristics, since no well-established compact model of ultrasmall nanoscale devices is available, to capture the discrete-dopant-position-induced fluctuations, a device–circuit coupled simulation approach [20] is employed, as shown in Fig. 1(g). The characteristics of the devices of the test circuit are first estimated by solving the device transport equations. The obtained result is then used as initial guesses in the coupled device–circuit simulation. The nodal equations of the test circuit are formulated and then directly coupled to the device transport equations (in the form of a large matrix that contains both circuit and device equations), which are simultaneously solved to obtain the circuit characteristics. The device characteristics, such as distributions of potential and current density, obtained by device simulation are input in the circuit simulation through device contacts. The effect of discrete dopants in the transistor on circuit characteristics is thus properly estimated. The characteristic fluctuation of the device was validated with reference to the experimentally measured data [7] to ensure the best accuracy.

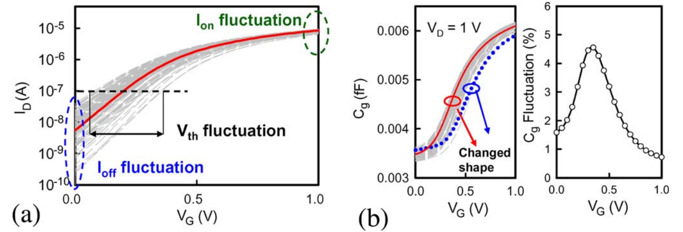
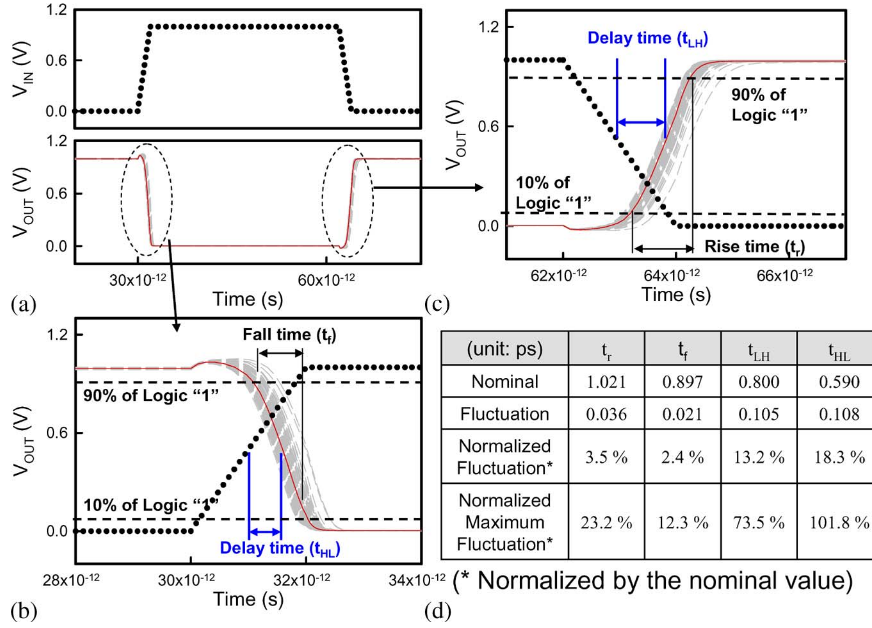
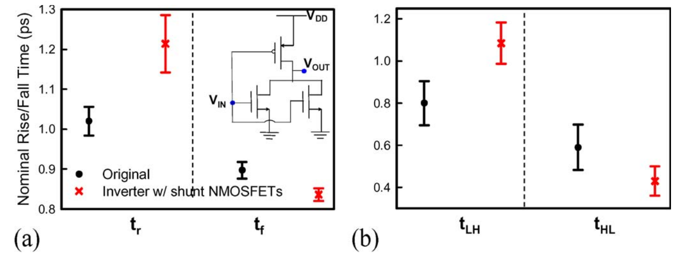


Fig. 2. (a) $I_D - V_G$ and (b) $C - V$ curves for the studied 16-nm-gate transistors with discrete dopant fluctuations.

III. Intrinsic Device and Circuit Fluctuations in Nanoscale MOSFETs

Fig. 2(a) plots the $I_D - V_G$ characteristics of 16-nm planar NMOSFETs with discrete dopant fluctuations; the solid line represents the nominal case (continuously doped channel with a doping concentration of $1.48 \times 10^{18}\ \text{cm}^{-3}$), and the dashed lines are random-dopant-fluctuated devices. For the device with between 0 and 14 discrete dopants, the threshold voltage fluctuation σV_{th} is about 58.5 mV, which may resulted in 7.9% and 54.5% fluctuations in ON- and OFF-state currents, respectively. Fig. 2(b) plots the capacitance–voltage $(C - V)$ characteristics of the studied transistors. The $C - V$ curves are horizontally shifted due to the variation of the effective channel doping concentration, which may be described using the corresponding V_{th} parameters in a compact model. Additionally, the shape of the curves is changed due to the randomness of the dopant position in the channel, which affects the shape of the depletion region [5]. To the best of the authors' knowledge, the fluctuation in the gate capacitance C_g has not yet been modeled, and a coupled device–circuit simulation must be performed to estimate it. The normalized C_g fluctuation is then calculated as a function of the gate bias, and the normalized maximum variation of C_g is about 18.9%. The discrete dopant effect not only causes fluctuations in V_{th} and current but also affects the gate capacitance of the transistor. Therefore, the transistor's intrinsic gate capacitance is used as a load capacitance herein, and the intrinsic timing fluctuations that are induced by discrete dopants are focused. Fig. 3 plots the input and output transition characteristics for the inverter circuit. Fig. 3(a) presents the input and output signals; the solid line represents the nominal case (continuously doped channel with a channel doping concentration of $1.48 \times 10^{18}\ \text{cm}^{-3}$), and the dashed lines represent cases with discrete dopant fluctuations. The rise time t_r, fall time t_f, and hold time of the input signal are 2, 2, and 30 ps, respectively. Fig. 3(b) and (c) displays the zoom-in plots of the





(unit: ps)	t_r	t_f	t_{LH}	t_{HL}
Nominal	1.021	0.897	0.800	0.590
Fluctuation	0.036	0.021	0.105	0.108
Normalized Fluctuation*	3.5 %	2.4 %	13.2 %	18.3 %
Normalized Maximum Fluctuation*	23.2 %	12.3 %	73.5 %	101.8 %

(* Normalized by the nominal value)

(d)

Fig. 3. (a) Input and output signals for the studied discrete-dopant-fluctuated 16-nm-gate inverter circuit. Zoom-in plots of the (b) fall and (c) rise transitions. (d) Summarized timing fluctuations in the 16-nm-gate inverter circuit.

falling and rising transitions, respectively. The term t_r is the time required for the output voltage $V_{\rm OUT}$ to rise from 10% of the logic "1" level to 90% of the same level, and t_f denotes the time required for the output voltage to fall from 90% of the logic "1" level to 10% of the same level. The low-to-high delay time $t_{\rm LH}$ and high-to-low delay time $t_{\rm HL}$ are defined as the difference between the times of the 50% points of the input and output signals during the rising and falling of the output signal, respectively. Fig. 3(d) plots the normalized timing characteristic fluctuations (the standard deviation/nominal value $\times$ 100%). For the 16-nm-gate CMOS inverter, as the number of discrete dopants varies from 0 to 14, normalized fluctuations of t_r, t_f, $t_{\rm HL}$, and $t_{\rm LH}$, of 3.5%, 2.4%, 18.3%, and 13.2%, respectively, may occur. The delay time fluctuations dominate the timing characteristics. The normalized maximum fluctuations (the maximum variation of time/nominal value $\times$ 100%) of the high-to-low and low-to-high delay times are about 101.8% and 73.5%, respectively. Notably, the maximum and minimum delays associated with this specific set of 125 randomized channels would vary such that their range would increase as the number of samples increased. For the high-to-low signal transition of the output signal, the delay time is dominated by the starting points of the signal transition and then controlled by the ON/OFF state of the NMOSFETs in the inverter circuit. Therefore, the fluctuation of the threshold voltage of NMOSFETs substantially affects the high-to-low delay time characteristic. Similarly, the low-to-high delay time fluctuation is strongly influenced by the $\sigma V_{\rm th}$ of PMOSFETs. $\sigma t_{\rm HL}$ exceeds $\sigma t_{\rm LH}$ because the $\sigma V_{\rm th}$ of NMOSFETs exceeds that of PMOSFETs. The $\sigma V_{\rm th}$ of NMOSFETs is larger because the majority carriers of NMOSFETs have a smaller effective mass and, thus, exhibit a larger mobility fluctuation than those of PMOSFETs. The rise/fall time fluctuations depend on the charge/discharge capability of the PMOSFETs/NMOSFETs. Therefore, σt_r exceeds σt_f because the driving capability of PMOSFETs is weaker than that of NMOSFETs in the given device dimensions scenario. The device with larger driving capability requires less time to charge and discharge a given load capacitance and, thus, exhibits less fall time fluctuations. The rise and fall time fluctuations, in general, may not be as important as the delay time fluctuation in circuit timing; however, their maximum variations can exceed 0.237 and 0.110 ps, respectively, which exceed the delay time fluctuation and should therefore be considered in statistical timing analysis in circuit and system design. Moreover, fluctuations in the rise and fall times can be added to the delay time, thus increasing the delay time fluctuations.

Fig. 4. (a) Rise/fall time and (b) low-to-high and high-to-low delay times for the studied discrete-dopant-fluctuated 16-nm-gate inverter circuit, where the inset shows the inverter with shunted NMOSFETs for mitigating the timing fluctuations induced by NMOSFETs.

IV. FLUCTUATION SUPPRESSION TECHNIQUES

In the study of fluctuation suppression techniques, since $\sigma t_{\rm HL}$ is a dominating factor in timing fluctuations and the PMOSFET is used as the control, the fluctuation suppression techniques are only applied to NMOSFETs.

A. Circuit-Level Suppression

From the circuit design viewpoint, an inverter with shunted NMOSFETs is proposed to mitigate the fluctuations in the timing characteristics that are induced by NMOSFETs, as shown in the inset of Fig. 4(a). Fig. 4(a) compares t_r and t_f for the original inverter and the shunted NMOSFETs inverter

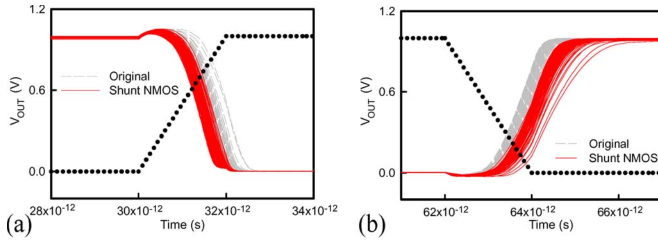


Fig. 5. Comparison of the (a) high-to-low and (b) low-to-high delay times for the (dashed lines) original inverter circuit and (solid lines) inverter circuit with shunted NMOSFETs.

circuits. Since the number of NMOSFETs used to discharge the load capacitance is increased with respect to the original inverter, the nominal value and the fluctuations of the fall time are reduced. However, the increased number of transistors increased the load capacitance and the number of fluctuation sources, affecting the rise time and its fluctuations. Fig. 4(b) compares $t_{\rm LH}$, $t_{\rm HL}$, and their fluctuations. $t_{\rm HL}$, $\sigma t_{\rm HL}$, and $\sigma t_{\rm HL}$ are reduced in the shunted NMOSFETs inverter circuits. Fig. 5(a) and (b) compares the high-to-low and low-to-high transitions for the original inverter and the shunted NMOSFETs inverter circuits, respectively. Since the high-to-low transition begins when one of the NMOSFETs is turned on, the $t_{\rm HL}$ and $\sigma t_{\rm HL}$ of the shunted NMOSFETs inverter are smaller than the original inverter because the shunted NMOSFETs inverter has a higher probability of having a low $V_{\rm th}$ NMOSFET than the original inverter. The $t_{\rm HL}$ of the inverter is possibly reduced with a low $V_{\rm th}$ NMOSFET shunted. The range of spread of $t_{\rm HL}$ is therefore reduced. Similarly, in a low-to-high transition, since the driving capability of PMOSFETs is lower than that of NMOSFETs, the rise transition starts when both of the shunted NMOSFETs are turned off. The $t_{\rm LH}$ of the inverter is possibly to be increased with a high $V_{\rm th}$ NMOSFET shunted, and therefore, the range of spread of $t_{\rm LH}$ is reduced. However, since the probability that the inverters with low $V_{\rm th}$ NMOSFETs is reduced, $t_{\rm LH}$ is significantly increased, as shown in Fig. 4(b). From the device design viewpoint, the inverter with the shunted transistors can be implemented by designing NMOSFETs with a double device width. The following simple analytical expression reveals that a device with large dimensions has a small threshold voltage fluctuation [6]:

$$\sigma V_{\rm th} = 3.19 \times 10^{-8} \frac{t_{\rm ox} N_A^{0.401}}{\sqrt{WL}} \ [\rm V] \tag{1}$$

where $t_{\rm ox}$ is the thickness of gate oxide; W and L are the width and length of the transistor, respectively. To compare the device characteristics on a fair basis, the nominal threshold voltages for devices with doubled width are calibrated to 140 mV. Fig. 6(a) and (b) displays the normalized rise/fall time and delay time for the original inverter, the inverter with the shunted NMOSFETs, and inverter with doubled NMOSFET width. As expected, the timing characteristics of the inverter with doubled NMOSFET width are similar to that of the inverter with the shunted NMOSFETs. The high-to-low timing characteristics of the inverter with doubled NMOSFET width are improved at the cost of a worse low-to-high signal transition. Notably, both approaches [i.e., (B) and (C)] may increase the short-circuit leakage power and chip area, potentially limiting the use of these fluctuation suppression techniques.

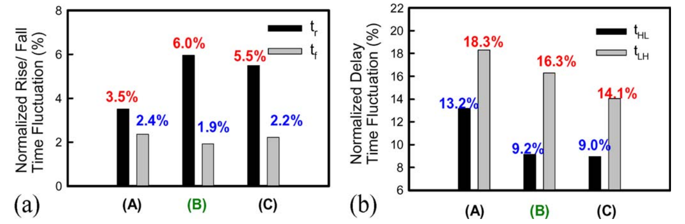


Fig. 6. Normalized (a) rise/fall time and (b) delay time for the (A) original inverter, (B) inverter with the shunted NMOSFETs, and (C) inverter with doubled NMOSFET width.

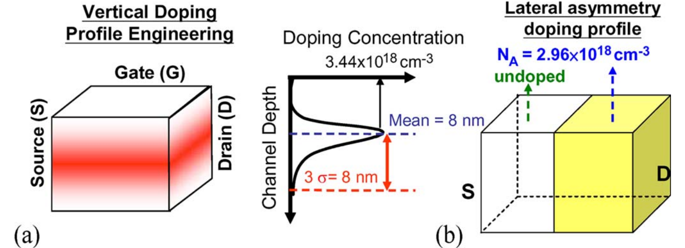


Fig. 7. Proposed (a) vertical doping profile engineering and (b) lateral asymmetry doping profile to suppress random dopant fluctuations.

B. *Device-Level Suppression*

To prevent the increase of the chip area, two channel engineering approaches (the vertical doping profile engineering and the lateral asymmetry doping profile, as shown in Fig. 7(a) and (b), respectively) are proposed to reduce the device and circuit characteristic fluctuations. As in the original doping profile, the numbers of channel dopants in the vertical doping profile engineering and the lateral asymmetry doping profile vary from 0 to 14; the average in each case is six. Similarly, to compare the device characteristics on a fair basis, the nominal threshold voltages of devices with channel engineering are calibrated to 140 mV, which is the same nominal threshold voltage as in the original cases. Notably, the effect of channel engineering approaches cannot be predicted by (1), and therefore, the coupled device–circuit simulation approach is adopted to examine their effectiveness. For the vertical doping profile engineering, the doping profile from the device surface to the substrate follows the normal distribution. The characteristic fluctuation is suppressed because fewer fluctuation sources (i.e., the discrete dopants) are located closer to the current-conducting path. In the lateral asymmetry doping profile, unlike the profiles of conventional lateral asymmetry devices with higher channel doping concentrations nearer the source end of the channel region, the channel doping concentration is higher when the dopants are nearer the drain end of the channel region. Dopants at the source end of the channel may induce a larger current fluctuation than they do at the drain end of the channel. Moreover, in the proposed lateral asymmetry doping profile, since most of the dopants are located near the drain end of the channel, the gate-to-drain capacitance C_{gd} fluctuation becomes the major source of the gate capacitance fluctuation. The gate-to-drain capacitance and its fluctuation are significantly suppressed with the increasing drain bias due to the increased depletion width close to the drain end of the channel region.

Table I summarizes the improvement of the timing characteristic fluctuations and nominal timing characteristics associated with the fluctuation suppression techniques from the

TABLE I
COMPARISON OF THE TIMING CHARACTERISTICS FOR FLUCTUATION AND NOMINAL TIMING CHARACTERISTICS AMONG SUPPRESSION TECHNIQUES
(Fluctuation $= ((t_{\text{original}} - t_{\text{suppressed}})/t_{\text{original}}) \times 100\%$)

	Circuit Design Viewpoint (A)	Device Design Viewpoint		
		(B)	(C)	(D)
Increment / decrement of the nominal timing characteristic				
t_f	-6.86%	-4.56%	~0.0%	-1.29%
t_r	+18.84%	+20.25%	~0.0%	+1.42%
t_{HL}	-26.66%	-20.70%	~0.0%	-5.23%
t_{LH}	+35.53%	+37.23%	~0.0%	-0.36%
Timing characteristic fluctuations				
σt_{f*}	23.61%	9.88%	7.74%	8.47%
σt_r	-101.97%	-88.36%	11.32%	1.53%
σt_{HL}	34.76%	39.17%	18.42%	46.59%
σt_{LH}	5.79%	6.76%	0.52%	1.71%
Area cost	25%	~20%	0	0

circuit (A: inverter with shunted NMOSFETs) and the device design viewpoints (B: inverter with doubled NMOSFET width; C: inverter with vertical doping profile engineering; and D: inverter with the lateral asymmetry doping profile). The "+" and "−" signs in the nominal timing characteristic indicate the increase and decrease of the corresponding timing characteristics, respectively. The "−" sign in the timing characteristic fluctuations represents the degradation of the corresponding timing characteristics. To improve high-to-low transition characteristics and reduce high-to-low timing fluctuations, the use of shunted NMOSFETs (A) and an increase in NMOSFET width (B) can be considered at the cost of worse low-to-high transition characteristics and increased chip area and power. In reducing delay time fluctuations, the lateral asymmetry doping profile (D) is the most effective. However, a large short-channel effect of the device and the consumption of leakage power should be considered. Without scarifying the chip area and device performance, vertical doping profile engineering (C) is effective for low-power applications.

V. CONCLUSION

In this brief, a 3-D "atomistic" coupled device–circuit simulation approach has been adopted to investigate the random-dopant-induced timing characteristic fluctuations in nanoscale CMOS inverter circuits, concurrently capturing the discrete-dopant-number- and discrete-dopant-position-induced fluctuations. The experimentally calibrated simulation technique predicted that the discrete-dopant-fluctuated 16-nm CMOS inverter circuit may exhibit 3.5%, 2.4%, 18.3%, and 13.2% normalized fluctuations in the rise time, fall time, high-to-low delay time, and low-to-high delay time, respectively. To suppress the discrete-dopant-induced timing fluctuations, four suppression techniques from the circuit and device design viewpoints have been examined. This brief provides an insight into random-dopant-induced timing characteristic fluctuations, which may benefit the development of state-of-the-art digital circuits with robust timing characteristics. This approach can further be used to study the intrinsic parameter fluctuations in various digital, analog/RF, and memory circuits.

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