Effects of Minority-Carrier Response Behavior on Ge MOS Capacitor Characteristics: Experimental Measurements and Theoretical Simulations

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***Abstract*—In this paper, we present MEDICI simulations of the admittance-voltage properties of Ge and Si MOS devices, including analyses of substrate conductance G_{sub} and high–low transition frequency f_{tran}, to explore the differences in the minority-carrier response. The Arrhenius-dependent G_{sub} characteristics revealed that a larger energy loss—by at least four orders of magnitude—occurs in Ge than in Si, reflecting the fast minority-carrier response rate, i.e., a higher value of f_{tran}. We confirmed that the higher intrinsic carrier concentration in Ge, through the generation/recombination of midgap trap levels as well as the diffusion mechanism, resulted in the onset of low-frequency C–V curves in the kilohertz regime, accompanying the gate-independent inversion conductance. The experimental data obtained from Al_2O_3/Ge MOS capacitors were consistent with the values of G_{sub} and f_{tran} obtained from MEDICI predictions and theoretical calculations. In addition, upon increasing the inversion biases, we observed shifts in the G_{sub}/f conductance peaks to low frequencies that mainly arose from the transition of minority carriers with bulk traps in the depletion layer. Meanwhile, we estimated that the bulky defects of ca. $(2-4) \times 10^{15}$ cm^{-3} exist in present-day low-doped Ge wafers.**

***Index Terms*—Bulk trap, germanium (Ge), MEDICI simulation, minority-carrier response, MOS capacitor, substrate conductance.**

I. Introduction

VARIOUS high-k gate dielectrics, substrate materials, and device structures have been proposed to relieve the enormous scaling burden required to improve transistor performance. High-k/Ge structure-based devices are considered new potential candidates to replace conventional Si MOSFETs for high-performance logic devices because of their high intrinsic carrier mobility. Much effort has been devoted to improve the high-k/Ge interface and junction leakage characteristics through both surface passivation [1]–[3] and process modification [4], [5]; several promising results have recently been demonstrated [6]–[8]. Interestingly, an uncommon electrical characteristic—the fast minority-carrier response—has been manifested during electrical measurements of Ge MOS capacitors; its variation with respect to the interface state response is also a noteworthy issue that requires clarification. In fact, many years ago, Nicollian and Brews [9] foresaw that it would be possible to observe an LF C–V curve for a narrow-gap material, such as Ge, at the standard HF used for traditional Si because of the higher intrinsic carrier concentration n_i. Such minority-carrier characteristics for capacitors deposited on Si substrates have been established and correlated to the effects of the temperature, doping concentration, and impurity contamination; however, similar studies using Ge substrates remain rare [10]–[12]. The influences of the doping concentration and the substrate type on this anomalous C–V behavior have been discovered in high-k/Ge MOS capacitors [13], [14]; the fundamental mechanisms were clarified through fitting of MOS-equivalent circuit models [10], [11] and measurements of Arrhenius-dependent conductance properties [12], respectively. In this paper, we utilized a 2-D MEDICI numerical simulator, accompanied by theoretical calculations, to comprehensively investigate the minority-carrier response—as functions of the doping concentration, measured frequency, and temperature—in terms of the electrical properties of Ge and Si MOS capacitors. We have also examined the underlying mechanistic differences through practical admittance measurements of atomic-layer-deposited (ALD) Al_2O_3 thin films on both types of Ge substrates.

Manuscript received August 26, 2008; revised December 4, 2008. First published March 16, 2009; current version published April 22, 2009. This work was supported by the National Science Council of the Republic of China (Contract NSC94-2215-E009-066). The review of this paper was arranged by Editor H. S. Momose.

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Digital Object Identifier 10.1109/TED.2009.2016020

II. MEDICI Simulation and Experimental Procedures

A. MEDICI Simulation Program

The computer simulation program MEDICI has been employed to predict the semiconductor device properties of several electronic structures, including HEMTs [15], MOSFETs [16],

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silicon oxide high-k oxide silicon [17], photodetectors [18], and junction diodes [19]. By self-consistently solving the Poisson equation and the continuity equations in MEDICI, we can simulate the admittance properties of MOS structures containing SiO_2 (30 Å) and Al gates to examine the minority-carrier characteristics in Si and Ge. In addition, MEDICI makes it possible to perform simulations at relatively high frequencies and low temperatures by providing the appropriate physical models and parameters. Most importantly, the contributions of the interface states to both the capacitance and conductance loss at depletion can be omitted, which is beneficial to the analysis of admittance-voltage data in the inversion region. Apart from a large difference in the value of the energy bandgap for these two substrates, both carrier lifetime and mobility, which are dependent on the carrier concentration and the temperature, are critical in determining the minority-carrier generation behavior. Moreover, the bulk trap level at midgap was assumed for both substrates.

B. Fabrication of the MIS Capacitor

We prepared p- and n-type Ge wafers that were doped with Ga and Sb dopants at levels of ca. 2×10^{15} and ca. 1×10^{14} cm^{-3}, respectively. The Si wafer, having a standard doping concentration of ca. 1×10^{16} cm^{-3}, was also studied for comparison. All wafers were precleaned through a cyclic rinse with dilute hydrofluoric acid and deionized water. The Al_2O_3 high-k layer was deposited using the ALD system at a substrate temperature of 100 °C; the physical thickness was ca. $64(\pm 2)$ Å according to the established growth rate of ca. 1.06 Å/cycle. Trimethylaluminum $[Al(CH_3)_3]$ and H_2O were chosen as the metal source and oxidant, respectively; they were alternatively pulsed into the reactor for 1 s per pulse separated by a N_2 purge of 10 s to remove the redundant reactants. The top capacitor electrode was formed via a shadow mask by depositing electron-beam Pt at a film thickness of ca. 700 Å(area, ca. 4×10^{-4} cm^2), whereas the backside contact was made through the thermal evaporation of Al. Finally, the entire MOS structure underwent forming gas annealing (N_2/H_2, 90:10) at 300 °C for 30 min. The admittance-voltage characteristics were measured in the parallel mode using HP4284, and then they were corrected by excluding the series resistance and parasitic components. The temperature- and frequency-dependent electrical curves in depletion and weak inversion were investigated to explore the latent minority-carrier mechanism.

III. Results and Discussion

Figs. 1 and 2 present the simulated C–V and G–V characteristics of Al/SiO_2 gate stacks on p-Si and p-Ge substrates at various temperatures, respectively. It was observed that the dielectric on Si [Fig. 1(a)] obviously presented the LF C–V curves only when raising the temperature up to 400 K and reducing the frequency to as low as 100 Hz. In contrast, such LF curves readily occurred at 300 K for Ge systems in which the doping concentrations were 10^{16} and 10^{14} cm^{-3} [Fig. 1(b) and (c), respectively]. We observed the minority-carrier behavior even at higher frequencies, e.g., 1 MHz, in the low-doped Ge. On the contrary, the complete HF C–V curves appeared only in the high-doped Ge at temperatures as low as 250 K. By examining the simulated conductance $G_{\rm mea}$ in the Si case [Fig. 2(a)], the inversion conductance $G_{\rm inv}$ revealed frequency independence up to 100 kHz; the values increased by about two orders of magnitude as we increased the temperature from 300 to 400 K. From Fig. 2(b) and (c), the Ge counterpart reveals two distinct features: The $G_{\rm inv}$ characteristics measured at low temperature (250 K) were identical to those in Si at high temperature (400 K); upon increasing the temperature to 350 K, the value of $G_{\rm inv}$ became proportional to the square of the angular frequency ω, which is similar to the curves observed in accumulation. The resultant w^2 dependence of G–V curves implied similar equivalent operation circuits in both accumulation and inversion for Ge MOS capacitors at higher temperatures, e.g., $>$ 300 K. In general, the electrical differences in inversion between Ge and Si are dependent on the dominance of either the $G_{\rm inv}$ or $wC_{\rm inv}$ term, which are further correlated to the measured temperature, frequency, and properties of the substrate material. We will understand the minority-carrier conductance loss through the theoretical calculations of these two components, together with the following experimental findings. Note that the absence of interface states was assumed in simulation; hence, they did not contribute to the energy loss, thereby causing the onset of a deeper "dip" in depletion.

Figs. 3 and 4 display the measured C–V and G–V characteristics of Pt/ALD-Al_2O_3 gate stacks deposited on p-Ge and n-Ge substrates, respectively. First, as illustrated in Figs. 3(a)–(c) and 4(a)–(c), the minority-carrier response occurred in C–V inversion for both types of Ge. The low-doped (10^{14} cm^{-3}) n-Ge exhibited a relatively faster rate with respect to p-Ge (2×10^{15} cm^{-3}), which we attribute to the resultant high-minority-carrier concentration. Moreover, Figs. 3(d)–(f) and 4(d)–(f) display the gate-bias-independent values of $G_{\rm inv}$ in Ge with more severe frequency dispersion upon increasing the measured temperature, unlike the exponential decline of the conductance curves in inversion for Si MOS capacitors (not shown here).

From the equivalent circuit model [20], the simulated values of $G_{\rm sub}$ in inversion, i.e., $G_{\rm inv}$, are the parallel combination of generation/recombination conductance $G_{\rm gr}$ and diffusion conductance $G_{\rm diff}$, where $G_{\rm gr}$ is due to the finite g–r within the depletion layer through the bulk traps, and $G_{\rm diff}$ is due to the diffusion current of the minority carriers from the bulk to the edge of the depletion region. At lower temperatures, $G_{\rm gr}$ is more significant [9], [20] and can be expressed using the equation

$$\frac{G_{\rm gr}}{A} = \frac{q}{\phi_S} \frac{n_i}{1} \frac{w}{\tau_T} \tag{1}$$

where ϕ_S and w are the surface potential and depletion layer width in inversion, respectively, and τ_T is the Shockley–Read–Hall lifetime determined by the density of g–r centers and the capture coefficients for electrons and holes, respectively. As the temperature further increases, $G_{\rm diff}$ becomes

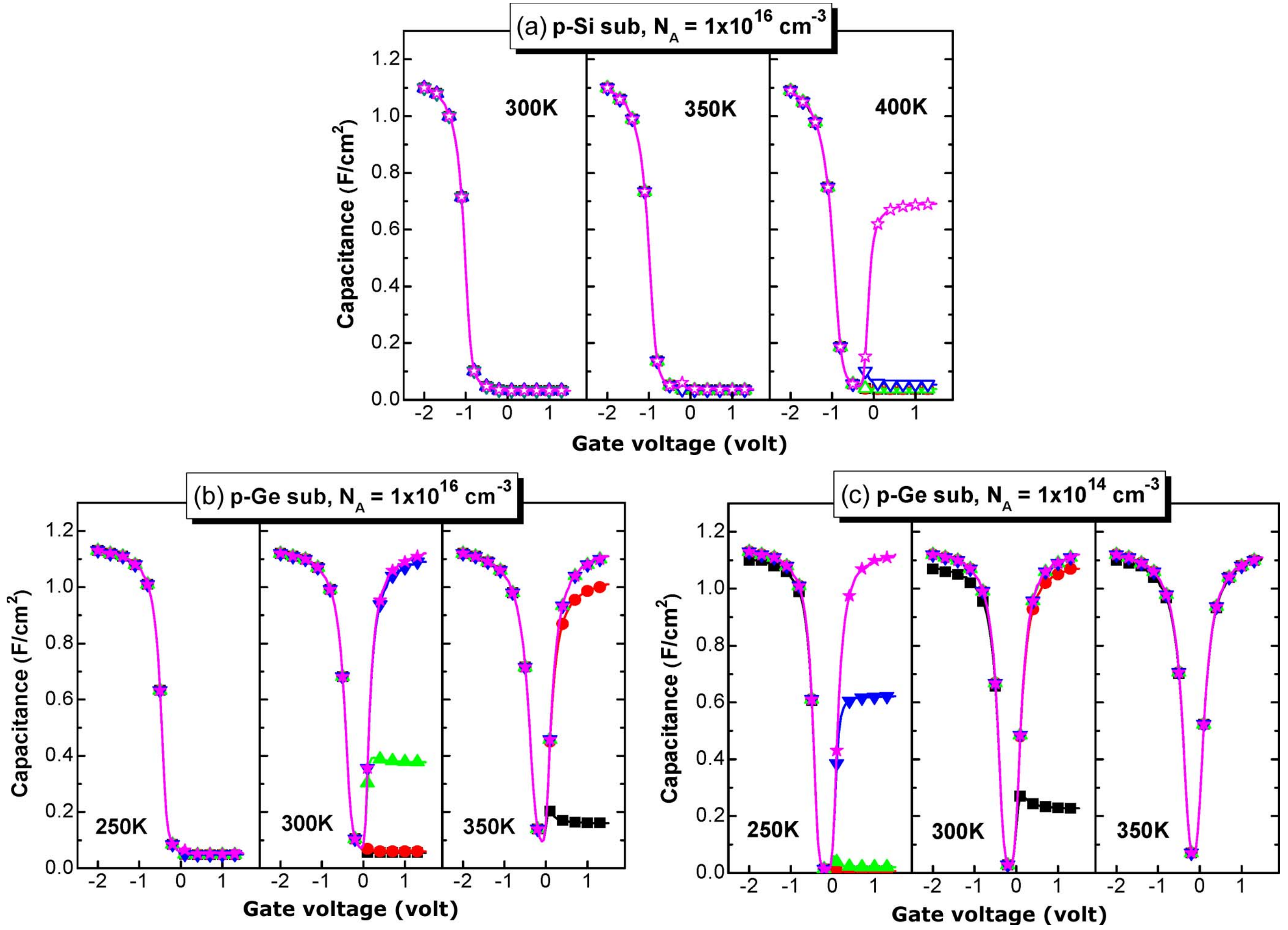

Fig. 1. MEDICI-simulated C–V curves of Al/SiO_2 gate stacks on Si and Ge substrates under measured temperatures ranging from 250 to 400 K. (a) p-Si, 10^{16} cm^{-3}. (b) p-Ge, 10^{16} cm^{-3}. (c) p-Ge, 10^{14} cm^{-3}. Note that the measured frequencies are labeled by solid symbols: square (1 MHz), circle (100 kHz), up-triangle (10 kHz), down-triangle (1 kHz), and star (100 Hz).

dominant because of the increasing function of n_i^2 [9], [20], as revealed by the following equation:

$$\frac{G_{\mathrm{diff}}}{A} = \frac{q^2}{kT}\frac{n_i^2}{N_{\mathrm{maj}}}\frac{L_{\mathrm{mir}}}{\tau_{\mathrm{mir}}} = \frac{qN_{\mathrm{mir}}\mu_{\mathrm{mir}}}{L_{\mathrm{mir}}} \tag{2}$$

where N_{maj} is the substrate doping concentration, and $L_{\mathrm{maj}}(\tau_{\mathrm{mir}})$ and μ_{mir} are the diffusion length (lifetime) and mobility of minority carriers in the bulk material, respectively. To correctly observe the temperature dependence of the minority-carrier response behavior, all of the parameters are a function of the temperature in the calculations, except for τ_T because of the weakly temperature dependence. In Fig. 5(a), we provide the simulated result of Arrhenius-dependent substrate conductance G_{sub} in Si and Ge at various dopant concentrations (10^{14} and 10^{16} cm^{-3}), plotted with experimental data obtained from this and previous studies. Note that these values of G_{sub} in inversion, i.e., G_{inv}, can be extracted by directly subtracting the reactance of the insulator capacitor C_{ins} from the commonly used parallel equivalent circuit. As seen for both Si and Ge cases, the simulated G_{sub} curves can be divided into two stages: one dominated by G_{diff} at high temperatures and the other by G_{gr} at low temperatures. Most importantly, the values of G_{inv} of the dielectric on Ge were larger than those on Si by at least four orders of magnitude, which is indicative of a larger energy loss occurring in Ge. Both our data of Al_2O_3/p-Ge and the reported HfO_2/n-Ge structure [12] are in agreement with the simulation results for the SiO_2/p-Ge structure.

Using (1) and (2), we evaluated the respective components of G_{gr} and G_{diff} in G_{inv} for these two substrates. A high bulk trap volume density N_T of 10^{15} cm^{-3} was assumed in Ge, which is relative to a value of 10^{14} cm^{-3} in Si, because Ge wafer quality has not yet developed to a satisfactory level. Fig. 5(b) reveals that the crossover temperature T_{C} at which the transition is made from the g–r mechanism dominating to the diffusion-controlled process was ca. 330 K for p-Ge, which is close to the value of ca. 318 K characterized for high-k/n-Ge($N_D =$ ca. 7×10^{14} cm^{-3}) [12]. Relative to the value of T_C of ca. 442 K for its Si counterpart, we ascribe the lower value for Ge to its higher value of n_i. Here, the deviations in the values of G_{inv} evaluated via the MEDICI simulations and the theoretical calculation arose from the adopted material parameters, e.g., the N_T value. We also calculated the magnitude of the wC_{inv} term for comparison with the values of G_{inv} in these two substrates, where C_{inv} is defined using the following [9]:

$$C_{\mathrm{inv}} = \frac{\varepsilon_s \varepsilon_o}{\sqrt{2}L_D}\frac{n_i}{N_{\mathrm{maj}}}\exp\left(\frac{-q\phi_S}{2kT}\right) \tag{3}$$

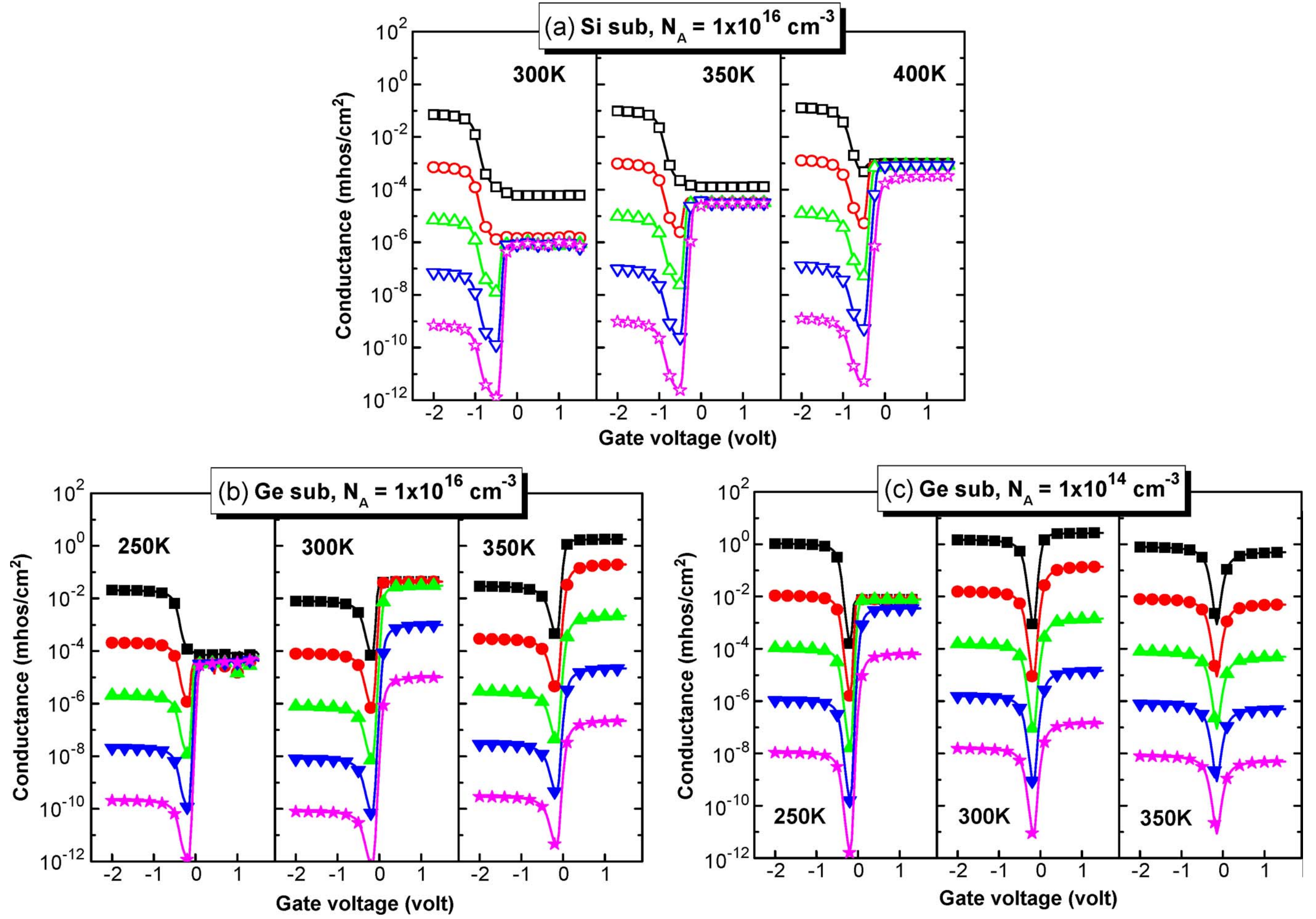

Fig. 2. MEDICI-simulated G–V curves of Al/SiO$_2$ gate stacks on Si and Ge substrates under measured temperatures ranging from 250 to 400 K. (a) p-Si, 10^{16} cm^{-3}. (b) p-Ge, 10^{16} cm^{-3}. (c) p-Ge, 10^{14} cm^{-3}. Note that the measured frequencies are labeled by solid symbols: square (1 MHz), circle (100 kHz), up-triangle (10 kHz), down-triangle (1 kHz), and star (100 Hz).

where ε_s is the substrate dielectric constant, L_D is the Debye length, and ϕ_S is equal to $2\phi_B$ at the threshold inversion point (ϕ_B is the bulk potential). The calculations revealed that $wC_{\rm inv} \gg G_{\rm inv}$ for the Si case at temperatures up to ca. 400 K; thus, the equivalent substrate circuit in inversion is often simplified further so that the depletion capacitance $C_{\rm dep}$ changes in parallel only with the $G_{\rm inv}$ term. This conclusion is only suitable for the Ge counterpart when the temperatures decrease below ca. 250 K; meanwhile, the opposite behavior, i.e., $wC_{\rm inv} \ll G_{\rm inv}$, occurs at temperatures above ca. 350 K. That is, at intermediate temperatures (250–350 K), the minority-carrier response in Ge MOS capacitors is strongly dependent on the measured temperature and frequency.

Here, we define the effective transition frequency $f_{\rm tran}$—at which the capacitance in inversion is midway between $C_{\rm ins}$ and the HF capacitance $C_{\rm hf}$—as marking the onset of the LF C–V behavior. Our experimental data for $f_{\rm tran}$ observed in Al$_2$O$_3$/p-Ge (Fig. 3) are within the MEDICI-simulated predictions in Fig. 6(a). The fast response rates in the Ge capacitors corresponded to the higher values of $f_{\rm tran}$, i.e., ca. 5 and 200 kHz at RT for Ge doped at 10^{16} and 10^{14} cm^{-3}, respectively. Higher degrees of substrate doping and lower measured temperatures accordingly lowered the order of $f_{\rm tran}$ due to the abatement of minority-carrier disturbance. From these studies, we conclude that the two energy loss mechanisms, i.e., $G_{\rm gr}$ and $G_{\rm diff}$, are responsible for the supply of minority carriers to the inversion layer, providing LF-like C–V properties in the kilohertz regime. Previously, Bai *et al.*[14] reported an interesting phenomenon in HfO$_2$/p-Ge: An increase in the degree of substrate doping from 10^{15} to 4×10^{17} cm^{-3} reduced the value of $f_{\rm tran}$ from greater than 100 kHz to less than 10 kHz. Upon increasing the Ge concentration to 3×10^{18} cm^{-3}, however, the value of $f_{\rm tran}$ increased again to greater than 1 MHz, which is opposite to the trend that we expected. To explain this anomalous behavior, we correlated the value of $f_{\rm tran}$ to the changes in $G_{\rm inv}$ using the following equation [9]:

$$f_{\rm tran} = \frac{G_{\rm inv}}{2\pi C_{\rm ins}} \left(1 - \frac{C_{\rm hf}}{C_{\rm ins}}\right) \quad (4)$$

using a value of $C_{\rm ins}$ of 1.11 μF/cm^2 as in our Al$_2$O$_3$/Ge cases, i.e., corresponding to the capacitance-equivalent thickness of 30 Å, and with the assumption that the number of bulk traps was proportional to the dopant concentration. We observe in Fig. 6(b) that Ge doped at 10^{18} cm^{-3} exhibited a relatively high value of $f_{\rm tran}$ with respect to that of the low-doped Ge. Considering that the values of N_T ranging from ca. 10^{14} to 10^{16} cm^{-3} have been reported for an intrinsic Ge epitaxial film [11]

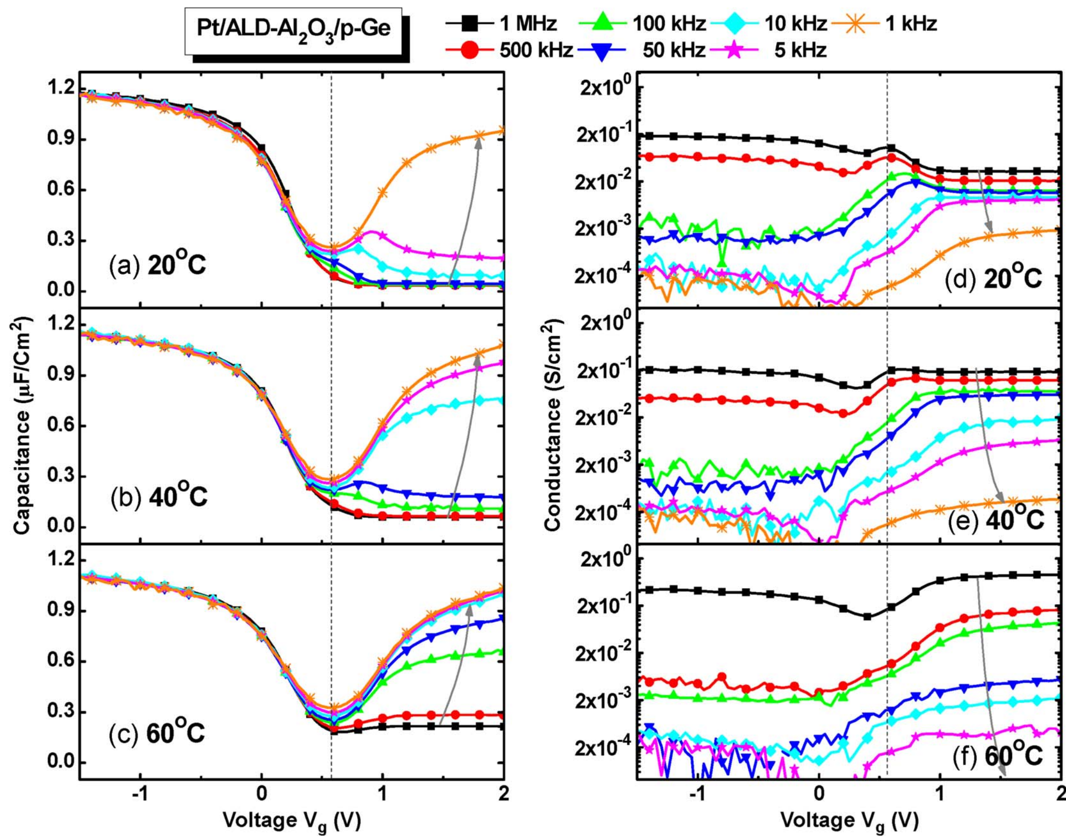

Fig. 3. (a)–(c) C–V and (d)–(f) G–V curves of Pt/ALD-Al_2O_3/p-Ge MOS capacitors measured at temperatures of 20 °C, 40 °C, and 60 °C, respectively.

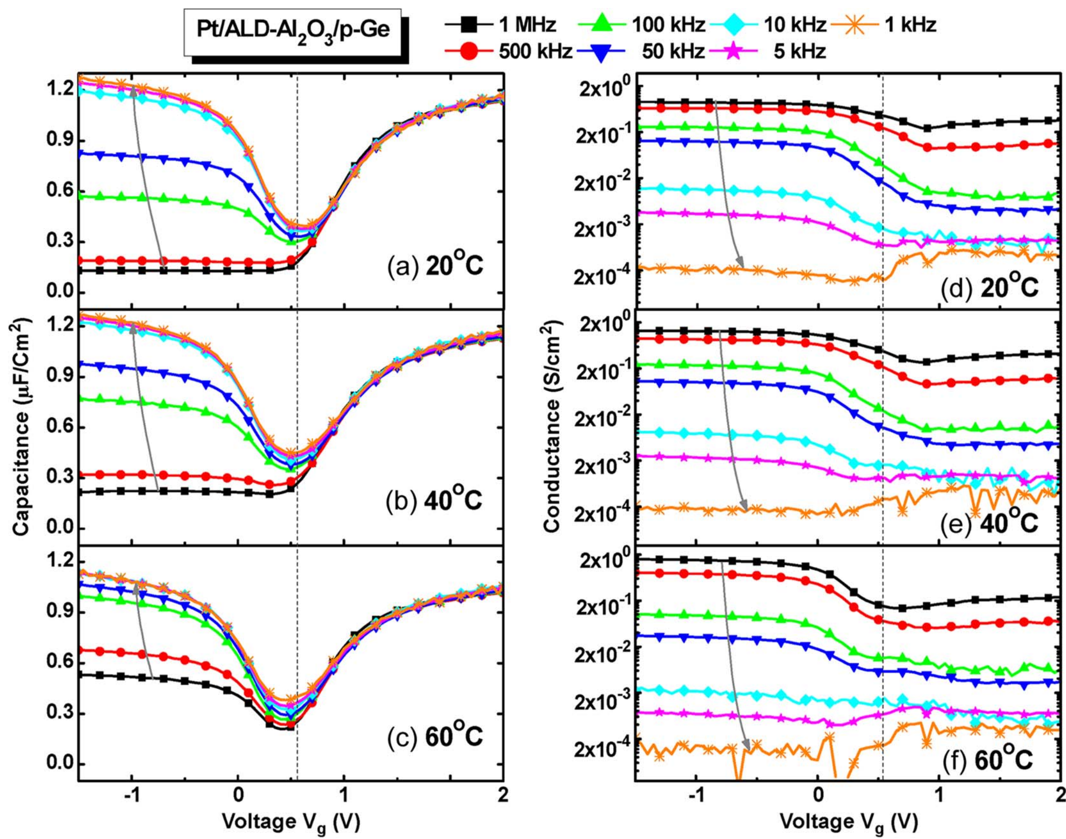

Fig. 4. (a)–(c) C–V and (d)–(f) G–V curves of Pt/ALD-Al_2O_3/n-Ge MOS capacitors measured at temperatures of 20 °C, 40 °C, and 60 °C, respectively.

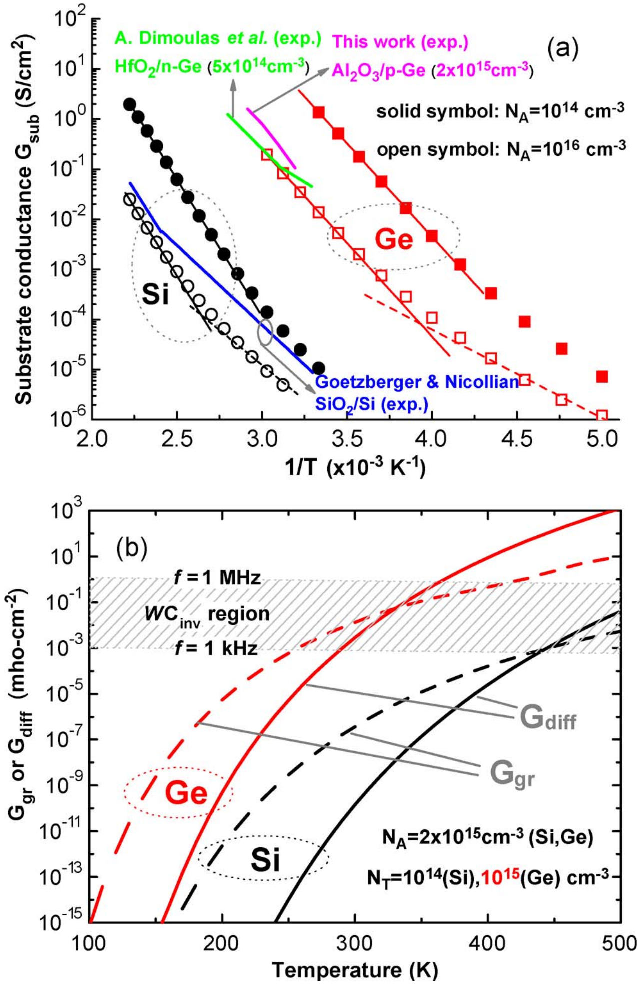

Fig. 5. (a) Simulated Arrhenius-dependent substrate conductances $G_{\rm sub}$ in Si and Ge at two dopant concentrations (10^{14} and 10^{16} cm^{-3}), plotted with the experimental data obtained in this and previous studies [9], [12]. The simulated $G_{\rm sub}$ data can be fitted by the (solid lines) diffusion conductances $G_{\rm diff}$ and (dashed lines) g–r conductances $G_{\rm gr}$. (b) Calculations of temperature-dependent $G_{\rm diff}$ and $G_{\rm gr}$ in Si and Ge substrates having dopant concentrations of 2×10^{15} cm^{-3}. The values of N_T were 10^{14} and 10^{15} cm^{-3} in Si and Ge, respectively. The values of the $wC_{\rm inv}$ term were also calculated in terms of the frequency range 1 kHz–1 MHz.

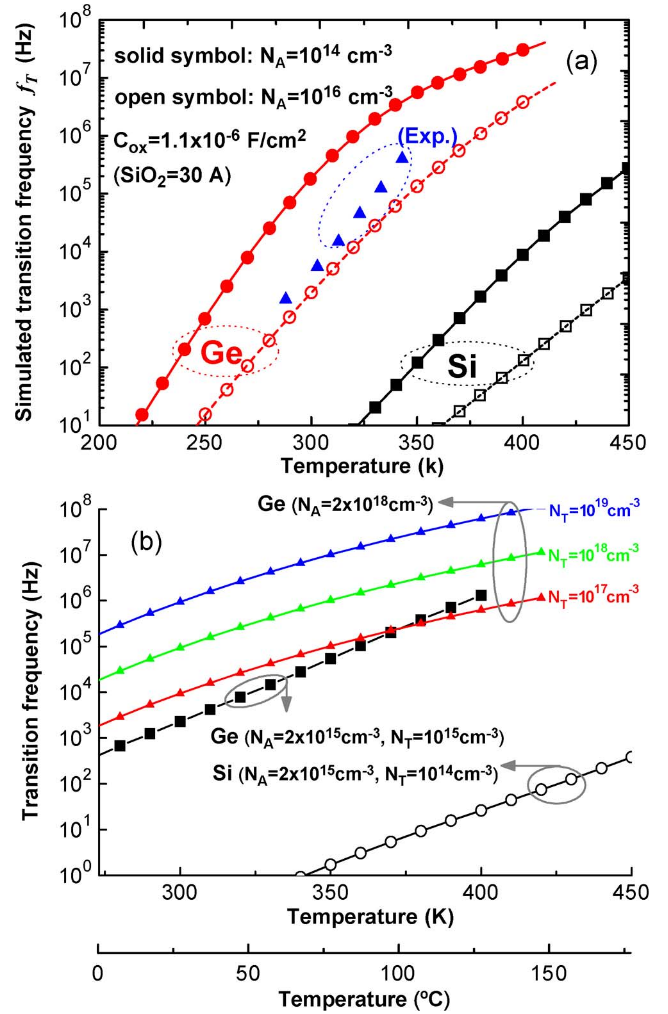

Fig. 6. (a) Simulated temperature-dependent transition frequencies $f_{\rm tran}$ in Si and Ge at two dopant concentrations (10^{14} and 10^{16} cm^{-3}), plotted along with our experimental data from Figs. 5 and 7. (b) Calculated temperature-dependent transition frequencies $f_{\rm tran}$ in Si and Ge substrates, determined according to the material parameters in Fig. 8. Different values of N_T ($10^{17} - 10^{19}$ cm^{-3}) were assumed for our highly doped Ge system.

and low-doped Ge substrates [21], [22], together with a maximum solid solubility of ca. 10^{19} cm^{-3} for p-type dopants, we suspect that the highly doped p-Ge wafer might contain a large number of midgap traps (e.g., 10^{17}–10^{19} cm^{-3}) inside the depletion layer [14], possibly arising from high degrees of Fe and Ni metal impurities [22], dopant precipitation, and/or metal–dopant combined defects. In reality, the density of bulky defects is governed not only by the wafer type and contamination by impurities but also by the device's fabrication [23], [24], in particular, the dielectric–Ge interface, which, in turn, influences the degree of the minority-carrier response on the measured frequency. In other words, the magnitude of $G_{\rm gr}$ is probably comparable with that of $G_{\rm diff}$—possibly even exceeding it at higher temperatures—but $G_{\rm diff}$ still immediately rules the inversion conductance $G_{\rm inv}$ as the temperature increases further.

On the other hand, because the device equivalent circuit in inversion is similar to that in depletion, it is essential to explore the differences between the minority-carrier-induced loss and the interface-state loss with respect to the measured frequency. Thus, we calculated the temperature dependence of the interface-state response frequency $f_{\rm it}$ as a function of the surface potential using the following equation [9]:

$$f_{\rm it} = \frac{v_{\rm th}\sigma_{\rm cap}n_i}{\pi} \exp\left(\frac{-q\phi_S}{kT}\right) \qquad (5)$$

where $v_{\rm th}$ is the thermal velocity, and $\sigma_{\rm cap}$ is the capture cross section. Supposing that the standard measured frequency is in the range 10^3–10^6 Hz, as depicted in Fig. 7(a), we can detect $D_{\rm it}$ close to the midgap in Ge only at values of $f_{\rm it}$ greater than 10^5 Hz, which is quite different from the $D_{\rm it}$ response observed as low as 10^3 Hz in Si. Indeed, we observed depletion bumps at frequencies of 50–1000 kHz for the Al_2O_3/p-Ge capacitors (Fig. 3) and at 1–100 kHz for the Al_2O_3/p-Si capacitors (not shown here). In contrast, we did not observe any such bump for the corresponding n-Ge case (Fig. 4) because of the intense minority-carrier loss. The calculated results in Fig. 7(b) and (c) suggest that continuously decreasing the temperature from 300

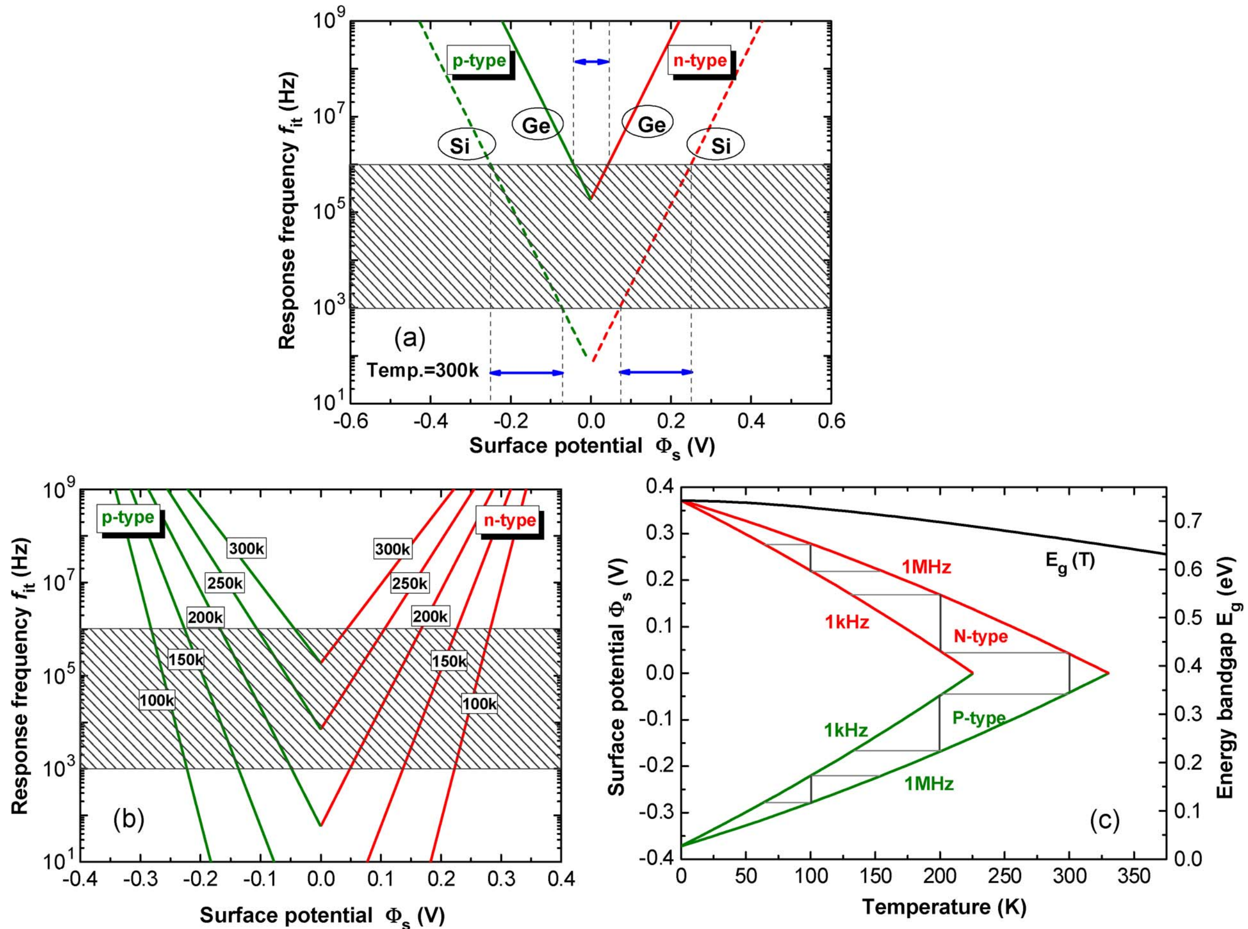

Fig. 7. (a) Calculated response frequency f_{it} of interface states plotted as a function of the surface potential ϕ_S for Si and Ge capacitors at RT. (b) Temperature dependence of the plots of f_{it} versus ϕ_S for the Ge capacitor. The shadow region represents the standard frequency range 1 kHz–1 MHz used for the measurements. (c) Plot of the ϕ_S dependence of observable D_{it} in the Ge bandgap at various measured temperatures (within the standard frequency range). For comparison, the temperature dependence of the Ge bandgap is presented on the right-hand y-axis.

to 100 K is a practical means of extracting the overall distribution of D_{it} within the Ge bandgap. Such a temperature-dependent conductance method is discussed in detail in a recent literature review by Martens *et al.*[10].

Fig. 8(a)–(f) displays the G_{sub}/f versus $\log f$ characteristics for both types of Ge under gate biases ranging from the midgap to the inversion. We employed the statistical conductance model to estimate the values of the midgap D_{it} for p-Ge and n-Ge of ca. $7(\pm 1) \times 10^{11}$ and $1.5(\pm 0.5) \times 10^{12}$ cm^{-2} eV^{-1}, respectively. An interesting trend appeared for the devices biased into the inversion conditions: The G_{sub}/f peak gradually moved to lower frequency, accompanied by an increased intensity, and upon raising the temperature; as a consequence, the overall conductance spectra shifted to higher frequency. Because of the presence of a high minority-carrier density, this phenomenon reveals that we must consider the communication of interface traps not only with majority carriers but also with minority carriers in Ge MOS capacitors. Even so, we still believe that such a shift in the frequency-dependent conductance peaks is mainly correlated to the G_{inv} loss within the substrate itself, overwhelming the D_{it}-induced energy loss in inversion. We rationalize this behavior by considering the following observations. First, from the viewpoint of the f_{it} calculation, the G_{sub}/f peaks appear far below 10^5 Hz, which is irrational for the D_{it} response in Ge devices that are close to RT. Next, assuming that the transition of the surface minority carriers with D_{it} dominates the conductance peaks in inversion, the resultant shorter lifetime in the charging/discharging of D_{it} should shift them to higher frequency, rather than lower frequency, upon increasing the inversion biases. In fact, a Λ-shaped distribution in the trap time constant across the overall Ge bandgap was observed under a quite low temperature of 80 K when employing a full conductance measurement [10], in which the G_{sub}/f peaks shifted initially to lower frequency and subsequently to higher frequency with respect to the gate bias. In addition, according to the classical bulk trap model proposed by Nicollian and Brews [9], the resultant frequency of the G_{sub}/f maximum should coincide with the value of f_{tran} observed in the C–V curves. Indeed, we observed that the conductance peaks (and values of f_{tran}) for p-Ge capacitors were located at ca. 4 (3), 20 (15), and 100 kHz (130 kHz) at 20 °C, 40 °C, and 60 °C, respectively, when V_g was equal to 1 V. The trends were also consistent for the n-Ge cases. In addition, we estimated the effective values of N_T simply from the corresponding magnitudes of G_{sub}/f by evaluating the depletion width swept out by 2-kT band bending; the resulting values of N_T for p-Ge and n-Ge were ca. 3.9×10^{15} and 2.5×10^{15} cm^{-3}, respectively, reflecting high levels of bulky defects existing in these particular Ge wafers.

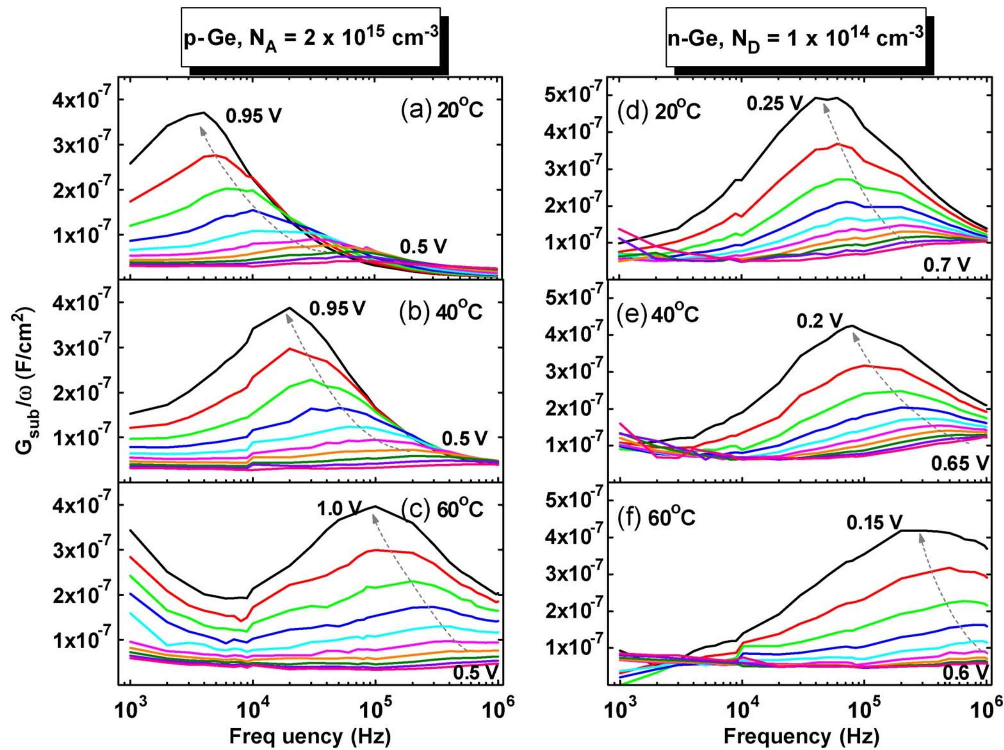

Fig. 8. Measured values of $G_{\rm sub}/w$ plotted with respect to the log frequency for Pt/ALD-Al_2O_3 gate stacks on (a)–(c) p-Ge and (d)–(f) n-Ge substrates at temperatures of 20 °C, 40 °C, and 60 °C, respectively.

IV. Conclusion

We have characterized the substrate conductance and transition frequency characteristics through MEDICI simulations and device experiments on Ge and Si substrates to understand their minority-carrier response behavior. The plot of the Arrhenius-dependent $G_{\rm sub}$ indicated a larger energy loss occurring in Ge than in Si by at least four orders of magnitude, corresponding to the fast minority-carrier response rate. Our $\rm Al_2O_3/Ge$ MOS capacitors exhibited values of $G_{\rm sub}$ and $f_{\rm tran}$ that were both close to those of the MEDICI prediction. We have also validated that a high value of n_i in Ge, via the bulk-trap generation/recombination as well as the diffusion from the bulk substrate, caused the onset of the LF C–V curves in the kilohertz regime and the gate-independent inversion conductance. In addition, we have suggested that the shift in the $G_{\rm sub}/f$ conductance peaks to low frequency upon increasing the inversion bias is mainly due to the transition of minority carriers with bulk traps in the depletion layer, in which the value of N_T reached as high as ca. $(2–4) \times 10^{15}$ cm^{-3} in the low-doped Ge.

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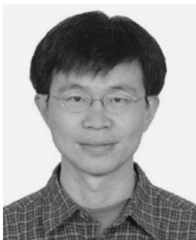

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