A Low-Power and High-Precision Spread Spectrum Clock Generator for Serial Advanced Technology Attachment Applications Using Two-Point Modulation

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***Abstract*—A new technique utilizing two-point (TP) modulation for a spread spectrum clock generator (SSCG) for serial advanced technology attachment is presented in which the divider ratio is varied by a digital $\Sigma\Delta$ modulator, and the voltage-controlled oscillator is modulated analogically. With this technique, the modulation bandwidth is enhanced in order that the modulation profile accuracy and jitter performance caused by the $\Sigma\Delta$ modulator can be improved at the same time. The order of the $\Sigma\Delta$ modulator and the loop filter can be reduced to save power and area, while the electromagnetic interference (EMI) suppression still satisfies specifications. The dual-path loop filter (DL) reduces the size of the loop capacitor and enables full integration. The proposed TPDL-SSCG has been fabricated in a 0.18-μm CMOS process. The size of the chip area is 0.44×0.48 mm^2. The circuit produces a clock of 1.5 GHz with a down-modulation ratio of 0.5%, 10.14 dB EMI of reduction, 5.485 ps rms jitter, and 35 ps peak-to-peak jitter. The power consumption, excluding an output buffer, is only 15.3 mW.**

***Index Terms*—Frequency modulation, phase-locked loops (PLLs), sigma–delta modulation, spread spectrum clock generator (SSCG).**

I. Introduction

SERIAL interfaces are widely used for high data rate transmission. For example, serial advanced technology attachment (SATA), which is the standard for high-speed storage devices such as hard disk drives and compact disk (CD)/digital versatile disk (DVD), can transmit data at rates up to 1.5 or 3 Gb/s for generation I and II, respectively [1]. High-speed clocks often cause electromagnetic interference (EMI). Therefore, the spread spectrum clock generators (SSCGs) are employed in SATA to reduce EMI levels. Typical specifications in SATA are the 5000 ppm down-modulation ratio, modulating frequency within 30–33 kHz, and EMI suppression of at least 7 dB. In order to realize such a fine modulation ratio, fractional-N phase-locked loops (PLLs) with a $\Sigma\Delta$ modulator are usually used [2]–[7]. This technique has the advantages of fully digital control and fine resolution. The modulator is normally driven by a triangular waveform. A nonlinear profile, known as the "Hershey-Kiss" profile, has been suggested for better EMI performance [8]. The nonlinear function of the "Hershey-Kiss" profile makes it more expensive due to large area and power consumption. Therefore, triangular waveforms are still used due to their simple implementation [4], [5]. Another important issue is the choice of loop bandwidth of PLL. The loop bandwidth has tradeoffs between the modulation profile and the jitter caused by the $\Sigma\Delta$ modulator. The profile is distorted and the effect of EMI suppression is degraded if the loop bandwidth is not wide enough. Therefore, the wide bandwidth leads to a request for a third-order $\Sigma\Delta$ modulator in order to suppress the in-band fractional spurious. A design of a third-order $\Sigma\Delta$ modulator with a third-order loop filter and a 300-kHz loop bandwidth to improve the jitter and the modulation profile was presented in [4]. However, the third-order $\Sigma\Delta$ modulator has high power consumption and occupies a large area. Recently, the method of two-point (TP) modulation, which has the divider and the voltage-controlled oscillator (VCO) modulated at the same time, was presented to enhance the bandwidth and improve EMI performance [9]. Here, a new version of SSCG with TP modulation is presented for the SATA application [10]. The jitter caused by the $\Sigma\Delta$ modulator can be reduced by a small loop bandwidth, while the modulation profile can still be maintained. Only a second-order $\Sigma\Delta$ modulator, as well as a second-order loop filter, is adopted. The chip area and power consumption are improved. In addition, aided with a dual-path loop filter (DL), the proposed TPDL-SSCG can be fully integrated.

The organization of the paper is as follows. Section II describes the proposed TPDL-SSCG including the linear model analysis, analysis of the noise power spectral density (PSD) from the $\Sigma\Delta$ modulator and VCO, the proposed digital modulation path, the proposed analog modulation path, and simulation results. Main circuits are briefly described in Section III. The measurement results are demonstrated in Section IV. Conclusions are given in Section V.

II. Proposed TPDL-SSCG

It is well known that the transfer function of the phase response from the feedback divider to VCO output is a low-pass function. On the contrary, the function from VCO input to VCO output is a high-pass function. A wideband response can be achieved if the loop is excited through these two points. The block diagram of the proposed SSCG is shown in Fig. 1 with a phase frequency detector (PFD), a DL containing

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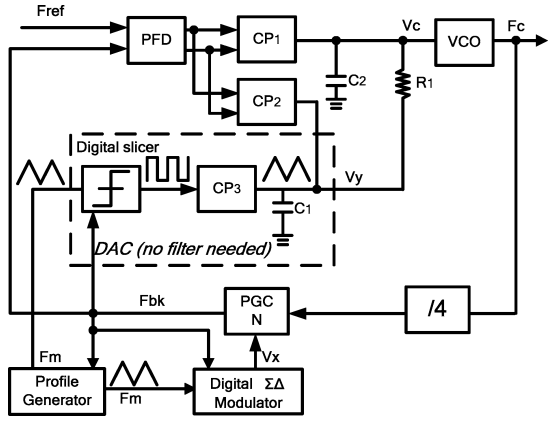

Fig. 1. Block diagram of the proposed TPDL-SSCG.

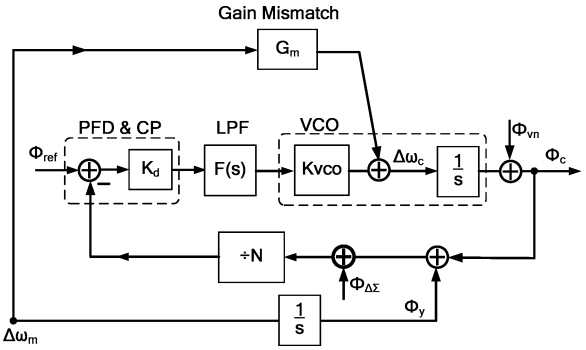

Fig. 2. Linear model of the proposed TPDL-SSCG.

$\mathrm{CP}_1, \mathrm{CP}_2, R_1, C_1$, and C_2, a VCO, a prescaler, a 5-bit programmable counter (PGC), a digital $\Sigma\Delta$ modulator, a modulation profile generator, and a digital-to-analog converter (DAC). Compared to the conventional one, this circuit incorporates two extra circuits of charge pump CP_2 and DAC. The staircase triangular waveform is digitally generated by the profile generator. The frequency modulation is obtained from two inputs V_x and V_y, where V_x is the input of the multimodulus divider and V_y is the input of the VCO. The all-pass behavior is obtained as long as the modulation coefficients along the two paths are matched. The modulation path from V_x to the output is referred as the digital modulation path while the modulation path from V_y to the output is referred as the analog modulation path.

A. Linear Model Analysis

Rather than finding out the phase relationship, here, the frequency relationship in s-domain is adopted to study the frequency modulation in SSCG. The linear model is shown in Fig. 2, where $\Delta\omega_c$ is the output frequency deviation, $\Delta\omega_m$ is the input modulating frequency deviation, and G_m is the gain mismatch factor stand for compensation between two paths. Two noise sources are taken into consideration: modulator quantization noise $\Phi_{\Delta\Sigma}$ and VCO phase noise Φ_{vn}. Here, only the gain mismatch is taken into consideration because the delay mismatch is assumed to be negligible due to the proposed DAC.

To see the advantage of TP modulation, we first examine the results with only one-point modulation V_x. For simplicity, the noise sources are ignored. The transfer function from $\Delta\omega_m$ to $\Delta\omega_c$ can be described as

$$\frac{\Delta\omega_c}{\Delta\omega_m} = \frac{K_{\mathrm{VCO}} K_d F(s)}{Ns + K_{\mathrm{VCO}} K_d F(s)}. \tag{1}$$

Here K_d is the gain of the PFD and the charge pump, N is the nominal divider value, $F(s)$ is the loop filter transfer function, and K_{VCO} is the conversion gain of the VCO. It is actually a low-pass behavior when $F(s)$ is taken into account. A triangular wave is given as a waveform sweeping frequency from low to high in one-half of period and from high to low in the other half of period. The variable $\Delta\omega_c$ can be given as

$$\Delta\omega_c = \frac{K_{\mathrm{VCO}} K_d F(s)}{Ns + K_{\mathrm{VCO}} K_d F(s)} \frac{M_{\mathrm{ramp}}}{s^2} \tag{2}$$

as a frequency ramp with a slope of M_{ramp} is applied, i.e., $s^2 \Delta\omega_m = M_{\mathrm{ramp}}$. Equation (2) can be rewritten as

$$\Delta\omega_c = \frac{Ks + K\omega_2}{s^2 + Ks + K\omega_2} \frac{M_{\mathrm{ramp}}}{s^2} \tag{3}$$

with $K = K_d \times K_{\mathrm{VCO}} \times R_1/N$, and is approximately equal to the loop bandwidth of PLL and $\omega_2 = 1/R_1 C_1 K_2$ is the zero of the loop filter. Here, the C_2 effect is neglected. The frequency error defined by $\Delta\omega_{\mathrm{err}} = \Delta\omega_m - \Delta\omega_c$ can be found by

$$\Delta\omega_{\mathrm{err}} = \frac{M_{\mathrm{ramp}}}{s^2 + Ks + K\omega_2}. \tag{4}$$

Using inverse Laplace transform and under $\omega_2 \ll K$, the transient response is obtained

$$\begin{aligned} \Delta\omega_{\mathrm{err}}(t) &= \frac{M_{\mathrm{ramp}}}{K - \omega_2} \left(e^{-\omega_2 t} - e^{-Kt}\right) \\ &\approx \frac{M_{\mathrm{ramp}}}{K} \left(e^{-\omega_2 t} - e^{-Kt}\right). \end{aligned} \tag{5}$$

The maximum frequency error $\Delta\omega_{\mathrm{err}}$ can be found by (5) as

$$\max\left(\Delta\omega_{\mathrm{err}}\right) \propto \frac{M_{\mathrm{ramp}}}{K}. \tag{6}$$

Equations (5) and (6) indicate how the low-pass behavior causes frequency errors and distorts the output. It is clear that $\Delta\omega_{\mathrm{err}} = 0$ only if $K = \infty$, i.e., the loop bandwidth is infinitely large.

With TP modulation activated, by the superposition principle, the closed-loop transfer function of Fig. 2 can be derived as

$$\frac{\Delta\omega_c}{\Delta\omega_m} = T(s) + (1 - T(s)) \times G_m \tag{7}$$

with

$$T(s) = \frac{K_{\mathrm{VCO}} K_d F(s)}{Ns + K_{\mathrm{VCO}} K_d F(s)}. \tag{8}$$

The first term in the right-hand side is the same as (1). The second term appears as a high pass and can be treated as a complementary part if $G_m = 1$. Therefore, from (7), $\Delta\omega_c$ is equal to $\Delta\omega_m$ if $G_m = 1$. This means that the output is all pass without distortion and bandwidth limitation.

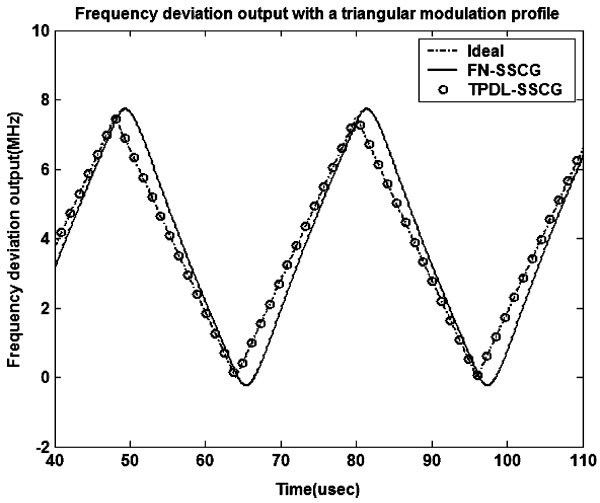

Fig. 3. Simulation results of frequency deviation output with a triangular modulation profile.

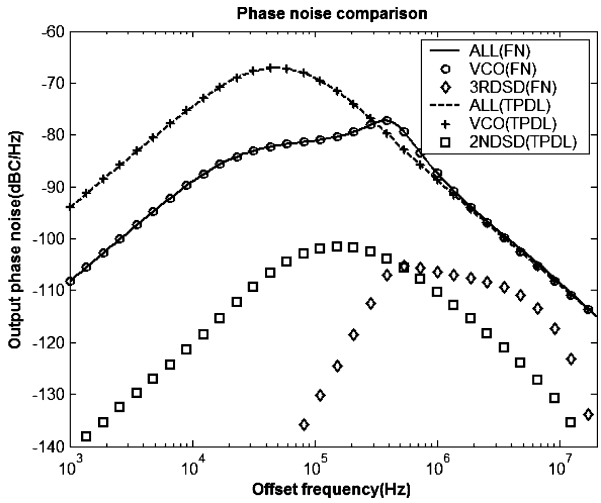

Fig. 4. Phase noise simulation for FN-SSCG and TPDL-SSCG.

A triangular waveform $\Delta\omega_m(t)$ with a mean of zero can be written as

$$\begin{aligned}\Delta\omega_m(t) &= 2\Delta f_{\text{amp}}(2f_m t - 0.5), \quad \text{for } \frac{n}{2f_m} \le t < \frac{2n+1}{2f_m} \\ &= 2\Delta f_{\text{amp}}(1.5 - 2f_m t), \quad \text{for } \frac{2n+1}{2f_m} \le t < \frac{n+1}{f_m}\end{aligned} \tag{9}$$

where Δf_{amp} is the amplitude of the waveform and n is an arbitrary integer number. The frequency deviation outputs for both one-point modulation and the proposed scheme, with the triangular modulation profile input from (9), are shown in Fig. 3. Here, $G_m = 1$, the modulating frequency is 31.25 kHz, and the target frequency deviation is 7.5 MHz, which is the same as SATA specification. The dashed-dotted solid line is the ideal all pass, the solid line is from (1), the FN-SSCG case, and the line with a circle mark is the output from (7), the TPDL-SSCG case. The solid line cannot track the input frequency change well due to insufficient loop bandwidth. On the contrary, the line with circle mark can always track the input so that the output error is eliminated. Thus, the proposed scheme can track the modulation waveform very well and is independent of the PLL bandwidth and other loop parameters as long as the paths are matched.

B. Analysis of Noise PSD From the $\Sigma\Delta$ Modulator and the VCO

The PSD is closely related to the order of the $\Sigma\Delta$ modulator and loop bandwidth. It is already known that a high-order $\Sigma\Delta$ modulator is used to reduce the fractional spur within the loop bandwidth. In this design, only a second-order $\Sigma\Delta$ modulator is chosen to save area and power, while maintaining jitter and EMI performance. To see the interrelation between the order of the $\Sigma\Delta$ modulator and PLL bandwidth, the output phase noise originating from the $\Sigma\Delta$ modulator and the VCO is investigated. The noise PSDs of the phase $S_\Phi(f)$ can be expressed as

$$S_\Phi(f) = S_{\Phi\text{VCO}}(f) + S_{\Phi\Delta\Sigma}(f) \tag{10}$$

where $S_{\Phi\text{VCO}}(f)$ and $S_{\Phi\Sigma\Delta}(f)$ are the noise of the VCO and the $\Sigma\Delta$ modulator, respectively. $S_{\Phi\Delta\Sigma}(f)$ [16] can be found as

$$S_{\Phi\Delta\Sigma}(f) = \frac{(2\pi)^2}{12 f_{bk}}\left[2\sin\left(\frac{\pi f}{f_{bk}}\right)\right]^{2(m-1)} |T(s)_{s=j2\pi f}|^2 \tag{11}$$

where m is the order of the modulator and f_{bk} is the operational frequency of the modulator. $S_{\Phi\text{VCO}}(f)$ can be easily derived as

$$S_{\Phi\text{VCO}}(f) = S_{\Phi vn}\,|1 - T(s)_{s=j2\pi f}|^2 \tag{12}$$

where $S_{\Phi vn}$ is the stand-alone VCO phase noise.

In general, the loop bandwidth is much less than the phase comparison frequency f_{bk} at the phase detector to avoid the spur. From (11), it is realized that the shape of output PSD, caused by the $\Sigma\Delta$ modulator, is increasing inside the PLL bandwidth with $f^{2(m-1)}$ and decreasing outside the PLL bandwidth. In other words, the smaller the PLL bandwidth, the lower the jitter caused by the $\Sigma\Delta$ modulator. However, a large PLL bandwidth is needed to pass faithfully the modulation profile. Otherwise, the spectrum appeared at the output of PLL will be distorted, the modulation ratio will be incorrect, and EMI performance will be degraded. Thus, the PLL bandwidth is a tradeoff between the modulation profile and the jitter performance. In the conventional situation [4], the bandwidth is approximately ten times the modulating frequency to obtain good performance. The in-band fractional spur is suppressed by a third-order $\Sigma\Delta$ modulator to minimize the phase noise and jitter. In addition, a third-order loop filter is needed to reduce the out-of-band phase noise and jitter caused by the comparison clock. In other words, it requires higher power consumption and more area. However, due to the all-pass nature in the proposed method, the PLL bandwidth can be shrunk for jitter without the modulation profile distortion.

The PSDs for the conventional fractional-N SSCG (FN-SSCG) and the TP SSCG (TPDL-SSCG) in nonspread spectrum mode are illustrated in Fig. 4. Only the VCO and the modulator quantization noise are taken into account. The VCO phase noise is measured as -89 dBc/Hz at the offset frequency of 1 MHz with the shape of f^{-2}. Other simulation parameters

TABLE I
SSCG SIMULATION PARAMETERS

	FN-SSCG	TPDL-SSCG
Input Frequency	25 MHz	25 MHz
Output Frequency	1500 MHz	1500 MHz
Modulation ratio	-0.5%-0	-0.5%-0
Modulating Frequency	31.25 kHz	31.25 kHz
VCO Gain	480 MHz/V	480 MHz/V
Loop Bandwidth	100/300 kHz	100/300 kHz
Modulator	third-order MASH	second-order MASH
Loop filter	third-order	second-order
Third pole frequency	4 MHz	N/A

are listed in Table I. Two different cases with loop bandwidths of 100 and 300 kHz are studied. A third pole of 4.5 MHz is needed for the FN-SSCG to further filter the quantization noise of the third-order modulator. The center frequency is set at 1500 MHz, the modulation ratio is -0.5%, and the modulating frequency is set at 31.25 kHz. The solid and dashed lines represent the total phase noise for the FN-SSCG with a 300-kHz loop bandwidth and TPDL-SSCG with a 100-kHz loop bandwidth, respectively. The contributions from the VCO are denoted by circle and plus marks in different cases. The phase noise from the $\Sigma\Delta$ modulator is denoted by diamond and square marks. Although the in-band phase noise in the TPDL-SSCG with a second-order $\Sigma\Delta$ modulator is larger than the case in the FN-SSCG with a third-order $\Sigma\Delta$ modulator, the TPDL-SSCG still has enough performance in terms of EMI suppression, modulation profile linearity, and jitter through the following analysis and measurements.

The chip areas for the second- and third-order multistage noise shaping (MASH) $\Sigma\Delta$ modulators are evaluated as 3920 and 4887, in units of gate counts, respectively. The power consumption using the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm process is 1.40 and 2.00 mW, respectively. The area is approximately 20% off in digital area and approximately 5% off in whole area and the power is approximately 4% off in whole power consumptions when using the second-order $\Sigma\Delta$ modulator. The 4%–5% difference is still important because the power and area of the proposed SSCG are only 15.3 mW and 0.21 mm^2, respectively. Hence, in this paper, a second-order $\Sigma\Delta$ modulator and a 100-kHz loop bandwidth, with a second-order loop filter, are designed for saving power and area.

C. Proposed Digital Modulation Path

The digital modulation path consists of a fractional-N-based PLL and the modulation profile generator. The block diagram of the proposed profile generator and $\Sigma\Delta$ modulator is shown in Fig. 5. The input range of the $\Sigma\Delta$ modulator must fulfill the requirement of 0 to -5000 ppm modulation ratio. In order to lower the speed requirement of the PGC from 1.5 GHz to 375 MHz, a divided-by-4 prescaler, implemented by the true single-phase clock (TSPC) logic, is ahead of the PGC. Accordingly, the fractional number is varied between 0.925 and 1. A MASH-type $\Sigma\Delta$ modulator has an input range of less than 1 and cannot be used in this application. To eradicate this issue, a new version of the MASH-1-1 $\Sigma\Delta$ modulator, with extended input range, is used to overcome the overflow problem in the modulator [13]. Stage 1 has two carry bits while stage 2 has only one carry bit. The two-bit carry outputs cause

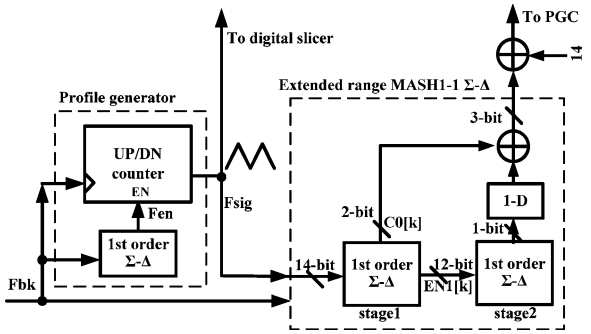

Fig. 5. Block diagram of the proposed profile generator and $\Sigma\Delta$ modulator.

inputs larger than, or equal to, 1 to quickly pass the integer part of the input to the output, and will not saturate the following stages. The advantages of this design are unconditional stability and small area similar to the conventional MASH-1-1 $\Sigma\Delta$ modulator. In addition, this circuit has approximately three times the input range of the conventional MASH-1-1 $\Sigma\Delta$ modulator.

The profile generator consists of an up/down counter and a first-order $\Sigma\Delta$ modulator [14]. In order to utilize the simple architecture of the MASH-type $\Sigma\Delta$ modulator, which is composed of adders and some simple logic circuits and whose output of each stag is the carry output of the adders, the bit number B of the adder should be power of 2. In addition, the modulating frequency must be within 30–33 kHz. With the aforementioned two constraints on the modulation profile generator, the operating frequency of the modulation profile generator may not the same as F_{bk}, the input clock of the modulator. The following analysis will show the reason. Assuming the actual operating frequency of the up/down counter to be $F_{\rm cnt}$, which is determined from the modulation ratio δ, the modulating frequency f_m, and the bit number of the MASH-1-1 $\Sigma\Delta$ modulator (B), it can be described by

$$f_{\rm cnt} = \frac{f_c}{4f_{bk}} \times 2 \times \delta \times 2^B \times f_{\rm sig}. \tag{13}$$

Therefore, an extra first-order $\Sigma\Delta$ modulator is added to generate the additional enable signal $f_{\rm en}$ to lower the operation frequency of the up/down counter, as shown in Fig. 5. The relationship between $f_{\rm cnt}$ and $f_{\rm en}$ is $f_{\rm cnt} = f_{\rm en}$ and f_{bk}. In this study, f_c is 1.5 GHz, f_m is 31.25 kHz, and δ is 0.5% to meet SATA specifications. In addition, $B = 12$ and $f_{bk} = 25$ MHz. One can calculate that $f_{\rm cnt} = 19.2$ MHz.

Unlike [4], the proposed model does not need some level shifters and comparators to increase the area and power consumption, nor does it require complicated $\Sigma\Delta$ modulator. Moreover, the loop bandwidth can be lowered to minimize the jitter contribution from the modulator through the following analysis.

D. Proposed Analog Modulation Path

The analog modulation path is composed of the DAC and the PLL, which is the same as the digital modulation path. The function of the DAC is redrawn in Fig. 6(a). It consists of a digital slicer, charge pump CP_3, and capacitance C_1. An analog triangular waveform across C_1 is obtained from a digital triangular waveform F_m. The digital triangular waveform is

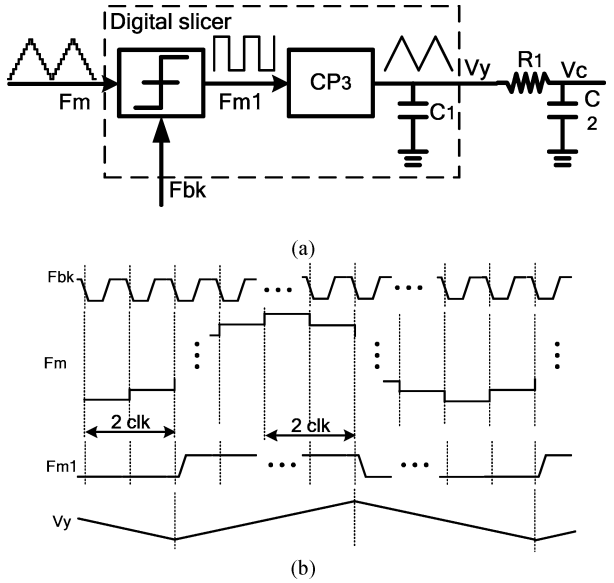

Fig. 6. (a) Proposed DAC. (b) Timing diagram for the proposed DAC.

first sliced into a square waveform F_{m1}, and then it charges the capacitor C_1 to achieve digital-to-analog conversion. The digital transition is smoothed out to reduce VCO interference. The analog modulation path, whose response is high-passed, serves as the compensation for the digital modulation path, whose response is low-passed. Unlike the VCO directly modulated SSCGs such as [21] and [24], the loop bandwidth does not need much smaller than the modulation frequency and the required capacitor in the loop filter can be much smaller. As compared to a traditional one [11], no high-resolution DAC or reconstruction filter is needed. Therefore, the power consumption and the chip area can be reduced.

The gain and delay mismatch is known to degrade the performance [11]. The following approach is utilized to eliminate this nonideality from the delay mismatch. Referring to the timing diagram in Fig. 6(b), F_{m1} and V_y are two clocks delayed with respect to F_m in order to synchronize the delay from F_m to the output of the $\Sigma\Delta$ modulator V_x. Because the digital slicer, the profile generator, and the $\Sigma\Delta$ modulator use the same clock F_{bk}, which is the output frequency of the PGC, the delay mismatch can be avoided.

The relation between controlled voltage V_c and the current I_{p3} of CP_3 can be written as

$$\frac{V_c}{I_{p3}} \approx \frac{1}{s\left(C_1 + C_2\right)} \tag{14}$$

under the condition $f_m \ll 1/(2\pi R_1 C_2)$. The loading effects of CP_1 and CP_2 are neglected due to high output impedances. Accordingly, the smooth triangular waveform is obtained as I_{p3} is a square waveform. Here, both C_1 and C_2 with one terminal grounded are implemented by the accumulation MOS capacitor to save area. Both have good distortion performance when the gate-source bias voltage is equal to, or large than, 1 V [12]. The modulation ratio $\delta \equiv \Delta f_c / f_c$ as a function of I_{p3} is predicted as

$$\delta = \frac{I_{p3} K_{\mathrm{VCO}}}{2\left(C_1 + C_2\right) f_m f_c} \tag{15}$$

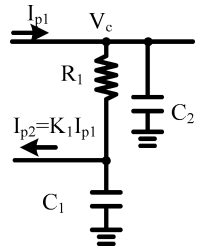

Fig. 7. Simplified block diagram of the DL.

where f_c is the carrier frequency, Δf_c is the peak deviation of the carrier frequency, f_m is the modulating frequency of the triangle wave, and K_{VCO} is the conversion gain of VCO.

From (15), since $C_{1(2)}$ is varied within 5% and I_{p3} is varied within 15% in the typical CMOS process, the gain mismatch is mainly contributed by K_{VCO}. Therefore, the VCO with low sensitivity to VCO gain is needed. In this paper, K_{VCO} is varied about $\pm 30\%$ over process, voltage, and temperature variations. It means G_m is changed from about 0.7 to 1.3. From the following simulation results (Section II-E), the gain mismatch impact on modulation ratio will be varied about 0.008% and the gain mismatch impact on EMI performance is about 0.23 dB. Moreover, the VCO calibration technique in [22] can be used to further improve the performance.

To save the capacitor area in the loop filter, a modified DL is utilized [7]. The paths of pumping currents are shown in Fig. 7, in which I_{p1} is the current of CP_1 and I_{p2} is the current of CP_2. Thus, $I_{p2} = K_1 I_{p1}$. The loading effect of CP_3 is neglected. The loop filter transfer function can be derived as

$$F(s) = \frac{V_c}{I_{p1}} = \frac{\left[R_1 C_1/(C_1 + C_2)\right]\left(s + (1/R_1 K_2 C_1)\right)}{s\left(1 + sR_1\left(C_1 // C_2\right)\right)} \tag{16}$$

where $K_2 = 1/(1 - K_1)$. The zero is at $1/(K_2 C_1)\ R_1$. From (16), the effect of capacitance multiplication is high when K_1 is close to 1. It means that the I_{p1} and I_{p2} are close to each other. However, the mismatch between I_{p1} and I_{p2} depends on the area. Therefore, a tradeoff should be made. Here, $K_1 = 0.75$ and $K_2 = 4$ such that the size of capacitance C_1 can be reduced by four times. Compared to the dual-path filter in [24], the dual-path filter adopted here does not need a unity-gain amplifier; therefore, the phase noise is smaller.

E. Simulation Results

To compare the performance between the FN-SSCG and the TPDL-SSCG, the following simulations are made. The same parameters listed in Table I are used. The output frequency swings are shown in Fig. 8. Four different modulation ratios of 0.545%, 0.523%, 0.506%, and 0.510% for the FN-SSCG with a 100-kHz BW denoted by curve (a), the FN-SSCG with a 300-kHz BW denoted by curve (b), the TPDL-SSCG with a 100-kHz BW denoted by curve (c), and the TPDL-SSCG with a 300-kHz BW denoted by curve (d) are obtained, respectively. The corresponding spectra results with the $\Sigma\Delta$ modulator noise are shown in Fig. 9. The simulated EMI reductions with $\Sigma\Delta$ modulator noise are 20.35, 19.69, 20.47, and 19.21 dB for curves (a), (b), (c), and (d) shown in Fig. 8, respectively. The simulation results are summarized in Table II. It is known that the larger the modulation

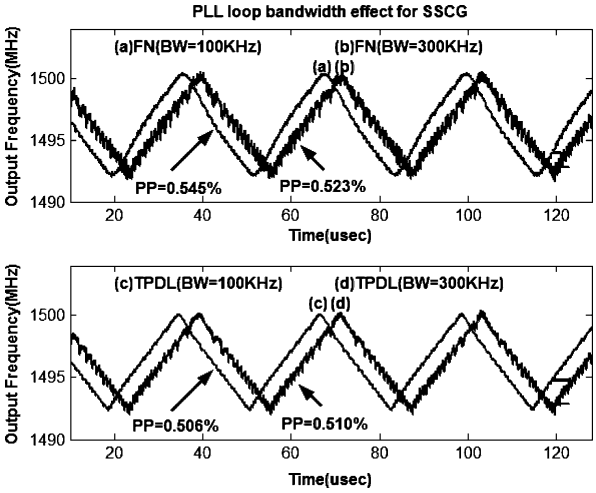

Fig. 8. Simulation results for the FN-SSCG and the TPDL-SSCG under different loop bandwidths.

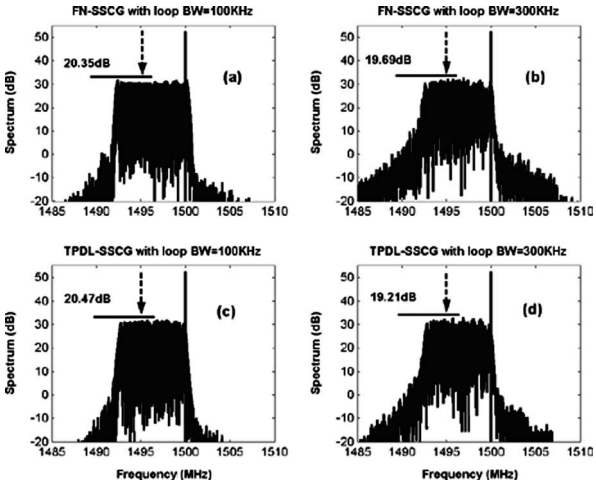

Fig. 9. Spectrum simulation results with the $\Sigma\Delta$ modulator noise for the FN-SSCG and the TPDL-SSCG under different loop bandwidths.

TABLE II
SSCG SIMULATION SUMMARY

	With $\Sigma\Delta$ noise			W/O $\Sigma\Delta$ noise
	Modulation ratio	$A_{\rm dB}$	$A_{\rm dB,norm}$	EMI
FN-SSCG (100 kHz)	0.545	20.35	37.34	20.32
FN-SSCG (300 kHz)	0.523	19.69	37.65	20.95
TPDL-SSCG (100 kHz)	0.506	20.47	40.45	20.76
TPDL-SSCG (300 kHz)	0.510	19.21	37.67	20.70
UNIT	%-pp	dB	dB/%	dB

ratio, the better the EMI performance if the frequency to the modulation profile keeps constant [23]. To see the efficiency of EMI attenuation performance, the EMI reduction and its modulation ratio need to be considered simultaneously. One more parameter, the normalized EMI attenuation ($A_{\rm dB,norm}$), is defined as

$$A_{\rm dB,norm} = 10\log_{10}\frac{10^{A_{\rm dB}/10}}{\delta\%} \tag{17}$$

is also evaluated, where $A_{\rm dB}$ is the measured or simulated EMI reduction level and $\delta\%$ is the modulation ratio in unit of percentage. The case of the FN-SSCG with a 100-kHz BW has the largest modulation ratio (0.545%) deviation from the ideal value 0.5%, and the smallest normalized EMI attenuation with the value of 37.34 dB/% because the PLL bandwidth is not enough that the output could not track the modulation profile and is distorted. Small peaks existed at two ends of the spectrum for the case of the FN-SSCG with a 100-kHz BW, meaning that it is not a good triangular waveform. The case of the FN-SSCG with a 300-kHz BW has better performance in terms of the modulation ratio (0.523%) and normalized EMI attenuation (37.65 dB/%) compared to one with a 100-kHz BW. However, it is clearly indicated that the case of the TPDL-SSCG with a 100-kHz BW has not only a more accurate modulation ratio (0.506%), but also better normalized EMI attenuation (40.45 dB/%) with respect to the two cases of the FN-SSCG because the case of the TPDL-SSCG with a 100-kHz BW has smaller $\Sigma\Delta$ modulator noise than the case of the FN-SSCG with a 300-kHz BW and utilizes the technique of the TP modulation to faithfully pass the modulation profile. This is also indicated from the spectrum shape that no obvious peaks appeared at the two ends of the spectrum. In addition, there is a 0.023% difference in modulation ratios for PLL bandwidths changing from 100 to 300 kHz for the FN-SSCG, while there is only 0.003% difference in modulation ratios for the TPDL-SSCG. The slight difference between curves (c) and (d) in Fig. 9 is due to the quantization noise influence. It implies that the effect of bandwidth is of little importance in the proposed modulation.

More effects are illustrated in Figs. 8 and 9, which show that the bigger loop bandwidth and worse jitter both appeared at the output. The cases with a 300-kHz BW show the bigger instantaneous frequency fluctuations from Fig. 8, and the higher noise level from Fig. 9, with respect to the cases with a 100-kHz BW in both architectures. This confirms the results in (11). The proposed TPDL-SSCG has the advantage of low distortion, so that the modulation profile is more like a triangular wave, and can improve the linearity of the modulation profile and the EMI performance at the same time.

In order to deeply investigate the jitter effect on the EMI suppression level, the spectra simulation results without the $\Sigma\Delta$ modulator noise for FN-SSCG and TPDL-SSCG under the same case as in Figs. 8 and 9 are drawn in Fig. 10. The simulation results are also summarized in Table II. The simulated spectra without the $\Sigma\Delta$ modulator noise are 20.32, 20.95, 20.76, and 20.70 dB for the FN-SSCG with a 100-kHz BW, the FN-SSCG with a 300-kHz BW, the TPDL-SSCG with a 100-kHz BW, and the TPDL-SSCG with a 300-kHz BW, respectively. It shows a 1.26 dB ($=20.95-19.69$) EMI degradation for the case of FN-SSCG with a 300-kHz BW when the $\Sigma\Delta$ modulator noise is taken into consideration, while it is 1.49 dB ($=20.70-20.70$) for the case of TPDL-SSCG with a 300-kHz BW. It is clearly to seen that there is only 0.29 dB ($=20.76-20.76$) impact on the EMI performance for the case of TPDL-SSCG with a 100-kHz BW. Therefore, the jitter introduced by the modulator has a deteriorating effect on the EMI suppression levels.

The impacts of the gain mismatch on modulation ratios and the EMI performance are verified. The cases for $G_m = 0.6$, $G_m = 1.0$, and $G_m = 1.4$ are simulated under different PLL

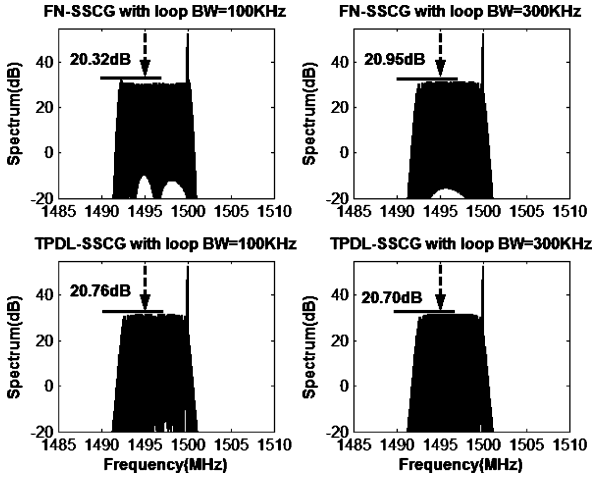

Fig. 10. Spectrum simulation results without the $\Sigma\Delta$ modulator noise for the FN-SSCG and the TPDL-SSCG under different loop bandwidths.

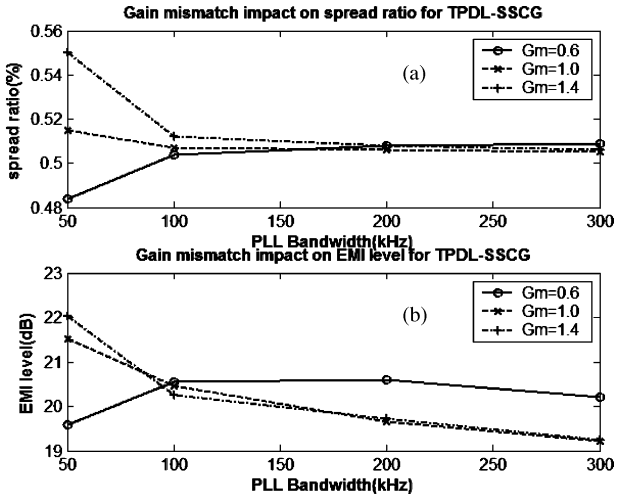

Fig. 11. Simulation results for gain mismatch impact on modulation ratio for the TPDL-SSCG.

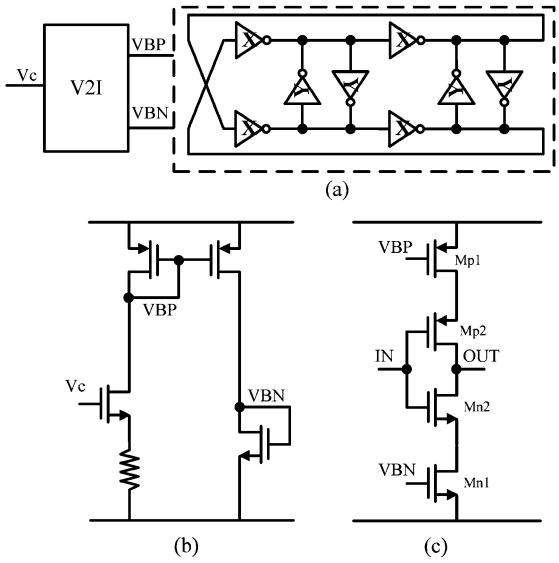

Fig. 12. VCO circuits.

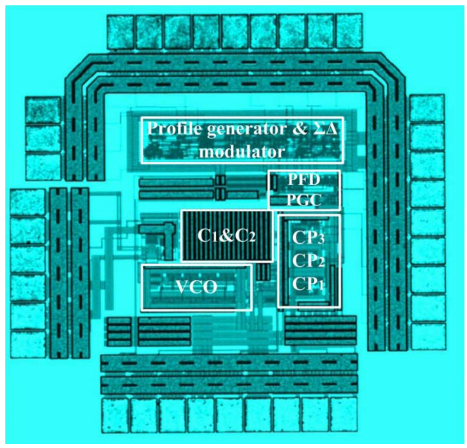

Fig. 13. Die photograph of the proposed TPDL-SSCG.

bandwidths. The impacts on modulation ratios are shown in Fig. 11(a). When the PLL bandwidth is smaller than 100 kHz, the modulation ratio is very sensitive to the gain mismatch between the two points. When the PLL bandwidth is larger than 100 kHz, the modulation ratio variation is small. The impacts on the EMI performance are shown in Fig. 11(b). When $G_m = 1.0$ or $G_m = 1.4$, the higher the PLL bandwidth, the worse the EMI performance is. When $G_m = 0.6$, the EMI reduction performance is less related to the PLL bandwidth. In addition, the EMI variation is sensitive to the gain mismatch when the PLL bandwidth is smaller than 100 kHz. The reason for gain mismatch effects on the proposed SSCG is described later. One can rewrite (8) as

$$\Delta\omega_{\text{out}} = T(s)\Delta\omega_{\text{sig}} + (1 - T(s)) \times G_m \Delta\omega_{\text{sig}}. \qquad (18)$$

The first term in (18) is contributed by the modulation of divider and the second term is contributed by the modulation of the VCO. When the loop bandwidth is quite low, the output is dominated by the second term in (18), meaning that the modulation ratio is sensitive to gain mismatch. In other words, when the loop bandwidth is quite high, the output is dominated by the first term in (18), meaning that the modulation ratio is less sensitive to gain mismatch. But, it is noted from the aforementioned analysis that the EMI performance will be degraded once the loop width is large due to the quantization noise of the modulator. Therefore, if the gain mismatch is small, one can lower the bandwidth to achieve the desired performance according to the aforementioned analysis. If the gain mismatch is high, or more than 0.4, one needs to tradeoff the loop bandwidth with the performance. Thus, in order to reduce the effect of gain mismatch, one can choose an appropriate loop bandwidth to let the first and the third Fourier frequencies of the triangular waveform to be passed through the divider path and to let the fifth and higher Fourier frequencies to be passed through the VCO path. This approach makes the output waveform dominated by the divider modulation path and aided by the VCO modulation path. A rule of thumb of three times the modulating frequency can be the target loop bandwidth. Thus, the 100-kHz loop bandwidth is adopted in this paper.

In short, the advantages of the proposed TPDL-SSCG are remarkable. First, a lower order $\Sigma\Delta$ modulator can be used for lower power consumption. Second, the lower order loop filter

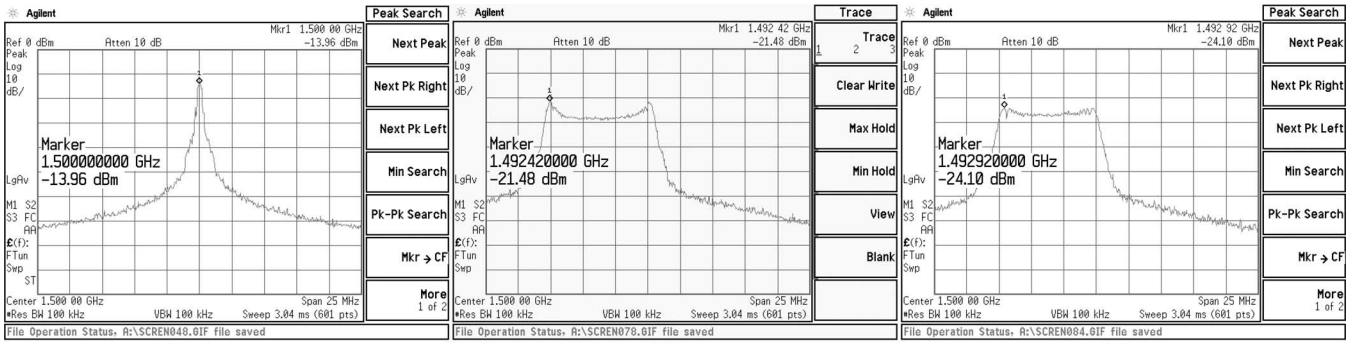

Fig. 14. Measured spectra. (a) Nonspread spectrum mode. (b) Conventional FN-SSCG. (c) Proposed TPDL-SSCG. Measurement condition: RBW = 100 kHz, video BW (VBW) = 100 kHz, and peak-hold mode.

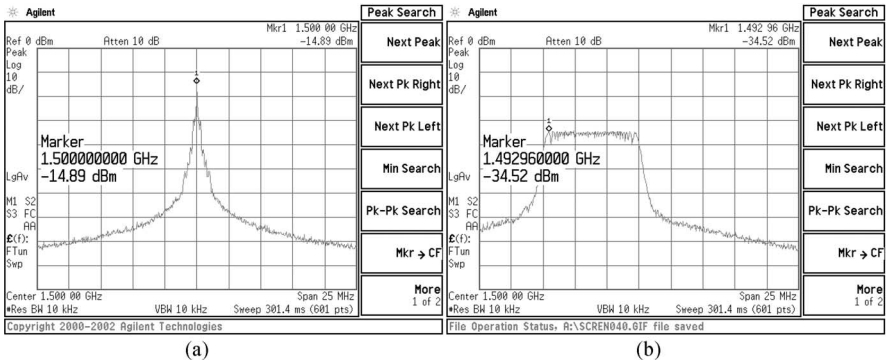

Fig. 15. Measured spectra for the TPDL-SSCG (a) with SSC-OFF (b) with SSC-ON. Measurement condition: RBW = 10 kHz, VBW = 10 kHz, and peak-hold mode.

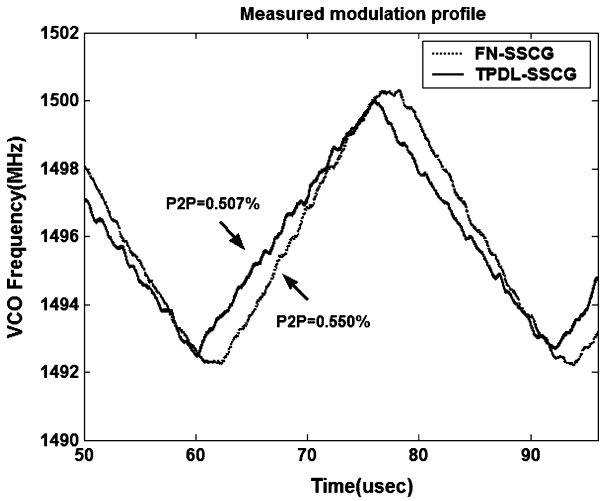

Fig. 16. Measured modulation profile in time domain.

can be used for a smaller chip area. Third, the linear modulation profile and small $\Sigma\Delta$ modulator noise can be optimized simultaneously.

III. Circuit Descriptions

Fig. 12 shows the schematic of VCO used in this paper [17], [18]. It is composed of four current starved inverters (denoted by X) as delay cells, two pairs of cross-coupled current starved inverters (denoted by Y), and a voltage to current converter (V2I). The detailed circuit of the V2I is shown in Fig. 12(b), and the inverters of X and Y are shown in Fig. 12(c). This simple architecture is selected for its large signal swing, which allows better phase noise performance and large tuning range. The cross-coupled inverters have two functions: one is to provide negative impedance to mandate the phase delay in each inverter at 90° and the other is to allow the VCO to operate pseudodifferentially to obtain better power supply rejection ratio (PSRR). In other words, the VCO is a two-stage differential type. The size of inverter Y is suggested to be more than 0.5 times the size of inverter X to maintain oscillation [17]. Here, the factor is 0.7 times to allow a higher oscillation frequency than that of the three-stage single-ended ring oscillator [17] because it has an additional coupling path from the cross-coupled inverters with reduced delay time. Therefore, the power consumption can be relaxed for a given frequency. Moreover, unlike a singled-ended ring oscillator, which produces a distorted triangular waveform output, this topology produces a sinusoidal output, and a more symmetrical waveform, to get better phase noise performance [19]. To further minimize the phase noise, a low VCO gain of 480 MHz/V is chosen to lower the phase noise due to the noise coupling to the VCO input node. The noise of the V2I is also a main contributor to the phase noise. Therefore, the size of the V2I is the same as that in inverter X to lower the up-conversion noise from the bias circuit. The measured phase noise at 1 MHz offset frequency is −89 dBc with a power consumption of 3 mA.

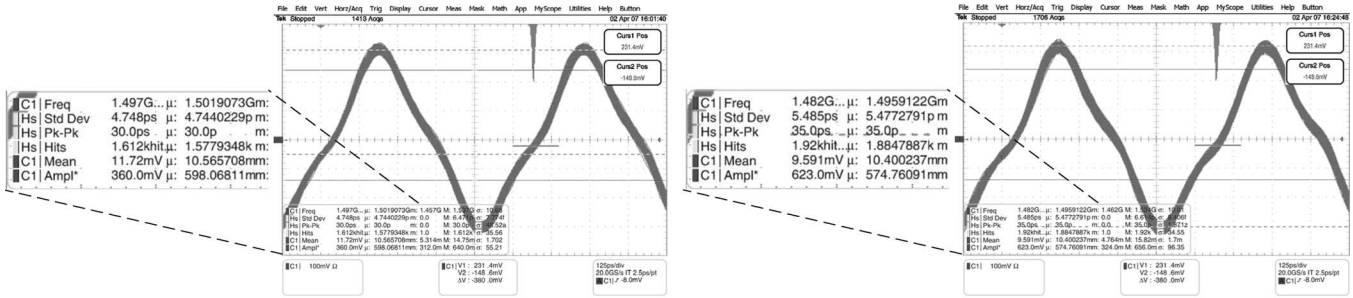

Fig. 17. Measured jitters for the TPDL-SSCG (a) with SSC-OFF and (b) with SSC-ON.

TABLE III
PERFORMANCE SUMMARIES

	This work	[4]	[5]	[3]	Spec.	Unit
Modulation method	Two-point	ΣΔ	ΣΔ	Phase interpolation	N/A	N/A
EMI reduction	10.14	10	9.8	5.43	>7	dB
Modulation frequency	31.25	31.1	30	31.6	30-33	kHz
PLL loop BW	100	300	N/A	N/A	N/A	kHz
RMS jitter	5.485	8.2	3.24	N/A	N/A	ps
Peak-Peak jitter	35.0	N/A	58.3	N/A	N/A	ps
Spread ratios	0.507	0.535	0.5	0.37	0.535	%
Technology	0.18	0.15	0.18	0.15	N/A	µm
Chip Area (active)	0.21	0.42	0.31	N/A	N/A	mm^2
Power consumption	15.3/27*	54	77	N/A	N/A	mW

*15.3mW measured without an output buffer and 27mW measured with an output buffer.

IV. MEASUREMENT RESULTS

The proposed SSCG is designed and fabricated by the TSMC 0.18-μm CMOS process. The die photograph is shown in Fig. 13. The active area is 0.42×0.48 mm^2. The output spectra without spreading, with spreading, using the conventional FN-SSCG, and with spreading using the TPDL-SSCG are shown in Fig. 14(a)–(c), respectively. The resolution bandwidth (RBW) is set to 100 kHz to meet SATA specifications [1]. A second-order loop filter and a PLL bandwidth close to 100 kHz are chosen for both Fig. 14(b) and (c). The second-order extended range MASH $\Sigma\Delta$ modulator is adopted for both Fig. 14(b) and (c). In other words, the conventional FN-SSCG is obtained just by switching off the path of the VCO modulation. The EMI reduction is approximately 7.52 dB for the conventional FN-SSCG and is approximately 10.14 dB for the TPDL-SSCG. The proposed SSCG has 2.62-dB improvements in EMI reduction. The concave shape of the modulation spectra in Fig. 14(b) for the FN-SSCG can be understood due to insufficient loop bandwidth to make the modulation profile more like a sinusoidal waveform. The slightly concave shape of the modulation spectra in Fig. 14(c) for the TPDL-SSCG is due to the addition of the whole sideband harmonics (resulting from the modulation process) falling inside this RBW = 100 kHz even with the triangular modulation profile. Therefore, in order to compare with the simulation results, the RBW needs to be smaller than the modulating frequency [15]. Therefore, the spectra for the TPDL-SSCG, with SSC OFF and ON using 10-kHz RBW, are measured and shown in Fig. 15(a) and (b), respectively. The measured EMI reduction is 19.63 dB and is close to the simulation results of 20.47 dB. No peak appeared in Fig. 15(b), which indicates that the modulation profile is nearly a triangular waveform.

It is difficult to determine the real peak–peak modulation ratio and the shape of the triangular modulation in the frequency domain. Therefore, the time-domain modulation profile is verified in Fig. 16. The solid line and dashed line represent the profile of the proposed TPDL-SSCG and the profile of conventional FN-SSCG, respectively. The measured modulation ratios are 0.55% and 0.507% for the conventional FN-SSCG and the TPDL-SSCG, respectively. The measured modulation ratio of the TPDL-SSCG is very close to the simulation results, 0.506%, listed in Table II. The measured modulation profile for the conventional FN-SSCG looks like a distorted triangular waveform due to the insufficient PLL bandwidth; therefore, the EMI performance is bad. The measured jitter, using a self-triggered method under different conditions, is shown in Fig. 17. The measured rms jitter is 4.748 and 5.485 ps at SSC-OFF and SSC-ON, respectively. The measured peak-to-peak jitter is 30 and 35 ps at SSC-OFF and SSC-ON, respectively. Only a 0.737-ps rms jitter is increased when the TPDL-SSCG is active, which is very close to the theoretical estimation of 0.556 ps (=0.5%/1500 MHz/6). Therefore, the rms jitter caused by the nonideality of the circuits (mostly from the $\Sigma\Delta$ modulator) is only 0.181 ps. The power consumptions with and without an output buffer are 15.3 and 27 mW, respectively. The lower power consumption is achieved due to the low-power VCO and the low-order $\Sigma\Delta$ modulator. Table III summarizes the performance of the proposed TPDL-SSCG and compares with previous work. In Table III, the EMI reduction amounts are compared for the 100-kHz RBW. Note that the proposed TPDL-SSCG results in smaller area, lower power consumption, and better peak-to-peak jitter performance. The EMI performance is comparable to other works.

V. Conclusion

In this paper, a new SSCG architecture with TP modulation is presented. The PLL bandwidth is effectively expanded to improve the modulation waveform. The modulation ratio can be finely controlled by a simple DAC. The most important success is the usage of the second-order $\Sigma\Delta$ modulator and the second-order DL, which remarkably reduce power consumption and chip area without the jitter penalty. In addition, the total integration is realized without using an external loop filter or a high-resolution DAC. The clock rate of 1.5 GHz with a down-modulation ratio of 0.5% is achieved. The jitter at SSC-ON is 5.485-ps rms and 35-ps peak-to-peak with only a 0.737-ps rms jitter attributed from spread spectrum clocking. The improvement in EMI reduction is better than 2.62 dB with respect to a conventional one-point implementation.

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References

[1] *Serial ATA Revision Specification 2.5* (2005, Oct.). Serial ATA International Organization. [Online]. San Francisco, CA. Available: https://www.sata-io.org

[2] M. Sugawara, T. Ishibashi, K. Ogasawara, M. Aoyama, M. Zwerg, S. Glowinski, Y. Kameyama, T. Yanagita, M. Fukaishi, S. Shimoyama, T. Ishihashi, and T. Noma, "1.5-Gb/s 5150-ppm spread-spectrum SerDes PHY with a 0.3-mW1.5-Gb/s level detector for serial ATA," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2002, pp. 60–63.

[3] M. Aoyama, K. Ogasawara, M. Sugawara, T. Ishibashi, T. Ishibashi, S. Shimoyama, K. Yamaguchi, T. Yanagita, and T. Noma, "3 Gb/s, 5000 ppm spread spectrum SerDes PHY with frequency tracking phase interpolator for serial ATA," in *Proc. Symp. VLSI Circuits*, Jun. 2003, pp. 107–110.

[4] M. Kokubo1, T. Kawamoto1, T. Oshima, T. Noto, M. Suzuki, S. Suzuki, T. Hayasaka, T. Takahashi, and J. Kasai, "Spread-spectrum clock generator for serial ATA with multi-bit $\Sigma\Delta$ modulator-controlled fractional PLL," *ICICE Trans. Electron.*, vol. E-89C, no. 11, pp. 1682–1688, Nov. 2006.

[5] H. R. Lee, O. Kim, G. Ahn, and D. K. Jeong, "A low-jitter 5000 ppm spread spectrum clock generator for multi-channel SATA transceiver in 0.18 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2005, pp. 162–163.

[6] W. T. Chen, J. C. Hsu, H. W. Lune, and C. C. Su, "A spread spectrum clock generator for SATA-II," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, vol. 3, pp. 2643–2646.

[7] Y. Moon, G. Ahn, H. Choi, N. Kim, and D. Shim, "A quad 6 Gb/s multi-rate CMOS transceiver with TX rise/fall-time control," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2006, pp. 233–242.

[8] K. B. Hardin, J. T. Fessler, and D. R. Bush, "Spread-spectrum clock generation for the reduction of radiated emissions," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Aug. 1994, pp. 227–231.

[9] Y. B. Hsieh and Y. H. Kao, "A fully integrated spread spectrum clock generator using two-point delta-sigma modulation," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2007, pp. 2156–2159.

[10] Y. B. Hsieh and Y. H. Kao, "A new spread spectrum clock generator for SATA using double modulation schemes," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2007, pp. 297–300.

[11] K. C. Peng, C. H. Huang, C. J. Li, and T. S. Horng, "High-performance frequency-hopping transmitters using two-point delta–sigma modulation," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 11, pp. 2529–2535, Nov. 2004.

[12] S. Pavan, Y. Tsividis, and K. Nagaraj, "Modeling of accumulation MOS capacitors for analog design in digital VLSI processes," in *Proc. IEEE Int. Symp. Circuits Syst.*, Jun. 1999, vol. 6, pp. 202–205.

[13] Y. B. Hsieh and Y. H. Kao, "A spread-spectrum clock generator using fractional-N PLL with an extended range $\Sigma\Delta$ modulator," *ICICE Trans. Electron.*, vol. E-89C, pp. 851–857, 2006.

[14] D. S. Kim and D. K. Jeong, "A spread spectrum clock generation PLL with dual-tone modulation profile," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2005, pp. 96–99.

[15] Y. Matsumoto, K. Fujii, and A. Sugiura, "An analytical method for determining the optimal modulating waveform for dithered clock generation," *IEEE Trans. Electromagn. Compat.*, vol. 47, no. 3, pp. 577–584, Aug. 2005.

[16] M. H. Perrott, T. L. Tewksbury,III, and C. G. Sodini, "A 27-mW CMOS fractional-N synthesizer using digital compensation for 2.5-Mb/s GFSK modulation," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2048–2060, Dec. 1997.

[17] K.-H. Kim, Y.-S. Sohn, C.-K. Kim, M. Park, D.-J. Lee, W.-S. Kim, and C. Kim, "A 20-Gb/s 256-Mb DRAM with an inductorless quadrature PLL and a cascaded pre-emphasis transmitter," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 127–134, Jan. 2006.

[18] D. A. Badillo and S. Kiaei, "A low phase noise 2.0V 900 MHz CMOS voltage controlled ring oscillator," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2004, vol. 4, pp. IV-533–IV-536.

[19] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jan. 1999.

[20] Y. Koo, H. Huh, Y. Cho, J. Lee, J. Park, K. Lee, D.-K. Jeong, and W. Kim, "A fully integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and cellular-CDMA wireless systems," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 536–542, May 2002.

[21] H. H. Chang, I. H. Hua, and S. I. Liu, "A spread-spectrum clock generator with triangular modulation," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 673–676, Apr. 2003.

[22] T. Kawamoto1, T. Takahashi, H. Inada, and T. Noto, "Low-jitter and large-EMI-reduction spread-spectrum clock generator with auto-calibration for serial-ATA applications," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2007, pp. 345–348.

[23] J. Balcells, A. Santolaria, A. Orlandi, D. Gonzalez, and J. Gago, "EMI reduction in switched power converters using frequency modulation technique," *IEEE Trans. Electromagn. Compat.*, vol. 47, no. 3, pp. 569–576, Aug. 2005.

[24] Y. B. Hsieh and Y. H. Kao, "A fully integrated spread spectrum clock generator by using direct VCO modulation," *IEEE Trans. Circuits Syst. I, Reg. Paper*, vol. 55, no. 7, pp. 1845–1853, Aug. 2008.

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