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Editorial

Special issue on cellular wave computing architectures, Part II

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In this second part of our Special Issue, five papers are presented all related to hardware implementations. In some way, this reflects also the growing importance of the cellular architectures where the geometric address of a processor and the local precedence is becoming a key factor. We are witnessing a proliferation of thousand processing core chips, both digital and mixed mode, as well.

In these new array processor chips, including champions like the 25 kilo-processor visual microprocessor (AnaFocus Ltd.), as well as the 1kilo-DSP slice FPGA (Xilinx Co.), the geometric address of a processor cell or core is an important parameter since the locality has a speed precedence. It is not surprising that according to the latest issue of the International Technology Roadmap for Semiconductors (ITRS), among the emerging architectures, CNN Technology is defined as one of the most actively studied area. Indeed, including the various physical implementations of the Cellular Wave Computers (mixed mode, digital, optical, etc.) this architecture shows the natural ingredients required by the sub-100nm CMOS physical limitations and possibilities.

In the first paper by P. Arena *et al.*, the winnerless competition paradigm in a Lotka–Volterra system is used and extended in a spatial–temporal setting to design a CNN dynamics for learning, and its efficient use is shown in an actual navigation task. Synchronization phenomenon is a major promise to detect complex spatial–temporal events. The second paper by Á. Tar *et al.* shows a test-bed composed of Chua's circuit cells in a CNN array, and an actual hardware implementation is used to show the operation including the discovery of novel spatial–temporal synchronization phenomena. A key problem in mixed-mode implementation of programmable spatial–temporal diffusion, via a linear A template, is the robustness. In the third paper, J. Fernández-Berni and R. Carmona Galán show the limitations of classical transconductance amplifier-based designs, and suggest alternative solutions. Fluid flow problems are the most computational-intensive problems

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in digital computing since the invention of the computer. In the paper by S. Kocsárdi *et al.* fluid flow simulation is implemented via the CNN Universal Machine on FPGAs. Finally, an interesting FPGA implementation problem is shown by Á. Rák *et al.* for stochastic bit streams.

We do hope that this second part of the Special Issue adds a lot of insight into the Cellular Wave Computing implementation, and shows a few original algorithmic solutions as well.

