A Fully Integrated Spread Spectrum Clock Generator Using Two-Point Delta-Sigma Modulation

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***Abstract*—A new spread spectrum clock generator (SSCG) using two-point delta-sigma modulation is presented in this paper. Not only the divider is varied, but also the voltage controlled oscillator is modulated. This technique can enhance the modulation bandwidth so that the effect of EMI suppression is improved. In addition, the method of two-path is applied to the loop filter to reduce the capacitance value such that the total integration can be achieved. The proposed SSG has been fabricated in a 0.35um CMOS process. The clock of 400MHz with center spread ratios of 1.25% and 2.5% are verified. The size of chip area is 0.90×0.89mm^2.**

I. INTRODUCTION

Spread-spectrum clock generators (SSCG) have been widely employed as high-speed sources with reduced EMI levels [1]-[7]. Basically, SSCG is a phase locked loop (PLL) with special case of frequency modulation. There are two kinds of modulation techniques employed in PLLs. One is to control the variation of the divider and the other is to modulate the VCO directly. In the former case a fractional-N PLL with a ΣΔ modulator is mostly used [1]-[7]. It has the advantage of being fully digital controlled. The modulator is controlled by a triangular wave generator. The loop bandwidth is traded off between modulation profile and jitter caused by ΣΔ modulator. As the loop bandwidth is not wide enough, the modulation profile is distorted and the effect of EMI suppression is reduced. The method of distorted triangle waveform has been presented to improve the modulation profile [8]. Here, the method of two-point modulation is presented to enhance the bandwidth and, in the meantime, maintain the linear saw-tooth waveform.

Actually two-point modulation in PLL has been used in the frequency generator with DC-FM feature. The transfer function appears as all-pass behavior with fine parameter adjustment. Recently, this technique is employed in frequency hopping spread-spectrum systems (FHSS) [9]. In this study, a modified SSCG with two-point modulation with dual-path loop filter (TPDL-SSCG) is presented to achieve wide bandwidth and full integration.

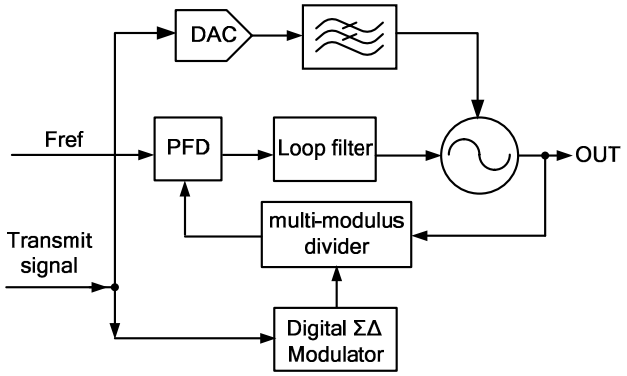

Figure 1. The typical TPDSM architecture [9]

II. PROPOSED TPDL-SSCG

The typical architecture of two-point modulation is shown in Fig. 1. There are two modulation points. One point is at the input of multi-modulus divider through the ΣΔ modulator. The other point is at the input of VCO through a DAC and a reconstruction filter. Usually a high resolution DAC is needed to achieve better performance due to the small modulation amplitude appeared at the input of VCO. It means high power consumption and has large area penalty. To achieve the total integration, the architecture is modified. The block diagram of proposed TPDL-SSCG is shown in Fig. 2 with a PFD, a dual path loop filter, a VCO, a 8-bit programmable counter (PGC), a digital ΣΔ modulator, a modulation profile generator, and a proposed DAC. The dual-path loop filter [10] consists of CP_1, CP_2, C_1, C_2, R_1, and a unity-gain amplifier. The proposed DAC consists of a digital slicer, CP_3, and C_1. The modulation profile generator produces a digital triangular wave, F_{sig}, to feed into the digital ΣΔ modulator and the digital slicer simultaneously. The digital slicer slices the triangular wave into a digital clock. Then, the digital clock charges and discharges the C_1 through the CP_3 to finish digital to analog conversion. Because the digital slicer, the modulation profile generator

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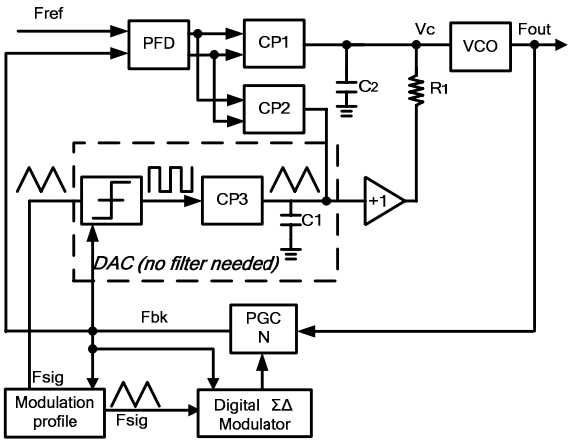

Figure 2. The block diagram of TPDL-SSCG

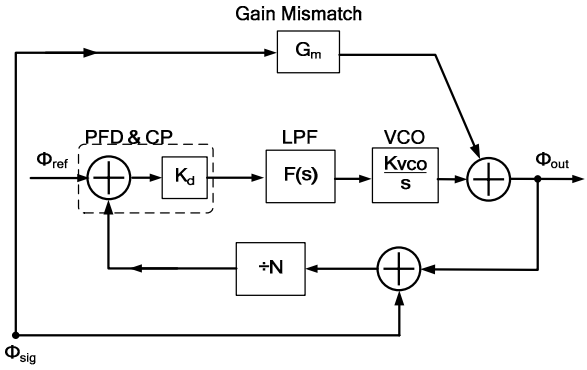

Figure 3. Linear model of TPDL-SSCG

and the digital ΣΔ modulator use the same clock domain, F_{bk}, the output of digital slicer can be tracked with triangular wave very well and the delay mismatch between two points can be eliminated.

Assume that I_{p3} is the current of CP_3. Ignoring CP_1 and CP_2, the relation between VCO controlled voltage V_c and I_{p3} is

$$\frac{V_c}{I_{p3}} \approx \frac{1}{sC_1} \tag{1}$$

under the condition of $F_{sig} << 1/(2\pi R_1 C_2)$. According to (1), the analog modulation signal (the analog triangular wave) is created as I_{p3} is a square wave. Here C_1 with one grounded terminal is implemented by the accumulation MOS capacitor to save area and has good distortion performance when the gate-source bias voltage is equal to or large than 1V [13]. The relation between I_{p3} and spreading ratio δ% is predicted as

$$\delta\% = \frac{I_{p3} K_{vco}}{2C_1 f_m f_c} \tag{2}$$

where f_c is nominal output frequency, f_m is the modulation frequency of the triangle wave and K_{vco} is the conversion gain of VCO.

The linear model of TPDL-SSCG is shown in Fig. 3. Φ_{out} is the phase of output signal F_{out}. Φ_{sig} is the phase of modulation signal. G_m is the gain factor for compensation between two modulation points. According to (2), the gain mismatch comes from the process variation of K_{vco}, I_{p3}, and C_1. Here the delay mismatch is assumed to be ignored due to the proposed DAC architecture. K_d is gain of the PFD and charge pump. F(s) is dual-path loop filter transfer function. The divider value is N. Assume that I_{p1} is the current of CP_1, I_{p2} is the current of CP_2 and $I_{p1}=BI_{p2}$. Here B=4. Ignoring the loading of CP_3, we can get the following relationship.

$$F(s) = \frac{V_c}{I_{p1}} = \frac{R_1\left(s + \frac{1}{R_1 B C_1}\right)}{s\left(1 + sR_1 C_2\right)}. \tag{3}$$

From (3), the zero is at $1/(BC_1)R_1$. Obviously, the magnitude of capacitance C_1 can be reduced by the factor B. It is a favor for total integration. The closed loop transfer function of Fig. 3 can be derived as

$$\frac{\Phi_{out}}{\Phi_{sig}} = \frac{K_{vco}K_d F(s)}{Ns + K_{vco}K_d F(s)} + \frac{Ns}{Ns + K_{vco}K_d F(s)} \times G_m. \tag{4}$$

The first term in the right hand side appears as a low pass and second term appears as a high pass as F(s) in (3) is taken into account. From (4), Φ_{out} is equal to Φ_{sig} if $G_m=1$. It means that if there are no any mismatches between two modulation points, the output signal can be modulated without distortion and bandwidth limitation.

The behavior simulation results by Matlab are shown in Fig. 4. The simulation condition is that the output frequency is 400MHz with the spread ratio of 2.5%, the modulation frequency is 40KHz, and the loop bandwidth is about 70KHz. The solid line represents the traditional SSCG using fractional-N PLL. The dashed line represents the proposed TPDL-SSCG. From the simulation, we can see clearly the advantage of TPDL-SSCG that the distortion is less than the traditional one, and the modulation profile is more like a

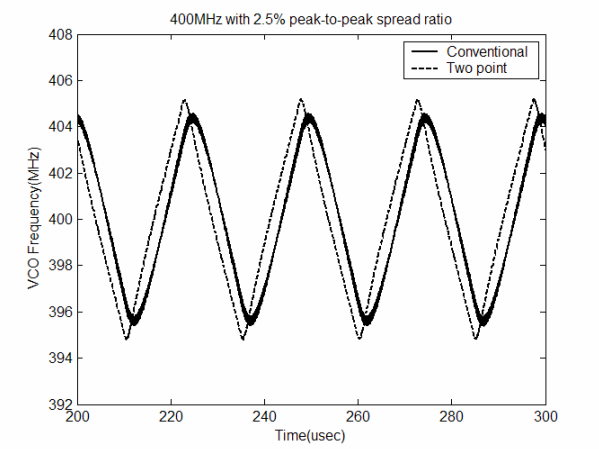

Figure 4. Simulation results of tranditonal SSCG and TPDL-SSCG.

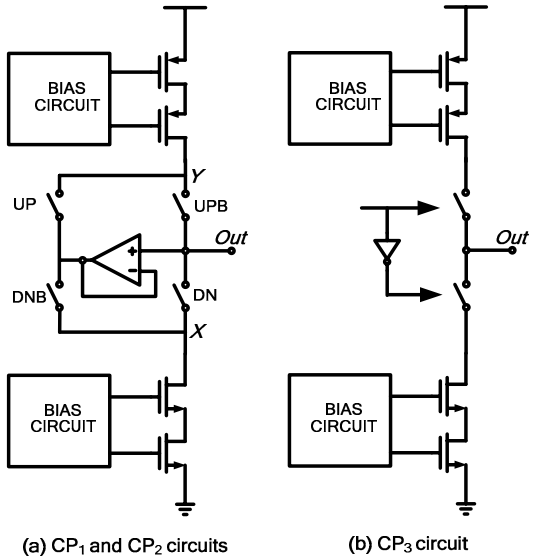

Figure 5. (a) CP_1 and CP_2 circuits and (b) CP_3 circuit

triangular wave even when the loop bandwidth is not wide enough.

III. Circuit Descriptions

The circuits used in the work are described briefly next. The charge-pump of $CP_{1(2)}$ and CP_3 are shown in Fig. 5(a) and 5(b), respectively. The cascoded current sources with wide-swing bias circuit in Fig. 5 are employed for good immunity against the power supply noise. The controlling signals for UP, UPB, DN and DNB switches are fed from the outputs of PFD. The input of CP_3 is from the output of digital slicer. A unity-gain buffer for CP_1 and CP_2 is used to reduce the charge sharing when switching. The unity-gain buffer is not needed for CP_3 due to the low input frequency. The low jitter wide band VCO [11] with sharp output waveform and full swing is employed here. The MASH-1-1 ΣΔ modulator with extended input range [7] is used here due to the advantage of unconditional stability, small area and wide input range.

IV. Measurement Results

The TPDL-SSCG is designed and fabricated by TSMC 0.35um single-poly quadruple-metal CMOS process. The die photograph is shown in Fig. 6 with area equal to 0.90×0.89 mm^2. The output spectrum without spreading is shown in Fig. 7(a) with clock speed at 400MHz. The amplitude of the peak is 3.30dBm. The output spectrum using traditional SSCG with 2.5% spread ratio is shown in Fig. 7(b). The amplitude is reduced to -14.73dBm. The peak reduction is about 18.03dB compared to that in Fig. 7(a). There exist two small peaks at two edges due to insufficient loop bandwidth. The output spectrum using the proposed TPDL-SSCG with the same spread ratio is shown in Fig. 7(c). The amplitude is -16.43dBm. The peak reduction factor is about 19.73dB compared to that in Fig. 7(a). The proposed TPDL-SSCG has 1.70dB improvement in EMI reduction. Table I gives the performance summary of TPDL-SSCG

V. Conclusion

In this study, the spread spectrum clock generator with two-point modulation is presented. The modulation bandwidth is effectively expanded with two-point modulation. The modulation profile is improved to be nearly linear. In the meantime the total integration without external loop filter and a high resolution DAC is realized. The improvement of EMI reduction is better than 1.70dB with respect to the conventional one.

Acknowledgment

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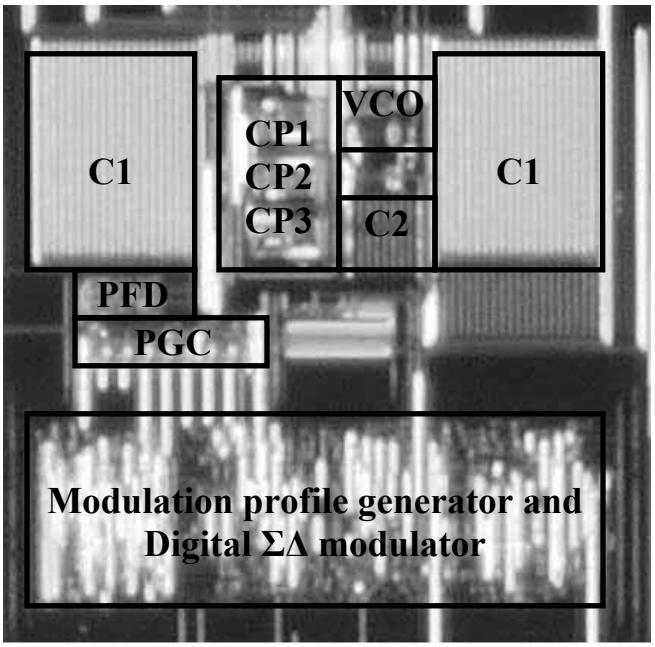
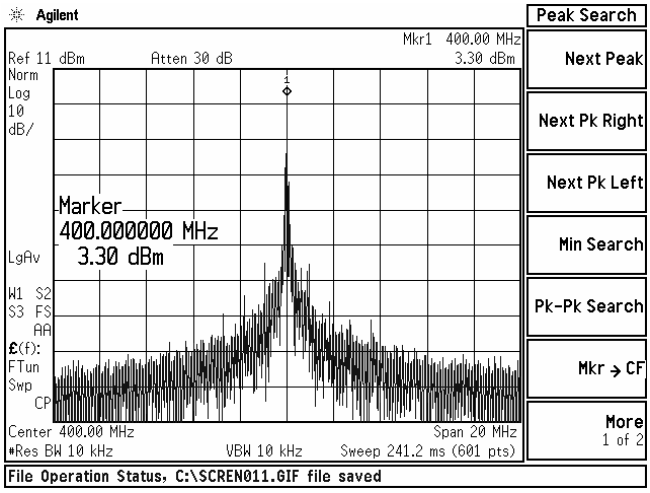


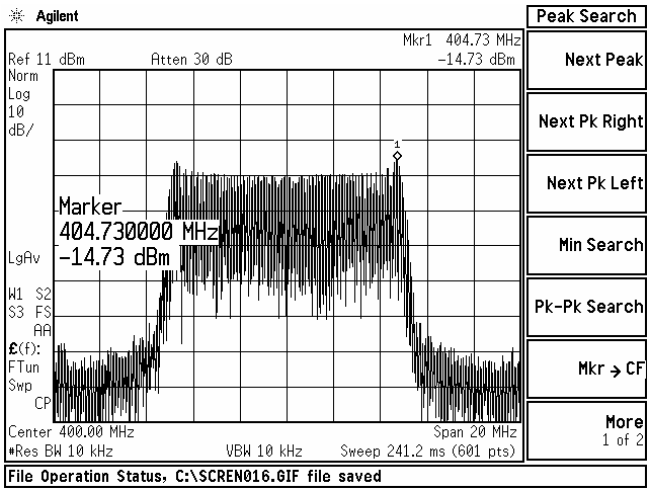
Figure 6. Die photograph of the proposed TPDL-SSCG

TABLE I. Performance Summary

Modulation Method	Two point
Modulation Type	Center-spread
Modulation Frequency	40KHz
Spread Ratios(pp)	1.25%, 2.5%
Output Frequency	400MHz
Input Frequency	14.31818MHz
Loop bandwidth	~70KHz
Loop filter	R1=12KΩ C1=400pF C2=40pF
EMI reduction	19.73dB @ 2.5% center spread ratio
Chip Area (active)	0.90x0.89 mm^2
Power Dissipation	33mW including output buffer @ 3.0V



(a)



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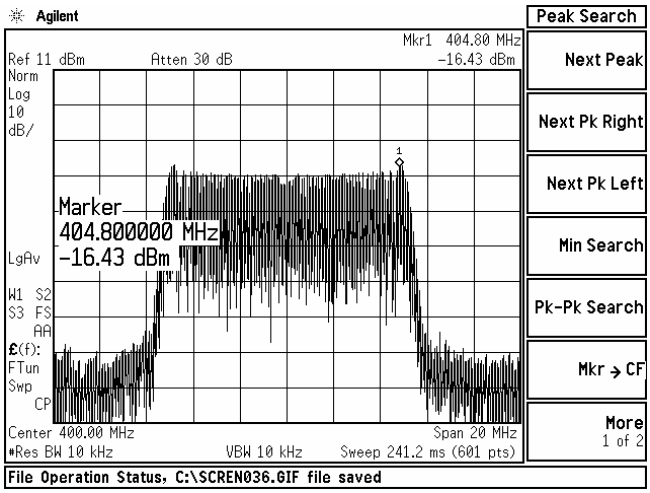

(c)

Figure 7. Measured spectra of 400MHz output frequency (a) at non-spread spectrum mode, (b) of traditinal SSCG with 2.5% spread ratio, and (c) of TPDL-SSCG with 2.5% spread ratio.

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