

國立交通大學

光電系統研究所

碩士論文

氣含量對非晶態透明半導體銦鋅錫氧薄膜電晶  
體特性之研究



**Study on the effect of oxygen incorporation on amorphous  
Indium Zinc Tin Oxide transparent thin film transistors**

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中華民國一零二年八月

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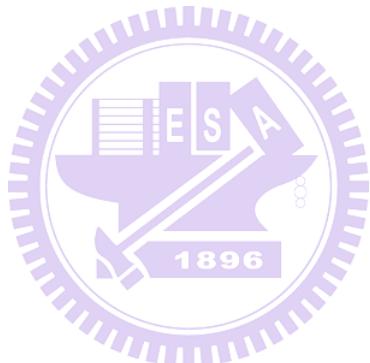
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## 摘要

近年來非晶態透明導電膜因具備高透光性與高電流驅動特性而受到矚目，而為了減少材料中稀有金屬的使用及提高載子遷移率的需求，我們研究了新材料 indium-zinc-tin oxide(IZTO)，對非晶態的 IZTO 電晶體進行電特性與材料特性的探討與分析。a-IZTO 的光學能隙高達 3.6eV 以上，僅會吸收波段小於 360nm 的紫外光，在可見光的波段具有高穿透性，再者 a-IZTO 在製程上可達到低退火溫度( $300^{\circ}\text{C}$ )與具有高載子移動率等優點，所以極有潛力成為下一代的主流顯示技術。

本研究中，探討不同氧含量的薄膜做為主動層對元件特性的影響，由實驗結果得知，微量的氧能修補薄膜內的缺陷進而達到優化的效果，然而薄膜內的缺陷態卻會隨著氧含量的增加而增加，而載子移動率隨之下降，再者，此實驗中

優化的元件在經過低溫退火後的最高載子移動率可達  $15 \text{ cm}^2/\text{V. s}$ ~ $20 \text{ cm}^2/\text{V. s}$ 。為了能進一步應用在平面顯示器上，我們將此最佳化的條件成功轉移於具可撓曲淺力之超薄(0.13mm)玻璃基板上，實驗結果顯示電晶體依舊能維持不錯的元件特性(載子移動率- $12\sim 13 \text{ cm}^2/\text{V. s}$ )。a-IZTO 具有高載子移動率與應用於可撓曲超薄玻璃基板之優勢，此研究的發展將極具淺力。



# **Study on the effect of oxygen incorporation on amorphous Indium Zinc Tin Oxide transparent thin film transistors**

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Recently, the thin film transistors (TFTs) with transparent amorphous conductive thin film as active layer perform higher mobility and better reliability than conventional hydrogenated amorphous silicon TFT (a-Si: H TFT). In addition, the uniformity of a-IGZO TFT is also superior to low temperature polycrystalline silicon TFT (LTPS TFT). However, the usage of the rare element(Ga) and further enhancement of device mobility will be an important issue for the long-term applications. In this work, we developed new amorphous oxide semiconductor--- amorphous Indium Zinc Tin Oxide (a-IZTO) TFTs.

phous In-Zn-Sn-O thin film transistors (a-IZTO TFTs). We investigated the effect of oxygen incorporation on a-IZTO thin film transistors. For the devices with different oxygen flow rate incorporation, the small quantity of oxygen can repair defects and optimize the characteristic, however, the trap states increase when oxygen flow rate increases, leading to the decreasing mobility. Moreover, the mobility of the optimized devices after annealing has reached  $15 \text{ cm}^2/\text{V.s} \sim 20 \text{ cm}^2/\text{V.s}$ . For the application of flat panel displays, we have successfully transferred the optimized device from Si wafer to the ultra thin glass (0.13mm) which has bending potential. Devices on ultra thin glasses have stable basic electrical characteristics and their mobilities were also comparable ( $12 \sim 13 \text{ cm}^2/\text{V.s}$ ). With the advantages of high mobility and ultra thin glass, these results show the future application potentials of a-IZTO TFT devices on flat panel display technology.

## Acknowledgements (誌謝)

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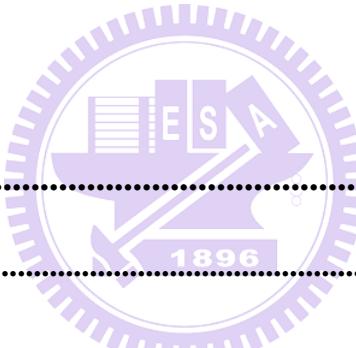
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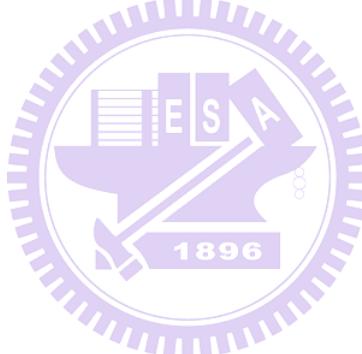
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# Chapter 1

## Introduction

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### 1.1 General Background

Thin-film transistors (TFTs) are fundamental building blocks and play a domination role for state-of-the-art microelectronics, such as flat-panel displays and system-on-glass. Furthermore, the fabrication of low-temperature TFTs will allow flexible large-area electronic devices to be developed. As shown in Fig.1-1, these devices are flexible, lightweight, shock resistant and potentially affordable—properties that are necessary for large, economic, high-resolution displays, wearable computers and paper displays [1]. Research on amorphous semiconductors started in 1950s to seek appropriate materials. And hydrogenated amorphous silicon (a-Si:H) is the first material which can control carrier concentration by impurity doping as in crystalline. Nowadays, the a-Si:H which is used widely in active-matrix flat-panel display (AMFPD) circuits. However, the growth of high-end commercial market with high-resolution such as ultra definition (2000x4000), high frame rate(>120Hz), and size larger than 50 in. necessitates the development of high-performance transistors (with field-effect mobility  $>3\text{cm}^2/\text{V.s}$ ).[2]

Hydrogenated amorphous silicon thin film transistor (a-Si:H TFT) is not an appropriate device for next generation displays on account of its low mobility ( $< 1 \text{ cm V}^{-1} \text{ s}^{-1}$ ), photo sensitivity (low band gap about 1.7ev) and rather high deposition temperature( $\sim 400^\circ\text{C}$ ). On the other hand, polycrystalline silicon (poly-Si) TFT which has high mobility ( $> 100 \text{ cm V}^{-1} \text{ s}^{-1}$ ) suffers from a problem with the variation of electrical properties due to grainy[ 3-4].The mobility of a-Si:H ( $\sim 1 \text{ cm}^2(\text{Vs})^{-1}$ ) is much smaller than that of single crystalline Si ( $\sim 200 \text{ cm}^2(\text{Vs})^{-1}$ ) due to the intrinsic chemical bonding nature. The average carrier transportation paths in covalent semiconductors, such as a-Si:H, consist of strongly directive  $\text{sp}^3$  orbital. The bond angle fluctuation significantly alters the electronic levels, causing high density of deep tail-states, as shown in Fig.1-2 [ 5]. In contrast, degenerate band conduction and large mobility ( $> 10 \text{ cm}^2/\text{V.s}$ ) are possible in amorphous oxide semiconductors (AOs) containing post-transition-metal cations. These features are completely different from those of the covalent semiconductors. Figure 1-2 illustrates the carrier transport paths in AOs. The bottom of the conduction band in the oxide semiconductors that has high ionicity is primarily composed of spatially spread metal ns orbitals with isotropic shape (here n is the principal quantum number), and direct overlap among the neighbouring metal ns orbitals is possible. The magnitude of this overlap is insensitive to distorted metal–oxygen–metal (M–O–M) chemical bonds that intrinsically exist in amorphous materials. Therefore, AOs exhibit Hall-effect mobilities similar to those of the corresponding crystalline phase, even if they are

formed at room temperature. These carrier transport properties are unique to oxide semiconductors, and are not seen in covalent amorphous semiconductors such as a-Si:H[1].

## **1.2 Amorphous Oxide Semiconductors**

### **1.2.1 Introduction of Amorphous Oxide Semiconductors**

Amorphous oxide semiconductors (AOSs) are expected as new channel materials in thin-film transistors (TFTs) for large-area and/or flexible flat-panel displays and other giant-microelectronics devices. So far, many prototype displays have been demonstrated in these four years since the first report of AOS TFT. The most prominent feature of AOS TFTs is that they operate with good performances even if they are fabricated at low temperatures without a defect passivation treatment. The TFT mobilities exceed  $10 \text{ cm}^2/\text{V.s}$ , which are more than ten times larger than those of conventional amorphous semiconductor devices.[6]

### **1.2.2 Material properties of zinc oxide (ZnO)**

Thin film transistors (TFTs) made with amorphous and poly silicon have become in the last 10 years the key point of the electronic flat panel display industry, just as silicon chips were earlier called the staple of the electronic computer revolution.[7] Very recently ZnO-based thin-film transistors (TFTs) have been reported to be drawing interest from researchers. It is because those TFTs may achieve the following important goals: depositing channel layer on a

flexible substrate through low temperature processes, realizing transparent TFTs and achieving extra functions such as photodetections using ZnO channel. Moreover, since deposited ZnO usually maintains a crystalline phase, although the deposition process is carried out even at room temperature, ZnO-based TFT probably exceeds a conventional amorphous Si TFT in terms of field effect mobility.[8-9] The combination of transparency, high mobility, and room temperature processing makes the ZnO-TFT a very promising low-cost optoelectronic device for the next generation of invisible and flexible electronics, such as switching for addressing AMOLED.[10]



### 1.3 Motivation

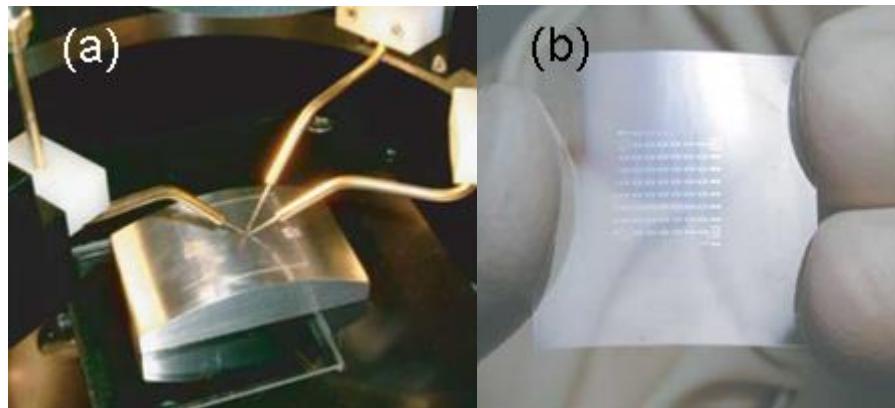
Transparent conducting oxides (TCOs) have both good optical transparency (in thin films) and high electronic conductivity ( $> 10^4$  S/cm).[11] Nevertheless, it is noted that the ZnO thin film can be very easily crystallized during the deposition process, leading to the formation of grain boundary defects. In 2004, Hosono et al explored a new class of amorphous oxide semiconductors based on InGaZnO (indium gallium zinc oxide, IGZO) and demonstrated that high-performance transistors ( $\mu_{FE} \sim 8.3$  cm $^2$  (Vs) $^{-1}$ ) can be fabricated using the IGZO thin film deposited even at room temperature. And now, a-IGZO is one of the most popular materials on active layer for flat panel display. [12] The mobility of the IGZO TFT is around 10 cm $^2$ V $^{-1}$ s $^{-1}$ , further improvement of the mobility is required for super high-definition display

or circuit integration in the displays.[13] On the purpose of mobility enhancement and rare element replacement, we investigated the InSnZnO as one candidate for achieving high  $\mu$  oxide TFTs and with no rare element (Ga). Amorphous InSnZnO (a-IZTO) is a promising candidate for substituting the indium tin oxide (ITO) due to its high optical transparency, good conductivity and high work function.[27] In former studies, a-IZTO films were generally analyzed with different deposition and annealing condition, few research has concerned the influence of oxygen incorporation on a-IZTO thin film. In our experiment, we investigated the effect of oxygen incorporation in a-IZTO thin film, changing the oxygen flow rate in order to improve the thin film quality.



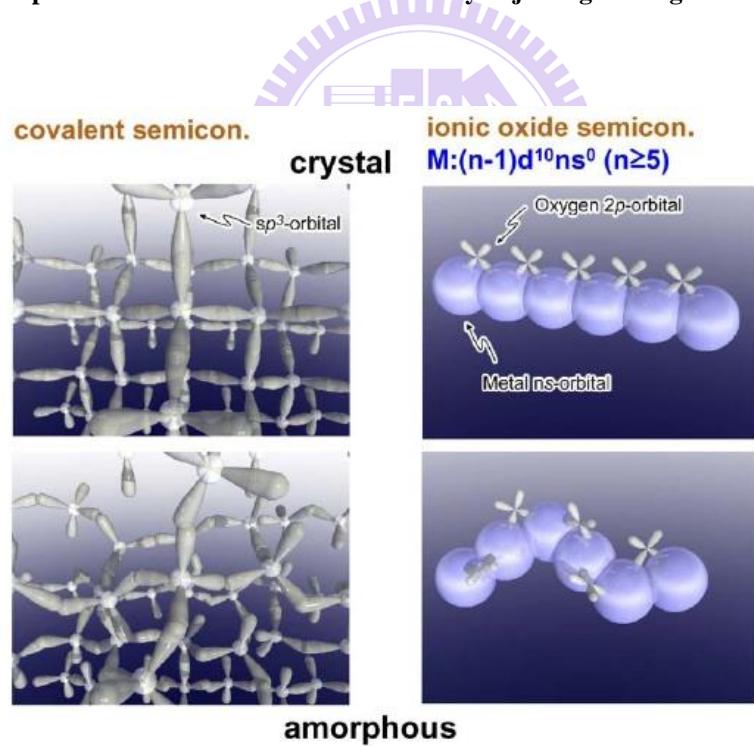
#### 1.4 Thesis Organization

This thesis is divided into four chapters. In **Chapter 2**, the measurement and extraction of electrical parameters are introduced. The fabrication flow of a-IZTO thin film transistors is also described. In **Chapter 3**, the electrical and material properties of a-IZTO films are presented. First, the oxygen effects and different thickness on a-IZTO TFTs is discussed. Second, Reliability analysis of a-IZTO TFTs with different oxygen flow rate are also presented. Third, photosensitivity characteristic of a-IZTO TFTs with different oxygen flow rate is investigated. Finally, conclusions and future works are summarized in **Chapter 4**.



K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* 432 488 (2004)

**Fig.1- 1 Flexible transparent TFTs (TIFTs)** (a) A photograph of the flexible TFT sheet bent at  $R = 30$  mm. The TFT sheet is fully transparent in the visible light range (b) a photograph of the flexible TFT sheet. The transparent TFT devices are made visible by adjusting the angle of the illumination



K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* 432 488 (2004)

**Fig.1- 2 Schematic orbital drawing of electron pathway (conduction band bottom) in conventional silicon-base semiconductor and ionic oxide semiconductor.**

# Chapter 2

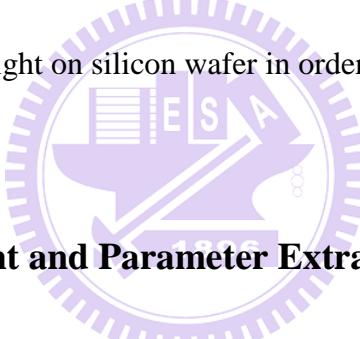
## Experimental Procedures

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### 2.1 Fabrication flow of thin film transistors

Fig.2-1 is the flow path in my experiment. We did both material and electric analysis to analyze our a-IZTO TFTs. Because of the innovation of sputter, the active layer with several channel thickness were formed by RF reactive sputter at room temperature in a mixture of argon(Ar) and oxygen (O<sub>2</sub>) with target composed of In<sub>2</sub>O<sub>3</sub>,ZnO,SnO<sub>2</sub>. And then, after the film deposition, we use the fixed annealing condition to define our device in order to figure out the effect of the difference of oxygen flow rate to a-IZTO TFTs. In our present work, the fabrication of bottom gate inverted staggered thin-film transistors using an n-type a-IZTO film as active layer will be described. Our IZTO-based TFT, as shown schematically illustrated cross-sectional and planed views in Fig.2-2 were fabricated on SiO<sub>2</sub>/n-Si substrates. Thermal oxide was chosen as the gate insulator. After patterning the a-IZTO films which are deposited by RF sputtering system at room temperature, source and drain electrodes were deposited and defined by a shadow mask. The film thickness was measured by AFM. The a-IZTO film was controlled at 10nm, 30nm, 50nm, ect and the electrodes of source/drain regions were Indium

Tin Oxide (ITO) with 50nm thick deposited upside of the a-IZTO channel by RF sputtering system. The width and the length range from 200um to 1000um, and the width/length ratio of our TFTs was about 0.2 to 5. Prior to the deposition of a-AZTO films, 100-nm-thick  $\text{SiO}_2$  layers were thermally grown by 650°C in Horizontal Furnace on n-type Si (100) substrates. This process was done in Class 10 in National Nano Device Laboratories. The active layer-a-IZTO film were deposited by sputtering IZTO target ( $\text{In}_2\text{O}_3$ :  $\text{ZnO}$ :  $\text{SnO}_2$  = 2:1:4 mol%) in RF power sputtering system at room temperature. Then, devices were thermally-annealed by a tube furnace in the nitrogen atmosphere for defect elimination. On the other hand, another part of a-IZTO film were deposited straight on silicon wafer in order to get the material analysis.



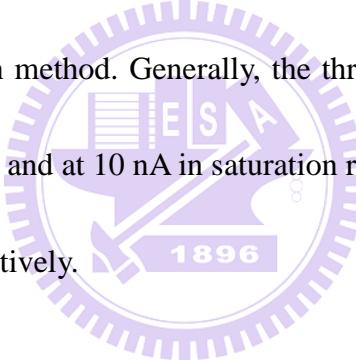
## 2.2 Electrical Measurement and Parameter Extraction Method

The devices electrical properties were measured by Keithley 4200 IV analyzer in a light-isolated probe station at room temperature. In  $I_{DS}$ - $V_{GS}$  measurement, the typical drain-to-source bias was swept from  $V_{GS} = -30\text{V}$  to  $V_{GS} = 40\text{V}$ . In  $I_{DS}$ - $V_{DS}$  measurement, the typical drain-to-source bias was swept from  $V_{DS} = 0\text{ V}$  to  $V_{DS} = 40\text{ V}$ .

In this section, we describe the methods of typical parameters extraction such as threshold voltage ( $V_{th}$ ), subthreshold swing (SS), On/Off current ratio ( $I_{on}/I_{off}$ ) and field effect mobility ( $\mu_{FE}$ ) from device characteristics.

### 2.2.1 Determination of the $V_{th}$

Threshold voltage ( $V_{th}$ ) was defined from the gate to source voltage at which carrier conduction happens in TFT channel.  $V_{th}$  is related to the gate insulator thickness and the flat band voltage. Plenty of methods are available to determine  $V_{th}$  which is one of the most important parameters of semiconductor devices. This thesis adopts the constant drain current method, which is, the voltage at a specific drain current  $NI_D$  is taken as  $V_{th}$ , that is,  $V_{th} = V_G$  ( $NI_D$ ) where  $V_{th}$  is threshold voltage and  $NI_D$  stands for normalized drain current. Constant current method is adopted in most studies of TFTs. It provides a  $V_{th}$  close to that obtained by the complex linear extrapolation method. Generally, the threshold current  $NI_D = I_D/(W/L)$  is specified at 1 nA in linear region and at 10 nA in saturation region; W and L represent for TFT channel length and width, respectively.



### 2.2.2 Determination of the Subthreshold Swing

Subthreshold swing (S.S. , V / decade.) is a typical parameter to describe the control ability of gate toward channel which is the speed of turning the device on and off. It is defined as the amount of gate voltage required to increase and decrease drain current by one order of magnitude. S.S. is related to the process, and is irrelevant to device dimensions. S.S. can be lessened by substrate bias since it is affected by the total trap density including interfacial trap density and bulk density. In this study, S.S. was defined as one-half of the gate voltage re-

quired to decrease the threshold current by two orders of magnitude (from  $10^{-8}\text{A}$  to  $10^{-10}\text{A}$ ).

The threshold current was specified to be the drain current when the gate voltage is equal to

$V_{th}$ .

### 2.2.3 Determination of the field effect mobility

Typically, the field-effect mobility ( $\mu_{FE}$ ) is determined from the transconductance ( $g_m$ ) at low drain bias ( $V_D = 0.1$  V). The TFT transfer I-V characteristics can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} [(V_G - V_{th}) V_D - \frac{1}{2} V_D^2] \quad (2-1)$$

Where

$C_{ox}$  is the gate oxide capacitance per unit area,

$W$  is channel width,  $L$  is channel length,  $V_{th}$  is the threshold voltage.

If  $V_D$  is much smaller than  $V_G - V_{TH}$  (i.e.  $V_D \ll V_G - V_{th}$ ) and  $V_G > V_{th}$ , the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} (V_G - V_{th}) V_D \quad (2-2)$$

The transconductance is defined as:

$$g_m = \mu_{FE} C_{ox} \frac{W}{L} V_D \quad (2-3)$$

Thus,

$$\mu_{FE} = \frac{2L}{C_{ox} W V_D} g_m \quad (2-4)$$

Similarly, we get mobility in the saturation region as

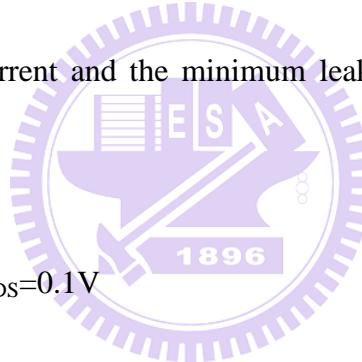
$$\mu = \frac{2L}{C_{ox}W} \left( \frac{\partial \sqrt{I_D}}{\partial V_G} \right)^2 \quad (2-5)$$

#### 2.2.4 Determination of On/Off Current Ratio

Drain on/off current ratio is another important factor of TFTs. High on/off current ratio represents not only the large turn-on current but also the small off current (leakage current). It affects AMLCD gray levels (the bright to dark state number) directly.

There are many methods to specify the on and off current. The easiest one is to define the maximum current as on current and the minimum leakage current as off current while drain voltage equal to 0.1V.

$$\text{on/off} = \frac{I_{DS\text{Max on}}}{I_{DS\text{Min off}}} \quad \text{when } V_{DS}=0.1V \quad (2-6)$$



#### 2.2.5 Extraction of Optical Band Gap

The optical band-gap ( $E_g$ ), which can be theoretically obtained according to Tauc model [14], and the Davis and Mott model in the high absorbance region, as followed :

$$(\alpha h\nu)^n = D^* (h\nu - E_g) \quad (2-7)$$

where

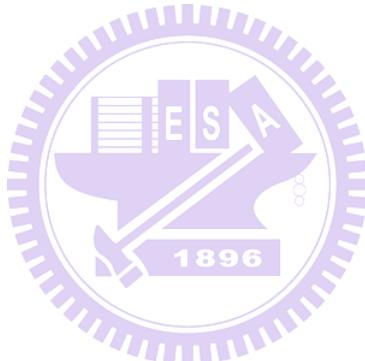
$\alpha$  is the absorption coefficient,

$h\nu$  is the photon energy,

Eg is the optical band gap,

and D is a constant.

The constant n is usually equal to 2 for amorphous semiconductors since it gives the best linear curve in the band-edge region. The absorption coefficient ( $\alpha$ ) can be obtained from the transmittance data by using the equation of  $\alpha = (1/d) * \ln(1/T)$ , where d and T are the thickness and the transmittance of the a-IZTO films with different oxygen flow rate.



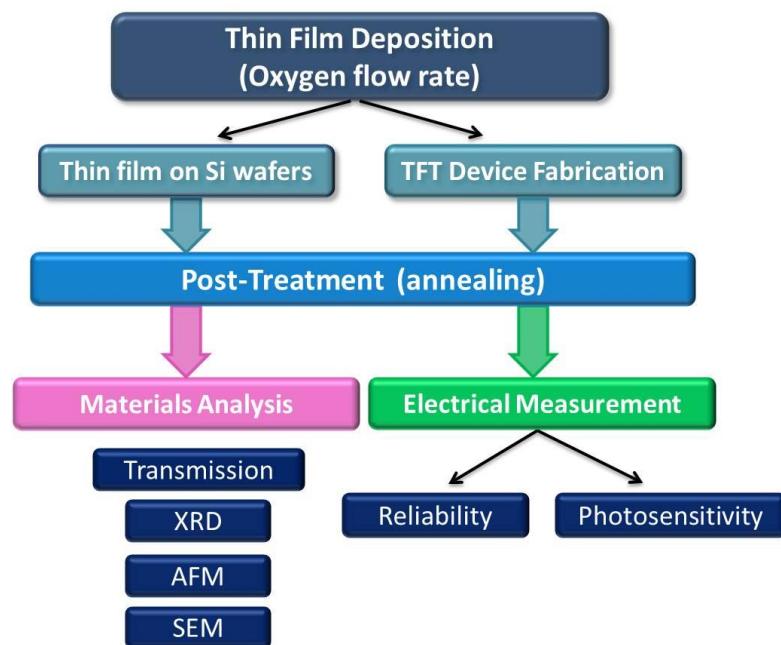


Fig.2- 1 The experimental flow path

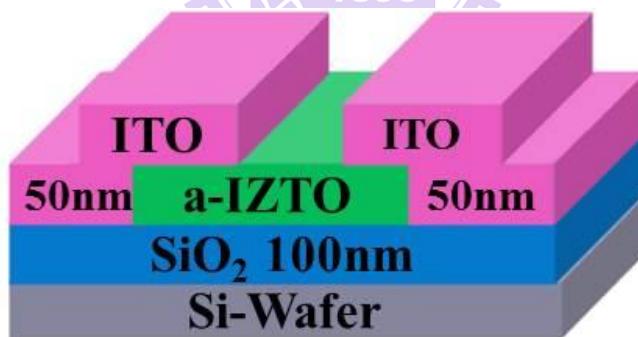


Fig.2- 2 a-IZTO TFT device structure

# Chapter 3

## Results and Discussion

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### 3.1 The effects of oxygen flow rate and channel thickness on a-IZTO TFTs

#### 3.1.1 Characteristic analysis of a-IZTO TFTs with different RF sputtering power

The a-IZTO thin film was deposited on Si wafer and glass substrate together with the devices for material analysis. After a-IZTO thin film deposited, all of them were annealed at 300°C for a half hours. Then we choose film thickness 30nm to have material analysis. Atomic force microscope (AFM), scanning electron microscope (SEM), and X-ray diffraction (XRD) were used to analyze the surface properties of thin film with different oxygen flow rate deposited after annealing process.

The AFM results of a-IZTO film roughness are shown in Fig.3-1(a), (b), (c), (d), and (e) . The thin film's roughness for oxygen flow rate 0, 0.1, 0.5, 1, and 1.5 after annealing process is 0.21, 0.35, 0.29, 0.25, and 0.19nm, respectively. Therefore, the film deposition with different oxygen flow rate incorporation after annealing process does not affect the morphology of a-IZTO thin film.

The SEM results of a-IZTO thin film's surface image are shown in Fig.3-2(a), (b), (c), (d), and (e). The images provide the short-range structures for a-IZTO thin film with different

oxygen flow rate and there is no grain boundary. Therefore, the thin films were still amorphous phase with different oxygen flow rate incorporation after annealing process.

Fig.3-3 shows structure characterizations of a-IZTO thin film. In XRD patterns, a-IZTO thin film with different oxygen flow rate incorporation do not exhibit sharp diffraction peaks assignable to crystalline phase or poly phase. As a result, the thin films with different oxygen flow rate remain the amorphous phase after annealing process. Table 3-1 shows the film elemental composition by XPS analysis, it reveals that oxygen incorporation doesn't have significant influence in elemental composition since the oxygen concentration in Table 3-1 has no obvious tendency.

The transfer characteristics and other parameters of a-IZTO TFTs fabricated by three different RF sputter power with the same thickness 30nm and consistent oxygen flow rate (0.5 sccm) were shown in Fig.3-4 and Table 3-2. From the Table 3-1, TFT with power 70w has the relatively good characteristic, as a result, we choose the power 70w as our experiment RF sputtering power.

Fig.3-5 shows the relation between deposition rate (nm/min) and oxygen flow rate(sccm) with power 70w. The film thicknesses were measured by AFM system in order to get the deposition rate. From the figure, we found that deposition rate is clearly deceases when the oxygen flow rate increases.

### 3.1.2 Characteristic analysis of a-IZTO TFTs with different oxygen flow rate

The a-IZTO TFTs using bottom gate staggered structure were fabricated with different oxygen flow rate and different thickness. The electrical performance shows in Fig.3-6(a), (b) and (c). Error bar in Fig.3-7 presents the overall characteristic of different oxygen flow rate with different thickness. The performance with different thickness has the same tendency for the mobility, threshold voltage, and sub-threshold swing. Mobility decreases as the oxygen flow rate increase. Threshold voltage increase as the oxygen flow rate increase, and sub-threshold swing increase when the oxygen flow rate increase as well. For the discussion of variation, devices with thickness 10nm have the lowest variation whether on mobility, threshold voltage, or sub-threshold swing. Also, devices with thickness 10nm have higher mobility and lower sub-threshold swing rather than the others.

When it comes to the same tendency of threshold voltage in three different thickness, from the literature, as the n-type oxide semiconductor, a well-known mechanism for doping is that the oxygen vacancy generates two free electrons in the conductor band and works as a shallow donor. The higher quantity of oxygen incorporation may decrease the oxygen vacancy in the a-IZTO film.[15,16] In our experiment, we also found that threshold voltage increases when the oxygen flow rate increases. From this result, we can infer that due to the increasing oxygen flow rate, oxygen vacancy decrease which results in the increasing threshold voltage.

On the other hand, the trap densities of a-IZTO film (N<sub>t</sub>) can be estimated from sub-threshold swing value with the following formula.[17,18]

$$S.S. = \ln 10 \times \frac{kT}{e} \times \left[ 1 + \frac{e(tN_t + D_{it})}{C_{ox}} \right] \quad (3-1)$$

where

k is Boltzmann constant

T is temperature(K)

t is the channel thickness(nm)

C<sub>ox</sub> is the gate capacitance per area

e is elementary electric charge

N<sub>t</sub> is the shallow trap density

D<sub>it</sub> is the interface trap density



Assuming the trap tN<sub>t</sub> dominated and D<sub>it</sub> is negligible, we can calculate the N<sub>t</sub> of different oxygen flow rate. From the Fig.3-8 and Table 3-3, take 10nm a-IZTO for example, we can find that trap states increase as oxygen flow rate increases. Moreover, we also discovered that when the oxygen flow rate increases from 0 sccm to 0.1 sccm, trap states apparently decrease. This result also indicates that the a-IZTO thin film requires proper quantity of oxygen to repair its defects and optimize the characteristic, but too much oxygen incorporation may contrarily result in increasing defect.

### 3.1.3 Characteristic analysis of a-IZTO TFTs with different channel thickness

Fig.3-9(a) shows the transfer characteristic of a-IZTO TFTs with no oxygen incorporation on three different channel thickness (10nm,30nm,50nm). From the figure, the device with no oxygen incorporation at 10nm shows the normal thin film transistor characteristic, however, the device with 30nm is more conductive than 10nm device with extra negative threshold voltage and 50nm has even more conductive characteristic than the others. Through the result, we can infer that the quantity of carriers increase when the channel thickness increases. When it compares with the device deposited with 0.1 sccm oxygen flow rate as shown in Fig.3-9(b), the result reveals the oxygen incorporation suppresses the carrier concentration that even 50nm device has thin film transistor characteristic although the threshold voltage are getting negative as the channel thickness increases.

When the oxygen flow rate increases to 0.5 sccm, three different thickness(10nm,30nm,50nm) devices are all have similar characteristic, and then, we fabricated thicker a-IZTO devices (70nm,90nm,110nm) as shown in Fig.3-10. The result indicates that the oxygen flow rate 0.5 sccm is not enough to suppress the carrier concentration of thicker a-IZTO thin film.

### 3.1.4 Summary

According to X-ray diffraction (XRD) pattern, we know that the structure of IZTO film

is still in amorphous phase with different oxygen flow rate incorporation after 300°C annealing process. The increasing oxygen flow rate cause (1) the mobility decreases ( $\mu \downarrow$ ), (2) the threshold voltage positively shifts ( $V_{th} \uparrow$ ), (3) sub-threshold swing increases (S.S.  $\downarrow$ ). On the other hand, the trap density increases when oxygen flow rate increases.

### **3.2 Reliability Analysis of a-IZTO TFTs**

#### **3.2.1 Electrical reliability analysis under gate bias stress**

As shown in Fig.3-7, the result shows that devices with thickness 10nm have the lowest variation whether on mobility, threshold voltage, or sub-threshold swing. For the discussion of the effect on different oxygen flow rate, we use the a-IZTO TFTs with thickness 10nm to have reliability analysis in vacuum in order to isolate from ambiance influence.

Fig.3-11(a),(b) shows the threshold voltage ( $V_{th}$ ) shift of a-IZTO TFT devices under positive gate bias stress (PGBS) and negative gate bias stress (NGBS) for the time duration of 2000 seconds, respectively. And Fig.3-12(a),(b) shows subthreshold swing (S.S.) shift of a-IZTO TFT devices under positive gate bias stress (PGBS) and negative gate bias stress (NGBS) for the time duration of 2000 seconds. The  $V_{th}$  shift of PGBS apparently increase with oxygen flow rate increases except the oxygen flow rate 0.1 sccm is 1.5V, a little bit smaller than 0 sccm about 1.6V.

The a-IZTO TFT devices with different oxygen flow rate don't have significant change

in subthreshold swing (S.S.) shift under positive gate bias stress (PGBS) and negative gate bias stress (NGBS) as shown in Fig.3-12. The phenomenon means the shift of  $V_{th}$  is not accompanied by the sub-threshold slope degradation, which indicates that the  $V_{th}$  shift in a-IZTO is attributed to the trapping of electrons in the interface or bulk dielectric layers with negligible creation of additional interface traps[19,20]. The trapped electrons partially screen the applied electric field so that the effective applied gate voltage is smaller when trapped electrons exist at the interface or bulk dielectric layers. When negative gate bias stress is applied to the gate electrode, the transfer curve hardly moves from the initial one, which is due to the depletion of carriers in the active layer. To better understand the mechanism in the process of the charge trapping and detrapping through bias stress, we found that our results show that the time dependence of the  $\Delta V_{th}$  is in agreement with the stretched exponential equation, which has been developed to model  $\Delta V_{th}$  by the charge trapping mechanism in *a*-Si TFTs. [21]

The stretched-exponential equation for the  $\Delta V_{th}$  is defined as :

$$|\Delta V_{th}| = |V_{th0}| \left\{ 1 - \exp \left[ - \left( \frac{t}{\tau} \right)^\beta \right] \right\} \quad (3-2)$$

Where

$$\Delta V_{th0} = V_{G\_Stress} - V_{th\_initial} \quad (3-3)$$

and

$$\tau = \tau_0 \exp \left( \frac{E_\tau}{kT} \right) \quad (3-4)$$

$\Delta V_{th0}$  is effective stress voltage

$V_{th\_initial}$  is the initial threshold voltage

$\tau$  is the characteristic trapping time of carriers

$\beta$  is the stretched exponential exponent

$E\tau$  is the average effective energy barrier that electrons in the a-IZTO TFT channel need to overcome before they can enter the insulator. And  $\tau$  is a significant parameter which can be inferred as the time duration of electron needed to be trapped or detrapped from the defect, which is mean, when the  $\tau$  is increase, the carriers need more time to be trapped by defects as we can say the defects or trap states decrease, and vice versa. Fig.3-13 shows that the logarithmic time dependence of  $\Delta V_{th}$  can be well fitted with the stretched-exponential equation, and the Table3-4 are the  $\tau$  and correlative parameters. From Table3-4, device with oxygen flow rate 0.1 sccm has the largest  $\tau$ , and it decease when oxygen flow rate increases. This result is consistent with the previous experiment in trap state extraction, the  $\tau$  of device with no oxygen incorporation is smaller than of 0.1 sccm. It confirms that defects increase when oxygen flow rate increases, but the proper quantity of oxygen can repair defects and optimize the characteristic.

### 3.2.2 The photosensitivity analysis

As shown in Fig.3-14(a), the 30nm film with different oxygen flow rate transparent through the visible spectrum. All the film transmittance is great than 80% from 400nm to 700nm. And from Tauc model as mentioned in eq.(2-7), Fig.3-14 (b) shows the relationships between  $(\alpha h\nu)^2$  and the photon energy ( $h\nu$ ), the optical band-gaps,  $E_g$ , can be obtained by extrapolating from the linear region onto the axis of photon energy through the fitting curve. And the Table3-5 shows the optical band-gaps for 30nm a-IZTO thin film with different oxygen flow rate extracted from Fig.3-14 (b). From the table, we observed that thin films do not have obvious difference approximately 3.7eV with different oxygen flow rate.

In order to study the instability under visible light illumination, for device different oxygen flow rate, the devices in 10nm a-IZTO expose in different wavelength illumination were investigated. Fig.3-15(a)~(e) show the corresponding transfer curves of devices with different oxygen flow rate, respectively, which are subjected to various colored visible light illumination (380nm~700nm) without applying bias. From Fig.3-15(a)~(e), we can find that the devices with different oxygen flow rate are insensitivity to the visible light.

For the further investigation of instability of reality, we use the light source with full-band spectrum similar to flat panel back light illumination. Fig.3-16 shows the back light spectrum with intensity. Fig.3-17(a) shows the the threshold voltage ( $V_{th}$ ) shift under light illumination for 2000 seconds without applying bias, and Fig.3-17(b) is recovery mesurement

at 1 hour, 3 hour, and 6 hour after the light illumination. From the figure, threshold voltage ( $V_{th}$ ) of all devices shift negatively for small amount about 1.3V, and will recover for a period of time. This result shows, the light generated electron hole pairs, causing more conductive on active layer. As in Fig.3-16, the wavelength in blue light has the highest intensity in this full band spectrum, even so, the threshold voltage ( $V_{th}$ ) shows a small amount of shift on a-IZTO TFT. It is clearly again to observe that the devices with different oxygen flow rate are insensitivity to the visible light.

Moreover, the negative bias illumination stress (NBIS) induced instability of the electrical properties was also investigated under the back light illumination. In the stress conduction, the gate voltage was fixed at the  $V_G$  of -25V and the S/D electrodes were grounded. In Fig.3-18(a), voltage shift doesn't have obvious tendency in different oxygen flow rate. The voltage shifts for five oxygen flow rates are about -15V which is much bigger than negative gate bias stress without illumination. The light induced electron hole pairs from deep level state, and free hole carriers were attracted to the interface by negative bias, as a result, electrons in channel result in the negative voltage shift. As we know from literature, electron hole pairs generated from illumination are come from deep level state [26], and this also means that oxygen incorporation doesn't have significant influence in deep level trap state since the voltage shifts are about -15V and with no obvious tendency. Again with stretch exponential fitting shown in Fig.3-18(b) and Table 3-6,  $\tau$  has no obvious tendency as well.

### 3.2.3 Summary

Through stretched exponential equation analysis under positive gate bias stress, the fitting result shows that defects increase when oxygen flow rate increases. And shifts of threshold voltage do not have obvious change in negative bias stress. The devices show insensitivity to the visible light, only under the full band spectrum with the highest intensity in blue light, the threshold voltage shifts negatively for about 1.3V. In NBIS, voltage shift doesn't have obvious tendency in different oxygen flow rate, that means, oxygen incorporation doesn't have significant influence in deep level trap state.



## 3.3 Application of a-IZTO TFTs for ultra-thin glass panel

### 3.3.1 Introduction

Recently, there has been considerable interest in flexible displays, as they facilitate the fabrication of displays that are thin, lightweight, robust, conformable, and flexible. [22] Large-area electronics composed of thin-film transistors TFTs have been fabricated mainly on rigid glass substrates. The substrates and the housing bodies to protect the substrates from the damage occupy the greater part of the electronics in volume and determine their total weight. [23] The primary flexible substrate candidates are plastics and thin glass. Plastic substrates are inexpensive, roll-to roll processable and can be laminated to multi-layers, but they also impose limitations with respect to thermal processing and barrier performance.

Ultra-thin glass (0.13mm) substrates have recently caught attention because they exhibit better thermal stability, light weight, higher visual transparency than plastics and the bending potential.[24] For the advantages of ultra thin glasses, they can also apply in transparent mobile display, google glass, etc.

### 3.3.2 Device structure

Fig.3-19 shows the structure of a-IZTO TFT fabricated on ultra thin glass (0.13mm). Fabrication flows were the same with the ones fabricated on Si wafer as written in chapter 2, except the gate insulator was fabricated by PECVD with 350nm and gate electrode was annealed at 300°C before the gate insulator deposited. 10nm a-IZTO TFTs with oxygen flow rate 0.1sccm fabricated on ultra thin glass were all have annealing process after the device fabrication. Fig.3-20 (a), (b) is the side view and top view of a-IZTO TFT fabricated on ultra thin glass.

### 3.3.3 Electrical characteristic analysis

Since the devices in 10nm have relatively nice characteristic, from the aspect of mobility, comparison of five different oxygen flow rate in mobility are shown in Table 3-7, the device with oxygen flow rate 0.1 sccm has the highest mobility. As a result, we choose this oxygen condition to transfer from Si wafer to ultra thin glass.

Fig3-21 shows the electrical performance of the device with oxygen flow rate 0.1 sccm. From the figure, it shows that the device fabricated on ultra thin glass still has good uniformity, and a little decrease in mobility about  $12\sim13\text{cm}^2/\text{V.s.}$  Table 3-8 compares the relative parameters for ultra thin glass and Si wafer.

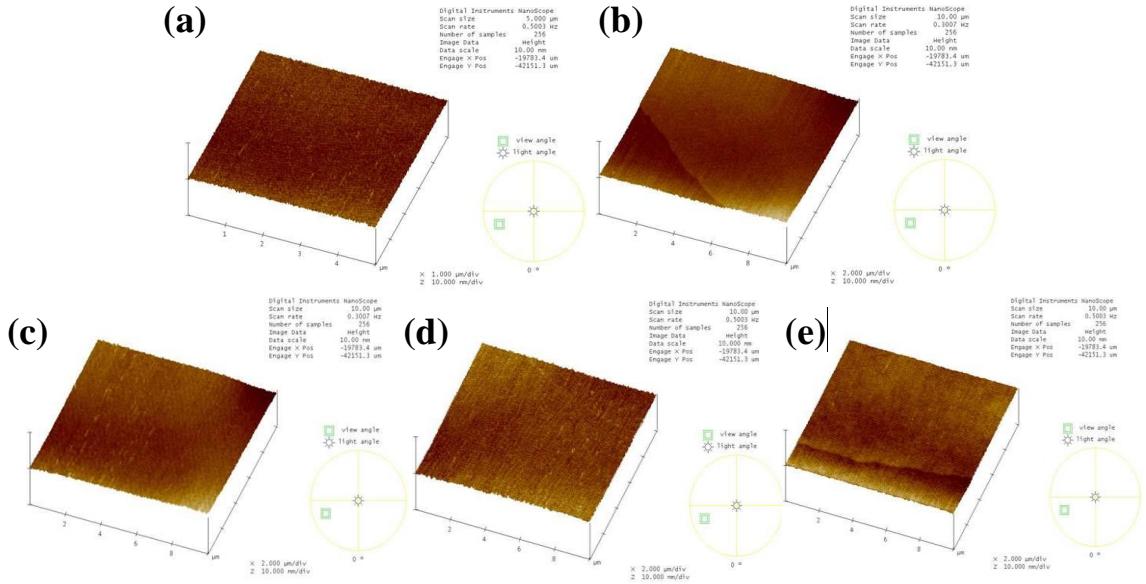
### 3.3.4 Electrical reliability analysis under gate bias stress

Fig.3-22 (a), (b) shows the electrical performance of a-IZTO TFT devices under positive gate bias (25V) stress (PGBS) and negative gate bias (-25V)stress (NGBS) for the time duration of 2000 seconds, respectively. We can clearly discover that the tendency of  $V_{th}$  shift is completely opposite to the tendency on Si wafer. In addition, a threshold voltage shift is easily observed as numbers of traps exist at the active layer/dielectric interface by forward/reverse voltage sweep. Therefore, the hysteresis measurement is usually performed to investigate the influence of charge trapping. [25] Fig.3-23 shows the hysteresis in transfer characteristics observed between forward ( $V_G = -40\text{V}$ to  $40\text{ V}$ ) and reverse ( $V_G = 40\text{ V}$  to  $-40\text{ V}$ ) gate voltage sweeps. Clearly, the threshold voltage shift ( $\Delta V_{th}$ ) is about  $-4\text{ V}$ . That is, from Fig.3-23 , the forward curve shows normal transistor characteristic, however in the reverse part, when positive gate bias( $40\text{V}$ ) continued sweep toward negative, this phnonmenon is similar to short period of positive gate bias stress. The threshold voltage shift negatively indicate that channel is easier to turn on. We guess that when gate electrode was treated by posi-

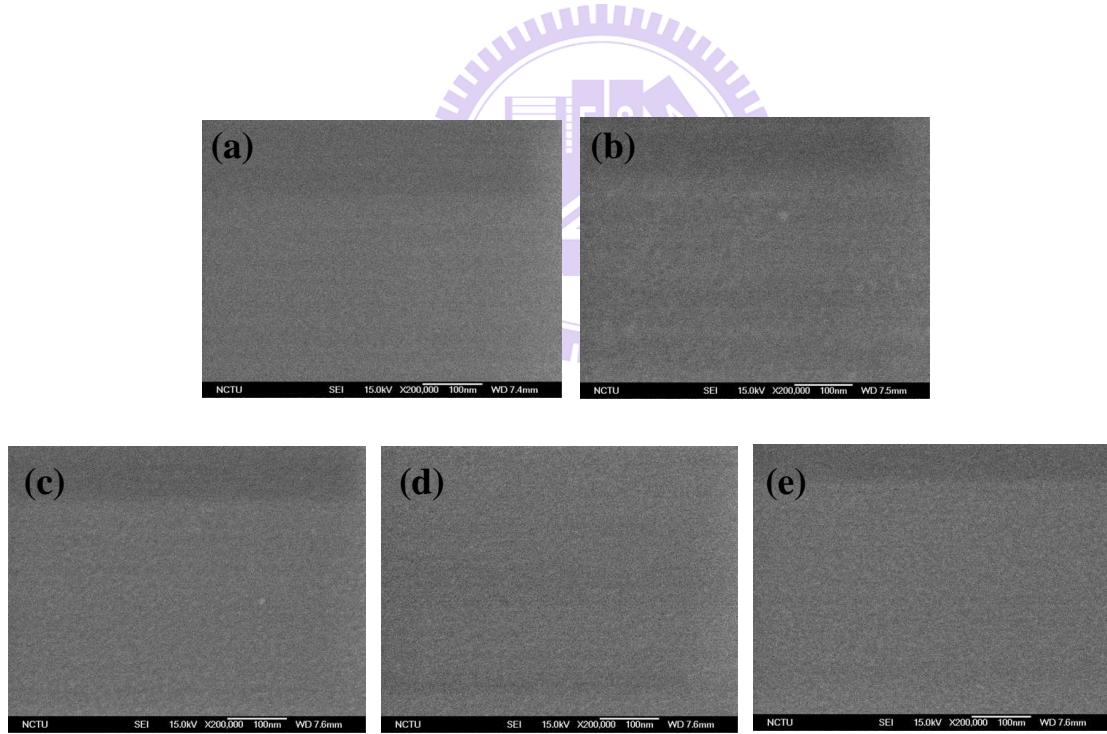
tive bias, free carriers with positive charging were depleted from gate electrode to gate insulator, catching more electrons on the interface of gate insulator and active layer, causing more conductive in TFT characteristic. And the negative gate bias stress can be explained in the same way as well. This phenomenon is not consistent with the devices fabricated on Si wafers, it reveals that the interface of gate electrode and gate insulator deposited by PECVD may need some of improvement.

### 3.3.5 Summary

10nm a-IZTO TFT device with oxygen flow rate 0.1 sccm was successfully transferred on the ultra thin glass with stable, uniform basic characteristic and not bad mobility ( $12\sim13\text{cm}^2/\text{V.s.}$ ) . However, the gate bias stress has opposite tendency, through hysteresis measurement, it is regarded as the poor interface of gate electrode and gate insulator deposited by PECVD.



**Fig.3- 1** The AFM results of 30nm IZTO film roughness for oxygen flow rate (a) 0 sccm, (b) 0.1 sccm, (c) 0.5 sccm, (d) 1 sccm, (e) 1.5 sccm, after annealing process



**Fig.3- 2** The SEM results of 30nm a-IZTO film surface for oxygen flow rate (a) 0 sccm, (b) 0.1 sccm, (c) 0.5 sccm, (d) 1 sccm, (e) 1.5 sccm, after annealing process

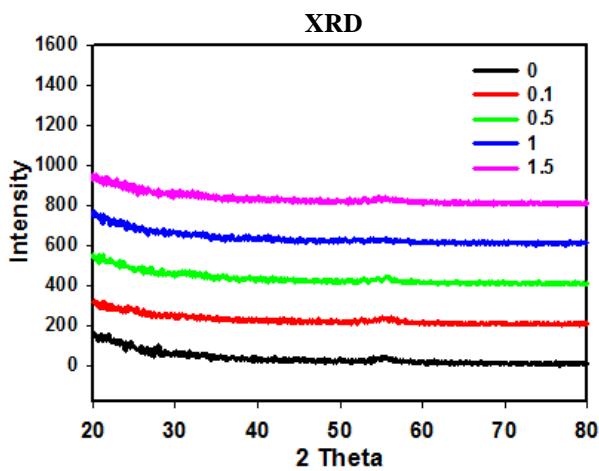


Fig.3- 3 XRD pattern of 30nm a-IZTO thin film for five different oxygen flow rate after annealing process

Atomic concentration(%)	In3d5	Zn2p3	Sn3d5	O1s
<b>target</b>	16.67	4.17	16.67	62.49
<b>0 sccm</b>	24.4284	6.0185	16.2646	53.2557
<b>0.1 sccm</b>	24.7969	5.9317	16.2594	52.6118
<b>0.5 sccm</b>	25.4067	4.1818	16.0316	54.3799
<b>1 sccm</b>	24.4678	4.5079	16.0626	54.9617
<b>1.5 sccm</b>	24.9013	4.9597	16.1194	54.0196
<b>0.5 sccm (no anneal)</b>	25.095	5.1886	15.9375	53.7789

Table 3-1 elemental composition of 30nm a-IZTO thin film examined by XPS analysis

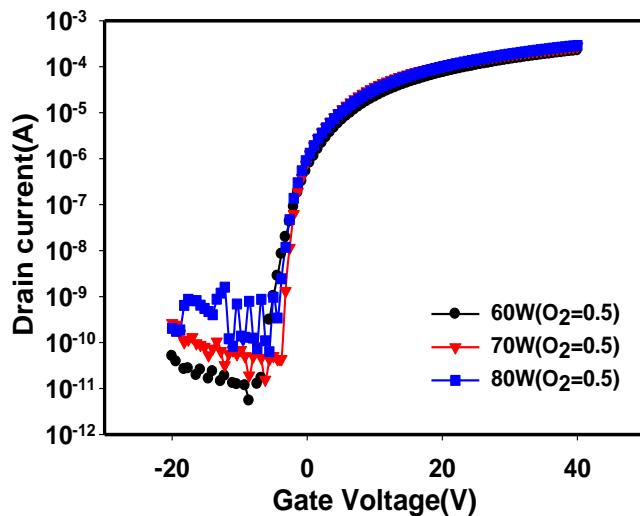


Fig.3- 4 Transfer characteristics of three different RF sputter power with the same thickness 30nm and consistent oxygen flow rate (0.5 sccm)

Sputtering power(w)	60w	70w	80w
$\mu$ (cm <sup>2</sup> /V.s)	11.0586	17.6081	14.4449
V <sub>th</sub> (V)	-3.71	-2.68	-3.31
S.S.(V/decade)	0.41	0.4	0.42

Table 3-2 Parameter of three different RF sputter power with the same thickness 30nm and consistent oxygen flow rate (0.5 sccm)

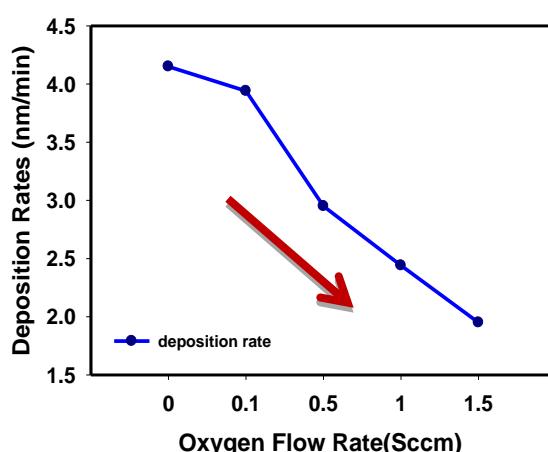


Fig.3-5 Relation between deposition rate (nm/min) and oxygen flow rate(sccm) with power 70w

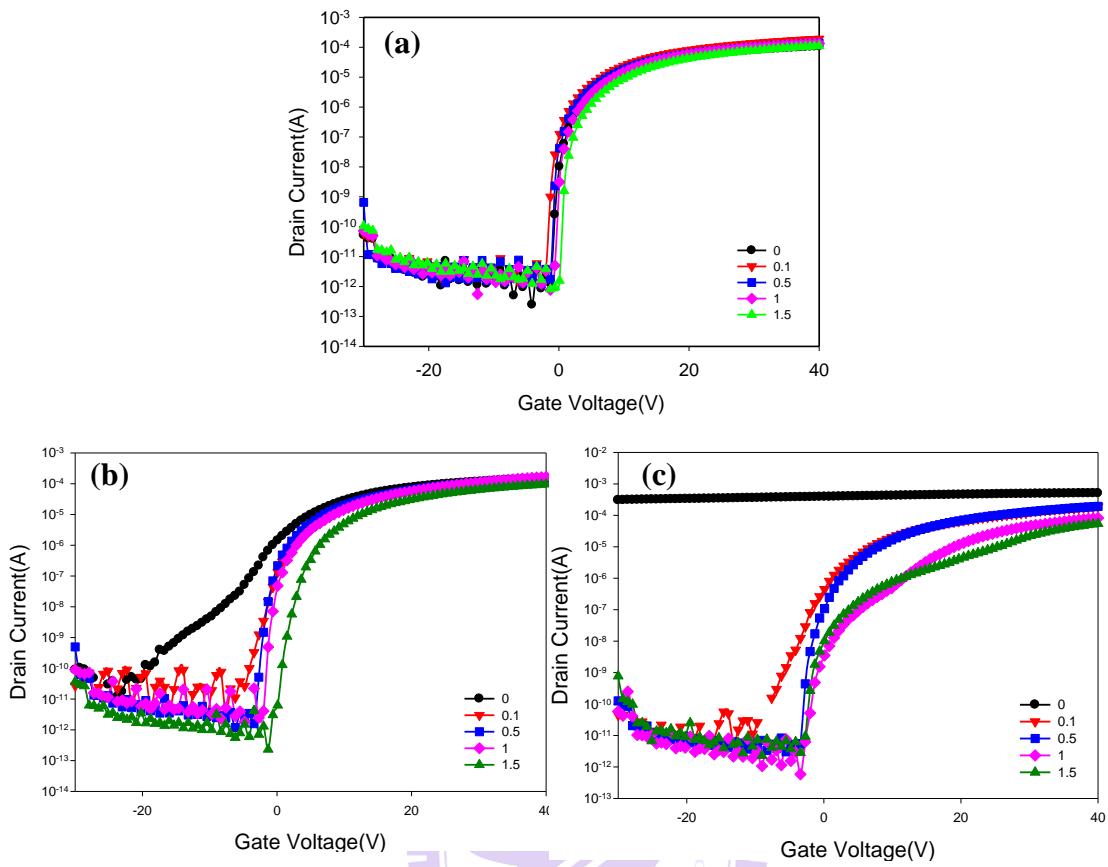


Fig.3-6 electrical performance with different oxygen flow rate in (a) 10nm (b) 30nm (c) 50nm.

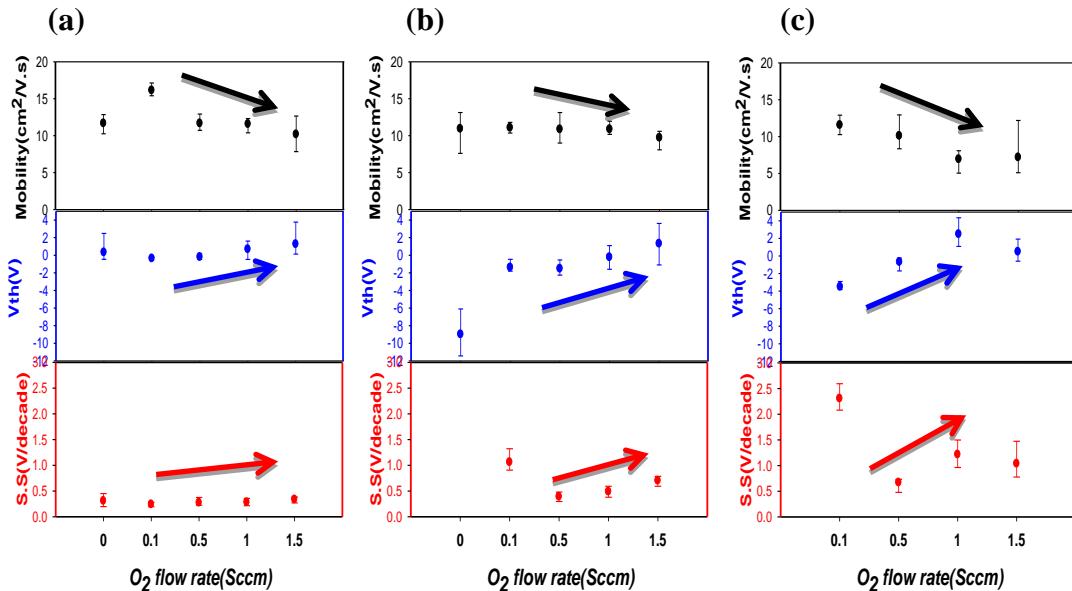


Fig.3-7 The overall characteristic of different oxygen flow rate with thickness (a) 10nm (b) 30nm (c) 50nm.

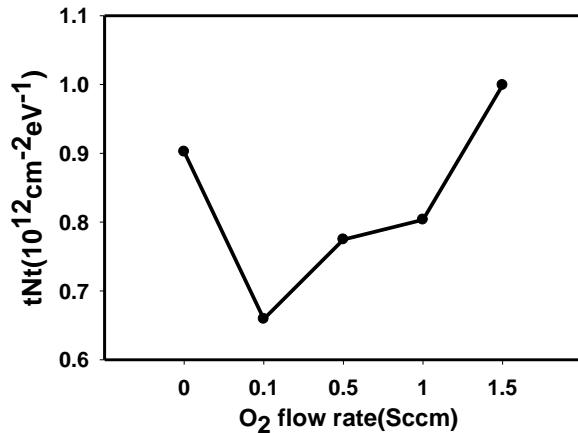


Fig.3-8 Relation between trap state and oxygen flow rate(sccm)

O <sub>2</sub> (sccm)	0	0.1	0.5	1	1.5
Nt(cm <sup>-3</sup> eV <sup>-1</sup> )	9.02x10 <sup>19</sup>	6.59x10 <sup>19</sup>	7.75x10 <sup>19</sup>	8.03x10 <sup>19</sup>	9.99x10 <sup>19</sup>

Table 3-3 Parameters of trap state of different oxygen flow rate with the thickness 10nm

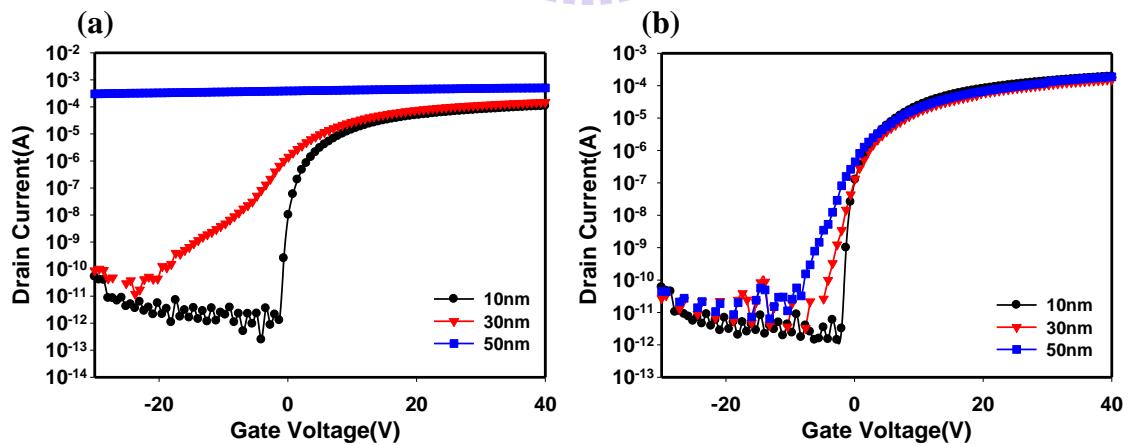


Fig.3-9 transfer characteristic of a-IZTO TFTs with oxygen flow rate (a) 0 sccm (b) 0.1 sccm in three different thickness.

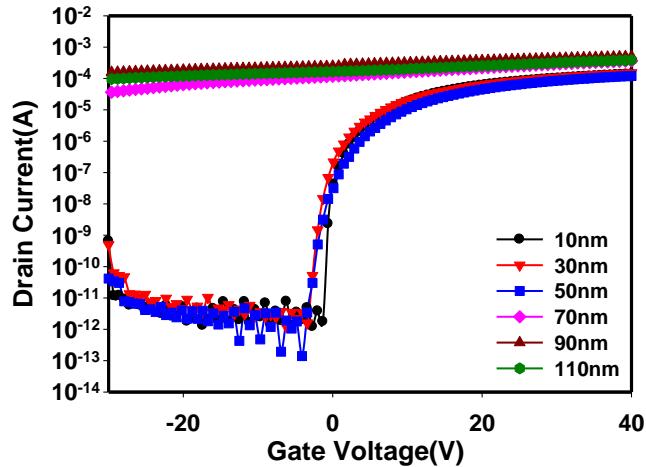


Fig.3-10 transfer characteristic of the oxygen flow rate 0.5 sccm with different thickness.

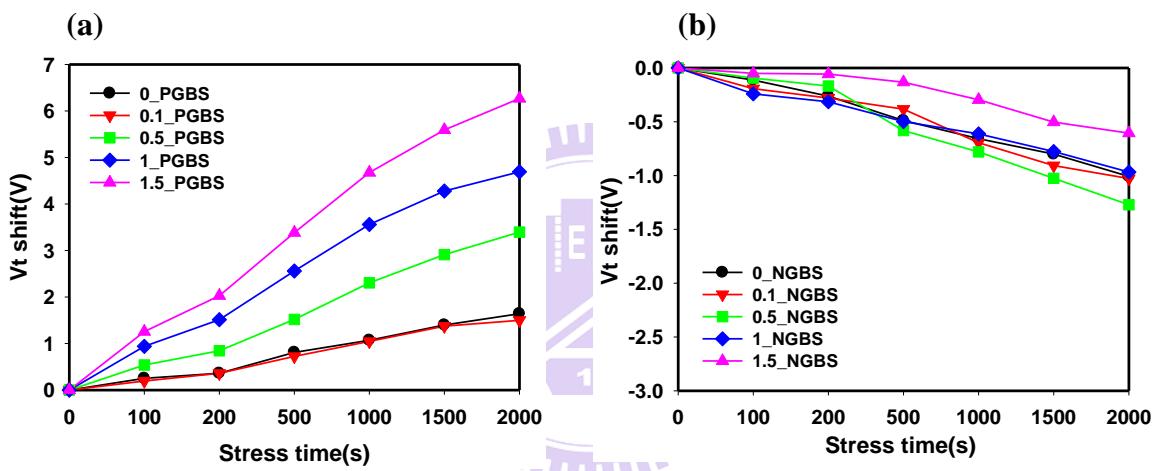


Fig.3-11 Threshold voltage ( $V_{th}$ ) shift of 10nm a-IZTO TFT devices under (a) positive gate bias stress (PGBS) and (b) negative gate bias stress (NGBS) for 2000 seconds.

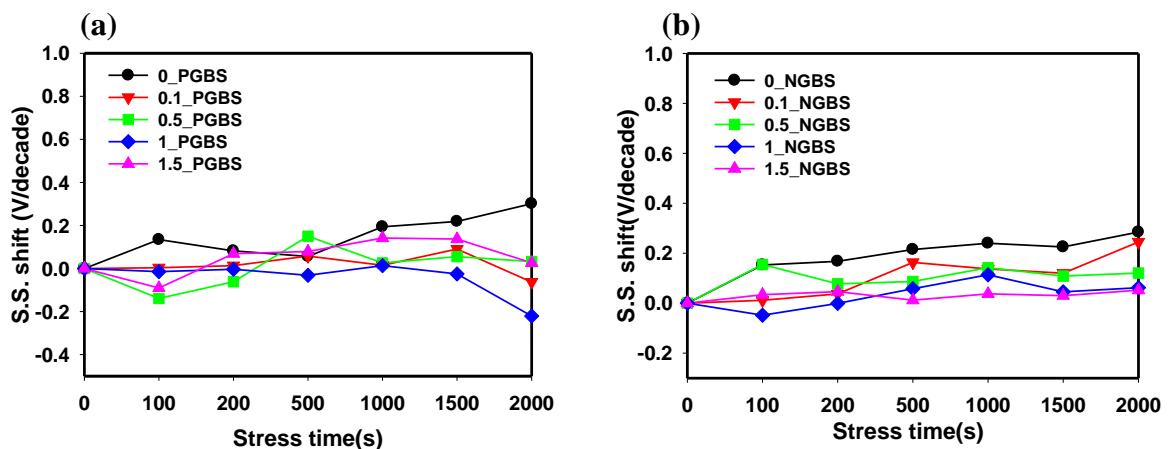


Fig.3-12 Subthreshold swing (S.S.) shift of 10nm a-IZTO TFT devices under (a) positive gate bias stress (PGBS) and (b) negative gate bias stress (NGBS) for 2000 seconds

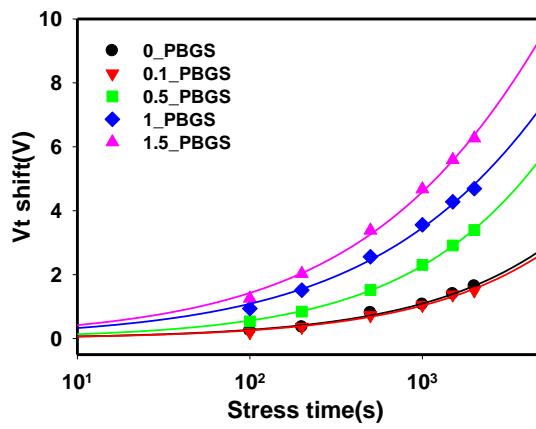


Fig.3-13 the logarithmic time dependence of  $\Delta V_{th}$  with the stretched-exponential fitting curve

$O_2$ (sccm)	0	0.1	0.5	1	1.5
$\Delta V_{th0}$	25.06	25.48	24.9	24.19	24.09
$\beta$	0.61	0.57	0.62	0.53	0.54
$\tau(s)$	$1.64 \times 10^5$	$1.17 \times 10^5$	$4.3 \times 10^4$	$3.48 \times 10^4$	$1.79 \times 10^4$

Table3-4 Correlative parameters of stretched-exponential fitting curve

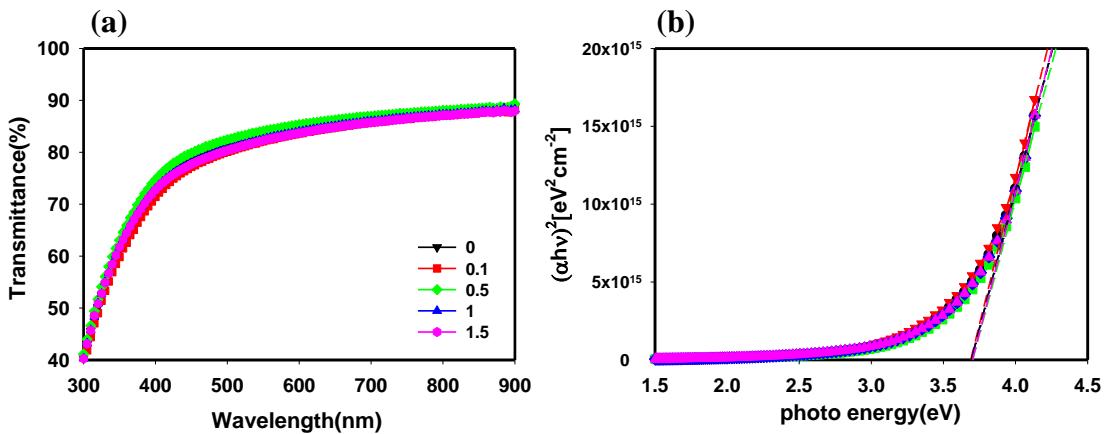


Fig.3-14 (a) the 30nm film transmittance with different oxygen flow rate transparent through the visible spectrum. (b) the relationships between  $(\alpha h\nu)^2$  and the photon energy ( $h\nu$ )

O <sub>2</sub> (sccm)	0	0.1	0.5	1	1.5
Band gap(eV)	<b>3.694</b>	<b>3.689</b>	<b>3.703</b>	<b>3.694</b>	<b>3.702</b>

Table3-5 optical band-gaps for 30nm a-IZTO thin film with different oxygen flow rate

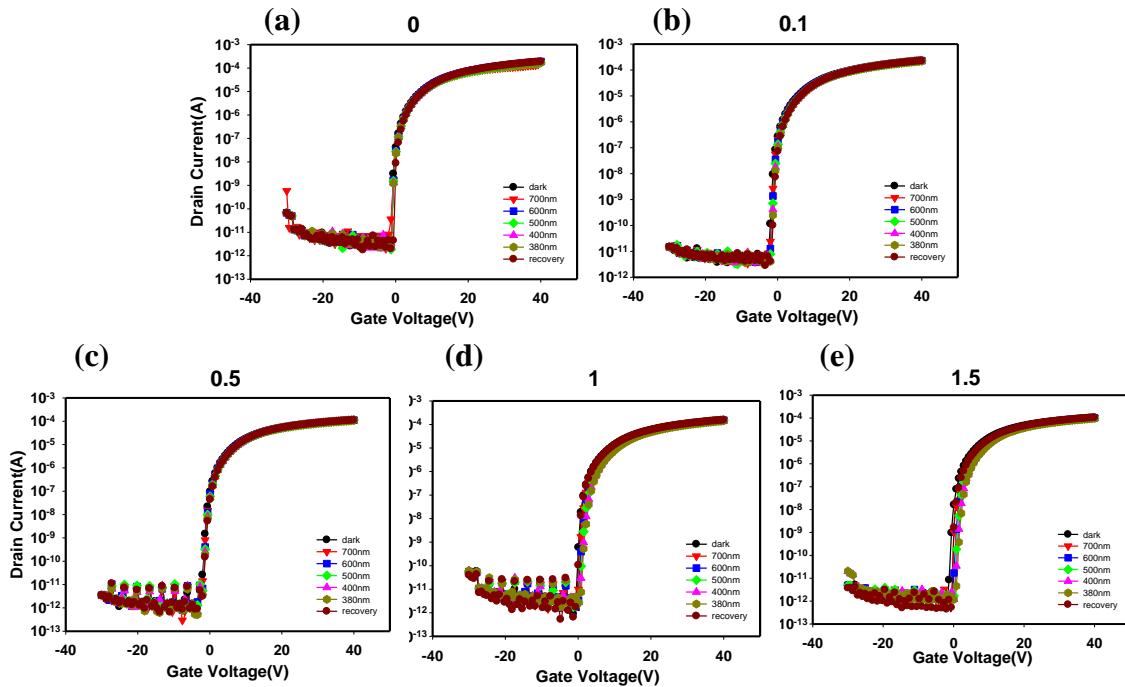


Fig.3-15 Transfer curves of devices with oxygen flow rate (a) 0 sccm, (b) 0.1 sccm, (c) 0.5 sccm, (d) 1 sccm, (e) 1.5 sccm under visible light illumination

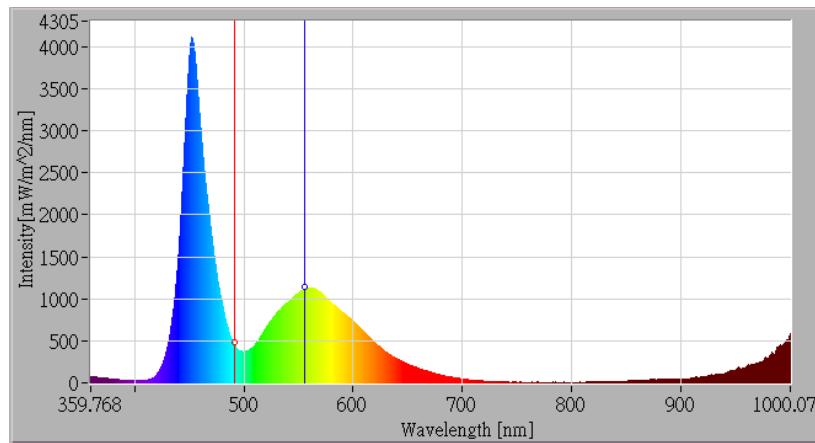


Fig.3-16 back light spectrum with intensity.

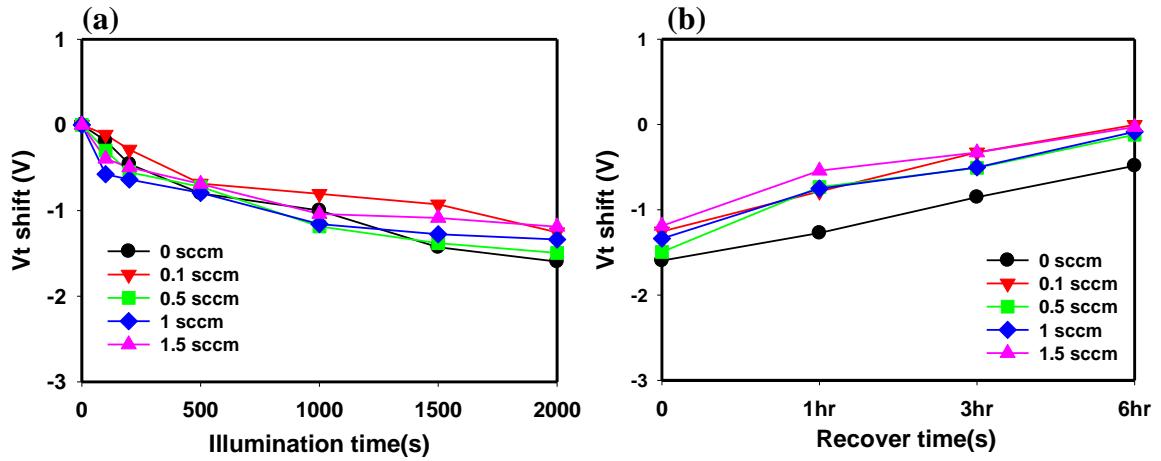


Fig.3-17 Threshold voltage ( $V_{th}$ ) shift of (a) light illumination for 2000 seconds without applying bias (b) recovery measurement at 1 hour, 3 hour, and 6 hour after the light illumination.

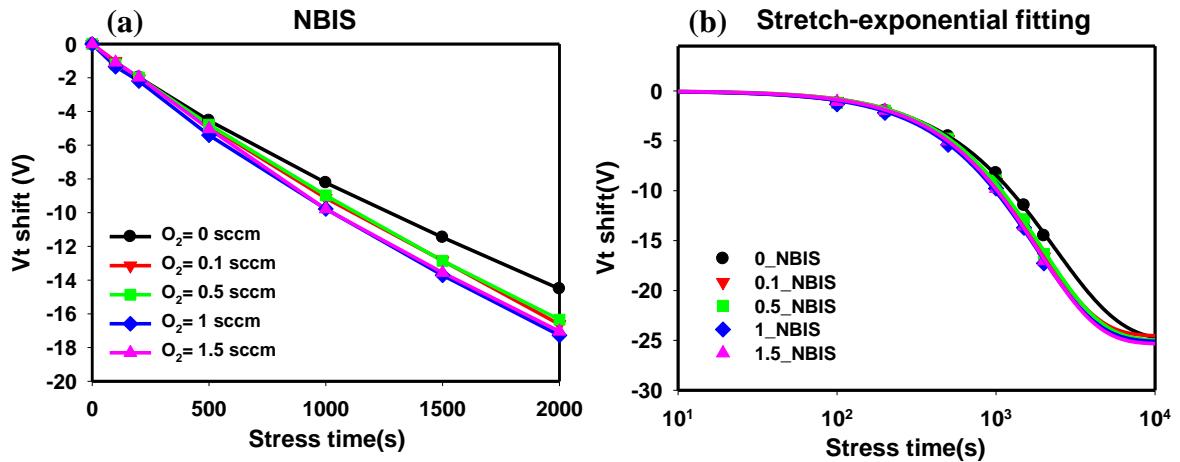


Fig.3-18 (a) Threshold voltage ( $V_{th}$ ) shift of light illumination for 2000 seconds with gate bias -25V (b) the logarithmic time dependence of  $\Delta V_{th}$  with the stretched-exponential fitting curve

	0	0.1	0.5	1	1.5
$\Delta V_{th0}$ (V)	-25	-24.6	-25.1	-25.12	-25.35
$\beta$	1.04	1.16	1.14	1.12	1.15
$\tau$ (s)	$2.35 \times 10^3$	$1.88 \times 10^3$	$1.96 \times 10^3$	$1.82 \times 10^3$	$1.85 \times 10^3$

Table 3-6 Correlative parameters of stretched-exponential fitting curve

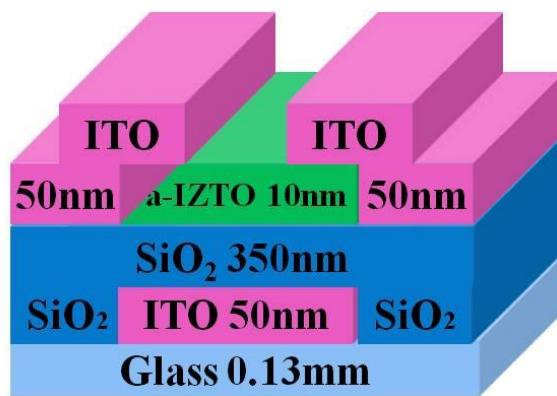


Fig.3-19 Structure of a-IZTO TFT fabricated on ultra thin glass

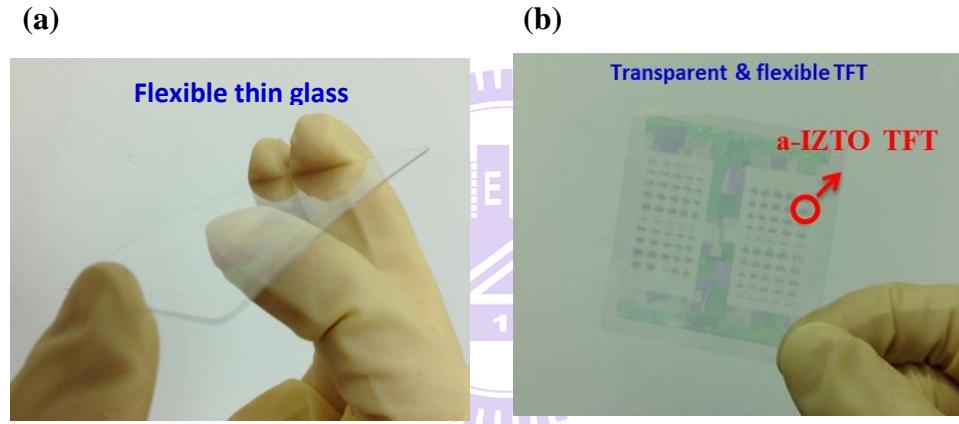


Fig.3-20 The (a) side view and (b) top view of a-IZTO TFT fabricated on ultra thin glass.

O <sub>2</sub> flow rate(sccm)	0	0.1	0.5	1	1.5
Mobility(cm <sup>2</sup> /V.s)	<b>10.49</b>	<b>15.4</b>	<b>12.93</b>	<b>10.76</b>	<b>9.85</b>

Table 3-7 Comparison of 10nm a-IZTO device on with five different oxygen flow rate in mobility (cm<sup>2</sup>/V.s)

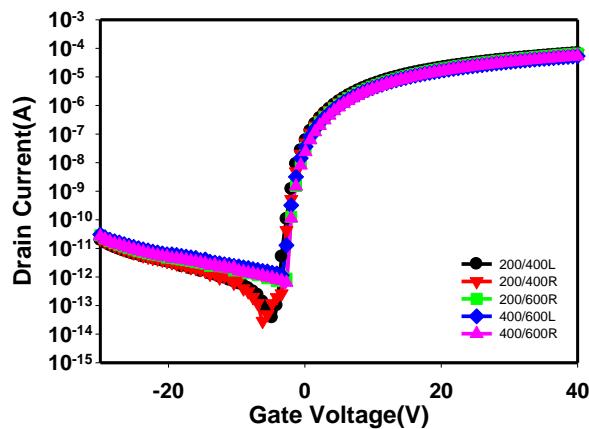


Fig 3-21 Electrical performance of the device with oxygen flow rate 0.1 sccm.

O2 (0.1 sccm)	Vth (V)	Mobility(cm <sup>2</sup> /V.s)	S.S.(V/decade)
glass	-0.605	12.1	0.43
wafer	-0.36	15.4	0.24

Table 3-8 comparison of the relative parameters for ultra thin glass and Si wafer.

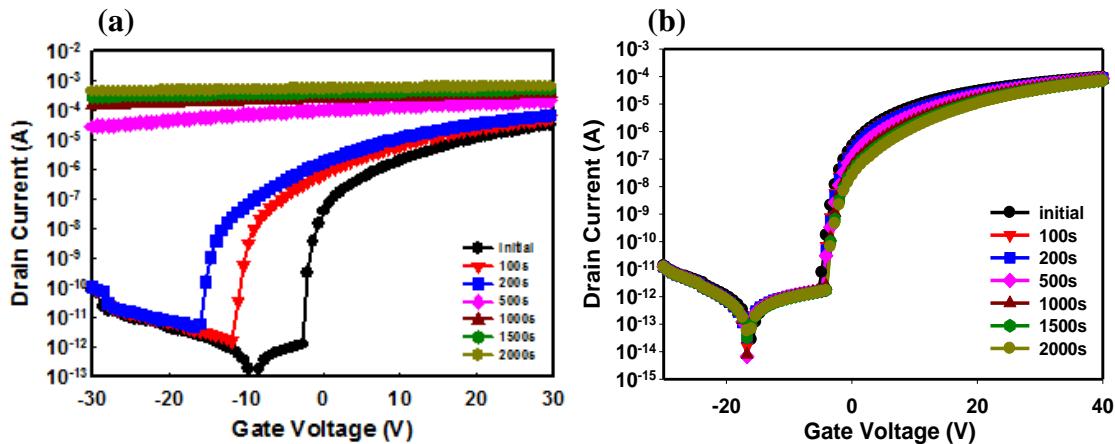


Fig.3-22 Electrical performance of a-IZTO TFT devices under (a) positive gate bias (25V) stress (PGBS) and (b) negative gate bias (-25V) stress (NGBS) for the time duration of 2000 seconds

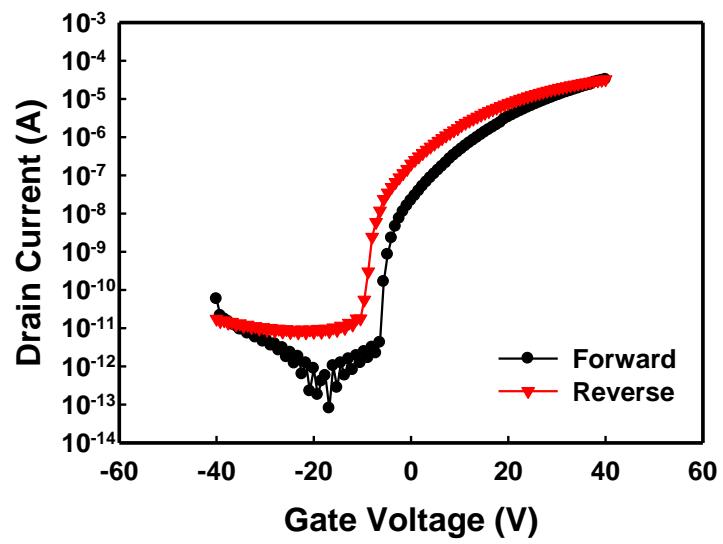
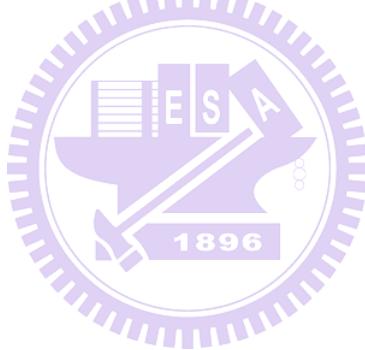


Fig.3-23 Hysteresis in transfer characteristics observed between forward ( $VG = -40V$  to  $40V$ ) and reverse ( $VG = 40V$  to  $-40V$ ) gate voltage sweeps.



# Chapter 4

## Conclusion

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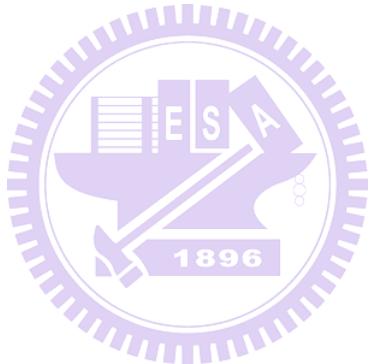
### 4.1 Conclusions

In this study, a-IZTO TFT was investigated with its (a) rare element (Ga) displacement, (b)High mobility, (c) relative low annealing temperature, and we obtained the optimized characteristic which is 10nm a-IZTO with oxygen flow rate 0.1 sccm. And the optimized mobility can reach  $15\sim17\text{cm}^2/\text{V.s.}$

From the trap state extraction and stretch-exponential fitting in PGBS , 10nm a-IZTO TFT with oxygen flow rate 0.1 sccm has the best reliability due to the less bulk trap density, and the defects concentration increase in a-IZTO thin film when the oxygen flow rate increases. In NBIS,  $V_{th}$  shifts don't have obvious difference in all oxygen flow rates, that is, oxygen incorporation does not have significant influence on deep level trap state. For the future application, optimized characteristic of a-IZTO TFT was successfully fabricated on ultra-thin glass. With its good uniformity, transparency and comparable mobility with it on Si wafers, this application shows potential in the future.

## 4.2 Future work

Base on the result of opposite tendency under the gate bias stress on ultra thin glass, the interface of gate electrode and gate insulator need to be improved. Changing the gate material is one of the possible ways to improve the interface quality. The a-IZTO TFTs with large channel thickness can be discussed in order to futher understand characteristic of thicker channel a-IZTO TFTs in reliability and photosensitivity.



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