Design, Fabrication, and Characterization of Novel Vertical Coaxial Transitions for Flip-Chip Interconnects

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***Abstract*—In this paper, a novel transition design using vertical "coaxial transition" for coplanar waveguide (CPW-to-CPW) flip-chip interconnect is proposed and presented for the first time. The signal continuity is greatly improved since the coaxial-type transition provides more return current paths compared to the conventional transition in the flip-chip structure. The proposed coaxial transition structure shows a real coaxial property from the 3-D electromagnetic wave simulation results. The design rules for the coaxial transition are presented in detail with the key parameters of the coaxial transition structure discussed. For demonstration, the back-to-back flip-chip interconnect structures with the vertical coaxial transitions have been successfully fabricated and characterized. The demonstrated interconnect structure using the coaxial transition exhibits the return loss below 25 dB and the insertion loss within 0.4 dB from dc to 40 GHz. Furthermore, the measurement and simulation results show good agreement. The novel coaxial transition demonstrates excellent interconnect performance for flip-chip interconnects and shows great potential for flip-chip packaging applications at millimeter waves.**

***Index Terms*—Coaxial, coplanar waveguide (CPW), flip-chip, interconnect, transition.**

I. Introduction

THE demands of high frequency interconnect techniques for monolithic microwave integrated circuits (MMICs) are growing with increasing operating frequencies in the wireless communication systems. Interconnect effects can have significant impacts on the overall system performance at high frequencies. There are several interconnect schemes at the chip level packaging. Wire bonding technique is one of those, which has been widely used in the chip level packaging for a long time. However, it suffers from serious parasitics when the operating frequency reaches the gigahertz range, due to its very long interconnect path. As a consequence, flip-chip technique is expected as a low cost alternative for high frequency packaging with better transition performances. Flip-chip interconnects have the advantages of shorter conducting path, lower parasitic effects, better heat dissipation, and smaller size over the traditional bonding-wire interconnects. Thus, a number of studies have been reported for designs and characterizations of flip-chip interconnects at high frequencies [1]–[8].

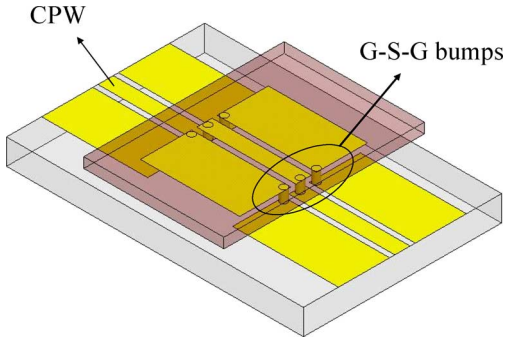

Fig. 1. Conventional vertical transitions of three bumps for CPW-to-CPW flip chip interconnects.

Flip-chip interconnects are more compatible with coplanar configurations, which are frequently used for very high frequency designs to minimize unwanted parasitics. Conventionally, solder or gold bumps are grown on the ground and signal path of the coplanar waveguide (CPW) structure at the vertical transition region to maintain the continuity in the current flow. Fig. 1 shows the conventional flip-chip interconnect structure with three bumps for CPW-to-CPW transitions. Theories and effects of the bump positions and dimensions have been presented and discussed in several papers [1], [2], [4]–[7]. In the conventional architecture, bump parameters and pad sizes are optimized for better transition characteristics. High impedance line and staggered bumps have been proposed to achieve broadband interconnect performances [1], [5], [7]. Another proposed design reported for better electrical shielding purpose was to use multiple ground bumps arranged in an annular form as the vertical transition at the flip-chip interconnect [8]. This was called pseudo-coaxial vertical transition. However, it was still not a real coaxial transition at the vertical interconnect. In this paper, we propose the coaxial transition for the flip-chip interconnect to replace the conventional two-ground-bump transition for the first time.

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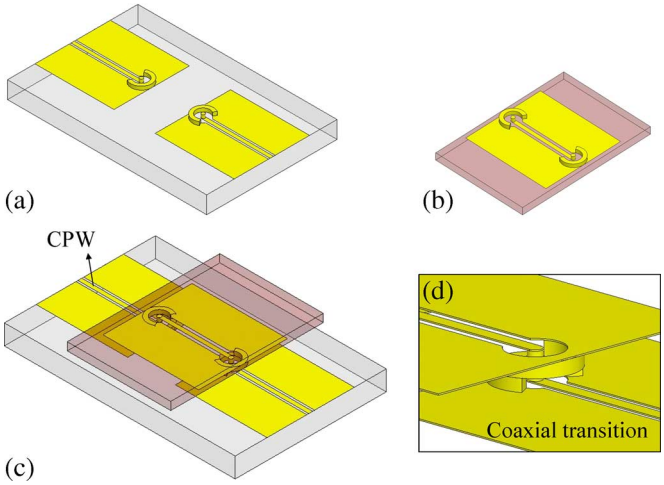

Fig. 2. Proposed structure of CPW-to-CPW interconnects with vertical "coaxial transitions." (a) Substrate-side view. (b) Chip-side view. (c) Full view. (d) Detailed view at transition.

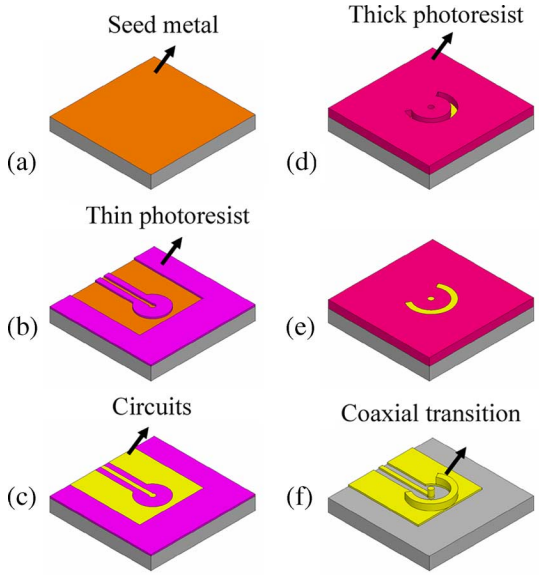

Fig. 3. Fabrication procedures of the coaxial transition structure.

The proposed coaxial transition structure has two C-shaped ground bumps on the substrate and chip respectively to replace the two ground bumps [9]. Fig. 2 shows the flip-chip interconnect structure with the novel vertical coaxial transitions. The open ends of the two C-shaped bumps are arranged in opposite directions. The two C-shaped ground bumps together with the center cylindrical signal path form a perfect coaxial structure for better signal transmission, and the performance and characteristic properties of this transition will be discussed throughout the rest of this paper.

This paper is organized as follows. First, the fabrication process to realize the coaxial transitions onto the CPW circuits is presented, where the key process step, the thick photoresist lithography, is described in detail. Subsequently, by using the full wave 3-D electromagnetic wave simulator CST Microwave Studio, the electric and magnetic fields are plotted to show the coaxial properties at the transition. In the subsequent section, the main physical parameters of the proposed coaxial transition are described, and the design parameters for the coaxial transition are discussed according to the full wave simulation results. The interconnect structures with the coaxial transitions have been successfully fabricated and then radio-frequency (RF) characterized up to 40 GHz to verify the key design parameter of the coaxial transition. The transition model has been exported from the full wave CST simulator and inserted into Agilent Advanced Design System (ADS) simulation tool to simulate the complete flip-chip assembly, which shows good agreement with the measured results. The excellent results demonstrate the potential and feasibility of such coaxial transition for the flip-chip applications at high frequencies.

II. Fabrication of Coaxial Transition

For the proposed coaxial transition in the flip-chip structure, the fabrication of the coaxial bumps is of critical importance. The fabrication process for the coaxial transition onto the CPW circuits was developed in-house and has successfully demonstrated the coaxial concept for the flip-chip interconnects.

Fig. 3 shows the diagrams of the fabrication process procedures. Alumina (Al_2O_3) and gallium arsenide (GaAs) were the materials for the substrate and the chip. The thickness of the Al_2O_3 substrate and GaAs chip were 254 and 100 μm, respectively. The Al_2O_3 substrate was 2-in square, and the GaAs was a 3-in wafer. The interconnect metal was gold and was formed by electroplating. First, metal Ti and Au (300 Å and 500 Å) were successively deposited using E-gun evaporator onto the GaAs chip and Al_2O_3 substrate to form continuous seed layers for the following Au electroplating, as shown in Fig. 3(a). The plating bath was cyanide based solution. Ti was used as an adhesion layer to improve the adhesion of Au to the Al_2O_3 and GaAs materials, and Au was used as a seed layer for the following electroplating Au onto the matrix. In Fig. 3(b), thin photoresist from Shipley Company was then patterned on the chip and substrate to electroplate the circuits of the test structures. After the electroplating of the Au circuits, the thin photoresist was then removed, as shown in Fig. 3(c).

To form the vertical coaxial transition on the CPW circuits, high aspect ratio photolithography was developed, which was the key step in the whole process procedures. The used thick phototresists was from TOK Company. A double coating technique for the thick photoresist was applied to achieve the flat surface of thick photoresist on the whole sample. At each coating step, the sample was baked on the hot plate at the temperature of 120 °C for 15 min to remove the solvents. A 60-μm-thick photoresist was obtained finally. The samples were then exposed using Karl-Suss MJB-3 aligner with a broadband exposure. The masks were of film type, which was a low-cost approach with acceptable inaccuracy in the dimensions. Fig. 4 shows the SEM pictures of the photoresist profiles with different exposing and developing conditions. Fig. 4(a) and (b) shows the profiles of the thick photoresist with the best exposing and developing conditions after fine tuning. The scanning electron microscope (SEM) pictures show excellent profiles with a smooth side wall and a clean bottom surface. However, if the exposure was insufficient, serious residues remained at the bottom of the exposed areas after developing. Fig. 4(c) shows the SEM image of the serious residues. Fig. 4(d) shows

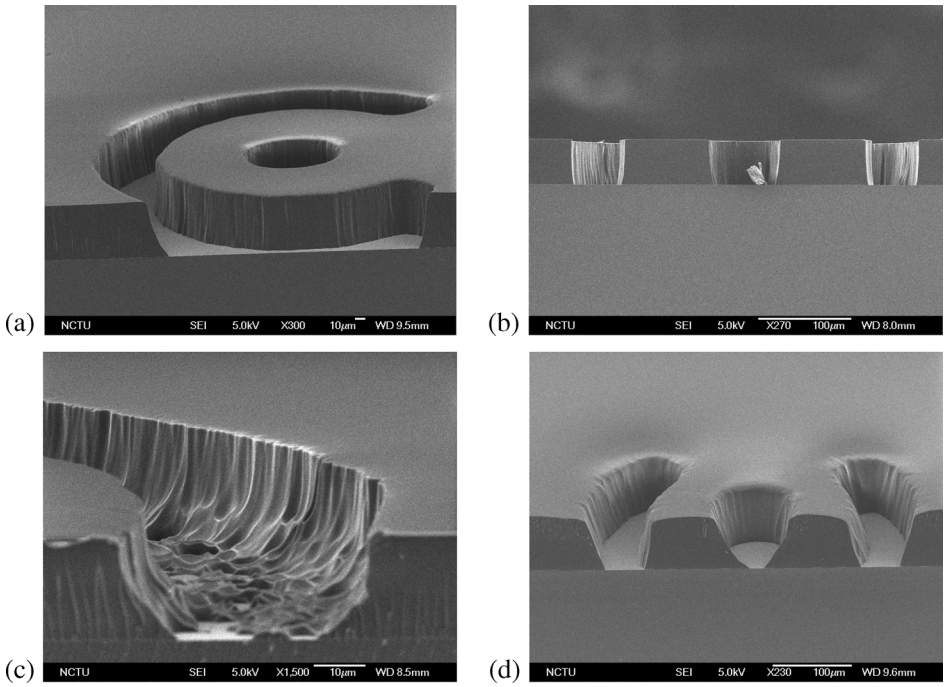

Fig. 4. SEM images of thick photoresist with different testing conditions. (a), (b) Exposing time: 9 min; developing time: 6 min. (c) Exposing time: 6 minutes; developing time: 6 min. (d) Exposing time: 9 min; developing time: 9 min.

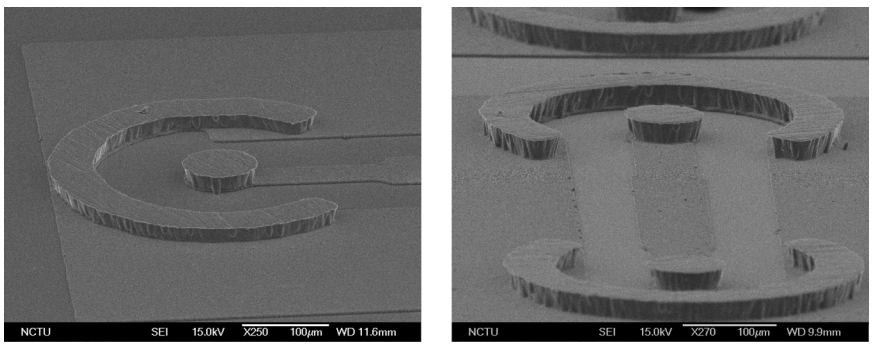

Fig. 5. SEM images of the fabricated coaxial transition structures.

the SEM image of the overdeveloped profile. An over developing time would bring a sloped side wall.

After the successful tests of the thick photoresist lithography, thick photoresist was coated; the positions and dimensions of the coaxial transitions bumps were then patterned both on the chip and substrate with the previously tested conditions, as shown in Fig. 3(d). Then, Au coaxial transitions were electroplated. By carefully controlling the electroplating current density and electroplating time, the bump of required heights were achieved, as shown in Fig. 3(e). The final step in the fabrication was the removal of the thick photoresist and seed layers. The seed layers were removed with $\mathrm{KI/I_2}$ solution for Au and HF dilute solution for Ti to finish the fabrication process, as shown in Fig. 3(f). After the thin metal etch, the test interconnect structure was successfully fabricated. The SEM images of the fabricated coaxial transition structures are shown in Fig. 5.

III. Electric and Magnetic Fields Properties of Coaxial Transition

The tool for the three dimensional electromagnetic (EM) field analysis of the coaxial interconnect structure is CST Microwave Studio. Fig. 6 shows the simulated structure. In the simulation model, the material of the substrate is alumina $(\mathrm{Al_2O_3})$, and the material of the chip is GaAs. The thickness of the alumina substrate and GaAs chip are 254 and 100 μm, respectively. The conductor metal is 3-μm gold. The transmission lines on both the chip and substrate are of CPW type.

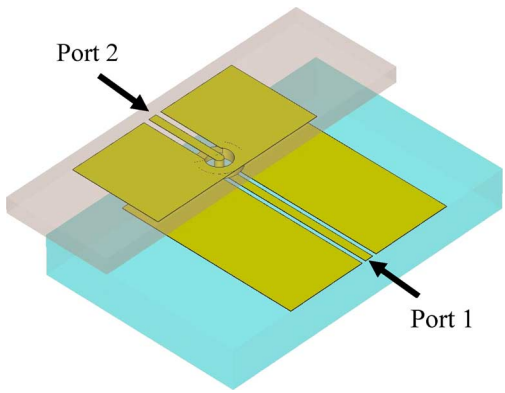

Fig. 6. Simulated flip chip interconnect structure with the proposed coaxial transition.

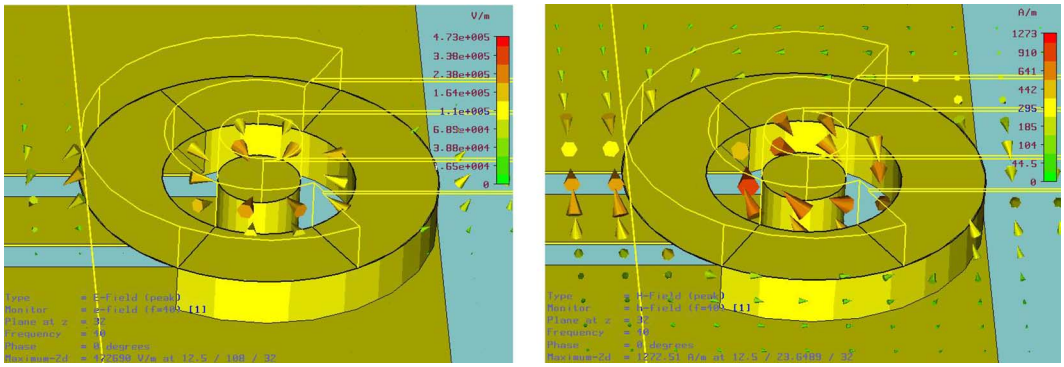

Fig. 7. (a) The electric field view of the coaxial transition. (b) The magnetic field view of the coaxial transition.

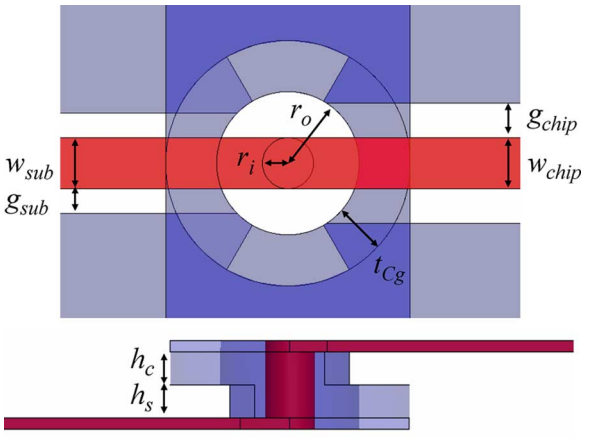

Fig. 8. Main parameters of the vertical coaxial transition are chip-side bump height (h_c), substrate-side bump height (h_s), C-shaped ground bumps wall thickness (t_{Cg}), and ratio of outer conductor radius to inner conductor radius at the coaxial transition ($R = r_o/r_i$).

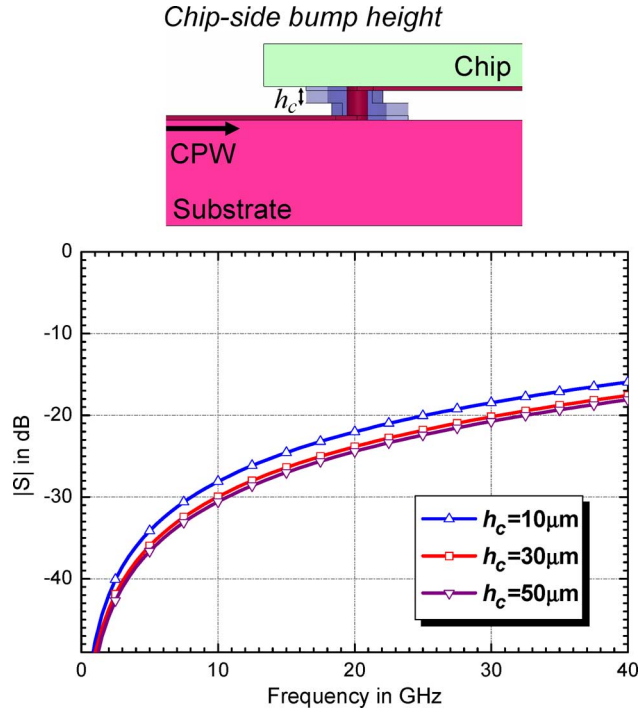

Fig. 9. Simulation results of return loss versus frequency. The parameters are various chip-side bump heights ($h_c = 10, 30, 50\ \mu$m) while h_s equals 30 μm, t_{Cg} equals 50 μm, and R equals 2.5 ($r_i = 25\ \mu$m, $r_o = 62.5\ \mu$m).

Fig. 7 shows the graphs of the electric field and magnetic filed of the proposed coaxial transition. From the plots, the coaxial transition shows better field confinement as compared to the conventional structure with three bumps at the CPW-to-CPW transitions.

IV. Parameters of Coaxial Transition and EM Simulation

The design and EM simulation of the proposed coaxial transitions are performed using the simulation tool CST Microwave Studio. The effects of the geometric parameters on the interconnect property are investigated, and the design rules are developed according to the simulation results. For the proposed coaxial transition structure, the geometric parameters in investigation are listed as follows:

1) chip-side bump height (h_c);
2) substrate-side bump height (h_s);
3) C-shaped ground bumps wall thickness (t_{Cg});
4) ratio (R) of outer conductor radius (r_o) to inner conductor radius (r_i) of the coaxial transition ($R = r_o/r_i$).

Fig. 8 shows the definitions of the parameters. The characteristic impedances (Z_0) of CPWs on the substrate and chip are 50 Ω. The signal widths on the chip ($w_{\rm chip}$) and substrate ($w_{\rm sub}$) are 50 μm. Thus, the spacing between the signal and ground on the chip and substrate are 34 μm ($g_{\rm chip}$) and 24 μm ($g_{\rm sub}$), respectively. Single flip-chip transition structure is simulated to study the reflection property of the interconnect.

Fig. 9 shows the simulation results of the return loss for different chip-side bump heights (h_c = 10 to 50 μm) while h_s, t_{Cg}, and R are 30 μm, 50 μm, and 2.5 ($r_i = 25\ \mu$m, $r_o = 62.5\ \mu$m). The results indicate that the increase in h_c from 10 to 30 μm improves the return loss by 1.6 dB at 40 GHz. However, further increase in h_c from 30 to 50 μm does not have much effect on the return loss. A similar trend as the parameter h_c is also observed for the parameter, the substrate-side bump heights (h_s).

The simulation results of return loss versus frequency with the same values of the substrate-side height and the chip-side bump height ($h_s = h_c$) are shown in Fig. 10. The results indicate that the increase in h_c and h_s from 10 to 30 μm improves the return loss by 2.6 dB at 40 GHz. Further increase in h_c and h_s from

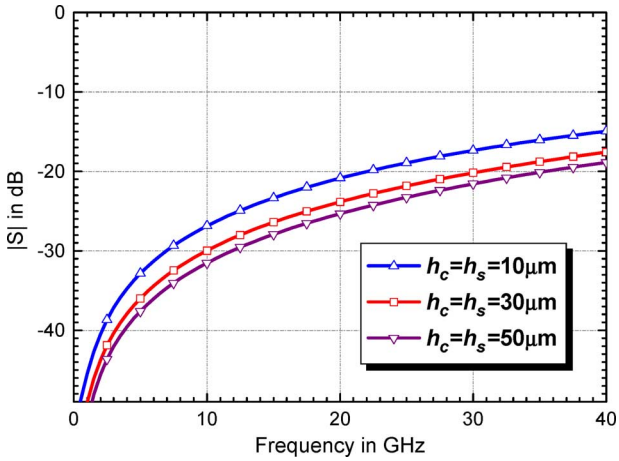

Fig. 10. Simulation results of return loss versus frequency. The parameters are various substrate-side and chip-side bump heights ($h_s = h_c = 10, 30, 50\ \mu\mathrm{m}$) while t_{Cg} equals 50 μm, and R equals 2.5 ($r_i = 25\ \mu\mathrm{m}$, $r_o = 62.5\ \mu\mathrm{m}$).

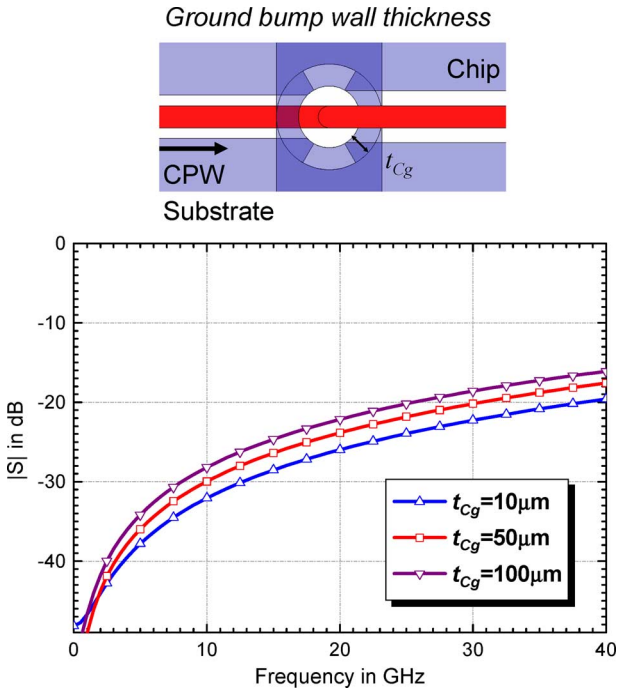

Fig. 11. Simulation results of return loss versus frequency. The parameters are various C-shaped ground bumps wall thickness ($t_{Cg} = 10, 50, 100\ \mu\mathrm{m}$) while h_c equals 30 μm, h_s equals 30 μm, and R equals 2.5 ($r_i = 25\ \mu\mathrm{m}$, $r_o = 62.5\ \mu\mathrm{m}$).

30 to 50 μm has only a small improvement of 1.2 dB at 40 GHz on the return loss.

Fig. 11 shows the simulation results of the return loss versus frequency of the third parameter, C-shaped ground bumps wall thickness (t_{Cg}) while the other parameters h_c, h_s, and R are 30 μm, 30 μm, and 2.5 ($r_i = 25\ \mu\mathrm{m}$, $r_o = 62.5\ \mu\mathrm{m}$). From the figure, it is observed that the smaller thickness (t_{Cg}) of the C-shaped bumps wall, the lower the return loss at the interconnect is achieved. As the two C-shaped ground bumps together with the center signal bump form a coaxial structure; they both go across the signal lines of the substrate and chip. In this way, the C-shaped ground bump gives a capacitive effect to the signal line and acts as a shunt capacitance. The thinner ground

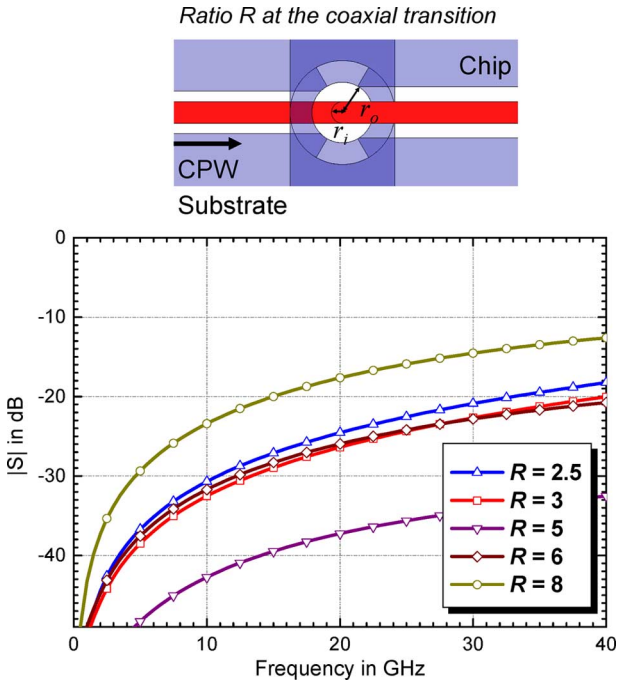

Fig. 12. Simulation results of return loss versus frequency. The parameters are various ratio of outer conductor radius to inner conductor radius of coaxial transitions ($R = r_o/r_i = 3, 4, 5, 6, 7$ while $r_i = 25\ \mu\mathrm{m}$) while h_c equals 30 μm, h_s equals 30 μm, and t_{Cg} equals 50 μm.

wall thickness (t_{Cg}) alleviates the capacitive effect and therefore helps improve the reflection property of the coaxial transition. Due to the process consideration, however, the parameter t_{Cg} can not be too small. The process limitation comes from the aspect ratio of the thick photoresist and the mask resolution. In this study, the masks are of film type, which limits the line width on the mask. The dimension of the C-shaped ground bumps wall thickness (t_{Cg}) is set to be 50 μm for the real fabricated coaxial structure in this study.

The most important parameter for the proposed coaxial transition is the ratio ($R = r_o/r_i$) of the outer conductor radius (r_o) to the inner conductor radius (r_i). Fig. 12 shows the simulation results of the return loss versus frequency of the parameter R ranging from 2.5 to 8 while the other parameters h_c, h_s, and t_{Cg} are 30, 30, and 50 μm respectively. From the figure, when R increases from 2.5 to 3, there is a small improvement in the return loss about 1.8 dB at 40 GHz. Further increase in R to 5 improves the return loss significantly. The return loss for single transition is much less than 20 dB at 40 GHz when the parameter R equals to 5, which shows very good interconnect performance. However, the return loss becomes worse when R increases further. In the case of $R = 8$, the return loss greatly degrades. From the results, it is suggested that there is an optimum value of R giving the lowest reflection at the transition.

For better understanding of the coaxial transition structure and the effect of the key parameter R, it is helpful to develop an equivalent circuit model for the coaxial transition structure. Fig. 13 shows the schematic of the coaxial transition and the developed equivalent circuit model. The associated equivalent circuit model of the coaxial transition consists of three physical transmission lines and two capacitors. The three transmission

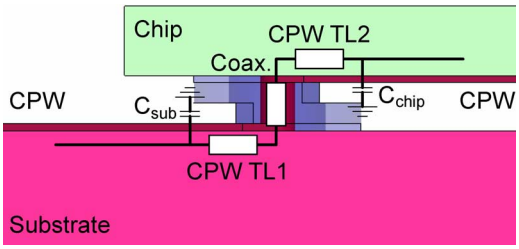

Fig. 13. Schematic of vertical coaxial transition with equivalent circuit model (TL: transmission line).

TABLE I
VERTICAL COAXIAL TRANSITION MODEL PARAMETERS ($R = 5$)

Transmission lines		
CPW TL1	Z = 66 Ω	length = 125 μm
Coaxial TL	Z = 96 Ω	length = 60 μm
CPW TL2	Z = 60 Ω	length = 125 μm
Lumped element		
C_{sub} = C_{chip} = 14 fF		

lines describe the two CPW transmission lines inside the area of the coaxial structure and the coaxial structure itself. The two capacitors are used to account for the induced capacitances of the C-shaped ground bumps to the signal lines. Table I lists the model parameters of the coaxial transition structure for the case of $R = 5$ after simulation and optimization. The shunt capacitances in the model were found to be $C_{\text{sub}} = C_{\text{chip}} = 14$ fF. The impedances of the two CPW transmission lines were calculated to be $Z_{\text{CPW-TL1}} = 66\,\Omega$ and $Z_{\text{CPW-TL2}} = 60\,\Omega$, and the impedance of the coaxial transmission line was $Z_{\text{coax}} = 96\,\Omega$. The high-impedance transmission lines, exhibiting an inductive effect, compensate the capacitive effect induced by the C-shaped ground bumps, which results in the low reflection property of the coaxial transition. When the parameter R is small, e.g. 2.5, the transition still shows an overall capacitive property because of the lower impedances (i.e. lower inductive effect) of the both CPW transmission lines and the coaxial transmission line and the excess capacitance. It explains why the increase of R from 2.5 to 3 just gives small improvement in the return loss of the transition. The further increase of R to 5 leads to higher impedance transmission lines, which enhances the inductive effect and makes the overall effect of the coaxial transition match to 50 Ω. In this case, it therefore gives the low return loss for the transition. However, when the value of R increases to 8, it results in too much inductive effect and causes an overall inductive property of the transition, which degrades the return loss.

From the simulation results, several rules for the design of the coaxial transition are concluded and summarized as follows. The higher bump height gives the lower return loss at the interconnect. The thinner C-shaped ground wall thickness also gives the lower return loss. However, these two parameters of the coaxial transition only show small improvement on the reflection property. The key parameter of the coaxial transition is the ratio R, which greatly affects the interconnect property. It is suggested that there is an optimum value of R, which gives the lowest reflection at the transition. With proper design, the proposed coaxial transition can provide good interconnect performance for the flip-chip interconnects with low return loss and low insertion loss over a broad bandwidth at high frequencies up to 40 GHz.

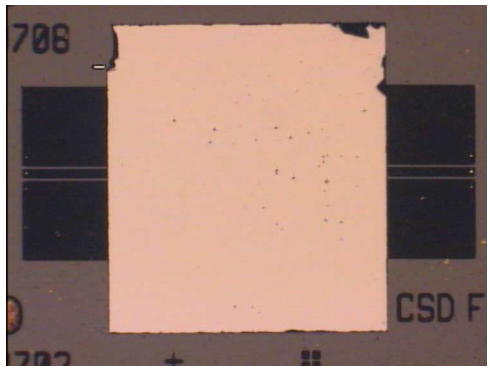

Fig. 14. Top-view photograph of one demonstrated structure.

V. EXPERIMENTAL RESULTS

According to the discussion in the previous section, the geometric parameters of the vertical coaxial transition are the bump height (h), the C-shaped ground wall thickness (t_{Cg}), and the ratio (R) of the outer conductor radius to the inner conductor radius at the coaxial transition, where R is the key design parameter. To demonstrate the proposed coaxial transition for the flip-chip application and verify the design rules, we have fabricated the back-to-back flip-chip interconnect structures with the vertical coaxial transitions for the various ratios (R) by using the in-house developed fabrication process, which has been presented and described in detail in Section II. The thermo-compression method was used to flip-chip bond the demonstrated samples. The compression during the bonding operations would bring some small changes to the original geometry of the coaxial transition. The bonding conditions were tested and optimized to avoid too much deformation of the bumps. However, it should be noticed that the best thermo-compression bonding conditions still caused little deformation of the bumps, including the reduction in the bump height and the shift in the parameter R of the coaxial transition. Fig. 14 shows the photograph of one flip-chip bonded interconnect structure. The scattering parameters of the test structures were then measured up to 40 GHz by the on-wafer probing measurement system with the Anritsu 37369C vector network analyzer.

For the demonstrated structures, the designed signal width of 50 Ω CPW was 70 μm both on Al_2O_3 substrate and on GaAs chip. The inner conductor radius (r_i) at the coaxial transition was 35 μm. The C-shaped ground bump wall thickness (t_{Cg}) was 50 μm. The height of the coaxial-type bump (h_c and h_s) was 30 μm both on the chip and substrate before flip-chip bonding. The interconnect structures with the various designed ratios (R) ranging from 3 to 6 were fabricated and RF characterized. Fig. 15 shows the measurement results of the insertion loss versus frequency of the CPW transmission line on the Al_2O_3 substrate and the flip-chip interconnect structure with the coaxial transitions where the designed $R = 3$. These two structures have equal length. Compared with the CPW transmission

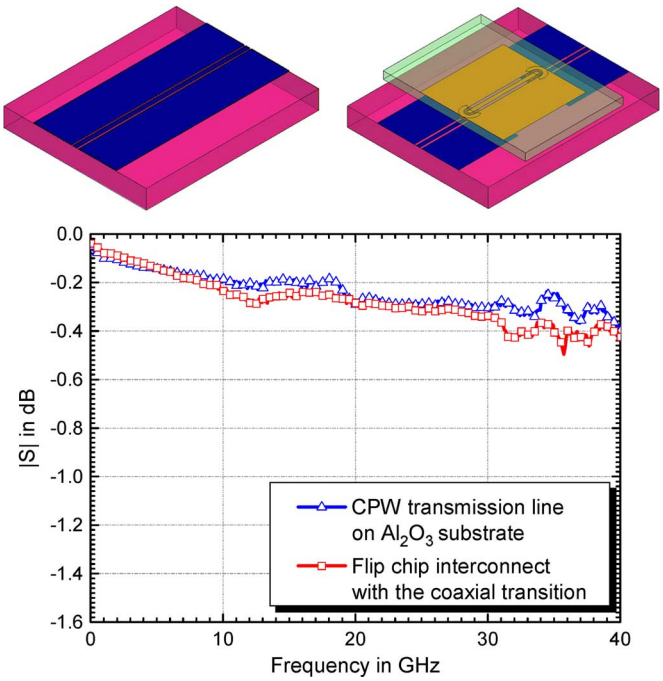

Fig. 15. Measurement results of insertion loss versus frequency. Comparison between the CPW transmission line and the flip chip interconnect structure with the proposed coaxial transition ($R = 3$).

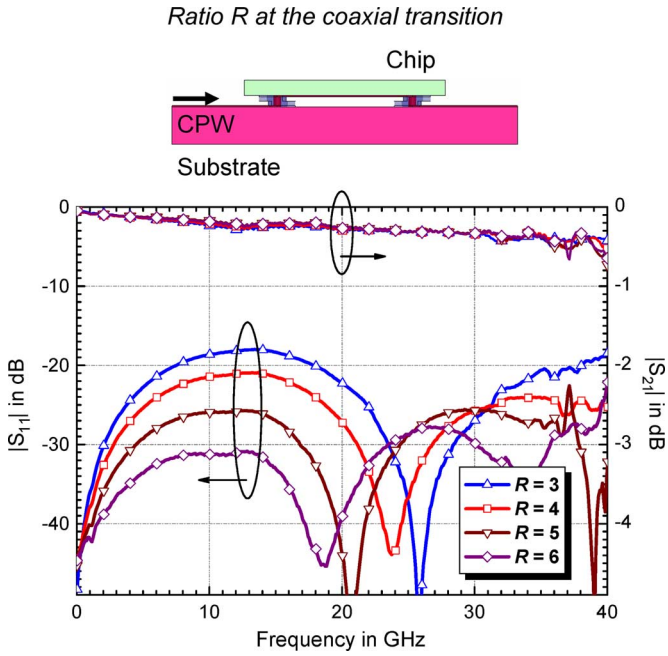

Fig. 16. Measurement results of return loss versus frequency. The parameters are various ratio of outer conductor radius to inner conductor radius of coaxial transitions ($R = r_o/r_i = 3, 4, 5, 6$) while h_c equals 30 μm, h_s equals 30 μm, t_{Cg} equals 50 μm.

line on the Al_2O_3 substrate, there are two more vertical coaxial transitions for the case of the flip-chip interconnect structure. Even so, from dc to 30 GHz, it shows no additional insertion loss. Above 30 GHz, the insertion loss only increases less than 0.1 dB.

Fig. 16 shows the measurement results of the return loss and the insertion loss versus frequency of the designed parameter R. In the figure, the measurement data show a similar trend as the simulation results. It can be seen that the best performance with a very low return loss was achieved for the designed parameter $R = 6$. From dc to 40 GHz, the return loss was less than 25 dB. The idea of the proposed coaxial transition for the flip-chip interconnects is clearly verified. However, it should be noticed that in reality the designed R shifted a little to the lower-value range because the thermo-compression bonding changed the originally designed parameter R. By SEM examination and calculation, for the case of the designed $R = 6$, it could be verified the designed parameter R was shifted to the value about 5. The designed coaxial transition structure was different from the real situation of the fabricated structure. This explains the phenomenon that the simulation and measurement results indicate the different optimum values for the parameter R. This should be taken into consideration in advance at the design stage.

About the performance comparison between the conventional three-bump (G-S-G) flip-chip interconnect structure and the proposed coaxial interconnect structure, there is actually no fair starting point to do the comparison because the proposed coaxial interconnect structure is completely different from the conventional one. Without compensation design, the return loss of the conventional flip chip interconnect was only about 18 dB from dc to 40 GHz [1], [2]. However, with high impedance compensation design at the transition, the return loss of the conventional one was further improved, which could be below 20 dB from dc to 40 GHz as indicated in [1]. In this study, the flip-chip interconnect structure using the proposed coaxial transition demonstrates an excellent reflection property below 20 dB from dc to 40 GHz as well. However, for the dimensional comparison with the conventional flip-chip structure, the coaxial approach requires a little more area in order to form the coaxial structure at the vertical transition.

After thermo-compression bonding, the designed parameters of the coaxial transition structure have changed. Therefore, we used the CST simulator to re-simulate the coaxial transition structure with the consideration of the reality. The coaxial transition model data were then exported from the CST simulator and inserted into the Agilent ADS circuit simulation tool to simulate the full back-to-back flip-chip interconnect structure. Fig. 17 shows the modeling circuits of the flip-chip interconnect structure with the vertical coaxial transition for the case of the designed parameter $R = 3$. The same modeling circuits were also used to simulate the interconnect structures with the different designed ratios R. The dimensions for the CPWs on the chip and the substrate are also shown in the figure.

The comparison between the simulated and the measured data is shown in Fig. 18. For the cases of $R = 3$, 4, and 5, the modeled and simulated curves show almost the same profiles. In the case of $R = 6$, the simulated and measured curves just show little difference. The simulated and measured results show excellent agreement, which validates the accuracy of the transition data exported from the EM wave simulation tool. In this way, designers can predict the final performance of the assembled circuits in the system. It also means that one can take the vertical coaxial transitions and interconnects into consideration in advance at the design stage to anticipate the circuit performance after packaging and have beforehand optimization.

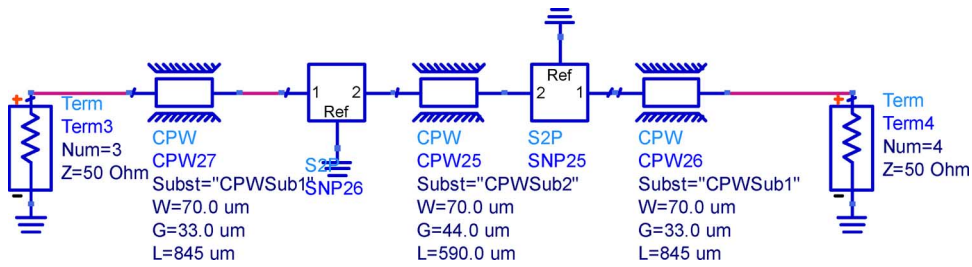

Fig. 17. Modeling of the back-to-back interconnect structure with the EM simulated transition model inserted.

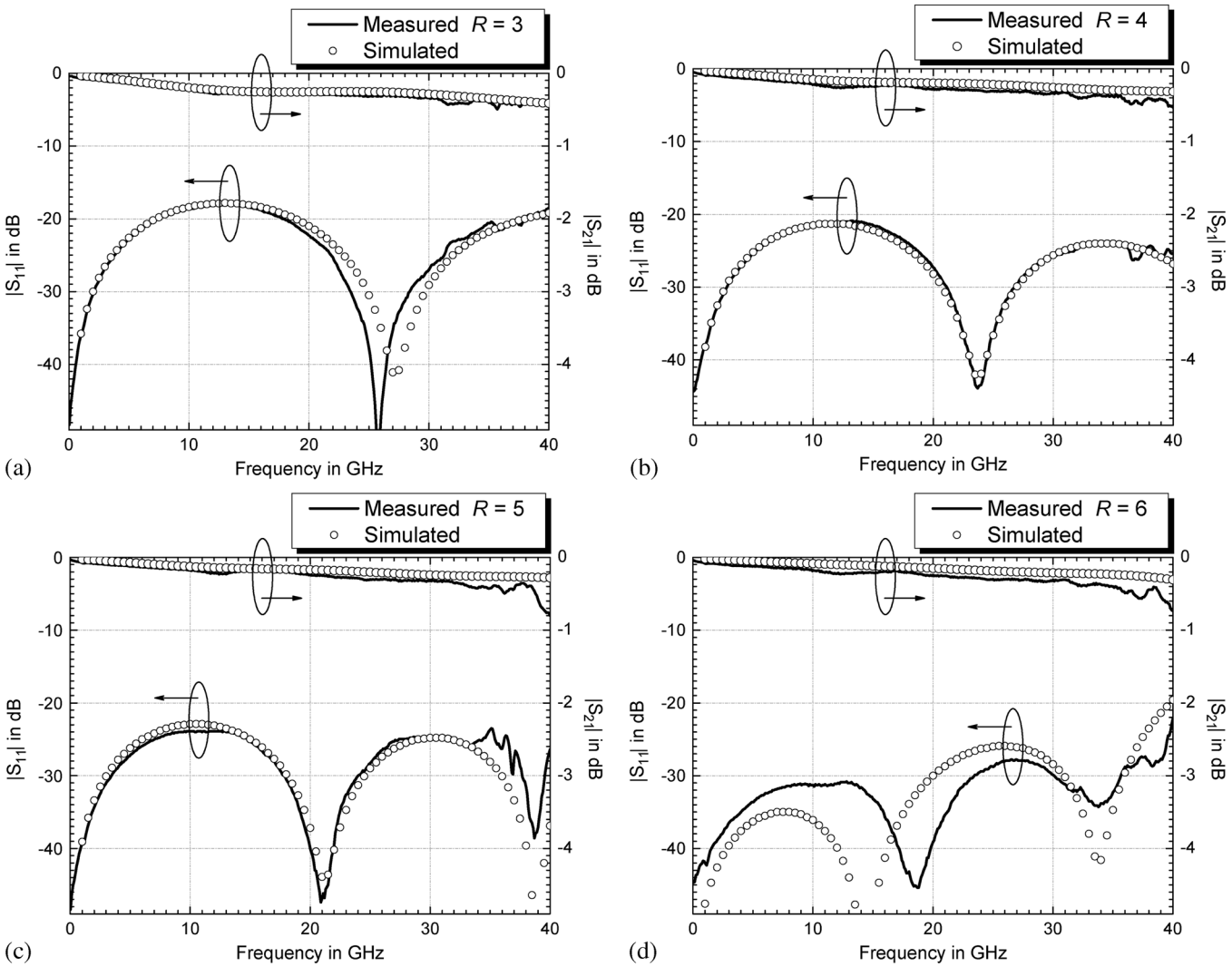

Fig. 18. The simulated and measured results of the flip chip interconnect structure with the different designed ratios R of the coaxial transitions.

VI. Conclusion

The novel coaxial transitions for flip-chip interconnects have been proposed and demonstrated for the first time in this study. To realize the coaxial transition for the flip chip interconnects, the complete fabrication process has been successfully developed. By performing the full wave electromagnetic simulation, the proposed coaxial transition has demonstrated the real coaxial properties. The physical parameters of the coaxial transition structure are well indicated; their effects on the interconnect performance are also well investigated. The design parameters for the coaxial transition are the bump height, the C-shaped ground wall thickness, and the ratio of the radius of the outer conductor to the radius of the inner conductor. Based on the EM simulation results, several rules for the design of the coaxial transition are developed. Higher bump height and thinner C-shaped ground wall thickness show a small improvement in reflection property at the interconnect. The key

design parameter in the coaxial transition design is the ratio R, which greatly affects the interconnect property. An optimum value of R gives the lowest reflection at the transition. The design concepts of the coaxial transition have been validated through the realization of the coaxial transition on the flip chip interconnects. The characterized results of the interconnect structures showed excellent performance, where no additional insertion loss was observed and the return loss was better than 25 dB from dc up to 40 GHz. The coaxial transition has been well modeled and extracted from the EM simulator; the simulated data showed good agreement with the measured data. The proposed coaxial transition has shown great potential as the candidate for flip-chip interconnects in the millimeter wave packaging applications.

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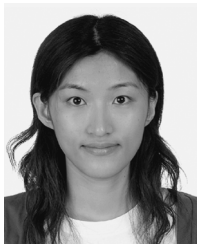

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