Distinguishing Between STI Stress and Delta Width in Gate Direct Tunneling Current of Narrow n-MOSFETs

Chen-Yu Hsieh, *Student Member, IEEE*, Yi-Tang Lin, and Ming-Jer Chen, *Senior Member, IEEE*

***Abstract*—Direct tunneling current across a 1.27-nm-thick gate oxide of n-MOSFETs under STI compressive stress is measured in a wide range of the drawn gate width W $(= 0.11, 0.24, 0.6, 1.0$ and $10\ \mu m)$. The *apparent* gate current per unit width exhibits an increasing trend with decreasing W. In this narrowing direction, two fundamentally different effects are encountered: one of the delta width (ΔW) near the STI edge, and the other of the enhanced STI stress in the channel. To distinguish between the two effects, a new analytical width-dependent direct tunneling model is developed and applied. Reasonable agreement with data is achieved. The resulting delta width effect is found to dominate over the stress effect in narrow devices, while for the wide ones, they are comparable. The extracted ΔW $(\sim 63$ nm) and the underlying channel stress (with the uncertainties identified) straightforwardly produce a good fitting of the drain current variation counterpart. Specifically, it is justified that the delta width and STI stress are cooperative in constituting gate current variation, but both have opposite effects on the drain current one.**

***Index Terms*—Delta width, layout, mechanical stress, MOSFET, piezoresistance, shallow trench isolation (STI), tunneling.**

I. Introduction

THE significance of the shallow-trench-isolation (STI)-induced mechanical stress in highly scaled MOSFETs has been widely recognized [1]. The linkage between layout design and the underlying STI stress has also been well constructed [2]–[4]. Further applications pertaining to the layout dependences of the STI-stress-altered dopant diffusion [5], [6], gate direct tunneling [6], [7], threshold voltage [6]–[8], subthreshold leakage [6], [8], and mobility [2], [4], [6], [7] have all been successfully demonstrated. However, care must be taken in the narrowing direction. The STI channel stress may be enhanced, but on the other hand, the delta width due to STI corner rounding is increasingly important. Thus, the ability to distinguish the delta width effect from the STI stress one is essential. Two such examples on drain current variation have recently been published [9], [10]. However, so far, effects on the gate direct tunneling counterpart were not yet addressed. Here, we elaborate on how to unambiguously elucidate the STI-stress-altered gate direct tunneling current in narrow devices.

Manuscript received October 7, 2008; revised January 31, 2009. First published March 31, 2009; current version published April 28, 2009. This work was supported by the National Science Council of Taiwan under Contract NSC 95-2221-E-009-295-MY3. The review of this letter was arranged by Editor K. De Meyer.

The authors are with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: chenmj@faculty.nctu.edu.tw).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2009.2015471

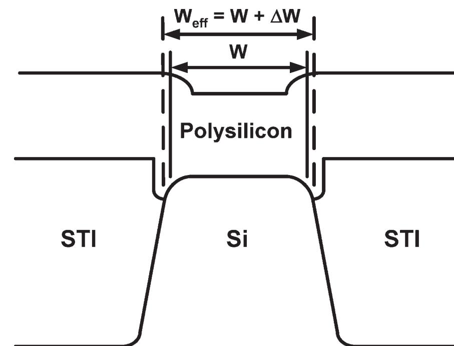

Fig. 1. Schematically drawn cross-sectional view of the device in the channel width direction, which can be obtained from the existing simulated device structure in a state-of-the-art manufacturing process [3]. The effective channel width designated W_{eff} is the drawn width W plus the delta width ΔW.

II. Experimental Setup

Some 1.27-nm gate oxide n-channel MOSFETs on (001) wafer were fabricated in a state-of-the-art manufacturing process. In this process, STI-induced compressive stress was applied. The gate-edge-to-STI spacing in the source diffusion, the gate length L along the direction $\langle 110 \rangle$, and the gate-edge-to-STI spacing in the drain diffusion were all fixed at 0.5 μm. The cross-sectional view of the test device is schematically shown in Fig. 1. The drawn gate width W spanned in a wide range of 0.11, 0.24, 0.6, 1.0, and 10 μm. The gate direct tunneling current was measured in inversion, with the source, drain, and substrate being tied to the ground. The change percentage of the *apparent* gate current per unit width, which is the actual gate current divided by corresponding W with respect to $W = 10\ \mu$m, is plotted in Fig. 2 versus W.

III. Data Fitting and Parameter Extraction

As shown in Fig. 1, the actual channel width designated W_{eff} is the drawn gate width plus the delta width: $W_{\text{eff}} = W + \Delta W$. The corresponding stress-altered gate tunneling current density can be expressed as a linear function of both the average longitudinal channel stress σ_x and the average transverse channel stress σ_y, which was obtained via a triangular potential-based

0741-3106/$25.00 © 2009 IEEE

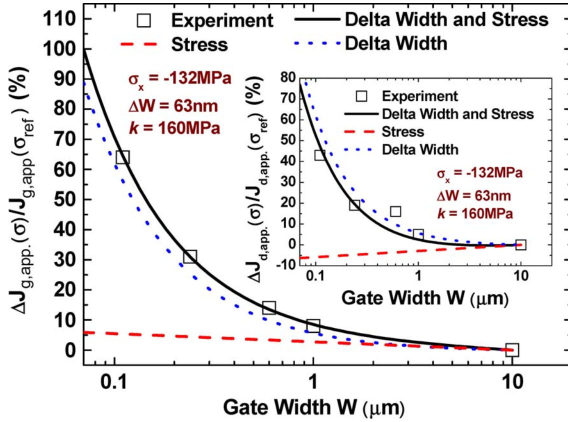

Fig. 2. Relative change of the *apparent* gate current per unit width at $V_g = 1$ V versus drawn gate width. The lines represent the calculated results. For the narrowest case $W = 0.11$ μm, the delta width effect contributes 56%, while the remaining percentage (5.5%) stems from the stress-induced SiO_2/Si barrier lowering. The combination of both effects produces a 65% change in the *apparent* gate current density. For sufficiently large W, however, both effects become comparable. The inset shows the relative change of the *apparent* drain current per unit width at $V_d = 1$ V and $V_g = 1$ V versus drawn gate width, along with the calculated results. Note that the piezoresistance coefficients used are the typical bulk values, which are close to those of the inversion-layer ones of state-of-the-art strained n-MOSFETs [12], valid only for the channel $\langle 110 \rangle$ direction on (001) wafer, as studied in this letter. $\Delta W = 63$ nm, $\sigma_x = -132$ MPa, and $k = 160$ MPa.

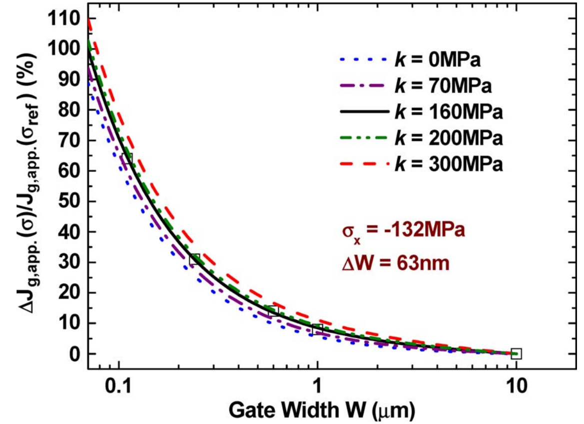

Fig. 3. Comparison of (symbols) gate current data corresponding to Fig. 2 with the calculated results. $\Delta W = 63$ nm, $\sigma_x = -132$ MPa, and with $k = 0{-}300$ MPa.

quantum simulation while incorporating the longitudinal and transverse stress dependences of the subbands [11]

$$\frac{\frac{I_g(\sigma)}{W+\Delta W} - \frac{I_g(0)}{W_{\rm ref}+\Delta W}}{\frac{I_g(0)}{W_{\rm ref}+\Delta W}} = a_x\sigma_x + a_y\sigma_y. \quad (1)$$

Here, the proportionality constants a_x and a_y are both equal to -1.745×10^{-10} $\rm m^2/Nt$. The same proportionality constant value was also utilized in our previous work concerning the longitudinal channel stress [6], [7]. On the basis of the 2-D STI stress distributions [3], [10], a certain relationship can be found: $\sigma_y = k \log(W/W_{\rm ref})$, where k is constant. Since only for sufficiently small W can the gate current variation be significantly noticed, the transverse channel stress at reference $W_{\rm ref}$ $(= 10$ μm) can be reasonably ignored.

By substituting the aforementioned logarithm form into (1), a new analytic model for the *apparent* gate tunneling current change can be straightforwardly derived

$$\frac{\Delta J_{g,\rm app.}(\sigma)}{J_{g,\rm app.}(\sigma_{\rm ref})} = \frac{\frac{I_g(\sigma)}{W} - \frac{I_g(\sigma_{\rm ref})}{W_{\rm ref}}}{\frac{I_g(\sigma_{\rm ref})}{W_{\rm ref}}}$$
$$= \frac{1+a_x\sigma_x+a_yk\log\frac{W}{W_{\rm ref}}}{1+a_x\sigma_x}\,\frac{W+\Delta W}{W_{\rm ref}+\Delta W}\,\frac{W_{\rm ref}}{W} - 1. \quad (2)$$

Here, the reference stress $\sigma_{\rm ref}$ corresponds to a fixed longitudinal stress under which the data were measured. First of all, according to the previous work [6], [7], σ_x under the same gate-to-STI spacing $(= 0.5$ μm) was estimated to be -132 MPa. Then, least squares fitting using (2) produced $k = 160$ MPa and $\Delta W = 63$ nm. The fitting quality is excellent over W, as shown in Fig. 2. The extracted ΔW is close to that of the existing simulated device structure (see [3, Fig. 5]). Therefore, in our work, the logarithmic form serves as a good approximation for W down to 0.11 μm, which is comparable with that (0.15 μm in the drain current fitting) of [10]. Further calculations were conducted for the two cases: 1) stress only, namely, (2) with $\Delta W = 0$, and 2) delta width only or (2) with $\sigma_x = 0$ and $k = 0$. The resulting delta width dominates over the stress in narrow devices, while for the wide ones, they are comparable. Note that both effects are cooperative in constituting gate current variation.

Obviously, ΔW is the principal factor. Thus, under the constraint of $\Delta W = 63$ nm, we performed additional calculations for different values of k. The results are shown in Fig. 3. Here, the uncertainty range of k between 70 and 200 MPa appears to deliver reasonable fitting. Moreover, we changed σ_x to those between -70 and -200 MPa; however, no noticeable change in the calculated gate current [directly from (2)] can be found (not shown here). Note that if σ_x is much larger in magnitude than σ_y, (2) reduces to the case of delta width only. Further calculation was conducted concerning the possibility that the narrowing action may affect σ_x. The corresponding gate current change for σ_x at $W = 0.11$ μm relative to σ_x $(= -132$ MPa) at $W = 10$ μm is shown in Fig. 4. Fig. 4 reveals that the effect of varying σ_x due to the narrowing action on data fitting is considerably weak.

IV. Confirmative Evidence

The change percentage of the *apparent* drain current per unit width at $V_d = 1$ V and $V_g = 1$ V is inserted to Fig. 2. The existing piezoresistance coefficients were cited for the fractional mobility change [12]: $\Delta\mu(\sigma)/\mu(0) = \pi_x\sigma_x + \pi_y\sigma_y$, where $\pi_x = 3.16 \times 10^{-10}$ and $\pi_y = 1.76 \times 10^{-10}$ $\rm m^2/Nt$. The measured threshold voltage shift was less than 5 mV, and therefore, the gate voltage minus the threshold voltage $V_{\rm th}$ remains unchanged. Then, according to the long-channel saturation drain current expression $I_{\rm dsat} = \mu C_{\rm inv}(W + \Delta W)(V_g - V_{\rm th})^2/2L$, where $C_{\rm inv}$ is the gate capacitance in inversion, another analytic model, which has the same expression as (2) but with a_x and

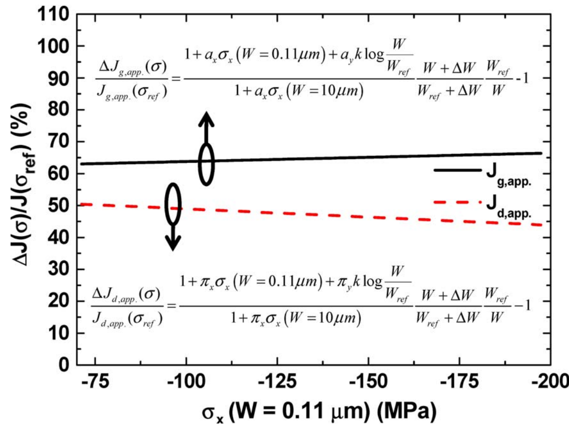

Fig. 4. Calculated gate and drain current change versus σ_x (from -70 to -200 MPa) at $W = 0.11$ μm relative to the nominal σ_x $(= -132$ MPa) at $W = 10$ μm. The formulas used are inserted. $\Delta W = 63$ nm and $k = 160$ MPa.

a_y being replaced by π_x and π_y, respectively, can be created for the drain current variation. Although the mobility in near equilibrium may not be the same as that in the saturation regime of operation, the same piezoresistance coefficients can essentially apply to the *relative* mobility change due to the applied mechanical stress. This argument remains reasonable for the long-channel devices used in this letter. The calculated results agree with data, as shown in the inset of Fig. 2. Analogous to the gate current case, the measured drain current was separated into the delta width only and the channel stress only. However, these two distinct effects exhibit opposite trends. Again, the effect of varying σ_x due to the narrowing action appears to be weak, as shown in Fig. 4.

V. Conclusion

We have systematically examined the delta width and channel stress effects on the gate direct tunneling current of narrow n-MOSFETs under STI compressive stress. Both effects have been decoupled using a new analytic direct tunneling model. The validity of the extracted transverse channel stress and delta width has been confirmed. The effect of varying longitudinal channel stress due to the narrowing action has been addressed. The corroborating evidence in terms of the drain current variation has been presented.

References

[1] G. Scott, J. Lutze, M. Rubin, F. Nouri, and M. Manley, "NMOS drive current reduction caused by transistor layout and trench isolation induced stress," in *IEDM Tech. Dig.*, 1999, pp. 827–830.

[2] R. A. Bianchi, G. Bouche, and O. Roux-dit-Buisson, "Accurate modeling of trench isolation induced mechanical stress effects on MOSFET electrical performance," in *IEDM Tech. Dig.*, 2002, pp. 117–120.

[3] Y. M. Sheu, C. S. Chang, H. C. Lin, S. S. Lin, C. H. Lee, C. C. Wu, M. J. Chen, and C. H. Diaz, "Impact of STI mechanical stress in highly scaled MOSFETs," in *Proc. Int. Symp. VLSI-TSA*, 2003, pp. 76–79.

[4] C. Gallon, G. Reimbold, G. Ghibaudo, R. A. Bianchi, R. Gwoziecki, S. Orain, E. Robilliart, C. Raynaud, and H. Dansas, "Electrical analysis of mechanical stress induced by STI in short MOSFETs using externally applied stress," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1254–1261, Aug. 2004.

[5] Y. M. Sheu, S. J. Yang, C. C. Wang, C. S. Chang, L. P. Huang, T. Y. Huang, M. J. Chen, and C. H. Diaz, "Modeling mechanical stress effect on dopant diffusion in scaled MOSFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 1, pp. 30–38, Jan. 2005.

[6] C. Y. Hsieh and M. J. Chen, "Electrical measurement of local stress and lateral diffusion near source/drain extension corner of uniaxially stressed n-MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 844–849, Mar. 2008.

[7] C. Y. Hsieh and M. J. Chen, "Measurement of channel stress using gate direct tunneling current in uniaxially stressed nMOSFETs," *IEEE Electron Device Lett.*, vol. 28, no. 9, pp. 818–820, Sep. 2007.

[8] C. Pacha, M. Bach, K. von Arnim, R. Brederlow, D. Schmitt-Landsiedel, P. Seegebrecht, J. Berthold, and R. Thewes, "Impact of STI-induced stress, inverse narrow width effect, and statistical V_{TH} variations on leakage currents in 120 nm CMOS," in *Proc. Eur. Solid-State Device Res. Conf.*, 2004, pp. 397–400.

[9] P. B. Y. Tan, A. V. Kordesch, and O. Sidek, "Analysis of deep submicron CMOS transistor Vtlin and Idsat versus channel width," in *Proc. Asia-Pacific Microw. Conf.*, 2005, pp. 1569–1572.

[10] R. Li, L. Yu, H. Xin, Y. Dong, K. Tao, and C. Wang, "A comprehensive study of reducing the STI mechanical stress effect on channel-width-dependent I_{dsat}," *Semicond. Sci. Technol.*, vol. 22, no. 12, pp. 1292–1297, Nov. 2007.

[11] Y. T. Lin, "Strained silicon physics in nanoscale MOSFETs," M.S. thesis, Nat. Chiao-Tung Univ., Hsinchu, Taiwan, 2008.

[12] S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-process-induced strained-Si: Extending the CMOS roadmap," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1010–1020, May 2006.