A 24-GHz CMOS Current-Mode Power Amplifier with High PAE and Output Power

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***Abstract*—A new 24-GHz CMOS current-mode power amplifier in 0.13-μm CMOS technology is proposed. By using the two-stage cascade current-mirror structure, the power amplifier has a maximum output power of 17.8 dBm, the OP_{1dB} of 13.8 dBm and the power gain of 23 dB under the supply voltage of 1.2V and the total power dissipation of 239 mW. As compared to other PAs at 17~24 GHz, the proposed current-mode PA has the highest power added efficiency (PAE) of 34.6% and the largest output power.**

I. INTRODUCTION

Recently, the research on radio frequency (RF) ICs in 24-GHz-band has been accelerated because of the potential Industrial, Scientific, and Medical (ISM) band and the wireless vehicular radar applications [1]-[4]. It is known that CMOS technology is capable to implement RF transceivers at 24 GHz. The most critical key block in a CMOS 24-GHz RF transceiver is the power amplifier (PA). As compared with GaAs and pHEMT technologies, standard CMOS technology has the inherent characteristics of low unity-power-gain frequency and lossy on-chip passive elements. This makes the design of RF CMOS PAs with high output power and high power added efficiency (PAE) very challenging. Although the output power can be increased by utilizing multiple parallel transistors [5], the PAE cannot be increased in such a structure. To improve the PAE, several design techniques have been proposed. By using the special structure of transmission line and additional algorithms, the PAE of a RF CMOS PA can be improved to around 10% [6]-[7].

So far, all RF CMOS PAs have been designed in voltage-mode operation. However, current-mode design has the advantages of low-voltage operation and low power dissipation. Moreover, the overall amplifier gain comes from amplifying current instead of voltage. Thus the constraint on the upper limit of supply voltage can be avoided.

In this work, a new 24-GHz current-mode power amplifier is proposed and analyzed in 0.13-μm CMOS technology. From the simulation results, the proposed PA has 34.6% peak PAE at 17.8-dBm output power. As compared with other PAs at 17-24 GHz, the proposed current-mode PA has the highest PAE and largest output power.

II. CIRCUIT DESIGN

The proposed 24-GHz current-mode PA shown in Fig. 1 is designed in 0.13-μm CMOS technology. The MOS devices M_1 and M_2 form a driver-stage current mirror and M_3 and M_4 form an output-stage current mirror. The inductors L_{c1}, L_{cb}, and L_{c4} are used to resonate with the gate capacitors of M_1, M_2/M_3, and M_4, respectively. The device capacitance between gate and drain of M_2 (M_4) is resonated by the inductor L_{gd2} (L_{gd4}). L_{gd2} and L_{gd4} are used in both stages in order to obtain higher reverse isolation. The capacitor C_1 and the inductor Lc1 serve as the input matching network. The capacitor C_4 and the inductor L_4 are the output impedance transfer network determined by load-pull simulation. C_{p1} (C_{p2}) represents the capacitance of input (output) pad.

The MOS dimension of M_4 in the output-stage current mirror shown in Fig. 2 is determined by the maximized power gain with the unity size of M_3. To find the optimal size of M_4, the width of MOS M_4 is swept from 50μm to 400μm, with 50-μm steps. The 50-μm step is realized by multiplying 2.5-μm*20-fingers because 20-finger structure has the largest maximum available gain (MAG) at 24 GHz in 0.13-μm CMOS technology. Because the output stage is simulated without the driver stage, an additional input matching network L_3 and C_3 has been added in order to transfer the input impedance of the output stage to the 50-ohm input port. The ideal capacitor C_4 is only used as a DC blocking. The optimized output impedance transfer network is determined by the load-pull simulation and not shown in Fig. 2. The values of C_3, L_3, L_{c3}, L_{c4}, and L_{gd4} are re-determined for each sweeping step. Ideal inductors and capacitors are used in sweeping process for simplicity. The load-pull technique for output impedance transfer network is simulated after the dimensions of all components have been determined. In load-pull simulation, input power is manually changed to see the power gain, 1-dB compression point (P_{1dB}), PAE at P_{1dB}, peak PAE, input power corresponding to peak PAE, and maximum output power corresponding to that input power. The results are shown in Figs. 3 and 4.

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In Fig. 4, $PAEP_{1dB}$ means the PAE at P_{1dB} and PeakPAE means maximum PAE, IP_{peak} means input power at peak PAE and OP_{max} means the maximum output power corresponding to IP_{peak}. As may be seen from Figs. 3 and 4, the OP_{1dB} value is increased with the increasing width of M_4. Further increasing the width, the power gain saturates. OP_{max} has the same trend as OP_{1dB}.

Based on two reasons, the final choice of the width of M_4 is 300 μm. The first reason is that OP_{max} should be kept not larger than 20 dBm [8]. The second one is to consider the current density of the inductor L_{c4}. After changing each ideal component to practical one, the performance parameters of the output stage can be obtained. The results are peak PAE of 53.9%, IP_{peak} of 11.9 dBm, and OP_{max} of 19.52 dBm.

Because the peak PAE operation is desired, a driver-stage shown in Fig. 5 is required to provide around 11.9-dBm input power to the output-stage current mirror. The sweeping process of the device size in the driver-stage current mirror is similar to that of device size in the output-stage current mirror. The sweeping range is from 10μm to 50μm, with 10-μm steps. Based on the required input power of the output-stage current mirror, the slave transistor width of 50μm in the driver-stage current mirror has been chosen. After using practical components, the driver-stage current mirror has peak PAE of 41.9 %, IP_{peak} of 5.8 dBm, and OP_{max} of 11.31 dBm.

According to the chosen device sizes in both stages, the impedance seen from the drain of MOS M_3 is much smaller than the impedance seen from the drain of MOS M_2 at 24 GHz. This property allows signal current going through without inter-stage matching network. Besides, two inductors L_{c2} and L_{c3} can be replaced by only one inductor L_{cb} to reduce physical area.

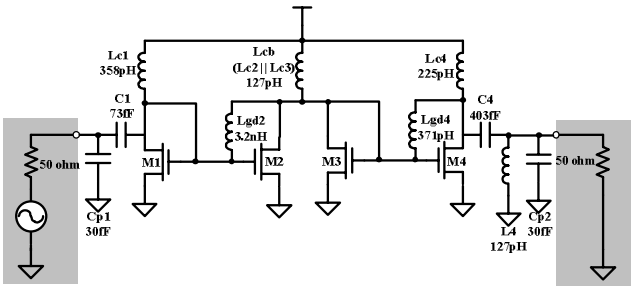

Figure 1. Two-stage current-mode power amplifier

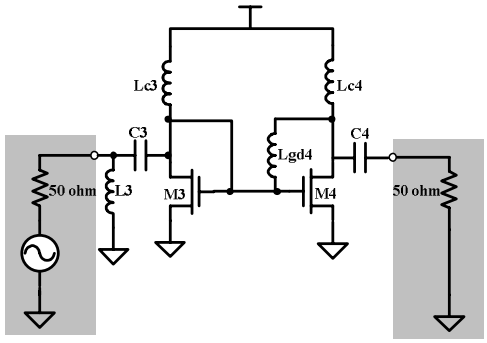

Figure 2. Output-stgae current mirror

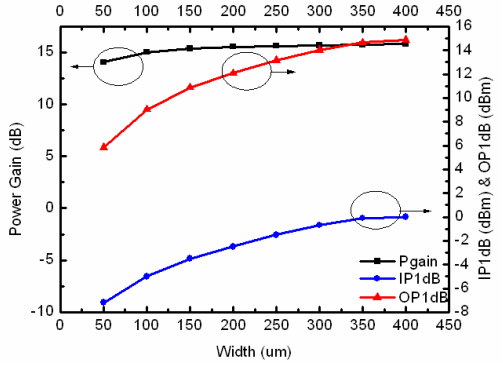

Figure 3. Power gain and P_{1dB} v.s. output-stage device size

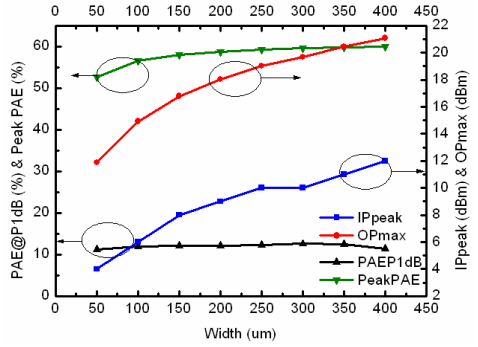

Figure 4. PAE, IP_{peak} and OP_{max} v.s. output-stage device size

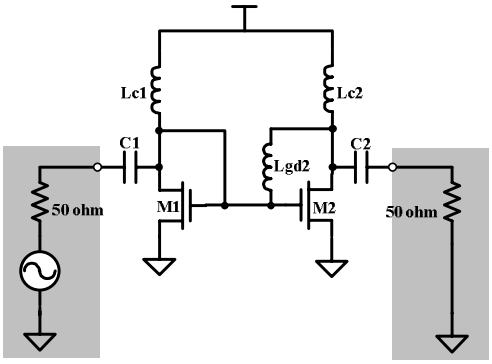

Figure 5. Driver-stage current mirror

III. SIMULATION RESULTS

The proposed CMOS current-mode PA of Fig. 1 is simulated by the Advanced Design System (ADS). All device models such as MOS, inductors, and capacitors are provided by 0.13-μm CMOS technology. The PA is operated at 1.2-V power supply with the total current of 199 mA.

Fig. 6 shows S_{11}, S_{12}, S_{21} and S_{22} between 15 GHz to 40 GHz. S_{11} is -47 dB at 24 GHz and smaller than -15 dB between 23.4 GHz to 24.7 GHz. S_{12} is -65 dB at 24 GHz and lower than -40 dB between DC to 40 GHz. This is because inductors are used to resonate C_{gd} of both MOS M_2 and M_4 at 24 GHz. High reverse isolation keeps input-matching the same before and after the output impedance is loaded. S_{21} is 23.37 dB at 24 GHz and its 3-dB bandwidth is 3.3 GHz (23.3 GHz~25.6 GHz). S_{22}, depending on output matching network, is around -8 dB. In the PA design, instead of conventional impedance conjugate matching, large signal output matching is considered. This leads to a low S_{22} value.

Output power and PAE versus input power is shown in Fig. 7 where the linear power gain (slope of P_{out} versus P_{in}) is 23.35 dB. Input- and output-refer 1-dB compression points are -8.5 dBm and 13.84 dBm, respectively. The PAE is 10.59 % at 1-dB compression point. The peak PAE is 34.64% with 7-dBm input power and 17.84-dBm output power. Slight difference between power gain and S_{21} comes from low S_{22} [9]. Because the optimized load impedances are different for both peak PAE and maximum output power as shown in Fig. 7, a trade-off between PAE and output power leads to the output power not as high as 19.52 dBm. Although the peak PAE occurs at the input power of 7 dBm, PAE can still be larger than 30 % when the input power is reduced to 0 dBm. The resultant decrease of output power is smaller than 0.5 dBm.

Different process corners and power supply variations have also been simulated. Corner simulations are performed by using FF, TT, and SS device parameters. Supply voltage variations are 1.4V, 1.2V, 1V and 0.8V. Figs. 8 and 9 are the simulation results. For the corner simulations of FF and SS, the simulated output power and PAE almost the same at FF and SS. For power supply variations, there is no change on power gain. The only change is the saturated output power and its corresponding PAE. From the above simulation results, it can be realized that the proposed CMOS current-mode PA is robust against both corner and power supply variations.

TABLE I is the performance summary of the proposed CMOS current-mode PA. TABLE II is the performance comparison to other silicon-based PAs. It can be seen that the proposed CMOS current-mode PA has the highest PAE and the largest output power among the RF PAs.

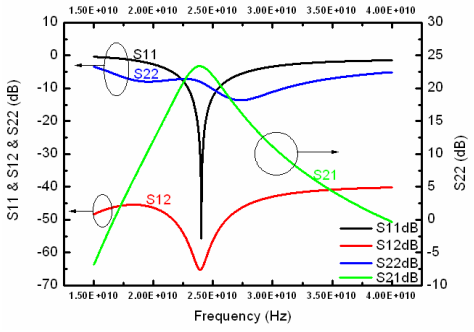

Figure 6. S-parameters

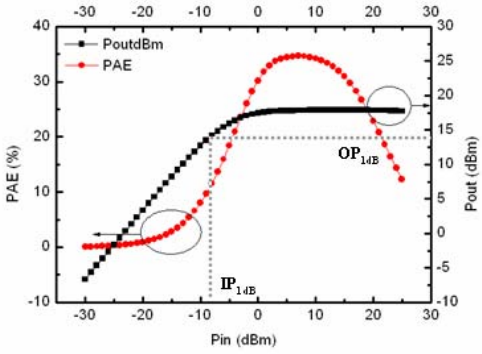

Figure 7. P_{out} v.s. P_{in} and PAE v.s. P_{in}

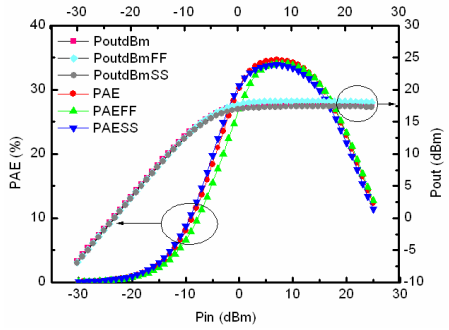

Figure 8. Result of different corner simulation

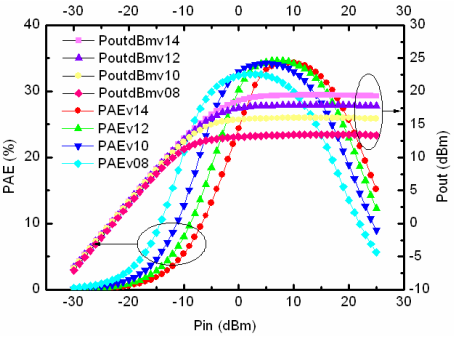

Figure 9. Result of power supply variation simulation

TABLE I. TWO-STAGE CURRENT-MODE PA SUMMARY

Parameter	Value
Technology	0.13-μm CMOS
Supply Voltage (Volt)	1.2
Power Consumption (mWatts)	239
S_{11} (dB)	-47
S_{12} (dB)	-65
S_{21} (dB)	23.37
S_{22} (dB)	-8
Total Current Gain@P1dB (dB)	22.3
Power Gain (dB)	23.35
IP_{1dB} (dBm)	-8.5
OP_{1dB} (dBm)	13.84
PAE@P1dB (%)	10.59
Peak PAE (%)	34.64
P_{in}@Peak PAE (dBm)	7
P_{out}@Peak PAE (dBm)	17.84

TABLE II. PERFORMANCE COMPARISONS OF SILICON-BASED POWER AMPLIFIERS

Ref.	[6]	[10]	[11]	[12]	This Work
Technology	0.18-μm CMOS	0.18-μm CMOS	SiGe HBT	0.13-μm CMOS	0.13-μm CMOS
Frequency (GHz)	24	24	24	17	24
Supply Voltage (Volt)	2.8	2.5	5V	1.5	1.2
S_{11}/S_{12} (dB)	-6.9/-40	-/-	-/-	-/-	-47/-65
Power Gain (dB)	7	-	18	4	23.35
DC Power (mWatts)	280	170	550	75	239
OP_{1dB} (dBm)	11	11	-	4.2	13.84
PAE@P_{1dB} (%)	4.45	-	-	3.45	10.59
Peak PAE (%)	6.5	6.5	3	-	34.64
Sat. P_{out} (dBm)	14.5	14	12	-	17.84
Topology	CSCG 2-Stage	CSCG 2-Stage	CS differential 3-Stage	CS differential 2-Stage	N-type Current Mirror 2-Stage
Note	P1dB Operation	P1dB Operation	Peak PAE Operation	P1dB Operation	Peak PAE Operation

IV. CONCLUSION

This paper presents a 24-GHz CMOS current-mode power amplifier in 0.13-μm technology. The PA uses 1.2-V supply voltage and the total power consumption is 239 mW. Its linear power gain is 23.35 dB, output power is 17.84 dBm, and PAE can be achieved as high as 34.64 % at the same time. Corner and supply voltage variations have also been considered. The simulation results have shown that the proposed current-mode PA is robust under these variations. The proposed CMOS current-mode PA is now under fabrication.

ACKNOWLEDGMENT

This work was supported by the National Science Council (NSC), Taiwan, under the Grant NSC-95-2221-E-009-292. The authors would like to thank the Chip Implementation Center (CIC), National Applied Research Laboratory, for the fabrication of testing chip. The authors would also like to thank the support of HFSS from Ansoft Taiwan.

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