Low-Ripple and Dual-Phase Charge Pump Circuit Regulated by Switched-Capacitor-Based Bandgap Reference

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***Abstract*—This paper proposes a low-ripple and dual-phase charge pump circuit regulated by switched-capacitor-based bandgap reference. Due to design of a buffer stage, a system can have better bandwidth and phase margin, and thus, the transient response and driving capability can be improved. Besides, the dual-phase control can reduce the output voltage ripple by means of only one closed-loop regulation in order to improve the power conversion efficiency. Besides, the proposed automatic body switching (ABS) circuit can efficiently drive the bulk of the power p-type MOSFETs to avoid leakage and potential latch-up. Usually, the regulated charge pump circuit needs a bandgap reference circuit to provide a temperature-independent reference voltage. The switched-capacitor-based bandgap reference circuit is utilized to regulate the output voltage. This chip was fabricated by Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm 3.3 V/5 V 2P4M CMOS technology. The input voltage range varies from 2.9 to 5.5 V, and the output voltage is regulated at 5 V. Experimental results demonstrate that the charge pump can provide 48 mA maximum load current without any oscillation problems.**

***Index Terms*—Bandgap reference, charge pump, dual-phase power stage, fast transient response, output ripple, system-on-chip (SoC).**

I. Introduction

AT THE PRESENT, portable electronic devices such as mobile phones or digital cameras are the emerging market of electronic devices, even called the daily essentials. The demand for the portable electronic devices makes the power supply circuit more and more important. In general, the operating time or standby time of the portable devices all depends on the battery capacity. Efficient power distribution is the main concern in the portable device [1]–[4]. On the other hand, the size and weight of these power devices are also important for the designers. The miniaturization of the power modules and the reduction of the external components are essential in portable devices. Besides, the size of the power supply circuit is the major design consideration, no matter whether the circuit is fabricated as a single chip or integrated into a system-on-chip (SoC) chip. For the portable electronic devices, the reduction of the area on silicon and printed circuit broad (PCB) means lower fabrication cost and tinier size. In other words, a compact power supply system is necessary for the power management of the SoC systems. Therefore, the trend is to focus on the CMOS implementation of power converters and insert the power modules into any portable device. Table I shows the different implementation techniques that can be used to supply different applications. For today's designers, how to find an optimum solution has become an urgent issue.

TABLE I
COMPARISON OF THE DIFFERENT POWER SUPPLY DEVICES

	LDO	Charge Pump	Switching Regulator
Efficiency	Bad $\eta \approx \frac{V_{OUTOUT}}{V_{INPUT}}$	Good $\eta \approx \frac{V_{OUTPUT}}{V_{INPUT} \cdot gain}$	Best Up to 95% and average about 90%
Cost	Best	Moderate Capacitor count, pin count, silicon area drive costs	Most expensive Inductor and other external components drive costs
Difficulty in Design	Easy	Harder	Most difficult
PCB Area	Very small	Small	Large Due to the height and area of inductor
Output Ripple	Very low	Moderate	Moderate
EMI	Very low	Low	Moderate
Load Capability	Moderate Up to 150mA	Moderate Up to 250mA	Best Able to above 500mA
Transformation Type	Step down	Step up Step down Inverter	Step up Step down Inverter

In dc/dc power converters, the charge pump needs less external components than the inductive switching converter. The advantages of the charge pump are that it is small, quiet, and moderately efficient. The small board size and small silicon area are the special competitive advantages of the power converters. The charge pump circuits can boost or buck voltage using only two external capacitors without the need of an external inductor. The size of the inductor is larger and its height is hard to be shrunk. Therefore, the size and height of the external components will limit the layout on the PCB, and hamper the minimization of portable devices. Thus, the power supplying system implemented by charge pump circuits is a good solution compared to the inductor-based switching circuits. The charge pump is a good selection under these concerns [5]–[8]. The charge pump provides an efficient approach to transfer different supply voltage levels. The use of energy in an electronic system more efficiently by means of the charge pump circuits can extend the employing time of a battery-powered electronic system. Furthermore, the silicon area of the charge pump and the size of the external components on PCB turn economic [9]–[13].

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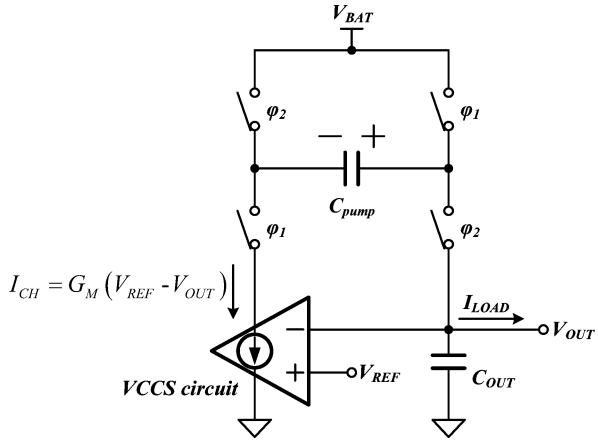


Fig. 1. Basic operation of the compact charge pump circuit.

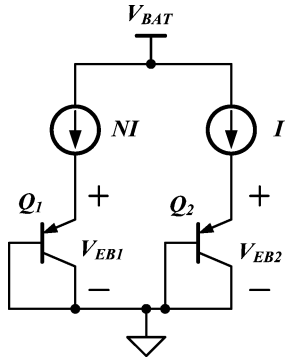


Fig. 2. Emitter-base voltages at the different biasing currents.

Under the consideration for the chip area, the switched-capacitor-based bandgap reference circuit is used instead of the conventional bandgap reference circuit so as to integrate into the charge pump [14]. In general, the charge pump referred to the bandgap reference circuit determines the value of the output voltage. This structure can effectively reduce the quiescent current and chip area. The load capacity always concerns designers of the charge pumps because the size and quantity of the power switches will degrade the advantages in the small silicon area. So, simplifying the control circuit to reserve the space for the large power switches is an important goal in the charge pump circuit design. However, a regulation problem exists in the charge pump design with the built-in bandgap. The output voltage is regulated for only one phase, and thus the output voltage ripple is large. Thus, the proposed method describes a new regulated charge pump circuit with dual-phase regulation, which uses the new proposed output dual-phase power stage. Due to the buffer stage design, the regulated charge pump can provide a maximum of 48 mA load current and regulates output voltage at 5 V for the LED module in the portable devices. The input voltage range is 2.9–5.5 V for the lithium battery.

In this paper, the basic behavior analysis of the proposed charge pump circuit is shown in Section II. Section III describes the circuit implementation. Experimental results are shown in Section IV. Finally, conclusions are provided in Section V.

II. Basic Behavior and Analysis of the Charge Pump

In particular, the low quiescent current and small chip area design are used to achieve high conversion efficiency and low cost in converters, a combinative scheme, as follows, of charge pump not only providing the temperature-independent reference, but also regulating and stabilizing the output voltage.

A. Basic Behavior of Combinative Charge Pump

In order to reduce the chip size and quiescent current, the combinative scheme of bandgap reference circuit and regulation circuit in Fig. 1 is reasonable. It has the charging (φ_1) and discharging (φ_2) phases. During the charging phase, the charging current $I_{\rm CH}$ is switched to charge the pumping capacitor $C_{\rm pump}$ and the output load is supplied by the output capacitor C_L simultaneously. The value of $I_{\rm CH}$ can be defined as (1), where G_m is the transconductance of voltage control current source (VCCS) circuit

$$I_{\rm CH} = G_m \left(V_{\rm REF} - V_{\rm OUT}\right). \tag{1}$$

Besides, during the discharging phase, the capacitor $C_{\rm pump}$ delivers energy to the load and capacitor C_L. Thus, the value of $I_{\rm CH}$ can also be defined as (2). Based on (1) and (2), the expression of the output voltage $V_{\rm OUT}$ can be derived as (3). Furthermore, this circuit is regulated with a fixed switching frequency since it is easy to filter out the noise

$$I_{\rm CH} = 2I_{\rm LOAD} \tag{2}$$

$$V_{\rm OUT} = V_{\rm REF} - 2\frac{I_{\rm OAD}}{G_m}. \tag{3}$$

B. Switched-Capacitor-Based Bandgap Reference

The conventional bandgap reference circuit in Fig. 2 is used to explain the basic operation. The base–emitter voltage $V_{\rm BE}$ of the bipolar junction transistor (BJT) has a negative temperature coefficient and the thermal voltage V_T has a positive temperature coefficient [15]. The expression for the reference voltage without the influence of temperature is expressed as follows:

$$V_{\rm REF} = V_{\rm BE} + V_T \ln N$$
$$\text{and} \quad \frac{\partial V_{\rm REF}}{\partial T} = \frac{\partial V_{\rm BE}}{\partial T} + \frac{V_T}{T} \ln N = 0. \tag{4}$$

The factor N is the multiple of the bias current on the BJT with the same junction area [16]. The term $\ln N$ should be kept at a constant value to minimize the temperature coefficient of the reference voltage. According to the concept of conventional bandgap reference circuit, the switched-capacitor-based bandgap reference circuit is used to integrate into the charge pump. As shown in Fig. 3 [13], this circuit generates two base–emitter voltage levels with negative temperature coefficient in the single p-n junction by biasing different current sources. This structure could save much area and power consumption. The BJT is biased by current I during phase φ_1 and by the multiple current *NI* during phase φ_2. Between these two phases, the

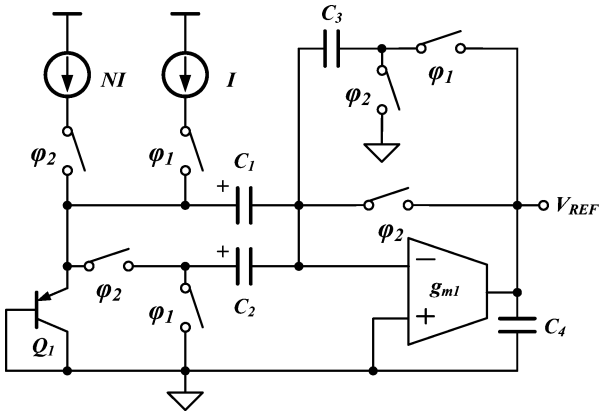


Fig. 3. Schematic of the switched-capacitor bandgap reference in [13].

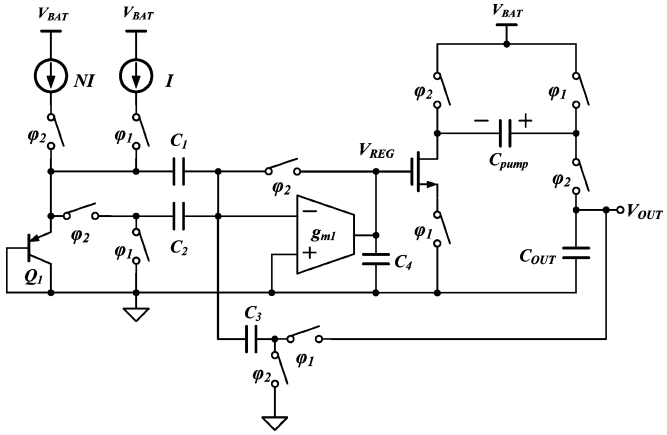


Fig. 4. Schematic of the compact charge pump circuit.

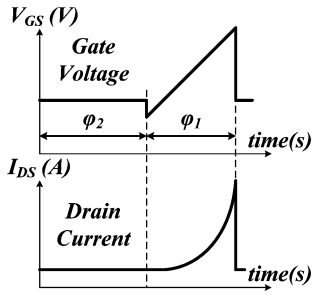


Fig. 5. Gate voltage and drain current of the g_m amplifier.

voltage difference $\Delta V_{\rm BE}$ can be derived as follows:

$$\Delta V_{\rm BE} = V_{\rm BE2} - V_{\rm BE1} = V_T \ln \frac{NI}{I_S} - V_T \ln \frac{I}{I_S} = V_T \ln N. \tag{5}$$

The operation of this reference circuit is by a switched-capacitor network. During phase φ_2, $V_{\rm BE2}$ of BJT is biased by *NI* and stored by C_2. The circuit is switched to "reset" mode. When the switches are changed to phase φ_1, the capacitor C_1 is used to store the value of $V_{\rm EB1}$. The circuit is set to the "amplify" mode. It generates the reference voltage from the summation of the two different voltages with different temperature coefficients. The reference voltage can be obtained by (6) according to the charge balance principle in (7). After several charge distributions, the potential on every capacitor comes off its initial state and the charge at the inverter terminal of the operation transconductance amplifier (OTA) stabilizes

$$V_{\rm REF} = \frac{C_2}{C_3}\left(V_{\rm BE2} + \frac{C_1}{C_2} V_T \ln N\right) \tag{6}$$

$$\Delta Q_1 + \Delta Q_2 = \Delta Q_3 \tag{7}$$

where $\Delta Q_1 = C_1 \Delta V_{\rm EB1} = C_1 V_T \ln N$, $\Delta Q_2 = C_2 \Delta V_{\rm EB2}$, and $\Delta Q_3 = C_3 \Delta V_{\rm REF}$.

Therefore, the parameter $\ln N(C_1/C_2)$ is fine-tuned to determine the zero temperature coefficient of the reference voltage. The parameter C_2/C_3 is used to determine the scale of the reference voltage. Besides, a drawback in Fig. 3 is that the produced reference voltage appears only during the "amplify" mode since the charge pump needs the reference voltage to determine the output voltage during phase φ_1.

As shown in Fig. 4, the bandgap reference circuit is integrated into the charge current controller. The terminal of the capacitor C_3 is connected to the output terminal of this charge pump. The charge at the inverter node of the OTA should be balanced during phase φ_1. The output voltage of the OTA directly controls the gate voltage $V_{\rm GS}$ of the MOSFET and determines the charging current $I_{\rm CH}$, which is called the voltage-mode control methodology. During the charging phase φ_1, the current $I_{\rm DS}$ may exceed the average load current since the drain current $I_{\rm DS}$ of the MOSFET is the square function of gate voltage in Fig. 5. Thus, the nonlinear drain current of MOSFET finds it difficult to stabilize the controlling loop and hence to increase the reliability in the voltage-mode control methodology. Therefore, the goal of this paper is not only to drive the white LED by a constant current of 20 mA with a compact solution, but also improve the reliability of the whole charge pump circuit. The proposed circuit increases the load current driving capability and still uses the compact switched-capacitor-based bandgap reference. The specification is defined for an LED driver with high load current driving capability and low output ripple.

C. Loop Gain of the Voltage-Mode Control Methodology

The charge pump with a fixed switching frequency determines the output voltage by controlling the ON-resistance of the switching transistors, as shown in Fig. 6. Varying the ON-resistance of the transistor, the voltage mode could determine the drop voltage between the two terminals of the switching transistor. Besides, it also determines the voltage across the pumping capacitor. According to the operation of the voltage mode, the value of the output resistance may become smaller than that of the load resistance at the heavy loads. Thus, it may lead to a serious problem at the heavy load. The pole at the output node is defined as (8). Since a large value of $C_{\rm OUT}$ is selected as the output capacitor, the output pole is the dominant pole at light loads

$$\omega_p = \frac{1}{(r_O // R_{\rm LOAD})\, C_{\rm OUT}} \approx \frac{1}{R_{\rm LOAD} C_{\rm OUT}} \text{ at heavy loads} \tag{8}$$

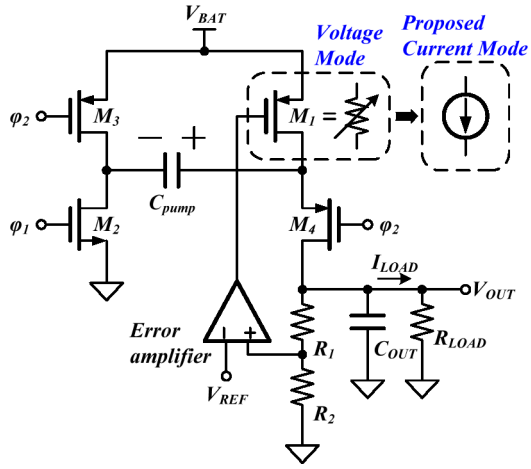


Fig. 6. Current-mode control replaces the ON-resistance with the current source.

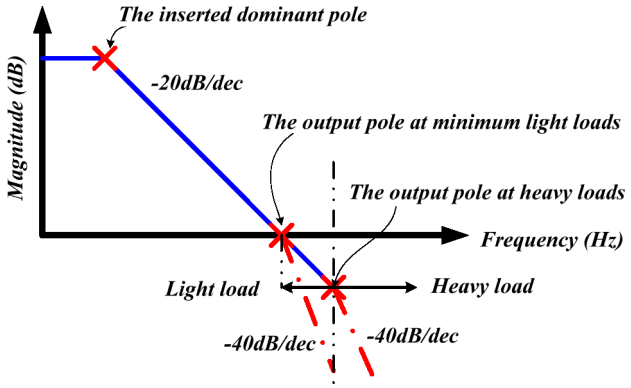


Fig. 7. Frequency response of the loop gain by means of the dominant pole compensation.

where R_{LOAD} is the load resistance and r_O is the output resistance of the switching transistor. However, at heavy loads, the output pole is smaller than the pole at the drain of transistor M_4 and becomes the first nondominant pole, i.e., there are two low-frequency poles leading to serious stability issue at heavy loads. The simplest compensation method is the dominant pole compensation that is used to stabilize the system. Thus, an additional fixed dominant pole is inserted at low frequency, and the frequency response is shown in Fig. 7. However, it deteriorates the bandwidth and results in slow transient response. Besides, it has the minimum load requirement. At light loads, the output pole is moved toward the origin and results in a phase margin smaller than 60°. Thus, it has a minimum load requirement after using the dominant pole compensation.

D. Proposed Current-Mode Control Methodology

The proposed current-mode control replaces the ON-resistance control device by the current source in Fig. 6, i.e., the transistor M_1 operates in saturation and works as a current source. At this time, the dominant pole is located at the output node since the output resistance of transistor M_1 is larger than the equivalent resistance of the switched capacitor, which is as follows:

$$r_O = \frac{1}{f_{\mathrm{CLK}} C_{\mathrm{pump}}}. \tag{9}$$

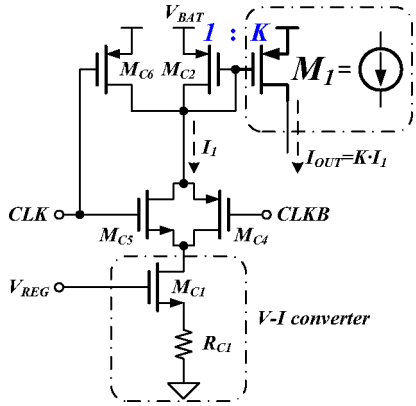


Fig. 8. Current mirror buffer is used as the output stage of the regulation circuit.

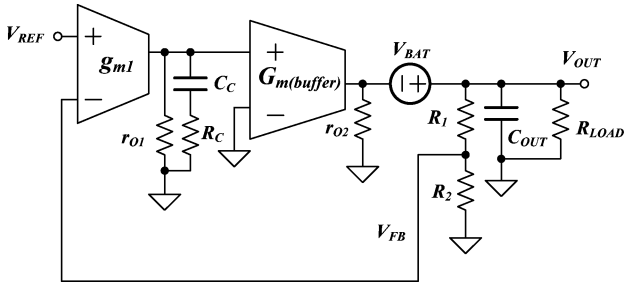


Fig. 9. Small signal model of the charge pump.

Thus, the impedance of the pumping capacitor must be set much smaller than the output impedance of the transistor M_1. In order to make sure that transistor M_1 operates in saturation region, the maximum voltage across the pumping capacitor must be defined as (10). The value of the charge pump capacitor can be decided by (11)

$$\Delta V_{C_{\mathrm{pump}},\mathrm{MAX}} = (V_{\mathrm{OUT}} - V_{\mathrm{SD},M_4}) - (V_{\mathrm{IN}} - V_{\mathrm{SD},M_3}) \tag{10}$$

$$C_{\mathrm{pump}} = \frac{I_{\mathrm{LOAD,MAX}}}{f_{\mathrm{CLK}} \Delta V_{C_{\mathrm{pump}},\mathrm{MAX}}}. \tag{11}$$

Consequently, the output stage of the regulation circuit can be implemented in Fig. 8. This output stage provides a constant current to ensure that transistor M_1 operates in the saturation region. The current I_1 is transferred by the voltage-to-current (V–I) converter that is composed of a transistor M_{C_1} and a resistor R_{C_1}. The degenerated resistor R_{C_1} makes the transconductance $G_{m\,(\mathrm{buffer})}$ $(= I_{\mathrm{OUT}}/V_{\mathrm{REG}})$ more linear. The transconductance of the current mirror buffer is determined by

$$G_{m(\mathrm{buffer})} = \frac{I_{\mathrm{OUT}}}{V_{\mathrm{REG}}} = \frac{g_{m(M_{C1})}}{1 + g_{m(M_{C1})} R_{C1}} K \approx \frac{K}{R_{C1}},$$

$$\text{where} \quad K = \frac{W_{M1}/L_{M1}}{W_{M_{C2}}/L_{M_{C2}}}. \tag{12}$$

The value of K should not be set too large because the capacitance at the gate of transistor M_1 may generate an additional low-frequency pole. The small-signal model is shown in Fig. 9. The locations of the pole and zero can be derived as (13)

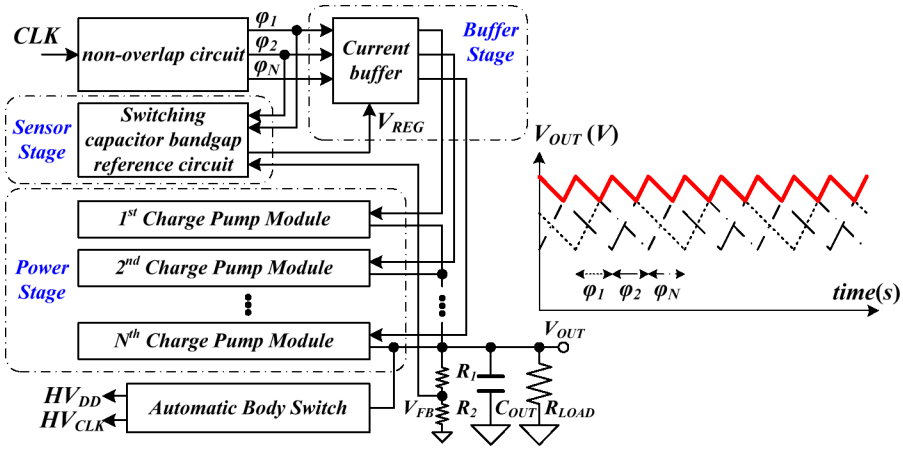


Fig. 10. Scheme of the proposed method with multiphase output.

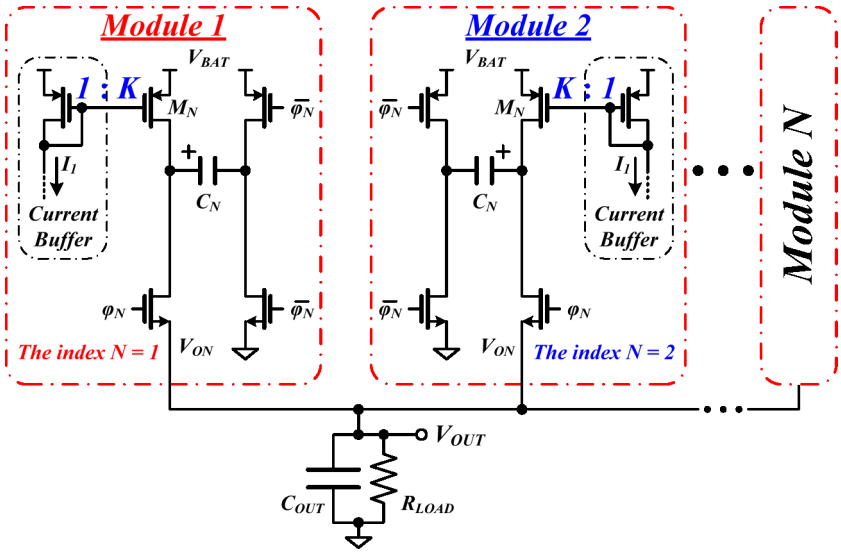


Fig. 11. Proposed dual-phase charge-pump circuit that is used to extend to multiphase charge pump.

and (14). The dominant pole is located at the output node as expressed in (13). The output of the first stage has a pole-zero pair ($f_{\rm ndp}$ and f_z), as shown in (14). The dc gain of the loop is described in (15)

$$f_{\rm dp} = \frac{1}{2\pi C_{\rm OUT}\left(r_{O2}//R_{\rm LOAD}\right)} \tag{13}$$

$$f_{\rm ndp} = \frac{1}{2\pi C_C\left(r_{O1}+R_C\right)} \quad \text{and} \quad f_z = \frac{1}{2\pi C_C R_C} \tag{14}$$

$$A_{\rm ALL} = A_1 A_2 = g_{m1} r_{O1} G_{m(\rm buffer)}\left(r_{O2}//R_{\rm LOAD}\right). \tag{15}$$

The strategy of stability is that the dominant pole is the output pole and the nondominant pole is located at the output of the OTA. The additional zero here is generated to compensate the effect of the first nondominant pole. The output impedance r_{O1} is too large to locate the additional zero close to that of the nondominant pole. However, the compensation zero is still set at least three to five times higher than the first nondominant pole. Since the nondominant pole and the additional zero are fixed, the dominant pole can be moved to higher frequency in case of load variations, i.e., the driving capability can be improved compared to that of the voltage-mode control methodology.

E. Proposed Multiphase Power Stage

As depicted in Fig. 10, the multiphase output is an effective way to reduce the output voltage ripple. The different voltage waveforms are summed on the output capacitor. If the waveforms have different phases to each other, the output ripples can be reduced. The dual-phase circuit is proposed to be finally extended to the multiphase output. The dual-phase circuit can provide twice the driving current to the load, and the output voltage ripple can be expressed as (16) when the equivalent series resistance (ESR) is considered

$$V_{\rm ripple} = \frac{I_{\rm LOAD}}{2 f_{\rm CLK} C_{\rm OUT}} + 2 I_{\rm LOAD} {\rm ESR}_{C_{\rm OUT}}. \tag{16}$$

Since the conventional voltage-mode control charge pump exports only the output current over half period, the charging or discharging current on the output capacitor is very drastic. Thus, the transient dip voltage is very large in case of load

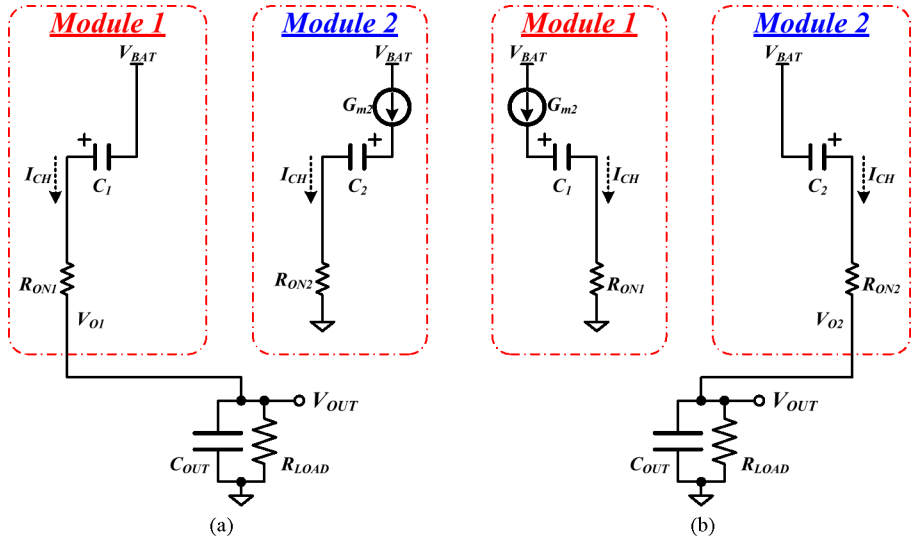


Fig. 12. Equivalent circuits of the power stage at the steady state (a) during phase φ_1 and (b) during phase φ_2.

variations. However, if the dual-phase method is utilized, the output current from the charge pump to the output load is continuous, and thus, the output ripple can be reduced effectively. The proposed dual-phase design is illustrated in Fig. 11. During phase φ_1, the closed-loop regulation is built up. Module 1 delivers charge to load and module 2 stores the same energy on the pumping capacitor C_2 at the same time. During phase φ_2, module 2 delivers the stored charge to load and module 1 stores energy via the supply voltage. During both phases, the output load can be driven by one of two charge pump modules, and that the output ripples can be reduced effectively is an advantage of the proposed dual-phase charge pump. Fig. 12(a) and (b) shows the equivalent circuits of steady state during phases φ_1 and φ_2, respectively. During phase φ_1, transistor M_2 of module 2 works as the VCCS circuit, as shown in Fig. 12(a). The VCCS circuit provides the same current $I_{\rm CH}$ with the transconductance equal to G_{m_2}. Meanwhile, the load current $I_{\rm LOAD}$ is drawn from module 1. During phase φ_2, the load current is driven by module 2. The following equations (17) and (18) stand for the equivalent charging current $I_{\rm CH}$ during the two phases, respectively

$$I_{\rm CH} = G_{m2}\left(V_{\rm REF} - V_{\rm OUT}\right) \text{ during } \varphi_1 \tag{17}$$

$$I_{\rm CH} = I_{\rm LOAD} \text{ during } \varphi_2. \tag{18}$$

According to (17), (18), and (19) can demonstrate the output voltage that can be regulated to the reference voltage

$$V_{\rm OUT} = V_{\rm REF} - \frac{I_{\rm LOAD}}{G_{m2}} \approx V_{\rm REF}. \tag{19}$$

III. Implementation of the Proposed Dual-Phase Charge Pump

In Fig. 10, the completely compact charge pump circuit with multiphase current-mode control is illustrated. It mainly consists of the sensor stage, the buffer stage, the power stage, the

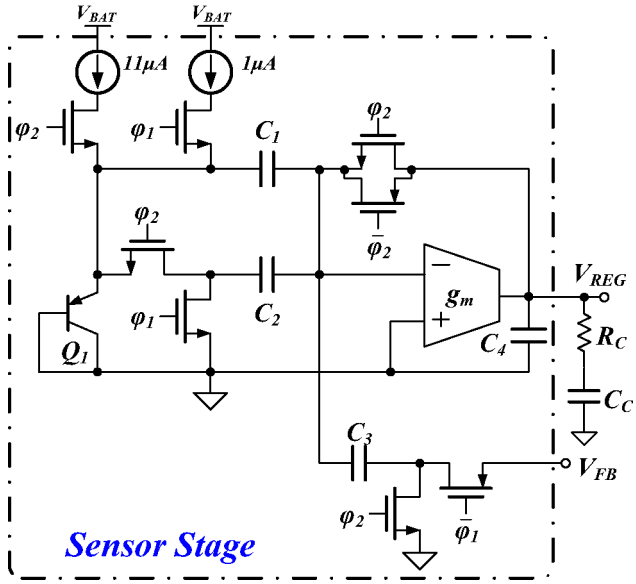


Fig. 13. Sensor stage.

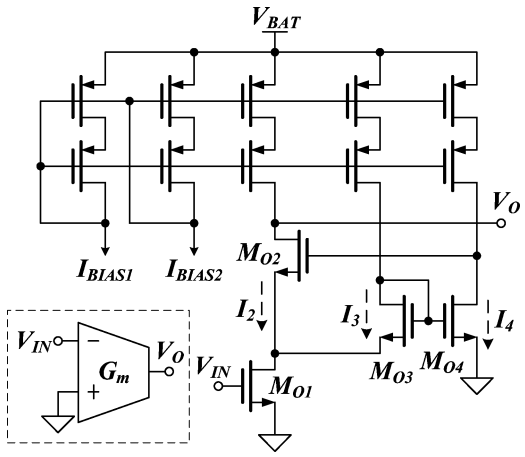


Fig. 14. Cascode amplifier with the gain boosting technique.

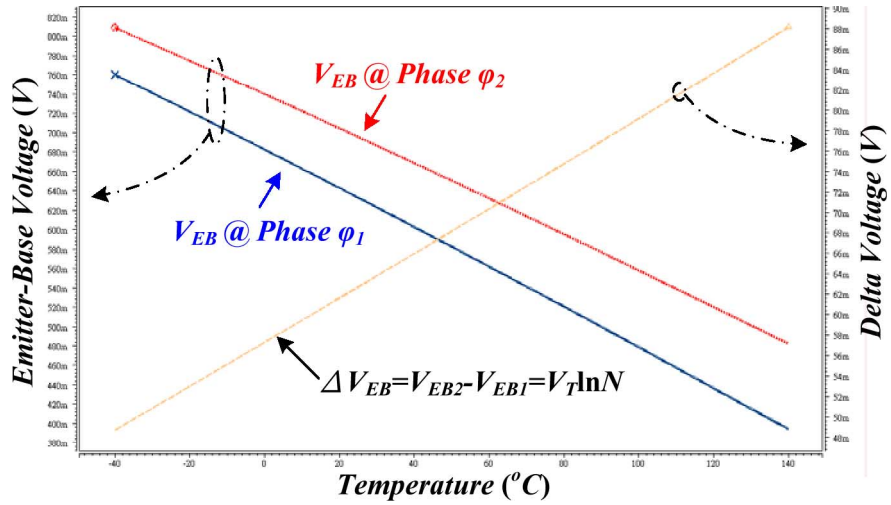


Fig. 15. $V_{\rm EB}$ and $\Delta V_{\rm BE}$ versus temperature.

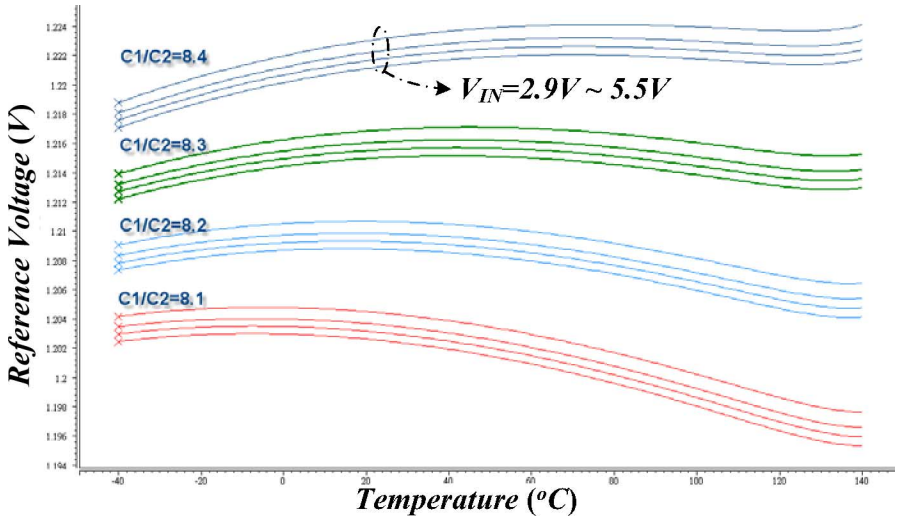


Fig. 16. Ratio of C_1/C_2 versus temperature.

automatic body switching (ABS) circuit, and the nonoverlap circuit. The function of each stage is describes as follows.

A. Sensor Stage

The proposed sensor circuit shown in Fig. 13 is composed of the current source, capacitors, switches, a BJT, and an error amplifier. The sensor stage is used to sense the feedback signal $V_{\rm FB}$ and the bandgap reference to produce a control signal $V_{\rm REG}$ to the next stage. In order to reduce the effect of charge injection, the switches are designed by using minimum size. Moreover, the sensor circuit is designed to operate at a very small current. Thus, the voltage drop on the minimum size switches can be ignored. A high-gain error amplifier is needed to make sure that the difference voltage generates the output voltage $V_{\rm REG}$ without being affected by the offset voltage of the error amplifier. The error amplifier of the sensor stage is shown in Fig. 14. Because of the autozeroing technique, the offset voltage of the error amplifier can be canceled in the switched-capacitor circuit [17]. Therefore, this error amplifier is designed by just a simple common-source cascode amplifier with gain-boosting technique for getting a high dc gain. Transistors M_{O3} and M_{O4} constitute a feedback loop to boost the output impedance and high gain. The feedback loop controls the value of the drain–source voltage of M_{O1}. The drain–source voltage of M_{O1} is equal to the difference between the gate–source voltages of M_{O3} and M_{O4} by the following equation:

$$V_{\rm DS(M_{O1})} \approx \sqrt{\frac{2}{\mu_n C_{\rm OX}}}\left(\sqrt{\frac{I_4}{(W/L)_{M_{O4}}}}-\sqrt{\frac{I_3}{(W/L)_{M_{O3}}}}\right). \tag{20}$$

Fig. 15 shows the temperature coefficient of $V_{\rm EB}$ during two different phases. The variation of temperature is from -40 °C to 140 °C. At the temperature equal to 75 °C, the temperature coefficient of $V_{\rm EB}$ is about -1.85 mV/°C and that of $V_{\rm EB}$ is about 0.22 mV/°C. According to (7), it is obvious that the term

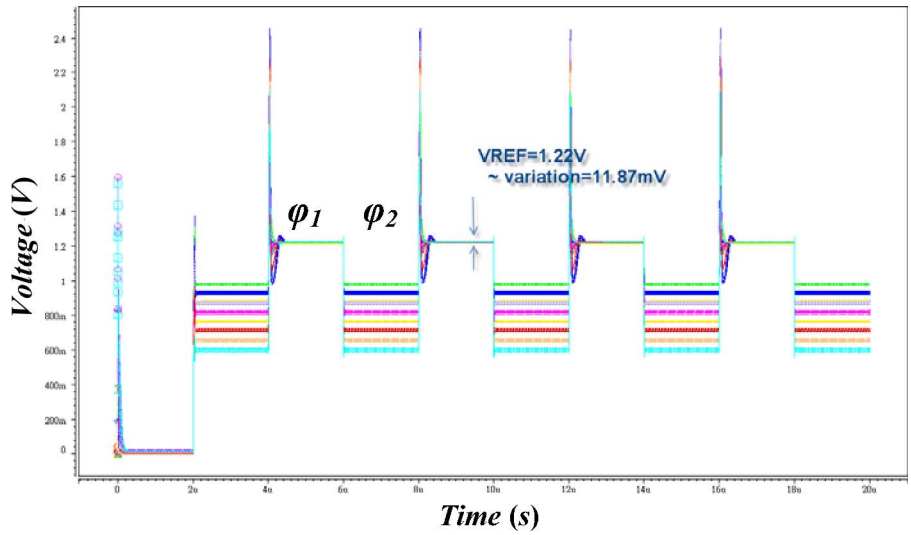


Fig. 17. Waveforms of the switched-capacitor bandgap reference circuit. (Temp $= -25$ °C–125 °C and $V_{\rm IN} = 2.5$–5.5 V under all process corners).

C_1/C_2 is used to cancel the negative temperature coefficient of the voltage $V_{\rm EB}$. Fig. 16 shows four sets of capacitor ratio (C_1/C_2) under different supply voltages. The ratio that makes the reference voltage be almost constant at high temperature is the better choice since the operating temperature of the chip is often hotter than the room temperature when the chip is delivering the load current. Thus, the ratio $C_1/C_2 = 8.4$ is selected. Certainly, the trimming circuit is also used to compensate the process variations.

Fig. 17 shows the reference voltage of the switched-capacitor-based bandgap reference circuit. It is obvious that the reference voltage is only produced during phase φ_1. The absolute variation of the reference voltage is 11.87 mV, which is equal to 64.86 ppm/°C. The absolute value of the result is not good due to variations in the process. However, the absolute value of the reference voltage can be fine-tuned by trimming the value of the capacitor C_3 in (7). It can improve the accuracy due to process variations without affecting the characteristic of the zero temperature coefficients.

B. Buffer Stage

The buffer stage is proposed in Fig. 18 [18]. Transistors $M_2 - M_8$ function as the current mirrors for driving the power MOSFETs at the power stage. The input consists of the transistor M_1 and the resistor $R_{\rm Gm}$ as a V–I converter. Transistors $M_{W_1} - M_{W_3}$ are the switches that make the current buffer stage turned off during phase φ_2, since the output stage is driven by the dual-phase power stage. The potential $\rm HV_{DD}$ is the highest potential in the whole charge pump circuit. This potential also supplies to the bulk terminal of the power MOSFETs. Transistor MP is the power MOSFET of the power stage. In this design, the variation of $V_{\rm REG}$ is 1.5 V at the minimum supply voltage 2.9 V, and the most heavy output current is 100 mA. Then, the transconductance of the current buffer stage has to be larger than that defined as

$$G_{m\,(\rm buffer)} \geq \frac{100\ \rm mA}{1.5\ \rm V} = 66.67\ \rm mS. \tag{21}$$

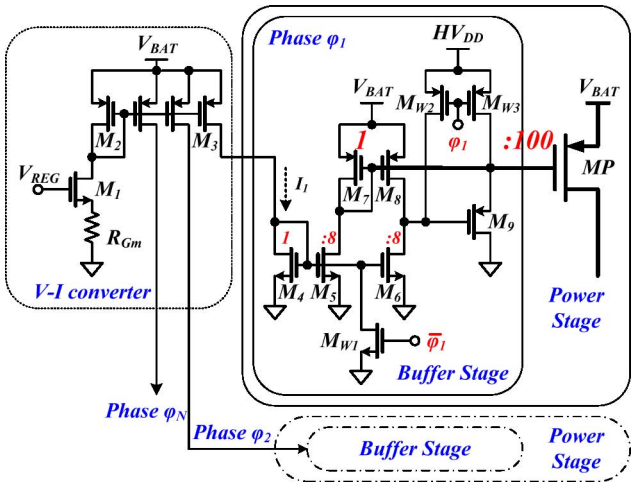


Fig. 18. Current buffer stage.

There is a current mirror with a ratio of 100, which is composed of M_7 and MP for driving the power MOSFET transistor. The output current on MP is 800 times than that flowing through transistor M_1. The overall transconductance from (22) is dominated by the resistor $R_{\rm Gm}$

$$G_{m\,(\rm buffer)} = 800s\frac{g_{m,M1}}{1 + g_{m,M1}R_{\rm Gm}} \approx \frac{800}{R_{\rm Gm}}. \tag{22}$$

The gate capacitance of the power MOSFETs in the next stage is huge. In order to speed up the transient response of the power MOSFETs, the transistor M_9 is used to precharge the gate capacitance of the power transistors. When the output current is exported during phase φ_1, M_9 is turned on to precharge the gate of the power MOSFET until M_7 can fully control MP.

C. Dual-Phase Power Stage

The dual-phase power stage is depicted in Fig. 19. The circuit consists of two charge pump modules. Transistor M_7 is in the

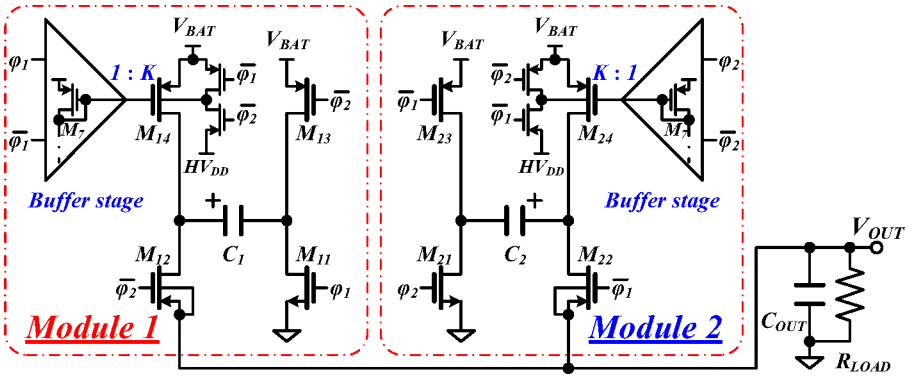


Fig. 19. Proposed dual-phase power stage.

buffer stage, and it mirrors K times current to the power MOSFETs M_{14} and M_{24}. During phase φ_1, module 1 charges the energy on capacitor C_1 by M_{14}. Meanwhile, transistor M_{24} in module 2 delivers the charge on the capacitor C_2 to the output load. During phase φ_2, module 1 delivers energy to the output load and module 2 stores the energy on the capacitor C_2 from the voltage supply. In order to set the frequency of the output pole in a controllable range, the transistors M_{14} and M_{24} in Fig. 19 are operated in the saturation region. The output resistance of the transistor in the saturation region is almost constant and relatively large. Therefore, the location of the output pole will be dominated by the load resistance. The stability of the system is easy to guarantee. The bulk terminals of the power MOSFETs are connected to the highest potential ($\mathrm{HV_{DD}}$) in the chip to eliminate reverse current. But the large source-bulk voltage will increase the threshold voltage of the power MOSFETs M_{14} and M_{24} because of the body effect. Fig. 19 shows the additional bulk bias circuit at the power stage. The bulk terminals of transistors M_{14} and M_{24} are biased to their source terminal when M_{14} and M_{24} are turned on. Therefore, the smaller size of the power MOSFETs has the same ON-resistance due to the smaller V_{TH} in (23). When M_{14} and M_{24} are turned off, their bulk terminals are biased to $\mathrm{HV_{DD}}$ to eliminate the reverse current

$$R_{\mathrm{ON}} = \frac{1}{\mu C_{\mathrm{OX}} (W/L) (V_{\mathrm{GS}} - V_{\mathrm{TH}})}. \tag{23}$$

D. ABS Circuit

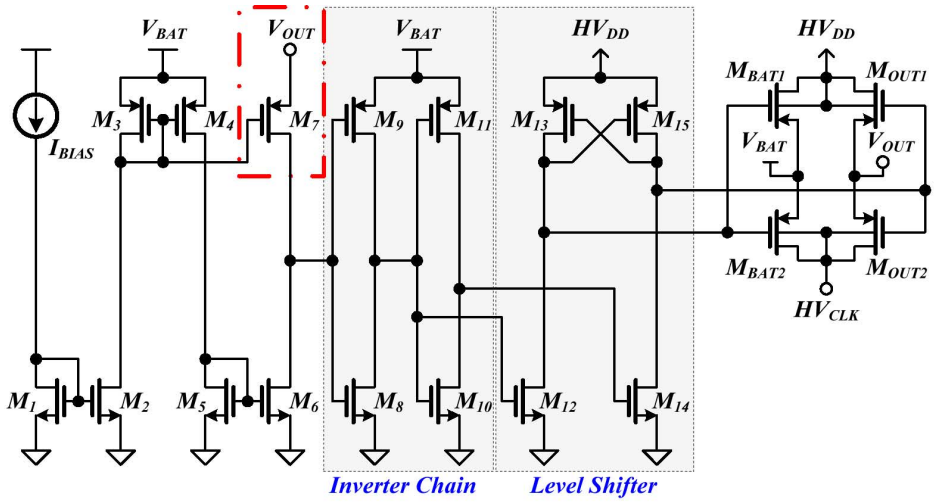
The low-voltage ABS circuit is necessary to drive the bulk of the power p-type MOSFETs to avoid leakage and potential latch-up. In order to bias the body of p-MOSFET with the maximum voltage to fully turn off p-MOSFET, Fig. 20(a) shows the schematic of an ABS circuit. The gate of the transistor M_7 is clamped to V_{BAT}. If the value of V_{BAT} is larger than that of V_{OUT}, then the drain of the transistor M_7 will be pulled low. After the operation of the inverter chain and level shifter, $\mathrm{HV_{DD}}$ can be rapidly switched to V_{OUT}. As shown in Fig. 20(b), experimental results demonstrate that power dissipation is better than that of the previous design [19] by about 54% after the test of triangular and square waveforms. There are two output nodes, $\mathrm{HV_{DD}}$ and $\mathrm{HV_{CLK}}$, in this circuit. $\mathrm{HV_{DD}}$ supplies the power MOSFETs and $\mathrm{HV_{CLK}}$ supplies the driver circuit.

E. Nonoverlap Circuit

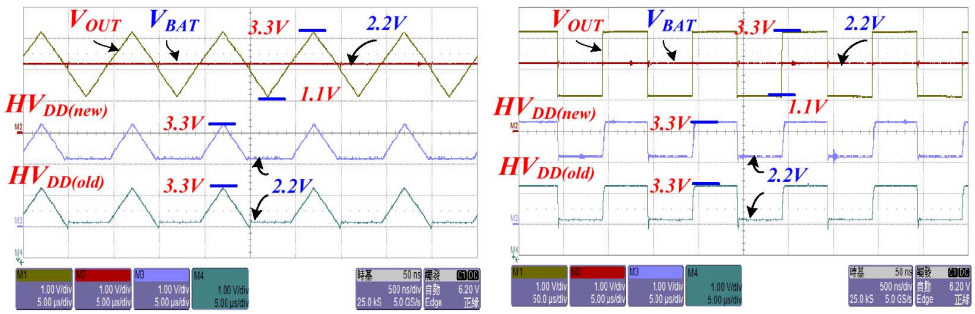
Fig. 21 shows the nonoverlap circuit for the driver of power MOSFETs, also called the dead-time controller. It is used to avoid the shoot-through current in the power MOSFETs. The NAND gates ensure that there is no overlapping between the phases φ_1 and φ_2. The transmission gate $\mathrm{TG_0}$ is used to ensure the same delay time as that of the inverter $\mathrm{INV_0}$. Hence, the size of $\mathrm{TG_0}$ should be equal to the size of $\mathrm{INV_0}$. The minimum delay time can be achieved by using the optimum fan-out value "e" (=2.71) for each stage in the driving chain. However, the minimum delay time is not essential to this charge pump circuit [20], [21]. The rising/falling and the nonoverlapping time are required to be determined in this circuit. In general, long delay time may cause the accuracy problem of the switched-capacitor circuit at the sensor stage. The larger fan-out will cause the longer delay time in the driving chain [22]–[24]. Fig. 22 shows the delay time between the phases φ_1 and φ_2 at all corners when the minimum battery and output voltages are 2.9 and 5 V, respectively. The different corners may produce the different rising/falling times and cause different delay times. The maximum delay time does not exceed 3.61 ns. The maximum rising time is 0.9 ns at the SS corner.

IV. Experimental Results

The proposed dual-phase charge pump circuit was fabricated in TSMC double-poly quadruple-metal 0.35-μm CMOS technology. The threshold voltages of nMOSFET and pMOSFET are 0.55 and 0.65 V, respectively. The chip micrograph is shown in Fig. 23 and the total silicon area is about 1615 μm $\times$ 1520 μm, including the testing pads. The dual-phase charge pump circuit can operate from 2.9 to 5.5 V with a regulated output voltage of 5 V. The summary of the performance is shown in Table II. Fig. 24 shows the regulated output voltage. The waveforms of the two terminals of the charge pump capacitor demonstrate the correctness of the proposed circuit. Due to the large parasitic resistance, the regulated output voltage is about 5.1 V. Fig. 25 shows the load transient response when load current changes



(a)



V_{OUT} is triangular wave and V_{IN} is a constant voltage

V_{OUT} is square wave and V_{IN} is a constant voltage

Input waveform	Ma et al. 2007 [19]	This work	Reduction Percentage
Triangular wave	54.36uW	25uW	54%
Square wave	56.33uW	24uW	54.39%

(b)

Fig. 20. Comparator is used to select the maximum potential for driving the bulk of the power p-type MOSFETs. (a) Schematic of the ABS circuit. (b)Experimental results demonstrate the low-power and high-accuracy characteristics of the ABS circuit.

from 4 to 48 mA or vice versa. The output ripple is smaller than $7\text{mV}_{\text{P-P}}$, which is effectively reduced by the proposed dual-phase charge pump circuit. The measured output ripple of the charge pump with voltage-mode control methodology is about $60\text{mV}_{\text{P-P}}$. Thus, the output ripple of the dual-phase charge pump is much smaller than that of the voltage-mode charge pump. The response time is about 20 μs, which is smoothly rising and falling in relation to regulated output voltage. It means that the phase margin is enough during the transient load condition since the current-mode control methodology is applied to the proposed dual-phase charge pump. Furthermore, the overshoot and undershoot voltages in the proposed charge pump disappear during load transient, when it compares with the load transient in the voltage-mode charge pump. The drop voltage is about 60 mV due to the large parasitic resistance of the bonding and PCB wires. Fig. 26 demonstrates the driving capability of the proposed circuit to be about 48 mA. When the load current is higher than 48 mA, the output voltage drastically decreases due to the unregulated results. When the load current is smaller than 48 mA, the efficiency decreases and is proportional to the increase in the input voltage, which is described by the charge pump theory. The efficiency is shown in Fig. 27.

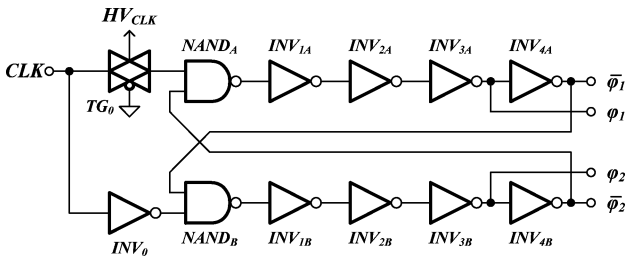


Fig. 21. Driver with nonoverlapping clocks for turning on/off the power MOSFETs.

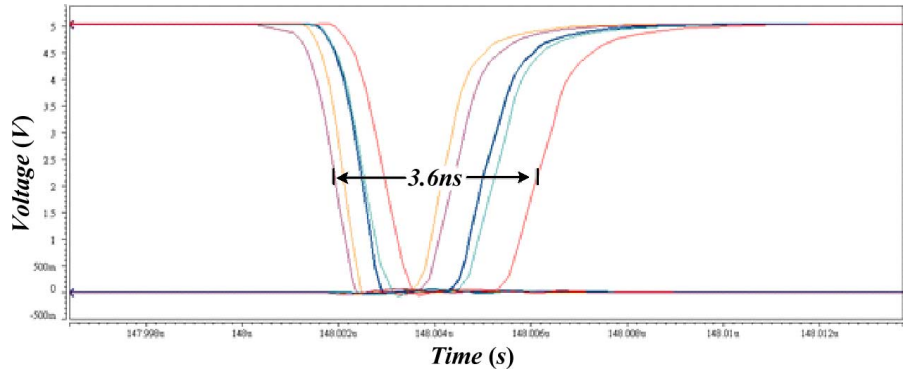


Fig. 22. Nonoverlapping time between phase φ_1 and φ_2 at all process corners.

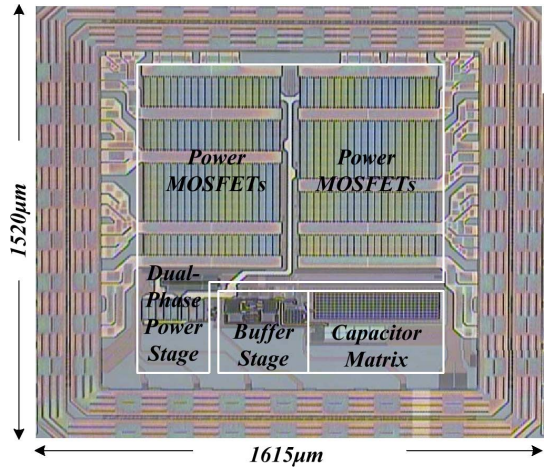


Fig. 23. Chip micrograph.

TABLE II
SUMMARY OF THE PERFORMANCE

Specification	Performance
Technology	TSMC 0.35μm 3.3V/5V CMOS technology
Pumping Capacitor	1μF
Output Capacitor	10μF
Switching Frequency	250 KHz
Input Voltage	2.9 V~5.5 V
Output Voltage	5 V
Maximum Output Current	48 mA
Output Ripple	1.473mV @ V_{IN}=2.9V, I_{LOAD}=48mA 6.254mV @ V_{IN}=2.9V, I_{LOAD}=4mA
Load regulation	16.7 mV/mA
Line regulation	9.258 mV/V
Temperature Drift	16.64 ppm/°C

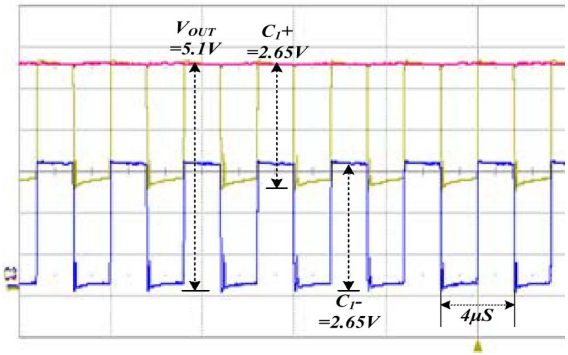


Fig. 24. Measured waveforms of V_{OUT} and the two terminals of the charge-pump capacitor. ($V_{\mathrm{BAT}} = 3$ V, $I_{\mathrm{OUT}} = 20$ mA).

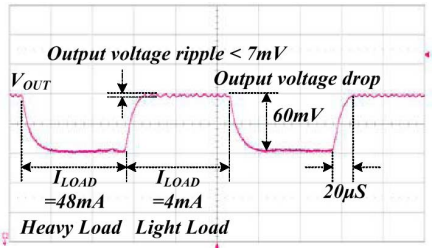


Fig. 25. Load transient waveform when $V_{\mathrm{BAT}} = 3.0$ V and I_{OUT} change from 4 to 48 mA, or vice versa.

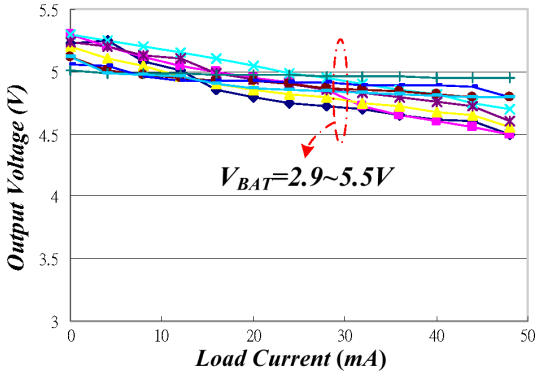


Fig. 26. Output voltage versus load current at different supply voltages ($V_{\mathrm{BAT}} = 2.9$–5.5 V).

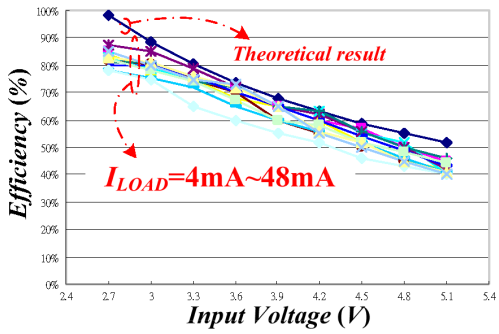


Fig. 27. Efficiency versus input voltage at different load currents ($I_{\mathrm{LOAD}} =$ 4–48 mA).

V. CONCLUSION

A dual-phase charge pump circuit by using switched-capacitor-based bandgap reference and current-mode control

methodology has been presented in this paper. The size of the regulated block in this structure is very small and most area on silicon is the power device. It helps in designing with minimum size and with low cost. The low output ripple and high system stability of the dual-phase charge pump circuit are demonstrated by the test chip, which was fabricated in TSMC 0.35 μm 3.3 V/5 V 2P4M CMOS technology. Due to the design of the buffer stage, the system can have better bandwidth and phase margin. Therefore, the transient response and driving capability can be improved. Besides, only one closed-loop regulation is utilized to generate the dual-phase charge pump circuit so as to improve the power conversion efficiency. Besides, the proposed ABS circuit can efficiently drive the bulk of the power p-type MOSFETs to avoid leakage and potential latch-up. The input voltage range varies from 2.9 to 5.5 V, and the output voltage is regulated at 5 V. Experimental results demonstrate that this charge pump can provide 48 mA maximum load current without any oscillation problem.

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REFERENCES

[1] T. Simunic, "Dynamic management of power consumption," in *Power Aware Computing*. Norwell, MA: Kluwer, 2002, pp. 101–125.
[2] F. Bedeschi *et al.*, "A low-ripple voltage tripler," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2006, pp. 2753–2756.
[3] H. Lee and P. K. T. Mok, "Switching noise and shoot-through current reduction techniques for switched-capacitor voltage doubler," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1136–1146, May 2005.
[4] T. R. Ying, W.-H. Ki, and M. Chan, "Area-efficient CMOS charge pumps for LCD drivers," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1721–1725, Oct. 2003.
[5] K.-S. Min, Y.-H. Kim, J.-H. Ahn, J.-Y. Chung, and T. Sakurai, "CMOS charge pumps using cross-coupled charge transfer switches with improved voltage pumping gain and low gate-oxide stress for low-voltage memory circuits," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2002, vol. 5, pp. V-545–V-548.
[6] J. A. Starzyk, Y.-W. Jan, and F. Qiu, "A DC–DC charge pump design based on voltage doublers," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 48, no. 3, pp. 350–359, Mar. 2001.
[7] C.-C. Wang and J.-C. Wu, "Efficiency improvement in charge pump circuits," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 852–860, Jun. 1997.
[8] J.-Y. Lee, S.-E. Kim, S.-J. Song, J.-K. Kim, S. Kim, and H.-J. Yoo, "A regulated charge pump with small ripple voltage and fast start-up," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 425–432, Feb. 2006.
[9] *LTC1733: Monolithic Linear Lithium-Ion Battery Charger with Thermal Regulation*. (2001). Linear Technology, Milpitas, CA. [Online]. Available: http://www.linear.com/
[10] E. Bayer, H. Schmeller, and G. Sporer, "Charge pumps become differentiated," in *Proc. Wireless Symp. Portable Des.*, 2000, pp. 1–8.
[11] *TPS6012X: Regulated 200-mA High Efficiency Charge Pump DC/DC Converter*. (2000). Texas Instruments, Inc., Dallas, TX. [Online]. Available: http://www.ti.com/
[12] E. Bayer and H. Schmeller, "Charge pump with active cycle regulation-closing the gap between linear and skip modes," in *Proc. IEEE 31st Annu. Power Electron. Spec. Conf.*, 2000, vol. 3, pp. 1497–1502.
[13] G. Thiele and E. Bayer, "Current mode charge pump: Topology, modeling and control," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, 2004, vol. 5, pp. 3812–3817.
[14] B. R. Gregoire, "A compact switched-capacitor regulated charge pump power supply," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1944–1953, Aug. 2006.
[15] R. J. Widlar, "New developments in IC voltage regulators," *IEEE J. Solid-State Circuits*, vol. SC-6, no. 1, pp. 2–7, Feb. 1971.
[16] K. E. Kuijk, "A precision reference voltage source," *IEEE J. Solid-State Circuits*, vol. SC-8, no. 3, pp. 222–226, Jun. 1973.
[17] B. R. Gregoire, "Switched capacitor voltage reference circuits using transconductance circuit to generate reference voltage," U.S. Patent 681 916 3, Nov. 16, 2004.
[18] C.-Y. Hsieh, P.-C. Fan, and K.-H. Chen, "A dual phase charge pump with compact size," in *Proc. 14th IEEE Int. Conf. Electron., Circuits Syst.*, Dec. 2007, pp. 202–205.
[19] D. Ma and W.-H. Ki, "Fast-transient PCCM switching converter with freewheel switching control," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 9, pp. 825–829, Sep. 2007.
[20] A. Rao, "An efficient switched capacitor buck-boost voltage regulator using delta-sigma control loop," M.S. thesis, Oregon State Univ., Corvallis, Jun. 2002.
[21] K.-H. Chen, C.-J. Chang, and T.-H. Liu, "Bidirectional current-mode capacitor multipliers for on-chip compensation," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 180–188, Jan. 2008.
[22] A. Cabrini, L. Gobbi, and G. Torelli, "A theoretical discussion on performance limits of CMOS charge pumps," in *Proc. Eur. Conf. Circuit Theory Des.*, 2005, vol. 2, pp. II/35–I/38.
[23] A. Cabrini, A. Fantini, and G. Torelli, "High-efficiency regulator for on-chip charge pump voltage elevators," *Electron. Lett.*, vol. 42, pp. 972–973, Aug. 2006.
[24] C. Boffino, A. Cabrini, O. Khouri, and G. Torelli, "High-efficiency control structure for CMOS flash memory charge pumps," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, vol. 1, pp. 121–124.

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