Switching Loss Calculation (SLC) and Positive/Negative Slope Compensation Dynamic Droop Scaling (PNC-DDS) Technique for High-Efficiency Multiple-Input–Single-Output (MISO) Systems

Tin-Jong Tai and Ke-Horng Chen, *Member, IEEE*

***Abstract*—Power management is implemented in a multiple-input–single-output system in this paper. Actually, the design of the switching loss calculation circuit in a dynamic droop system (DDS) can decide the optimum driving solution according to the loading condition, i.e., more than one input source is disabled to reduce the switching loss at light loads. On the other hand, multiple-input sources are preferred to reduce the conduction loss at heavy loads. In other words, DDS with power management can achieve low drop output voltage and high efficiency over a wide load range. The positive/negative-compensated technique enhances the performance of the output voltage stability. Experimental results show that efficiency can be improved approximately 12% at light loads when two input sources are regulated at the switching frequency equal to 5 MHz. Simultaneously, good current sharing is also guaranteed.**

***Index Terms*—Dynamic droop, multiple input, positive/negative compensated (PNC), single output, switching loss calculation (SLC).**

I. Introduction

THE INCREASING demand of green energy in today's electronic devices needs multiple-input sources to deliver high driving capability to a single output. Thus, parallel dc–dc converters are widely used to achieve large driving capability, i.e., the paralleling of dc–dc converter modules offers a number of advantages over a single centralized power supply. High current driving capabilities, flexibility of power delivering capability, and high conversion efficiency over a wide load range force the increasing development of the parallel system.

When several dc–dc converters are connected in parallel, the major concern is the uniform current distribution of each converter. Several current sharing methods with different design complexities and current sharing performances were proposed in the previous literature [1]–[4]. Among these methods, the the droop technique is lower in cost due to minimum interconnections between the paralleled connected modules. The droop method with a large droop resistance will result in a steeper droop slope, and will thus have a better current sharing performance, but it increases the output voltage drop and the conduction loss. The voltage variation may exceed the allowable minimum output value $V_{(o_{\min})}$ at maximum current load $I_{o(\max)}$. The dynamic droop scaling method proposed a new current compensation method to minimize the conduction loss on the path of large output current because of the implementation of dual–current-sensing loops. And the positive/negative slope compensation method compensated the large droop voltage by the slope changing circuit, which keeps the output voltage above the allowable minimum output voltage in case of the increasing load current.

As we know, the conduction loss is much larger than the switching loss at heavy loads. It means that the parallel modules are suitable for improving conversion efficiency due to the less conduction loss. Contrarily, at light loads, the parallel modules consume much power than that of single supply module due to the large switching loss. Thus, a well-designed parallel system must have the ability to decide how many power modules are needed to supply the output load according to the load condition. As conceptually depicted in Fig. 1, the proposed PNC-DDS circuit with power management has the ability to enhance the

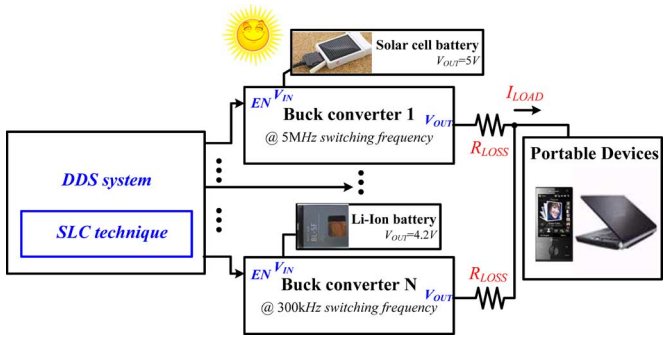


Fig. 1. With the SLC circuit, the proposed PNC-DDS circuit implements power management in the paralleling system.

Manuscript received November 17, 2008; revised February 2, 2009. Current version published May 8, 2009. This work was supported by the National Science Council, Taiwan, under Grant NSC 97-2221-E-009-172 and Grant NSC 97-2220-E-009-027. Recommended for publication by Associate Editor B. Lehman.

T.-J. Tai was with the Department of Electrical and Control Engineering, National Chiao Tung University, Hsinchu 300, Taiwan. He is now with Richtek, Jhubei City 302, Taiwan (e-mail: stratos.ece91@nctu.edu.tw).

K.-H. Chen is with the Department of Electrical and Control Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: khchen@cn.nctu.edu.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2009.2016099

0885-8993/$25.00 © 2009 IEEE

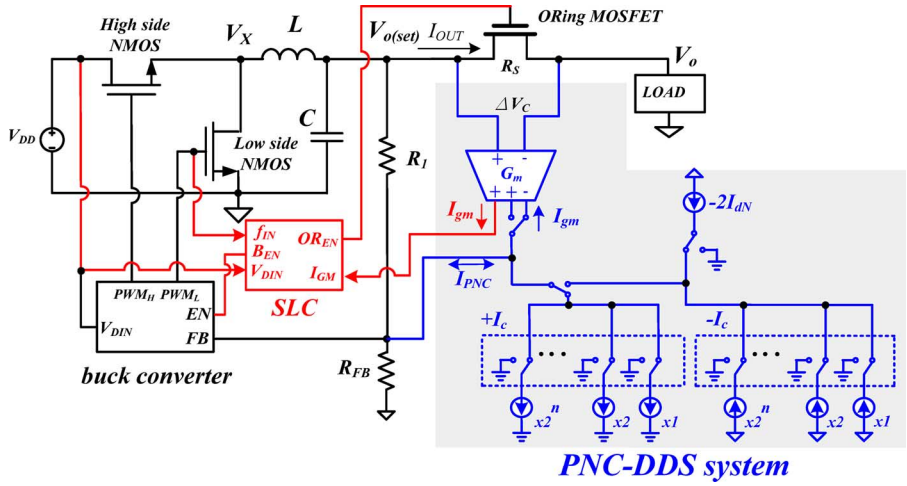


Fig. 2. Current sharing controller with PNC-DDS technique in single module operation.

power conversion efficiency by selecting the number of power converters. Therefore, the PNC-DDS circuit with power management needs a switching loss calculation circuit to decide when the parallel modules have the optimum power conversion efficiency in case of load variations.

In this paper, the PNC technique with the switching loss calculation (SLC) circuit is used to implement the mechanism of power management while it compensated the output voltage droop in the DDS system, as shown in Fig. 2. Due to the SLC circuit, the DDS system can decide how many paralleling power modules are needed to drive the output load. Especially, the input sources can have different input voltages and conversion switching frequencies. In other words, the flexibility is another advantage of the SLC circuit. According to the PNC compensation technique, the output voltage can meet the requirement of minimum allowable voltage while enhancing the current sharing performance.

This paper is organized as follows. Section II introduces the principle of the PNC method and the circuit implementation. Section III describes the concept of the SLC circuit. Analytic results show that the switching loss can be reduced by the SLC circuit. Experimental results in Section IV demonstrate the correctness and performance of the SLC technique in the DDS circuit. Finally, conclusions are drawn in Section V.

II. Positive/Negative Slope Compensation Method

The droop method needs to consider the current balancing performance and the minimum allowable output voltage at the same time. Thus, the DDS method is analyzed and discussed first for extending the current balancing performance within the minimum allowable output voltage. In order to ensure the system stability, the PNC slope compensation method is presented to reduce the oscillation possibility in the DDS method while keeping the same current sharing performance within the minimum allowable output voltage. Furthermore, the positive/negative slope compensation is monotonically added to the whole system without affecting the current balancing speed.

A. Analysis of the Droop Method and the PNC Enhancement Technique

As illustrated in Fig. 3(a), when two buck converters in parallel drive the output $V_{\rm out}$, two cascading resistances are needed to connect the output $V_{\rm out}$ and the two converter outputs (V_{o1} and V_{o2}). The insertion of the cascading resistance R_s can prevent the parallel system from the short circuit effect since there is an initial output voltage mismatch ΔV_o between the outputs (V_{o1} and V_{o2}) of the two converters. The initial current difference ΔI_o can be derived as (1). I_{o1} and I_{o2} are the output currents of the dc–dc converter modules 1 and 2, respectively

$$\Delta I_o = |I_{o1} - I_{o2}| = \frac{|V_{o2} - V_{o1}|}{R_S} = \frac{\Delta V_o}{R_S}. \tag{1}$$

The increasing value of the resistance R_s in Fig. 3(b) can reduce the current difference between the two input sources in parallel. The current difference between the two converter modules on the right side is much lesser than that on the left. The larger value of the resistance R_s can result in a good current sharing performance, but, as shown in Fig. 3(c), it also increased the voltage drop $V_{o(\rm drp)}$ across the resistance R_s and therefore results in the paralleling output $V_{\rm out}$ much below the minimum allowable output voltage $V_{o(\rm min)}$ in Fig. 3(b). The closed loop constituted in the power module regulates the signal FB close to the internal reference voltage $V_{\rm ref}$. The expression of the output voltage $V_{\rm out}$ can be written as (2) with a droop slope that is equal to $-R_s$. The value of the resistance R_s cannot be infinitely increased since the increasing conduction loss further deteriorates the power conversion efficiency of the parallel system

$$V_{\rm out} = V_{\rm ref}\left(1 + \frac{R_1}{R_2}\right) - R_s I_o, \qquad \text{where } V_{o(\rm drp)} = R_s I_o. \tag{2}$$

Obviously, the droop voltage is proportional to the value of the droop resistance. In order to use a large droop resistance for enhancing the current sharing performance and meet the requirement of the minimum allowable output voltage V_o, the

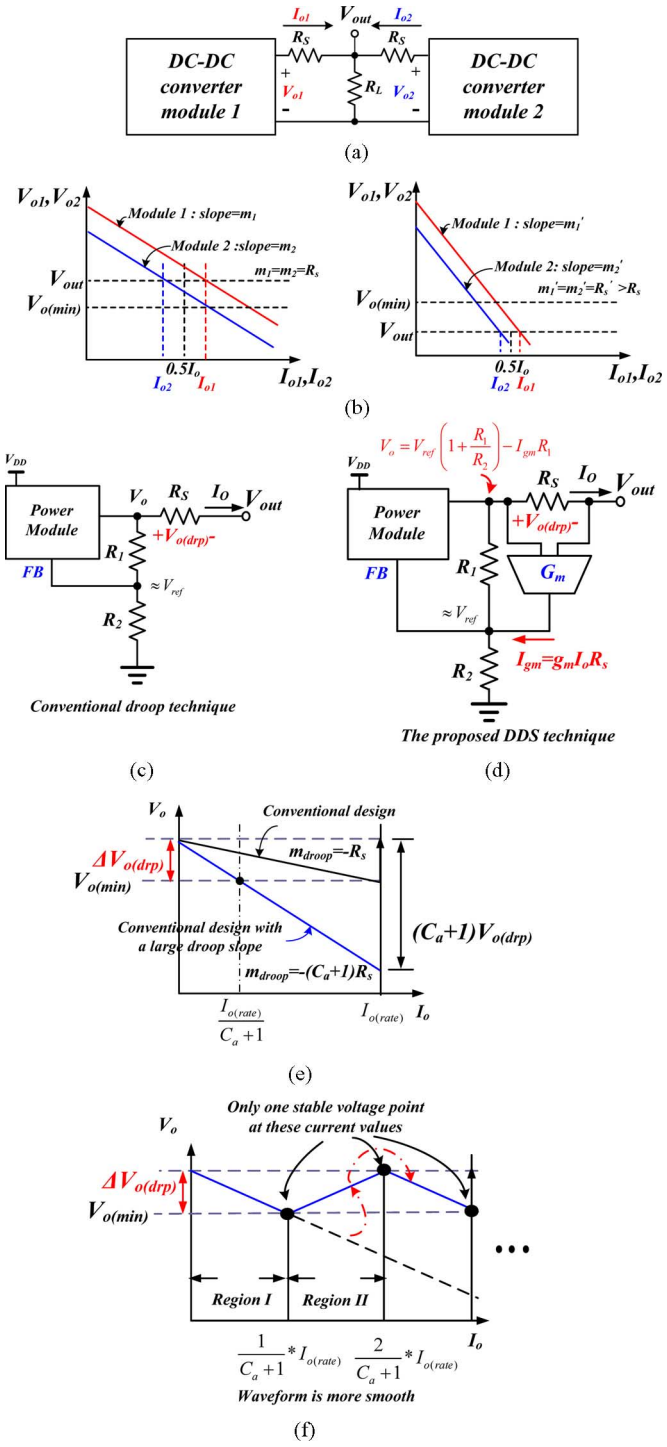


Fig. 3. (a) Block diagram of the paralleling connected dc–dc converters and (b) output voltage waveform for different values of droop resistance. (c) Conventional droop technique. (d) Proposed DDS technique. (e) V–I curve shows the relationship between the minimum allowable output voltage and the rated load current. (f) Solution proposed by the PNC technique.

proposed DDS technique uses a transconductance amplifier G_m, as shown in Fig. 3(d), to convert the signal $V_{o(\mathrm{drp})}$ into a current signal I_{gm}, which is proportional to output current I_o. The current signal I_{gm} is fed back to the terminal FB of the power module. Since the terminal FB will be regulated by the closed-loop negative feedback in steady state, most of the current signal I_{gm} flows through the resistor R_1 to cause the output voltage of the power module equal to (2a). The expression of the output voltage V_{out} in the proposed DDS technique can be derived as (2b)

$$V_o = V_{\mathrm{ref}}\left(1+\frac{R_1}{R_2}\right) - I_{gm}R_1 \tag{2a}$$

$$V_{\mathrm{out}} = V_{\mathrm{ref}}\left(1+\frac{R_1}{R_2}\right) - (1+R_1 g_m)R_s I_o = V_{\mathrm{ref}}\left(1+\frac{R_1}{R_2}\right) - (1+C_a)R_s I_o \qquad \text{where } C_a = R_1 g_m. \tag{2b}$$

The current sharing factor C_a can increase the droop slope from $-R_s$ to $-(1+C_a)R_s$. Interestingly, the currents flowing through the resistor R_s in Fig. 3(c) and (d) have the same value, and thus, the same conduction loss is achieved by the proposed DDS technique. The transconductance amplifier G_m is only used to enhance the value of droop slope. Besides, the power consumption of the resistor R_1 is not changed since the value of current I_{gm} is much less than that of I_o.

As illustrated in Fig. 3(e), the large voltage drop, which is $(C_a+1)V_{o(\mathrm{drp})}$, is still a problem to be solved while enhancing the current sharing performance. Assume that the specification defines the maximum output current as $I_{o(\mathrm{rate})}$ and the minimum allowable paralleling output voltage as $V_{o(\mathrm{min})}$. Since the droop slope is (C_a+1) times that of the original design, it needs to add a compensation voltage to keep the output voltage above $V_{o(\mathrm{min})}$ when the output current I_o exceeds the value of $I_{o(\mathrm{rate})}/(C_a+1)$. At first, the range of the rated current $I_{o(\mathrm{rate})}$ is divided into several segments. Each small region has the size of $I_{o(\mathrm{rate})}/(C_a+1)$. In every region, the proposed PNC method changes the sign of the droop slope but keeps the absolute value of the droop slope to maintain the output voltage in the allowable region. As depicted in Fig. 3(f), the continuous V–I waveform shows only one corresponding output voltage for the current value in the range of the rated current $I_{o(\mathrm{rate})}$. Especially, at the transition point of every region, the specific current value can define only one output voltage value. It implies that the transition between the two adjacent regions is stable and well defined.

B. Design Methodology of the PNC Technique

In Fig. 4(a), a buck converter named as "buck L" has a regulated output voltage $V_{oL(\mathrm{set})}$ at no load. The maximum allowable peak-to-peak voltage variation is $2V_{oL(\mathrm{drp})}$ and the rate current is $I_{oL(\mathrm{rate})}$. The output current of the transconductance amplifier is I_{gmL}. The sinking current at the FB pin is defined as I_{+gmL}, which is proportional to that value of I_{gmL} in order to generate the waveform of V_{+IgmL}. On the other hand, the waveform of V_{-IgmL} is produced by sourcing the current I_{-gmL}, which is proportional to that value of I_{gmL}, at the FB pin. The values of the negative droop slope and the positive droop slope are $-(1+C_a)$ and $(1+C_a)$, respectively. The ratio of the sinking current I_{+gmL} to the sourcing current I_{-gmL} is expressed as (3) since the transconductance amplifier has to reverse the droop current flowing through the resistor R_s. The triangle waveform generated by the PNC technique is composed of the pieces of the

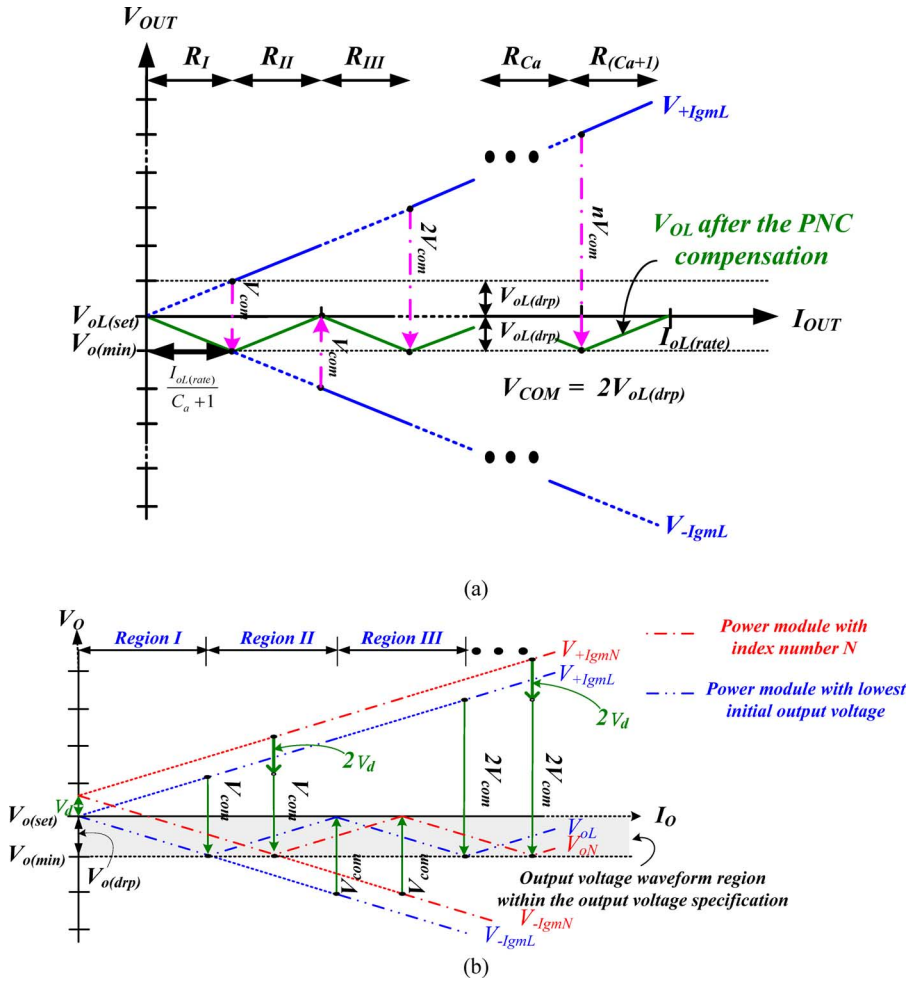


Fig. 4. PNC method analysis for (a) one buck converter with lowest no-load output voltage and (b) analysis for paralleling situation.

waveforms V_{+IgmL} and V_{-IgmL}. As a result, the droop slope of each odd region is $-V_{o(\mathrm{drp})}(C_a+1)/I_{o(\mathrm{rate})}$ and each even region has a slope of $V_{o(\mathrm{drp})}(C_a+1)/I_{o(\mathrm{rate})}$

$$\frac{I_{+gmL}}{I_{-gmL}} = \frac{C_a+2}{C_a}. \tag{3}$$

Besides, a compensation voltage, which has a value of multiple V_{com}, is defined to shift the dc voltage level at the transition between two adjacent regions. According to the value of $V_{oL(\mathrm{drp})}$, the compensation voltage V_{com} can be generated and converted to the compensation current $I_{\mathrm{com}L}$ for each transition point written as

$$I_{\mathrm{com}L} = \sigma \left[\frac{N}{2}\right] \frac{2V_{oL(\mathrm{drp})}}{R_1},$$

where $\sigma = -1^N$ for region $N \neq 1$, $\sigma = 0$ for region I. (4)

Fig. 4(b) shows a paralleling system composed of two buck converters, which are "buck L" and "buck N" as an example to demonstrate the operation of the PNC technique. Assume that the buck converter buck L has the lowest voltage output in the two parallel buck converters at no load. As a result, the output current I_{oL} of buck L can be used as the dominant current to decide the operation region for the paralleling system, i.e., the buck converter buck N follows the region transition of the buck converter buck L. The PNC technique uses the value of $V_{\mathrm{com}L}$ to compensate the waveform of the buck L, and thus, the output voltage V_{oL} is limited within the range formed by $V_{o(\mathrm{set})}$ and $V_{o(\mathrm{min})}$. However, the buck N not only needs the compensation voltage $V_{\mathrm{com}L}$ but also requires the additional compensation $2V_d$ to limit the output voltage V_{oN} within the range formed by $V_{o(\mathrm{set})}$ and $V_{o(\mathrm{min})}$. The value of the additional compensation voltage is generated by injecting the current I_{dN}, which is the difference current between the currents I_{oN} and I_{oL}, to the node FB to flow through the resistor R_1 in Fig. 3(d). The expression of the voltage V_d can be written as

$$\begin{aligned} V_d &= V_{+IgmN} - V_{+IgmL} = g_m R_s \left(I_{oN} - I_{oL}\right) R_1 \\ &= g_m R_s I_{dN} R_1 = \left(I_{+gmN} - I_{+gmL}\right) R_1. \end{aligned} \tag{5}$$

In the positive slope region, it seems that the stability of the paralleling system may be disturbed when the buck converter with larger output current is compensated to a larger output voltage compared to the other buck converter with lower output current. Fortunately, the advantage of the additional compensation voltage V_d can also provide the negative feedback loop for stabilizing the paralleling system during the positive slope

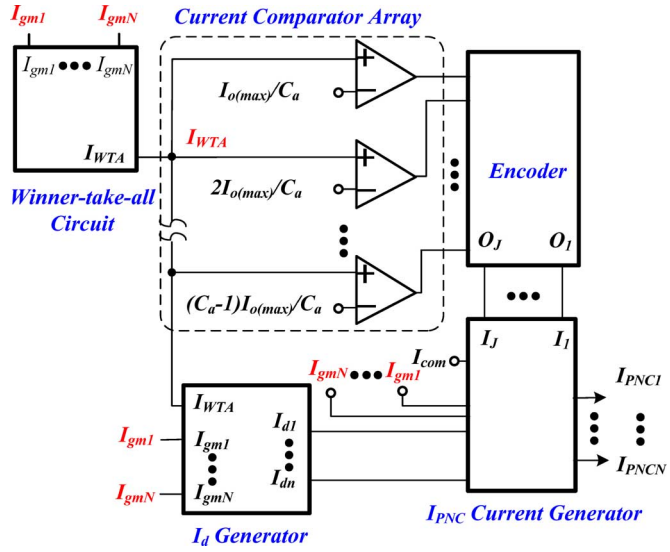


Fig. 5. Block diagram of the PNC circuit.

region. If random perturbation occurs and increases the current difference between the buck converters buck N and buck L, the additional compensation voltage V_d provides additional voltage drop at buck N and reduces the output voltage difference between the buck converters buck N and buck L. As a result, it forces the current difference back to the setting of the PNC technique. Finally, the expression of the current $I_{\rm PNCN}$ for the buck converter buck N is written as (6) where $\sigma = (-1)^k$ for region $k \neq 1$ and $\sigma = 0$ for region I

$$I_{\rm PNCN} = -\sigma I_{gmN} + \sigma \left[\frac{K+1}{2}\right] \frac{2V_{oL(\rm drp)}}{R_1} + (\sigma+1) I_{dN}. \tag{6}$$

C. Block Diagram and Circuit Implementation of the PNC Method

The block diagram of the PNC circuit is depicted in Fig. 5. The winner-take-all (WTA) circuit is utilized to indicate which buck converter contains the lowest output current I_{gmL} among I_{gm1} to I_{gmN} of the N paralleling buck converters. The lowest current is sent to the current comparator array to compare with the internal reference current, and thus, the result can indicate the load condition, i.e., the outputs of the comparator array can be encoded by the encoder to a binary output to indicate the operation region. I_d generator outputs the difference current I_{dK} between the current I_{gmK} of the buck converter with index k and the lowest current I_{gmL}. The compensation current $I_{\rm com}$ defined by the buck converter of the parallel system with the lowest output current can be generated by the system biasing current generator. As a result, for the buck converter with index k, $I_{\rm PNC}$ generator uses the current inputs I_{gmK}, $I_{\rm com}$ and I_{dK} to generate the droop enhancement current $I_{\rm PNCK}$ according to the operation region obtained from the encoder.

Fig. 6(a) shows the implementation of the WTA circuit, which can select the minimum current among N transconductance current [5]. The input currents $I_{gm1} - I_{gmn}$ are converted to the

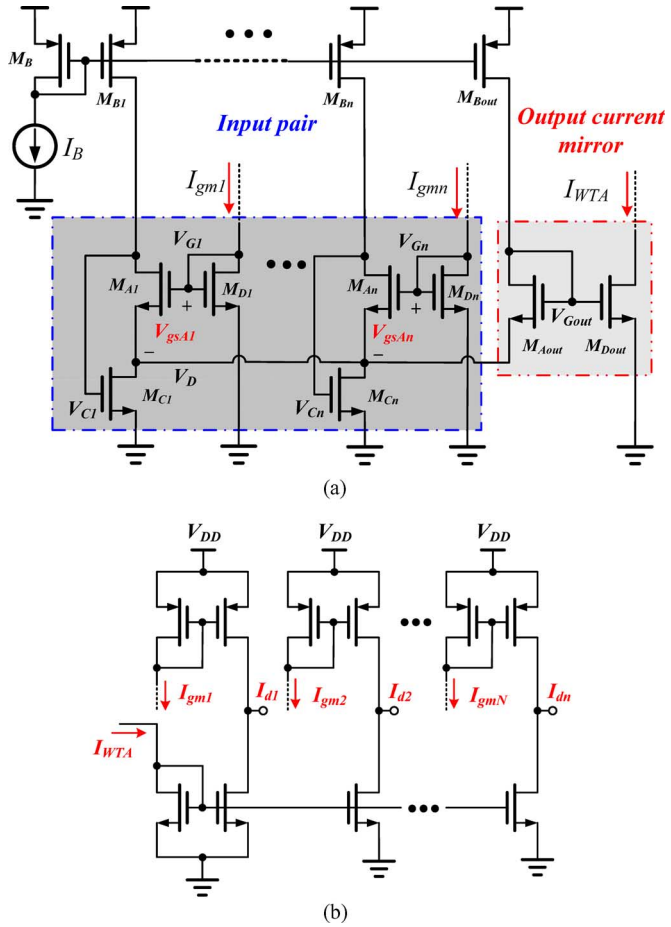


Fig. 6. (a) Implementation of the WTA circuit. (b) I_d generator is used to generate the difference current compared to the minimum current $I_{\rm WTA}$.

voltage signals $V_{G1} - V_{Gn}$ by the diode-connected MOSFETs $M_{D1} - M_{Dn}$. Then, the voltage signals are used to control the gates of the competition MOSFETs $M_{A1} - M_{An}$, which are biased by the same current I_B. Suppose that I_{gm1} is the lowest current, and thus, the voltage V_{G1} is also the lowest voltage too. As a result, the voltage V_D, which is a common source node of all competition MOSFETs $M_{A1} - M_{An}$, is clamped by the lowest voltage V_{G1} due to the biasing current I_B. The value of the voltage V_D is equal to

$$V_D = \sqrt{\frac{I_{gm1}}{(1/2)\mu_n C_{ox}\,(W/L)_{M_{D1}}}} - \sqrt{\frac{I_B}{(1/2)\mu_n C_{ox}\,(W/L)_{M_{A1}}}}. \tag{7}$$

Since V_{gsAk} is larger than V_{gsA1} where $k = 2, 3, \ldots, n$, the drain voltages $V_{C2} - V_{\rm Cn}$ of the MOSFETs $M_{A2} - M_{An}$ will be greatly decreased to keep the same biasing current I_B, and thus, the MOSFETs $M_{C2} - M_{\rm Cn}$ are turned OFF. As a result, the gate voltage $V_{G\rm out}$ of the MOSFET $M_{A\rm out}$ is equal to V_{G1}. The output MOSFET $M_{D\rm out}$ of the output current mirror determines that the output current $I_{\rm WTA}$ is equal to the minimum current I_{gm1}. Furthermore, in order to generate the difference current between all the transconductance currents $I_{gm1} - I_{gmn}$ and the

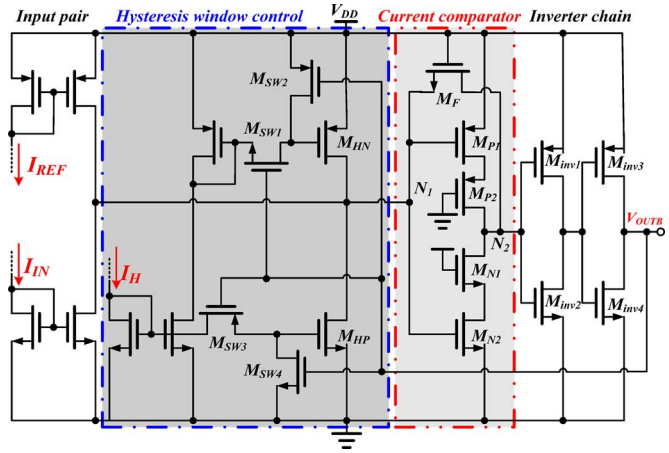


Fig. 7. Circuit implementation of the current comparator.

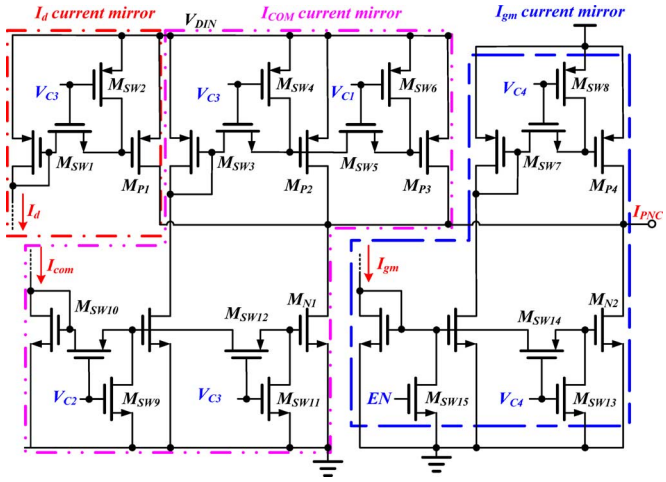


Fig. 8. Circuit implementation of the PNC current generator.

minimum current I_{WTA}, I_d generator shown in Fig. 6(b) is utilized to generate the difference currents $I_{d1} - I_{dn}$.

Fig. 7 depicts the implementation of the current comparator. The hysteresis control part provides the hysteresis window, which is controlled by the hysteresis current I_H and the switches $M_{\mathrm{SW1}} - M_{\mathrm{SW4}}$. The MOSFET M_{HN} sources a hysteresis current I_H to node N_1 when the voltage $V_{\mathrm{OUT}B}$ is high. Contrarily, the MOSFET M_{HP} sinks a hysteresis current I_H at node N_1 when the voltage $V_{\mathrm{OUT}B}$ is low. The hysteresis current window can be adjusted by controlling the width sizes of the MOSFETs M_{HN} and M_{HP}. The comparator part uses the MOSFET M_F to provide a negative feedback loop to reduce the input and output resistances at nodes N_1 and N_2, respectively [6]. The small input resistance results in the small voltage swing at node N_1. As a result, it increases the resolution and reduces the transition time of the comparator. The small output resistance scales down the output voltage swing of the comparator, thereby reducing the transition time. Due to the small input voltage swing at node N_1, the transistors M_{P2} and M_{N1} that operate in the triode region are added to clamp the quiescent current of the current comparator.

The circuit implementation of the PNC current generator is illustrated in Fig. 8. Assume that the paralleling system set the value of the current sharing enhancement coefficient C_a equal to 4 as an example in this paper. The PNC current generator controls the MOSFET switches from M_{SW1} to M_{SW15} to sum the currents I_d, I_{com}, and I_{gm}. The current I_{gm} is generated by the transconductor. The control signals $V_{C1} - V_{C4}$ are generated by the encoder. The corresponding logic signals for different regions are shown in Table I.

TABLE I
CORRESPONDING LOGIC SIGNALS IN DIFFERENT REGIONS

	V_{C1}	V_{C2}	V_{C3}	V_{C4}
Region I	0	1	0	1
Region II	0	0	1	0
Region III	0	0	0	1
Region IV	1	0	1	0

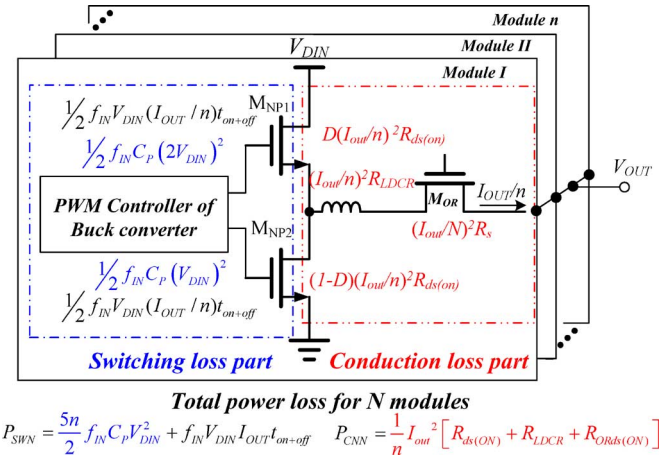


Fig. 9. Loss calculation about one of the buck converters for paralleling N modules.

III. SLC CIRCUIT

According to the function of the SLC circuit, the PNC-DDS system can decide how many paralleling power modules are needed to drive the output load. Especially, the input sources can have different input voltages and conversion switching frequencies. The following subsection will describe the design of the SLC circuit.

A. Analysis of Switching Loss and Conduction Loss in Single Module and Parallel Modules

Supposing that the value of the output current I_{OUT} is several amperes, the internal loss of each buck converter can be ignored. Thus, the major power loss of the external power MOSFET are the switching loss P_{SW} and conduction loss P_{CN}. The output power loss calculation of the buck converter in single module is depicted in Fig. 9 when N is equal to 1. Besides, the droop resistor is implemented by an ORing MOSFET. Due to the bootstrap technique applied to the high-side N-type power MOSFET, the

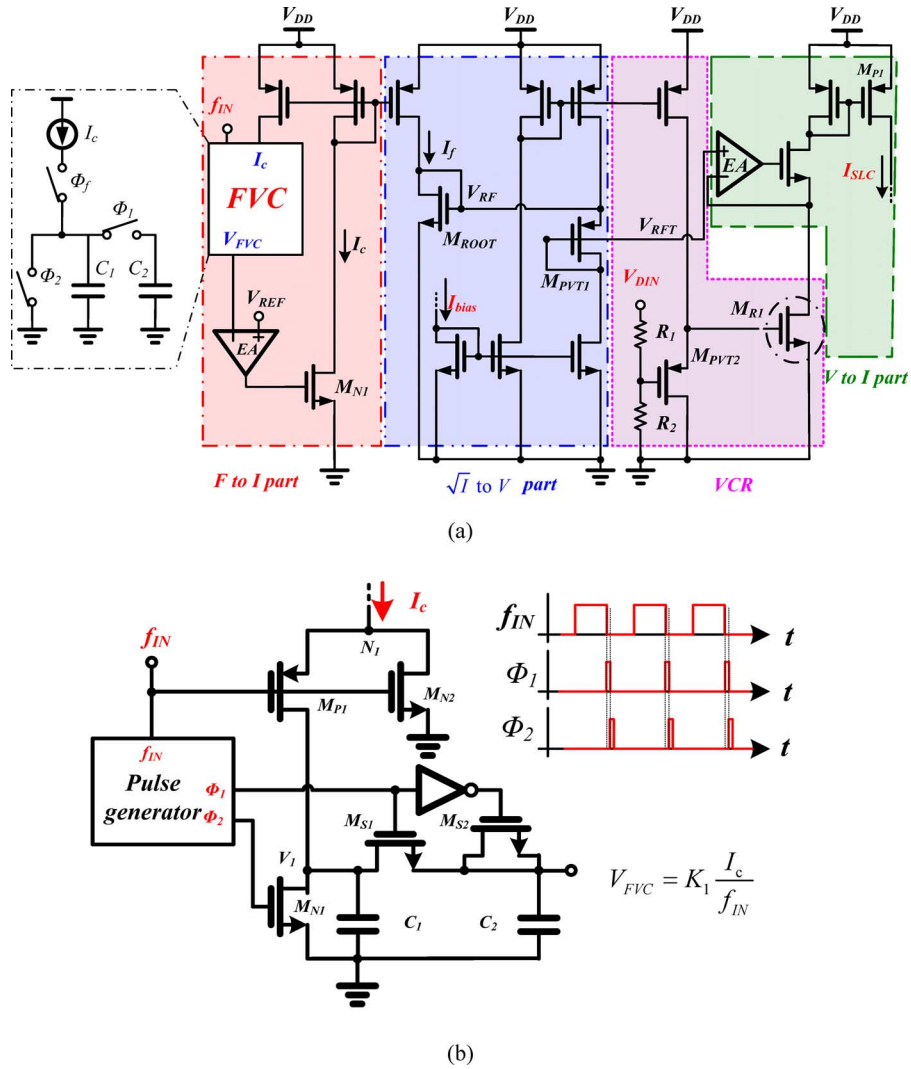


Fig. 10. (a) Schematic of the FIC circuit. (b) FVC circuit and operation waveform.

switching loss of the high-side MOSFET M_{NP1} is four times that of low-side power MOSFET M_{NP2}.

Similarly, as illustrated in Fig. 9, the output power loss is calculated for one of the n buck converters in the paralleling system [7]. Comparing with the power loss in the single module, if the uncharged part is disregarded, the value of $P_{\mathrm{SW}n}$, which is the total switching loss of the n power modules, is n times that of P_{SW1} in a single power module. Besides, the value of the conduction loss P_{CN1} in a single power module is n times that of $P_{\mathrm{CN}n}$, which is the total conduction loss of the n power modules. The switching loss depends on the switching frequency f_{IN} and not on I_{out}. Hence, an incremental power module increases more switching loss but decreases conduction loss. The suitable addition of a single power module can be derived by

$$\Delta P_{\mathrm{SW}} = \Delta P_{\mathrm{CN}} \Rightarrow \frac{5(n-1)f_{IN}C_pV_{\mathrm{DIN}}^2}{2} = \frac{n-1}{n}I_{\mathrm{outp}}^2\left[R_{ds(\mathrm{ON})} + R_s + R_{\mathrm{LDCR}}\right]. \quad (8)$$

C_p is the input capacitor of the power NMOS transistor. R_s and $R_{ds(\mathrm{ON})}$ are the ON-resistances of the ORing MOSFET and power MOSFET, respectively. R_{LDCR} is the dc resistance of the inductor.

In the power loss calculation of a single module, the current sharing issue is not considered. Therefore, $R_{\mathrm{OR}ds(\mathrm{ON})}$ can be scaled down to reduce the conduction loss of oring MOSFET. Assuming that the paralleling system uses n paralleling ORing MOSFETs, the single module has R_s/n and (9)–(10) can be derived

$$\frac{5f_{IN}C_pV_{\mathrm{DIN}}^2}{2} > \frac{1}{n}I_{\mathrm{outp}}^2[R_{ds(\mathrm{ON})} + R_{\mathrm{LDCR}}] \quad (9)$$

$$I_{\mathrm{outp}} = \sqrt{\frac{5nC_p}{2(R_{ds(\mathrm{ON})}+R_{\mathrm{LDCR}})}}\sqrt{f_{IN}}V_{\mathrm{DIN}} = K_C\sqrt{f_{IN}}V_{\mathrm{DIN}}. \quad (10)$$

The current I_{outp} is defined as the transition current between single module and paralleling modules. When the output current I_{out} is lesser than I_{outp}, the conduction loss increased by

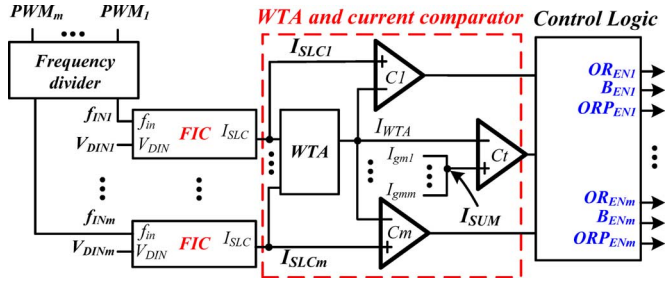


Fig. 11. Parallel control circuit.

paralleling modules is less than the increasing switching loss produced by it. Thus, using only one converter to supply output load current is more efficient. Since the capacitance C_p, the resistances $R_{ds(\mathrm{ON})}$, and R_{LDCR} only depend on the output current specification, a constant value of K_C is used to simplify (10), i.e., the value of I_{outp} is proportional to product of the root of f_{IN} and V_{DIN}. These two parameters have different definitions due to different buck converters. It means that the transition current I_{outp} takes the important parameters of buck converters into consideration to decide the optimum driving condition.

B. Frequency-to-Current Converter Circuit

As illustrated in Fig. 10(a), the frequency-to-current converter (FIC) circuit implements the signal I_{outp} in (10). The FIC circuit can output the current signal I_{SLC} that is proportional to $\sqrt{f_{IN}}$ and V_{DIN}, i.e., the value of current signal I_{SLC} is also proportional to the root of the switching power loss P_{SW}. This FIC circuit can be divided into three blocks, which are the FIC, the $\sqrt{I}$–V converter, and the V–I converter.

The implementation of the frequency-to-voltage converter (FVC) [8] is shown in Fig. 10(b). The charging current is the current signal I_c. The switching frequency f_{IN} decides the turning ON/OFF of the switches M_{P1} and M_{N2}. The sampling clock ϕ_1 is used to sample and hold the voltage from the capacitor C_1 to the capacitor C_2. The switch M_{S2} is used as a dummy transistor to cancel the effect of charge injection and clock feedthrough of the switch M_{S1}. Finally, the reset clock ϕ_2 is used to clear the voltage on the capacitor C_1. The clocks ϕ_1 and ϕ_2 are generated by the pulse generator and the voltage signal V_{FVC} can be expressed as

$$V_{\mathrm{FVC}} = K_1 \frac{I_C}{f_{IN}}, \qquad \text{where } K_1 = \frac{1}{2C_1} \text{ is a constant.} \quad (11)$$

An error amplifier is used to regulate the value of V_{FVC} to that of the reference voltage V_{REF}. The transistor M_{N1} converts V_{FVC} into a current signal I_f.The current signal I_C is a mirrored current from the current I_f. As a result, the current I_f is proportional to f_{in} and expressed as (12)

$$I_f = I_C = K_2 f_{in}, \qquad \text{where } K_2 = \frac{V_{\mathrm{REF}}}{K_1}. \quad (12)$$

The function of the $\sqrt{I}$–V converter is used to generate the root of the current I_f. After using the level-shift transistor M_{PVT1}, which is biased by a small current I_{bias}, the gate voltage V_{RFT} is equal to $V_{RF} - V_T$. The value of V_{RFT} is also

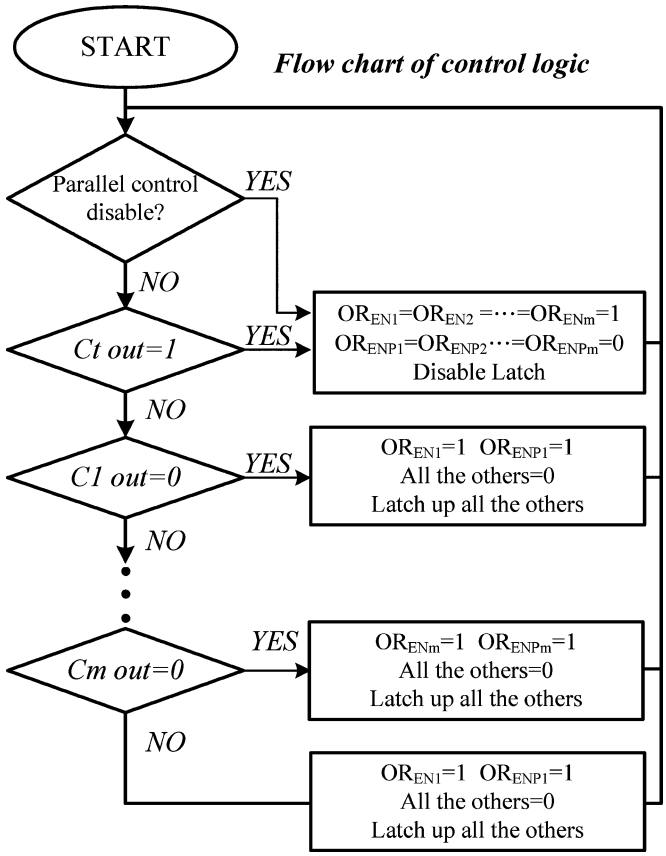


Fig. 12. Flowchart of the control logic for N buck converters in parallel control circuit.

proportional to $\sqrt{f_{IN}}$ and expressed as

$$V_{\mathrm{RFT}} = K_4 \sqrt{K_2 f_{IN}}, \qquad \text{where}$$

$$K_4 = \sqrt{\mu_n C_{ox} \frac{W}{L}_{(M_{\mathrm{ROOT}})}} \text{ is a constant.} \quad (13)$$

In the design of V–I converter, the conversion resistance is implemented by a voltage-control-resistor (VCR). The VCR resistance R_{MR1} is equal to $K_3 V_{\mathrm{DIN}}^{-1}$ and K_3 is a constant value. The resistors R_1 and R_2 make sure that the transistor M_{R1} operated in deep triode region and the transistor M_{PVT2} worked as a level shifter to compensate the voltage V_T of the transistor M_{R1}. Then, the resistance R_{MR1} is the conversion resistance in the V–I converter. Finally, the value of I_{SLC} is decided by (13) and proportional to the value of I_{outp}

$$I_{\mathrm{SLC}} = V_{\mathrm{RFT}} / R_{MR1} = K_5 \sqrt{f_{in}} V_{\mathrm{DIN}},$$

where

$$K_5 = K_4 \frac{\sqrt{K_2}}{K_3} \quad \text{and} \quad K_3 = \frac{1}{\mu_n C_{ox} \frac{W}{L}_{(M_{R1})}}. \quad (14)$$

C. SLC Circuit

Fig. 11 shows the block diagram of parallel control circuit with SLC technique. The pulse-width-modulation signals $\mathrm{PWM}_1 - \mathrm{PWM}_m$ of the parallel buck converters

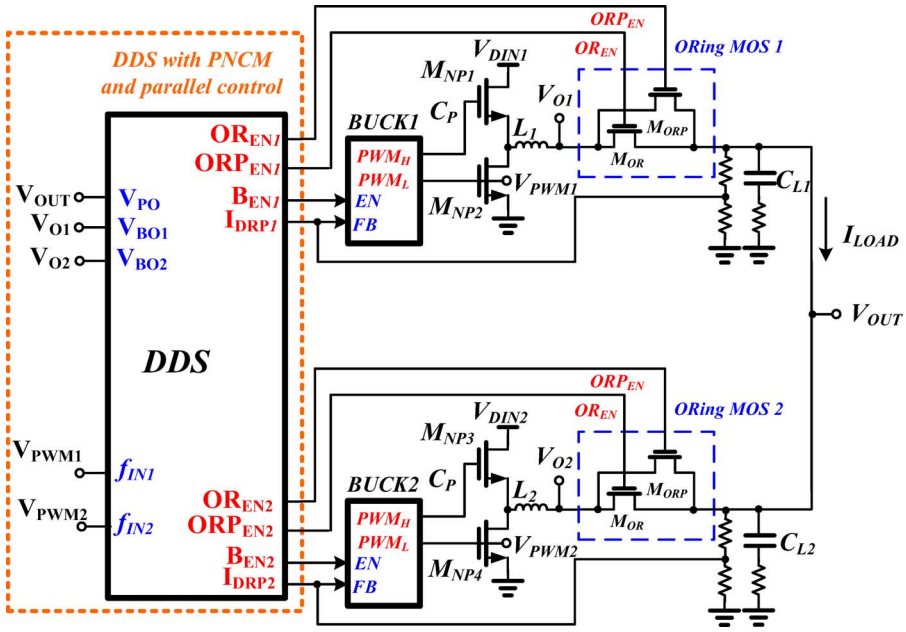


Fig. 13. Implementation of DDS with SLC technique with two buck converters as an example.

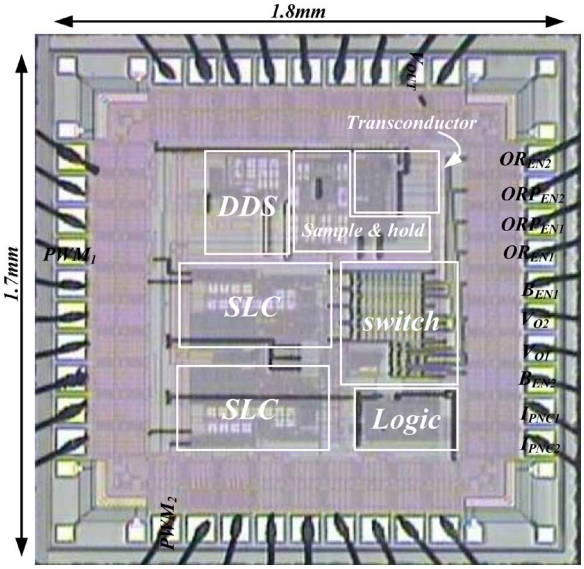


Fig. 14. Chip micrograph of the PNC-DDS circuit with SLC technique.

$\text{buck}_1 - \text{buck}_m$ are used as inputs to the frequency divider to generate the frequency signals $f_{IN1} - f_{INm}$ with fixed duty of 50%. The input supply voltages of the parallel buck converters are $V_{\text{DIN1}} - V_{\text{DIN}m}$. The outputs of the FIC circuits are the current signals $I_{\text{SLC1}} - I_{\text{SLC}m}$ corresponding to the buck converters $\text{buck}_1 - \text{buck}_m$.

The WTA circuit outputs a minimum current I_{WTA}, which is equal to minimum $(I_{\text{SLC1}}, \ldots, I_{\text{SLC}m})$. The value of I_{WTA} is proportional to $I_{\text{out}pL}$ that is equal to minimum $(I_{\text{outp1}}, \ldots, I_{\text{outp}m})$. The current comparators $C_1 - C_m$ compare I_{WTA} with the values of $I_{\text{SLC1}} - I_{\text{SLC}m}$. Due to the hysteretic window in current comparator, the output of comparators decides which buck converter contains the lowest current $I_{\text{out}p}$. It means that the buck converter with lowest value of $I_{\text{out}p}$ should be kept turned ON during single module to achieve minimized switching loss. On the other hand, the other converters with higher values of $I_{\text{out}p}$ are turned OFF to save much switching loss. The current comparator C_t compares the current I_{SUM}, which is written as (15), with the current I_{WTA} to detect whether I_{out} is larger than $I_{\text{out}pL}$ or not, and thus, the operation region can be decided

$$I_{\text{SUM}} = \frac{K_5 \sum_{k=1}^{m} I_{gmk}}{K_C} = \frac{K_5 K_T \sum_{k=1}^{m} I_k}{K_C} = \frac{K_5 K_T I_{\text{out}}}{K_C} \quad \text{where } K_T = g_m R_s. \tag{15}$$

I_k is the output current of the buck converter k and K_C is a constant value as shown in (10). The control logic circuit controls the signal OR_{EN} that connects to the gate of ORing MOSFET in order to decide whether the buck converter needs to deliver the energy from the power source to the output or not. Besides, the signal OR_{ENP} connected to the paralleling ORing MOSFET can determine the value of R_s. The signal B_{EN} connected to the enable pin of buck converter is used to disable the buck converter when the SLC circuit detects higher $I_{\text{out}p}$ in single module operation. Assuming that I_{outp1} is not the lowest among the n buck converters, the converter BUCK1 is disabled and the no-switching signal PWM_1 makes $I_{\text{SLC1}} = 0$ set the operation in single module. However, the value of I_{WTA} is wrong in this condition and may cause the system unstable since the BUCK 1 is turned OFF and has a minimum I_{SLC} value. Thus, the previous output of control logic needs to be on hold to keep the operation of system correct until the system is switched back to the operation of paralleling modules or the enable signal

TABLE II
EXPERIMENTAL PARAMETER

	$R_{ds(on)}$	R_s	C_P	C_{ESR}	R_{ESR}	L	R_{LDCR}	V_{DIN}	f_{IN}	I_{LOAD}	C_a
Buck 1	5mΩ	5mΩ	2000pF	16000μF	1.5mΩ	4.7μH	1mΩ	5V	1MHz	0A to 42A	4
Buck 2	5mΩ	5mΩ	2000pF	16000μF	1.5mΩ	4.7μH	1mΩ	4.2V	300kHz	0A to 42A	4

TABLE III
TRANSITION CURRENT $I_{\rm SLC}$ AND ITS CORRESPONDING $I_{\rm OUTP}$ IN DIFFERENT CONDITIONS

Switching Frequency (f_{IN})	*I_{SLC} @V_{DIN}=4.2V / 5V*	*I_{outp}*
300k	*6.27uA/7.89uA*	*3.79A/4.78A*
500k	*8.11uA / 9.15uA*	*4.86A / 5.49A*
1M	*11.47uA / 12.9uA*	*6.89A / 7.74A*
2M	*16.34uA / 18.49uA*	*9.81A / 11.09A*
5M	*26.51uA / 30.49uA*	*15.57A / 18.29A*

of parallel control circuit is reset. The flowchart of the control logic for the case with N buck converters is shown in Fig. 12.

Fig. 13 illustrates the implementation of the improved PNC-DDS with SLC for the case that contains two paralleling buck converters. The input supply voltages V_{DD1} and V_{DD2} can come from different voltage sources like the NiH battery, the NiCd battery, the Li-ion battery, or the solar cells. The switching frequencies of the two buck converters can be different from each other. The PNC-DDS circuit with SLC circuit can control the paralleling buck converters to achieve high efficiency over a wide load range with good current sharing performance.

IV. EXPERIMENTAL RESULTS OF THE PARALLEL SYSTEM

The improved DDS circuit with power management was fabricated in a TSMC 0.35-μm 2P4M process. The threshold voltages of nMOSFET and pMOSFET are 0.55 and 0.65 V, respectively. Fig. 14 shows the micrograph of the proposed PNC-DDS and SLC circuits. The silicon area is about 3.06 mm^2. The used transistor count is about 3350 and the power consumption of the chip is 2.2 mW.

Two buck converters are used to emulate the paralleling system and test current sharing control by means of using external N-type power MOSFETs for delivering high output current. The high-side power MOSFET uses the bootstrap technique to reduce the conduction loss. The values of $R_{ds(\rm ON)}$ of power MOSFET and R_s of ORing MOSFET are approximated to 5 mΩ. The value of the input capacitor C_P of each power MOSFET is approximated to 4000 pF. An inductor of 4.7 μH with a dc resistance $R_{\rm LDCR} = 1$ mΩ is utilized. The value of the output capacitor C_L is 12 000 p with an ESR resistance $R_{\rm CESR} = 1.5$ mΩ. The testing load current $I_{\rm LOAD}$ varies from 0 to 40 A while the output voltages of two buck converters are $V_{O1} = 2$ V and $V_{O2} = 2.02$ V, respectively at no-load condition. The supply voltage is 4.2 V operating at 300 kHz for one buck converter and is 5V at 5 MHz for the other. The experimental parameters are shown in Table II.

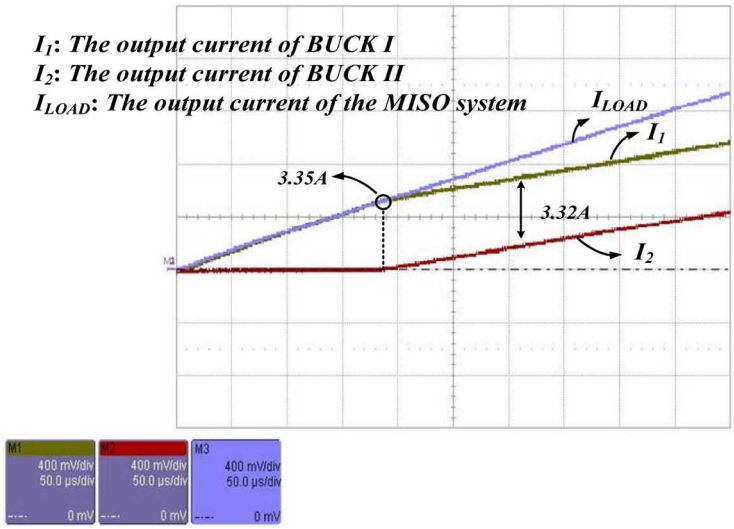
Table III shows the transition current $I_{\rm SLC}$ and its corresponding $I_{{\rm out}p}$ at different input supply voltages and operation frequency conditions. Fig. 15(a) shows the current waveform of the conventional droop method since the dc resistance $R_{\rm LDCR}$ of the inductor increases the resistance at the output current path of both buck converters. Thus, the current difference is about 3.32 A. Fig. 15(b) shows the measured voltage waveform for the PNC-DDS method, the triangle output voltage waveform keeps the parallel output voltage above $V_{o(\min)} = 1.9$ V, and the voltage difference is shrunk from 20 to 5 mV. Fig. 15(c) shows the current waveform of these buck converters, the current difference is reduced from 3.32 to 1 A and the transition current is 3.79 A at these input conditions and the corresponding PWM signal can prove parallel control system works well in this situation.

Fig. 16 shows the efficiency of the buck converters operated in single mode and parallel modules when $V_{\rm DIN} = 5$ V and the switching frequency $f_{IN} = 5$ MHz. The crossover current $I_{\rm CROSS}$ of the efficiency graph is 19.02 A and $I_{{\rm out}p}$ is 18.29 A. The error is about 4%, which is small than the previous data since the power loss can be ignored at heavy loads. The efficiency is derived by (16)

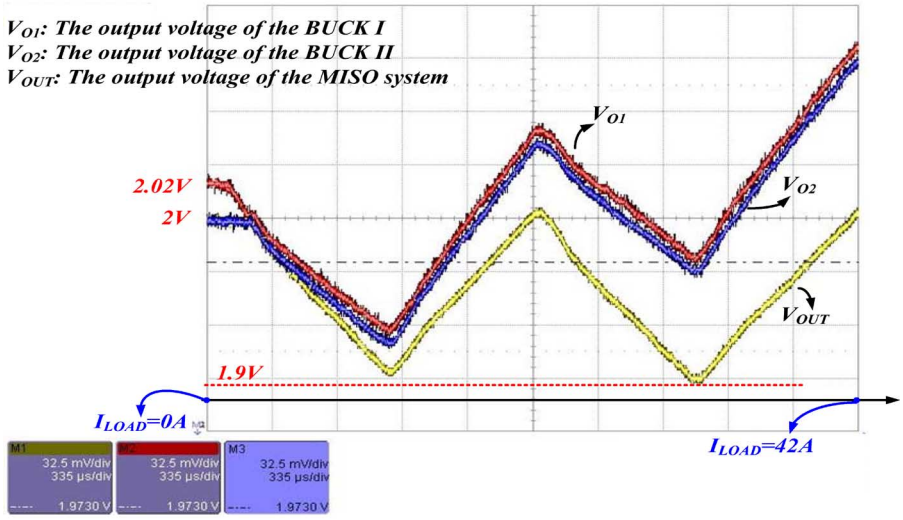
$$\text{Efficiency} = \frac{V_{{\rm OUT}n} I_{On}}{V_{INn} I_{OAVGn}}. \tag{16}$$

I_{On} is the output current, $V_{{\rm OUT}n}$ is the output voltage, and V_{INn} is the supply voltage of buck converter n. After averaging the values of 100 duty cycles, I_{OAVGn} is the mean of the output current from V_{INn}. The crossover current $I_{\rm cross}$ is 3.47 A and $I_{{\rm out}p}$ is 3.79 A in the efficiency graph. The error percentage is about 8.4%, which is caused by the static power loss of buck converters that is ignored compared to the total output power.

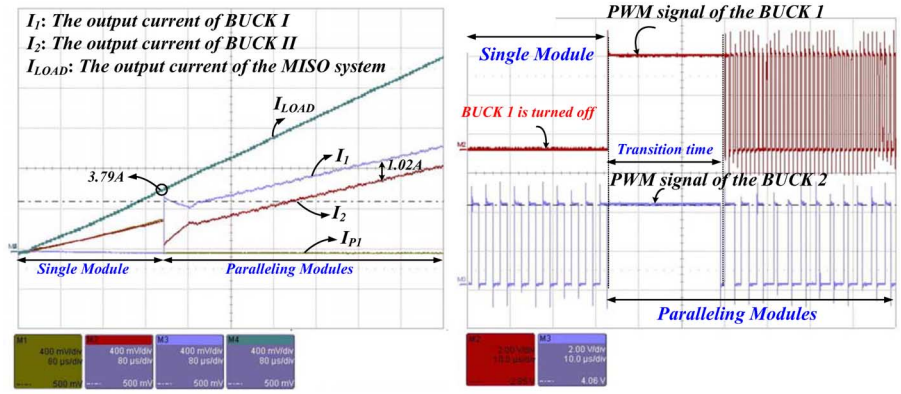
The comparison with other current sharing technique or light-load efficiency enhancement techniques is shown in Table IV. The PNC-DDS with SLC parallel control system can really provide good current sharing performance and improves the light-load efficiency at the same time.



(a)

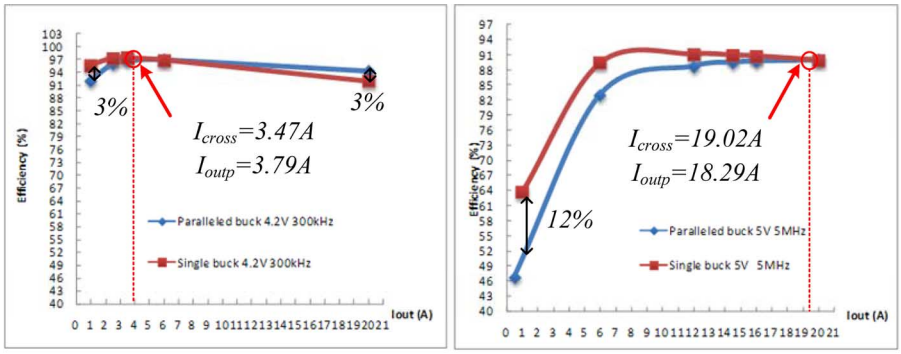


(b)



(c)

Fig. 15. (a) Current waveforms of the conventional method. (b) Measured output voltage waveforms. (c) Enlarged measurement current waveforms at the transition point with the PWM signals of the two buck converters. The current probe magnitude is set 5×.



(a) (b)

Fig. 16. Comparison of the efficiency between single and paralleled buck converters in (a) $V_{\rm DIN}$ = 4.2 V at f_{IN} = 500 kHz and (b) $V_{\rm DIN}$ = 5 V at f_{IN} = 5 MHz.

TABLE IV
COMPARISON WITH CURRENT SHARING TECHNIQUE OR LIGHT-LOAD EFFICIENCY ENHANCEMENT TECHNIQUES

	This work	[9]	[10]	[11]	[12]	[13]
Technology	0.35-μm CMOS	CMOS	0.35-μm CMOS	0.35-μm CMOS	0.35-μm CMOS	0. 5-μm CMOS
Current sharing Performance increased	75% @C_a=4 87.5%@C_a=8 91.7%@C_a=12	90%	75% @C_a=4 87.5%@C_a=8 91.7%@C_a=12	No current sharing	No current sharing	No current sharing
Sharing buss	No need	Need	No need	No	No	No
Voltage variation at transition point	0V	0V	$\Delta V_{o(drp)}$	0V	0V	0V
Power loss reduction at light loads	12% for output current 1A	0%	0%	10% for output current 0.1A	3% for output current 0.1A	11.8% for output current 0.1A
Power loss reduction at heavy loads	3% for output current 20A	0%	0%	0%	0%	0%

V. CONCLUSION

An improved dynamic droop scaling circuit with SLC effectively achieves current sharing control and also increases the power efficiency by dynamically selecting the optimal number of power modules to supply output load. Experimental results show that the paralleling system can always be kept at high conversion efficiency due to the optimization achieved by the switching loss calculation circuit.

ACKNOWLEDGMENT

The authors wish to thank RichTek Technology Corporation and Chunghwa Picture Tubes Ltd. for their help.

REFERENCES

[1] J. A. Abu-Qahouq, L. Huang, and D. Huard, "Sensorless current sharing analysis and scheme for multiphase converters," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2237–2247, Sep. 2008.

[2] J.-W. Kim, H.-S. Choi, and B. H. Cho, "A novel droop method for converter parallel operation," *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 25–32, Jan. 2002.

[3] V. J. Thottuvelil and G. C. Verghese, "Analysis and control design of paralleled DC/DC converters with current sharing," *IEEE Trans. Power Electron.*, vol. 13, no. 4, pp. 635–644, Jul. 1998.

[4] B. Tomescu and H. F. Vanlandingham, "Improved large-signal performance of paralleled DC–DC converters current sharing," *IEEE Trans. Power Electron.*, vol. 14, no. 3, pp. 573–577, May 1999.

[5] J. Ramírez-Angulo, G. Ducoudray-Acevedo, R. G. Carvajal, and A. López-Martín, "Low-voltage high-performance voltage-mode and current-mode WTA circuits based on flipped voltage followers," in *Proc. TCSII 2005*, pp. 420–423.

[6] S. Khucharoensin and V. Kasemsuwan, "Robust high-speed low input impedance CMOS current comparator," in *Proc. IEEE MWSCAS*, Jul. 2004, pp. 93–96.

[7] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronic*, 2nd ed. Norwell, MA: Kluwer, 2001.

[8] A. Djemouai, M. Sawm, and M. Slamani, "High performance integrated CMOS frequency-to-voltage converter," in *Proc. ICM 1998*, pp. 63–66.

[9] J. Abu-Qahouq, H. Mao, and I. Batarseh, "Multiphase voltage-mode hysteretic controlled DC–DC converter with novel current sharing," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1397–1407, Nov. 2004.

[10] H.-H. Ho, K.-H. Chen, and W.-T. Chen, "Dynamic droop scaling for improving current sharing performance in a system with multiple supplies," in *Proc. IEEE ISCAS*, 2007, pp. 545–548.

[11] T. Y. Man, P. K. T. Mok, and M. Chan, "An auto-selectable-frequency pulse-width modulator for buck converters with improved light-load efficiency," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 440–626.

[12] E. Bonizzoni, F. Borghetti, P. Malcovati, F. Maloberti, and B. Niessen, "A 200 mA 93% peak efficiency single-inductor dual-output DC–DC buck converter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 526–619.

[13] M. D. Mulligan, B. Broach, and T. H. Lee, "A 3MHz low-voltage buck converter with improved light load efficiency," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 528–620.

Tin-Jong Tai was born in Hsinchu, Taiwan, in 1983. He received the B.S. and M.S. degrees from the National Chiao Tung University, Hsinchu, in 2006, 2008, respectively.

He was with the Low Power Mixed Signal Laboratory, where he was engaged in current sharing techniques and dc–dc converters. He is currently with Richtek, Ltd., Dongguan, China. His research interests include dc–dc converters, current sharing techniques, and analog integrated circuit design.

Ke-Horng Chen (M'04) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1994, 1996, and 2003, respectively.

From 1996 to 1998, he was a Part-Time IC Designer at Philips, Taipei. From 1998 to 2000, he was an Application Engineer at Avanti Ltd., Taiwan. From 2000 to 2003, he was a Project Manager at ACARD Ltd., where he was engaged in designing power management ICs. He is currently an Associate Professor in the Department of Electrical and Control Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he organized a Mixed-Signal and Power Management IC Laboratory. He is the author or coauthor of more than 65 papers published in journals and conferences, and also holds several patents. His current research interests include power management ICs, mixed-signal circuit designs, display algorithms and driver designs of liquid crystal display (LCD) TV, RGB color sequential backlight designs for optically compensated bend panels, and low-voltage circuit designs.