# 國立交通大學

材料科學與工程學系

## 博士論文

覆晶封裝銲錫接點的電遷移與應力遷移行為之 研究

Electromigration and stress migration behaviors in flip-chip solder joints

研 究 生: 梁右峻

指導教授:陳智教授

中華民國一零二年八月

# 覆晶封裝銲錫接點的電遷移與應力遷移行為之研究 Electromigration and stress migration behaviors in flip-chip solder joints

研究生: 梁右峻 Student: Yu-Chun Liang

指導教授:陳智 Advisor: Chih Chen

國立交通大學材料科學與工程學系博士論文

A Thesis

Submitted to Department of Materials Science and Engineering

College of Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy

in

Materials Science and Engineering

August 2013

Hsinchu, Taiwan, Republic of China

中華民國一零二年八月

#### 覆晶封裝銲錫接點的電遷移與應力遷移行為之研究

學生:梁右峻 指導教授:陳智 教授

國立交通大學材料科學與工程學系

#### 摘要

覆晶封裝銲錫接點的電遷移是一個重要的可靠度議題,是故了解 覆晶封裝銲錫接點內的電流密度及溫度分佈相當重要。另外,本研究 第一個觀測到銲錫內有應力遷移現象,並導致大裂縫生成。我們利用 實驗觀測,配合有限元素分析法與理論計算模型研究覆晶封裝銲錫接 點的電遷移與應力遷移行為。

本研究探討了銅柱金屬墊層對於覆晶封裝銲錫接點內電遷移的電流聚集效應與焦耳熱效應的影響。三維電流密度分佈的模擬結果顯示銅柱金屬墊層改變了電流聚集效應在銲錫接點內的位置以及嚴重程度,進而改變了兩種不同銲錫接點結構的電遷移破壞模式。經由紅外線熱像儀的觀察,銅柱金屬墊層在降低銲錫接點內電流聚集效應的同時也減少了銲錫接點在通電時所產生的焦耳熱。因此,銅柱金屬墊層有助於提升銲錫接點的電遷移壽命。另外,孔洞生成與金屬墊層消

耗兩種電遷移破壞模式皆出現在無溫度梯度的錫銀銲錫接點中。藉由 理論模型計算錫原子在介金屬化合物與銲錫界面上電遷移通量和化 學勢能通量的差異,若通往陽極端的電遷移通量較大,破壞模式為孔 洞生成;而當通往陰極端的化學勢能通量較大,則破壞模式為金屬墊 層消耗。且此理論計算模型與實驗結果吻合。

另一方面,應力遷移亦會導致銲錫接點的破壞。錫鉛複合銲錫接點在經過500週期的溫度循環測試後,應力梯度驅使錫原子移動,導致非等向性長條狀的錫晶粒粗化並聚集在銲錫接點的頸縮處。接著,由熱應力引起的裂縫便沿著長條狀的錫晶粒與富鉛相界面傳播。在經過14410週期的溫度循環測試後,裂縫會擴大並延伸穿過整個銲錫接點。應力模擬結果顯示銲錫接點的頸縮處是張應力區域,且裂縫的生成起始於錫鉛的界面上。

THE PARTY OF THE P

# Electromigration and stress migration behaviors in flip-chip solder joints

Student: Yu-Chun Liang Advisor: Dr. Chih Chen

#### **Department of Materials Science and Engineering**

**National Chiao Tung University** 

#### Abstract

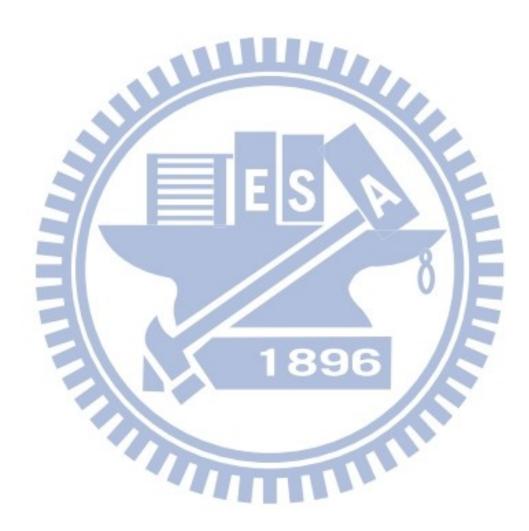
Electromigration (EM) has been an important reliability issue in flip-chip solder joints. Thus, to investigate the current density and temperature distribution in a solder joint is of great significance. In addition, we first reported stress migration in solder joints and it induced large cracks. In this study, we studied the EM and stress migration experimentally and adopted finite element analysis and theoretical analysis to provide further understanding of the two issues.

Influence of Cu column under-bump-metallizations (UBMs) on current crowding and Joule heating effects of electromigration in flip-chip solder joints have been investigated. A three-dimensional simulation of the current density distribution was performed to provide a better understanding of the current crowding behavior, which

was found to account for the different failure modes for the two kinds of solder bumps. One more important finding is, as confirmed by infrared (IR) microscopy, that the alleviation of current crowding by Cu column UBMs also helped decrease Joule heating effect in solder bumps during current stressing. Therefore, the measured failure time for the solder joints with Cu column UBMs appears to be much longer than that of the ones with the 2-µm Ni UBMs. In addition, void formation and UBM consumption failure mechanisms occurred respectively at the stressing conditions both without a thermal gradient in the SnAg solder joints with 5-μm-Cu/3-μm-Ni UBM measured by IR microscopy. We proposed a model considering the flux divergence at the intermetallic compound/solder interface to calculate the Sn EM fluxes toward the anode side and the chemical potential-driven fluxes toward the cathode side. UBM consumption is responsible for the failure when the Sn chemical potential flux surpasses the EM flux. Yet, voids formed at the interface when the trend reverses. This model successfully explains the experimental results.

On the other hand, stress migration results in large cracks in solder joints. After 500 cycles of temperature cycling tests (TCTs) between -55 and 125 °C in SnPb composite solder joints, the Sn grains coarsened and developed anisotropic stripes close to the necking site in the solder joint because of stress-induced atomic migration. Then, cracks triggered by thermal stress were observed to propagate along the Sn

stripe interfaces. After a prolonged 14410 cycles of TCT, the cracks expanded across the entire solder joint.



#### Acknowledgements

感謝我的指導教授陳智老師的指導,老師對我的教導除了在專業領域的知識之外,跟在老師身邊學習的五年時間裡,我也在老師的身上學到許多做人處事的道理,皆讓我在此生的人生道路上獲益良多。老師培養我獨立思考的能力,並時常鼓勵我保持樂觀積極的態度來面對種種的困境。另外,老師給我許多出國參與國際研討會的機會,這些難得的機會不僅讓我和國際上知名學者有知識交流的機會,並可以體驗到各國的風俗民情,更重要的是培養我的國際觀,寬闊我的視野。也特別感謝在UCLA的杜經寧教授,多次在實驗上給予我重要而且實貴的建議。在此也要感謝我的口試委員:高振宏教授、廖建能教授、吳子嘉教授以及張立教授,對於我的博士論文細心的指導與建議。

感謝曾經伴我在實驗室中一起成長的學長姐、同學及學弟妹們: 翔耀、世緯、筱芸、宗寬、元蔚、詠湟、健民、佳凌、漢文、瑋安、 建志、岱霖、朝俊、曉蔵、若薇、以撒、韋嵐、育安、天麟、明墉、 韋奇、致嘉、俊毅、偉豪、秉儒、竣傑、玉龍、奕丞、皆安、瓈云、 順財、岱陽。還要特別感謝指導我專題研究的國原學長以及牧龍學長。 因為你們,我的研究生涯才得以豐富及順利。

感謝我的家人、朋友及女朋友,一路上的陪伴、支持與付出。還 有所有曾經在我研究生涯幫助過我的人,點滴之恩,銘記在心,謝謝。

### **Contents**

摘要	i
Abstract	iii
Acknowledgements	vi
Contents	vii
List of tables	xi
List of figures	xii
Chapter 1 Overview of interfacial reaction, electromigration, thermo	omigration
and stress migration in flip-chip technology	
1.1 Flip-chip technology	1
1.2 Interfacial reaction	3
1.3 Electromigration	5
1.3.1 Failure sites and flux divergence	7
1.3.2 Current crowding effect	9
1.3.3 Joule heating effect	11
1.3.4 Mean time to failure	13
1.4 Thermomigration	14
1 4 1 Measurement of the heat of transport	15

1.4.2 Thermomigration accompanying electromigration in flip-chip	solder
joints	17
1.4.3 Thermomigration in composite SnPb flip-chip solder joints	18
1.4.4 Thermomigration in Pb-free flip-chip solder joints	19
1.5 Stress migration.	20
1.6 Motivation	21
Chapter 2 Influence of Cu column UBMs on current crowding and Joule he effects of electromigration in flip-chip solder joints	ieating
2.1 Introduction	35
2.2 Experimental procedure	37
2.3 Simulation	39
2.4 Results and discussion	39
2.4.1 Electromigration failure site and failure mechanism change	39
2.4.2 Current crowding effect	42
2.4.3 Joule heating effect	44
2.4.4 Mean time to failure	46
2.5 Summary	47

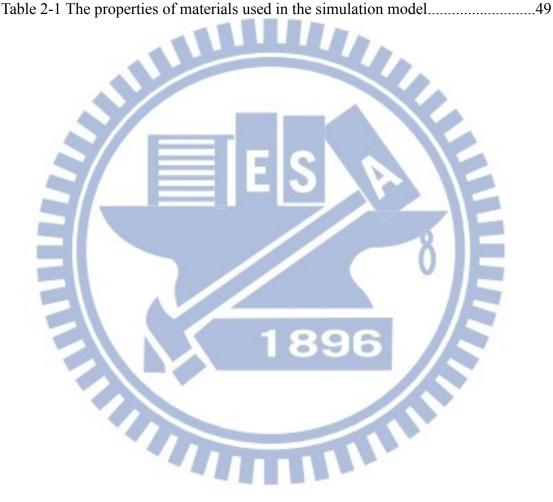
Chapter	3 Chemical	potential-driven	Sn at	oms refill	against	electron	wind	force
during c	urrent stress	sinσ						

3.1 Introduction.	59
3.2 Experimental procedure	60
3.3 Results and discussion	62
3.3.1 Electromigration behaviors at various stressing conditions	62
3.3.2 Theoretical analysis on flux divergence at the IMC/solder interface	63
3.4 Summary	67
Chapter 4 Stress-migration-induced anisotropic grain growth and	crack
propagation in eutectic microstructure under cyclic temperature annealing	ng in
flip-chip SnPb composite solder joints	
4.1 Introduction.	73
4.2 Experimental procedure	75
4.3 Results and discussion.	76
4.3.1 Anisotropic Sn stripe formation in TCT	76
4.3.2 Circular Sn grain formation in isothermal annealing	78
4.3.3 Unmixing of the high-Pb and the eutectic SnPb in isothermal and cy	cling
annealinσ	79

4.3.4 Three-dimensional finite element analysis of thermal stress distribution8	30
4.3.5 Stress-migration-induced anisotropic grain growth of Sn	31
4.3.6 Crack propagation along the Sn/Pb interfaces	2
4.4 Summary8	3
Chapter 5 Conclusions9	13
STED BY	95
Publication list	2

#### List of tables

Table 1-1 Melting temperature, diffusivity and diffusion mechanism for	Cu, Al, Pt
and SnPb solder [16]	22
Table 1-2 Experimental values of $Q_A^*$ in some pure metals [34]	23
Table 2.1 The preparties of materials used in the simulation model	40



#### List of figures

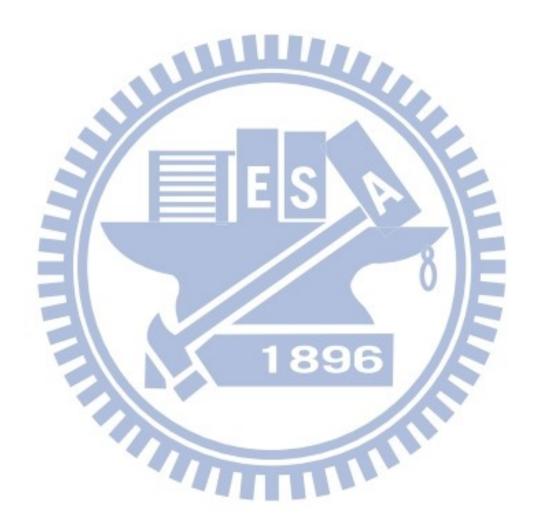
Figure 1-1 (a) A tilt-view of SEM image of arrays of solder bumps on silicon die. (b)
A flip-chip solder joint to connect the chip side and the module side. (c) The chip
placed upside down (flip chip), and all the joints are formed simultaneously between
chip and substrate by reflow [1,5]24
Figure 1-2 (a) Blech's pioneering electromigration sample, showing an aluminum
strip deposited on a conducting TiN layer. (b) An SEM image of the morphology of a
Cu strip tested for 99 h at 350 °C with current density of $5 \times 10^5$ A/cm <sup>2</sup>
[16,18]25
Figure 1-3 A schematic diagram of two-dimensional conductor film with grain
boundary and intersection [18]26
Figure 1-4 (a) The unique line to bump geometry of a flip-chip solder bump joining to
a interconnect line on the chip side (top) and a conducting trace on the substrate side
(bottom). (b) The two-dimensional simulation of current density distribution in a
solder joint [16,42]
Figure 1-5 (a) The SEM image of a sequence of void formation and propagation in a
flip-chip eutectic SnPb solder bump stressed at 125 °C and $2.25 \times 10^4$ A/cm <sup>2</sup> for 40 h.
(b) The SEM image of void formation in a flip-chip 95.5Sn-4.0Ag-0.5Cu solder bump
stressed at 146 °C and 3 $67 \times 10^3$ A/cm <sup>2</sup> [24 25]

Figure 1-6 Plot of carbon content (logarithmic scale) vs. 1/T for sectioned alpha iron
specimen [26]
Figure 1-7 The formation of voids on the chip side and accumulation of solder on the
substrate side for the solder bump with (a) downward electron flow and (b) upward
electron flow [27]
Figure 1-8 (a) A cross section of a composite 97Pb3Sn and 37Pb63Sn flip-chip solder
joint. (b) The SEM image of the cross section. The darker region at the bottom is the
eutectic SnPb. The brighter region is the 97Pb3Sn phase [37,42]31
Figure 1-9 (a) A schematic diagram depicting 24 bumps on the periphery of a Si chip.
Each bump has its original microstructure, as shown in Figure 1-9(b), before EM
stressing. EM was conducted at 1.6 $ imes$ 10 <sup>4</sup> A/cm <sup>2</sup> at 150 °C through only four pairs
of bumps on the chip's periphery: pairs 6/7, 10/11, 14/15, and 18/19. (b) TM affected
all the un-powered solder joints: The darker eutectic phase moved to the hot Si side
[37]
Figure 1-10 SEM images of cross-sectioned bump with markers before and after TM
test at 1.01× 10 <sup>4</sup> A/cm <sup>2</sup> and 100 °C. (a) Before TM, and (b) After 800 h of the TM
test. The markers moved toward the substrate side [38]
Figure 1-11 (a) Cross-sectional SEM images representing the microstructure for an
un-powered bump before a TM test. (b) Temperature distribution measured by an

infrared microscope when the neighboring bumps were stressed by 0.55A at 150 °C.
The built-in thermal gradient was 1143°C/cm across the solder bump. (c) After the
TM test for 60 h. The Cu UBM was dissolved [42]
Figure 2-1 Schematics of the flip-chip solder joints with (a) a Ni UBM and (b) a Cu
column UBM in this study50
Figure 2-2 The simulation model for one pair of the flip-chip solder joints. The arrows
show the direction of the electron flow
Figure 2-3 Cross-sectional SEM images of a solder bump with a 2- $\mu$ m Ni UBM
stressed at $2.16 \times 10^4$ A/cm <sup>2</sup> at 150 °C for (a) 0 h, (b) 42.7 h with upward electron
flow, (c) EDS analysis at the point A in (b), and (d) 42.7 h with downward electron
flow
Figure 2-4 Cross-sectional SEM images of a solder bump with a Cu column UBM
stressed at $2.16 \times 10^4$ A/cm <sup>2</sup> at 150 °C for (a) 0 h, (b) 286.5 h with upward electron
flow, and (c) 286.5 h with downward electron flow
Figure 2-5 Simulation results for current density distribution in the solder bump with
a 2-µm Ni UBM when powered by 1.5 A
Figure 2-6 Simulation results for the current density distribution in (a) the Cu column
UBM and (b) the solder bump beneath when powered by 1.5 A
Figure 2-7 Temperature increases in solders with 2-μm Ni UBMs and Cu column

OBMs during current stressing as a function of applied currents and current
density56
Figure 2-8 IR images showing the temperature distribution in solder bumps with (a) a
$2\text{-}\mu m$ Ni UBM and (b) a Cu column UBM during current stressing of $2.30\times10^4$
A/cm <sup>2</sup> at 100 °C
Figure 2-9 (a) The temperature profile along the $\overline{AB}$ line in Figure 2-8(a). (b) The
temperature profile along the $\overline{\text{CD}}$ line in Figure 2-8(b)
Figure 3-1 Cross-sectional schematic structure of (a) the electromigration tests layout
design and Kelvin bump probe structure for measuring bump resistance and (b) the
solder joint configuration used in this study69
Figure 3-2 Cross-sectional SEM image showing the microstructure of the solder joint
after current stressing by (a) 1.15 $\times$ 10 <sup>4</sup> A/cm <sup>2</sup> at 133.2 °C for 474.7 h and (b) 5.3 $\times$
10 <sup>3</sup> A/cm <sup>2</sup> at 175.3 °C for 83.2 h70
Figure 3-3 Schematic drawing of a solder joint subject to a downward electron
flow71
Figure 3-4 The calculated curves for the Sn EM and chemical potential fluxes stressed
by (a) $1.15 \times 10^4$ A/cm <sup>2</sup> at 125 °C and (b) $5.3 \times 10^3$ A/cm <sup>2</sup> at 175 °C as a function of
time
Figure 4-1 (a) Schematic diagram for the solder joint structure used in this study. (b)

Cross-sectional SEM images showing the as-reflowed SnPb composite solder joint. (c
SEM image showing the FIB-polished second cross-section of the as-fabricated solder
bump
Figure 4-2 (a) and (b) Cross-sectional SEM images showing the solder bump after
500 cycles of TCT. (c) SEM image showing the FIB-polished second cross-section of
the solder bump after 500 cycles of TCT86
Figure 4-3 (a) and (b) Cross-sectional SEM images showing the solder bump after
1500 cycles of TCT. (c) SEM image showing the FIB-polished second cross-section
of the solder bump after 1500 cycles of TCT87
Figure 4-4 (a) and (b) Cross-sectional SEM images showing the solder bump after
14410 cycles of TCT. (c) SEM image showing the FIB-polished second cross-section
of the solder bump after 14410 cycles of TCT88
Figure 4-5 Cross-sectional SEM image and SEM image showing the FIB-polished
second cross-section of the solder bump after an isothermal annealing at 150 °C for
(a), (b) 500 h, (c), (d) 1000 h, and (e), (f) 2160 h89
Figure 4-6 The average IMCs thickness as a function of time
Figure 4-7 Simulation results for the total mechanical and thermal equivalent strain
distribution in (a) the solder bump and (b) the Sn63Pb37 presolder after one cycle of
TCT 01



Chapter 1 Overview of interfacial reaction, electromigration, thermomigration and stress migration in flip-chip technology

#### 1.1 Flip-chip technology

To meet the relentless demand for miniaturization of portable devices, flip-chip technology has been adopted for high-density packaging due to its excellent electrical characteristic and superior heat dissipation capability [1]. As the required performance in microelectronics devices becomes higher, flip-chip technology was adopted to increase more signal and power interconnections than wire bonding in electronic devices. In 1960s, IBM first developed the flip-chip technology, called as controlled-collapse-chip-connection (C4) [2-4]. In the C4 technology, high-Pb solder with high melting temperature of 320 °C was used as the joint material [5]. Then the chip was aligned on the ceramic substrate. This C4 technology gained wide utilization in the 1980s since it can provides the advantages in size, performance, flexibility, and reliability over other packaging methods. Owing to the area array capability in flip-chip technology, the size of product, the height of solder bump, and the length of interconnect are effectively reduced, the higher input/output (I/O) pin count and speed in electronic devices was provided.

Before flip-chip assemblies, solder bumps need to be deposited onto the under-bump-metallization (UBM) on the chip side. The requirements for UBMs are: (1) it must adhere well both on the underlying metal line, like Al or Cu, and on the surrounding IC passivation layer, (2) it is able to provide a strong barrier to prevent the diffusion of bump metals into the integrated circuit (IC) and (3) it needs to be readily wettable by the bump metals during solder reflow. For example, a thin film Cr/Cu/Au UBM is adopted for the high-Pb solder alloy in the C4 technology.

The tilt view of solder joints on silicon chip is shown in Figure 1-1(a). Figure 1-1(b) is the cross-sectional view of the flip-chip solder joints. As depicted in Figure 1-1(c), the chip with IC is then placed upside down (flip chip), and all the joints are formed simultaneously between chip and substrate during the reflowing process. In flip-chip process, electrical connections are the array of solder bumps on the chip surface, hence interconnects distance between package and chip is effectively reduced. The density of I/O is limited by minimum distance between adjacent bonding pads. For high ends device, when size reduction is the main concern, area-arrayed flip-chip technology is the only choice to meet the needs.

However, the flip-chip technology has some evolutions due to certain concern. In order to cost down the consumer electronics, the polymer substrates, like Bismaleimide Triazine (BT) or Flame Retardant 4 (FR4), are used to replace the

ceramic substrate. For this concern, the high-Pb solder has no longer been used due to its high melting point of 320 °C since polymers have very low glass transition temperature. Thus, the eutectic SnPb solder alloy can been used to solve this problem by its low melting point of 183 °C. Next, owing to the environment concern, the Pb-free solder alloys replace the Pb-containing solder alloys due to the toxic of Pb. Then, the thin film UBM will not be suitable for this change. Therefore, the electroplating 5-µm Cu or 5-µm Cu/3-µm Ni was used as the UBM for the Pb-free solder joints. Because of these evolutions, several kinds of solder alloys and UBMs are proposed for the flip-chip assemblies. This makes the flip-chip technology become complex to study since there has too many combinations. The best solder alloy and UBM will provide a lot of benefit for the industry.

# 1896

#### 1.2 Interfacial reaction

Solder is widely used to connect chips to their packaging substrates in flip-chip technology as well as in ball-grid-array (BGA) technology [6]. In the last 50 years, the electronics industry has relied mainly on one type of solder (Sn–Pb solder) in products manufacture [7]. With the discovery of Pb as a contaminant both to the environment and to human health, new developments have been made to steer away from the use of Sn–Pb solder [8,9]. In 2000, National Electronics Manufacturing

Initiative (NEMI) recommended to replace eutectic Sn–Pb solder by eutectic Sn–Ag–Cu solder in reflow processing and eutectic Sn–Cu solder in wave soldering [6].

A reliable solder joint can be formed by metallurgical reactions between molten solders and UBM on a chip or metallization on the substrate, which produces stable intermetallic compounds (IMCs) at the joint interfaces [10]. During the soldering process, the formation of IMCs between solder alloys and the metallization layer is inevitable. The growth of these IMCs can strongly affect the mechanical reliability of the solder joints [11-13]. As a result, selection of appropriate UBMs plays an important role in developing a reliable flip-chip solder joint, especially the adoption of the lead-free solders due to environmental concerns.

Copper is widely used in the UBM and substrate metallization for flip-chip and BGA applications. It is known that at the Cu/solder interface, Sn reacts rapidly with Cu to form Cu–Sn IMC, which weakens the solder joints due to the brittle nature of the IMC [14]. Therefore, Ni is used as a diffusion barrier layer to prevent the rapid interfacial reaction between solder and Cu layer in electronic devices.

Recently, the reaction between solder and Ni has received much attention because the reaction rate is about two orders of magnitude slower than that of Cu, so the effect of spalling of IMC on thin film Ni is less serious and Ni can also serve as diffusion barrier. Why the reaction rate between Ni and solder is much slower than

that between Cu and solder has been an interesting kinetic question. The answer is not very clear right now; mostly it is because the supply of Ni to the reaction that may be much slower than Cu. The supply may depend on the diffusion of Ni along the interface between Ni<sub>3</sub>Sn<sub>4</sub> and Ni and also the solubility of Ni in the molten solder [15].

#### 1.3 Electromigration

Electromigration (EM) is the phenomenon of mass transportation due to momentum transfer from high current density. Such a mechanism can result in open or short circuit modes of failure. The mechanism also impacts both the design and manufacturing of metallization. For electromigration in a metal, the driving force of the net atomic flux consists of two forces: (1) the direct action of electrostatic field on the diffusion atom, electrostatic force, and (2) the momentum exchange between the moving electrons and the ionic atoms on the diffusion atom, electron wind force. It can be expressed as

$$F = F_{direct} + F_{wind} = Z^* e E = (Z_{el}^* + Z_{wd}^*) e E$$
 (1-1)

where  $Z^*$  is the effective charge number, e is the electron charge, and E is the electric field. The effective charge  $Z^*$  is consisted of two terms,  $Z^*_{el}$  and  $Z^*_{wd}$ .  $Z^*_{el}$  is positive and can be regarded as the nominal valence of the diffusion ion in the metal

when the dynamic screening effect is ignored. When these positively charged metal ions are under the field effect, this so called "direct force" draws atoms towards the negative electrode. In the contrary,  $Z_{wd}^*$  the wind force, is usually negative and represents the momentum effect from electron flow that pushes atoms towards the positive electrode. Generally, the electron wind force dominates and is found to be on the order of 10 for a good conductor like Ag, Al, Cu, Pb, Sn, etc [16].  $Z_{wd}^*$  can also be positive, but it was found only in transition elements with complex band structures where electron hole conduction plays a more important role [17]. The atomic flux is related to the electric field and thus the current density. The flux equation can then be expressed as the following:

$$J = J_{chem} + J_{em} = -C \frac{D}{kT} \frac{\partial \mu}{\partial x} + C \frac{D}{kT} Z^* eE$$
 (1-2)

$$E = \rho j \tag{1-3}$$

where C is atomic concentration, D is atomic diffusivity, k is Boltzmann's constant, and T is temperature. P is resistivity and j is current density. The flux is a function of temperature. As shown in the equation below, the atomic diffusivity is exponentially dependent on temperature.

$$D = D_0 exp\left(-\frac{Q}{RT}\right) \tag{1-4}$$

where  $D_0$  is diffusion coefficient, R is gas constant, and Q is activation energy of diffusion.

For electromigration to occur, a nonvanishing divergence of atomic flux is a requirement. The divergence may be due to a temperature gradient or microstructural inhomogeneity. Since electromigration is cumulative, it affects the failure rate. Therefore, the mean time to failure (MTTF) in the presence of electromigration is given by the equation

$$MTTF = A \frac{1}{i^n} exp\left(\frac{Q}{kT}\right) \tag{1-5}$$

The electromigration exponent ranges from n=1 to n=6, i.e. n=2 for Al interconnect. The failure mechanism results in voids, cracks, and hillocks in the samples.

#### 1.3.1 Failure sites and flux divergence

Electromigration was first observed in Al metal interconnects. Less than 0.2% Cu atoms were added to Al line to reduce the effect of electromigration [16]. Blech first developed a structure of a short Al or Cu strip in a base line of TiN to conduct electromigration tests as shown in Figure 1-2(a) [18,19]. Because Al or Cu has lower resistance, as electric field was applied on two ends of TiN line, electric current in TiN took a detour to go along the strip of Al or Cu. After electromigration test, a depleted region occurs at the cathode and an extrusion is observed at the anode. Figure 1-2(b) is the scanning electron microscope (SEM) image of the morphology of

a Cu strip tested for 99 h at 350 °C with a current density of 5×10<sup>5</sup> A/cm<sup>2</sup>. By conservation of mass, both depletion and extrusion should have the same volume change. We can then calculate the drift velocity from the rate of depletion. In the past years, an impetus to study electromigration in very fine conductors has arisen from the development of very large-scale integrated circuits. The conductors are not only interested in small dimensions; they are often assembled into multilayered structure with a certain combination of conductors and insulators. This gives rise to electromigration problems which is distinctly different from simple single-level conductor line.

The metal layer is a two-dimensional (2D) conductor film that can be considered as an ensemble of grain boundaries and their intersections as illustrated in Figure 1-3. Experimental observations have indicated that in most cases, mass depletion and accumulation initiate at grain boundary intersection such as triple junctions. The former would eventually lead to the formation of voids or cracks and the latter to hillocks or whiskers. The reason that the grain boundary intersections are likely to be the failure sites is that they often represent the spots where the mass flux would diverge the most. At the grain boundary intersections, there could be an abrupt change in grain size, which produces a change in the number of paths for mass movement; there also could be a change in atomic diffusivity due to the change in grain boundary

microstructure.

Recently damascene structure have been developed to form Cu interconnect. Cu material is used to replace Al due to its higher electrical conduction. Because Cu has higher melting temperature, its diffusion mechanism is surface diffusion instead of grain boundary diffusion [20]. As for solder joints, because it has lower melting temperature, the diffusion mechanism is lattice diffusion for most solders at a typical operation temperature of an electronic device around 100 °C. Table 1-1 lists the melting temperature of Al, Cu, SnPb solder, and their corresponding diffusion mechanism.

#### 1.3.2 Current crowding effect

Within a metal line, as soon as the electromigration-induced damage forms, current density also becomes non-uniform. As voids or cracks grow, the non-uniformity of the current density over a conductor line increases. Since the Joule heating is proportional to the square of the current density, the local temperature will also increase rapidly. The current crowding effect therefore plays dual roles here: both the elevated local density and temperature accelerate the electromigration process. Thus obtaining an accurate current crowding density distribution is necessary in determining the flux divergence [20].

Current crowding phenomenon is an even more serious issue in flip-chip solder joints. Figure 1-4(a) demonstrates the unique line to bump geometry of a flip-chip solder bump joining an interconnect line on the chip side (top) and a conducting trace on the substrate side (bottom) [17,21,22,23]. Because the cross section of the line on the chip side is about two orders of magnitude smaller than that of a solder joint, the current density changes significantly from the metal line to the solder as current enters the solder joint. The change leads to the current crowding at the entrance into the solder bump, thus resulting in the change of magnitude of current density from 10<sup>5</sup> A/cm<sup>2</sup> to 10<sup>4</sup> A/cm<sup>2</sup> at the current crowding region in a typical Al line to solder bump structure. Figure 1-4(b) is a 2D simulation of current distribution in a solder joint. Note that this current crowding phenomenon leads to non-uniform current distribution inside a solder joint. The current density at the current crowding region is one order of magnitude higher than the average current density at the center of the solder joint. Since the drift velocity is proportional to the current density and non-uniform temperature distribution inside a solder joint due to local Joule heating effect (see Section 1.3.3), electromigration-induced damage occurs near the contact between the on-chip line and the bump; voids formation for the bumps with electrons downward and hillock or whisker for the bumps with electrons upward. Therefore, current crowding effect plays a crucial role in the flip-chip solder joints under electromigration. Consequently, electromigration damage occurs near the contact between the line and the bump; voids induced from the damage can propagate along the interface due to the non-uniform current distribution [24].

In those flip-chip solder joints using a thin film UBM, the current crowding leads to a pancake-type void across the entire cathode contact [25,26]. Figure 1-5(a) displays the SEM images of eutectic SnPb after electromigration [24]. After current stressing for 40 h at 125 °C and 2.25 × 10<sup>4</sup> A/cm<sup>2</sup>, voids are seen in the left-upper corner since electron flow entered the bump from the upper-left corner of the joint. Similar phenomena were also observed in Sn-4.0Ag-0.5 Cu Pb-free solder joints as shown in Figure 1-5(b) [25]. Pancake-type void is clearly seen at the corner of flip-chip solder joints when the cathode is on the chip side. With current stressing time increases, pancake-type voids propagate across the top of solder joints, resulting in open failure.

#### **1.3.3 Joule Heating Effect**

When the current flow passes through a conductor, the heat generated due to the electrons vibrating the atoms in the conductor. This is so called Joule heating effect.

The heating power can be describe as:

$$P = I^2 R = j^2 \rho V \tag{1-6}$$

where P is heating power, I is applied current, R is resistance of the conductor, j is current density,  $\rho$  is resistivity of the conductor, and V is volume of the conductor. Thus, the heating is controlled by two factors: first is the applied current, and the other is the resistance of the conductor.

When the current applied to a flip-chip solder joint is relatively high, the whole system will generate a huge amount of heat resulting from the conducting traces and solder bumps. Generally, the total length of the Al trace can reach few meters, which the effective resistance is approximately few ohms. In contrast, the resistances of the solder bumps and the Cu trace on the substrate are relatively low, typically in the order of few or tens of milliohms. Therefore, the major contribution for Joule heating in flip-chip solder joints comes from the Al trace [27-29]. As a result, the temperature in the bumps during accelerated testing is likely to be much higher than that of the ambient because of the Joule heating. Moreover, the current crowding effect will cause the local high current density; in other words, there will be a local Joule heating in the solder joints and result in a non-unformed temperature distribution. Chiu et al reported the "hot spot" exists inside the solder bumps at the current crowding region [29,30]. The combination of the Joule heating of Al interconnects on the chip side and the non-uniform current distribution will lead to a temperature gradient across the solder joints. Consequently, Joule heating effect induced temperature increase in the

flip-chip solder joints under electromigration significantly affects the analysis of failure time.

#### 1.3.4 Mean time to failure

Electromigration requires a nonvanishing divergence of atomic flux. Since electromigration is cumulative, it affects the failure rate. In statistical study, the test samples should be stressed at the same current and temperature conditions. Then, the failure times or lifetimes can be recorded and plot by Weibull or normal distribution. In Weibull distribution, the time of 63.2% of reliability is denoted as the mean-time-to-failure (MTTF) [31]. In 1969, James R. Black explained the MTTF in the presence of electromigration is given by the equation [32]:

$$MTTF = A \frac{1}{j^n} exp\left(\frac{Q}{kT}\right) \tag{1-5}$$

where A is a constant, j is the current density, n is a model parameter, Q is the activation energy, k is the Boltzmann's constant, and T is the average temperature. There are four of parameters: j, n, Q, and T needed to be examined and analyzed. However, the current crowding effect and the Joule heating effect play important roles under electromigration in flip-chip solder joints. To further consider about these two effects in MTTF analysis, the modified Black's equation becomes:

$$MTTF = A \frac{1}{(cj)^n} exp\left[\frac{Q}{k(T+\Delta T)}\right]$$
 (1-7)

by multiplying j with a crowding ratio c and adding an increment of  $\Delta T$  due to Joule heating [33]. For the following discussion, the estimated MTTF will be a key result to compare to each other.

#### 1.4 Thermomigration

Thermomigration (TM) is the flux of component in a solution induced by the temperature gradient. The phenomenon has also been called thermal diffusion. When a concentration gradient is established due to the impressed temperature, it is known as Ludwig-Soret Effect [26]. From the atomic point of view, temperature gradient can lead to the un-mixing of an initially homogenous alloy due to a biasing of the atomic jump [17]. Instead of electrical field, as in the case for electromigration, the effective driving force exerted by the temperature gradient is expressed as

$$F = \frac{Q^*}{T} \frac{dT}{dx} \tag{1-8}$$

where  $Q^*$  is the experimental determined parameter which describes the sign and magnitude of the thermo-transport effect. It is called the heat of transport of the component.  $Q^*$  is positive in the flux equation when the flux is from hot to cold region. For situation in which one component is diffusing, e.g. an interstitial alloy, the flux equation is then given as [27, 39]

$$J = J_{chem} + J_{TM} = -C \frac{D}{kT} \frac{\partial \mu}{\partial x} - C \frac{D}{kT} \frac{Q^*}{T} \frac{dT}{dx}$$
 (1-9)

D/kT is the mobility of the diffusing component, and dC/dx is the concentration gradient at constant temperature. Note that D is the diffusion coefficient. The temperature gradient does not change the jump mechanism or mean jump frequency at any given temperature. However, it biases the direction of jump.

#### 1.4.1 Measurement of the heat of transport

 $Q^*$  can be obtained by two methods. One method is to allow flux to go to zero in a temperature gradient and measure the concentration gradient at J=0. The other method is to measure the flux through an open system at a known temperature gradient. Figure 1-6 demonstrates the concentration of carbon content in an initially single-phase alloy (0.01%C) under a temperature gradient until a steady state was established. Note the final concentration gradient across the specimen is a linearly relationship with temperature and concentration becomes higher at the hot end. With the flux equals to zero, equation (1-9) becomes

$$\frac{dlnC_1}{dx} = -\frac{Q_1^*}{RT^2} \frac{dT}{dx} \tag{1-10}$$

The method allows  $Q^*$  to be obtained from the slope of the curve without any information on the diffusion coefficient. In the case of the  $\alpha$ -Fe shown in Figure 1-6,  $Q_c^* = -96\,$  kJ/mol. It means carbon moves toward the hot end.

In pure metal diffusion occurs by the motion of vacancies so the flux of atom is

highly affected by the change in the equilibrium vacancy with temperature. The flux of the element under a temperature gradient can be expressed as

$$J = -\frac{D_A}{\Omega} \frac{(Q_A^* - H_v)}{RT^2} \frac{\partial T}{\partial x}$$
 (1-11)

where  $\Omega$  is atomic volume and  $H_v$  is enthalpy of formation of vacancies.  $Q_A^*$  is heat of transport for element A. Experiments have been done by heating one end of pure metal and cooling the other end or by heating the center of a sample by passing an electric current through it and keeping the end cold. The net flux of atom is then measured by the motion of inert marker relative to the end of the sample. Table 1-2 [34] lists the experimental values of  $Q_A^*$  for several pure metals. All the values for  $H_v$  are invariably larger than  $Q_A^*$  so the vacancy concentration gradient dominates and the net flux of vacancies is always toward the cold end. As a result, more vacant sites at the hot end allow atoms to jump into on its higher temperature side than on its lower temperature site. An increase in the distance between markers in the hottest parts of the sample is observed [17]. Since the effect of  $Q_A^*$  is small relative to the vacancy gradient effect,  $Q_A^*$  cannot be measured with much accuracy. The situation becomes even more complex when it becomes binary alloys. Whether one element becomes enriched at the hot end or cold end of the sample is determined by the competition between the flows of the two elements relative to the lattice under the temperature gradient.

#### 1.4.2 Thermomigration accompanying electromigration in flip-chip solder joints

Thermomigration has been reported to accompany electromigration in flip-chip solder joints recently [35,36]. The major heat source exerted on solder joints is from Al trace on the Si die side. Longer electric current path and high current density in Al trace increase the temperature of the Si chip tremendously. As a result, a temperature gradient existed across solder joints and thermomigration can occur along with electromigration. Figures 1-7(a) and (b) show the SEM images of an example of a pair of eutectic SnPb solder joints after current stressing. The sample was finely polished to half of the bump before the testing. Figure 1-7(a) shows the formation of the voids on the chip side and accumulation of solder on the substrate side for the solder bump with downward electron flow. However, as shown in Figure 1-7(b), for the solder bump with upward electron flow, voids were also observed on the chip side. This phenomenon cannot be explained by electromigration since the atomic movement is against electron flow on the chip side. It is due to the competing effect of electromigration and thermomigration, as further proved by the marker movement. From temperature measurement and simulation, it was estimated that a temperature difference of 15 °C generated across a solder joint of 100 µm in diameter, and the temperature gradient of 1500 °C/cm seems sufficient to cause thermomigration in eutectic SnPb solder joints.

### 1.4.3 Thermomigration in composite SnPb flip-chip solder joints

The combination effect of electromigration and thermomigration was observed for powered bump. When the electronic device is large and thermal dissipation is sufficient on the Si chip, signal bump or unpowered bump has minimal thermal effect. However, when the electronic device and bump pitch become smaller, thermal effect from the powered bump can no longer be neglected.

To induce thermomigration in the composite solder joints, we used the temperature gradient induced by Joule heating in electromigration test. A set of flip-chip samples is depicted in Figure 1-8(a) [37], wherein there are 24 bumps on the periphery of a Si chip, and all the bumps have their original microstructure, as shown in Figure 1-8(b), before electromigration stressing. After electromigration was conducted through only four pairs of bumps—pairs 6/7, 10/11, 14/15, and 18/19 in Figure 1-9(a), thermomigration affected all the unpowered solder joints, as shown in Figure 1-9(b). All the Sn (the darker image) migrated to the hot Si side, whereas the Pb migrated to the cold substrate side. The redistribution of Sn and Pb was caused by the temperature gradient across the solder joints because no current was applied to them. Since Si has a very good thermal conductivity, the Joule heating of Al interconnects on the chip side of the four pairs of powered bumps has heated the

entire Si chip to induce a temperature gradient and in turn the thermomigration across all the unpowered bumps.

### 1.4.4 Thermomigration in Pb-free flip-chip solder joints

Hsiao et al. [38] performed thermomigration by operating with alternating current (AC) and direct current (DC). The advantage of AC is that there would be no electromigration under AC, and this will be a good way to decouple electromigration and thermomigration. The schematic diagram of a Pb-free solder bump used in thermomigration study is shown in Figure 1-10(a). After 800 h of  $1.01 \times 10^4$  A/cm<sup>2</sup> current stressing at 100 °C, hillocks are present on the chip side, as shown in Figure 1-10(b). The hillocks are formed by the mass transfer in the solder bump caused by thermomigration and comprised of Sn confirmed using a SEM energy dispersive spectroscopy (EDS). This result reveals that Sn atoms are driven from cold side to the hot side under thermomigration.

Moreover, during electrmigration test which will couple with thermomigration, not only solder (Sn or Pb) will affect but also UBMs. The dissolution of Cu and Ni in Pb-free solders is quite high, and the diffusion of Cu and Ni in Sn is anisotropic and very fast. The diffusion rate along the c-axis of Sn crystals is faster than that in the a-and b-axis. The dissolution of Cu and Ni atoms may occur under a thermal gradient

[39]. Figure 1-11(a) shows a eutectic SnAg solder bump with a 5-µm UBM on the chip side before a TM test. This bump was next to a bump that was under EM stressing at 0.55 A and 150 °C. This joint had no current passing through it but possessed a thermal gradient of 1143 °C/cm, as illustrated in Figure 1-11(b). After 60 h of the TM test, the Cu-Sn IMC migrated to the cold (substrate) end, as shown in Figure 1-11(c). Although this bump was un-powered, the damage is clear near the upper left corner, as indicated in Figure 1-11(c). The Cu UBM dissolved almost completely into the solder. This dissolution can be attributed to the TM of Cu atoms by fast interstitial diffusion and the reaction with Sn atoms to form Cu-Sn IMCs inside the solder bump.

# 1.5 Stress migration

At high homologous temperatures and low stresses polycrystalline materials deform by diffusional creep. Material redistribution during the creeping process can either occur as the result of the diffusional transport of material through the grains or along the grain boundaries. Nabarro originally described the process of creep deformation by lattice diffusion, and a general framework for analyzing diffusive mechanisms was developed by Herring [40,41]. According to Nabarro-Herring model of creep, atomic flux will diffuse from the compressive region to the tensile region.

The atomic flux is related to the stress gradient, and the flux equation can then be expressed as the following:

$$J = C \frac{D}{kT} \frac{d\sigma\Omega}{dx} \tag{1-12}$$

where C is the concentration, D is the atomic diffusivity, kT has the usual meaning,  $\Omega$  is the atomic volume, and  $d\sigma/dx$  is the stress gradient. When crystalline solids are tested under creep conditions at low stresses and high homologous temperatures, the creep rates vary linearly with the applied stress so that strain is accumulated through the processes of Nabarro-Herring creep, and how the stress migration affect the evolution of the microstructure in the solder joints will be discussed later.

### 1.6 Motivation

In this thesis, we study the electromigration behavior and the stress migration behavior in the solder joints. When the system is subject to electromigration, thermomigration, and stress migration, the overall flux can be expressed in terms of chemical force, electrical wind force, thermal gradient, and stress gradient as the following:

$$J = -C\frac{D}{kT}\frac{\partial\mu}{\partial x} + C\frac{D}{kT}eEZ^* - C\frac{DQ^*}{kT^2}\frac{dT}{dx} + C\frac{D}{kT}\frac{d\sigma\Omega}{dx}$$
(1-13)

Detailed discussion on the contribution of each term will be reported in the later chapters.

Table 1-1 Melting temperature, diffusivity and diffusion mechanism for Cu, Al, Pb and SnPb solder [16].

	Melting point (°K)	Temperature ratio 373°K/Tm	Diffusivities at 100°C [373°K] (cm²/sec)	
Cu	1356	0.275	Surface $\mathbf{D}_s = 10^{-12}$	
Al	933	0.4	Grain Boundary $\mathbf{D}_{gb}$ =6x10 <sup>-11</sup>	
Pb	600	0.62	Lattice $\mathbf{D}_i$ =6x10 <sup>-13</sup>	
Eutectic SnPb	456	0.82	Lattice $\mathbf{D}_{i} = 2 \times 10^{-9} \text{ to } 2 \times 10^{-10}$	



Table 1-2 Experimental values of  $Q_A^*$  in some pure metals [34].

Q* in Pure Metals				
Metal	$H_m$ (kJ)	$H_{\nu}$ (kJ)	Q* (kJ)	
Ag	81	97	0	
Au	86	84	-25	
Al	60	63	7	
Pb	60	49	9	
Pt	132	153	65	

Hans Wever, Elektro- u. Thermo-transport in Metallen, J. A. Barth, Leipzig (1973), p. 216.



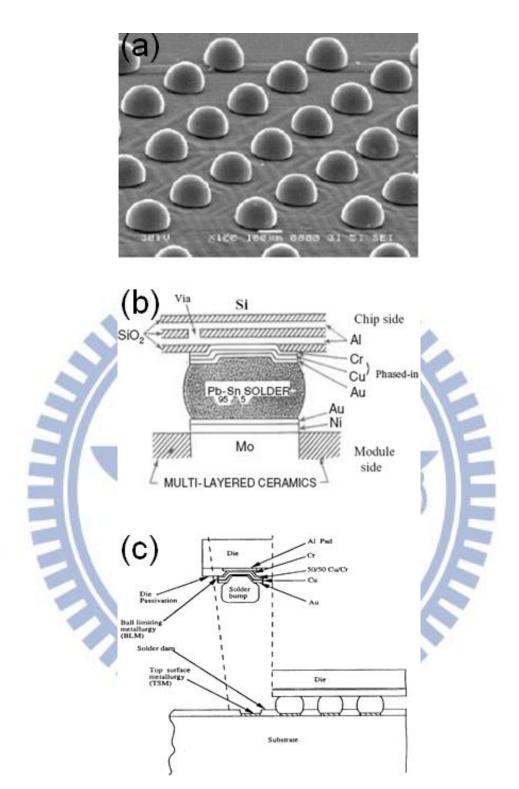
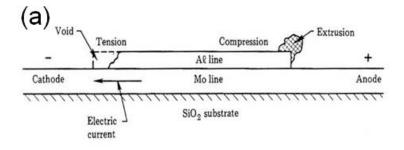


Figure 1-1 (a) A tilt-view of SEM image of arrays of solder bumps on silicon die. (b) A flip-chip solder joint to connect the chip side and the module side. (c) The chip placed upside down (flip chip), and all the joints are formed simultaneously between chip and substrate by reflow [1,5].



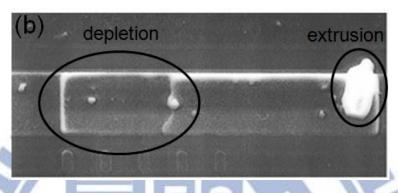


Figure 1-2 (a) Blech's pioneering electromigration sample, showing an aluminum strip deposited on a conducting TiN layer. (b) An SEM image of the morphology of a Cu strip tested for 99 h at 350 °C with current density of  $5 \times 10^5$  A/cm<sup>2</sup> [16,18].

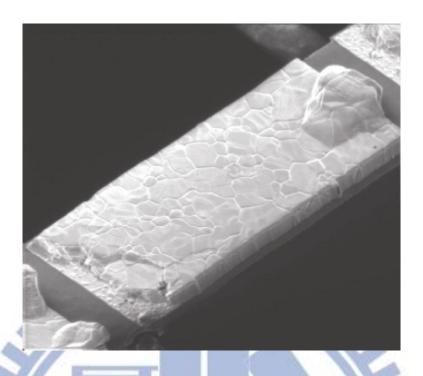
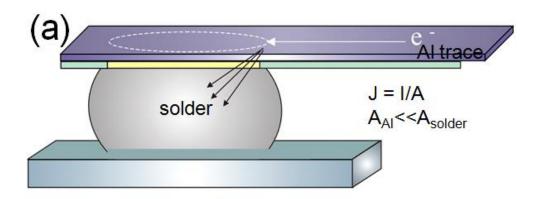


Figure 1-3 A schematic diagram of two-dimensional conductor film with grain boundary and intersection [18].



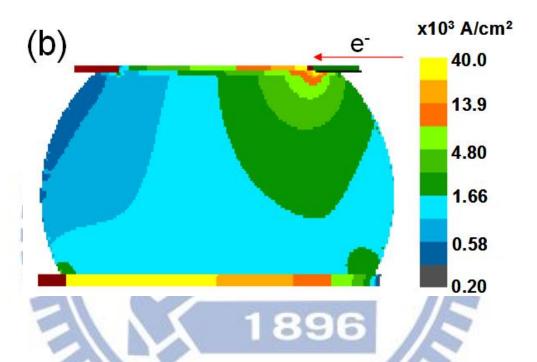


Figure 1-4 (a) The unique line to bump geometry of a flip-chip solder bump joining to a interconnect line on the chip side (top) and a conducting trace on the substrate side (bottom). (b) The two-dimensional simulation of current density distribution in a solder joint [16,42].

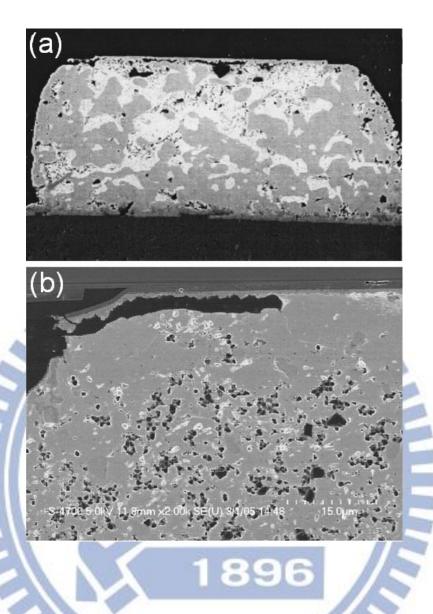


Figure 1-5 (a) The SEM image of a sequence of void formation and propagation in a flip-chip eutectic SnPb solder bump stressed at 125 °C and  $2.25 \times 10^4$  A/cm<sup>2</sup> for 40 h. (b) The SEM image of void formation in a flip-chip 95.5Sn-4.0Ag-0.5Cu solder bump stressed at 146 °C and  $3.67 \times 10^3$  A/cm<sup>2</sup> [24,25].

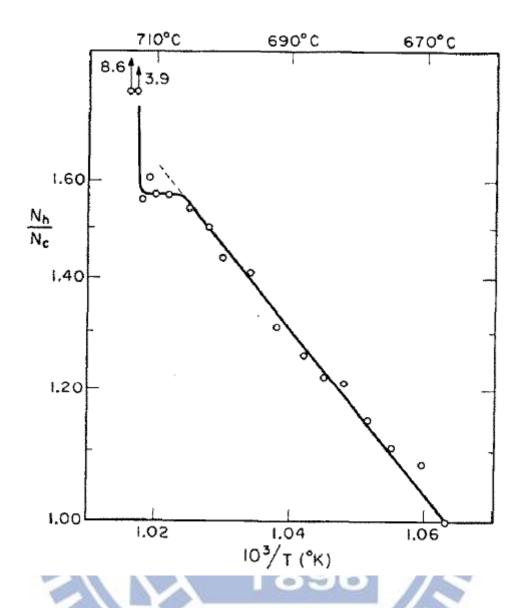
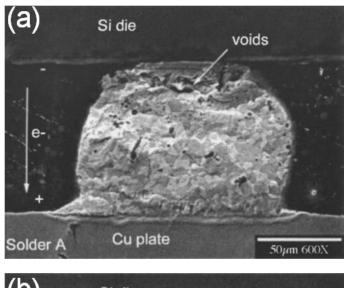


Figure 1-6 Plot of carbon content (logarithmic scale) vs. 1/T for sectioned alpha iron specimen [26].



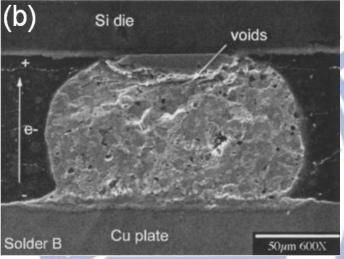


Figure 1-7 The formation of voids on the chip side and accumulation of solder on the substrate side for the solder bump with (a) downward electron flow and (b) upward electron flow [27].

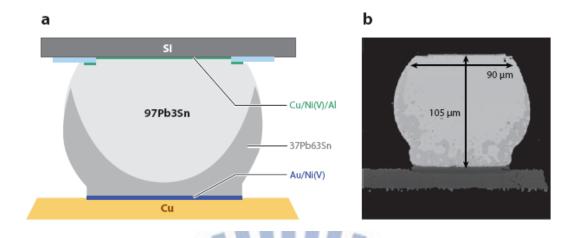
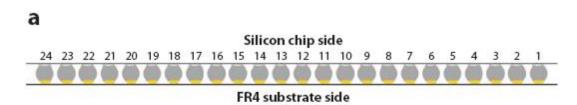


Figure 1-8 (a) A cross section of a composite 97Pb3Sn and 37Pb63Sn flip-chip solder joint. (b) The SEM image of the cross section. The darker region at the bottom is the eutectic SnPb. The brighter region is the 97Pb3Sn phase [37,42].





8 7 6 5 4 3 2 1

16 15 14 13 12 11 10 9

23 22 21 20 19 18 17

Figure 1-9 (a) A schematic diagram depicting 24 bumps on the periphery of a Si chip. Each bump has its original microstructure, as shown in Figure 1-9(b), before EM stressing. EM was conducted at  $1.6 \times 10^4$  A/cm<sup>2</sup> at 150 °C through only four pairs of bumps on the chip's periphery: pairs 6/7, 10/11, 14/15, and 18/19. (b) TM affected all the un-powered solder joints: The darker eutectic phase moved to the hot Si side [37].

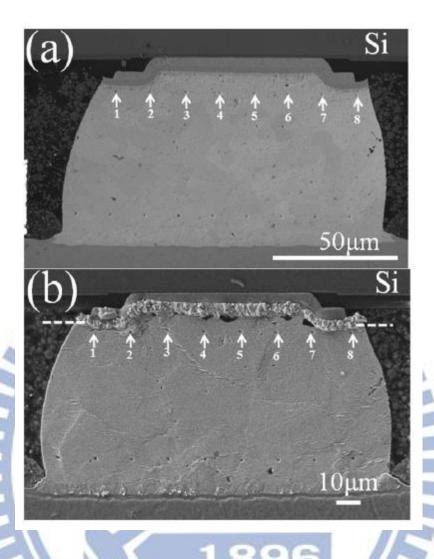


Figure 1-10 SEM images of cross-sectioned bump with markers before and after TM test at  $1.01 \times 10^4$  A /cm<sup>2</sup> and 100 °C. (a) Before TM, and (b) After 800 h of the TM test. The markers moved toward the substrate side [38].

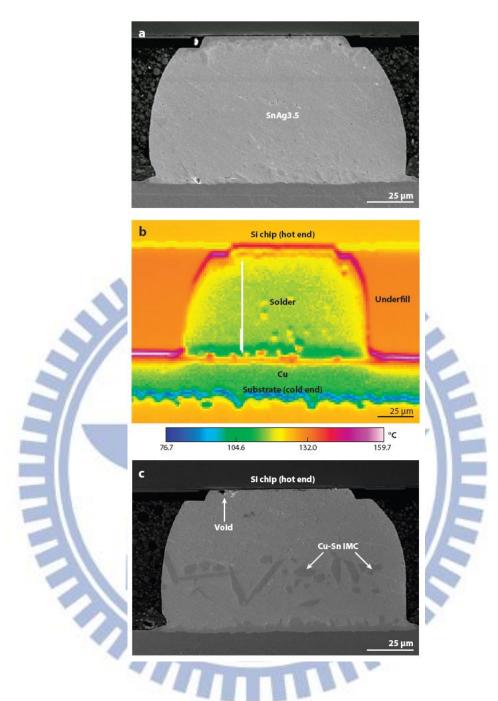


Figure 1-11 (a) Cross-sectional SEM images representing the microstructure for an un-powered bump before a TM test. (b) Temperature distribution measured by an infrared microscope when the neighboring bumps were stressed by 0.55A at 150 °C. The built-in thermal gradient was 1143 °C/cm across the solder bump. (c) After the TM test for 60 h. The Cu UBM was dissolved [42].

Chapter 2 Influence of Cu column UBMs on current crowding and Joule heating effects of electromigration in flip-chip solder joints

### 2.1 Introduction

For high-density packaging, the application of flip-chip solder joints has become the most important technology in the microelectronic industry [16]. To accommodate the performance requirement of portable devices, the number of input/output (I/O) continues to increase and the size of the joints continues to shrink. This trend has been accounted for the increase in current density and temperature rise in solder joints, and also known as the current crowding effect and Joule heating effect, respectively. Accordingly, these two effects cause serious reliability issues in flip-chip solder joints such as electromigration and thermomigration [42].

Several studies about electromigration of flip-chip solder joints have been reported [24,29,33,35,43-46]. Current crowding especially has strong effect at the entrance spot of the Al trace into the solder joint, thus the main factor responsible for the failure near the chip/anode side in most solder joints [24,44]. On the other hand, Joule heating effect also occurs during accelerated electromigration tests [29,33,35,45,46]. The temperature increase due to Joule heating effect may be over 30

°C when a solder bump is stressed by a 1.0 A current [33,35,44]. Therefore, Cu column UBM, a structure with a thick UBM, was developed to alleviate both the current crowding and Joule heating effect in flip-chip solder joints under normal operating conditions [47]. The operating temperature may affect the MTTF significantly, as depicted by Black's equation [32]:

$$MTTF = A \frac{1}{i^n} exp\left(\frac{Q}{kT}\right)$$
 (2-1)

where A is a constant, j is the current density in amperes per square centimeter, n is a model parameter for current density, Q is the activation energy, k is Boltzmann's constant, and T is the average bump temperature in degrees Kelvin.

Only few studies have been reported on the EM failure mechanism for solder joints with Cu column UBMs [48-50]. Nah *et al.* reported electromigration in flip-chip solder joints with 50-µm thick Cu columns and they found that the Cu columns can relieved the current crowding effect in solder [48]. Lai *et al.* investigated the MTTF and failure mechanism of electromigration in solder joints with 62-µm thick Cu columns, and they found the MTTF of the joints was enhanced by the thick Cu columns [49]. Xu *et al.* reported that electromigration accelerated the consumption rate of the Cu columns and transformed almost the entire solder into IMCs [50]. However, no study addresses the Joule heating effect of the solder joints with Cu UBMs. In this study, we investigate EM failures in the solder bumps with 64-µm thick

Cu column UBMs. Electromigration tests were also performed in solder joints with 2-µm thick Ni UBMs for comparison. The wiring circuits are the same for both sets of solder joints. Therefore, this study provides a direct comparison on the failure mode and thermo-electrical characteristics between regular solder joints and the solder joints with Cu column UBMs. MAN

## 2.2 Experimental procedure

In order to investigate the influence of Cu columns on current crowding and Joule heating effects, two types of flip chip solder joints were tested: one type has traditional solder joints with 2-um-thick Ni UBMs and one type has an addition of 64-µm-thick Cu column UBMs followed by a coated layer of 4-µm-thick Ni layer.

The test vehicles were  $13.5 \times 13.5 \times 1.39$  mm flip-chip packages, which involve a  $3.8 \times 3.8 \times 0.73$  mm silicon chip interconnected to a substrate. The pitch between adjacent solder joints was 270 µm. The diameter of UBM opening and passivation opening were 110 µm and 90 µm, respectively. Printed solder of Sn-2.6Ag and Sn-3.0Ag-0.5Cu solder were formed on the chip side. The substrate pad metallization features the solder on pad (SOP) surface treatment, i.e., with printed Sn-3.0Ag-0.5Cu pre-solder on the Cu pad surface. The printed solder and the SOP were then reflowed together to become lead-free solder bumps as schematically shown in Figures 2-1(a)

and 2-1(b). For electromigration tests, the stressing condition was  $2.16 \times 10^4$  A/cm<sup>2</sup> at 150 °C.

Microstructure and composition were examined by a JEOL 6500 field-emission SEM and EDS, respectively. The IMC of (Cu,Ni)<sub>6</sub>Sn<sub>5</sub> was formed at the interface of the Ni layer and the solder on the chip side while Cu<sub>6</sub>Sn<sub>5</sub> without Ni dissolution was formed at the interface of the solder and the Cu metallization layer on the substrate side. In addition, Ag<sub>3</sub>Sn IMCs were formed dispersedly in the solder bumps.

To investigate the Joule heating issue during current stressing, infrared (IR) microscopy was employed. Solder joints are completely enclosed by a Si chip, underfill, and a polymer substrate so it is difficult to examine the temperature inside solder joints directly. To overcome this difficulty, samples were polished laterally close to a point near the centers, and the temperature distribution inside the solder bump was measured directly by an IR microscope at various stressing conditions. Prior to current stressing, the emissivity of the specimen was calibrated at 100 °C. After calibration, solder joints were powered by a desired current. Temperature measurement was then performed to record the temperature map distribution at a constant rate. The temperatures in the solder joints were mapped by a QFI thermal infrared microscope, which has 0.1 °C temperature resolution and 2-μm spatial resolution.

#### 2.3 Simulation

Three-dimensional (3D) finite element analysis was employed to simulate the current density distribution in the solder joints. The model included two solder joints, an Al trace, and two Cu lines as shown in Figure 2-2, and the direction of the electron flow was shown by two of the arrows. The dimensions of the Al trace, pad opening, and the Cu line were identical to the real flip-chip samples. The IMCs formed between the UBM and the solder were also considered in the simulation models. Layered IMCs of Cu<sub>6</sub>Sn<sub>5</sub> were used in this simulation to avoid difficulty in mesh. The resistivity values of the materials used in the simulation are listed in Table 2-1. The resistivity of Sn-2.6Ag cannot be found in literature. Thus, we adopted the resistivity of Sn-3.0Ag-0.5Cu for the solder, which should be very close to the resistivity of Sn-2.6Ag. The model used in this study was SOLID5 8-node hexahedral coupled field element using ANSYS simulation software.

## 2.4 Results and discussion

#### 2.4.1 Electromigration failure site and failure mechanism change

The case without a Cu column UBM is presented here first. Figure 2-3(a) illustrates the cross-sectional SEM image of a solder bump with a Ni UBM before EM

tests. Figures 2-3(b) and 2-3(d) show the cross-sectional SEM images of solder bumps with Ni UBMs after upward and downward current stressing of  $2.16 \times 10^4$  A/cm<sup>2</sup> at 150 °C for 42.7 h, respectively. The current density was calculated based on the area of passivation opening on the chip side. Open failure occurred after 42.7 h of current stressing, and the damage in the Al trace between two solder bumps can be observed by IR microscopy. When the direction of electron flow was from the substrate side to the chip side as shown in Figure 2-3(b), some of the Cu metallization layer on the substrate side was consumed and reacted with solder to form Cu<sub>6</sub>Sn<sub>5</sub> IMCs. A slight amount of Cu<sub>6</sub>Sn<sub>5</sub> IMCs in the solder bump near the substrate side was aligned with the direction of electron flow because of electromigration effect in the solder joint. A crack formed along the chip/solder interface, which may be attributed to polishing during sample preparation for cross-sectional SEM observation. Additionally, some voids were observed in the Al trace on the chip side, as labeled in Figure 2-3(b). Some of voids were filled with Sn atoms. Figure 2-3(c) shows the EDS analysis for the location A in Figure 3(b), and the results indicated the element there was almost pure Sn. We will discuss this interesting point later. When the direction of electron flow was from the chip side to the substrate side as shown in Figure 2-3(d), the solder melted because of serious Joule heating effect. Furthermore, underfill layer was also damaged. However, the EM failure mode of the solder joints with Cu columns is quite

different. Figure 2-4(a) shows the cross-sectional SEM image of a solder bump with a Cu column UBM before EM tests. Figures 2-4(b) and 2-4(c) show the cross-sectional SEM images of solder bumps with Cu column UBMs after upward and downward current stressing of  $2.16 \times 10^4$  A/cm<sup>2</sup> at 150 °C for 286.5 h, respectively. During this period of current stressing time, the total resistance, which includes two solder joints and Al trace, is raised by 50 m $\Omega$  from 145 m $\Omega$  to 195 m $\Omega$ . When the direction of electron flow was from the substrate side to the chip side as shown in figure 2-4(b), voids of about 84.7 µm long can be observed clearly at the interface of Cu<sub>6</sub>Sn<sub>5</sub> IMCs and the solder on the substrate side. The voids in the middle of solder may be attributed to reflow process. This crack was the main reason of resistance increase during the failure. Similar to the results in the solder joint with a 2-µm Ni UBM in Figure 2-3(b), extensive dissolution of Cu layer on the substrate side took place, resulting in the massive formation of the Cu-Sn IMCs in the solder. Yet, there was no voids found in the substrate side in Figure 2-3(b). Ke et al. reported two failure mechanisms may occur in solder joints with Cu UBM: void formation and Cu dissolution [51]. It is not clear at this moment that why voids did not form in the solder joints in Figure 2-3(b).

When the direction of electron flow was from the chip side to the substrate side as shown in figure 2-4(c), the IMCs at the interface of the Ni layer and the solder

became thinner whereas the IMCs at the interface of the solder and the Cu metallization layer on the substrate side became thicker because of the polarity effect. Void of about 28 µm long was formed at the top-right-hand corner in the solder bump, and some Kirkendall voids can be observed at the interface of Cu<sub>3</sub>Sn IMCs and the Cu metallization layer on the substrate side. The Cu column and the Ni layer beneath remained intact within our experimental time frame.

#### 2.4.2 Current crowding effect

Current crowding effect plays a crucial role in the electromigration failure of solder joints. Since the current density in the Al trace is typically one or two orders in magnitude larger than that in the solder, current crowding occurs at the entrance point of the Al trace into the solder joint. Figure 2-5 depicts the 3D simulation of the current density distribution in the solder bump with Ni UBMs. The applied current was 1.5 A from the chip side to the substrate side, which resulted in a current density of  $1.54 \times 10^6$  A/cm<sup>2</sup> in the Al trace. The calculated average current density was  $2.16 \times 10^4$  A/cm<sup>2</sup> based on the area of passivation opening on the chip side. However, due to the current crowding effect, the maximum current density inside the solder bump is as high as  $7.8 \times 10^4$  A/cm<sup>2</sup> as shown in Figure 2-5.

With a Cu column UBM, a more uniform distribution of current density was

obtained in the solder bump as shown in Figures 2-6(a) and 2-6(b). Same as in Figure 2-5, the applied current was 1.5 A from the chip side to the substrate side. The maximum current density in the Cu column is  $1.0 \times 10^6$  A/cm<sup>2</sup>. It can be seen that the current crowding effect still occurs in the Cu column UBM near the entrance of the Al trace into the solder joint. However, since Cu has a much higher melting point than the SnAg solder (Cu: 1084 °C; SnAg: 221 °C), there was little EM damage in Cu in the present stressing condition. The Cu column UBM is thick enough, therefore the solder is kept away from the current crowding region, and the maximum current density in the solder bump dramatically decreases to  $4.0 \times 10^4$  A/cm<sup>2</sup>, which is only 51% of the maximum current density inside the solder bump with the 2-um Ni UBM. In other words, the current flow spreads out and becomes more uniform before reaching the solder bump when Cu column UBM is utilized. As a result, instead of locating on the chip side, the current crowding region in the solder bump with Cu column UBMs is actually located on the substrate side. This result agrees with the phenomenon observed in Figure 2-3(c) and Figure 2-4(b). electromigration-induced damage position in the solder bump moved from the chip side to the substrate side because of the existence of Cu column UBMs.

### 2.4.3 Joule heating effect

The existence of Cu column UBMs also has influence on the Joule heating effect in the solder bump. Current stressing was carried out at the temperature of 100 °C on a hotplate. Figure 2-7 shows the temperature increases in solders with 2-µm Ni UBMs and Cu column UBMs during current stressing as a function of applied currents and current densities. Current stress was applied to solder joints with the current density in the range of  $2.88 \times 10^3$  A/cm<sup>2</sup> to  $2.30 \times 10^4$  A/cm<sup>2</sup> in the passivation opening. Figures 2-8(a) and 2-8(b) show the temperature distribution of the cross-sectioned solder bump with Ni UBMs and Cu column UBMs during current stressing of  $2.30 \times 10^4$ A/cm<sup>2</sup> at 100 °C, respectively. The temperature scale bars are shown at the bottom of figures. The average temperature increases were 17.9 °C and 14.4 °C in the solder bump with Ni UBMs and Cu column UBMs, respectively. In this study, the mean temperature was determined by averaging the values of 1000 pixels surrounding an approximately  $65 \times 40 \ \mu \text{m}^2$  rectangle area in the center of the solder bump. Under the same current density, the alleviation of current crowding by the Cu column UBM consequently decreased the temperature rise in the solder bump. It is also known that Al trace under current stressing is a stable heating source, and the heat generated by the Joule heating of Al trace should always flow from a high temperature region toward a low temperature region. We have noticed, however, as shown in Figure 2-8(b) for the case with a Cu column UBM, that the temperature increase in the Cu column UBM seems to be lower than that in the solder bump. The seemingly contradicting result actually comes from the difference between "thermal gradients" and "radiance gradient." Because Cu and solder's surface characteristic are different, what was measured does not represent the real temperature difference between Cu column UBM and the solder joint. Nevertheless, in general, the temperature increase in various solder bumps can still been compared, since the emissivity of solder is consistent.

The Cu column also decreases the thermal gradient in the solder during high-current stressing. Figure 2-9(a) shows the temperature profile along the red line  $\overline{AB}$  in Figure 2-8(a). The temperature difference is 6.0 °C across the line and the calculated thermal gradient is 600 °C/cm. Here, the thermal gradient is defined here as the temperature difference between the two ends of the line divided by the length of the line. However, there is no obvious thermal gradient in the solder joint with the Cu column under the same stressing condition. Figure 2-9(b) presents the temperature profile along the red line  $\overline{CD}$  in Figure 2-8(b). No obvious temperature difference is found across the line  $\overline{CD}$ . Therefore, thermomigration may be relieved in the joints with Cu column.

#### 2.4.4 Mean time to failure

The solder joints with a Cu column UBM have a longer failure time than the ones with a 2-µm Ni UBM, because the Cu column helps reduce current density in solder and Joule heating effect. As described by the Black's equation in Eq. (2-1), the MTTF can be prolonged when the current density and the temperature in solder can be reduced, provided the activation energy remains the same. In general, the value nin Eq. (2-1) is close to 2, which means the MTTF will double if the current density in solder reduces to half of its original value [33]. As shown in Figure 2-5, the maximum current density inside the solder bump with a 2- $\mu$ m Ni UBM is as high as  $7.8 \times 10^4$ A/cm<sup>2</sup>; whereas the maximum current density in the solder bump with a 64-μm Cu column dramatically decreases to  $4.0 \times 10^4$  A/cm<sup>2</sup>, which is only 51% of the maximum current density inside the solder bump with the 2-µm Ni UBM. Therefore, the lower current density renders a longer MTTF of the solder bump with the Cu column. In addition, the MTTF increase exponentially when the real temperature in solder joints decrease. The results in Figures 2-8 indicate that the Cu column reduces the Joule heating effect. Thus, the real temperature in the solder bump with the Cu column appears lower than that in the solder joint with a 2-µm Ni UBM, which also increases the MTTF of the solder joint with the Cu column. For the solder joints with 2-µm Ni UBMs, open failure took place at 42.7 h when they were subjected to a

current density of  $2.16 \times 10^4$  A/cm<sup>2</sup> at 150 °C as shown in Figure 2-3. However, for the solder joint with the Cu column, the resistance increases only 50 m $\Omega$  after 286.5 h at the same stressing condition. The thick Cu column keeps the solder away from the region with a high current density. In addition, it possesses a high thermal conductivity, so the heat generated by Joule heating effect can be conducted away efficiently. Moreover, the thick Cu column also keeps the solder away from the hot-spot region [52], therefore, the temperature in the solder is reduced.

The voids in the Al trace in Figure 2-3(b) were caused by electromigration. It is reported that electromigration in the Al trace also occurs when the current density is larger than  $1.0 \times 10^6$  A/cm<sup>2</sup> at 150 °C [53,54]. In the present study, the current density is  $1.54 \times 10^6$  A/cm<sup>2</sup> in the Al trace and thus voids may form in the cathode end of the Al trace, as labeled in the figure. Once voids formed in the Al trace, the Sn atoms may -51 HOW. be pushed into the voids by the upward electron flow.

## 2.5 Summary

Electromigration-induced failures in SnAg solder bumps with and without Cu column UBMs have been investigated under the current density of  $2.16 \times 10^4$  A/cm<sup>2</sup> at 150 °C. When SnAg solder bumps with 2- $\mu$ m Ni UBMs were stressed at  $2.16 \times 10^4$ A/cm<sup>2</sup>, open failure occurred in the bump that had electron flow direction from the chip side to the substrate side. However, when Sn-3.0Ag-0.5Cu solder bumps with Cu column UBMs were stressed at  $2.16 \times 10^4$  A/cm², cracks formed along the interface of Cu<sub>6</sub>Sn<sub>5</sub> IMCs and the solder on the substrate side. The three-dimensional simulation on current density distribution supports the contention that the current crowding effect was responsible for the failure on both the chip and the substrate side for the two kinds of solder bumps. On the other hand, being confirmed by IR microscopy, the alleviation of current crowding by the Cu column UBMs also helped decrease the Joule heating effect in the solder bump during current stressing. Therefore, the solder joints with Cu column UBMs have a higher EM resistance than the traditional flip-chip solder joints.



Table 2-1 The properties of materials used in the simulation model.

Mariala	Resistivity at 20°C			
Materials	(μΩ-cm)			
Al	3.2			
Cu	1.7			
Ni	6.8			
Cu <sub>6</sub> Sn <sub>5</sub>	17.5			
Sn-3.0Ag-0.5Cu solder	12.3			

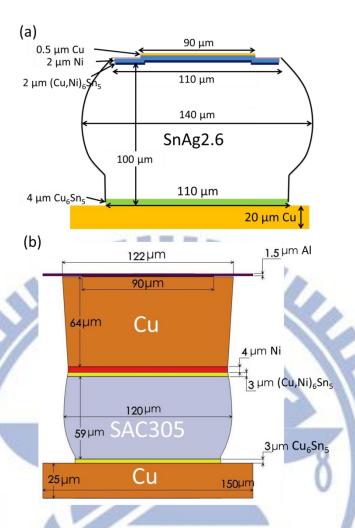


Figure 2-1 Schematics of the flip-chip solder joints with (a) a Ni UBM and (b) a Cu column UBM in this study.

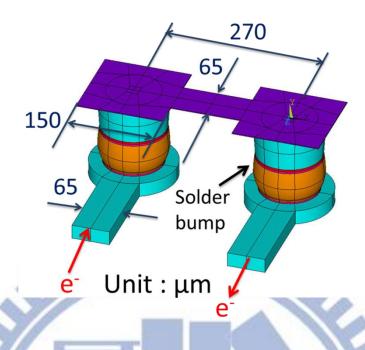


Figure 2-2 The simulation model for one pair of the flip-chip solder joints. The arrows show the direction of the electron flow.

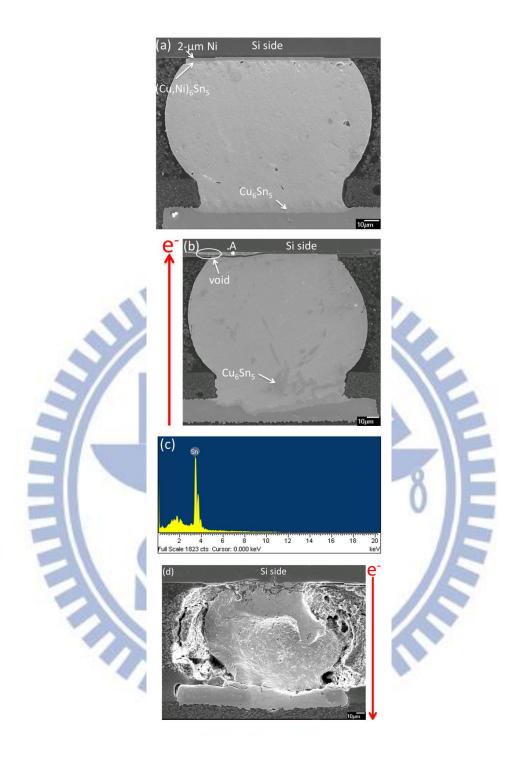


Figure 2-3 Cross-sectional SEM images of a solder bump with a 2- $\mu$ m Ni UBM stressed at 2.16  $\times$  10<sup>4</sup> A/cm<sup>2</sup> at 150 °C for (a) 0 h, (b) 42.7 h with upward electron flow, (c) EDS analysis at the point A in (b), and (d) 42.7 h with downward electron flow.

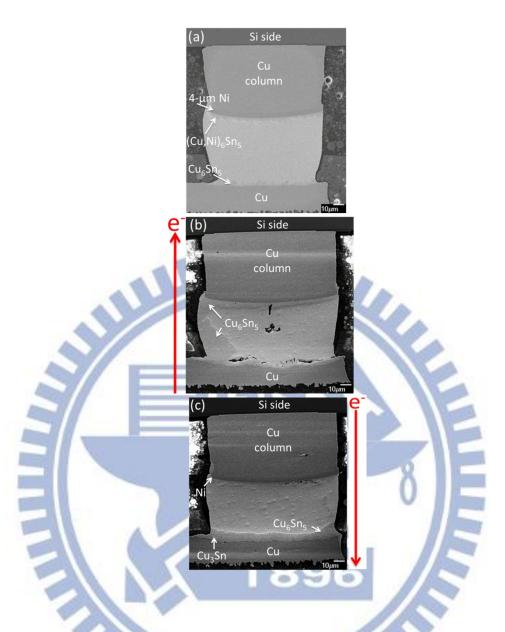


Figure 2-4 Cross-sectional SEM images of a solder bump with a Cu column UBM stressed at  $2.16 \times 10^4$  A/cm<sup>2</sup> at 150 °C for (a) 0 h, (b) 286.5 h with upward electron flow, and (c) 286.5 h with downward electron flow.

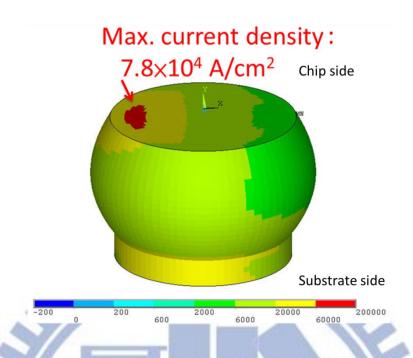


Figure 2-5 Simulation results for current density distribution in the solder bump with a 2- $\mu$ m Ni UBM when powered by 1.5 A.



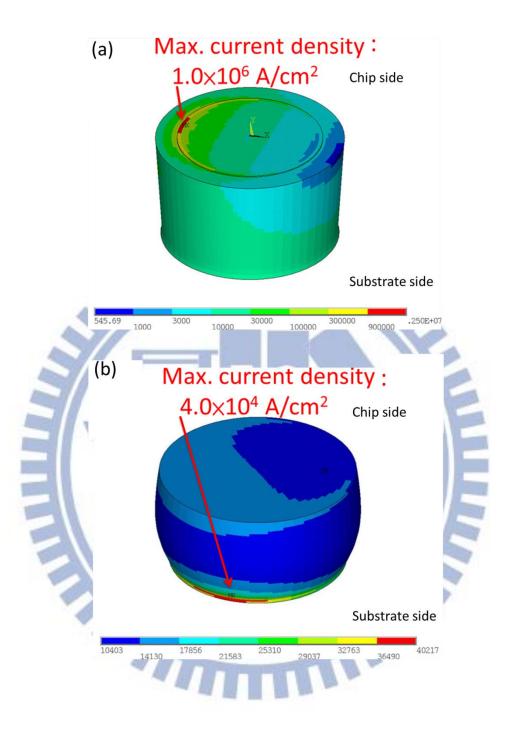


Figure 2-6 Simulation results for the current density distribution in (a) the Cu column UBM and (b) the solder bump beneath when powered by 1.5 A.

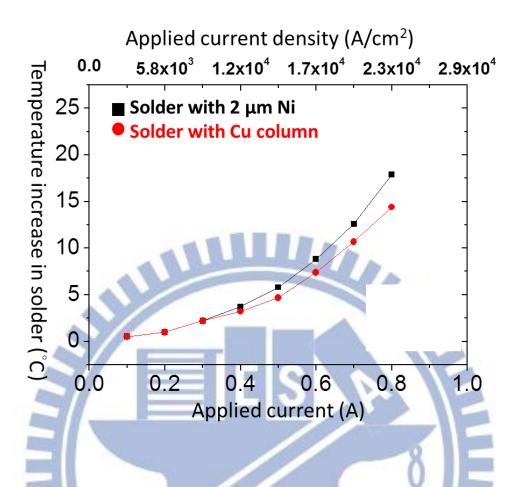


Figure 2-7 Temperature increases in solders with 2-µm Ni UBMs and Cu column UBMs during current stressing as a function of applied currents and current density.

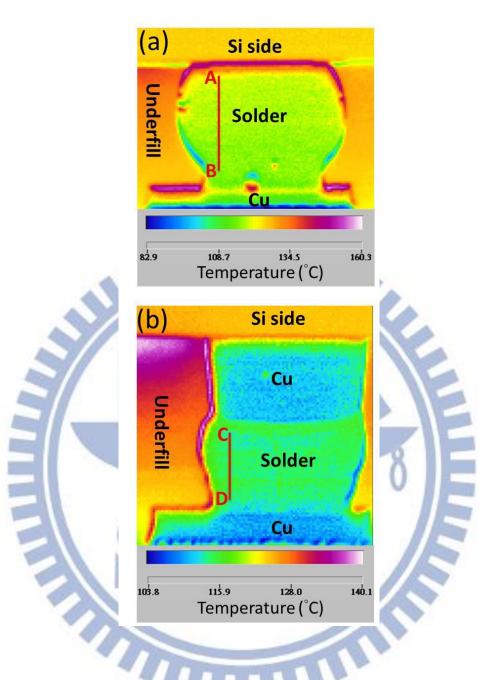


Figure 2-8 IR images showing the temperature distribution in solder bumps with (a) a 2- $\mu$ m Ni UBM and (b) a Cu column UBM during current stressing of  $2.30 \times 10^4$  A/cm² at 100 °C.

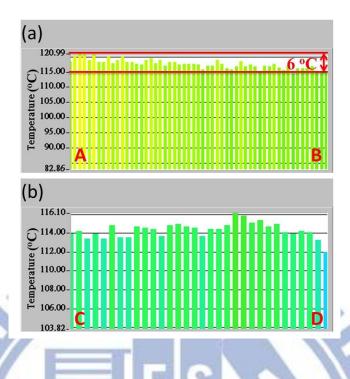


Figure 2-9 (a) The temperature profile along the  $\overline{AB}$  line in Figure 2-8(a). (b) The temperature profile along the  $\overline{CD}$  line in Figure 2-8(b).

# Chapter 3 Chemical potential-driven Sn atoms refill against electron wind force during current stressing

#### 3.1 Introduction

For high-density packaging, the application of flip-chip solder joints has become the most important technology in the microelectronic industry [16]. To accommodate the performance requirement of portable devices, the number of input/output (I/O) continues to increase and the size of the joints continues to shrink. This trend has been accounted for the increase in current density and temperature rise in solder joints. Accordingly, these two effects cause serious reliability issues in flip-chip solder joints such as electromigration and thermomigration [42].

Cu and Ni serve as the most two popular UBM materials. Cu has a good wettability and a high reaction rate with solders [55]. On the other hand, a few microns thick Ni layer UBM has been coated at the surface of the Cu as a diffusion barrier because of its slow reaction rate with solders [56-58]. Several studies about the two major EM failure mechanisms have been reported: void formation [16,44,59-61] and UBM consumption [16,50,61]. For the UBM consumption failure mechanism, little voids can be observed at the interface between the solder and the IMC layer on the cathode side. In the literature, only a few studies have been reported regarding the

Sn atoms migration to the chip side due to the TM force to the hot end [38,62]. However, the Sn atoms refill to the cathode side against the electron wind force requires a systematic study.

In this study, we investigate the EM failure mechanisms in SnAg solder joints with 5- $\mu$ m-Cu/3- $\mu$ m-Ni UBM on the chip side. It is found that both the void formation and the UBM consumption mechanisms occur at the stressing conditions without a thermal gradient in the solder bump. We also propose a model considering the Sn EM fluxes toward the anode side as well as the chemical potential-driven fluxes toward the cathode side, and it is able to successfully explain the experimental results.

#### 3.2 Experimental procedure

In order to investigate the EM failure mechanisms, a layout of Kelvin bump probes was adopted, as illustrated schematically in Figure 3-1(a). On the chip side, a 0.3 μm Ti layer was sputtered as an adhesion/diffusion-barrier layer between the UBM and the Al trace which connect four bumps together labeled as b1 to b4. The solder joints comprised eutectic SnAg solder bumps with electroplated 5-μm-Cu/3-μm-Ni UBM as shown in Figure 3-1(b). The bump height was 50 μm, and the diameter of the passivation opening as well as the UBM opening were 85 μm and 120 μm, respectively. The IMC of Ni<sub>3</sub>Sn<sub>4</sub> was formed at both the top and the bottom

interfaces. The dimension of Al trace on the chip side was 100  $\mu$ m wide and 1.5  $\mu$ m thick, while the dimension of the Cu lines on the substrate side was 100  $\mu$ m wide and 30  $\mu$ m thick. On the substrate side, six Cu nodes were fabricated and labeled as n1 to n6. By the nodes n3 to n6, the resistance of the bump b3 was monitored.

Electromigration tests were performed at the current densities of  $1.15 \times 10^4$  A/cm<sup>2</sup> at 100 °C and  $5.3 \times 10^3$  A/cm<sup>2</sup> at 170 °C on a hotplate. The calculated current densities were based on the UBM opening. As the measured bump resistance increased 100% of its original value, the current stressing was terminated. Then the EM failure modes were examined by an SEM, and the compositional analysis was performed by EDS.

Infrared microscopy was employed to measure the temperature distribution in the solder bump during current stressing. Solder joints are completely enclosed by a Si chip, underfill, and a polymer substrate so it is difficult to examine the temperature inside solder joints directly. To overcome this difficulty, samples were polished laterally close to a point near the centers, and the temperature distribution inside the solder bump was measured directly by an IR microscope at various stressing conditions. Prior to current stressing, the emissivity of the specimen was calibrated at 100 °C. After calibration, solder joints were powered by a desired current. Temperature measurement was then performed to record the temperature map

distribution at a constant rate. The temperatures in the solder joints were mapped by a QFI thermal infrared microscope, which has 0.1 °C temperature resolution and 2-μm spatial resolution. The joule heating in the solder bumps for the current densities of 1.15 × 10<sup>4</sup> A/cm<sup>2</sup> and 5.3 × 10<sup>3</sup> A/cm<sup>2</sup> were 33.2 °C and 5.3 °C, respectively. Consequently, the real temperatures considering the joule heating were 133.2 °C and 175.3 °C, respectively. In the following text, we will refer the real temperature as the stressing temperature. However, no thermal gradient can be observed in the solder bumps for both the two current densities. That is, no TM occurred in these two stressing conditions.

#### 3.3 Results and discussion

#### 3.3.1 Electromigration behaviors at various stressing conditions

The EM failure mode was attributed to void formation at the interface of the IMC and the solder on the chip side when the solder joint was stressed by  $1.15 \times 10^4$  A/cm<sup>2</sup> at 133.2 °C. Figure 3-2(a) shows the cross-sectional SEM images of the solder bump after downward electron flow stressing of  $1.15 \times 10^4$  A/cm<sup>2</sup> at 133.2 °C for 474.7 h. The bump resistance increased 100% of its original value after 474.7 h. The voids first formed at the interface of the IMC and the solder, and then propagated along the interface, which is known as the pancake-type voids [24,25]. The results

indicated that the Sn atoms migrated to the substrate side due to the electron wind force and vacancies accumulated at the interface.

However, the failure mode switched to UBM dissolution on the chip side when the solder joint was stressed by 5.3 × 10<sup>3</sup> A/cm<sup>2</sup> at 175.3 °C. Figure 3-2(b) presents the cross-sectional SEM images of the solder bump after downward electron flow stressing of 5.3 × 10<sup>3</sup> A/cm<sup>2</sup> at 175.3 °C for 83.2 h. The bump resistance reached to 2 times of its initial value after only 83.2 h. Most of the Ni UBM and even the Cu UBM was consumed obviously, and there were (Cu,Ni)<sub>6</sub>Sn<sub>5</sub> IMCs formed in the solder bump. However, it is intriguing that no voids were observed at the interface of the IMC and the solder. The results indicated that the dissolution of the Ni and Cu UBMs served as the main failure mode at this stressing condition.

### 1896

#### 3.3.2 Theoretical analysis on flux divergence at the IMC/solder interface

To explain the failure mode transition, we develop a model to calculate the EM flux and chemical potential flux of Sn at the IMC/solder interface. Figure 3-3 illustrates schematic drawing of the solder joint subject to a downward electron flow.  $J_{Sn\ in\ Sn}$  stands for the downward EM flux of Sn atoms in the solder, while  $J_{Sn\ in\ IMC}$  represents the upward chemical potential flux of Sn atoms in the IMCs against the electron wind force. Considering the flux divergence at the interface of the solder and

the IMC, when the downward Sn flux leaving the interface is larger, voids will form at the interface. Nevertheless, when the upward Sn flux is larger, the interfacial IMC will grow and no voids will form at the interface. In the following, we will calculate the two fluxes quantitatively using the available data in literature. Electromigration flux,  $J_{EM}$  is typically expressed as [63]

$$J_{EM} = C \frac{D}{RT} Z^* e \rho j \tag{3-1}$$

where C is concentration, D is diffusivity, T is temperature, R is gas constant,  $Z^*$  is effective charge number, e is electron charge,  $\rho$  is resistivity, and j is current density. In solder near the IMC, Sn will migrate toward the substrate side by the electron wind force. The Sn EM flux is

$$J_{Snin\,Sn} = C_{Snin\,Sn} \frac{D_{Snin\,Sn}}{RT} Z_{Snin\,Sn}^* e \rho_{Sn} j \tag{3-2}$$

The  $Z^*$  of Sn is 9.6 [64]. The resistivity of Sn is  $1.23 \times 10^{-7} \,\Omega \cdot m$ , and the self-diffusivity of Sn is [65]

$$D_{Snin Sn} = 1.2 \times 10^{-9} \times \exp\left(-\frac{43890}{RT}\right) \left(\text{m}^2/\text{s}\right)$$
 (3-3)

Thus

$$J_{Snin\,Sn} = \left[ 1.03 \times 10^{-6} \times \frac{1}{T} \times \exp\left(-\frac{43890}{RT}\right) \right] j \tag{3-4}$$

At the IMC/solder interface, the Sn atoms in the solder also diffuse upward to react with the UBM to form IMCs due to the chemical potential force. We will take the IMC growth rate constants and transfer them into the required Sn chemical

potential fluxes. The Sn chemical potential flux is

$$J_{Snin\,IMC} = \frac{k \times A \times V_{Sn} \times d_{Sn}}{V_{IMC} \times M_{Sn} \times A \times t}$$
(3-5)

where k is IMC growth rate constant, A is area,  $V_{Sn}$  is molar volume of Sn,  $d_{Sn}$  is density of Sn,  $V_{IMC}$  is molar volume of IMC,  $M_{Sn}$  is atomic weight of Sn, and t is time. The IMC growth rate constants for Ni<sub>3</sub>Sn<sub>4</sub> IMC in a Sn-Ag-Ni system are 0.0088 and 0.1178 μm/h<sup>0.5</sup> at 125 °C and 175 °C, respectively [66]. In addition, the IMC growth rate constant for  $Cu_6Sn_5$  IMC in a Sn-Cu-Ni system is 0.2232  $\mu$ m/h<sup>0.5</sup> at 150 °C [67]. With these parameters, we can plot the downward Sn EM flux and the upward Sn chemical flux as a function of time. Figure 3-4(a) shows the curves for the Sn EM and chemical potential fluxes stressed by  $1.15 \times 10^4$  A/cm<sup>2</sup> at 125 °C as a function of time. Electromigration flux driven by a given current density at a constant temperature is independent of time, so it appears a horizontal line in the plot as a function of time. However, chemical potential flux at a constant temperature is inverse proportional to the square root of time as described in Eq. (3-5), so the curve behaves like a hyperbolic curve in the plot. The Sn EM flux is always larger than the chemical potential flux in the 474.7 h stressing time, which agrees well with the void formation failure mode as shown in Figure 3-2(a).

On the contrary, chemical potential force may increase as the temperature increases because the metallurgical reaction rate is higher at high temperatures. Figure

3-4(b) shows the curves for the Sn EM and chemical potential fluxes stressed by  $5.3 \times 10^{-2}$ 10<sup>3</sup> A/cm<sup>2</sup> at 175 °C as a function of time. The chemical potential flux represents the sum of the two upward Sn fluxes to form Ni<sub>3</sub>Sn<sub>4</sub> and (Cu,Ni)<sub>6</sub>Sn<sub>5</sub> IMCs. As shown in Figure 3-2(b), both of the Ni and Cu UBMs were consumed obviously, and the original Ni<sub>3</sub>Sn<sub>4</sub> IMCs were converted to (Cu,Ni)<sub>6</sub>Sn<sub>5</sub> IMCs on the chip side. That is, the upward Sn fluxes supplied the UBMs to form Ni<sub>3</sub>Sn<sub>4</sub> and (Cu,Ni)<sub>6</sub>Sn<sub>5</sub> IMCs continuously, so the two Sn chemical potential fluxes were combined together. The results indicate that there is a cross over at the 45<sup>th</sup> h, below which the chemical potential flux is larger than the EM flux. Since the total upward atomic flow represented by the area under the chemical flux curve is larger than the downward atomic flow driven by the electron wind force in the 83.2 h stressing time, the calculated results stand for the UBM dissolution failure mode as shown in Figure 3-2(b). From the mention above, the theoretic calculation successfully explains the experimental results.

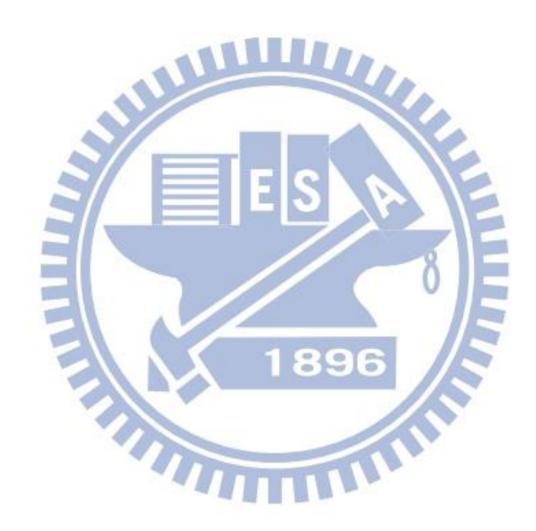
It is noteworthy that some Sn atoms refill to the cathode side against electron wind force may be attributed to back stress of EM [68,69]. The Cu, Ni, and Sn atoms migrated to the substrate side because of electron wind force. However, the solder joints were confined by the underfill, and there were no hillocks or extrusion on the substrate side to release the compressive stress on the substrate side. At the same time,

a tensile stress was developed on the chip side due to the deficiency of Cu, Ni, and Sn atoms. Therefore, a stress gradient was built up across the solder joints, which triggered the migration of Sn atoms to the original location of UBMs. On the other hand, the EM behaviors at the IMC/solder interface may be also affected by the Sn grain orientations [70]. When the electron flow direction is along the c-axis of Sn crystals, rapid depletion of the UBM dominates the EM behavior due to the fast diffusion of Cu and Ni atoms. However, so far, there is no available way to control the Sn grain orientation in a solder bump, and it deserves more study.

#### 3.4 Summary

In summary, we investigated the EM failure mechanisms in SnAg solder joints with 5-µm-Cu/3-µm-Ni UBM at various stressing conditions. It was found that both the void formation and the UBM consumption failure mechanisms occurred at the stressing conditions without a TM driving force confirmed by IR microscopy. By considering the flux divergence at the IMC/solder interface, we proposed a model to calculate the Sn EM fluxes as well as the chemical potential fluxes. When the Sn EM flux is larger, void formation at the interface was responsible for the failure. However, UBM dissolution and IMC formation dominated the failure mechanism when the Sn chemical potential flux toward the cathode side exceeded. This model successfully

explains the experimental results.



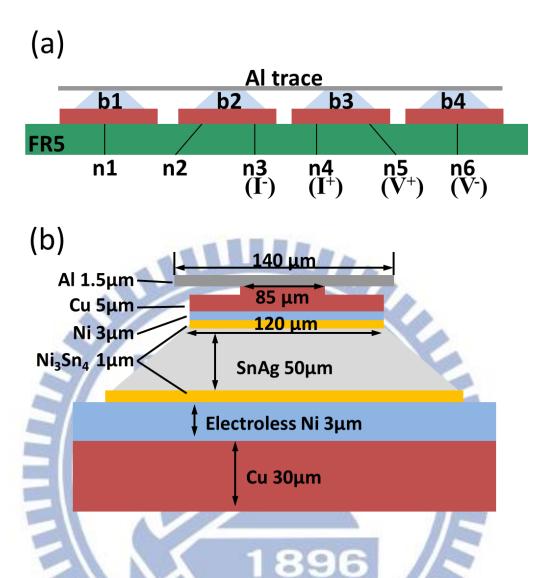


Figure 3-1 Cross-sectional schematic structure of (a) the electromigration tests layout design and Kelvin bump probe structure for measuring bump resistance and (b) the solder joint configuration used in this study.

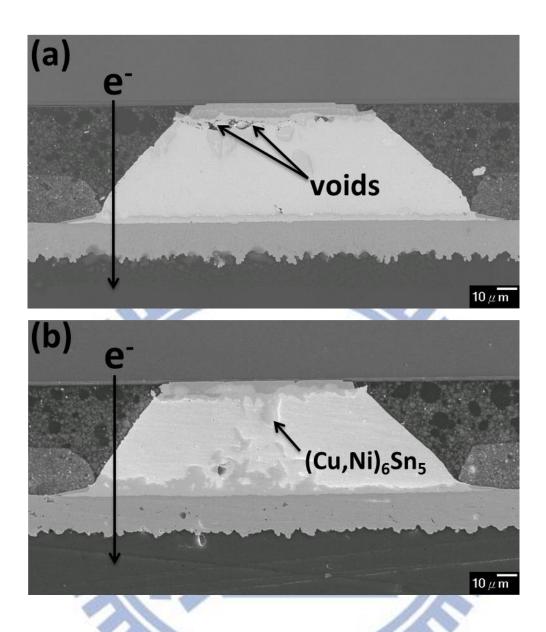


Figure 3-2 Cross-sectional SEM image showing the microstructure of the solder joint after current stressing by (a)  $1.15 \times 10^4$  A/cm<sup>2</sup> at 133.2 °C for 474.7 h and (b)  $5.3 \times 10^3$  A/cm<sup>2</sup> at 175.3 °C for 83.2 h.

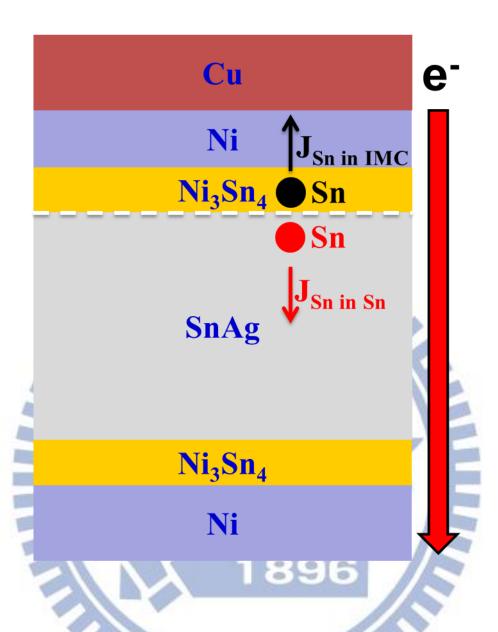


Figure 3-3 Schematic drawing of a solder joint subject to a downward electron flow.

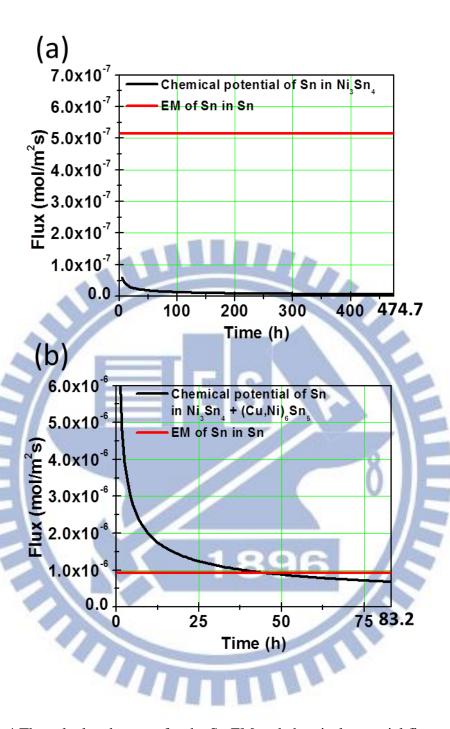


Figure 3-4 The calculated curves for the Sn EM and chemical potential fluxes stressed by (a)  $1.15 \times 10^4$  A/cm<sup>2</sup> at 125 °C and (b)  $5.3 \times 10^3$  A/cm<sup>2</sup> at 175 °C as a function of time.

Chapter 4 Stress-migration-induced anisotropic grain growth and crack propagation in eutectic microstructure under cyclic temperature annealing in flip-chip SnPb composite solder joints

Willey,

#### 4.1 Introduction

For high-density electronic packaging, the application of flip-chip solder joints has been well received in microelectronic industry [71]. High-lead (Pb) solders such as Sn5Pb95 [3,4,72-74], are presently granted immunity from the Restriction of Hazardous Substances (RoHS) requirements for their use in high-end flip-chip devices, especially in military applications. In flip-chip technology for consumer electronic products, organic substrates have replaced ceramic substrates due to the demand for less weight and low cost. However, the liquidus temperatures of high-Pb solders are over 300 °C which would damage organic substrates during reflow because of the low glass transition temperature. To overcome this difficulty, the composite solder approach was developed [13]. By using an eutectic Sn63Pb37 solder bump on the substrate side in combination with a high-Pb solder bump on the chip side, as illustrated in Figure 4-1(a), a much lower reflow temperature (slightly over the melting point of the eutectic solder) can be used without damaging the organic substrates. During reflow, the Sn63Pb37 solder melted and dissolved some of the Sn5Pb95 solder to form a joint. As shown in Figure 4-1(b), most of the eutectic phase remained on the substrate side in the solidified composite solder joint. No intermixing of the high-Pb and the eutectic occurs.

In the literature, several studies regarding the reliability issues of flip-chip SnPb composite solder joints have been reported [37,75-78]. Fatigue failure of flip-chip SnPb composite solder joints has been researched through various reliability tests [75]. Chang *et al.* investigated the intermixing of the high-Pb and the eutectic during reflow [76]. They found that the latter had a calyx shape and the height of the calyx-shape bump increased with the reflow times. This group also reported that the IMC Ni<sub>3</sub>Sn<sub>4</sub> on the chip side converted into (Cu,Ni)<sub>6</sub>Sn<sub>5</sub> after an extended aging time [77]. In addition, electromigration and thermomigration induced failure have been observed in SnPb composite solder joints [78,37].

Several investigations on stress-induced migration in Cu interconnects have been carried out [79-81]. However, no study has addressed the phenomenon of stress-induced migration in flip-chip SnPb composite solder joints. We note that temperature cycles occur in satellite operation [82]. How does cyclic thermal stress induced stress-migration affect the reliability of solder joints requires a systematic study. In this study, we investigate the evolution of microstructure in the composite

solder joint under isothermal and temperature cycle annealing. The latter has caused stress-induced growth of anisotropic Sn grains and crack formation and propagation along the Sn/Pb interfaces over the entire composite solder joint.

#### 4.2 Experimental procedure

The test vehicles were  $27 \times 27 \times 1.39$  mm flip-chip packages, which involve a  $7.62 \times 7.62 \times 0.73$  mm silicon chip interconnected to a 0.56 mm thick organic substrate by 720 solder joints. The pitch between adjacent solder joints was 270  $\mu$ m. Beneath a 3  $\mu$ m thick Ni UBM, an electroplated solder of Sn5Pb95 was reflowed at 350 °C to form a spherical high-Pb solder bump with a diameter of 95  $\mu$ m on the chip side. The substrate pad metallization featured the SOP surface treatment, i.e., with printed Sn63Pb37 eutectic solder on the Cu pad surface. The high-Pb solder bump and the SOP were then reflowed at 240 °C to become SnPb composite solder joints as shown in Figures 4-1(a) and 4-1(b).

To investigate the evolution of eutectic microstructure in flip-chip SnPb composite solder joints, the samples were subjected to either temperature cycling test (TCT) or isothermal annealing. The TCT condition was between -55 and 125 °C for 100, 500, 1500, 2160, and 14410 cycles with each cycle period of 1 h. Isothermal annealing tests at 150 °C for 100, 500, 1000, 2160 h were also applied to fresh

samples, providing a comparison of the thermo-mechanical characteristics of the different heat treatments.

Cross-sections of the samples after the TCT and the isothermal annealing test were mechanically polished, and the microstructure on the cross-sections was observed by SEM with a back-scattered electron image (BEI) detector. Moreover, the composition of the solder joints and the IMCs were examined by EDS. The IMC of Ni<sub>3</sub>Sn<sub>4</sub> was formed at the interface of the Ni UBM and the high-Pb solder on the chip side, whereas Cu<sub>6</sub>Sn<sub>5</sub> and Cu<sub>3</sub>Sn were formed at the interface of the eutectic solder and the Cu metallization layer on the substrate side. Growth rate of the IMC was quantified by calculation on the basis of image analysis software, which measured the IMC area on the cross-section and then divided by the interfacial length between the IMC and the UBM.

#### 4.3 Results and discussion

#### 4.3.1 Anisotropic Sn stripe formation in TCT

Under TCT, the formation of horizontally anisotropic Sn stripes in the composite solder joints was observed. Figures 4-2(a) and 4-2(b) show the cross-section of two solder bumps after 500 cycles of TCT. The grains of the Sn-rich phase coarsened along the horizontal direction and laid at a similar position in height, before and after

the thermal cycles. The position was at about one-third of the bump height from the Cu pad metallization layer, which was close to the necking site in the solder bump due to the pad opening definition by the solder mask at the substrate side. Also the position is close to the interface between the high-Pb and the eutectic, because the height of the eutectic solder before joining to the high-Pb is defined by the solder mask. After 1500 cycles of TCT, as demonstrated in Figures 4-3(a) and 4-3(b), the small Sn grains grew into a longer Sn stripe near the necking site in the solder bump.

Figures 4-4(a) and 4-4(b) illustrate the cross-section of two solder bumps after 14410 cycles of TCT. The anisotropic growth of the Sn stripe appears to have grown across the entire solder bump. However, cracks propagation along the horizontal Sn/Pb interfaces in the solder bump can be observed clearly after 14410 cycles of TCT.

To examine the crack propagation, a second cross-section across the horizontal Sn stripe interfaces polished by focused ion beam (FIB) rendered a better crack appearance. Using FIB, the cracks were clearly revealed without coverage by impurities during the mechanical polishing. Figures 4-1(c), 4-2(c), 4-3(c), and 4-4(c) represent the second cross-sections of the solder bumps polished by FIB after 0, 500, 1500, and 14410 cycles of TCT, respectively. We note that these images have been rotated 90 degree, with respect to those in Figures 4-1(b), 4-2(b), 4-3(b), and 4-4(b). It

can be seen that the cracks formed along the Sn/Pb interfaces in the as-fabricated state and expanded greatly along the stripe Sn/Pb interfaces after 14410 cycles of TCT.

#### 4.3.2 Circular Sn grain formation in isothermal annealing

In order to verify that the anisotropic Sn stripe formation is unique to TCT, the microstructure evolution of the composite samples after isothermal annealing was also examined. Figures 4-5(a), 4-5(c), and 4-5(e) show the cross-section of the solder bumps after isothermal annealing at 150 °C for 500, 1000, and 2160 h. During isothermal annealing, some of the Sn-rich phase was consumed by reacting with the Ni UBM and the Cu metallization pad layer to form IMCs. The remaining Sn grains became circular and dramatically decreased in volume in the SnPb composite solder joint. Figures 4-5(b), 4-5(d), and 4-5(f) demonstrate the second cross-sections of the solder bumps polished by FIB after isothermal annealing at 150 °C for 500, 1000, and 2160 h. We found that the cracks along the Sn/Pb interfaces still existed in isothermal annealing, yet they did not propagate across the entire solder joint because the circular Sn grains are isolated from each other.

Figure 4-6 plots the average IMCs thickness as a function of time. The growth rate of the IMCs during isothermal annealing is faster than that during TCT. During isothermal annealing, the Sn atoms diffused a distance about 50  $\mu$ m to react with

UBMs to form IMCs, instead of forming Sn stripes as in TCT. Additionally, as illustrated in Figures 4-5(a), 4-5(c), and 4-5(e), no Sn stripes except circular Sn grains were observed in the solder bump. A literature search revealed that the present finding of isothermal annealing is consistent with the previous studies [75,77].

## 4.3.3 Unmixing of the high-Pb and the eutectic SnPb in isothermal and cycling annealing

A very interesting observation of the microstructure evolution is that there is little intermixing of the high-Pb phase and the eutectic SnPb phase in both isothermal and cycling annealing. This is because in a binary eutectic phase diagram such as SnPb, below the eutectic temperature, a constant temperature line is a tie-line of constant chemical potential. The phases along the tie-line, including the two primary phases at the ends of the two-phase region are at equilibrium. It means there is no driving force or no chemical potential gradient for compositional intermixing. In cycling annealing, there is a temperature change and in turn a potential change. However, as long as the temperature change is uniform across the entire samples, or as long as there is no temperature gradient in the sample at any short period of time, the concept of tie-line holds.

The thickening of the Sn-rich and the Pb-rich phases can be due to ripening

which reduces the total surface area or energy. Ripening can explain the growth of circular Sn grains, but it cannot explain the formation of the anisotropic Sn stripes.

Furthermore, the IMC formation by interfacial reactions with the Ni UBM and Cu bond-pad cannot explain the Sn stripe formation too. Therefore, we are left with the only driving force coming from the thermal stress potential gradient in cyclic annealing. It explains the formation of the Sn stripes and the crack formation along the Sn/Pb interfaces, to be discussed below.

#### 4.3.4 Three-dimensional finite element analysis of thermal stress distribution

Three-dimensional finite element analysis was employed in order to simulate the strain distribution and the stress distribution in the composite solder joints in TCT. The model included the Si chip, the Ni UBMs, the solder joints, the Cu pads, the organic substrate, and the underfill, as demonstrated in Figure 4-1(a). In the simulation, the solder joint was composed of the spherical Sn5Pb95 solder bump above and the cup-like structure of the eutectic Sn63Pb37 solder beneath. The dimensions of the model were identical to those in the real flip-chip samples.

The strain distribution and the stress distribution in the Sn5Pb95 solder are different from those in the Sn63Pb37 eutectic solder. Figure 4-7(a) depicts a 3D simulation of the total mechanical and thermal equivalent strain distribution in the

solder bump after one cycle of TCT. It is obvious that the Sn63Pb37 eutectic solder endured most of the strain, and the maximum tensile strain position in the eutectic solder was pointed out by the arrow, as shown in Figure 4-7(b). The simulation results of maximum strain position agree well with the experimental results that the crack formation was observed to initiate at the interfaces between the Sn-rich phase and the Pb-rich phase. Figures 4-8(a) and 4-8(b) illustrate the 3D simulation of the hydrostatic stress distribution in the solder bump at the extreme temperatures, -55 °C and 125 °C, respectively. The scale bars are shown beside the figures. The positive values in the scale bars represent the tensile stresses, while the negative values stand for the compressive stresses. It can be observed that a tensile stress existed in the Sn5Pb95 on the chip side, whereas a compressive stress existed in the Sn63Pb37 eutectic on the substrate side. During TCT, the compressive stress region became larger when the ambient temperature was lower.

#### 4.3.5 Stress-migration-induced anisotropic grain growth of Sn

Under an elastic stress, microstructure evolution may occur to relieve the stress by creep, provided that atomic diffusion driven by the stress potential gradient can take place. Since Sn has a low melting point (505 K) and since the upper temperature of 125 °C (398 K) in the cycling tests is much above 0.5 of the melting point in

absolute temperature, creep can occur. For the anisotropic growth of Sn grains in the horizontal or lateral direction, we need stress-potential gradient in the vertical direction.

According to Nabarro-Herring model of creep, atomic flux will diffuse from the compressive region to the tensile region. In Figures 4-8(a) and 4-8(b), it is shown that the high-Pb is under tension and the eutectic is under compression, we expect Sn atoms to diffuse from the eutectic to the necking region. Then vertical instead of horizontal stress gradient in the necking region, as shown in Figures 4-8(a) and 4-8(b), will induce a vertical diffusion of Sn from the high compressive stress region in the bottom of the joint to the necking region. This explains the anisotropic growth of Sn stripe in the interfacial region between the high-Pb and the eutectic instead of Sn-rich phase accumulation at the middle or edge of the solder joint under TCT. In addition, the diffusivity of Sn and Pb were  $7.77 \times 10^{-29}$  m<sup>2</sup>/sec and  $1.64 \times 10^{-29}$  m<sup>2</sup>/sec at -55 °C, and they were  $4.16 \times 10^{-18}$  m<sup>2</sup>/sec and  $1.13 \times 10^{-18}$  m<sup>2</sup>/sec at 125 °C, respectively. It is obvious that the stress-migration flux of Sn is larger when the ambient temperature is higher due to the higher atomic diffusivity [83].

#### 4.3.6 Crack propagation along the Sn/Pb interfaces

Generally speaking, crack does not form along the lamellar interfaces in eutectic

structure, especially in eutectic SnPb solder which has been widely used for a very long time. It is a unique finding here that crack forms in composite SnPb solder joints under TCT. Crack tends to form under tension, not under compression. Indeed there is a tensile component in the stress distribution in the composite solder joint as shown in Figures 4-8(a) and 4-8(b). Furthermore, the thicker the Sn phase, the larger the thermal strain due to the difference in thermal expansion coefficient between Sn and Pb. However, in TCT, we need to consider the fatigue contribution to the residual stress in crack formation in the composite solder joint. There must be a significant contribution from plastic deformation in the crack formation and propagation. The analysis of plastic contribution is beyond the scope of this study. To do so experimentally, a change of the cyclic period to affect the creep process, in turn to affect the residual stress and strain, will be informative. More simulation work will clearly be needed. 

#### 4.4 Summary

The evolution of eutectic structure under isothermal and temperature cycle annealing has been studied. When the SnPb composite solder joints were subjected to a TCT between -55 and 125 °C after 500cycles, the Sn grains coarsened and formed anisotropic Sn stripes near the necking site in the solder joint due to the stress

migration. Then the cracks, arising from the thermal stress, propagated along the Sn/Pb interfaces. After the prolonged 14410 cycles of TCT, the Sn stripes almost penetrated the entire solder joint, and the cracks expanded accordingly. The 3D simulation of the strain distribution supports the contention that the crack formation started at the Sn/Pb interfaces. Furthermore, instead of Sn stripes, only coarsened circular Sn grains were observed in the solder joints after a pure isothermal annealing at 150 °C. Therefore, stress migration of the Sn-rich phase triggered by the temperature cycling tests is a critical reliability issue in SnPb composite solder joints.

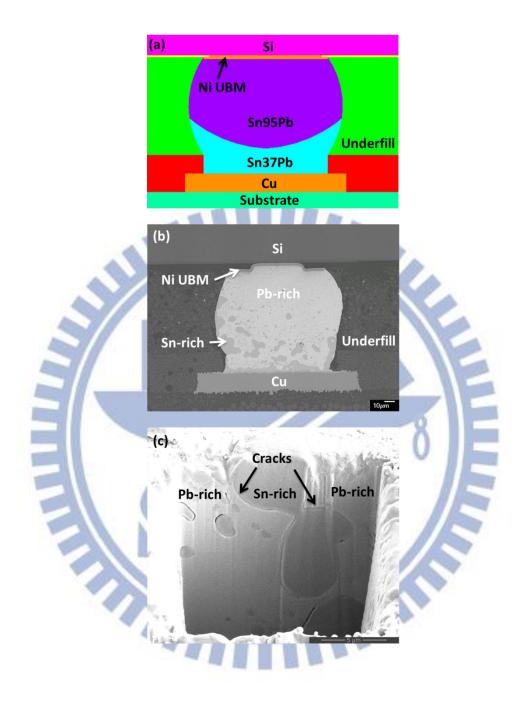


Figure 4-1 (a) Schematic diagram for the solder joint structure used in this study. (b)

Cross-sectional SEM images showing the as-reflowed SnPb composite solder joint. (c)

SEM image showing the FIB-polished second cross-section of the as-fabricated solder bump.

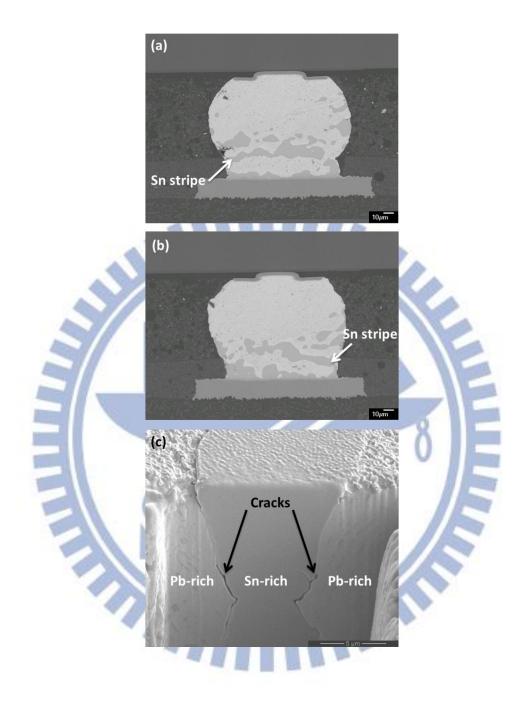


Figure 4-2 (a) and (b) Cross-sectional SEM images showing the solder bump after 500 cycles of TCT. (c) SEM image showing the FIB-polished second cross-section of the solder bump after 500 cycles of TCT.

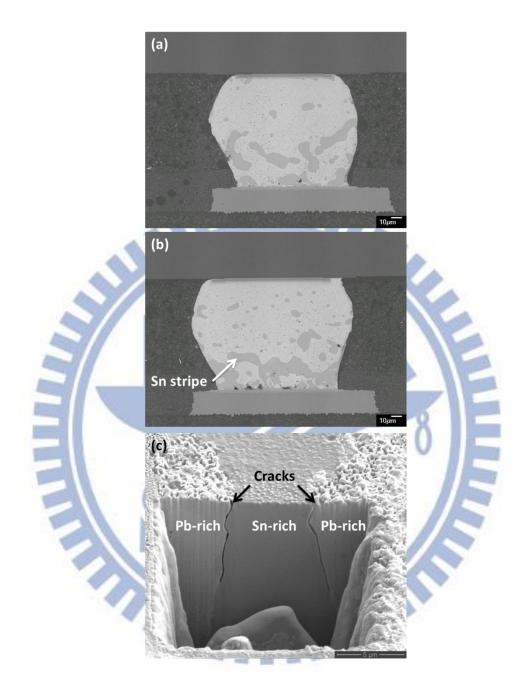


Figure 4-3 (a) and (b) Cross-sectional SEM images showing the solder bump after 1500 cycles of TCT. (c) SEM image showing the FIB-polished second cross-section of the solder bump after 1500 cycles of TCT.

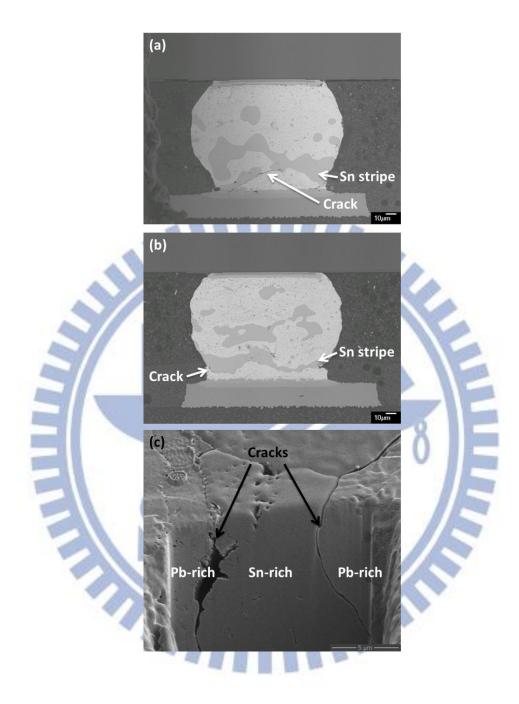


Figure 4-4 (a) and (b) Cross-sectional SEM images showing the solder bump after 14410 cycles of TCT. (c) SEM image showing the FIB-polished second cross-section of the solder bump after 14410 cycles of TCT.

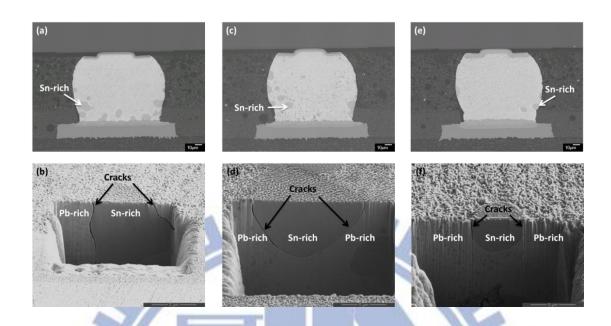


Figure 4-5 Cross-sectional SEM image and SEM image showing the FIB-polished second cross-section of the solder bump after an isothermal annealing at 150 °C for (a), (b) 500 h, (c), (d) 1000 h, and (e), (f) 2160 h.



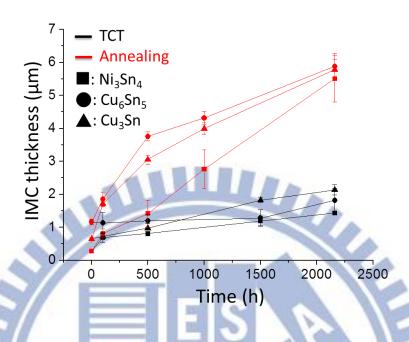
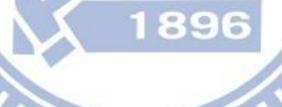


Figure 4-6 The average IMCs thickness as a function of time.



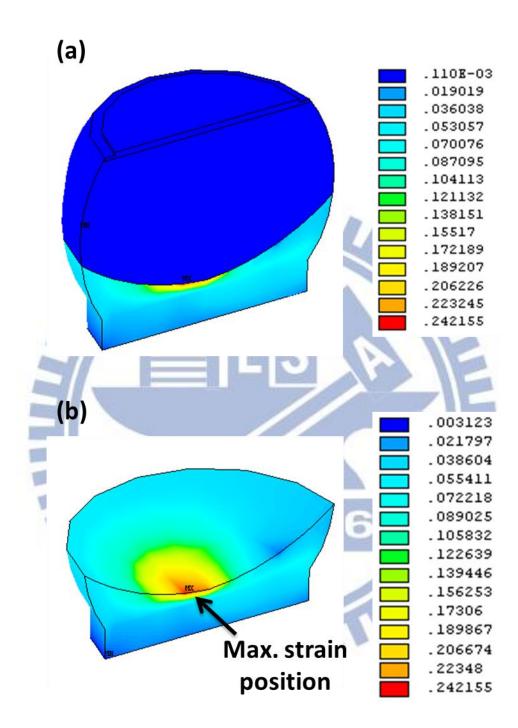


Figure 4-7 Simulation results for the total mechanical and thermal equivalent strain distribution in (a) the solder bump and (b) the Sn63Pb37 presolder after one cycle of TCT.

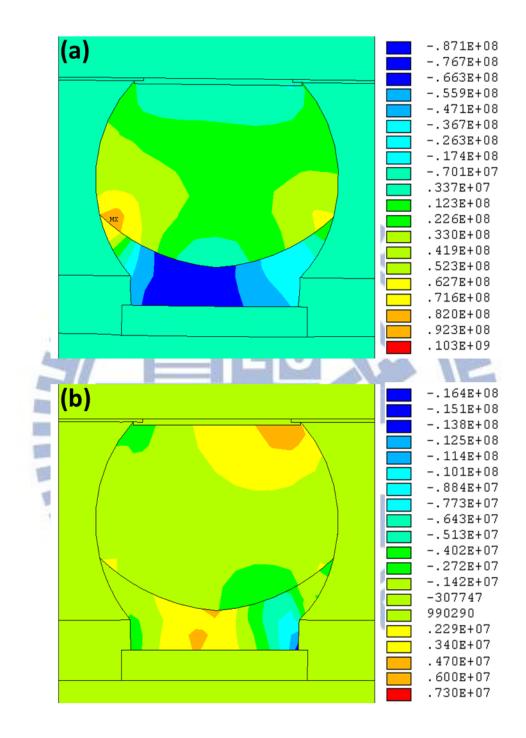


Figure 4-8 Simulation results for the hydrostatic stress distribution in the solder bump at (a) -55  $^{\circ}$ C and (b) 125  $^{\circ}$ C.

## **Chapter 5 Conclusions**

In conclusion, EM failure mechanisms in Pb-free solder joints and stress migration failure mechanisms in SnPb composite solder joints were investigated in this study. Both finite element analysis and theoretical analysis explained the experimental results well. When SnAg solder bumps with 2-µm Ni UBMs were stressed at  $2.16 \times 10^4$  A/cm<sup>2</sup> and 150 °C, open failure occurred in the bump that had electron flow direction from the chip side to the substrate side. However, when Sn-3.0Ag-0.5Cu solder bumps with Cu column UBMs were stressed at  $2.16 \times 10^4$ A/cm<sup>2</sup> and 150 °C, cracks formed along the interface of Cu<sub>6</sub>Sn<sub>5</sub> IMCs and the solder on the substrate side. The 3-D simulation on current density distribution supports the contention that the current crowding effect was responsible for the failure on both the chip and the substrate side for the two kinds of solder bumps. Furthermore, being confirmed by IR microscopy, the alleviation of current crowding by the Cu column UBMs also helped decrease the Joule heating effect in the solder bump during current stressing. Therefore, the solder joints with Cu column UBMs have a higher EM resistance than the traditional flip-chip solder joints.

In addition, the EM failure mechanisms in SnAg solder joints with  $5-\mu$ m-Cu/ $3-\mu$ m-Ni UBM were changed according to the flux divergence at the

IMC/solder interface at various stressing conditions. It was found that both the void formation and the UBM consumption failure mechanisms occurred at the stressing conditions without a TM driving force confirmed by IR microscopy. When the Sn EM flux is larger, void formation at the interface was responsible for the failure. However, UBM dissolution and IMC formation dominated the failure mechanism when the Sn chemical potential flux toward the cathode side exceeded. This model successfully explains the experimental results.

On the other hand, stress migration brought about failures in solder joints. When the SnPb composite solder joints were subjected to a TCT between -55 and 125 °C after 500cycles, the Sn grains coarsened and formed anisotropic Sn stripes near the necking site in the solder joint due to the stress migration. Then the cracks, arising from the thermal stress, propagated along the Sn/Pb interfaces. After the prolonged 14410 cycles of TCT, the Sn stripes almost penetrated the entire solder joint, and the cracks expanded accordingly. The 3D simulation of the strain distribution supports the contention that the crack formation started at the Sn/Pb interfaces. Furthermore, instead of Sn stripes, only coarsened circular Sn grains were observed in the solder joints after a pure isothermal annealing at 150 °C. Therefore, stress migration of the Sn-rich phase triggered by the temperature cycling tests is a critical reliability issue in SnPb composite solder joints.

## **References**

- 1. J. H. Lau, "Flip Chip Technologies" (McGraw-Hill, New York, 1995), pp.123.
- 2. E. M. Davis, W. E. Harding, R. S. Schwartz, and J. J. Corning, Solid logic technology: versatile, high performance microelectronics, IBM J. Res. Develop. 44, 56 (2000).
- 3. L. F. Miller, Controlled collapse reflow chip joining, IBM J. Res. Develop., 13, 239 (1969).
- 4. P. A. Totta and R. P. Sopher, SLT device metallurgy and its monolithic extensions, IBM J. Res. Develop 13, 226 (1969).
- 5. K. Puttlitz and P. A. Totta, "Area Array Interconnection Handbook" (Kluwer Academic, Boston, MA, 2001).
- 6. K. Zeng and K.N. Tu, Mater. Sci. Eng. R. 38, 55 (2002).
- 7. A. Sharif and Y.C. Chan, Mater. Sci. Eng. B. 106, 126 (2004).
- 8. J.W. Yoon, S.W. Kim, and S.B. Jung, Mater. Trans. 45, 727 (2004).
- 9. K. Suganuma, Curr. Opin. Solid State Mater. Sci. 5, 55 (2001).
- 10. S. K. Kang and V. Ramachandran, Scripta Mat. 14, 421 (1980).
- 11. M. O. Alam, Y. C. Chan, and K. C. Hung, J. Electron. Mater. 31, 1117 (2002).
- 12. K.H. Prakash and T. Sritharan, J. Electron. Mater. 32, 939 (2003).

- 13. K. N. Tu and K. Zeng, Mater. Sci. and Eng. R 34, 1 (2001).
- 14. J. W. Yoon, C. B. Lee, and S. B. Jung, J. Electron. Mater. 32, 1195 (2003).
- 15. W. G. Bader, Weld. J. Res. Suppl. 28, 551 (1969).
- 16. K. N. Tu, J. Appl. Phys. 94(9), 5451 (2003).
- 17. P. G. Shewmon, "Diffusion in Solids" (TMS, Warrendale, PA 1989), Chapter 7.
- 18. K. N. Tu, Solder Joint Technology \_Springer, New York, 2007, pp. 211–287.
- 19. M. E. Looms and M. E. Fine, Metall. Mater. Trans. A 31A, 1155 (2000).
- 20. A. Christou, "Electromigration and electronic device degredation" Wiley, New York (1994).
- 21. Q. T. Huynh, C. Y. Liu, C. Chen, and K. N. Tu, J. Appl. Phys. 89, 4332 (2000).
- 22. J. W. Jang, C. Y. Liu, P. G. Kim, K. N. Tu, A. K. Mal, and D. R. Frear, J. Mater.
  Res. 15 1679 (2000).
- 23. Y. Guo, W. T. Chen, and C. K. Lim, Proceedings of the ASME Conference in Electronic Packaging, San Jose, CA, 1992, pp. 199.
- 24. E. C. C. Yeh, W. J. Choi, K. N. Tu, P. Elenius, and H. Balkan, Appl. Phys. Lett. 80(4), 580 (2002).
- L. Y. Zhang, S. Q. Ou, J. Huang, K. N. Tu, S. Gee, and L. Nguyen, Appl. Phys.
   Lett. 88, 012106 (2006).
- 26. R. A. Oriani, J. Phys. Chem. Solids 30, 339 (1969).

- 27. H. Ye, C. Basaran, and D. Hopkins, Appl. Phys. Lett. 82(7), 1045 (2003).
- 28. T. L. Shao, S. H. Chiu, C. Chen, D. J. Yao, and C. Y. Hsu, J. Electron. Mater. 33, 1350 (2004).
- 29. S. H. Chiu, T. L. Shao, C. Chen, D. J. Yao, and C. Y. Hsu, Appl. Phys. Lett. 88, 022110 (2006).
- 30. S. H. Chiu, Thesis, National Chiao Tung University, 2007.
- 31. 何煇耀, 可靠度保證-工程與管理技術之應用: 中華民國品質學會發行。
- 32. J. R. Black, IEEE Trans. Electron Devices ED 16, 338 (1969).
- 33. W. J. Choi, E. C. C. Yeh, and K. N. Tu, J. Appl. Phys. 94, 5665 (2003).
- 34. H. Wever, Elektro u. Thermo-transport in Metallen, J. A. Barth, Leipzig 1973, pp. 216.
- 35. H. Ye, C. Basaran and D. C. Hopkins, Appl. Phys. Lett. 82, 1045 (2003).
- 36. C. Basaran, H. Ye, D. C. Hopkins, D. R. Frear, and J. K. Lin, J. Electronic Packaging, 27, 157 (2005).
- 37. A. Huang, A. M. Gusak, K. N. Tu, and Y. S. Lai, Appl. Phys. Lett., 88, 141911 (2006).
- 38. H. Y. Hsiao and C. Chen, Appl. Phys. Lett., 94, 092107 (2009).
- 39. H. Y. Chen, C. Chen, and K. N. Tu, Appl. Phys. Lett. 93,122103 (2008).
- 40. F. R. N. Nabarro, Deformation of crystals by the motion of single ions, Report of

- conference on Strength of Solids, Physical Society, London (1948).
- 41. C. Herring, J. Appl. Phys. 94, 437 (1950).
- 42. C. Chen, H. M. Tong, and K. N. Tu, Annu. Rev. Mater. Res. 40, 531 (2010).
- 43. C. Y. Liu, C. Chen, C.N. Liao, and K. N. Tu, Appl. Phys. Lett. 75, 58 (1999).
- 44. T. L. Shao, Y. H. Chen, S. H. Chiu, and C. Chen, J. Appl. Phys. 96, 8, 4518 (2004).
- 45. S. W. Liang, Y. W. Chang, and C. Chen, Appl. Phys. Lett. 88, 172108 (2006).
- 46. H.Y. Hsiao and C. Chen, Appl. Phys. Lett. 90, 152105 (2007).
- 47. S. W. Liang, T. L. Shao, C. Chen, E. C. C. Yeh, and K. N. Tu, J. Mater. Res. 21, 1 (2006).
- 48. J. W. Nah, J. O. Suh, K. N. Tu, S. W. Yoon, V. S. Rao, V. Kripesh, and Fay Hua, J. Appl. Phys. 100, 123513 (2006).
- 49. Y. S. Lai, Y. T. Chiu, and J. Chen, J. Electron. Mater. 37, 1624 (2008).
- 50. L. Xu, J. K. Han, J. J. Liang, K. N. Tu, and Y. S. Lai, Appl. Phys. Lett. 92, 262104 (2008).
- 51. J.H. Ke, T.L. Yang, Y.S. Lai, and C.R. Kao, Acta Mater. 59, 2462 (2011).
- 52. H.Y. Hsiao, S. W. Liang, M. F. Ku, C. Chen, and D. J. Yao, J. Appl. Phys. 104, 033708 (2008).

- F.Y. Ouyang, K. N. Tu, C.L. Kao, and Y.S. Lai, Appl. Phys. Lett., 90, 211914
   (2007).
- 54. S. W. Liang, S. H. Chiu, and C. Chen, Appl. Phys. Lett., 90, 082103 (2007).
- 55. H. K. Kim, K. N. Tu, Appl. Phys. Lett. 67, 2002 (1995).
- 56. P. G. Kim, J. W. Jang, T. Y. Lee, J. Appl. Phys. 86, 6746 (1999).
- 57. H. F. Hsu, S. W. Chen, Acta Mater. 52, 2541 (2004).
- 58. C. Schmetterer, H. Flandorfer, H. Ipser, Acta Mater. 56, 155 (2008).
- Y. C. Hsu, T. L. Shao, C. J. Yang, C. Chen, J. Electron. Mater. 32(11), 1222
   (2003).
- 60. Y. W. Chang, S. W. Liang, C. Chen, Appl. Phys. Lett. 89, 032103 (2006).
- 61. H. Y. Chen, M. F. Ku, C. Chen, Adv. Mater. Res. 1, 83 (2012).
- 62. F. Y. Ouyang, C. L. Kao, J. Appl. Phys. 110, 123525 (2011).
- 63. H. B. Hungtington, A. R. Grone, J. Phys. Chem. Solids. 20, 76 (1961).
- 64. P. H. Sun, M. Ohring, J. Appl. Phys. 47, 478 (1976).
- 65. W. Seith, T. Heumann, Diffusion of metals: exchange reactions. Washington, DC: United States Atomic Energy Commission; 1962. Translated from a publication of Springer, Berlin. pp. 65.
- 66. K. Y. Lee, M. Li, D. R. Olsen, W. T. Chen, B. T. C. Tan, S. Mhaisalkar, in: Proc. 51st Electron. Compon. Technol. Conf., IEEE, New York, 2001, pp. 478.

- 67. J. W. Yoon, Y. H. Lee, D. G. Kim, H. B. Kang, S. J. Suh, C. W. Yang, C. B. Lee, J.
- M. Jung, C. S. Yoo, S. B. Jung, J. Alloys Compd. 381, 151 (2004).
- 68. I. A. Blech, C. Herring, Appl. Phys. Lett. 29, 131 (1976).
- 69. F. Y. Ouyang, K. Chen, K. N. Tu, Appl. Phys. Lett. 91, 231919 (2007).
- 70. M. Lu, D. Y. Shih, P. Lauro, C. Goldsmith, D. W. Henderson, Appl. Phys. Lett. 92, 211909 (2008).
- 71. C. S. Chang, A. Oscilowski, R. C. Bracken, IEEE Circuits and Devices Mag. 14,45 (1998).
- 72. D. O. Powell, A. K. Trivedi, in Proc. 43rd Electron. Compon. and Technol. Conf. 182 (1993).
- 73. R. K. Doot, in Proc. 46th Electron. Compon. and Technol. Conf. 535 (1996).
- 74. J. H. Lau, Ball Grid Array Technology, McGraw-Hill, New York, 1995.
- 75. L. Y. Hung, P. H. Chang, C. C. Chang, Y. P. Wang, C. S. Hsiao, C. R. Kao, in Proc. 3rd Int. Microsyst. Packag. Assem. Circuits Technol. 255 (2008).
- 76. C. C. Chang, Y. W. Lin, Y. S. Lai, C. R. Kao, J. Electron. Mater. 38(11), 2234 (2009).
- 77. C. C. Chang, Y. W. Wang, Y. S. Lai, C. R. Kao, J. Electron. Mater. 39(8), 1289 (2010).
- 78. C. L. Lai, C. H. Lin, C. Chen, J. Mater. Res. 19(2), 550 (2004).

- 79. E. T. Ogawa, J. W. McPherson, J. A. Rosal, K. J. Dickerson, T. C. Chiu, L. Y. Tsung, M. K. Jain, T. D. Bonifield, J. C. Ondrusek, W. R. McKee, in Proc. 40th Annu. Int. Reliab. Phys. Symp. 312 (2002).
- 80. T. C. Wang, T. E. Hsieh, M. T. Wang, D. S. Su, C. H. Chang, Y. L. Wang, J. Y. M. Lee, J. Electrochem. Soc. 152(1), G45 (2005).
- 81. H. Tsuchikawa, Y. Mizushima, T. Nakamura, T. Suzuki, H. Nakajima, Jpn. J. Appl. Phys. 45(2A), 714 (2006).
- 82. K. Suganuma, A. Baated, K. S. Kim, K. Hamasaki, N. Nemoto, T. Nakagawa, T. Yamada, Acta Mater. 59, 7255 (2011).
- 83. D. Gupta, K. Vieregge, W. Gust, Acta Mater. 47(1), 5 (1999).

## **Publication list**

### **International journals**

- Liang, Y. C., Tsao, W. A., Yao, D. J., Lai, Y. S., Chen, C., Huang, A. T., Feb.
   2012, Influence of Cu column under-bump-metallizations on current crowding
   and Joule heating effects of electromigration in flip-chip solder joints, J. Appl.
   Phys. 111, 043705.
- Liang, Y. C., Chen, C., Tu, K. N., Aug. 2012, Side wall wetting induced void formation due to small solder volume in microbumps of Ni/SnAg/Ni upon reflow, ECS Solid State Letters 1(4), 60.
- Liang, Y. C., Lin, H. W., Chen, C., Chen, H. P., Tu, K. N., Lai, Y. S., Mar. 2013,
   Anisotropic grain growth and crack propagation in eutectic microstructure under cyclic temperature annealing in flip-chip SnPb composite solder joints, Scripta Mater. 69, 25.

#### **International conferences**

 Liang, Y. C., Chen, C., Oct. 2009, Direct measurement of hot-spot temperature in flip-chip solder joints with Cu columns under current stressing using infrared microscopy, International Microsystems, Packaging, Assembly and Circuits

- Technology Conference, pp. 158-161.
- Liang, Y. C., Chen, C., Yao, D. J., Apr. 2010, Direct measurement of hot-spot temperature in flip-chip solder joints with Cu columns under current stressing using infrared microscopy, MRS Spring Meeting.
- Liang, Y. C., Chen, C., Yao, D. J., Chang, T. C., Zhan, C. J., Juang, J. Y., Oct.
   2010, Direct measurement of temperature distribution in flip-chip micro-bumps
   under current stressing by using infrared microscopy, International Microsystems,
   Packaging, Assembly and Circuits Technology Conference.
- Liang, Y. C., Chen, C., Yao, D. J., Chang, T. C., Zhan, C. J., Juang, J. Y., Sep.
   2011, Joule heating effect in microbumps for 3D IC packaging, International
   Union of Materials Research Societies International Conference in Asia.
- Liang, Y. C., Chen, C., Oct. 2011, Microstructure evolution in a sandwich structure of Ni/SnAg/Ni microbump during reflow, International Microsystems, Packaging, Assembly and Circuits Technology Conference.
- Liang, Y. C., Tsao, W. A., Yao, D. J., Lai, Y. S., Chen, C., Dec. 2011, Influence
  of Cu columns on current crowding effect in electromigration in flip-chip solder
  joints, Electronics Packaging Technology Conference.
- Liang, Y. C., Chen, C., Tu, K. N., Jan. 2013, Side wall wetting induced void formation due to small solder volume in microbumps of Ni/SnAg/Ni upon reflow,

Pan Pacific Microelectronics Symposium.

# **Domestic journals**

• Liang, Y. C., Tsao, W. A., Chen, C., Nov. 2010, Influence of Cu columns on current crowding effect in electromigration in flip-chip solder joints, ASE Tech.

