國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

以深層暫態能譜分析碳化矽缺陷之研究暨溝槽式接面蕭基位障二極體之設計分析

A study on the Defect in SiC by Deep Level Transient Spectroscopy (DLTS) and Design Analysis of the SiC Trench Junction Schottky Barrier (TJBS) Diode

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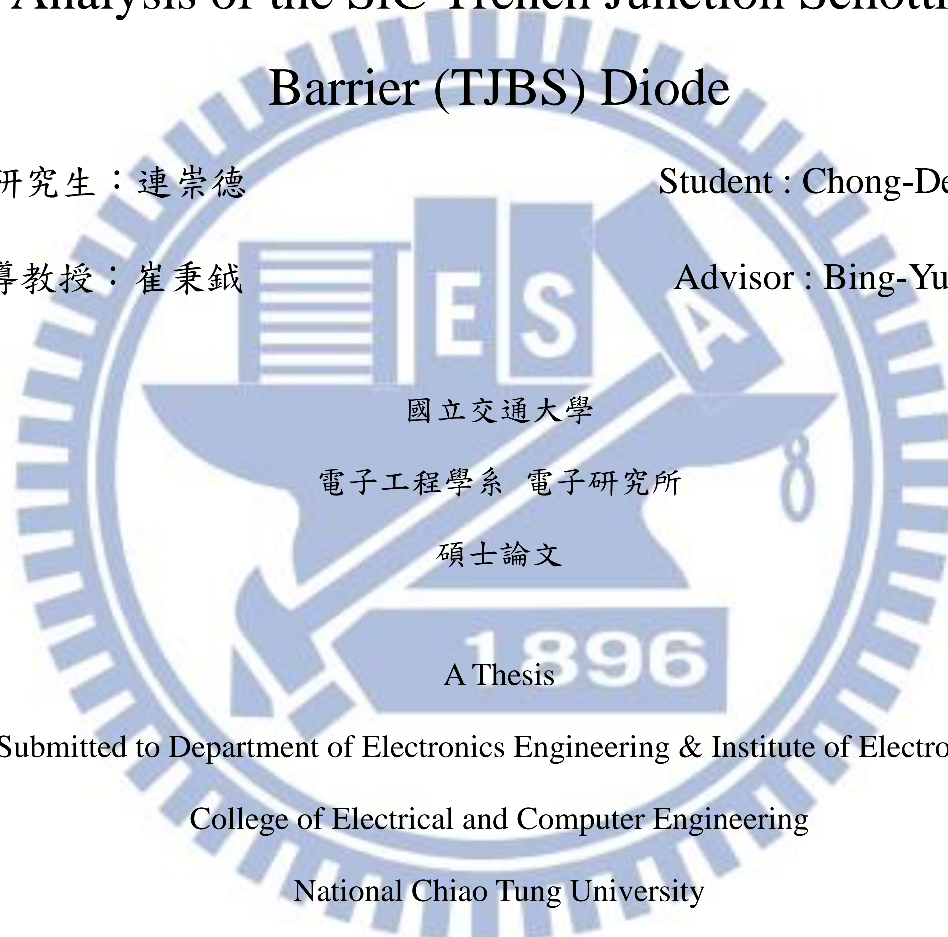

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摘要

由於碳化矽具有高崩潰電場和高導熱係數，應用於高溫高壓的元件是非常好的半導體材料。對於高壓元件而言，磊晶層的品質會影響到導通電阻、崩潰電壓和逆偏漏電，所以是非常重要的一環。深層暫態能譜分析能夠測量出缺陷能階、捕獲截面積，以及缺陷密度。此外，深層暫態能譜分析對於缺陷擁有高靈敏度，而且與其它偵測系統比起來相對容易去架設，因此我們選擇深層暫態能譜分析來偵測磊晶層之中的缺陷。而碳化矽中最廣泛的高壓元件應用就是蕭基位障二極體、接面二極體和接面蕭基位障二極體。為了改進接面蕭基位障二極體的特性或是簡化製程，有許多不同的結構變化。溝槽式接面蕭基位障二極體是當中最新的結構，因此我們將會利用Sentaurus TCAD tool，對於溝槽式接面蕭基位障二極體去找出其設計概要。

深層暫態能譜分析的架設是利用安捷倫半導體儀器分析儀和有溫度控制器的探測台。利用市售之深層暫態能譜分析系統來作為我們深層暫態能譜分析之系統驗證。我們的系統與市售系統在相同位置有一樣的峰值，只是我們的半導體儀器分析儀的電容量測速度比較慢，所以我們的系統有著相對弱的訊號。

試片方面製作了鎳金屬於碳化矽上的蕭基位障二極體和電容去量測磊晶層的缺陷。對於蕭基二極體而言，深層暫態能譜分析系統沒有量測到任何的缺陷。因此利用低劑量之氮離子佈值去創造缺陷。經過離子佈值之後，有非常強烈的深

層暫態能譜訊號被偵測到，但是這訊號是由不同缺陷組成的，所以無法萃取缺陷能階。我們也利用不同的方式去減少離子佈值造成的缺陷，當中最有效的是 1600 度的高溫退火，幾乎所有離子佈值造成的缺陷都可以被修復，只是高溫退火同時也會產生缺陷 $Z_{1/2}$，而缺陷 $Z_{1/2}$可以利用高溫退火前之碳離子佈值，或是碳化矽之氧化去消除。

在本次研究中，我們也使用深層暫態能譜分析系統去量測碳化矽電容之介面能態。而電容的介電層是利用熱氧化方式生長在碳化矽上的二氧化矽。而電容量測到的深層暫態能譜並不是介面能態，反而是被介電層缺陷所主導整個分析。若是深層暫態能譜量測到含有其他種缺陷，那麼利用深層暫態能譜萃取出之介面能態將會是不正確的。而利用離子佈值後的磊晶層所做出之電容，展現了非常差的電容對電壓曲線，但是在深層暫態能譜分析方面卻與蕭基位障接面二極體有一樣的結果。

溝槽式接面蕭基位障二極體之模擬分析已經利用不同的布局參數去找到它的設計概要。當溝槽之深度加深時，因為從側壁來的額外電流，所以有比較小的臨界電壓。轉換電壓被定義成電流導通機制由單極電流 (蕭基接面電流) 轉換成雙極電流 (介面二極體電流)的電壓。與一般接面蕭基二極體相比，溝槽式接面蕭基位障二極體有比較低的轉換電壓，且導通之後有相對低的導通電阻和比較的順向導通電流。轉換電壓會隨著蕭基接面的寬度增加而增加，但是會隨著接面二極體之寬度和溝槽深度而減少。

與一般接面蕭基位障二極體相比，由於溝槽式接面蕭基位障二極體有溝槽底部有溝槽角落和較薄的磊晶層，所以會有比較低的崩潰電壓。而對於溝槽式接面蕭基位障二極體而言，崩潰發生的原因是來自於結構上的設計，因此並不能用邊緣終端技術來提高它的崩潰電壓。溝槽式接面蕭基位障二極體比較適合應用在高電流之元件應用，然而一般接面蕭基位障二極體卻是比較適合應用在高壓操作使用。

總體而言，深層暫態能譜分析系統之架設與驗證已經完成。因為氮離子佈值所造成的不同缺陷已經被偵測到，而且這些缺陷可以藉由 1600 度的退火去除，但是同時也會產生缺陷 $Z_{1/2}$。深層暫態能譜分析於碳化矽電容上量到的訊號主要是介電層缺陷所主導；若是深層暫態能譜量到有其他缺陷，那麼在轉換至介面能態時，介面能態將會被高估。在相同條件下，蕭基位障二極體與電容有一樣的深層暫態能譜。溝槽式接面蕭基位障二極體的設計概要已經被分析出來，而溝槽結構會對元件的所有特性造成影響。溝槽式接面蕭基位障二極體比較適合應用在高電流之元件應用，然而一般接面蕭基位障二極體卻是比較適合應用在高壓操作使用。

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Abstract

Silicon carbide (SiC) is an ideal semiconductor material for the higher power and high temperature applications due to its wide bandgap, high critical electric field, and good thermal conductivity. For high breakdown voltage device, the quality of the n^- epi-layers is very important, because it influences the on-resistance, junction leakage current, and breakdown voltage of device. Deep level transient spectroscopy (DLTS) is capable of characterizing the defect energy, defect capture cross section, and density of defect quantitatively. Besides, DLTS has high sensitivity and is relatively easier than the other defect detection systems to be setup. Hence, we choose DLTS to analysis the defects in the epi-layer. The widest applications of SiC are its power diodes like Schottky barrier diode, pn diode, and junction barrier Schottky (JBS) diode. The JBS diodes have many different variations of structure for the improvement in performance or the ease of process. The trench junction barrier Schottky (TJBS) diode is one of the latest innovations, so we are going to figure out

the design guidelines of the TJBS diodes by the Sentaurus TCAD tool.

The setup of DLTS system consists of a semiconductor parameter analyzer with a capacitance measurement unit and a probe station with a temperature heating controller. Our DLTS system can measure the same signal but weaker signal intensity in comparison with the commercial DLTS system due to the sampling rate limitation of the capacitance measurement unit.

To measure the defects in epi-layer, Ni/SiC Schottky barrier diode and SiC MOS capacitor are fabricated. For the Schottky barrier diode, there is no defect measured by our DLTS system. In order to create defects in the epi-layers, low dose nitrogen ion implantation is introduced. After ion implantation, strong signal is measured in the DLTS, but severe overlap of signals from different defects makes it hard to extract the defect energy. Different processes are applied to eliminate the defects induced by ion implantation. The most effective one is annealing at 1600 ^{o}C.Almost all the defects induced by ion implantation are eliminated. However, high temperature annealing could generate $Z_{1/2}$ defect.

The interface state of the SiC MOS capacitor is also investigated by our DLTS system. The gate dielectric of MOS capacitor is thermal oxide. The DLTS of MOS capacitor is dominated by oxide trap in SiO_2. The signals from oxide traps overlap the signals from interface states. If the DLTS is not only composed of interface states, the direct transformation of DLTS into interface state density would be incorrect. For MOS capacitor fabricated on the ion-implanted epi-layer, poor capacitance-voltage characteristic is exhibited, but the DLTS result is the same as that measured on the Schottky barrier diode.

The design guidelines of the TJBS diode have been investigated by considering different geometric parameters. As the trench depth becomes deeper, the cut-in voltage becomes slight lower due to the extra sidewall current. We define the

transition voltage as the voltage at which the current transport changes from unipolar conduction (Schottky junction dominant) to bipolar conduction (pn junction dominant). TJBS diodes have lower transition voltage, and thus lower specific on-resistance and higher forward conduction current after bipolar conduction. The transition voltage increases as wider Schottky contact width, but decreases as wider pn junction width or deeper trench depth. Because of trench corner and thinner epi-layer under the pn junction due to the trench structure, relatively low breakdown voltage is observed on TJBS diodes than JBS diodes. For TJBS diodes, the breakdown voltage depends on structural design, which can be compensated by edge termination design.

In conclusion, the setup and verification of DLTS system have been accomplished. Different defects after nitrogen ion implantation has been detected in Schottky barrier diode. These defects can be annihilated by a 1600 ^{o}C annealing, but meanwhile $Z_{1/2}$ defect will be generated. The DLTS of MOS capacitor are dominated by oxide trap. The D_{it} from DLTS would be overestimated if other traps are mixed in the signal. Under the same process condition, Schottky barrier diode has identical DLTS result to MOS capacitor. The design guidelines of TJBS diodes are proposed. The trench affects all the characteristics of device. It is suggested that TJBS diodes are suitable for the higher current application, while JBS didoes are favored for high voltage application.

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Chapter 1
Introduction

1-1 History of Power Devices

The first power device is germanium diode appeared in 1952. In 1957, Silicon controlled rectifier (SCR) [1], also called thyristor, was invented in a 4-layer structure with alternating n-type layer and p-type layer. SCR has the advantages of high blocking voltage and high on-current. The structure of SCR contains 3 bipolar junctions. These junction capacitances result in low switching speed of about 50 to 60 Hz [2].

Bipolar Junction Transistor (BJT) was introduced in 1960s, which is capable of withstanding high reverse blocking voltage and high on-current. In the meanwhile, BJT overcomes the slow switching speed of SCR and can be controlled by external signal [3]. However, it still takes time to charge junction capacitances in BJT which slows the switching speed [4]. Furthermore, BJT has poor current gain in the high frequency applications [5].

With the mature of semiconductor process technology, the power MOSFET commercial products became available in 1970s. Power MOSFET has high input impendence and low input driving current. MOSFET has also much faster switching speed than BJT, because MOSFET is free of minority carrier storage phenomenon [3]. The main drawback of MOSFET is that it's limited to lower power applications [6].

Insulated Gate Bipolar Transistor (IGBT) combines the advantages of BJT and MOSFET [3]. IGBT has the gate-structure of MOSFET and bipolar conduction of BJT, which can be controlled by external signal. Better conducting current and higher breakdown voltage than MOSFET can be achieved. However, if the switching speed

in IGBT become faster, the forward voltage drop will become larger. IGBT has slower switching speed than MOSFET, although this problem has been solved in recently researches [3].

Since the introduction of power device to today, it has been passed over several decades, and most of power devices are made of silicon. Many efforts have been devoted to meet the requirements of power devices, and the most important characteristics of power devices are high breakdown voltage, low on-resistance, low reverse leakage current, high operation temperature, and fast switching speed. The followings are the fundamentals of these characteristics:

1. Breakdown voltage

Impact ionization is the phenomenon that electron gain energy from semiconductor band bending. Once the electron energy reaches 1.5 times of the semiconductor bandgap [7], the electron can generate an electron-hole pair. The generated electron and hole gain energy from band-bending again, and induce another two electron-hole pairs. Such a multiplication process is called avalanche breakdown.

2. On–resistance (R_{on})

The ideal R_{on} of the drift region is expressed in eq. (1-1) [7].

$$R_{on} = \frac{4BV^2}{\varepsilon_s \mu_n E_c} , \qquad \text{eq. (1-1)}$$

where BV is the breakdown voltage of device, ε_s is the dielectric constant of semiconductor (F/cm^{-2}), μ_n is the electron mobility (cm^2/V·s) in drift region. E_c is the critical breakdown electric field (V/cm), which is proportional to the semiconductor bandgap. The increasing of doping concentration of the drift region helps in reducing on-resistance, but it also decreases the breakdown voltage of devices.

3. Reverse leakage current

Junction reverse leakage current is directly proportional to the intrinsic carrier density (n_i). From eq. (1-2) [9], the greater the intrinsic carrier density is, the larger leakage current is.

$$J_L=\frac{qn_iW}{\tau_e} + q\left(\frac{D_h}{\tau_h}\right)^{1/2} \frac{n_i^{\,2}}{N_D}, \qquad \text{eq. (1-2)}$$

where n_i is the intrinsic carrier concentration (cm^{-3}), W is the depletion region width (cm), τ_e is the lifetime of electrons (s), N_D is the donor concentration (cm^{-3}), D_h is the diffusion constant of holes in the n-type region (cm^2/s), and τ_h is the lifetime of holes.

In the view of intrinsic carrier density, as the bandgap (E_g) becomes larger, the intrinsic carrier density becomes smaller as expressed in eq. (1-3) [10].

$$n_i = \sqrt{N_C N_V}\; e^{-\frac{E_g}{2kT}}, \qquad \text{eq. (1-3)}$$

where N_C is the effective density of states in conduction band (cm^{-3}) and N_V is the effective density of states in valence band (cm^{-3}), E_g is the bandgap, k is Boltzmann constant, and T is the temperature in Kelvin.

4. High operation temperature

For applications of power devices in special situations, like car engine, jet aircraft engine, or deep oil extraction, the operation temperature of environment is normally higher than 150°C [11] At such a high temperature, reverse leakage current will increase remarkably according to eq. (1-3), which is not desire for high power devices. For all mentioned above, the bandgap of material is a very important material characteristics for high power device. Since the bandgap of silicon is only 1.12 eV, it's necessary to use wide bandgap material to match the requirements of power devices.

1-2 Overview of Wide Bandgap Materials

Recently advances in semiconductor process technology have pushed the

silicon-based power devices to the theoretical limit of silicon material. Even though, silicon-based devices cannot satisfy all of the requirements of power devices, like higher breakdown voltage, lower on-resistance, smaller reverse leakage current, and higher operation temperature. Hence, many kinds of wide bandgap semiconductors have been raised to break through the limitation of silicon as listed in Table 1 [11]. Silicon Carbide (SiC), Gallium nitride (GaN), and diamond have 3 times wider bandgap than that of silicon. Accompanying with wider bandgap, the intrinsic carrier density becomes smaller, so the reverse leakage current can be lower. Due to higher critical electric field, which allows higher doping concentration in drift region, the breakdown voltage and on-resistance of power device under the same requirement can be improved future more. In addition, the total area of device can be reduced.

Among these materials, diamond has the best material properties, but it is too expensive for massive production of semiconductor and its technology is not mature enough to fabricate power devices. For the rest of wide bandgap materials, GaN shows the best physical properties with wider bandgap and higher electron mobility which benefits high frequency applications [12]. However, there are some disadvantages on GaN-based devices. First, GaN has no native oxide like silicon [11], so it's hard to fabricate MOSFET on GaN substrate. Second, the crystal growth of GaN has to be heteroepitaxy on sapphire or SiC substrate, the quality of GaN wafer and the cost are still issues. Though, pure GaN substrate is available, but it's much more expensive than heteroepitaxy.

When it comes to SiC, all the problems mentioned in GaN are relaxed. SiC has native oxide like silicon, and it's relatively easy to transfer the matured silicon-based technology to SiC-based technology. SiC boules can be grown, so the cost of SiC wafer is lower than that of GaN wafer. The most important advantage of SiC over GaN is its excellent thermal conductivity, about 4 times higher than GaN [11],

because under high power and high temperature operation situation the dissipation of heat generated by device inside must be conducted very quickly.

As discussed above, the excellent electrical and material properties of SiC are very suitable for high temperature and high power devices.

1-3 Silicon carbide (SiC) Crystals

Silicon carbide (SiC) is composed of a silicon atom and a carbon atom, and each silicon atom is covalently bonded with 4 carbon atoms in the tetrahedral arrangement as shown in Fig.1-1. The lattice structure of SiC is hexagonal, and all the atoms have the suited position in lattice structure as shown in Fig. 1-2. There are more hundreds of prototypes of SiC, because they all have different crystal stacking orders. If all the bilayers of SiC have the same orientation, with an ABCABC stacking order in Fig.1-3, we call it 3C-SiC with face-centered cubic (FCC) structure [13]. 3C-SiC is the only one cubic structure in all the prototypes of SiC [14]. When the stacking sequences become ABAB with a hexagonal-closed packed (HCP) structure, we call it 2H-SiC.

All the SiC structures are described by hexagonal coordinate system. The hexagonal coordinate system is composed by three plane coordinates: a_1, a_2, a_3 and a c-axis coordinate. As shown in Fig.1-4, a_1, a_2, a_3 are the plane coordinates with an angle of 120° to each other, and c-axis is perpendicular to the plane coordinates, which represents the stacking layer direction. If only three Miller indices, the symmetry of lattice structure of hexagonal is not obvious, so four Miller indices is quietly suitable for SiC crystals [14].

Different prototypes of SiC have different physical and electrical properties. Here we interest in 4H-SiC and 6H-SiC with bandgap equal to 3.26 eV and 3 eV, respectively. 4H-SiC and 6H-SiC are the combination of hexagonal and cubic types of

SiC. 4H-SiC has the ABAC structure order, and 6H-SiC has the ABCACB stacking sequences as shown in Fig. 1-3. Although they have similar physical and electrical properties, 4H-SiC has about 2 times higher electron mobility than 6H-SiC. In addition, 4H-SiC shows isotropic electrical characteristics in anisotropic direction of lattice, but 6H-SiC doesn't, which is not ideal for vertical structure [14]. Hence, 4H-SiC is the most widely used crystal in power devices.

1-4 Quality of SiC epi-layer

4H-SiC is an ideal candidate for high power devices. With a 3.26 eV bandgap, 4H-SiC has a critical electrical field about 10 times of silicon. Benefited from this, 4H-SiC power devices have higher breakdown voltage and lower on-resistance as shown in Fig. 1-5 [15], as well as lower reverse leakage current. Besides, excellent thermal conductivity promises the high temperature application of 4H-SiC power devices [16]. Power devices are used as a discrete component in circuits, so there's no interconnection problem; in order to spare the device area and utilize the 4H-SiC substrates, almost all the power devices are fabricated in vertical structure, like VDMOSFET, UMOSFET, BJT and IGBT as shown in Fig.1-6 [16, 17].

For all the power devices, the lightly doped region to sustain high breakdown voltage is essential. In silicon, this region can be doped by dopant diffusion, but it's impossible in SiC due to extreme low diffusivity of dopant in SiC [18]. Ion implantation causes lattice damages, and the electrical properties may be degraded even after high temperature activation annealing [19]. Consequently, for SiC, adapting epi-layers as the lightly doped region is vital, and the qualities of SiC epi-layers directly affect the performance of SiC-based power device [20]. Defects in SiC epi-layers cause the premature of breakdown and increase of leakage current and

on-resistance [21]. The structure defects in SiC epi-layers include stacking faults, inclusions of prototypes, micro-pipes, dislocations, pits, carrots…, and all of them can be inspected by techniques like optical microscopy (OM), scanning electron microscopy (SEM), atomic force microscopy (AFM), x-ray diffraction (XRD) [22, 23]. However, some defects inside the epi-layers like vacancy, interstitials, and carbon-clusters in SiC epi-layer cannot be detected easily by the above methods, but they still affect the electrical properties directly.

Many techniques have been proposed to characterize the quality of epi-layer. The simplest one is measuring the resistance of the epilayer, but it's unable to locate the defect energy level in the bandgap of semiconductor. There are some methods can determine the energy level of trap. Photoluminescence (PL) and deep level transient spectroscopy (DLTS) are the most common techniques used to characterize the energy levels of traps in semiconductors [23, 24]. PL is a non-destructive technique with very high spectrum resolution to atom-sized defect. However, PL cannot detect some defects like di-vacancy and only neutral-charged trap can be characterized, called quenching in PL. In addition, the intensity of PL spectrum is not proportional to the density of defect, so it's impossible to calculate density of defect from PL [25].

DLTS has high sensitivity to defects, and almost all defects can be characterized under proper measurement conditions. Not only substrate defects but also interface states of MOS structure can be characterized [26]. More information can be provided from DLTS, like trap energy level, trap capture cross section, and trap density. DLTS can even characterize the space distribution of defects in device. Besides, setting up a DLTS measurement system only needs a capacitance versus time (C-t) meter, and a temperature controller. It's relatively easy to establish and operate in comparison with other techniques. In order to verify the quality of 4H-SiC epi-layers after ion implantation and dopant activation, we setup a DLTS measurement system and DLTS

measurement is performed on samples with different processes in this thesis.

1-5 Power diodes of SiC

As far as now, SiC-based power devices are the most matured technology among the other wide bandgap materials. 4H-SiC Schottky barrier diodes (SBDs) have been widely used in fast switching and high temperature applications as shown in Fig. 1-7 [27, 28]. The most commonly metals used on 4H-SiC SBDs are nickel (Ni) and titanium (Ti) with Schottky barrier heights (SBH) equal to 1.6 eV and 1.2 eV, respectively. The breakdown of Schottky diode occurs at the interface between metal and SiC.

The PiN diode shown in Fig. 1-8 provides higher breakdown voltage than Schottky barrier diode. With a built-in potential of 2.7 eV, an even lower reverse leakage current in PiN diode is obtained than in Schottky barrier diode, but higher forward voltage drop in PiN diode is not desired in some applications. Although PiN has higher forward voltage drop, Schottky barrier diode has no enough breakdown voltage.

In order to solve this dilemma, junction barrier Schottky (JBS) diode was introduced as a new device. As shown in Fig. 1-8, there are some p-type grids underneath the Schottky contact [29]. In forward operation, the Schottky contact will turn on at low voltage; in reverse bias, the p-type grids will deplete the n-drift region to provide higher breakdown voltage and lower leakage current from Schottky contact. Hence, the JBS diode does not breakdown at the Schottky contact interface, but at the boundary of pn junction.

Different JBS diodes have been proposed to ease the process of p-type dopant activation or to improve the performances of JBS diodes with the same basic theory,

like dual-metal trench Schottky diode and MOS trenched Schottky barrier diode [28]. As shown in Fig. 1-9, by etching SiC substrate first, these trenches are filled with high work-function metal or fabricated as trenched MOS capacitor [28]. Both of the devices deplete n-drift region under reverse bias similar to the p-type grids in JBS diode.

The trench junction barrier Schottky barrier (TJBS) diode is shown in Fig.1-10 [30]. TJBS diode is expected to provide more on-current from the sidewall of Schottky contact than JBS, and maintain the same breakdown voltage as JBS. Here, we simulate the TJBS structure in Sentaurus TCAD. We expect to figure out the design guidelines of TJBS.

1-6 Thesis Organization

The first chapter includes the introduction of history of power devices, wide bandgap materials, and fundamentals of SiC crystals. Different structures of SiC-based power devices are introduced briefly. The importance in the quality of epilayers of SiC and different characterization technologies of epilayer-quality are discussed. The next chapter exhibits the theory and setup of DLTS system. Verifications of DLTS system are also resented. Sample preparations of DLTS measurement and results of different treatment are also discussed.

Then, the third chapter contains the simulation of new structures of TJBS and geometric parameters, forward current characteristics, and breakdown voltage compared to JBS. Finally, we will summarize the design guidelines of TJBS. The last chapter is conclusions and suggested future works.

Table 1-1 Physical characteristics of Si and main wide bandgap semiconductor [11]. $\varepsilon = \varepsilon_r \cdot \varepsilon_0$, where $\varepsilon_0 = 8.85 \cdot 10^{-14}$ F/cm

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap, E_g (eV)	**1.12**	**1.43**	**3.03**	**3.26**	**3.45**	**5.45**
Dielectric constant ε_r	**11.9**	**13.1**	**9.66**	**10.1**	**9**	**5.5**
Electric Breakdown Field, E_c (MV/cm)	**0.3**	**0.4**	**2.5**	**2.2**	**2**	**10**
Electron Mobility, μ_n (cm^2/V-sec)	**1500**	**8500**	**// c-axis:80 ⊥c-axis:500**	**1000**	**1250**	**2200**
Hole Mobility, μ_p (cm^2/V-sec)	**600**	**400**	**101**	**115**	**850**	**850**
Thermal Conductivity, λ (W/cm-K)	**1.5**	**0.46**	**4.9**	**4.9**	**1.3**	**22**
Saturated Electron Drift Velocity (x10^7 cm/s)	**1**	**1**	**2**	**2**	**2.2**	**2.7**

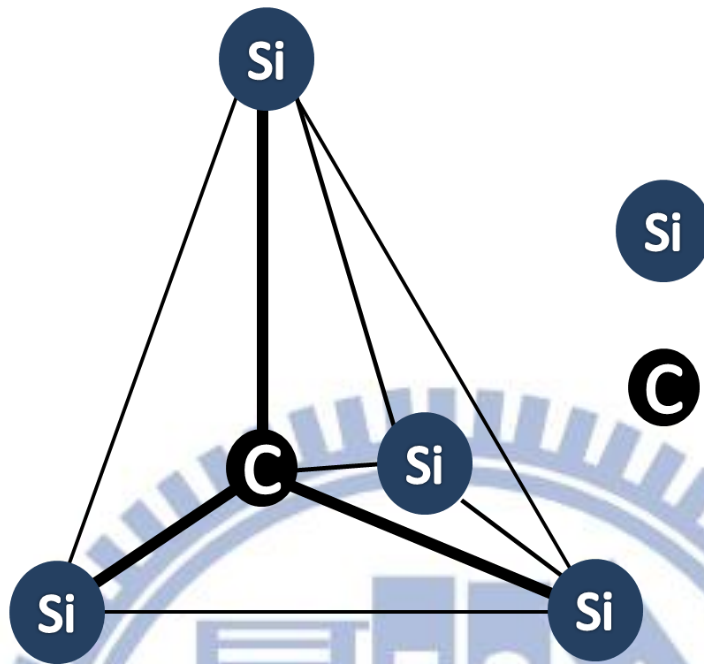


Fig.1-1 In SiC, silicon atom is covalently bonded with 4 carbon atoms in the tetrahedral arrangement [13].

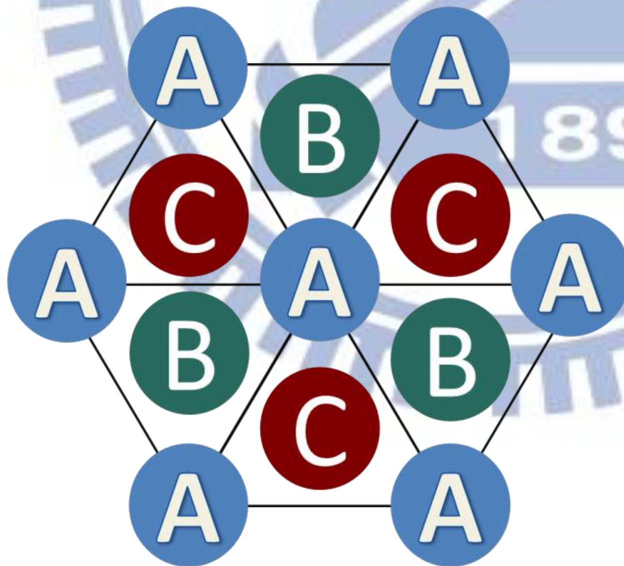


Fig.1-2 Three possible suited positions for hexagonal structure [14].

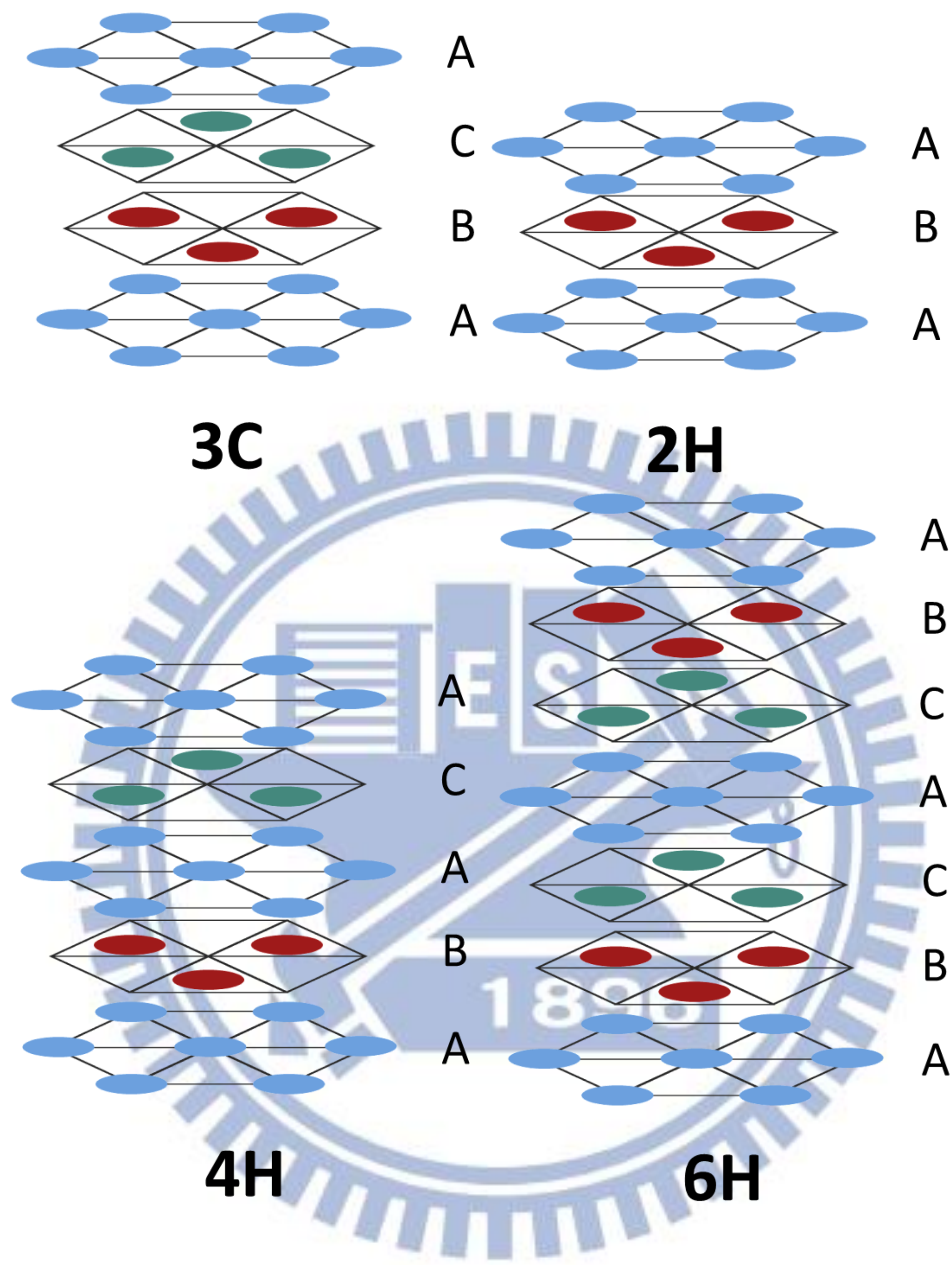


Fig.1-3 Common prototypes of SiC with different stacking orders [14]

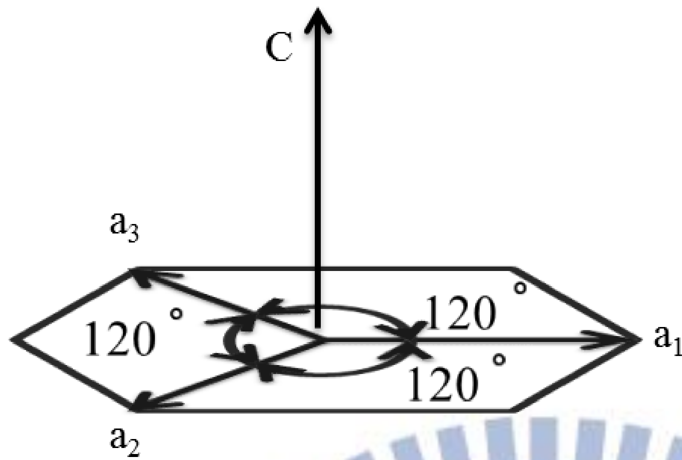


Fig.1-4 Four Miller Indices (a_1 a_2 a_3 c) in hexagonal structure [14].

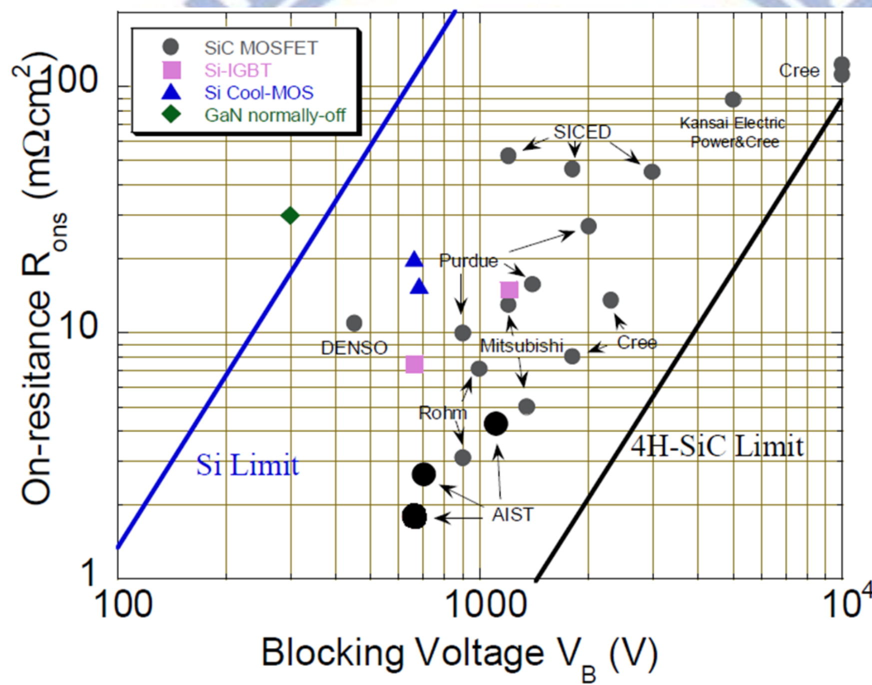
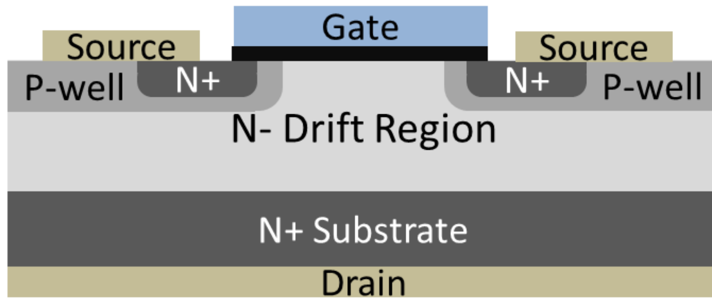
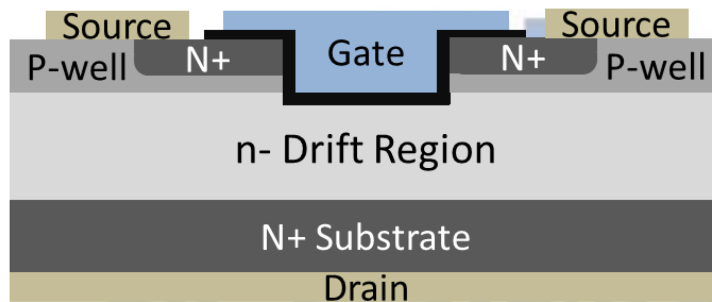
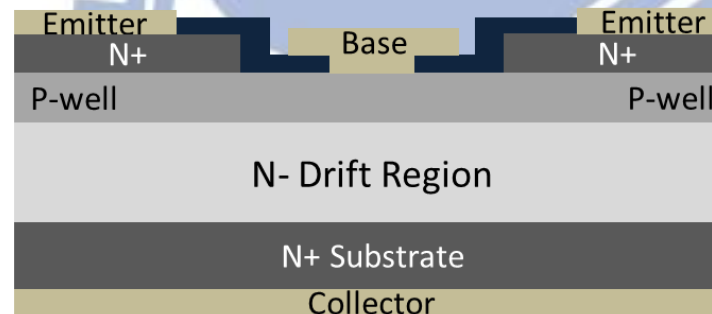


Fig.1-5 Comparison of unipolar limit of specific on-resistance versus blocking voltage for some device types in Si and SiC [15].







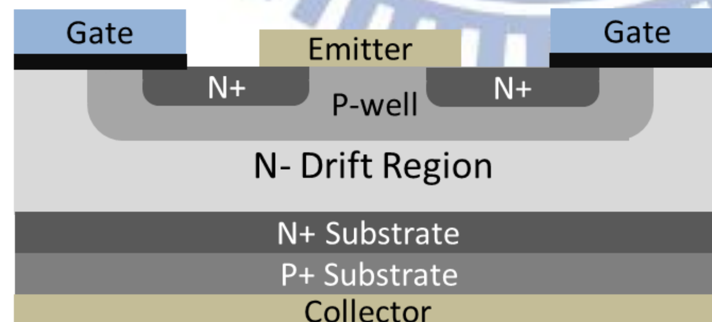


Fig.1-6 Cross section schematic of VDMOSFET, UMOSFET, BJT, IGBT [16, 17].

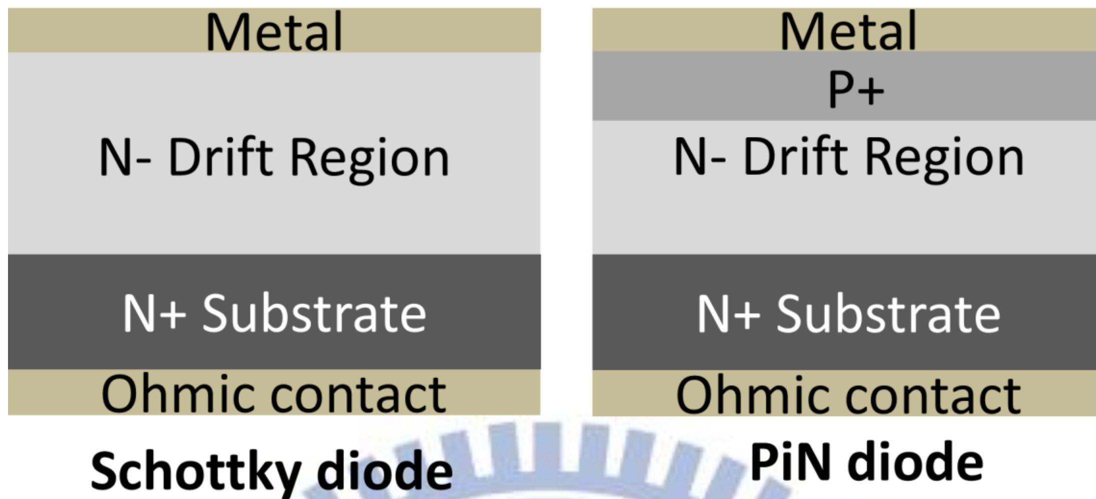


Fig. 1-7 Cross section schematics of Schottky diode and PiN diode in vertical structure

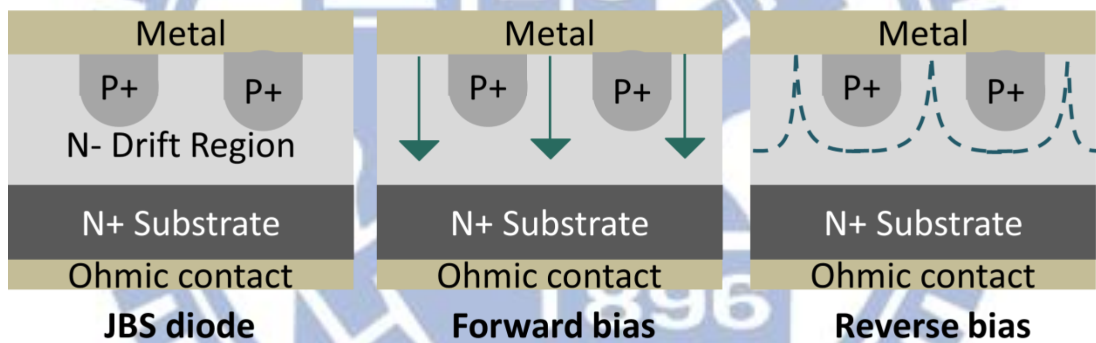


Fig. 1-8 Cross section schematics of junction barrier diode (JBS). In forward bias, the Schottky contact will turn on at low voltage; in reverse bias, the p-type grids will deplete n-drift region to provide higher breakdown voltage and smaller leakage [28].

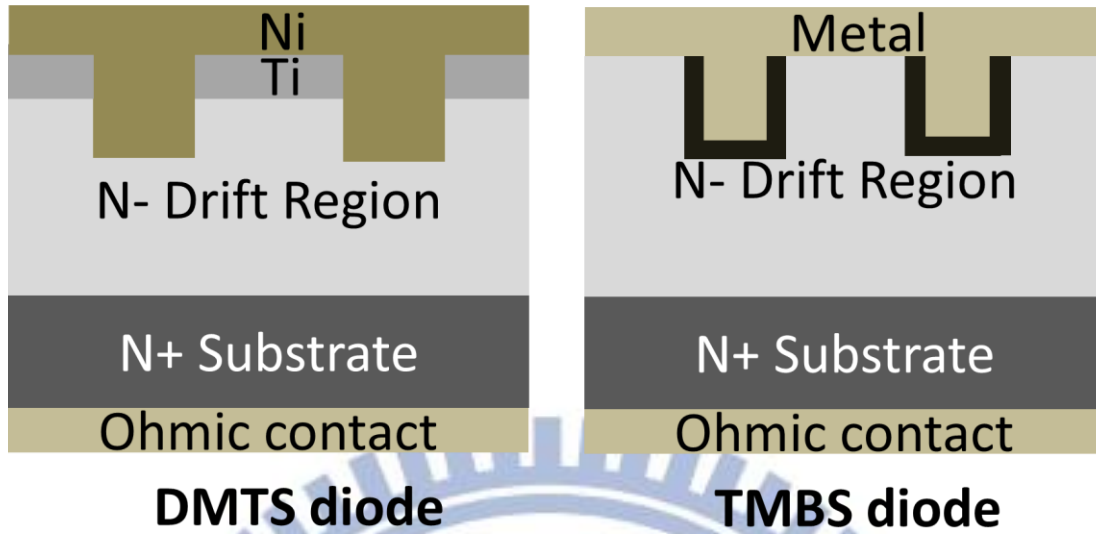


Fig. 1-9 Dual-metal trenched Schottky diode (DMTS) with two different metals to achieve and trenched MOS barrier Schottky diode (TMBS) with MOS structure are introduced by the same basic theory of JBS [28].

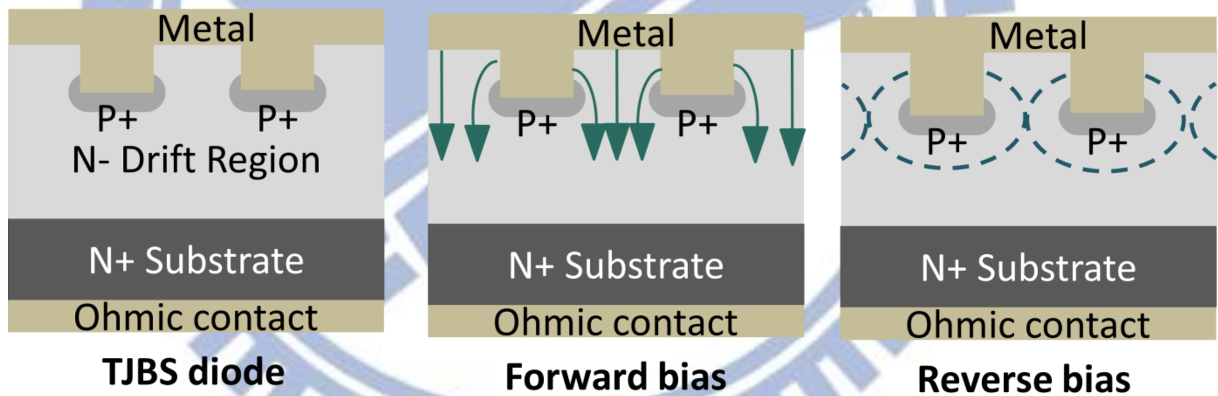


Fig. 1-10 Device configuration of trenched junction barrier Schottky diode (TJBS) [30]. In forward bias, the Schottky contact will turn on at low voltage,and sidewall of schoottky diode can provide more on-current to lower down its on-resistance; in reverse bias, the p-type grids will deplete n-drift region to maintain breakdown voltage and smaller leakage

Chapter 2

Defects in 4H-SiC by deep level transient spectroscopy

2.1 Introduction to deep level transient spectroscopy (DLTS)

Deep level transient spectroscopy (DLTS) is a defect detection technique, which was first proposed by D. V. Lang in 1974 [31]. DLTS is a capacitance transient spectroscopy and it can acquire more information effectively than traditional defect detection techniques [32].

The concept of DLTS is on the bases of the change in capacitance of depletion region in a pn diode or Schottky diode [31, 33]. The operation principle is shown in Fig. 2-1. First, the diode is kept at a reverse bias V_R to empty electrons in depletion region. Second, the device is pulsed with a voltage V_P, so the depletion region becomes very small. The change in the width of depletion region results in the change in capacitance. The original empty defects capture electrons from conduction band. Last, after pulse, the voltage across the diode returns to the reverse bias V_R. The free majority carrier can responds the bias soon, but the trapped electron cannot. Hence, the depletion region would be wider than its original width to compensate the trapped electrons, which corresponds to a smaller junction capacitance. The trapped electrons will emit from defects eventually, so the depletion region will be back to steady state as well as the junction capacitance [33].

The transient capacitance is a function of time as expressed in eq. (2-1) [33]. According to eq. (2-2), by selecting two different time points t_1 and t_2, in a transient capacitance, we can calculate the capacitance difference, δC, between t_1 and t_2.

$$C(t) = C_0\left[1 - \frac{n_T}{2N_D}\exp(-\frac{t}{\tau_e})\right],$$ eq. (2-1)

$$\delta C = C(t_1) - C(t_2) = \frac{n_T}{2N_D}C_0\left\{\exp\left(-\frac{t_2}{\tau_e}\right) - \exp(-\frac{t_1}{\tau_e})\right\},$$ eq. (2-2)

where C_0 is the capacitance in steady state, n_T is the defect concentration (cm^{-3}), N_D is the donor concentration (cm^{-3}), τ_e is the emission time of the trapped electron (s), and t is the time passed (s).

The emission time of trapped electron depends on the depth of the energy level from band edge and the temperature during measurement as shown in eq. (2-3). In Fig. 2-2, if the temperature is low, the change of capacitance will be very slow, so the δC will be very small; at high temperature, the emission time of the trapped electron is short and the change of capacitance will be very fast, so the δC will be very small, too. Consequently, at proper temperature T_1, δC will reach its maximum value [33]. By differentiating eq. (2-3) to τ_e, we can get the relation of τ_e between t_1 and t_2 as expressed by eq. (2-4). With eq. (2-4) and proper temperature T_1, we can get the energy level and the capture cross section of the traps from eq. (2-3).

$$\tau_e = \frac{\exp((E_C - E_T)/kT)}{\gamma_n \sigma_n T^2},$$ eq. (2-3)

$$\tau_{e,max} = \frac{t_2 - t_1}{\ln(t_2/t_1)},$$ eq. (2-4)

where τ_e is the emission time of trapped electron (s), E_C is the conduction band energy (eV), E_T is the energy of the deep trap in bandgap (eV), k is the Boltzmann constant, T is the temperature in Kelvin, γ_n is a constant ($cm^{-2} \cdot s^{-1} \cdot T^{-2}$), and σ_n is the capture cross section (cm^2).

As mentioned above, we can acquire the deep trap level and capture cross section from the DLTS effectively [31]. Since the introduction of DLTS in 1974, many improvements have been proposed, like lock-in amplifier DLTS, CCDLTS, Correction DLTS, isothermal DLTS, and Laplace DLTS [33]. Here, we established a conventional

DLTS system.

2.2 Setup of DLTS system

In order to detect the defects in the 4H-SiC epi-layer and the traps after ion implantation and dopant activation processes, we establish a conventional DLTS system. The DLTS system requires two basic elements: transient capacitance meter (C-t meter) and temperature controller [31].

The C-t meter in our DLTS system is a multi-frequency capacitance measurement unit of module B1520A appended in the Agilent B1500A semiconductor device parameter analyzer. The specifications of the C-t function of the B1520A are listed in Table 2-1 [34]. Measurements are conducted in a probe station of model Lake Shore CPX-VF with a temperature controller. The probe station can be vacuumed to about 10^{-5} torr to avoid the condensation of moisture and residual gases. The temperature of chuck can be cooled down to 77 K by liquid N_2 circulation and be raised with regular ramping rate to 400 K by temperature heating controller.

Computer program written in HT BAISC language controls the B1520A and the temperature controller simultaneously [35, 36]. The algorism of the program is presented in Fig. 2-3. First, the chuck is cooled down to 77 K and maintaining at 77 K for 20 minutes with probing on device. After setting measurement conditions in program, the measurement procedure starts. During the Capacitance-time-temperature (C-t-T) measurement, the program will acquire the temperature of chuck firstly. Then, the program will invoke the B1520A to execute a C-t measurement and return the data to computer. By repeat these two steps, the C-t-T measurement are done till the temperature of chuck researches 400 K. By changing t_1 and t_2 according to eq. (2-4), we can get different τ_e to shift the positions of peaks on temperature axis as shown in

Fig. 2-4. Then, we can draw the "$\ln(\tau_e T^2) - 1/kT$" plot [33]. From the slope of the linear regression line, we can obtain the energy of the traps, and from the interception on y-axis, we can obtain the capture cross section [33].

2.3 Verifications of DLTS system

To verify our DLTS system, the same sample was measured by our DLTS system and by a commercial purchased DLTS system. The commercial DLTS system is provided by the Sula Technologies Co. and was installed in Professor J. F. Chen's lab in the Department of Electrophysics of National Chiao Tung University. The sample used here is sample IA. The process flow will be introduced in next section. Only substrate defect is observed on sample IA from the DLTS result.

Fig. 2-5 shows the DLTS results measured by the commercial DLTS system and our system. For the same emission time constant, the signal peak occurs at the same temperature. The large signal intensity difference comes from the relatively slow sampling rate of the B1520A. As shown in Fig. 2-6, the selection in different time points will have the same time emission constant but different δC. The shortest sampling rate of the commercial DLTS system is less than 100 μs [37]. This system selects time points automatically according to the specified emission time constant, but the actually time points are unknown. For our DLTS system, the actually time points is known. However, the relatively slow sampling rate of the B1520A, 10ms, is the main reason for the large difference in signal intensity. The signal intensity doesn't affect the temperature position of peak, so the function of our DLTS system is verified.

2.4 Sample fabrication for DLTS measurements

2.4.1 Ni/SiC Schottky barrier diode

The starting material is a 4-inch (0 0 0 -1)-oriented n-type 4H-SiC substrate with a 5-µm-thick epi-layer purchased from Cree. The substrate is doped by nitrogen to a concentration of $5x10^{18}$ cm^{-3}. The nitrogen concentration N_D in the epi-layer is equal to 10^{15} cm^{-3}. The 4H-SiC wafer was cut into small pieces. These samples were cleaned by standard RCA clean process and followed by different treatments as summarized in Table 2-2. These are four kinds of treatments. They are wet oxidation (W), nitrogen ion implantation (I), N_2 annealing (N), and 1600^oC high temperature activation (A). The sample ID indicates the composition of these treatments. For example, sample IN indicates that the sample receives nitrogen ion implantation and N_2 annealing. The samples experienced 1600 ^oC annealing were capped with carbon layer before annealing to avoid Si sublimation. The carbon layer was removed by a 900 ^oC oxidation for 1 hour in O_2 ambient. Before depositing PECVD oxide as field oxide, all the substrates were cleaned by SPM (H_2SO_4:H_2O_2 = 3:1) and dipped by diluted HF. A 100-nm-thick Ni and a 10-nm-thick TiN were sputtered at samples' backside followed by a 1000^oC RTA for 30s to form backside ohmic contact. Then, contact holes were defined by conventional lithography process and the field oxide was etched by BOE. The Schottky metal of 10-nm-thick Ni was deposited by a sputtering system. Samples were immediately loaded into a thermal coater within 5 min to evaporate a 300-nm-thick Al as electrode. Finally, the residual metal was removed by a lift-off process. The schematic structure of the Ni/SiC Schottky barrier diode (SBD) is shown in Fig. 2-7.

2.4.1 SiC MOS capacitor

Metal-oxide-semiconductor (MOS) capacitors were fabricated on the same 4H-SiC epi-wafer. After standard RCA clean, some samples were implanted by nitrogen at 200 keV to a dose of 10^{11} cm^{-2}. After ion implantation, samples were cleaned by RCA clean process again and followed by 1050 ^oC wet oxidation for 5 hr. Some samples received NH_3 plasma treatment for 5 min to reduce the interface states (D_{it}) [38]. The main process conditions for the MOS capacitors are summarized in Table 2-3. There are for process steps: wet oxidation (W), nitrogen ion implantation (I), NH_3 plasma treatment (P), and high temperature activation (A). Aluminum was deposited by thermal evaporation and patterned by lithography and wet etching to form gate electrode. The backside of wafer was cleaned by BOE and followed by Al deposition as backside contact. All the samples were sintered at 400 ^oC for 30 min in N_2 ambient. The schematic structure of the SiC MOS capacitor is shown in Fig. 2-8.

2.5 Ni/SiC Schottky barrier diode

2.5.1 Current - voltage characteristics

The I-V characteristics of the Ni/4H-SiC Schottky barrier diode (SBD) fabricated with different processes as listed in Table 2-2 are shown in Fig. 2-9. The reference sample shows ideal SBD characteristics. The Schottky barrier height is 1.5 eV and the ideality factor is 1.12. For the ion implanted samples, I, IN, and IW, the distorted I-V curves and low forward current at 3 V are observed at forward bias. If we raising the measurement temperature, kink phenomenon occurs and the forward current increases to normal value at high forward bias as shown in Fig. 2-10 ~ Fig. 2-12. This observation can be explained by a two energy barriers model - one is the Schottky barrier and the other one comes from the damaged region formed by ion implantation.

The raising of forward bias bends the energy band gradually so that electrons can overcome the two barriers sequentially. The kink indicates electron overcomes the potential barrier due to the high-low junction. As the measurement temperature becomes higher, electron can overcome the barrier easier by thermionic emission. Hence, the kink phenomenon fades out and the cut-in voltage drops due to higher temperature. The other phenomenon like higher resistance is electrons suffers from more phonon scattering at higher temperature [39].

Sample IA has the same forward current at 3 V as the reference sample, but kink phenomenon is observed at lower voltage. Because the reverse current increases apparently, it is suspected that there are two Schottky barrier heights at the Ni/SiC contact. From thermionic emission equation [39], the two extracted Schottky barrier heights are 0.6 eV and 1.3 eV. The low Schottky barrier may be originated from the surface local defects induced by ion implantation and activation [40]. Fig. 2-13 and Fig. 2-14 shows the cross sectional TEM micrographs of sample I and sample IA, and much poorer surface morphology is observed on sample IA which is corresponding to the double barrier. The high Schottky barrier height is lower than the Schottky barrier of the reference sample. During the epi-layer growth of SiC, the gas flow ratio of C/Si has direct impact on the Schottky barrier height [41]. The lower the C/Si ratio is, the lower the Shcottky barrier height is. This implies more carbon vacancy in SiC under the lower C/Si ratio condition. Because of the generation of carbon vacancy after high temperature, a relatively lower Schottky barrier is measured in sample IA compared to the reference sample [42].

2.5.2 Capacitance - voltage characteristics

The C-V characteristics of all samples are shown in Fig. 2-15. The reference sample shows the largest junction capacitance, but for samples I, IN, and IW, relatively low capacitance was measured. Because of the ion implantation damage, the damaged region is easily depleted so the total junction capacitance is much lower than the reference sample. As for sample IA, the 1600 ^{o}C annealing activates the nitrogen from ion implantation, so the effective N_D at the surface region may be slightly higher than original N_D as observed in Fig.2-16. Theoretically, the capacitance should be larger due to the higher N_D, but the result is opposite. The relatively low Schottky barrier height and surface defects may be the reason for the lower capacitance compared to the reference sample.

2.5.3 DLTS results of Ni/SiC Schottky barrier diode

The DLTS measurement conditions are listed in Table 2-4. Sample IA has different measurement condition because of the smaller turn-on voltage due to its relatively low Schottky barrier height. This measurement condition can reflect the change in depletion width clearly.

The DLTS of reference sample is shown in Fig. 2-17. There is no significant signal compared to the DLTS of sample I shown in Fig. 2-18. The DLTS of sample I has distinct signals at 270 K and 370 K obviously. These signals are too broad to result from a single trap. It's impossible to identify the trap energy because the severe overlap of signals. Different pulse voltages (V_P) of sample I have similar results. The slightly difference in signal intensity comes from the difference in depletion width at different V_P, so different amounts of traps can be detected. Besides, if the V_P becomes

higher, the edge of the depletion region becomes closer to the surface of substrate. The spatial distribution of defect can be detected.

In order to eliminate the ion implantation induced defects in the 4H-SiC epi-layer, post implantation annealing was conducted. Annealing at 1050 ^{o}C for 5 hour in N_2 or O_2 ambient was performed for defect recovery. Some defects can be annihilated by thermal annealing and oxidation [43]. In order to avoid defects generation during oxidation, DLTS of sample W was also measured and the result is shown in Fig. 2-19. No significant signal is observed. As the results in Fig 2-20 and Fig 2-21, the DLTS of sample IN and sample IW still have obvious signals. Even they are distinct to be identified, but all of them are still too broad to be considered as a single trap. For V_P = 1 V, both of the samples IN and IW have almost identical spectra, which represents the same defects. While V_P = 2 V, a new signal appears at 170 K, which is located spatially near the SiC surface. We can distinguish it barely composed of two traps ID_4 and ID_8 with activation energies E_C-0.37 eV and E_C-0.45 eV, respectively [44]. As to the extra peak at 300 K in the DLTS of sample IW, it's a single trap S2 with activation energy E_C-0.70 eV [45]. In the DLTS of sample IN and sample IW, the other un-discussed signals are still too broad to be a single trap, and are hard to be distinguished.

The DLTS result of sample IA is shown in Fig 2-22, almost all traps are vanished, and only one trap, known as $Z_{1/2}$ with activation energy E_C-0.60eV, is observed [44]. High temperature annealing is effective in reducing defects, but in the meanwhile it could generate large amount of $Z_{1/2}$ trap [42]. By drawing the $\ln(\tau_e T^2) - 1/kT$ plot, activation energy and capture cross section can be extracted from the slope and interception on y-axis, respectively. The extracted results are shown in Fig. 2-23.

On sample I, traps ID_4 and ID_8 are not obvious, but after 1050 ^{o}C annealing they become distinct. During 1050 ^{o}C annealing, some defects may be mobile and migrate

together to form stable structural defects. Oxidation of SiC will form carbon interstitial (C_i) [46]. Some C_i will pile up at the interface between SiO_2 and SiC, which leads to large amount of D_{it}, and some C_i will diffuse into the substrate [46, 47]. From previous study, the trap S2 is a complex of C_i, so the appearance of trap S2 in sample IW near SiC surface is reasonable [45]. After 1600 ^oC annealing, the trap $Z_{1/2}$ shows up, which corresponds to carbon vacancy (V_c) [42]. The origin of $Z_{1/2}$ in the epi-layer may diffuse from the n^+ SiC substrate where high concentration of V_C presents [42]. The $Z_{1/2}$ traps can be reduced by thermal oxidation or carbon implantation to improve the quality of epi-layers [42, 46].

2.6 SiC MOS capacitor

2.6.1 Capacitance – voltage characteristics

The high frequency and quasi-static C-V curves of SiC MOS capacitors are shown from Fig. 2-24 to Fig. 2-27. Expect for the sample IP, the D_{it} extracted by the high-low frequency method are shown in Fig. 2-28 [38]. It can be observed that the samples with NH_3 plasma treatment have lower D_{it} than the sample without plasma treatment [38]. As to the sample IP, ion implantation produces an damaged region as mentioned before. According to previous study, the MOS capacitor fabricated on high resistive substrate suffers from seriously series resistance [48]. As shown in Fig. 2-29, the equivalent circuit has to be modified to accommodate the frequency dependence. With the presence of highly resistive substrate, the measured accumulation capacitance at high frequency is relatively small to the capacitance of oxide, whereas the accumulation capacitance at low frequency is not affected [48]. Fig.2-30 shows the simulated and measured C-V curves from previous study which matches our observation on sample I [48].

For C-V characteristics over temperatures, since sample IP exhibits abnormal C-V characteristic, it is not discussed here. A large flat band voltage shift can be observed on the rest samples as shown from Figs. 2-31, 3-32, and 3-33, flat band voltage shift is originated from the large amount of D_{it} [47]. At high temperature, the traps are capable of emitting the trapped electrons by thermal emission, and the response is fast enough to follow the gate voltage sweep. At low temperature, the same traps are unable to thermally emit their captured electrons within the time frame of the measurement, so that the trapped charge is frozen in. These trapped electrons at D_{it} in all the samples make the flat band voltage shift.

2.6.2 DLTS results of SiC MOS capacitor

The DLTS measurements are performed on the SiC MOS capacitors. There are three types of traps can be identified by DLTS as shown in Fig. 2-34. They are substrate defect, interface state (D_{it}), and oxide trap [49]. It's relatively easy to distinguish substrate defect from the other trap, because substrate defect does not distribute continuously in the bandgap. The D_{it} and oxide trap are continuously distributed in the bandgap so that both of them result in broader DLTS signals. Oxide trap has relatively slow emission time constant and the time constant depends on electric field in the gate dielectric [49]. The signal intensity of substrate defect and D_{it} will saturate as the V_P increasing due to the limited defect density of them near surface. For oxide trap, the signal intensity keeps increasing, because more electrons are trapped deeper into the dielectric [54]. Dipole-like relaxation will result in opposite transient capacitance as shown in Fig. 2-35 [50]. The dipoles will be arranged during the pulse, and become disordered during the measurement, so the transient capacitance will decrease gradually.

SiC MOS capacitors with different processes listed in Table 2-3 were fabricated. Because of different flat band voltages on different samples, the parameters of DLTS measurement are varied for different samples as listed in Table 2-5. The V_p was adjusted so that the electric field in dielectrics are the same. Because of the flat band voltage shift at low temperature, the larger V_P was applied to make sure all the D_{it} will be measured.

In Fig. 2-36, the DLTS of sample W exhibits a continuous signal. The intensity of signal increases and the peak position changes as V_P increasing. Only oxide trap exhibits the behavior with the dependence with applied voltage. For V_P = 5.5 V, the dipole-like relaxation becomes obvious. Because at high temperature the de-trapping of electron becomes very fast, the transient capacitance due to electron de-trapping is too fast to be measured, so the relatively slow dipole-like relaxation becomes the dominant phenomenon. At higher V_P, it will induce more dipoles, so the dipole-like relaxation becomes more obvious. If applying eq. (2-5) to transform the DLTS result to the corresponding D_{it}, the D_{it} extracted from DLTS is much higher than that extracted from the high-low frequency method as shown in Fig. 2-37 [26]. Because of the presence of oxide trap, the D_{it} extracted from DLTS includes oxide trap and D_{it}, and we cannot separate them apart from the DLTS signal. The DLTS of sample P as shown in Fig.2-38 shows similar V_P dependence as that on sample W, and oxide trap signal dominates the entire DLTS. The D_{it} extracted from DLTS is also higher than that extracted from the high-low frequency method as shown in Fig.2-39.

$$E_{it} = E_C - kT\,ln\left\{\frac{\gamma_n \sigma_n T^2 (t_2 - t_1)}{ln(t_2/t_1)}\right\}, \quad D_{it} = -\frac{\varepsilon_r \varepsilon_0 N_D C_{OX}}{kTC_{t_1}^3 \ln(t_2/t_1)}, \qquad \text{eq. (2-5) [26]}$$

where E_{it} is the energy level below conduction band (eV), ε_r is the dielectric constant of SiC, ε_0 is the vacuum permittivity (F/cm), C_{t1} is the transient capacitance at time point t_1 (F/cm^2).

Sample IP has a high resistance damaged layer due to ion implantation induced damages. In Fig. 2-40, the DLTS of sample IP shows three peaks as the V_P increases from 3 V to 8 V. More electrons are trapped, so the signal becomes more obvious. The DLTS theory is based on the change in depletion width [31]. It should be noted that only the traps above Fermi level can be detected, because the trapped electrons are hard to be emitted [52]. If we change the V_R, the DLTS signal becomes weak, because the depletion region is not dominated by the damaged region. Instead, the un-damaged epi-layer dominates the most of depletion, so the δC will be very small. Hence, we redraw it in Fig. 2-41, and a peak is observed at 370 K compared to V_R = 0 V. The DLTS of the MOS capacitor sample IP and the SBD sample IW exhibit the same signal at the same temperature position which matches to each other very well.

Sample IAP was annealed at 1600 ^oC to repair the lattice damages and to activate dopants. In Fig. 2-42 the DLTS of sample IAP is the same as that of sample W, except the peak related to substrate defect at 270 K. The substrate defect is detected on SBD sample IA, too. In Fig. 2-43, the D_{it} extracted by DLTS measurement is higher than that extracted by high-low frequency method. Besides, the D_{it} extracted by DLTS measurement is affected by substrate defect.

2.7 Summary of DLTS results

Different ion implantation damages in 4H-SiC epi-layer have been investigated by DLTS. These traps are corresponding to ID_4 and ID_8 with activation energies E_C-0.37 eV and E_C-0.45 eV, respectively. Due to severe overlap of signals, the other defects are hard to be distinguished [44]. The carbon interstitial generated from thermal oxidation induced a new trap S2 with activation energy E_C-0.70 eV [45, 46]. The carbon interstitials comes from oxidation, so the position of the S2 trap is near the

surface of substrate. The DLTS of the SBD sample IW is consistent with that of the MOS capacitor sample IP. For the 1600 ^{o}C annealed sample, both diode and capacitor have the defect $Z_{1/2}$ with activation energy E_C-0.60 eV, which is generated after higher temperature annealing [42, 44].

Oxide traps dominates the DLTS result of the MOS capacitor [49]. With the presence of oxide trap, substrate defect, and dipole-like relaxation, eq. (2-5) would result in overestimation of D_{it} in comparison with the D_{it} extracted from high-low frequency method [33, 49, 50].

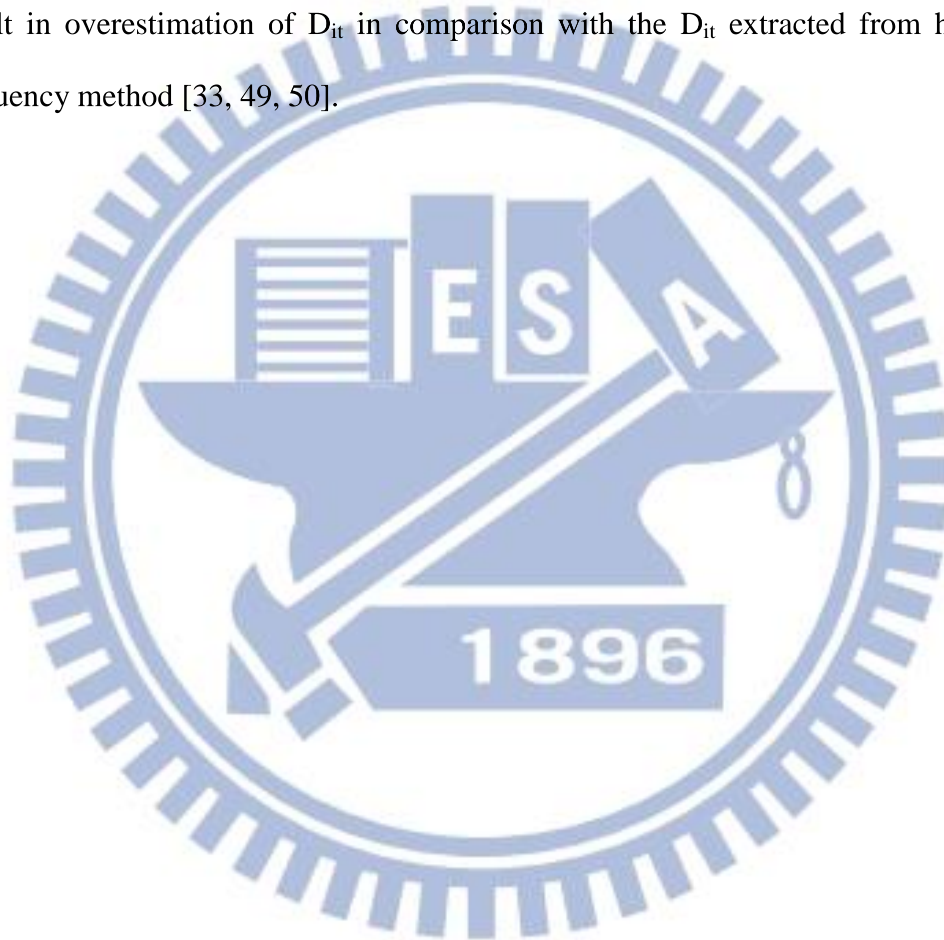


Table 2-1 Specifications of C-t function in Agilent B1500A semiconductor device parameter analyzer [34].

Frequency	1 kHz to 5 MHz
DC bias	0 V to ± 25 V
Oscillation level	10 mVrms to 250 mVrms
Pulse width	≧ 10 ms
Pulse voltage	0 V to ± 25 V
Hold time of measurement after pulse	≧ 10 ms
Sampling interval of C-t function	≧ 10 ms

Table 2-2 Main processes conditions of Ni/SiC Schottky barrier diodes.

Sample ID	Reference	W	I	IN	IW	IA
Main process			Nitrogen implantation at 200 keV to a dose 10^{11} cm^{-2}			
		wet oxidation 1050 °C 5 hr		N_2 anneal 1050 °C 5 hr	wet oxidation 1050 °C 5 hr	1600 °C 30 min anneal with carbon capping

Table 2-3 Main processes conditions of SiC MOS capacitors.

<table>
<tr><td>Sample ID</td><td>W</td><td>P</td><td>IP</td><td>IAP</td></tr>
<tr><td rowspan="4">Main process</td><td></td><td></td><td colspan="2">Nitrogen implantation at 200 keV to a dose 10^{11} cm^{-2}</td></tr>
<tr><td></td><td></td><td></td><td>1600 ^{o}C 30 min anneal with carbon capping.</td></tr>
<tr><td colspan="4">RCA and wet oxidation 1050 ^{o}C 5 hr</td></tr>
<tr><td></td><td colspan="3">NH_3 plasma treatment 150 W for 5 min</td></tr>
</table>

Table 2-4 Measurement conditions in DLTS of Ni/SiC Schottky barrier diodes. Sample IA has different turn-on voltage, so the depletion width doesn't change under the same DLTS measurement condition as the other.

<table>
<tr><td>Sample ID</td><td>Reference</td><td>W</td><td>I</td><td>IN</td><td>IW</td><td>IA</td></tr>
<tr><td>V_R</td><td colspan="5">0 V</td><td>-1 V</td></tr>
<tr><td>V_P</td><td colspan="5">1 V , 2 V</td><td>0 V, 1 V</td></tr>
<tr><td>Pulse width</td><td colspan="6">100 ms</td></tr>
</table>

Table 2-5 Measurement conditions in DLTS of SiC MOS capacitors. The V_P is depend on the V_{FB} of each sample, and all the sample have the same electric field.

<table>
<tr><td>Sample ID</td><td>W</td><td>P</td><td>IP</td><td>IAP</td></tr>
<tr><td>V_{FB}</td><td>0.3 V</td><td>0.8 V</td><td>-</td><td>1.3 V</td></tr>
<tr><td>V_R</td><td>0.0 V</td><td>0.5 V</td><td>0.0 V, -5.0V</td><td>1.0 V</td></tr>
<tr><td>V_P (fixed electric field)</td><td>0.5 V ~ 2.5 V</td><td>1.0 V ~ 2.5 V</td><td rowspan="2">3.0 V, 5.0 V, 8.0 V</td><td>1. 5 V ~ 3.0 V</td></tr>
<tr><td>V_P (sweep all bandgap)</td><td>5.5 V</td><td>5.5 V</td><td>5.5 V</td></tr>
<tr><td>Pulse width</td><td colspan="4">100 ms</td></tr>
</table>

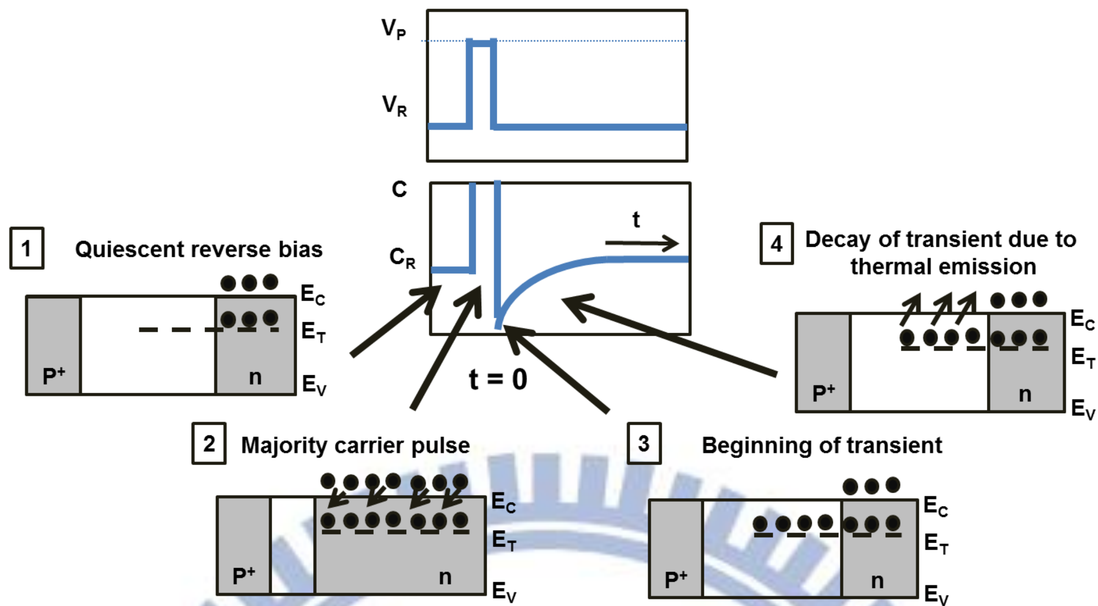


Fig. 2-1 Operation principle of DLTS: the dash line in depletion is defect.

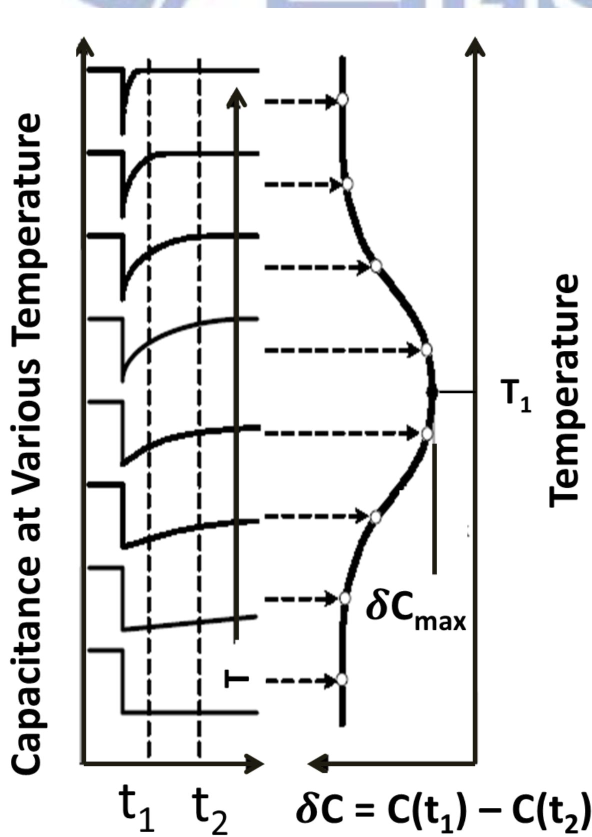


Fig. 2-2 Extraction of transient capacitance with different temperatures. Select two time points $t = t_1$ and $t = t_2$, so at proper temperature T_1 the δC will be maximum.

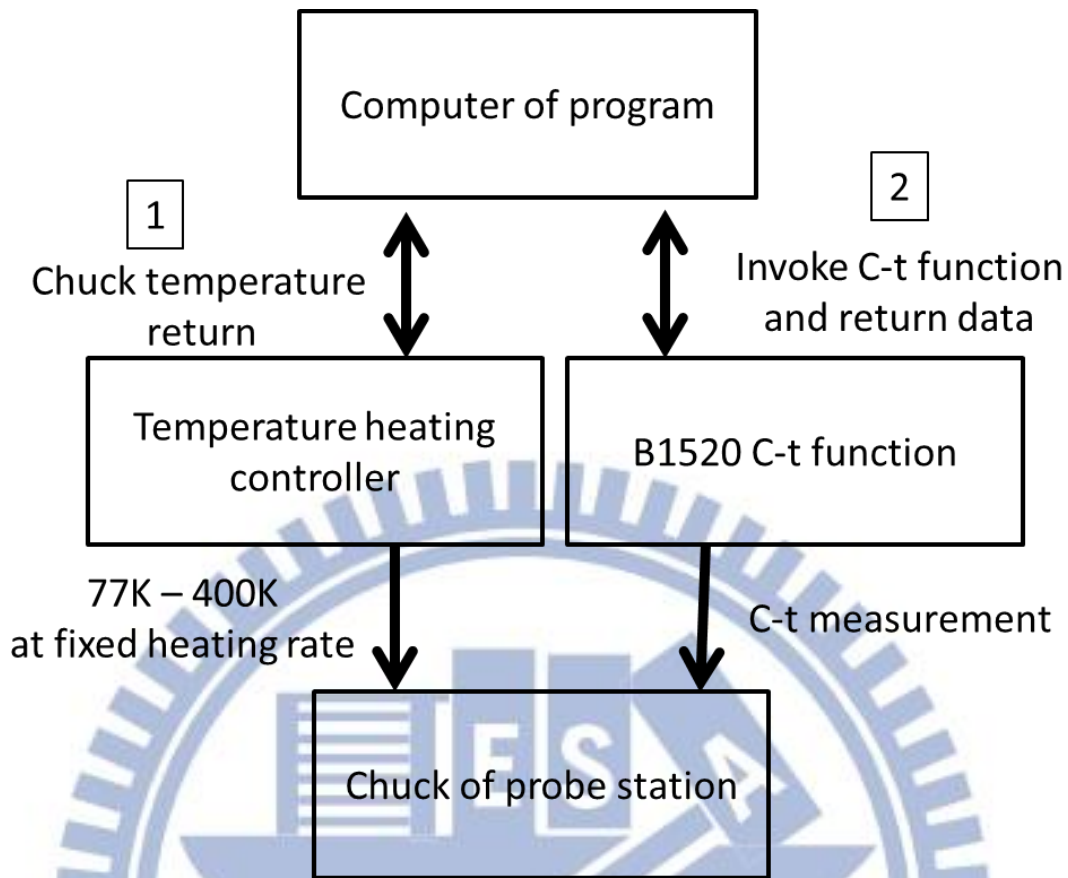


Fig. 2-3 Capacitance-time-Temperature measurement flow: *1*. Check the temperature of chunk *2*. Invoke C-t measurement.

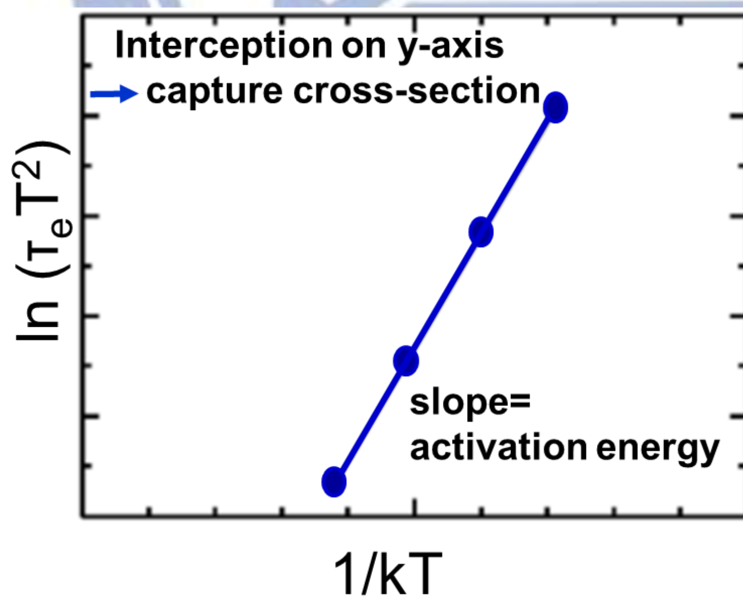


Fig. 2-4 "ln($\tau_e T^2$) – 1/kT" plot. From the slope of regression line, we can get energy of trap, and from the interception on y-axis, we can obtain the capture cross section.

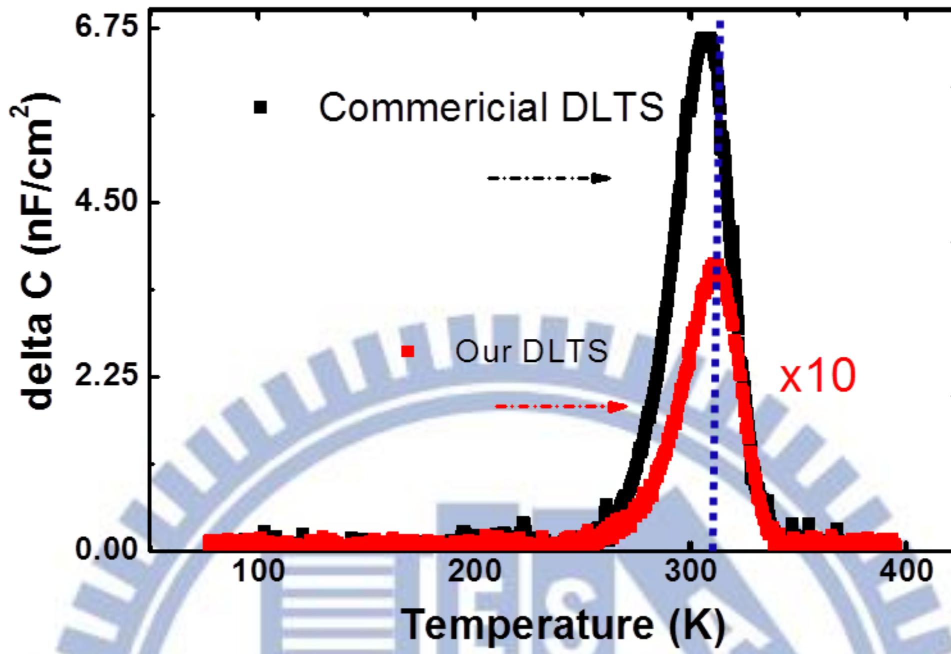
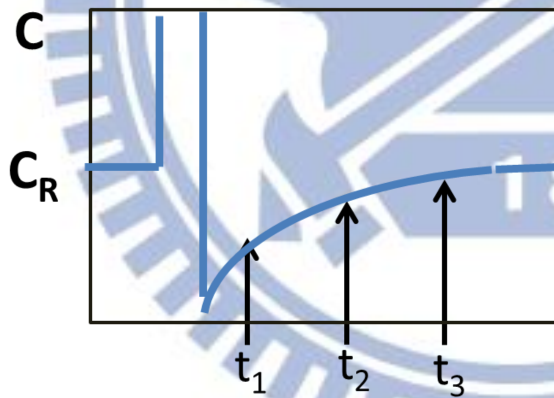


Fig. 2-5 Measured DLTS of commercial DLTS system and our DLTS system.



$$\tau_e = \frac{t_3 - t_1}{\ln(t_3/t_1)} = \frac{t_3 - t_2}{\ln(t_3/t_2)}$$

$$C_{t_3} - C_{t_1} > C_{t_3} - C_{t_2}$$

Fig. 2-6 Schematic of different sampling time has the same emission time constant.

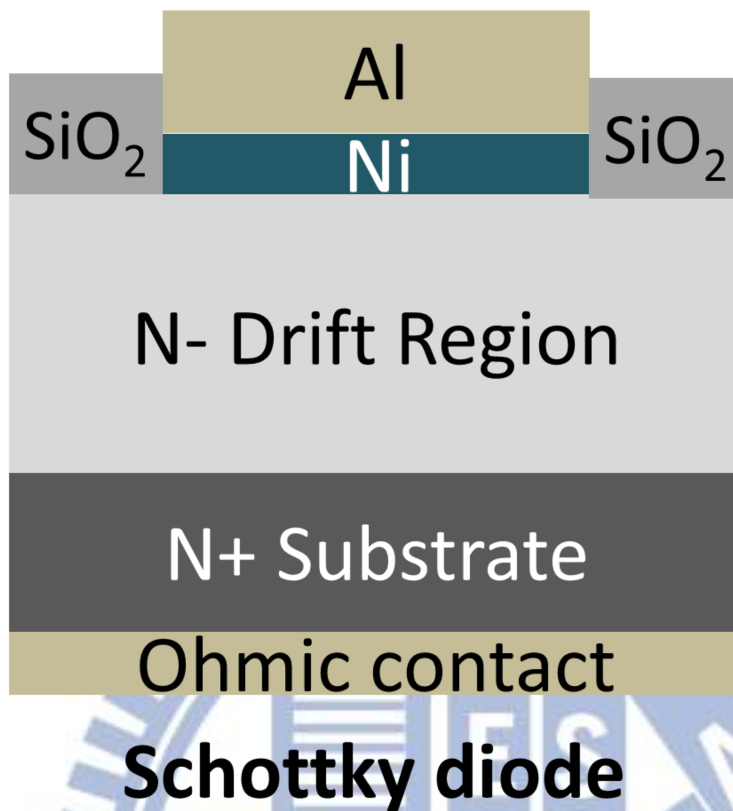


Fig. 2-7 Configuration of Ni/SiC Schottky barrier diode (SBD)

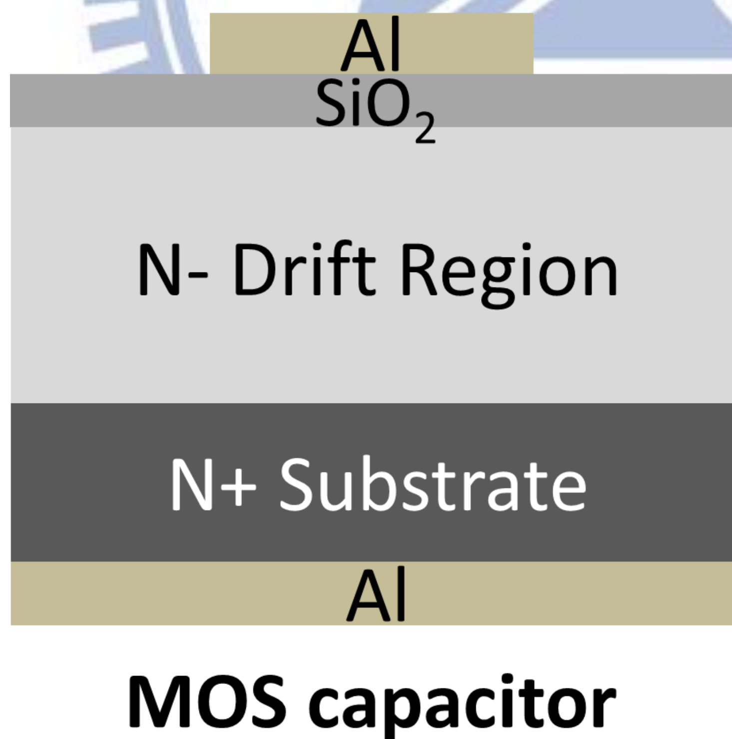


Fig. 2-8 Configuration of SiC MOS capacitor

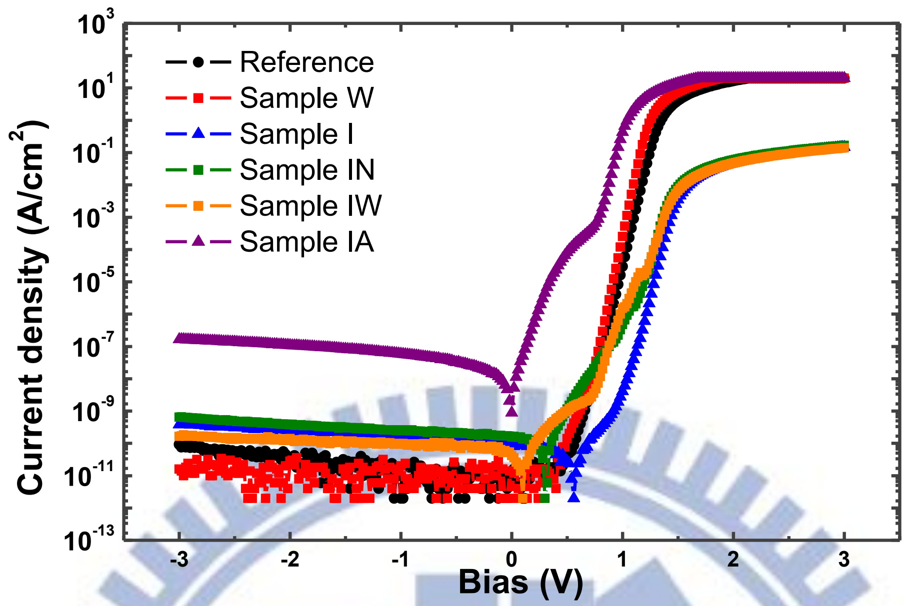


Fig. 2-9 Current-voltage characteristics of Ni/4H-SiC SBD fabricated on different processed epi-layers

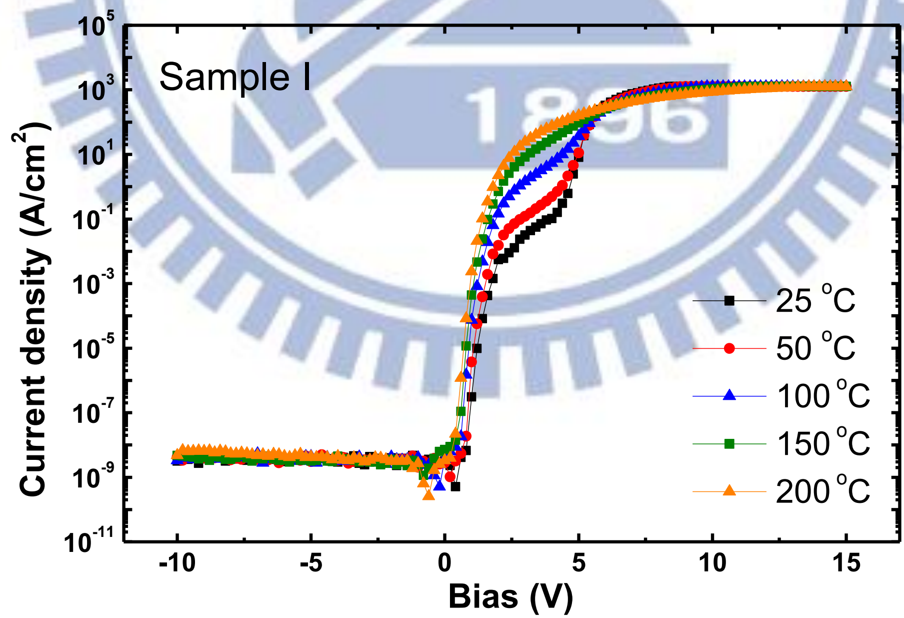


Fig. 2-10 Current-voltage characteristics over temperature characteristics of Ni/4H-SiC SBD sample I with ion implantation

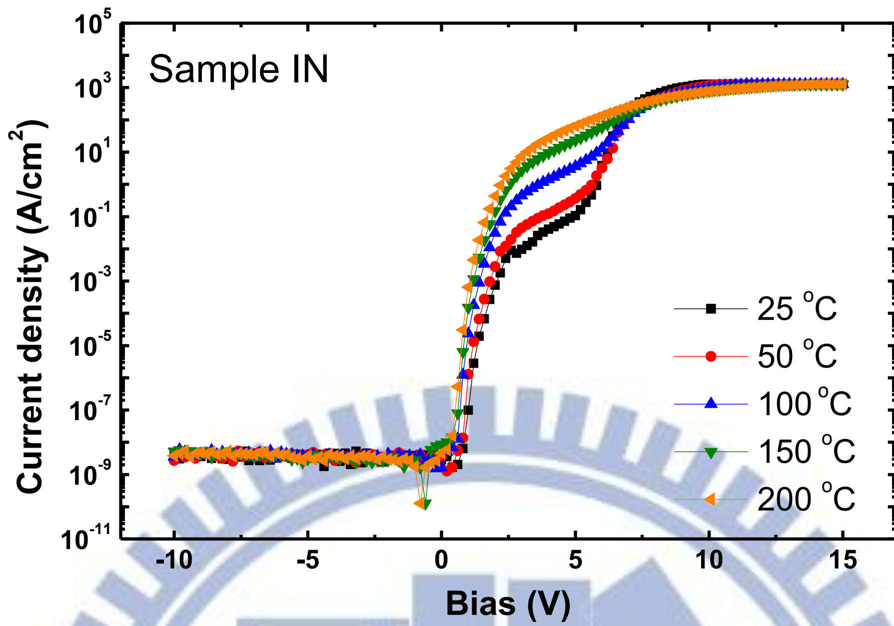


Fig. 2-11 Current-voltage over temperature characteristics of Ni/4H-SiC SBD sample IN with ion implantation and 1050 °C N_2 annealing

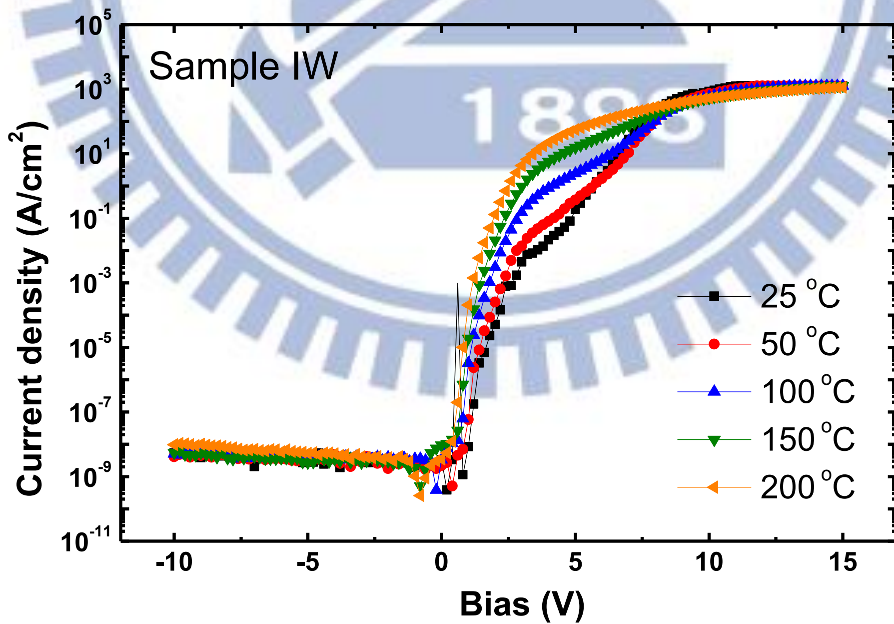
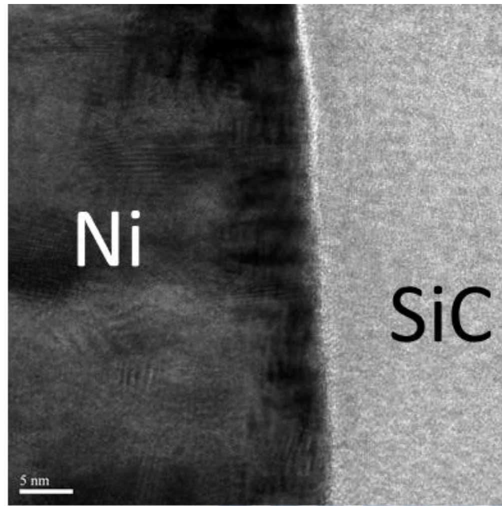
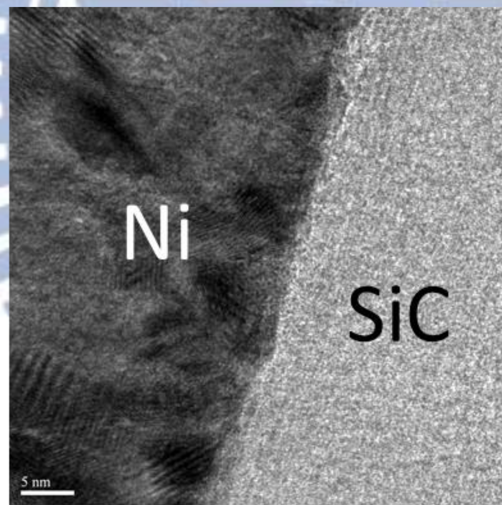


Fig. 2-12 Current-voltage over temperature characteristics of Ni/4H-SiC SBD sample IW with ion implantation and 1050 °C wet oxidation



As implantation

Fig. 2-13 Cross section of sample I by TEM, and smooth morphology is observed.



1600 °C activation

Fig. 2-14 Cross section of sample IA by TEM, and poor morphology is observed which is responding for phenomenon of double barrier and high reverse leakage current.

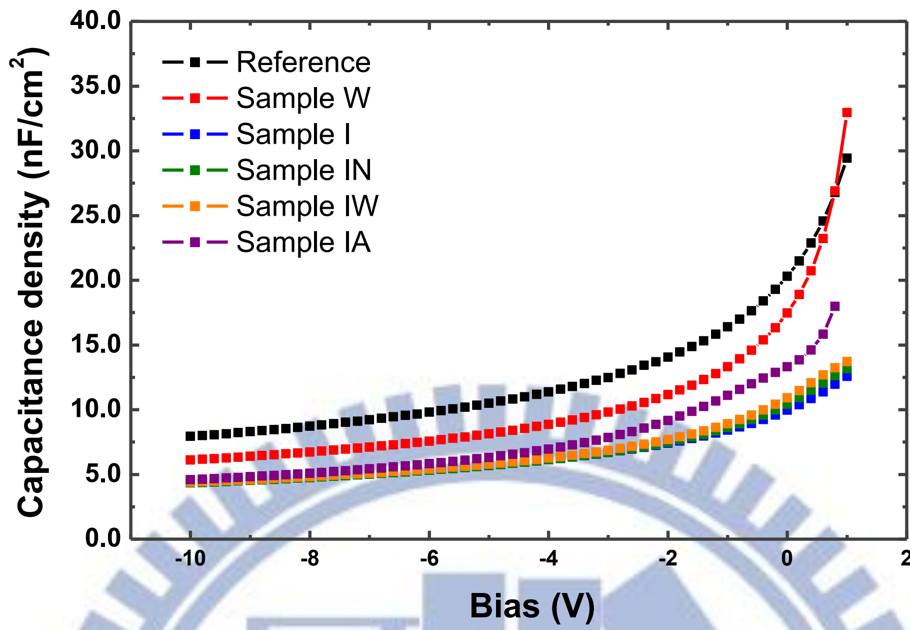


Fig. 2-15 Capacitance-voltage characteristics of Ni/4H-SiC SBD fabricated on different processed epi-layers

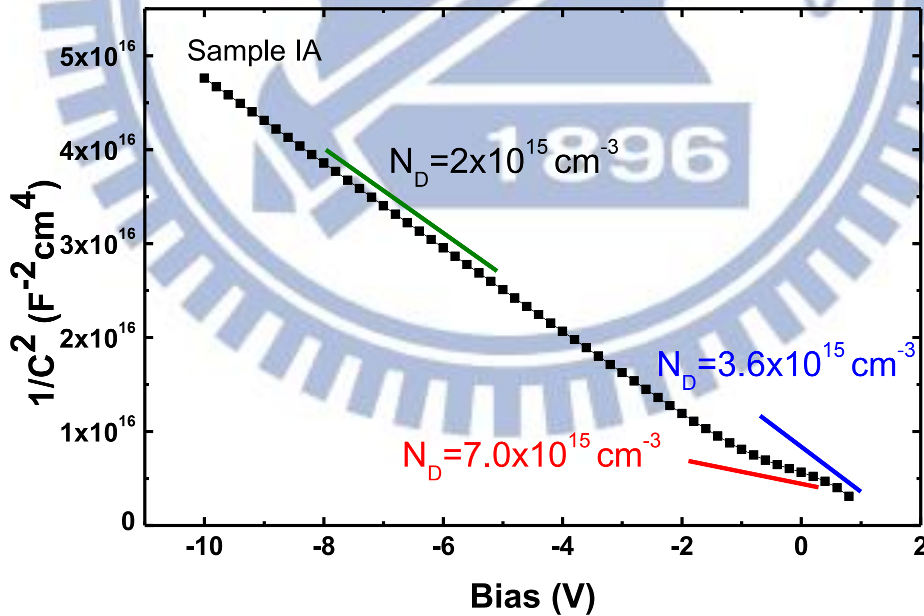


Fig. 2-16 C^{-2}-V characteristics of Ni/4H-SiC SBD sample IA. The slope reflects the donor concentration of epi-layer after dopant activation.

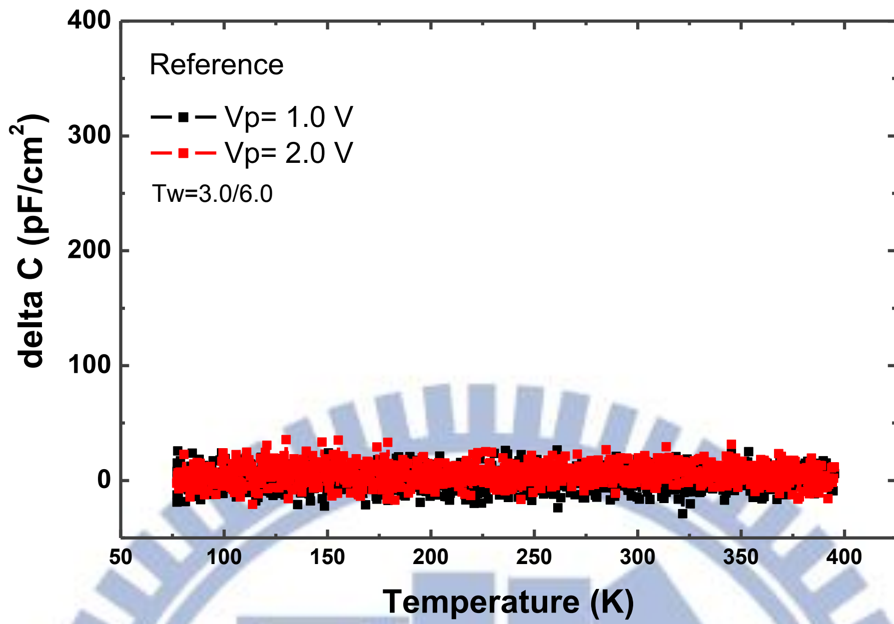


Fig. 2-17 Measured DLTS result of Ni/4H-SiC SBD reference sample.

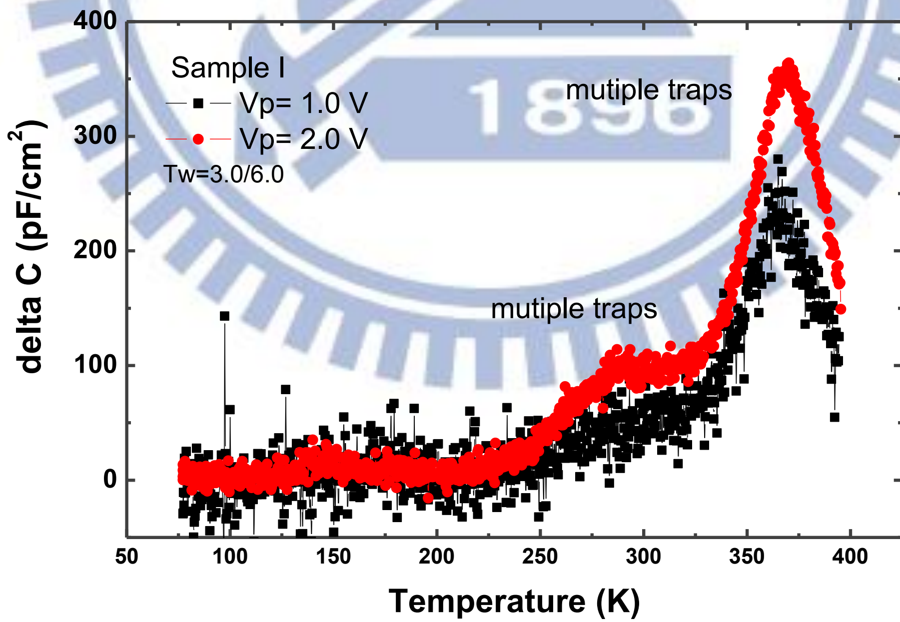


Fig. 2-18 Measured DLTS result of Ni/4H-SiC SBD sample I.

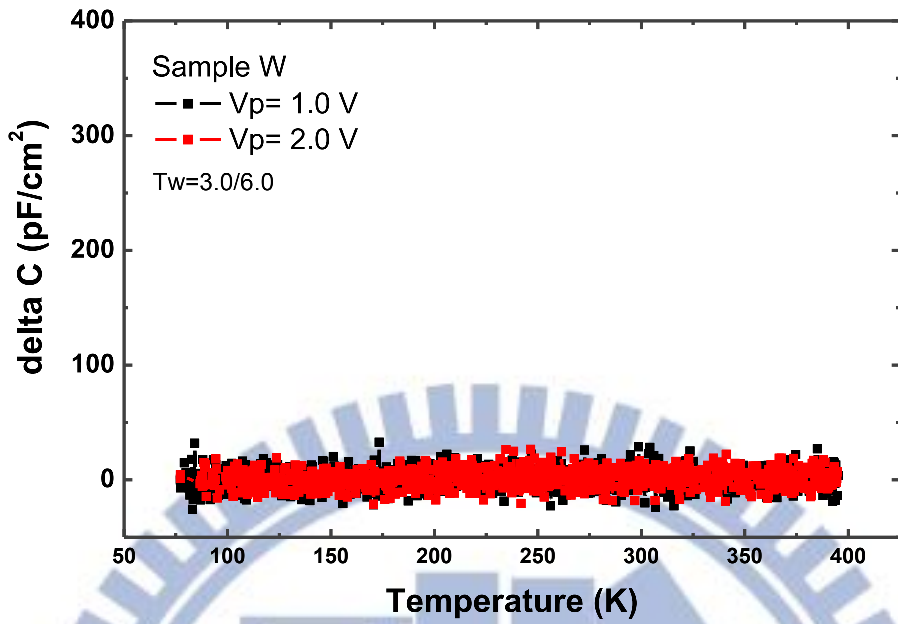


Fig. 2-19 Measured DLTS result of Ni/4H-SiC SBD sample W.

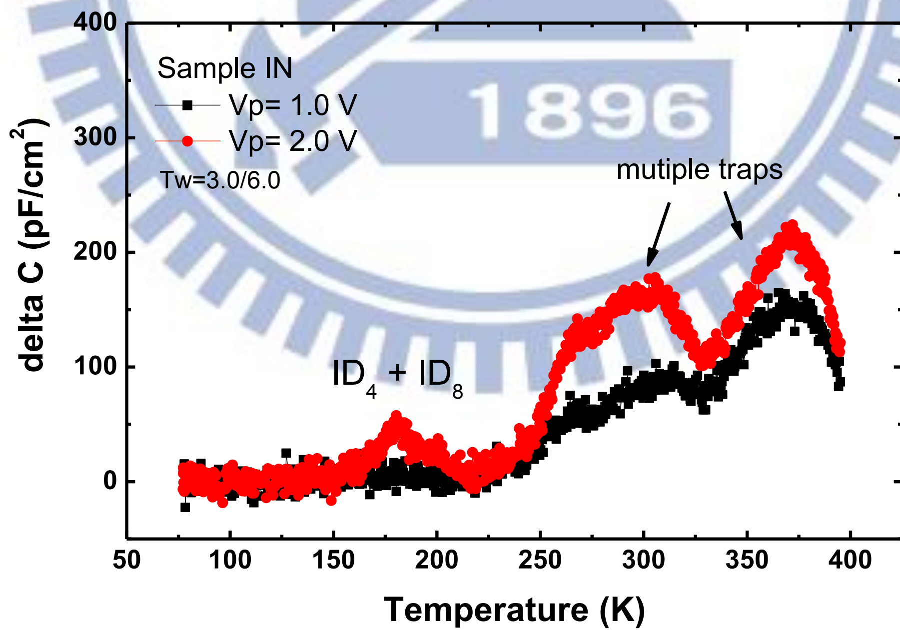


Fig. 2-20 Measured DLTS result of Ni/4H-SiC SBD sample IN.

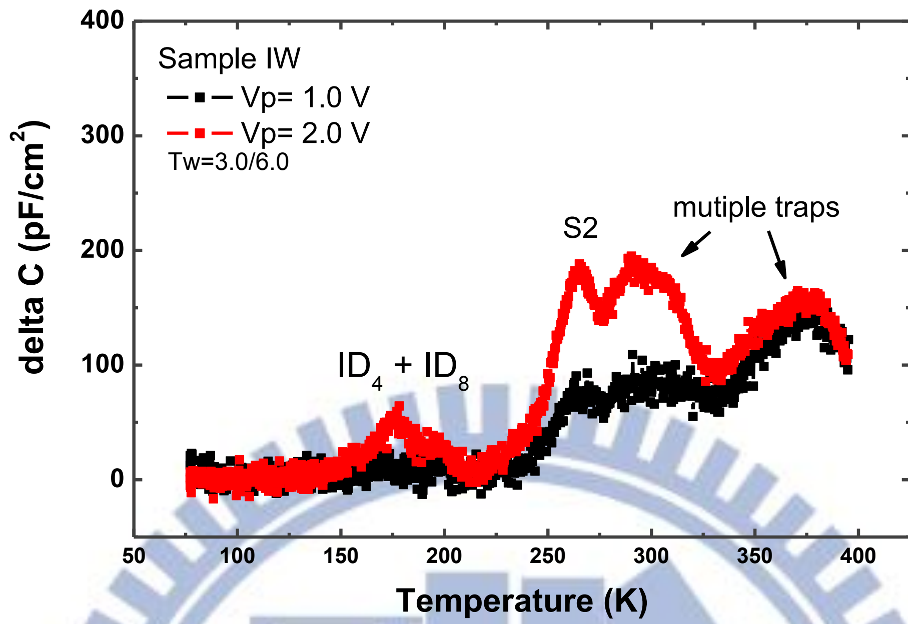


Fig. 2-21 Measured DLTS result of Ni/4H-SiC SBD sample IW.

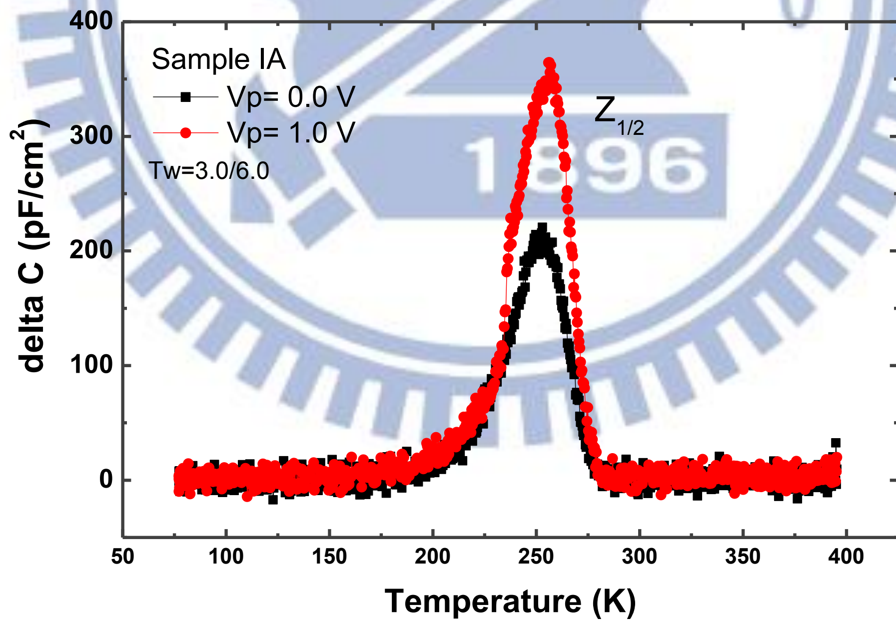


Fig. 2-22 Measured DLTS result of Ni/4H-SiC SBD sample IA.

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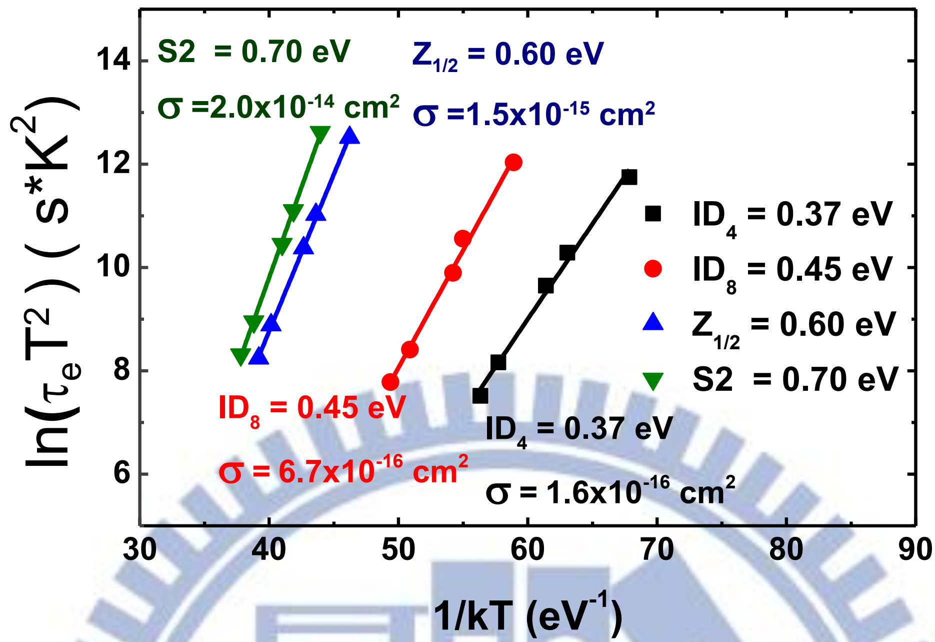

Fig. 2-23 $\ln(\tau_e T^2)$ – 1/kT plot. Activation energy and capture cross section can be extracted from the slope and interception on y-axis.

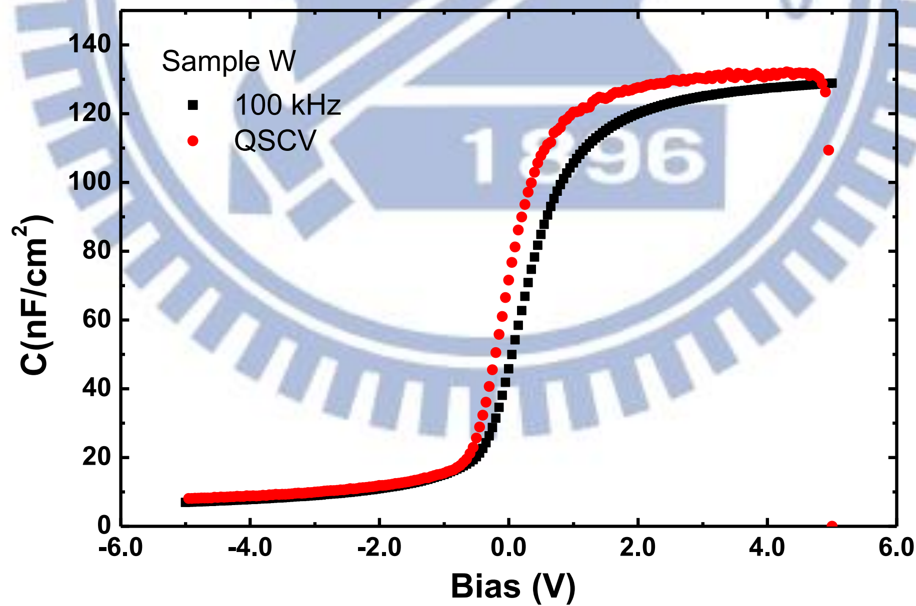

Fig. 2-24 High-low frequency C-V characteristics of SiC MOS capacitor sample W.

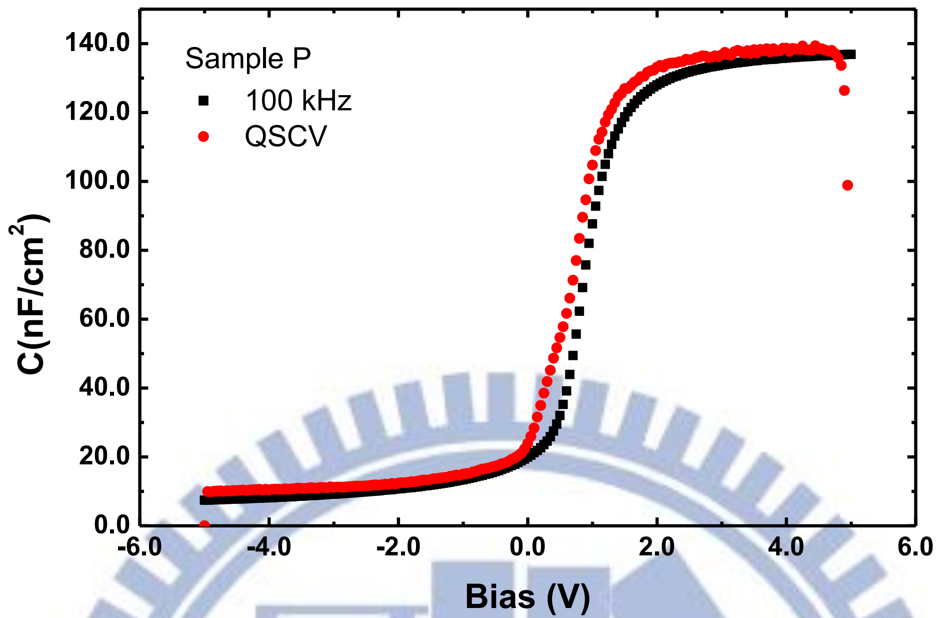

Fig. 2-25 High-low frequency C-V characteristics of SiC MOS capacitor sample P.

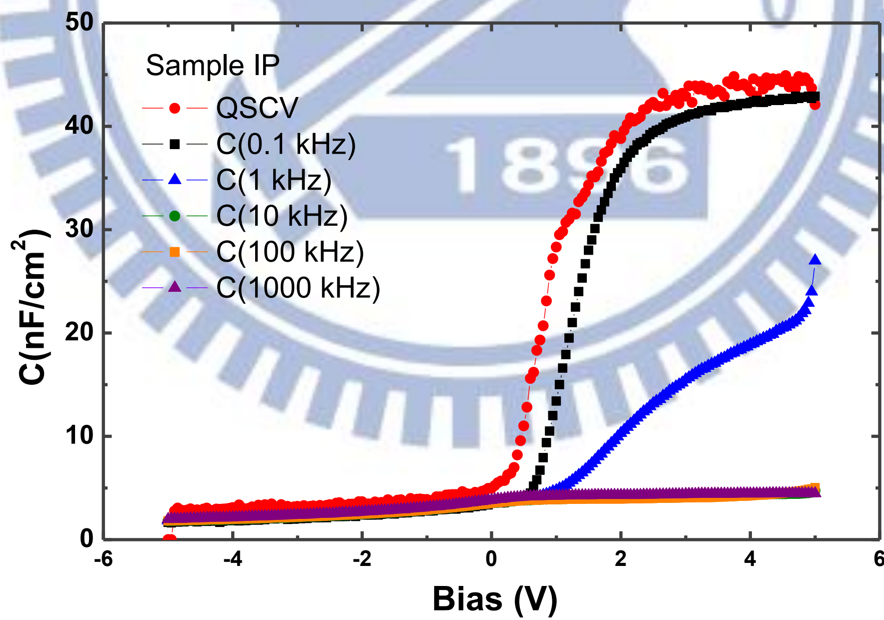

Fig. 2-26 Different frequency C-V characteristics of SiC MOS capacitor sample IP.

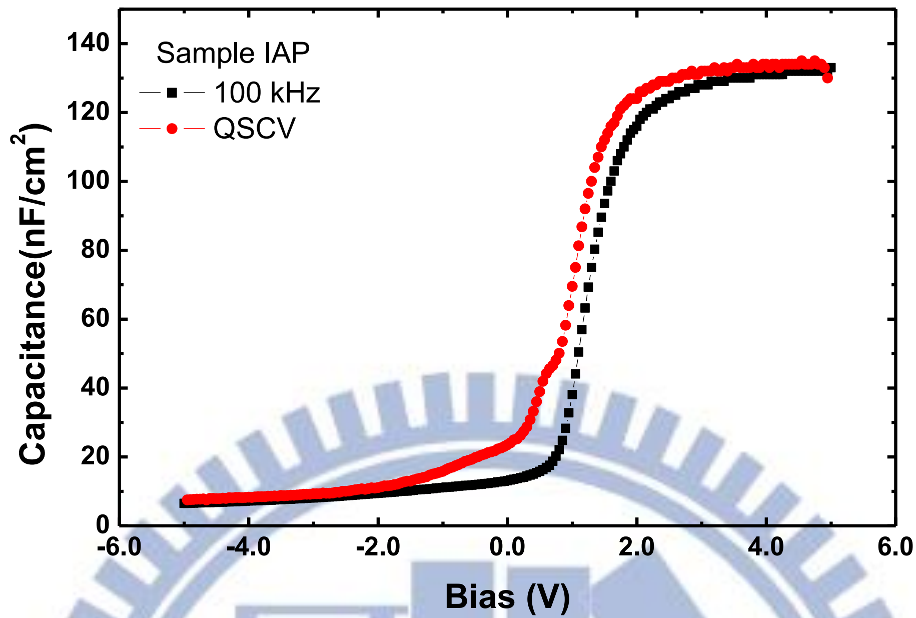

Fig. 2-27 High-low frequency C-V characteristics of SiC MOS capacitor sample IAP.

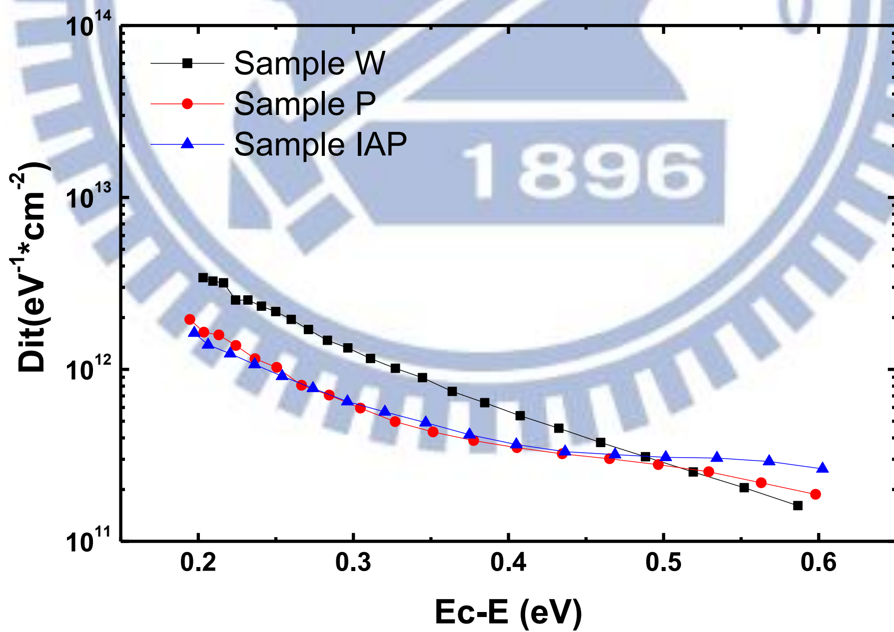

Fig. 2-28 Measured D_{it} from high-low frequency C-V method

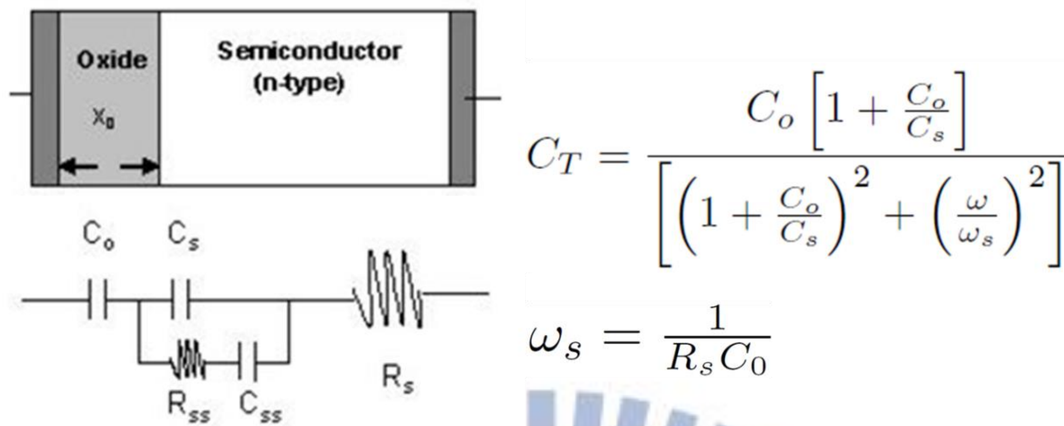

Fig. 2-29 Equivalent circuit of MOS capacitor with highly resistive substrate [48]

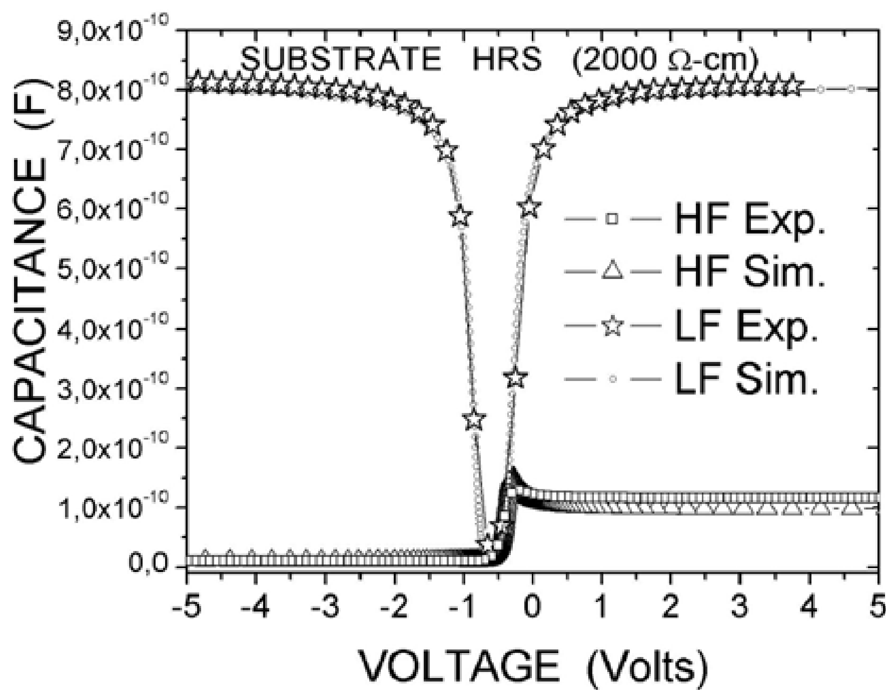

Fig. 2-30 Simulation and experiment result of MOS capacitor with highly resistive substrate [48]

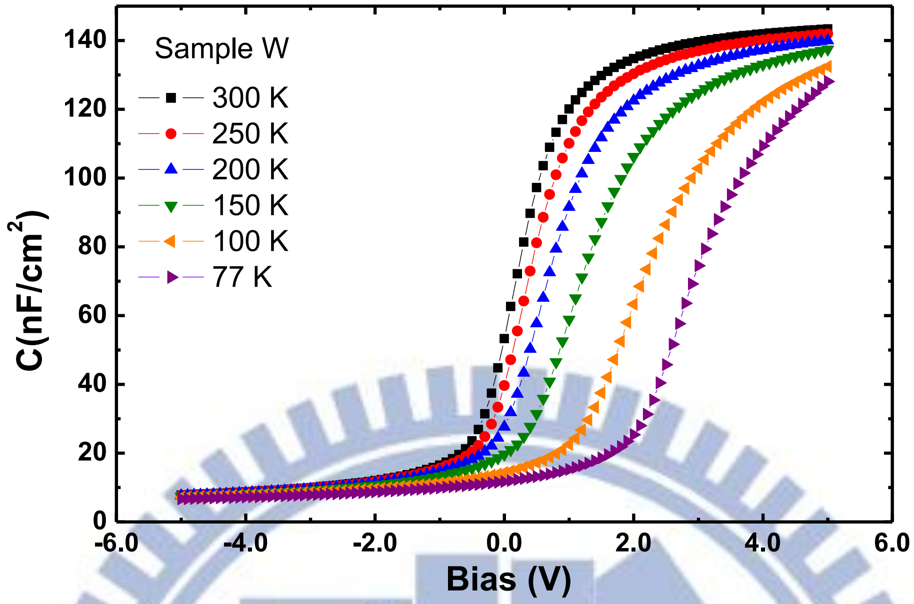

Fig. 2-31 Capacitance-voltage characteristics over temperatures of SiC MOS capacitor sample W.

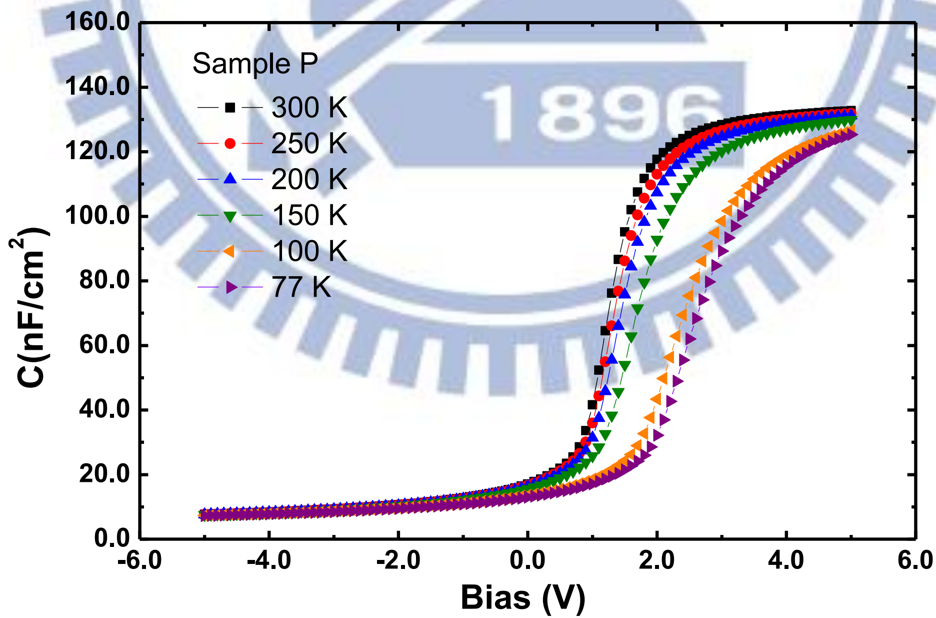

Fig. 2-32 Capacitance-voltage characteristics over temperatures of SiC MOS capacitor sample P.

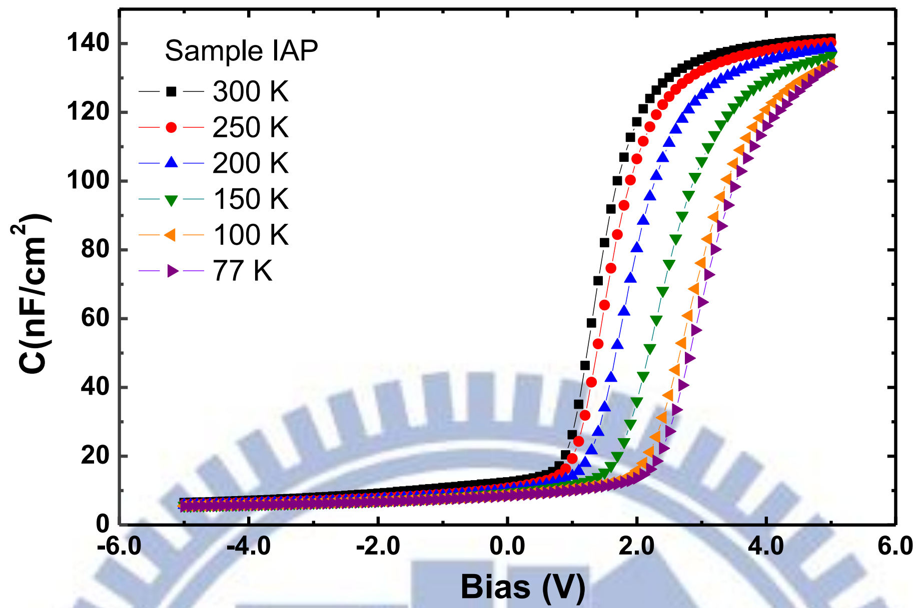

Fig. 2-33 Capacitance-voltage characteristics over temperatures of SiC MOS capacitor sample IAP.

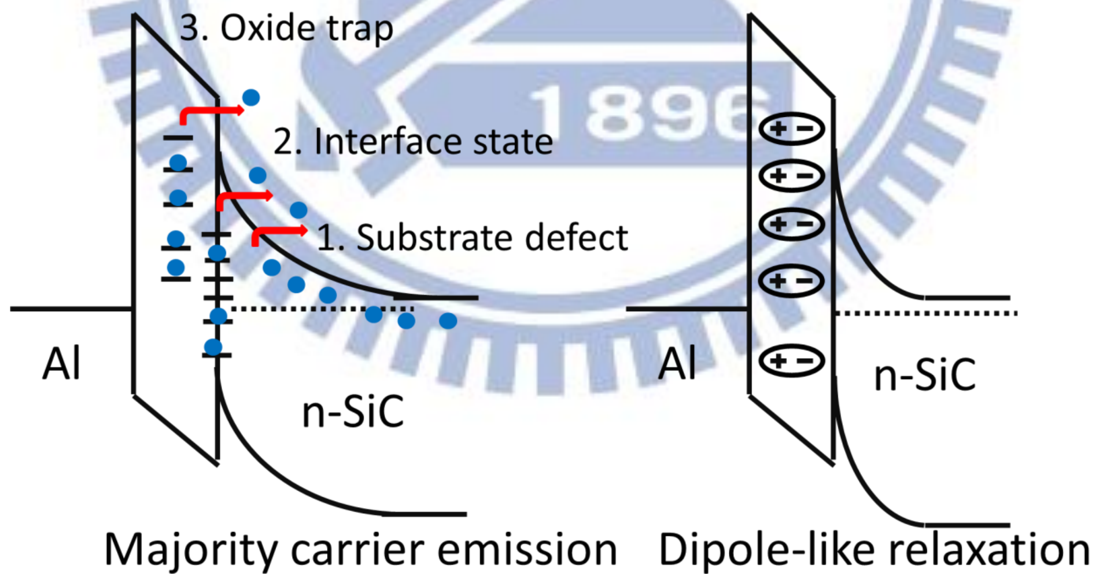

Fig. 2-34 Traps can be detected by DLTS system [50].

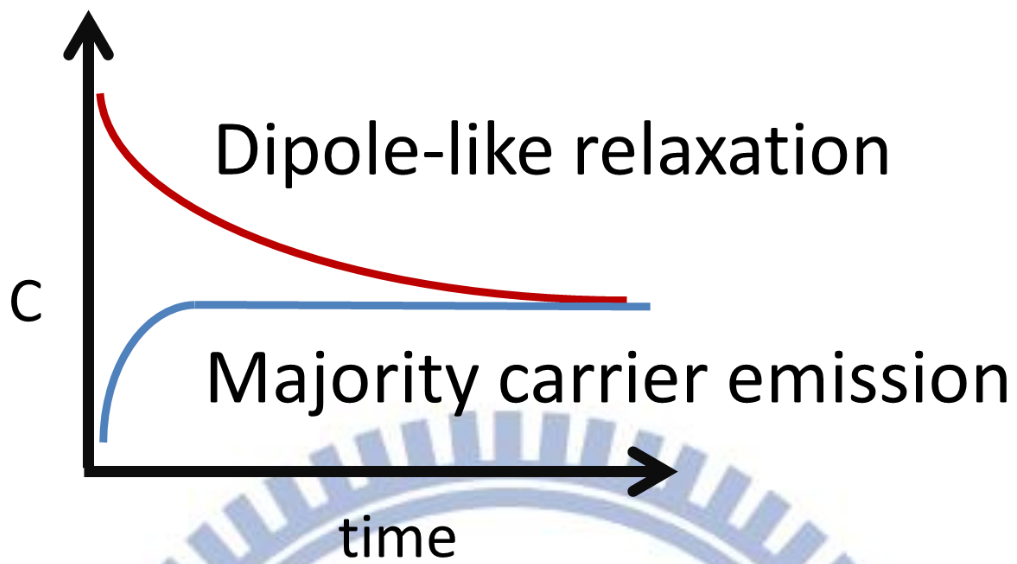

Fig. 2-35 Transient capacitance of two different mechanisms [50].

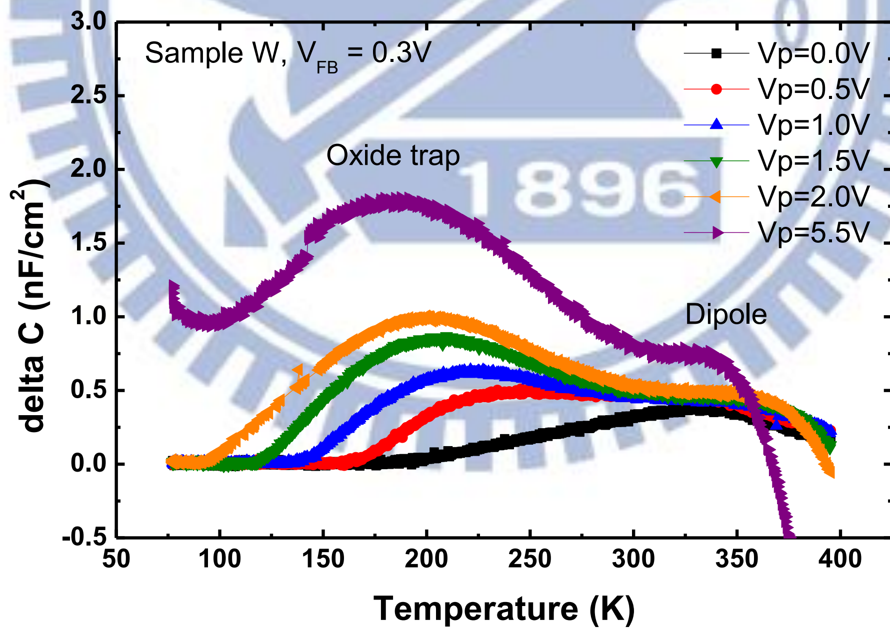

Fig. 2-36 Measured DLTS of SiC MOS capacitor sample W

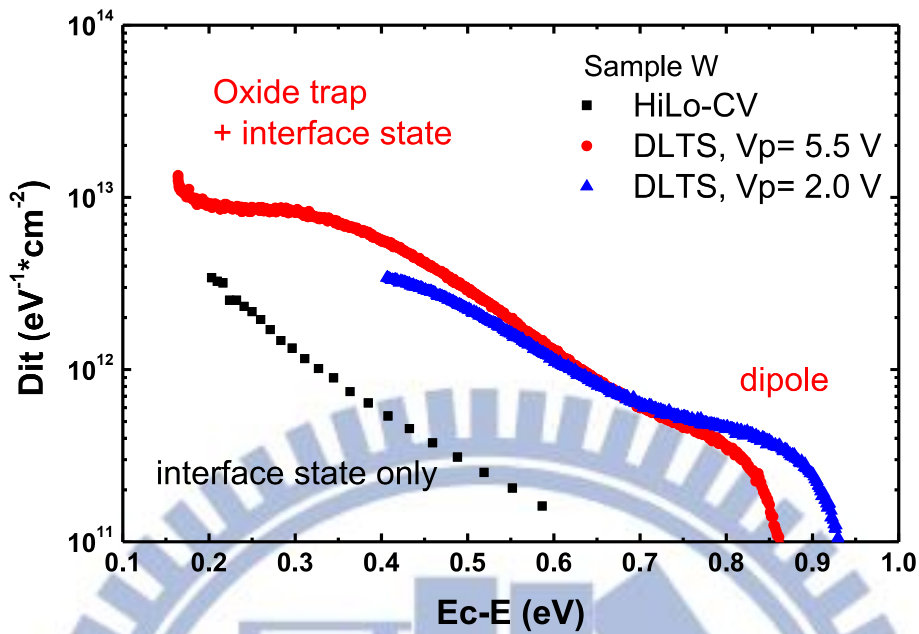

Fig. 2-37 Measured D_{it} from of SiC MOS capacitor sample W

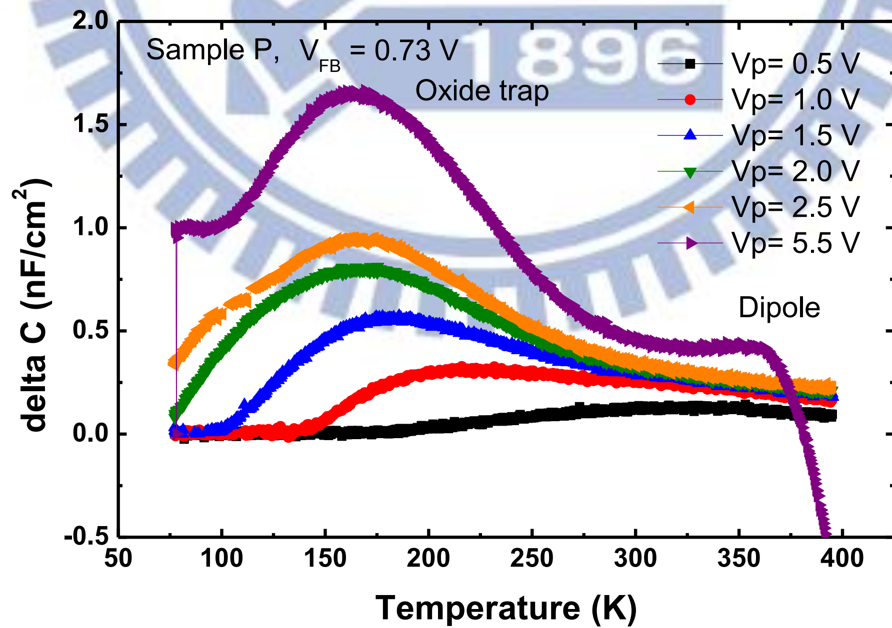

Fig. 2-38 Measured DLTS of SiC MOS capacitor sample P

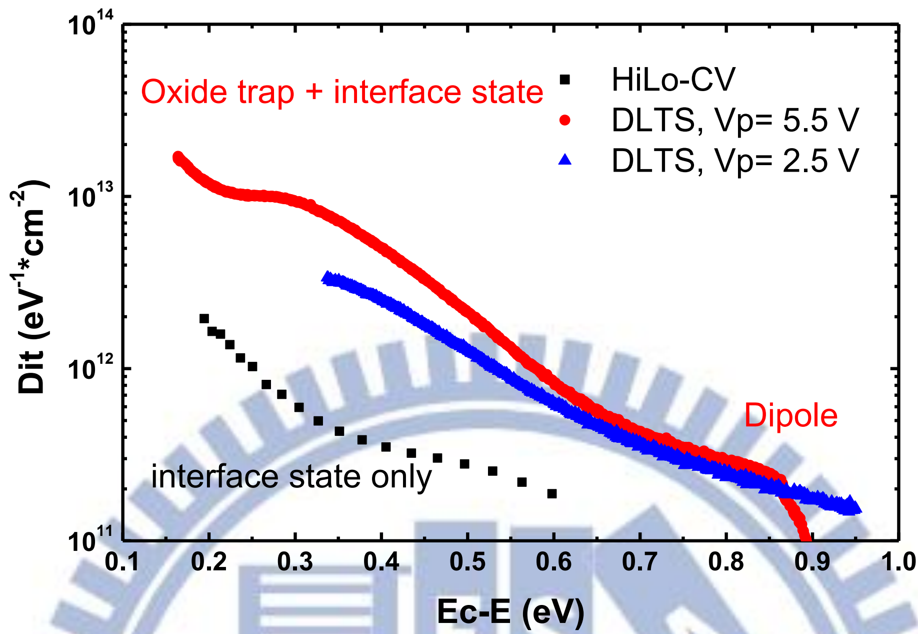

Fig. 2-39 Measured D_{it} from of SiC MOS capacitor sample P

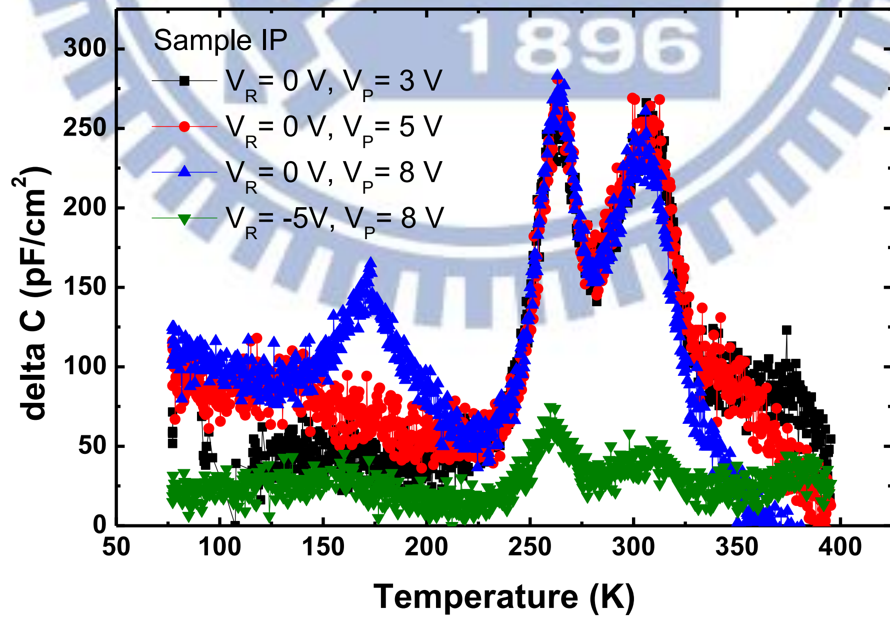

Fig. 2-40 Measured DLTS of SiC MOS capacitor sample I.

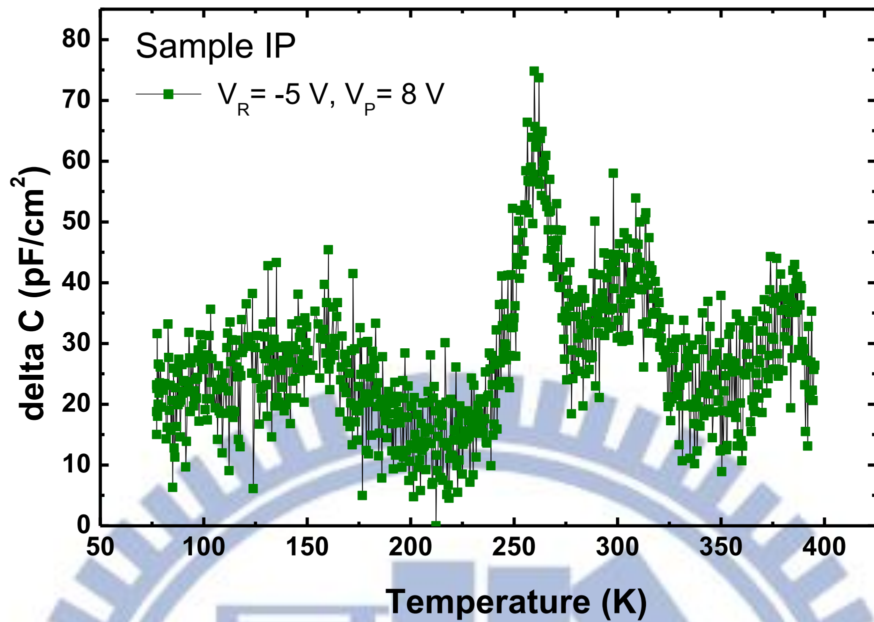

Fig. 2-41 Measured DLTS of SiC MOS capacitor sample I with larger reverse bias to observe the substrate defect with higher activation energy.

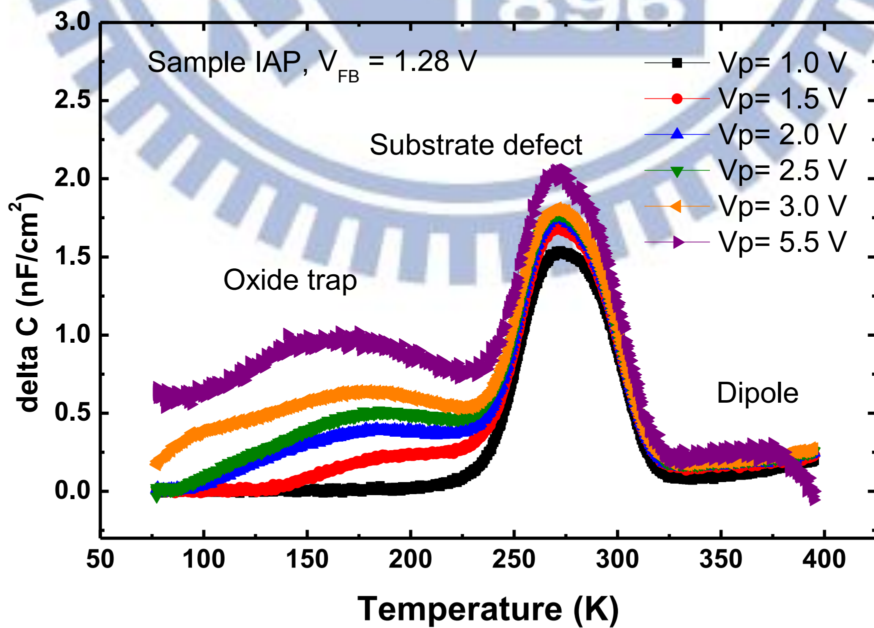

Fig. 2-42 Measured DLTS of SiC MOS capacitor sample IAP

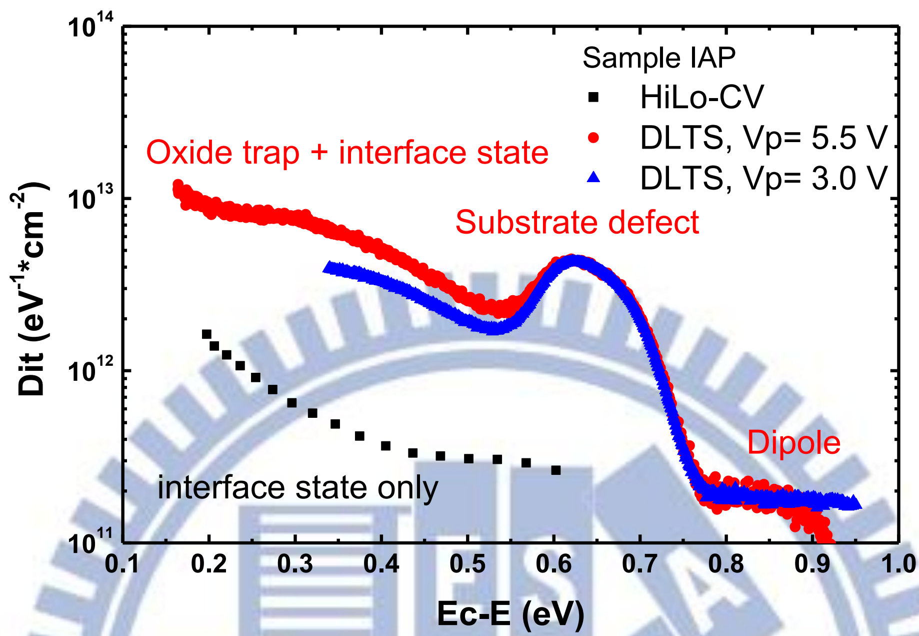

Fig. 2-43 Measured D_{it} from of SiC MOS capacitor sample IAP

Chapter 3

Design Analysis of the SiC Trench Junction Schottky Barrier (TJBS) Diode

3-1 Structure and parameters in simulation

Many different JBS diodes in SiC have been proposed to ease the process complexity or to enhance performance, for example, dual-metal trench Schottky (DMTS) diode, trench MOS Schottky barrier (TMBS) diode, and trench junction barrier Schottky barrier diode (TJBS) [29, 30]. For the DMTS diode and TMBS diode, many researches have been done to enhance the performances [53, 54, 55]. The TJBS diode proposed by C. F. Huang is the latest diode among them, so there are few relevant studies on it [30]. Hence, we expect to figure out the design guidelines of the TJBS by two-dimensional TCAD simulation to explore the knowledge of TJBS.

We simulate the performance of JBS diode and TJBS diode with different geometric parameters by the Sentaurus TCAD tool [56]. Even our main purpose is the design of the TJBS diode, the JBS diode can be regarded as a TJBS with trench depth equals 0 as shown in Fig. 3-1. Due to the symmetry of the diode structure, we construct only a half pitch of the device. The JBS diode structure has a 5-μm-thick epi-layer with a constant doping concentration of $N_D= 5x10^{15}$ cm^{-3}. The dopant profile of the p-type region is assumed Gaussian distribution with the highest concentration of $N_A= 1x10^{20}$ cm^{-3} and a junction depth of 0.2 μm. The lateral diffusion factor is equal to 0.5. Generally, there should be an n^+ substrate underneath the epi-layer to form ohmic contact in real device. However, it's not important for our simulation. In addition, to solve the failure of convergence in simulation, we remove it and ohmic contact is directly placed below the epi-layer. Parameter Ws is the length of Schottky

contact region, and parameter Wp is the length of p-type region with ohmic contact. Because only a half pitch of diode is simulated, a half of Ws and a half of Wp are constructed in the structure. For the TJBS diodes, parameter D is the trench depth and the sidewall of the trench is defined as Schottky contact. It's worthwhile to note that the p^+ region must be thick enough and surround the bottom corner of the trench sufficiently otherwise the premature of breakdown at corner tends to occur.

Different parameters of Ws, Wp, and D are split to investigate the design guideline of the TJBS. The split values of Ws and Wp are 0.25, 0.5, 1, 2, and 3 μm. The split values of D are 0, 0.5, and 1 μm. The JBS diode is the case while D=0 μm. The Schottky barrier height is about 1.2 eV, which equals the Schottky barrier height of Ti on n-type 4H-SiC [27]. Physical parameters of 4H-SiC have been built in the Sentaurus TCAD tool [56]. The breakdown voltage of device is defined as the voltage at which the electric field reaches the critical electric field of 4H-SiC 3.2 MV/cm. The sidewall area is not involved in the calculation of current density, because from the top view of device the trench is not accounted for the footprint.

3-2 Forward bias characteristics of JBS diode

The forward bias characteristics of the JBS diode with fixed value of Ws and different values of Wp are simulated firstly. For Ws= 0.25 μm and 0.5 μm in Fig. 3-2 and Fig. 3-3, respectively, the conduction path of the Schottky junction is affected by the depletion region of the pn junction, so the cut-in voltage becomes close to that of the pn junction. This is similar to the JFET effect of the VDMOSFET [57]. For Ws= 1, 2, and 3 μm in Figs. 3-4, 3-5, and 3-6, respectively, the conduction path are not depleted completely by the pn junction, so the cut-in voltage is dominated by the cut-in voltage of the Schottky junction. It can be observed that the cut-in voltage is

dependent of the Schottky contact width Ws while independent of the pn junction width Wp. Fig.3-7 compares the forward characteristics of devices with different values of Ws at fixed Wp= 3 μm. As Ws increases, the cut-in voltage returns to the normal value of the Schottky juncton. The unipolar current is also higher due to wider conducting path free from the influence of the depletion region of the pn junction. Besides, the increase of Ws also retards the transition to bipolar conduction as shown in Fig. 3-8. As to the increase of Wp, the switch of conduction mechanism occurs earlier because higher voltage drops on the right-hand side of the pn junction away from the Schottky contact and the higher bipolar conduction current.

It's noticeable that current discontinuity occurs at the transition point from unipolar conduction to bipolar conduction. This discontinuity occurs while Ws becomes larger. Hence, we investigate the smooth curve as Ws= 0.5 μm and the discontinuity curve as Ws= 3 μm while both Wp= 3 μm in detail. Fig. 3-9 shows the depletion region before and after the transition point. As Ws= 0.5 μm, the depletion regions are quite the same. As Ws= 3 μm, before the transition, the lateral non-uniformity of depletion region shows the partial conduction of the pn junction. The change in depletion region after transition shows the complete turn-on of the pn junction. From the distributions of electron current density and hole current density shown in Fig. 3-10, it's apparent to see the change in current density after transition as Ws= 3 μm, while Ws= 0.5 μm is not. As Ws= 3 μm, the conduction mechanism changes from unipolar conduction to bipolar conduction. As well as the conduction mechanism, the electrostatic potential under the pn junction shown in Fig. 3-10 has the same behavior. Different electrostatic potential is due to different transition voltage of the diodes with Ws= 0.25 μm and 3 μm. More voltage drop on the pn junction after the transition as Ws= 3 μm. As Ws= 0.5 μm, the diode is always

dominated by minority carrier conduction, so no more change on the electrostatic potential will be observed.

The abrupt turn-on of the pn junction near the Schottky contact seems like the main reason of the discontinuity in the forward I-V curve. If we reduce the voltage step of simulation, the numerical calculation of Sentaurus TCAD tool at the transition point from unipolar conduction to bipolar conduction still results in such a discontinuity, especially when Ws is large. However, the total current density after transition is at the same level as that of the diode with smooth I-V curve.

3-3 Forward bias characteristics of TJBS diode

We expect to observe extra current from the sidewall Schottky contact and other effect on the TJBS diode. An extra trench depth parameter D is involved in the simulation structure as shown in Fig. 3-1. The split values of parameter D are 0.5 μm and 1 μm.

At fixed trench depth value of D= 0.5 μm, the I-V characteristics with Ws= 0.25 μm and 0.5 μm are shown in Fig. 3-12 and Fig. 3-13, respectively. The TJBS diode has similar characteristics as the JBS diode and the cut-in voltage is still suffered from JFET effect. When Ws= 1 μm in Fig.3-14, the cut-in voltage return to the normal value of the Schottky contact. The main unipolar conduction resistance comes from the narrow path in the epi-layer nearby the pn junction. Hence, if the unipolar current is the same with regardless of Wp, the wider Wp would result in smaller unipolar current density but higher bipolar and total current density. Fig. 3-15 and Fig. 3-16 are corresponding to Ws= 2 μm and 3 μm, respectively. As the Schottky contact width Ws increases, the conducting path becomes wider, so the phenomenon associated with parameter Wp is less obvious. Fig. 3-17 compares the TJBS diodes with different Ws

values. The trench depth D and Wp are fixed at 0.5 μm and 3 μm, respectively. It can be seen that the cut-in voltage as Ws= 1 μm is still influenced by the depletion region of the pn junction. The effect on transition voltage of Ws and Wp are still opposite for the TJBS diodes as show in Fig. 3-18.

3-4 Comparison of electrical characteristics of TJBS diode

In this section, the performance of the TJBS diodes with D= 0 μm, 0.5 μm, and 1 μm are compared. It is noted that the TJBS diode with D= 0 μm is the JBS diode actually. As Ws= 0.25 μm as shown in Fig.3-19, Schottky contact region is depleted by the pn junction. Before the turn-on of the pn junction, the Schottky junction is pinched off so that each device behaves like a pn diode and the cut-in voltage is high. The bipolar current is higher as the trench is deeper because of the lower resistance from the thinner epi-layer beneath the pn junction. As Ws increases to 0.5 μm as shown in Fig. 3-20, the cut-in voltages of the TJBS diodes are still affected by the depletion region of the pn diode while the JBS diode is affected slightly. The turn-on of the TJBS becomes not influenced by the pn junction until Ws increases to 1 μm as shown in Fig.3-21, but the poor ideality factors reflect the narrow conduction path. From the inset in Fig. 3-22, the current level of TJBS diodes is higher than JBS diode at low bias region. Hence, only at low current level, the current conduction will not be affected. If the value of Ws becomes wider than 1 μm, the utility of sidewall becomes obvious as shown in Fig. 3-23. The Schottky junction turns on much earlier than the pn junction and the cut-in voltage is smaller as the trench becomes deeper because the extra current component from the sidewall Schottky contact [30]. On the TJBS diodes, the narrow path of unipolar conduction results in the higher resistance. However, the higher bipolar current could be obtained due to the lower resistance of thinner

epi-layer. Furthermore, the pn junction turns on earlier as the trench depth become deeper, which results in higher conduction current at high forward bias.

Breakdown voltages of the JBS diode and TJBS diode are shown from Fig. 3-24, Fig. 3-25, and Fig. 3-26. The wider Ws and deeper D are, the lower of the breakdown voltage will be. These diodes have symmetric structures, so the SiC nearby the Schottky junction would be depleted by the pn junction to maintain the breakdown voltage. If the value of Ws is small, the depletion regions of the neighboring pn junctions would connect together in a smooth shape. Hence, the higher breakdown voltage will be obtained with a smaller value of Ws. The function of the p^+ region of the pn junction is to provide enough acceptor concentration. If the acceptor concentration is high enough, the pn junction length Wp is not an important factor for breakdown voltage. The TJBS diodes have a lower breakdown voltage than the JBS diode under the same Ws and Wp parameters. First, the trench corner suffers from higher electric field. Second, the total length of the epi-layer is reduced because of the trench. Hence, the relatively low breakdown voltage will be obtained in TJBS diodes. It's should be noted that the p^+ region must be thick enough and surrounds around the trench corner well, otherwise the premature of breakdown at corner tends to occur.

3-5 Summary of the TJBS diodes

The geometric parameters of the TJBS diode have been investigated. The cut-in voltage is mainly affected by the Schottky contact width Ws and the trench depth D. The value of Ws can change the cut-in voltage greatly due to the depletion region of pn junction as Ws is narrower than 1 μm, i.e. the JFET effect. The value of D modulates the cut-in voltage slightly because extra sidewall current is provided at low forward bias. As the trench becomes deeper, the unipolar conduction current will be

lower, but higher bipolar conduction current will be obtained. Namely, the TJBS diodes have a lower specific on-resistance in bipolar operation. The value of Wp also influenced the bipolar current level. As to the transition voltage of the conduction mechanism, all the parameters have their effect. The larger value of Ws is, the greater transition voltage will be, while opposite in lager value of Wp and D. The smaller cut-in voltage of the TJBS diodes is in agreement with Huang [30], but different in the transition voltage. To ease fabrication complexity, the electrode of pn junction is not ohmic contact in previous study [30]. Partial voltage is consumed by the poor contact on pn junction, so higher transition voltage will be.

The breakdown voltage is mainly influenced by the value of Ws and D. With the increase of Ws, the shape of the depletion edge can not be plat, so the breakdown voltage reduces. With deep trench depth D, the trench corner and thinner epi-layer reduce the breakdown voltage. The breakdown of the TJBS diodes comes from the trench structure unlike pn diode which can be compensated by junction termination. The tradeoff between electrical characteristics like cut-in voltage, transition voltage, specific on-resistance after bipolar conduction, and breakdown voltage with different parameters are summarized in Fig. 3-27.

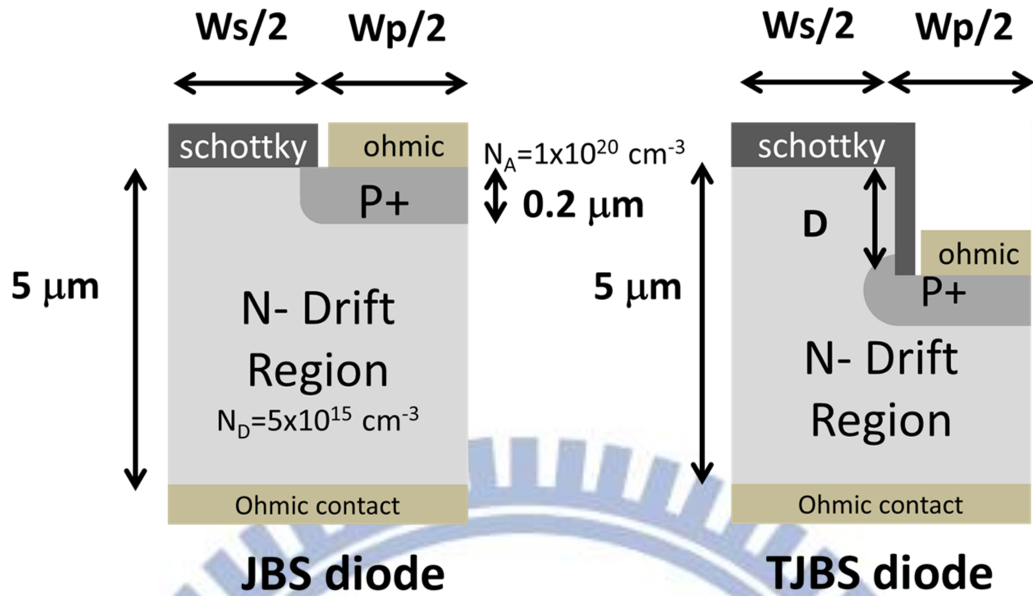

Fig. 3-1 Simulation structure and geometric parameters of JBS diode and TJBS diode.

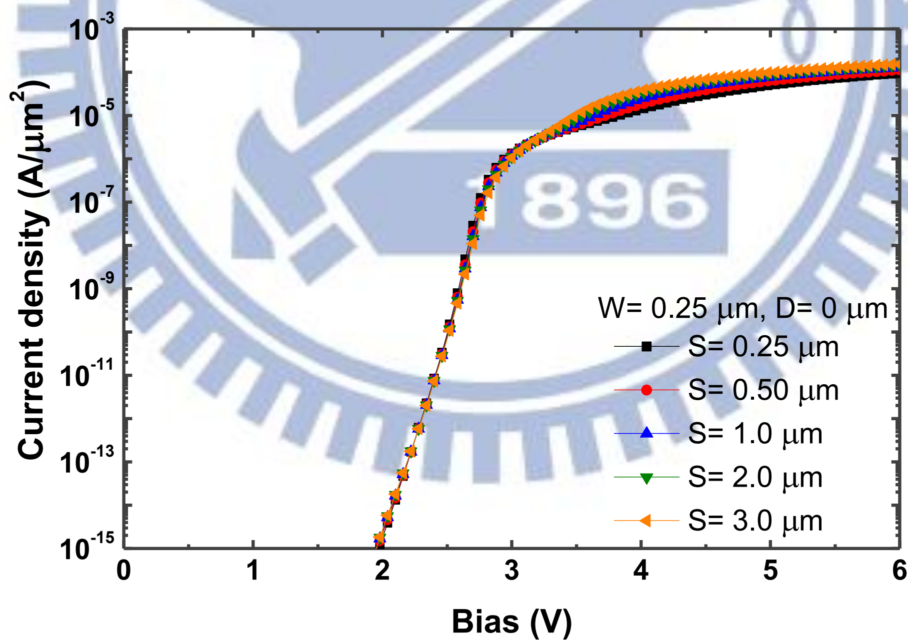

Fig. 3-2 Simulated forward characteristics of JBS diode with Ws= 0.25 μm and different values of Wp.

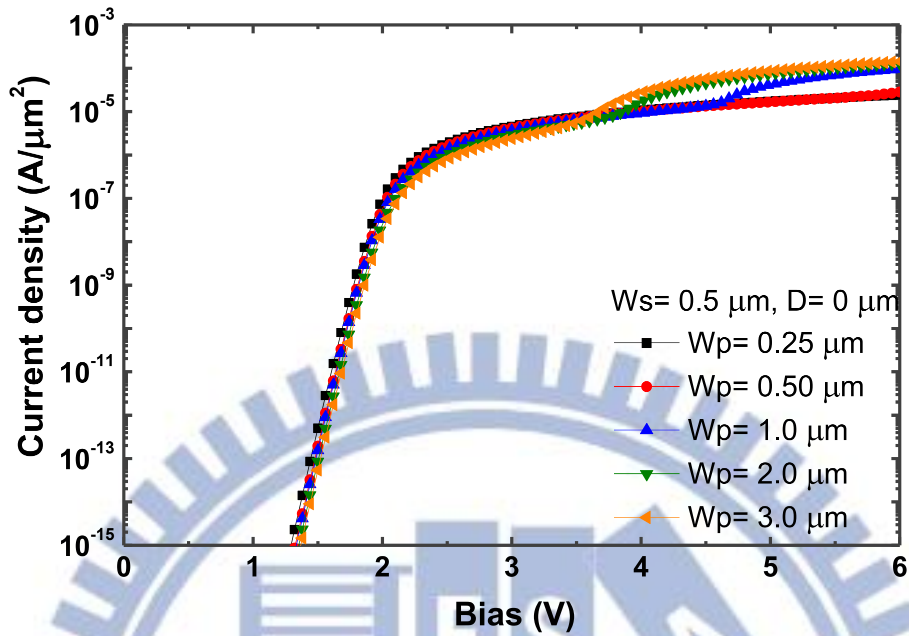

Fig. 3-3 Simulated forward characteristics of JBS diode with Ws= 0.5 μm and different values of Wp.

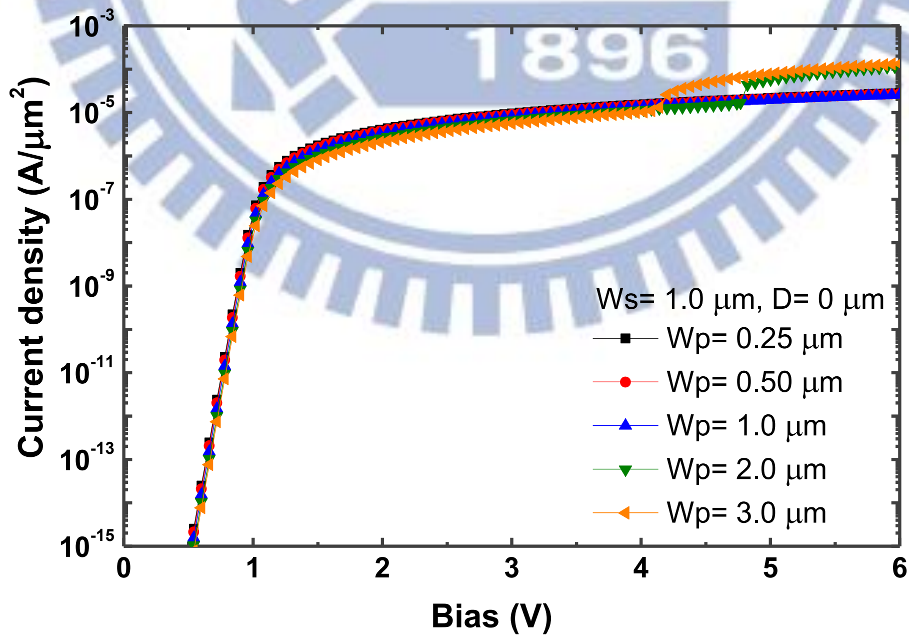

Fig. 3-4 Simulated forward characteristics of JBS diode with Ws= 1 μm and different values of Wp.

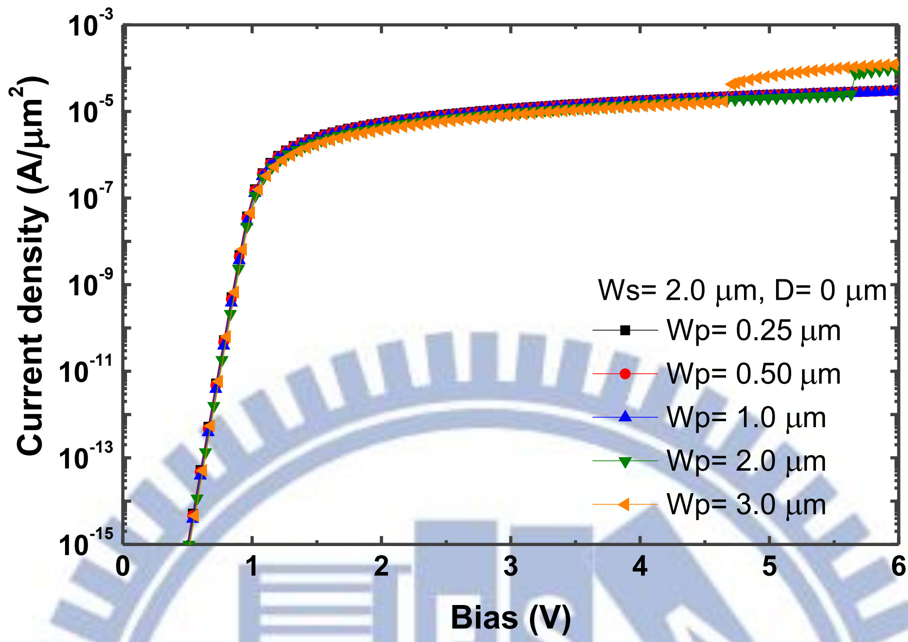

Fig. 3-5 Simulated forward characteristics of JBS diode with Ws= 2 μm and different values of Wp.

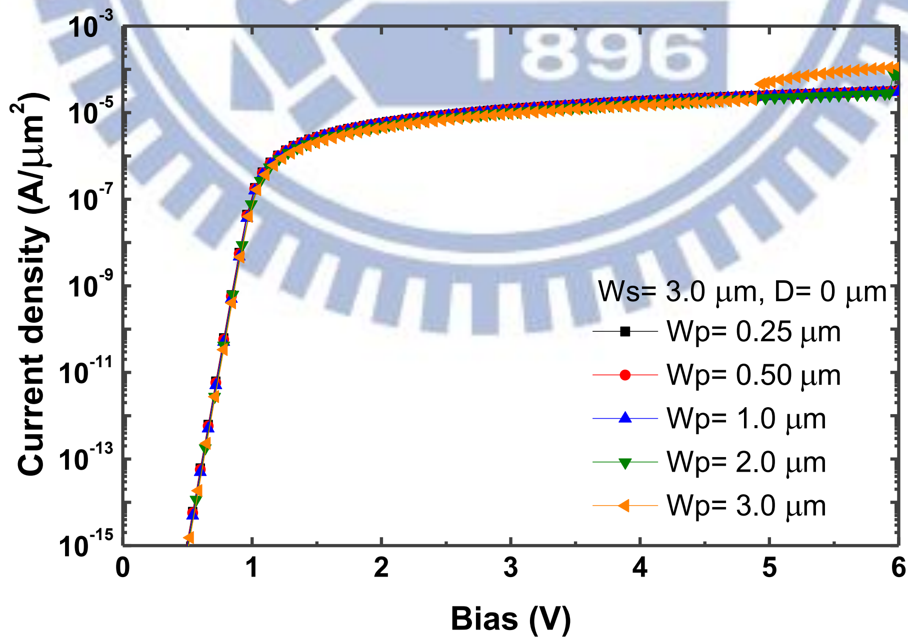

Fig. 3-6 Simulated forward characteristics of JBS diode with Ws= 3 μm and different values of Wp.

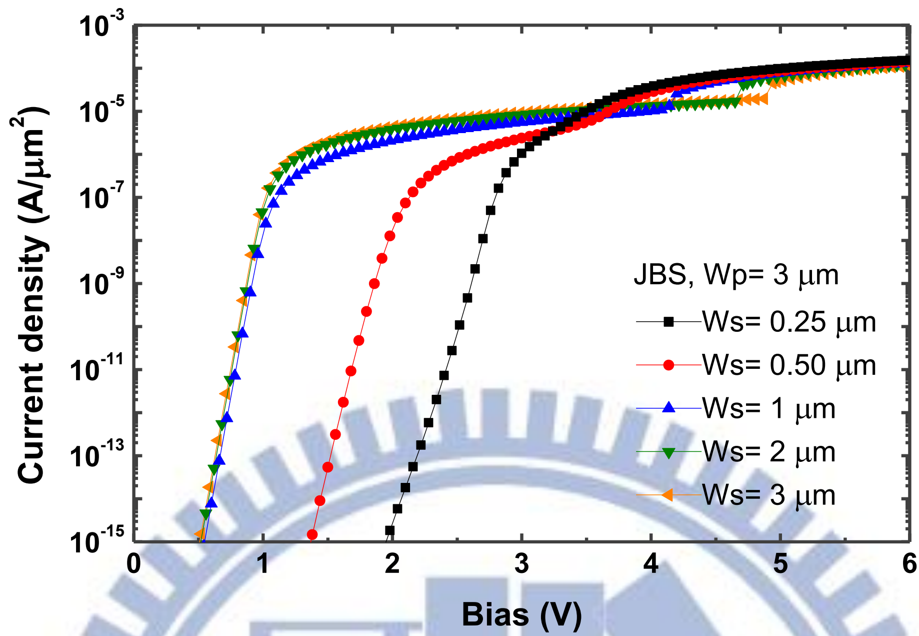

Fig. 3-7 Simulated forward characteristics of JBS diode with Wp= 3 μm and different values of Ws.

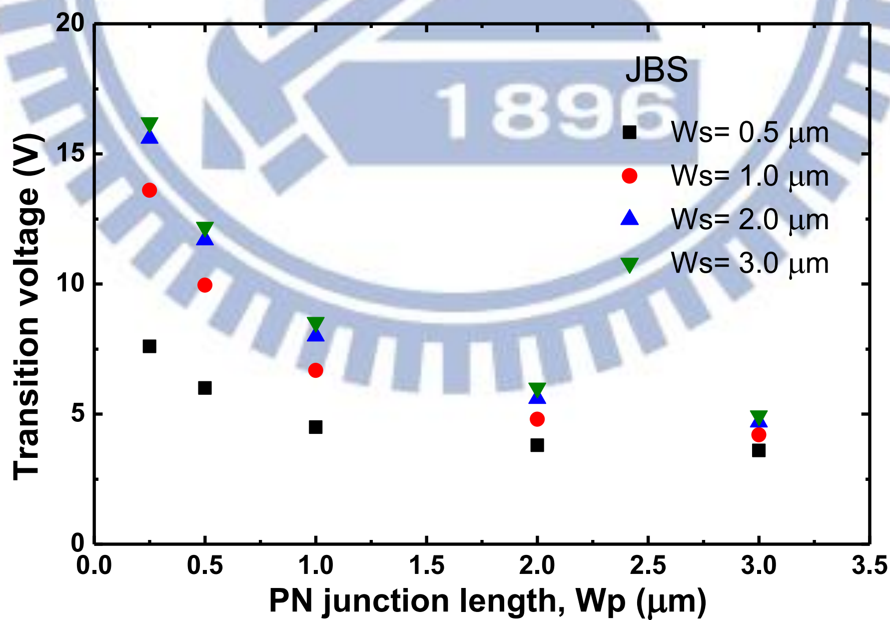

Fig. 3-8 Relations of transition voltage with Wp and Ws in JBS diodes.

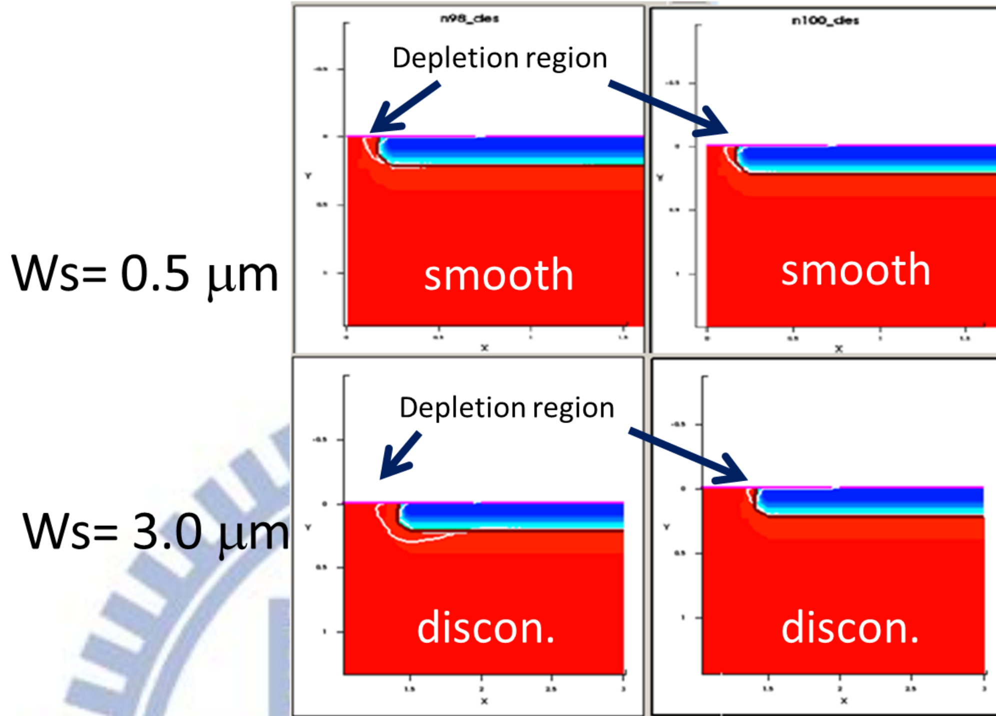

Fig. 3-9 Depletion region edge before and after the bipolar switch of smooth and discontinuous I-V curve.

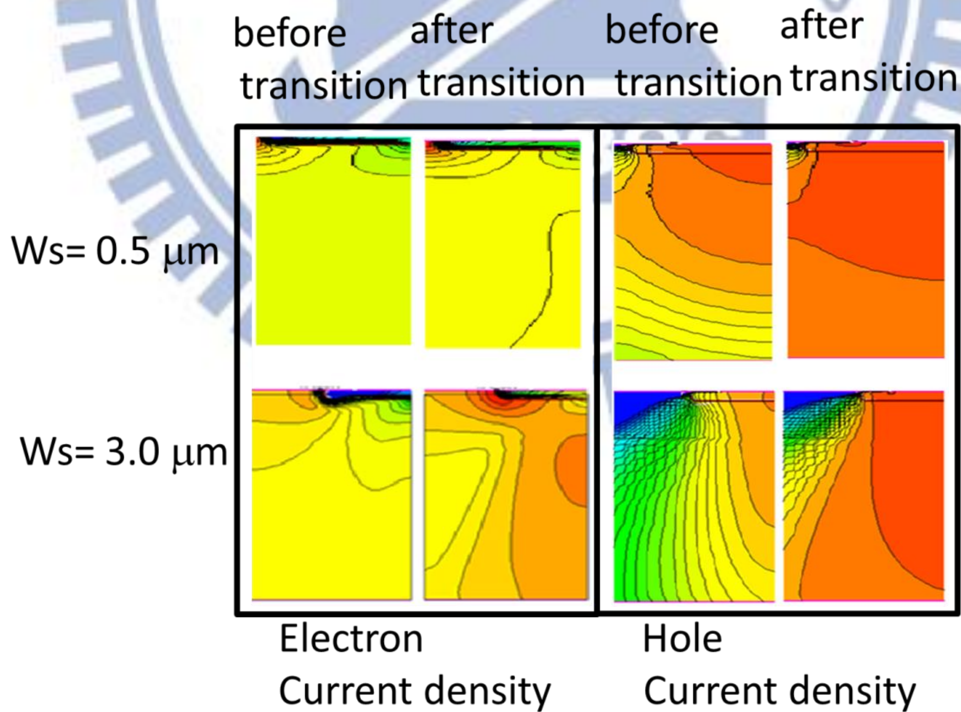

Fig. 3-10 Electron current density and hole current density before and after the bipolar switch of smooth and discontinuous I-V curve.

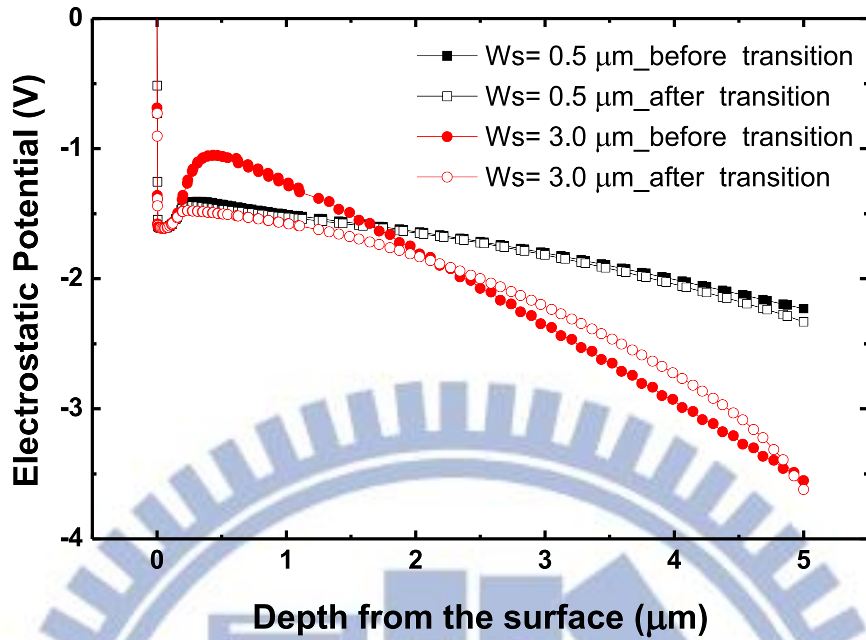

Fig. 3-11 Electrostatic potential at the pn junction near the Schottky contact before and after the bipolar switch of smooth and discontinuity I-V curve. Different total electrostatic potential is due to different transition voltage of Ws= 0.25 μm and 3 μm.

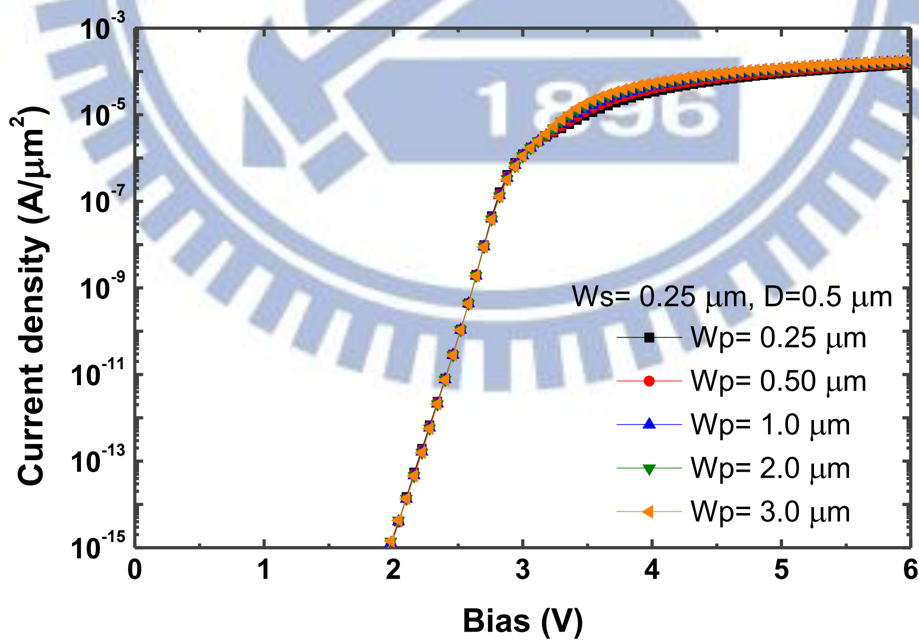

Fig. 3-12 Simulated forward characteristics of TJBS diode with D= 0.5 μm, Ws= 0.25 μm and different values of Wp.

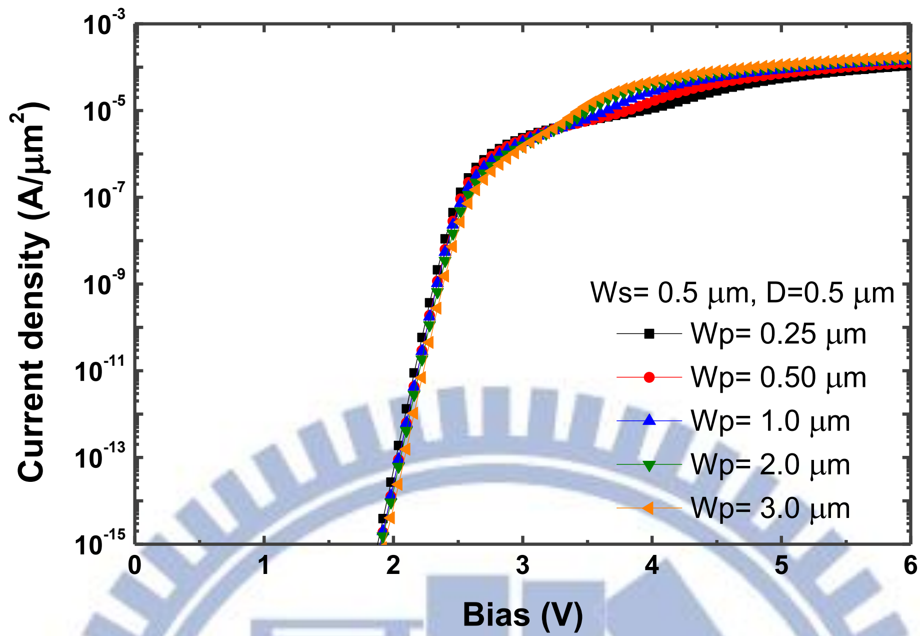

Fig. 3-13 Simulated forward characteristics of TJBS diode with D= 0.5 μm, Ws= 0.5 μm and different values of Wp.

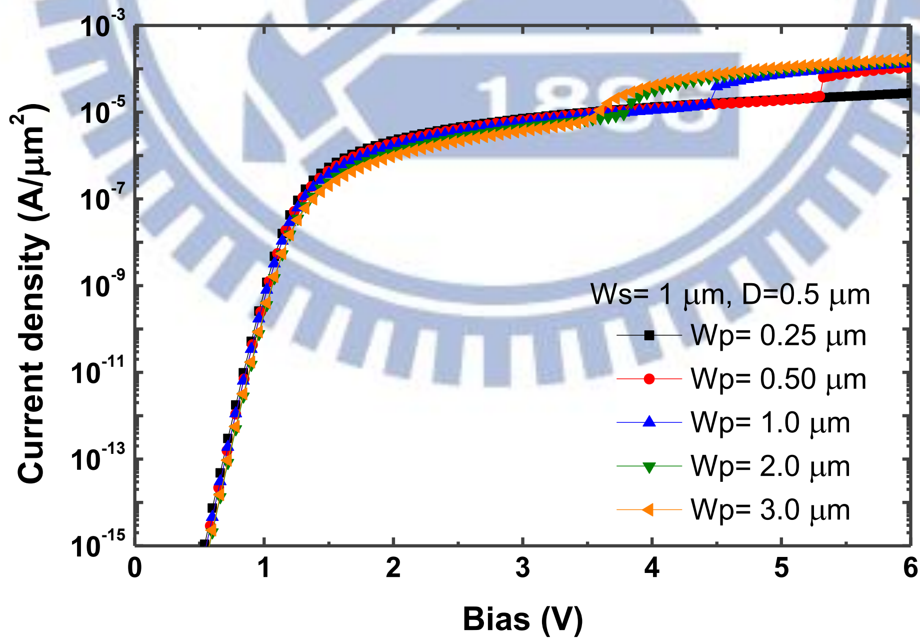

Fig. 3-14 Simulated forward characteristics of TJBS diode with D= 0.5 μm, Ws= 1.0 μm and different values of Wp.

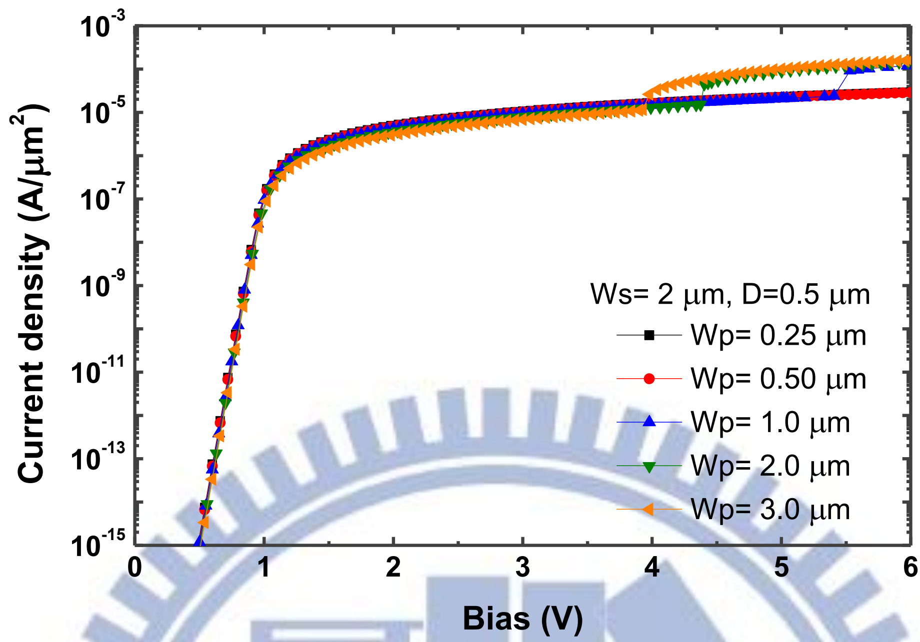

Fig. 3-15 Simulated forward characteristics of TJBS diode with D= 0.5 μm, Ws= 2.0 μm and different values of Wp.

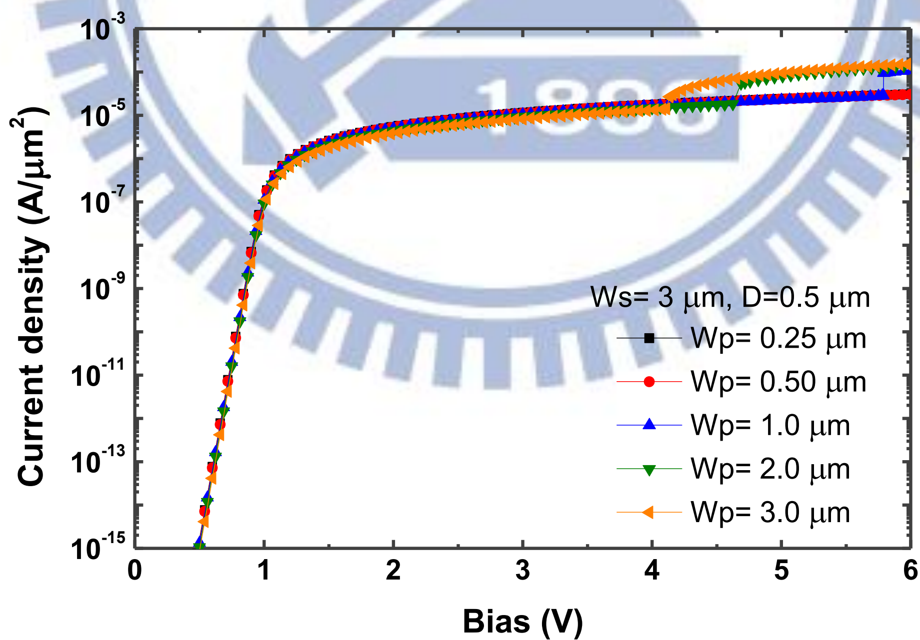

Fig. 3-16 Simulated forward characteristics of TJBS diode with D= 0.5 μm, Ws= 3.0 μm and different values of Wp.

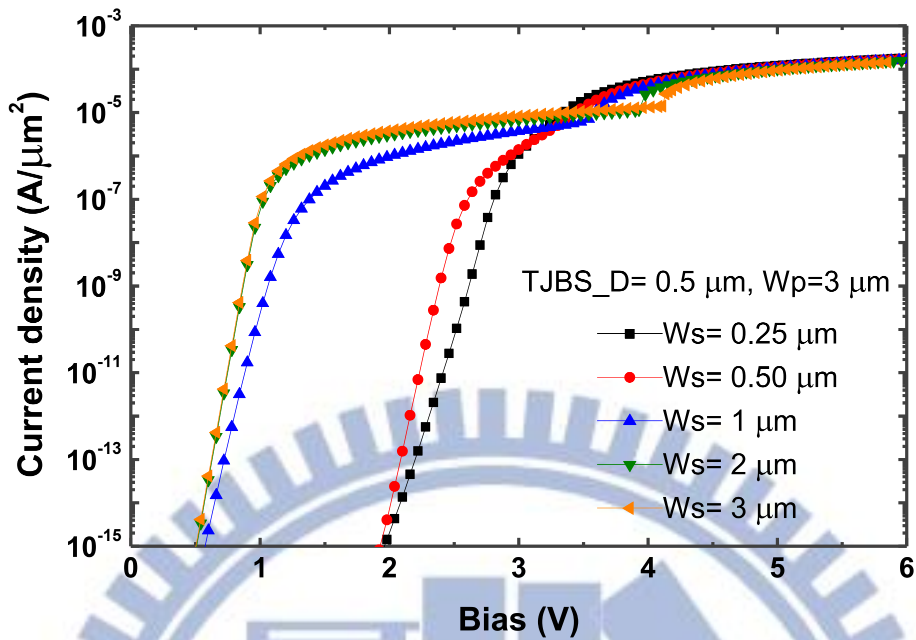

Fig. 3-17 Simulated forward characteristics of TJBS diode with D= 0.5 μm, Wp= 3.0 μm and different values of Ws.

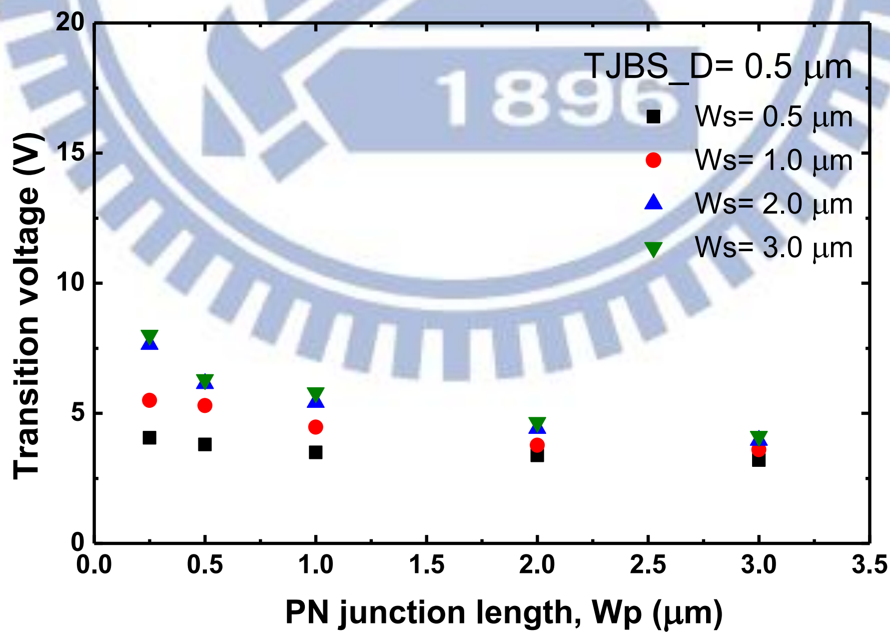

Fig. 3-18 Relations of transition voltage with Wp and Ws in TJBS diodes with D= 0.5 μm.

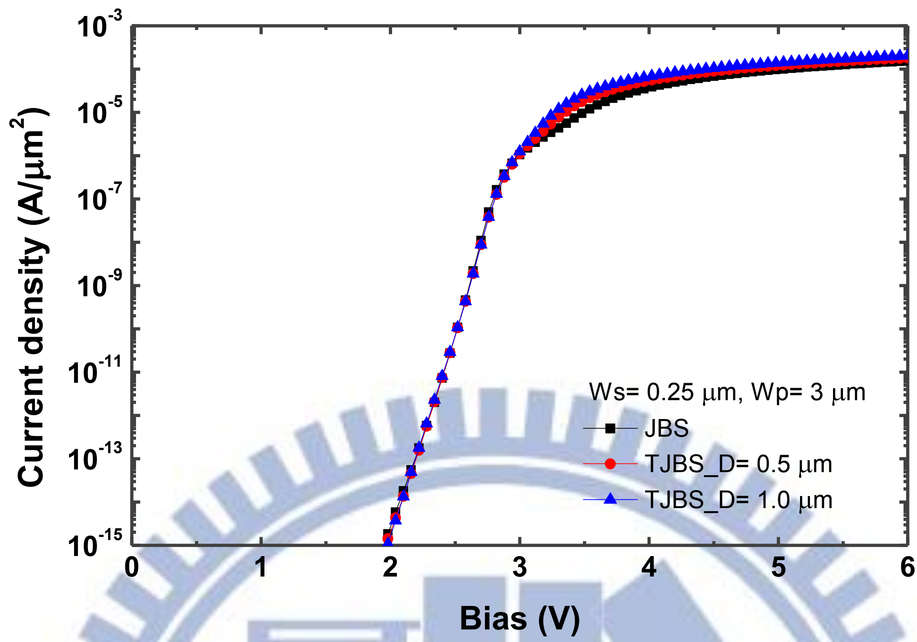

Fig. 3-19 Comparison of simulated forward characteristics of JBS diode and TJBS diodes with Ws= 0.25 μm and Wp = 3 μm.

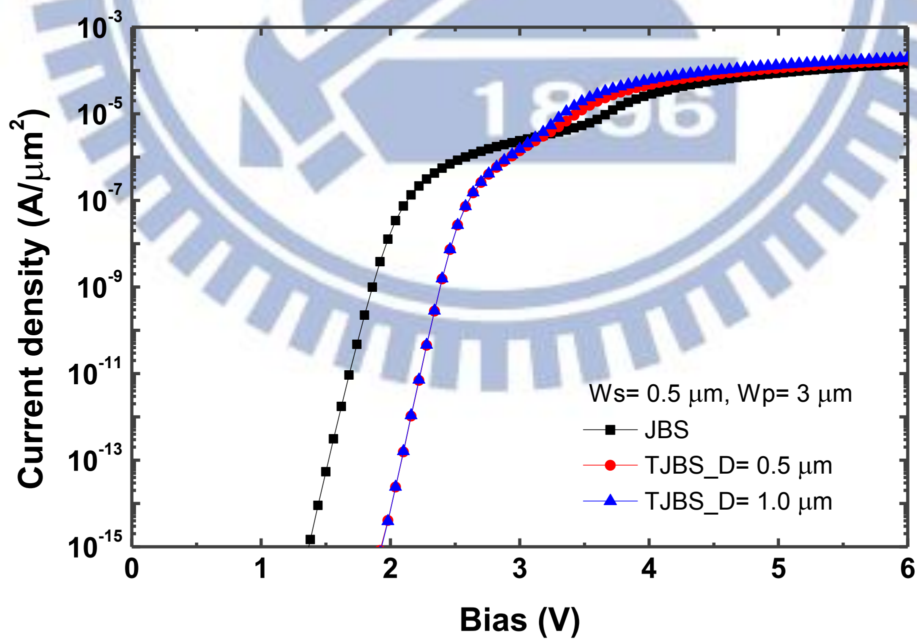

Fig. 3-20 Comparison of simulated forward characteristics of JBS diode and TJBS diodes with Ws= 0. 5 μm and Wp = 3 μm.

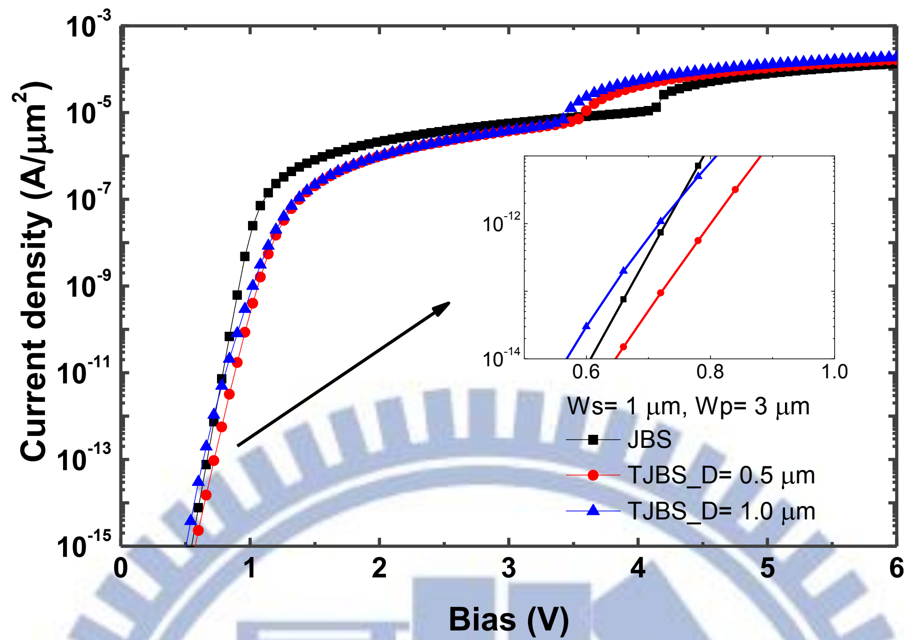

Fig. 3-21 Comparison of simulated forward characteristics of JBS diode and TJBS diodes with Ws= 1.0 μm and Wp = 3 μm.

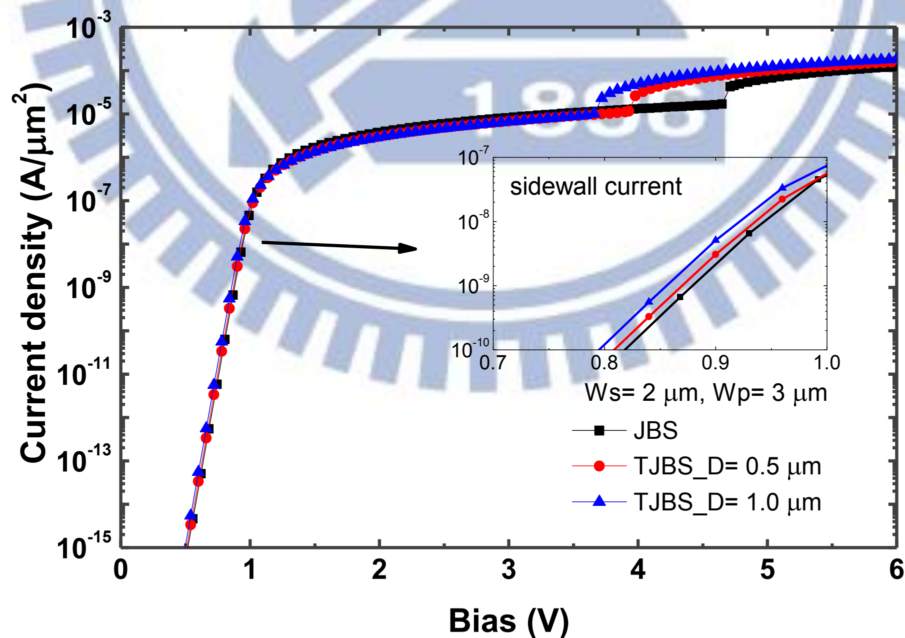

Fig. 3-22 Comparison of simulated forward characteristics of JBS diode and TJBS diodes with Ws= 2.0 μm and Wp = 3 μm.

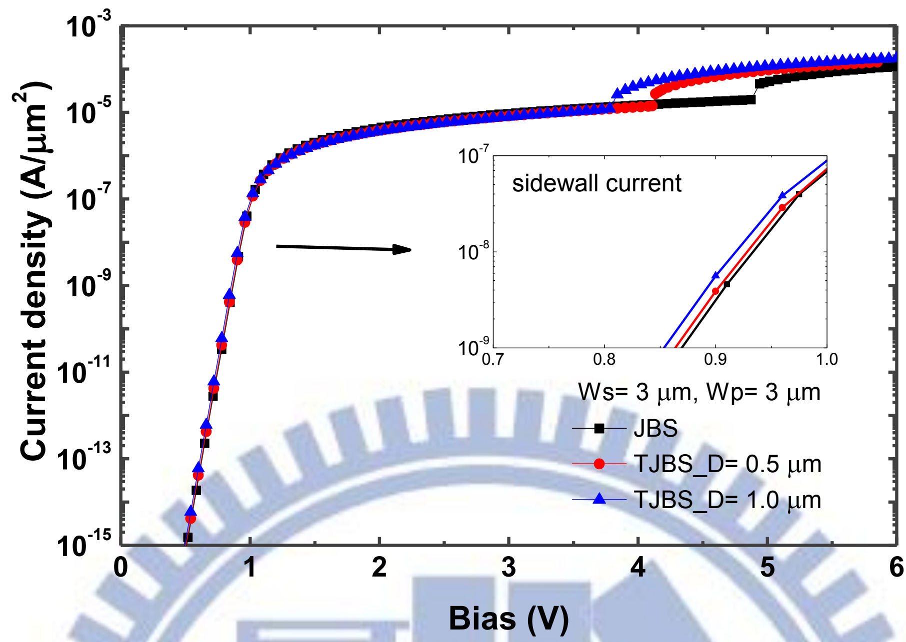

Fig. 3-23 Comparison of simulated forward characteristics of JBS diode and TJBS diodes with Ws= 3.0 μm and Wp = 3 μm.

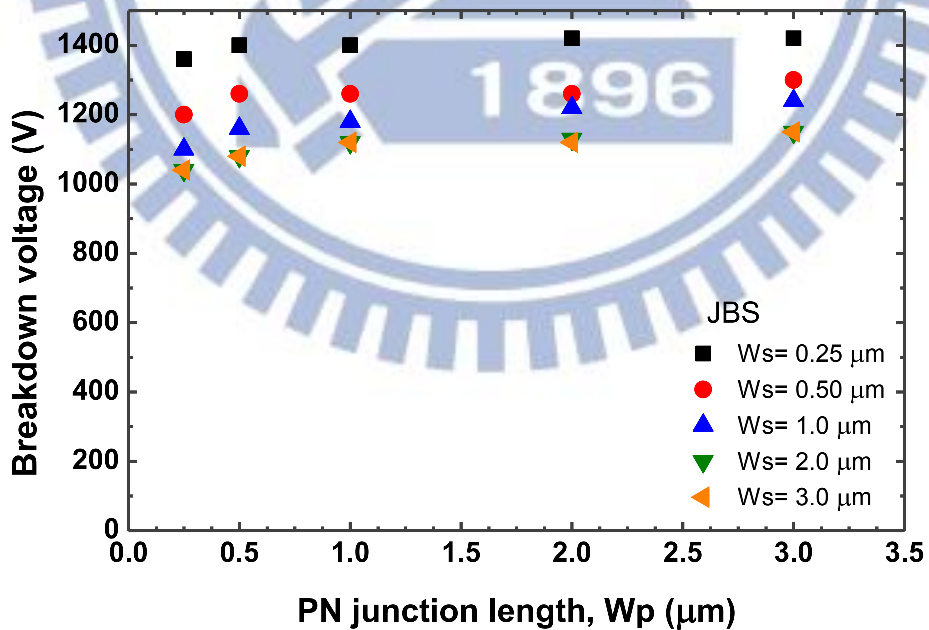

Fig. 3-24 Breakdown voltage of JBS diode with different parameters.

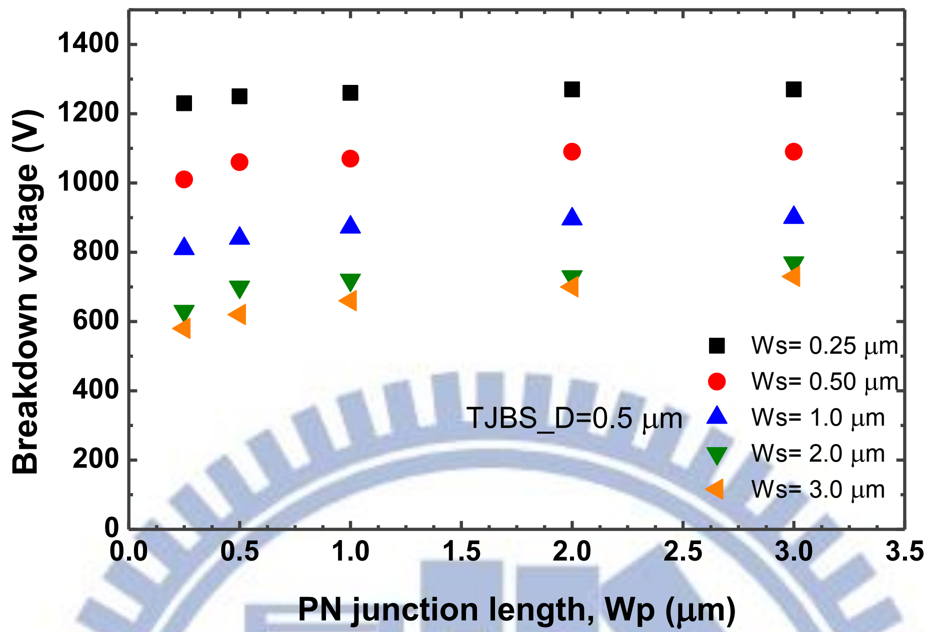

Fig. 3-25 Breakdown voltage of TJBS diode with D= 0.5 μm. and different parameters.

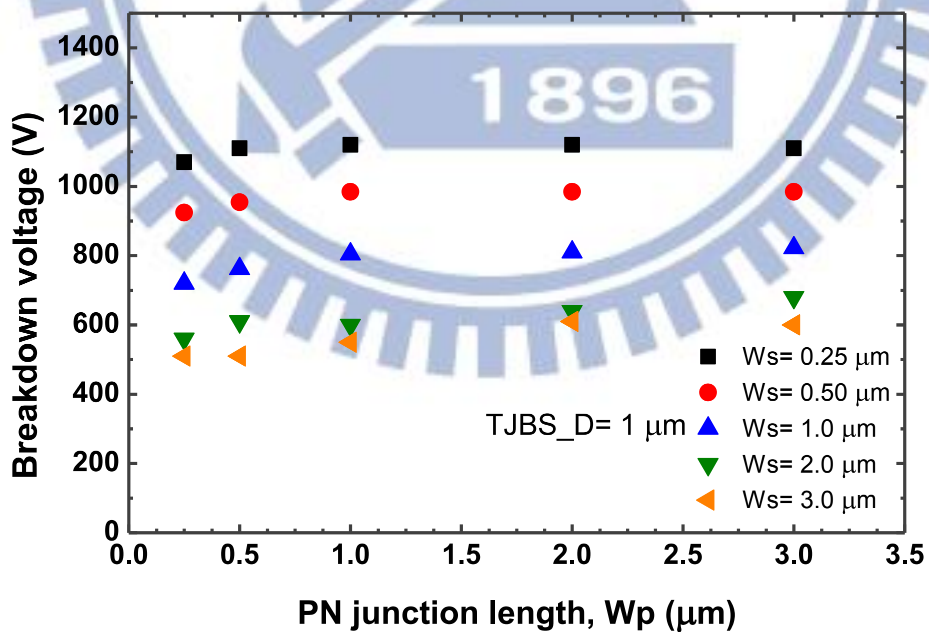

Fig. 3-26 Breakdown voltage of TJBS diode with D= 1 μm. and different parameters.

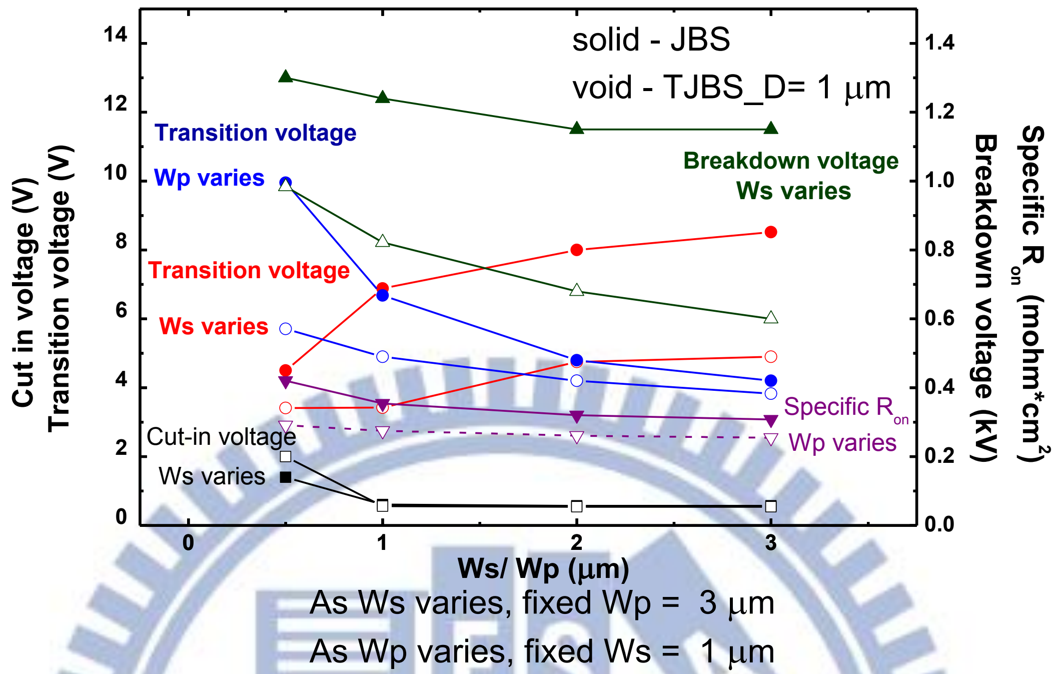

Fig. 3-27 Relations of different electrical characteristics with different parameters.

Chapter 4

Conclusions and Future works

4-1 Conclusions

In the thesis, we setup a conventional DLTS system. This DLTS system is composed of a semiconductor parameter analyzer of model Aglient B1500A with a multi-frequency capacitance measurement unit of model B1520A and a probe station of Lake Shore CPX-VF with a temperature heating controller. The DLTS system is verified with the commercial DLTS system produced by Sula Technologies, which is installed at the Department of Electrophysics in National Chiao-Tung University. Our DLTS system has the same DLTS result as the commercial system. The relative weaker signal intensity is due to longer measurement delay time of the B1520A.

The quality of 4H-SiC epi-layer as an important parameter of power devices is investigated using our DLTS system. For the un-implanted SBDs, no defect is detected. To those epi-layer damaged by nitrogen ion implantation, the DLTS shows large amount of defects. After 1050 ^{o}C post ion implantation annealing in N_2 ambient, different DLTS is measured due to the migration of defects. Almost all the signals of defects are mixed together, and it's hard to distinguish them. The only one mixed signal we can identify is composed of ID_4 and ID_8 at E_C-0.37 eV and E_c-0.45 eV, respectively. For the SBD experiences 1050 ^{o}C wet oxidation after ion implantation, the carbon interstitials generated by oxidation result in extra defects S2 at E_C-0.7 eV near the SiC surface. For the 1600 ^{o}C high temperature annealed SBD, almost all the defects are eliminated except for $Z_{1/2}$ at E_C- 0.6 eV. The $Z_{1/2}$ defect is regarded as a carbon vacancy and is originated from the n^+ substrate during high temperature

annealing. It can be eliminated by carbon ion implantation or oxidation.

The DLTS of the 4H-SiC MOS capacitor are dominated by oxide trap which overlaps the signal of interface state. The MOS capacitor with ion implantation or high temperature annealing shows the same structural defects in SBD. The dipole-like relaxation happens at higher pulse voltage and high temperature measurement, because dipole arranged well and faster de-trapping of electron. If signals from several kinds of defects are mixed in the DLTS, the direct extraction of interface state from DLTS would be incorrect.

In the part of TJBS diodes design, the effects of different geometric parameters of TJBS diodes are investigated and the design guidelines for TJBS diodes are figured out. In the view of forward bias characteristics, the cut-in voltage is influenced by the JFET effect of the neighboring pn junctions if the Schottky contact width is less than 1 μm. Deeper trench depth can slightly reduce the cut-in voltage due to the contribution of sidewall current. With the increase of Schottky contact width, the transition voltage for the current changing from unipolar conduction (Schottky junction dominant) to bipolar conduction (pn junction dominant) increases, while the increment of pn junction width and trench depth have opposite effect. The transition voltage influenced by the voltage drop on Schottky junction and pn junction, so all the geometric parameters should be taken into consideration. With lower transition voltage, higher bipolar conduction current could be obtained under the same forward bias. From the aspect of breakdown voltage, the breakdown voltage is mainly affected by the Schottky contact width and the trench depth. As the increase of Schottky contact width, the edge profile of the depletion region becomes curved, so the breakdown voltage reduces. The deeper trench is, the lower breakdown voltage is. Namely, TJBS diodes have lower breakdown voltage than JBS diodes due to the trench corner and the thinner epi-layer under the pn junction. Furthermore, TJBS

diodes suffer from the low breakdown voltage of its structural design unlike pn diode which can be compensated by junction termination. It is concluded that the TJBS didoes have the potential on higher current application, while for high breakdown voltage devices, the JBS diode is a better choice.

4-2 Future works

In this study, important results have been summarized in previous section. However, many works are worthy for further investigation. They are listed here.

4. The smoother and stronger DLTS signal can be obtained by shortening the sampling delay time. A much better signal can be obtained like commercial system. However, for the DLTS signal consist of multiple traps, and the improvement in signal intensity still does not help in distinguishing them. It's better to apply a lock-in amplifier such as SR830 or Laplace DLTS by computer computation. This helps the verification and extraction of defect energy so that more accurate result can be obtained.
5. The other works on DLTS system is to check the lowest defect density that can be measured by our DLTS system. The best choice is the 1600 ^{o}C annealing sample, which contains only one kind of defect. In addition, the defect density can be reduced by oxidation. By repeating the oxidation process, we can get the detect limitation of our DLTS system.
6. For TJBS diodes, the fabrication of device should be realized. Besides, different parameters can be involved in the reticle design to verify the results of simulation.
7. The cut-in voltage of JBS diodes is influenced by depletion region. By applying low Schottky barrier height metal, we can change the Schottky metal width to

modulate the cut-in voltage. In addition, the cut-in voltage modulation can be achieved by nitrogen implantation to contract the depletion region.

8. The transition voltage of TJBS diode is affected by the voltage drop on the pn junction, so the doping concentration and thickness of the epi-layer have its own influence, too. These factors would affect the device deign and should be studied.
9. The breakdown of TJBS diode occurs at the trench corner. Instead of a right angle, the trench corner can be a bevel or a rounding corner in practice. Different shapes of trench may also have different influences on the forward characteristics of TJBS diodes. The profile of p^+ implantation can be also studied to prevent the premature of breakdown in TJBS diode.
10. For trench with a gradual sidewall slope, the p-type ion implantation on the sidewall is relative easy to occur. With p-type doping on sidewall, a stronger JFET effect is expected, but the influence on the breakdown voltage is un-cleared. Besides, with different p-type concentration, different phenomenon would be observed, too.
11. The trench structure has been applied in JBS diodes to become TJBS diodes. Hence, it can be applied into the edge termination structure with above mentioned works. The effect of trench shape, implantation on sidewall or top of the un-etched epi-layer, and the trench depth can be taken into consideration to evaluate the trench termination structure.

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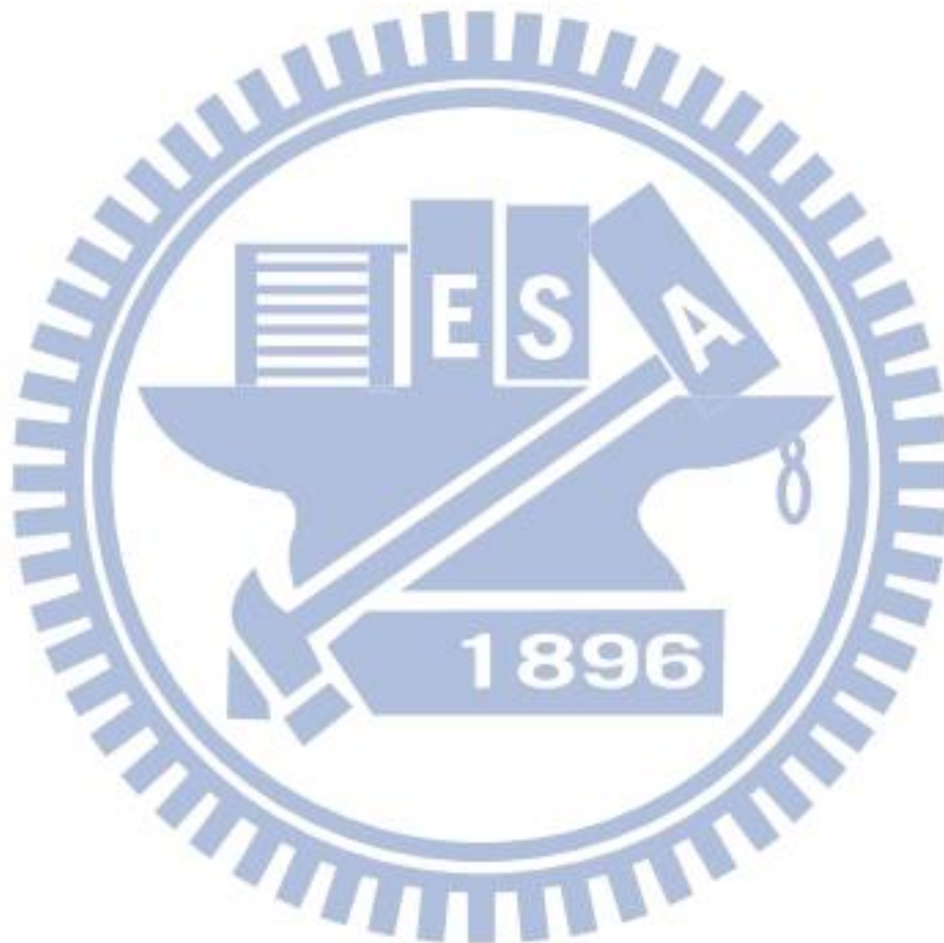

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碩士論文題目：

以深層暫態能譜分析碳化矽缺陷之研究暨溝槽式接面蕭基位障二極體之設計分析

A study on the Defect in SiC by Deep Level Transient Spectroscopy (DLTS) and Design Analysis of the SiC Trench Junction Schottky Barrier (TJBS) Diode