A 1 V 23 GHz Low-Noise Amplifier in 45 nm Planar Bulk-CMOS Technology With High-Q Above-IC Inductors

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***Abstract*—A 23 GHz electrostatic discharge-protected low-noise amplifier (LNA) has been designed and implemented by 45 nm planar bulk-CMOS technology with high-Q above-IC inductors. In the designed LNA, the structure of a one-stage cascode amplifier with source inductive degeneration is used. All high-Q above-IC inductors have been implemented by thin-film wafer-level packaging technology. The fabricated LNA has a good linearity where the input 1 dB compression point ($\mathrm{IP}_{-1\ \mathrm{dB}}$) is $-9.5\ \mathrm{dBm}$ and the input referred third-order intercept point (P_{IIP3}) is $+2.25\ \mathrm{dBm}$. It is operated with a 1 V power supply drawing a current of only 3.6 mA. The fabricated LNA has demonstrated a 4 dB noise figure and a 7.1 dB gain at the peak gain frequency of 23 GHz, and it has the highest figure-of-merit. The experimental results have proved the suitability of 45 nm gate length bulk-CMOS devices for RF ICs above 20 GHz.**

***Index Terms*—CMOS, electrostatic discharge (ESD) protection, 45 nm, K -band, low-noise amplifier (LNA).**

I. Introduction

THE rapid development of bulk-CMOS technologies makes the realization of low-cost and high-integration RF integrated circuits at frequencies above 20 GHz feasible. The low-noise amplifier (LNA) is a key building block in the RF receiver front-ends. So far, numerous bulk-CMOS LNAs designed at frequencies around 20 GHz have been reported [1]–[8], but not in 45 nm bulk-CMOS technologies. Among them, the single-ended structure has been used in [2]–[7], whereas the differential topology has been adopted in [1] and [8]. The inductive degeneration at the source of the input transistor is used in [2]–[3], [6]–[8] to achieve both noise and input impedance matching. To obtain high gain, the multi-stage configuration has been proposed [1], [5]–[8]. But they generally consume more power and lose the linearity performance. Generally, the single-ended structure has the advantage of a good noise figure (NF) and low-power consumption.

In this work, a LNA is designed and implemented in 45 nm gate length planar bulk-CMOS devices (fabricated at IMEC) to verify its feasibility in RF-IC design. The single-ended one-stage cascode structure with inductive source degeneration is adopted to achieve low power dissipation, high linearity, and good NF. The electrostatic discharge (ESD) protection circuits for both power pins and bias pins have been implemented in the designed LNA. The fabricated LNA has a small power consumption of 3.6 mW under 1 V power supply. It has good linearity performances with the values of $\mathrm{IP}_{-1\ \mathrm{dB}}$ and P_{IIP3} $-9.5\ \mathrm{dBm}$ and $+2.25\ \mathrm{dBm}$, respectively. Furthermore, the LNA has a NF of 4 dB and a gain of 7.1 dB at the peak gain frequency of 23 GHz. The measurement results of the fabricated LNA have the highest figure-of-merit (FOM) as compared with other LNAs.

The circuit design is presented in Section II, while the experimental results are described in Section III. Finally, the conclusion is given in Section IV.

II. Circuit Design

In the 45 nm planar bulk-CMOS technology, the transistor has been demonstrated with a peak cut-off frequency (f_T) around 300 GHz with the achievable transconductance efficiency (g_m/I_D) of 2.5 V^{-1}. In the back-end process, the 45 nm CMOS technology offers five layers of metal in the Cu damascene process and metal-insulator-metal (MIM) capacitor.

The circuit diagram of the designed one-stage LNA is shown in Fig. 1. The cascode amplifier formed by M_1 and M_2 is used to reduce the Miller effect of M_1 and to achieve good reverse isolation. The degenerative inductor L_s at the source of M_1 is used to provide the real-part impedance for the input impedance matching. With L_s, the design goals of both noise and input impedance matching can be achieved simultaneously. Furthermore, L_s does not seriously degrade the NF performance. However, increasing the value of L_s reduces the gain of the amplifier. The value of L_s in this design is set at 0.2 nH.

With a minimum channel length of 45 nm, the widths of M_1 and M_2 are chosen by setting the bias current to the optimal current density J_{OPT} of minimum noise figure $\mathrm{NF}_{\mathrm{min}}$ to minimize the noise contributions from M_1 and M_2. The J_{OPT} is $0.15\ \mathrm{mA}/\mu\mathrm{m}$ approximately, which is nearly independent of CMOS technologies [9]. The widths of M_1 and M_2 are chosen as 30 μm each when the power consumption is designed to be less than 5 mW from 1 V power supply. The input matching network has been designed by using L_g, C_1, C_2, and the parasitic capacitance C_{pad1} of the input pad.

The output is loaded with an inductor L_d to provide parallel resonance and to increase the gain at the desired frequency. The

Manuscript received September 19, 2008; revised January 12, 2009. First published April 24, 2009; current version published May 08, 2009.

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Digital Object Identifier 10.1109/LMWC.2009.2017611

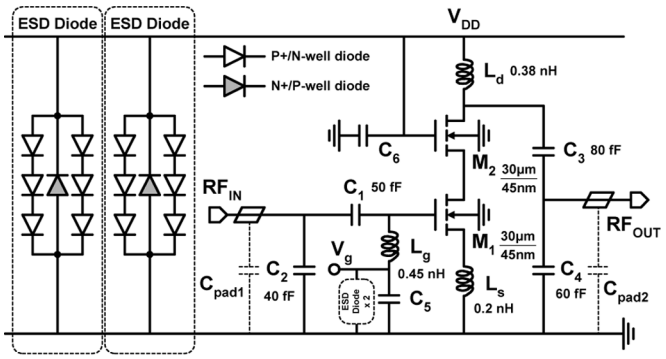

Fig. 1. Circuit diagram of the one-stage cascode LNA with ESD power clamp diodes.

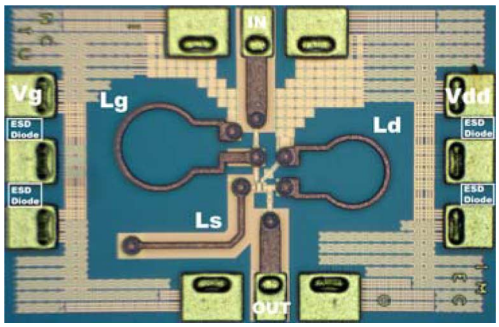

Fig. 2. Chip microphotograph of the one-stage cascode LNA with the size of $0.72 \times 1.12\ \mathrm{mm}^2$ including testing pads.

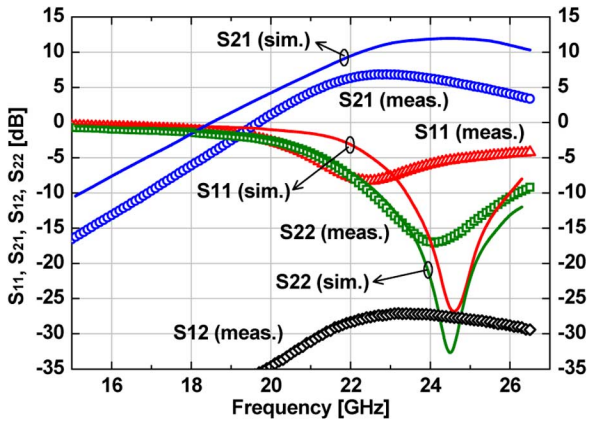

Fig. 3. Measured and simulated S-parameters of the one-stage cascode LNA.

output matching network has been designed to match 50 Ω by L_d, C_3, C_4, and the parasitic capacitance C_{pad2} of output pad. The bypass capacitors $C_5(C_6)$ is added between $V_g(V_{DD})$ and ground in order to stabilize the bias voltage (supply voltage) and to isolate the bias (supply) noise from entering the LNA.

In this design, the wafer-level packaging (WLP) technology [10] is used to realize the low-cost high-Q above-IC inductors L_d, L_g, and L_s. L_d and L_g are one-turn spiral inductors. L_s is a microstrip transmission line inductor, where the signal path is realized in the WLP process, and the ground path is realized by the metal-1 and metal-2 of the back-end process in this 45 nm gate length planar bulk-CMOS technology. In the WLP process, the 5 μm thick electroplated metal layer of Cu on the 20 μm low-K dielectric of BenzoCycloButhene (BCB) has been post-processed on top of the 45 nm planar bulk-CMOS process. From the HFSS simulation, the Q factors of L_d, L_g, and L_s at 23 GHz

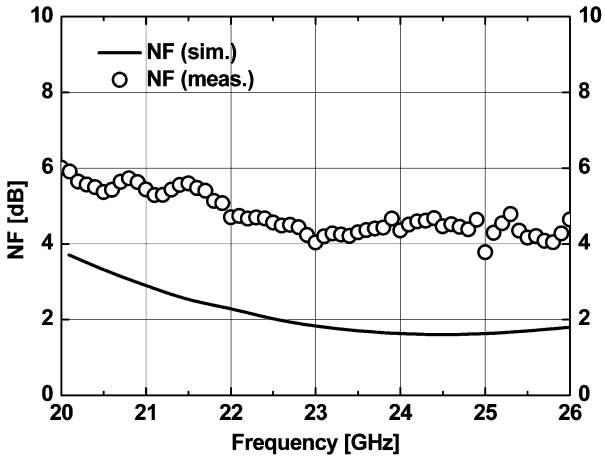

Fig. 4. Measured and simulated NF of the one-stage cascode LNA.

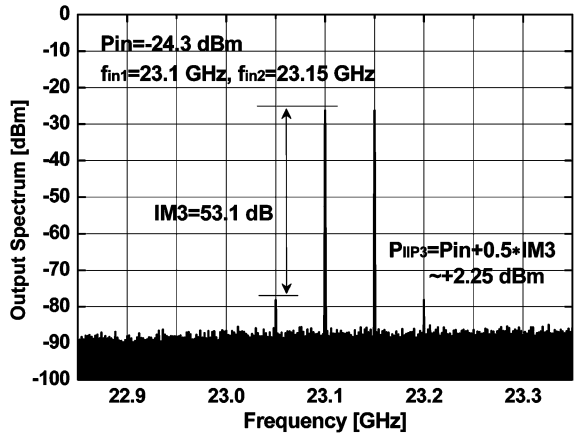

Fig. 5. Two-tone measured results of the one-stage cascode LNA.

TABLE I
HBM ESD ROBUSTNESS OF POWER-CLAMP STI DIODE

	Positive	Negative
V_{DD} (V_G) to V_{SS}	3 kV	6 kV

can be extracted as 41, 39, and 39, respectively. In addition, the values of L_d, L_g, and L_s are 0.38 nH, 0.45 nH, and 0.2 nH, respectively. The shallow trench isolation (STI) $P+/N$-well and $N+/P$-well diodes are implemented between supply/bias (V_{DD} and V_G) and ground for ESD protection. The drawing dimension of each STI diode is 19.35 μm by 1.85 μm.

III. EXPERIMENTAL RESULTS

Fig. 2 shows the chip microphotograph of the fabricated LNA where the dimension is of 0.72 mm × 1.12 mm including the testing pads. On wafer measurements have been performed on the LNA. The circuit draws 3.6 mA from a 1 V supply voltage. The measured and simulated S-parameters are shown in Fig. 3 where the measured gain S_{21} of the LNA is 7.1 dB. In this experimental chip, the measured S_{11} of around -8 dB is marginally acceptable. The measured and simulated NF are shown in Fig. 4 where the measured NF at 23 GHz is about 4 dB. The simulated characteristics are based on the preliminary version of 45 nm planar bulk-CMOS transistor models. The measured

TABLE II
PERFORMANCE COMPARISON WITH BULK-CMOS LNAS AROUND 20 GHZ

	Bulk-CMOS Technology	Freq. (GHz)	Gain (dB)	NF (dB)	IP_{-1dB} (dBm)	P_{IIP3} (dBm)	Supply (V)	Power (mW)	Area (mm2)	FOM_{LNA} (GHz)	Circuit topology [a]
This work [b]	45 nm	23	7.1	4	–9.5	+2.25	1	3.6	0.81	15	1-stage cascode
[1] ISSCC'08	130 nm	18	22.4	4.1	--	–5.6	1.5	36	0.23	1.2	2-stage, pseudo differential
[2] RFIC'06	130 nm	26.2	8.4	4.8	--	–13	1	0.8	0.16	2.1	1-stage cascode
[3] SiRF'06 [b]	90 nm	20	8.4	3.1	--	+4.8	1.4	14	0.56	10.9	1-stage cascode
[4] RFIC'07	90 nm	28.5	20	2.9	–17	–7.5	1	16.25	0.67	3.3	2-stage, CS+Cascode
[5] APMC'05 [b]	90 nm	20	8	5.3	--	+3.8	0.66	11	0.84	4.6	2-stage, CS+CS
[6] MWCL'04	180 nm	24	13.1	3.9	–12.2	–0.54	1	14	0.34	4.7	2-stage, CS+CS
[7] MWCL'04	180 nm	23.7	12.86	5.6	–11.1	+0.24	1.8	54	0.73	1.2	3-stage, CS+CS+CS
[8] MWCL'05	130 nm	20	9	5.5	–11	–4	1.2	24	0.8	0.4	2-stage differential cascode

[a] CS: common source. [b] Above-IC inductors in WLP process are adopted.

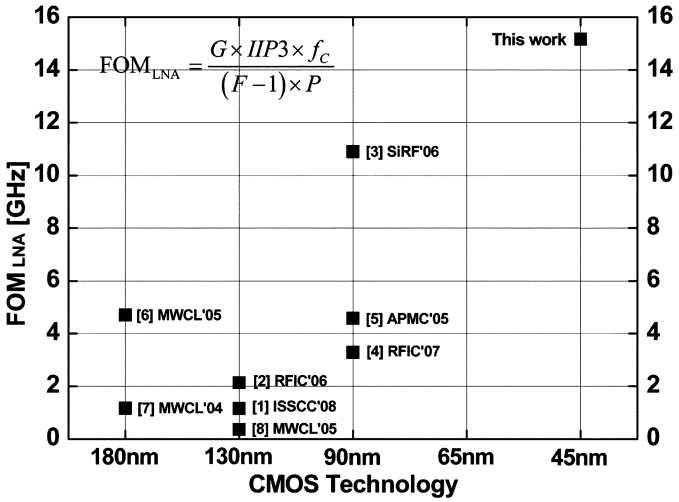

Fig. 6. Comparison with the published bulk-CMOS LNAs around 20 GHz by $\mathrm{FOM_{LNA}}$.

value of $\mathrm{IP_{-1\ dB}}$ is $-9\ \mathrm{dBm}$. The linearity performance is verified by two-tone testing. Two RF inputs with the same input signal power level P_{in} of $-24.3\ \mathrm{dBm}$ are at the frequencies of 23.1 and 23.1 GHz. The two-tone measured results shown in Fig. 5 reveal that the P_{IIP3} is $+2.25\ \mathrm{dBm}$. It is shown that the fabricated LNA has good linearity.

Human-body-model (HBM) ESD tests were performed at the supply and biasing pads for both positive and negative test voltages. The HBM ESD robustness of power-clamp STI diodes is summarized in Table I. In the worst case, HBM ESD protection level of 3 kV is achieved.

The measured results of the fabricated LNA are compared with those of published CMOS LNAs around 20 GHz in Table II. As can be seen from Table II, the fabricated LNA has good linearity performance as well as low power consumption. The LNAs in [3] and [5] have better linearity performance than this work at the cost of higher power consumption.

To characterize the performance of all LNAs, the FOM defined in [11] has been used. It can be written as

$$\mathrm{FOM_{LNA}} = \frac{G \times \mathrm{IIP3} \times f_C}{(F-1) \times P} \tag{1}$$

where G represents the gain, *IIP3* denotes the linearity, f_C is the operating frequency, F is the noise factor, and P is the power dissipation. In (1), G and F are in absolute values, P and P_{IIP3} are in units of mW, and f_C is in the unit of GHz. The values of $\mathrm{FOM_{LNA}}$ are calculated for different LNAs and are presented in Table II and Fig. 6. As shown in Fig. 6, the fabricated 45 nm CMOS LNA has the highest $\mathrm{FOM_{LNA}}$ as compared with other published bulk-CMOS LNAs around 20 GHz.

IV. CONCLUSION

A 23 GHz LNA has been designed and fabricated in 45 nm gate length planar bulk-CMOS technology. The fabricated LNA has a NF of 4 dB and a P_{IIP3} of $+2.25\ \mathrm{dBm}$ at the 1 V supply voltage and 3.6 mW power consumption with the chip size of $0.72 \times 1.12\ \mathrm{mm^2}$. As compared with other bulk-CMOS LNAs around 20 GHz, the fabricated LNA has good linearity, low power dissipation, low NF, and the highest FOM. From the above experimental results, it is shown that 45 nm gate length planar bulk-CMOS technology is suitable for the design of high-performance LNAs and other RF ICs above 20 GHz.

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