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博 士 論 文

以凱文錫球結構及有限元素分析法研究覆晶銲錫凸塊與微凸塊的電遷移破壞機制

Study of Failure Mechanisms in Flip-Chip Solder Joints and Microbumps under Electromigration Using Kelvin Bump Structures and Finite-Element Analysis

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摘要

於此研究中，共三種預先設計好、包含凱文錫球結構之銲錫凸塊被用於非破壞性觀測電遷移測試時的電阻變化。

第一種是覆晶銲錫凸塊，其凸塊電阻小於 1 毫歐姆、成長時呈現凹口向上之趨勢，直到凸塊電阻上升超過 10 毫歐姆時，會開始急遽上升而後斷路；內部對應之微結構是孔洞的成核與成長，孔洞首先生成於電流集中區然後沿著介金屬化合物與銲錫間介面成長，在測試的末期，電遷移導致的相粗化減緩了電遷移產生的破壞，且可以發現孔洞在電遷移測試末期會分成兩段；且根據實驗結果，我們計算得到一個可表達剩餘接觸面積與凸塊電阻的關係式。

第二種試片則是六微米高的微凸塊，其微凸塊電阻呈現凹口向下之行為，從 15 毫歐姆開始急遽增加，然後在測試 400 小時後達到一個定值，早期急劇增加的幅度約 5 毫歐姆，這與有限元素分析法所得之結果相符；在電遷移測試中，陰極金屬墊層會與銲錫反應並將整個微凸塊轉變為 Ni_3Sn_4，Ni_3Sn_4 具有較銲錫佳之抗電遷移特性，所以導致凸塊電阻維持一個定值；在不同角度的凸塊電阻指出了電流集中效應雖然沒有發生在銲錫中，依舊發生在金屬墊層裡，對於微凸塊來說，完整的電壓降應該是由 0 度所量到的值，而這個值比 180 度所得到的值高了 7 倍，也就是說，其實微凸塊所造成的容／阻延遲相當的大；而為了要簡化描述微凸塊電阻、電流集中比與凸塊尺寸的關係，一個數值分析模型在此被提出，根據此模型，微凸塊電阻與電流集中的關係可以被表達為簡單的關係式。

最後一種試片則是十微米高的微凸塊，其電阻開始時呈現凹口向下，然後轉

變為凹口向上，原因在於，其銲錫的量太多，而無法被中介板端的金屬墊層消耗完；開始時，凹口向下的反應行為與矮的微凸塊相當接近，不過因為銲錫的量太多，所以在電子流向上（由中介板端流向晶片端）之微凸塊中，2 微米厚之鎳層會受電遷移影響而融入銲錫中，當這些鎳用完以後，孔洞就會產生在這些金屬墊層本來的位置上，且造成電阻曲線又轉變成凹口向上。

根據這些結果，由凱文錫球結構所獲得凸塊電阻的曲線行為經由有限元素模型的幫助，可以在測試中用來檢視其微結構的變化，有限元素模型可以很清楚的表現出不同電遷移階段電流密度的演進，因此可以幫助預測電遷移破壞的機制；此外，凱文錫球結構與過去最常用於分析墊遷移之雛菊花環結構完全的相容，兩個值可以在同時量測取得，此一點是凱文錫球結構之一大優勢。

Abstract

In this study, three types of solder bump samples with Kelvin bump structures were employed to monitor non-destructively the evolution of resistance during electromigration (EM) testing.

The first type of sample was flip-chip bumps. The bump resistance was found to be less than 1 mΩ and increase as a concave-up curve. After the bump resistance increased to more than 10 times its initial value, it started to grow rapidly and then failure. The corresponding microstructure showed void nucleation and propagation. The void first formed near the current crowding spot and then grew along the interface between the intermetallic compound (IMC) and the solder. At the end stage of EM testing, phase coarsening caused by EM retarded the failure, and the void split into two parts. The relation between the remaining contact area and the bump resistance was calculated.

The second type of sample was 6-μm microbumps. The microbump resistance curve was concave-down. It started around 15 mΩ, increased rapidly in the beginning, and then reached a constant value after 400 hr of testing. The increase in the early stage of testing was around 5 mΩ, which was reasonable when compared with the results of finite-element models (FEMs). During EM testing, the cathode-side under-bump-metallization (UBM) reacted with the solder and transformed the entire microbump into Ni_3Sn_4. Ni_3Sn_4 has better EM resistance than the solder and caused the bump resistance to remain at a constant value. The bump resistances at different angles indicated that current crowding still took place, but in the Cu UBM and not in the solder. The complete voltage drop across the microbump was the value obtained at

0°. However, the bump resistance obtained at 0° was 7 times larger than that measured at 180°. That is, the RC delay caused by microbump is actually very large. For simplicity of description on the relation between microbump resistances, crowding ratio, and structural dimensions, a numerical model was built. The expressions of microbump resistance and the crowding ratio were also obtained.

The last type of sample was the 10-μm microbumps. The resistance behaved first concave-down and then concave-up because the solder was too much for the interposer-side UBM to consume. The concave-down curve was first observed for the same reason as that of the low-bump-height case. However, the height of the solder was around 10 μm, which was too high for the interposer-sider UBM to react with. When the electrons flow upward (from interposer to chip), the interposer-side UBM, 2-μm Ni, was the cathode side. Driven by EM, the-2μm Ni quickly dissolved into the solder. After the 2-μm Ni ran out, the void was formed, causing the bump resistance curve to become concave-up again.

The solder height affected the failure mechanism. When the solder height was 25 μm, void propagation was the main failure mechanism. When the solder height decreased to 10 μm, the mechanism became the combination of void propagation and IMC growth. When it was 6 μm, the failure mechanism changed to IMC growth only. The FEM described clearly the evolution of current density distribution at various stages of EM and therefore helped predict accurately the failure mechanism. Moreover, the Kelvin bump structure is compatible with the generally used daisy chain structure. Both bump resistance and daisy chain resistance could be obtained at the same time.

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能夠博士班就讀期間順利完成本研究，敝人的指導教授陳智老師自是功不可沒，當我面臨研究瓶頸的時候不斷提供寶貴而適切的建議與幫助，而在成果豐碩的時候也不吝於給予熱烈的鼓勵。此外，正所謂身教重於言教，陳智老師對於研究積極的熱誠與付出更是令我尊敬的榜樣，也因為追隨著陳智老師這樣的目標，本研究才得以順利完成。且於就學過程中，敝人經由陳智老師推薦而參與龍門計畫，因而難能可貴的得到了一年在異鄉求學的經驗，其中的感謝之情難以言述。

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Chapter 1. Introduction

1.1. Flip-Chip Technology

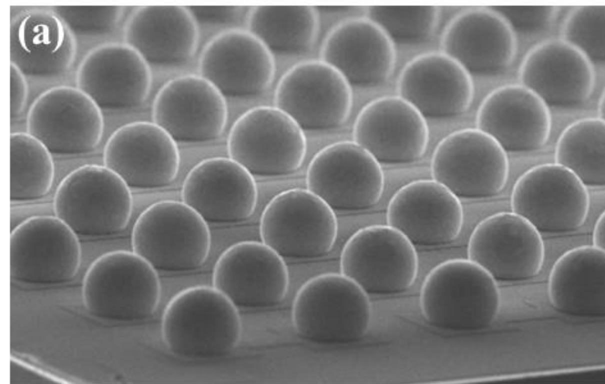
In order to satisfy the requirement of miniaturization of portable devices, flip-chip technology has been adopted for high-density packaging due to its excellent electrical characteristic and superior heat dissipation capability [1-2]. Owing to the demand for higher performance in microelectronics devices, flip-chip technology was adopted to generate more signals and power interconnections than wire bonding in electronic devices. In the 1960s, IBM first developed the flip-chip technology, known as controlled-collapse-chip-connection (C4) [3-5]. In the C4 technology, high-Pb solder with high melting temperature (around 320℃) was used as the joint material [6]. At that time, chips were aligned on ceramic substrates. This C4 technology gained wide utilization in the 1980s since it provided advantages in size, performance, flexibility, and reliability among all packaging methods. Because of area array capability in flip-chip technology, product size, solder bump height, and interconnect length are all effectively reduced, providing higher input/output (I/O) count and faster speed in electronic devices.

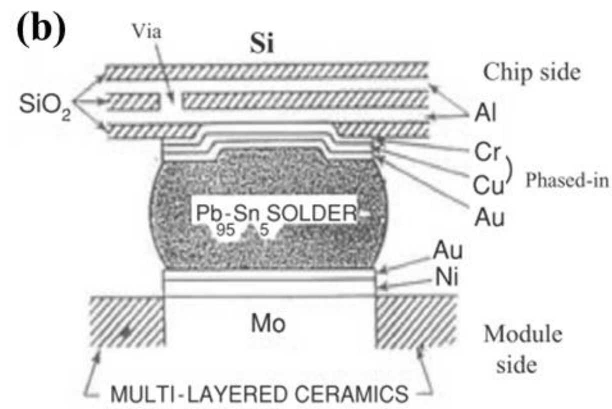
In the procedure of flip-chip assemblies, solder bumps need to be deposited first onto the under bump metallurgy (UBM) on the chip side. The functions for under bump metallurgies are: (1) to adhere well on the underlying metal line such as Al or Cu, and on the surrounding IC passivation layer, (2) to act as a strong barrier, thus preventing the diffusion of bump metals in the integrated circuit (IC), and (3) to become readily wettable to the bump metals during solder reflow. For example, a thin film Cr/Cu/Au UBM is adopted for the high-Pb solder alloy in the C4 technology.

The tilt view of solder joints on silicon ship is shown in Figure 1-1 (a). Figure

1-1 (b) is the cross-sectional view of the flip-chip solder joints. As depicted in Figure 1-1 (c), the chip with IC is then placed upside down (flip-chip), and all the joints are formed simultaneously between chip and substrate during the reflowing process. In the flip-chip process, electrical connections are the array of solder bumps on the chip surface; hence, the interconnect distance between package and chip is effectively reduced. In addition, the consequent resistance / capacitance (RC) delay is also reduced, too. The density of I/O is limited by minimum distance between adjacent bonding pads. For high-end devices and when size reduction is the main concern, area-arrayed flip-chip technologies offer the only choice that meets the current needs.

However, the flip-chip technology continues to evolve due to certain concern. In order to reduce the budget of the consumer electronics, polymer substrates, such as Bismaleimide Triazine (BT) or Flame Retardant 4 (FR4), are induced to replace ceramic substrates. Consequently, high-Pb solder is no longer used due to its high melting temperature (320℃) since polymers have very low glass transition temperature. Instead, the eutectic SnPb (E-SnPb) solder alloy is used in view of its low melting point of 183℃. Next, owing to environment concern, Pb-free solder alloys replace toxic Pb-containing solder alloys thus rendering thin-film UBMs no longer suitable for the original purpose. Therefore, electroplated 5-μm Cu or 5-μm Cu/3-μm Ni was used as the UBM for the Pb-free solder joints to avoid balling that comes with the adoption of the Pb-free solder alloys. With these evolutions, several kinds of solder alloys and UBMs have been proposed for flip-chip assemblies, and the many combinations make the flip-chip technology complicated and complex to study. Nevertheless, knowledge of the best solder alloy and UBM will be of much use and provide lots of benefits to the companies.





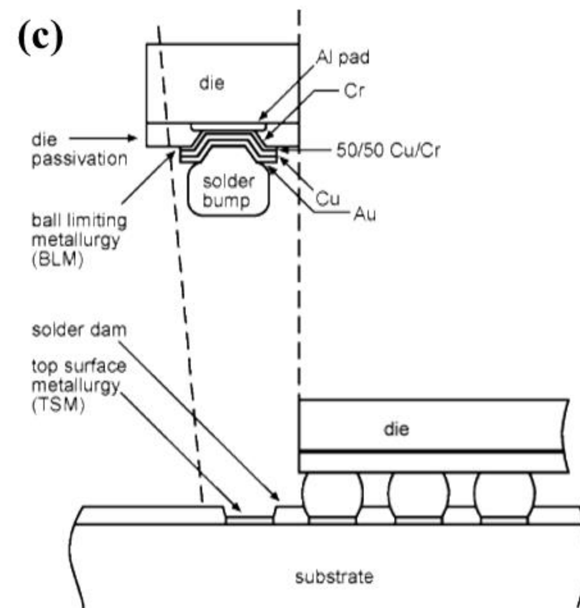


Figure 1-1 (a) Tilt-view SEM image of solder bumps array on silicon die [2]; (b) a flip-chip solder joint connecting the chip side and the substrate side [2]; and (c) the chip placed upside down onto the substrate and the joint formed simultaneously between chip and substrate by reflow [1].

1.2. Microbump Technology

In order to keep up with the increasing demand for higher density and Input / Output (I/O) count in high-performance electronics, size of individual devices must shrink accordingly. However, further shrinking of device size under nano-scale is extremely challenging and not cost-effective. Consequently, some solutions have been proposed to meet the inevitable trend and three-dimensional integrated circuit (3D-IC) has emerged as a preferable solution for the next-generation products. 3D-IC can be utilized mostly due to the improvement of three key technologies: wafer thinning, through-silicon-via fabrication, and microbump bonding with microbumps playing an important role in serving as interconnects between different chips [7-9]. Presently, 3D-IC is mostly fabricated by stacking chips vertically and interconnecting chips with wire-bonding at the edge of chips. Such packaging method reduces the product size, but the electrical performance is limited by both high resistance and inductance of wires. Significant RC delay may occur under high wire resistance. Therefore, the utilization of ultra-fine-pitch microbumps has become the most promising alternative to wire-bonding in 3D-IC due to its shorter interconnection and higher density.

The main differences between a microbump and a flip-chip bump are the dimension and the volume, which significantly affect both electrical performance and metallurgical reactions. The dimensions of flip-chip bumps are usually 100 micron in diameter and 100 micron in height. However, the diameter and the height of a microbump are about 20-30 micron, which is only one fifth that of a flip-chip bump. As a result, the contact area in a microbump is only 4% that of a flip-chip bump, and the volume is less than 1% that of a flip chip bump. The reduction of both dimensions and volume has dramatic effect the electrical performance and metallurgical reactions. In today's circuit design, each solder joint will carry 0.2 A and it is expected to be doubled

in the near future. [10] As a result, the average current density in a 20-μm microbump is about 5×10^4 A/cm^2 when a current of 0.2 A is applied. Electromigration effect in the solder is activated under such high current density. [11-13] Therefore, it is imperative to understand the electrical behavior inside a single ultra-fine-pitch microbump solder joint. Some researchers have reported the value of resistances in microbumps, but there is no study yet examining specifically the current density distribution, and the relationship between current crowding effect and microbump resistance. [14-18]

Al-Sarawi *et al*. and Ladani *et al*. have reported that the 3D-IC packaging owns many outstanding advantages comparing with 2D packaging. The advantages include (1) ability of multifunction integration; (2) better performance; (3) higher I/O density; (4) low power consumption; (5) lower cost; (6) parallel processing ability; and (7) lower delay and noise [19-20]. Furthermore, Patti claimed that 3D-IC packaging technology is the hope for industry to maintain Moore's law [21]. Figure 1-2 (a) indicates the difference between 2D and 3D packaging structure in the fabrication of integration circuits, and Figure 1-2 (b) tells the difference between SIP and SoC technology, which are already applied generally in industry and 3D-IC technology [22]. However, according to the recent issues and phenomena found during the development of 3D-IC, Tu proposed several important topics including (1) Joule heating effect; (2) electro- and thermo-migration; (3) warpage; (4) IMC formation in microbumps; and (5) thermal stress [7].

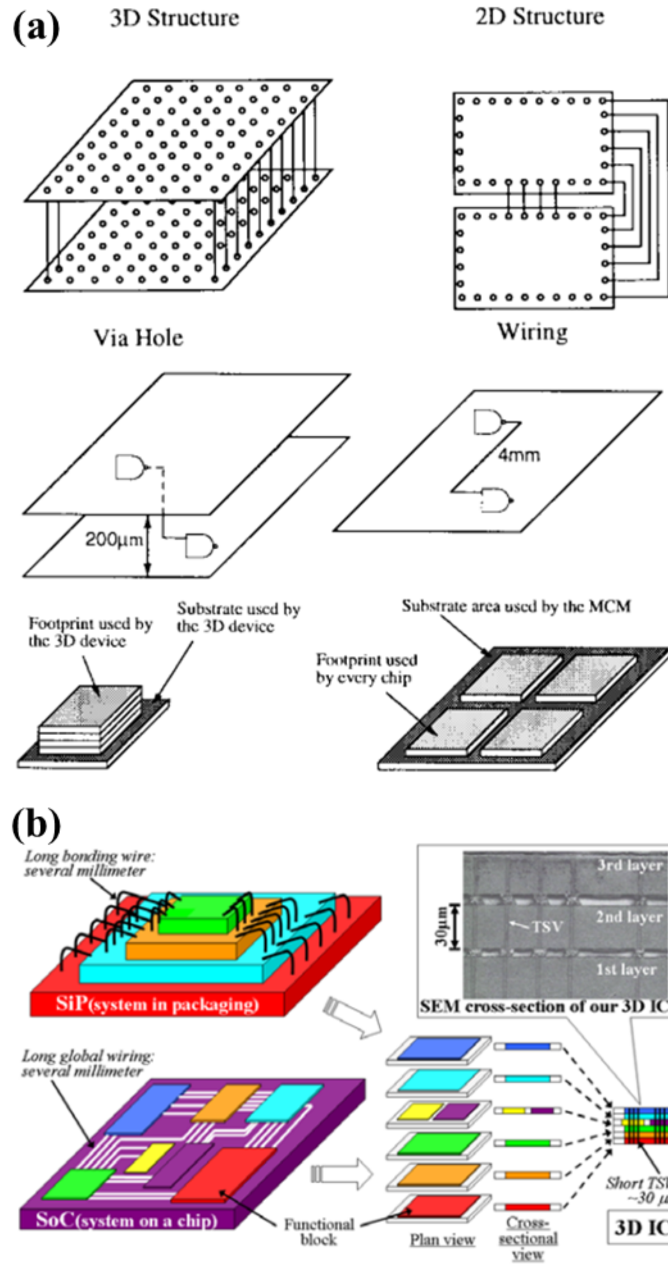


Figure 1-2 (a) Difference between 2D and 3D structure in fabrication of integration circuits [19]; and (b) difference between SIP/SoC and 3D-IC technology [22].

1.3. Electromigration

Electromigration (EM) has been the most persistent reliability issue in interconnects of microelectronic devices. Electromigration is the phenomenon of mass transportation due to momentum transfer from the electron flow in the high-density current. Such a mechanism results in open or short circuit modes of failure. The mechanism impacts both the design and manufacturing of metallization. For EM in metal, the driving force of the net atomic flux consists of two forces. They are (1) the electrostatic force, which is the direct action of electrostatic field on the diffusion atom, and (2) electron wind force, which is the momentum exchange between moving electrons and the ionic atoms. These two forces can be expressed as [23]

$$F = F_{direct} + F_{wind} = Z^{*}eE = (Z^{*}_{el} + Z^{*}_{wd})eE \qquad \text{Equation 1-1}$$

Where Z^* is the effective charge number, e is the electron charge, and E is the electric field. The effective charge Z^* consists of two terms, Z_{el}^* and Z_{wd}^*. Z_{el}^* is positive and can be regarded as the nominal valence of the diffusion ion in the metal when the dynamic screening effect is ignored. When these positively charged metal ions are under the field effect, this so-called “direct force” draws atoms toward the negative electrode. On the contrary, Z_{wd}^*, the wind force, is usually negative and represents the momentum effect from electron flow that pushes atoms towards the positive electrode. Generally, the electron wind force dominates and is found to be on the order of 10 for a good conductor, such as Ag, Al, Cu, Pb, and Sn [10]. Z_{wd}^* can also be positive, but it is found only in transition elements with complex band structures [10]. The atomic flux is related to the electric field and thus the current density. The flux equation can then be expressed as follows:

$$J_{em} = C\frac{D}{kT}Z^{*}eE \qquad \text{Equation 1-2}$$

$$E = \rho j \qquad \text{Equation 1-3}$$

Where C is the atomic concentration, D is the atomic diffusivity, k is Boltzmann's constant, and T is temperature. ρ is the resistivity and j is the current density. The flux is a function of temperature. As shown in the equation below, the atomic diffusivity is exponentially dependent on temperature.

$$D = D_0 \exp\left(-\frac{Q}{RT}\right) \qquad \text{Equation 1-4}$$

Where D_0 is the diffusion coefficient, R is the gas constant, and Q is the activation energy of diffusion. The equation of flux indicates that it is related only to the magnitude of current density and temperature but not to time. As time goes by, the flux maintains the same as long as the microstructure does not change significantly.

Electromigration (EM) was first observed in Al metal interconnects. Less than 0.2% of Cu atoms were added to the Al line to reduce the EM effect [10]. Blech first developed a structure of a short Al or Cu strip in the base line of TiN to conduct EM tests, as shown in Figure 1-3 (a) [25-27]. Because Al or Cu, with the exception of Ag, as electric field was applied on the two ends of the TiN line, the electric current in TiN took a detour and went along the strip of Al or Cu. After EM testing, a depleted region occurs at the cathode and an extrusion is observed at the anode. Figure 1-3 (b) is the SEM image of the morphology of a Cu strip tested for 99 hr at 350℃ with current density of 5×10^5 A/cm^2. According to mass conservation, both depletion and extrusion should occupy the same volume. The drift velocity can then be calculated from the depletion rate.

In recent years, an impetus to study EM in very fine conductors has arisen from the development of very large-scale integrated circuits. The conductors are not only interesting in small dimensions; they are often assembled into multilayered structure with a certain combination of conductors and insulators. This gives rise to EM problems which is distinctly different from the simple single-level conductor. The

metal layer is a two-dimensional conductor film that can be considered as an ensemble of grain boundaries and their intersections as illustrated in Figure 1-3 (c). Experimental observations have indicated that in most cases, mass depletion and accumulation initiate at grain boundary intersection, such as triple junctions. Mass depletion would eventually lead to the formation of voids or cracks while mass accumulation would result in hillocks or whiskers. The reason why the grain boundary intersections are likely the failure sites is that they often represent the spots where the mass flux would diverge or converge most. At the grain boundary intersection, there could be abrupt changes in grain size, which produce a change in paths for mass movement. Moreover, there could also be a change in atomic diffusivity due to the change in grain boundary microstructure.

In recent years, damascene structure has been developed to form Cu interconnect. Cu material is employed to replace Al due to its high electric conduction. Because Cu has higher melting temperature, its diffusion mechanism is surface diffusion instead of grain boundary diffusion [28]. As for solder joints with lower melting temperature, the diffusion mechanism is lattice diffusion for most solders at a typical operation temperature of an electronic device around 100℃. Table 1-1 lists the melting temperatures of Al, Cu, and SnPb solder and their corresponding diffusion mechanisms.

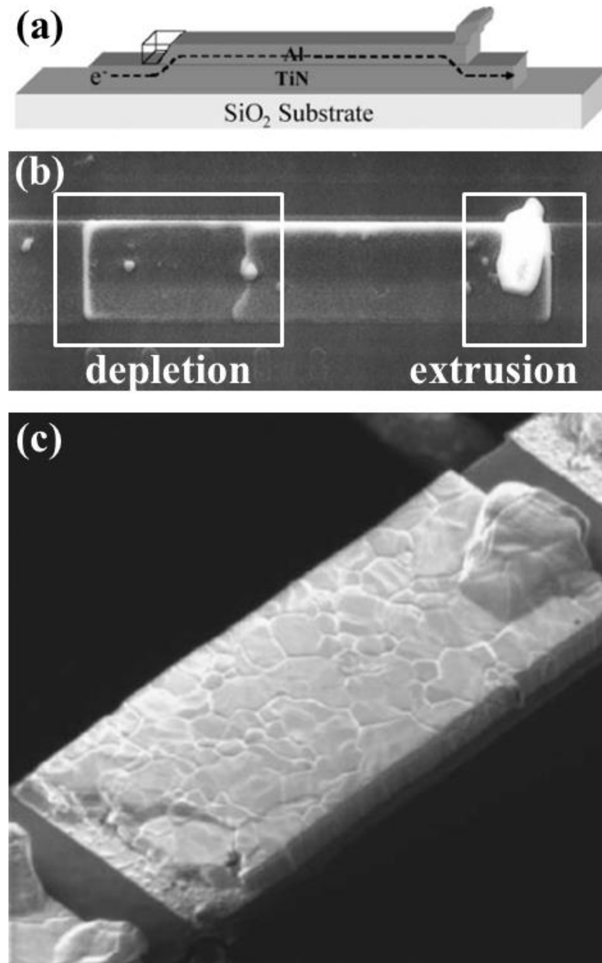


Figure 1-3 (a) Blech's structure, showing an aluminum strip deposited on a TiN layer [2]; (b) morphology of a Cu strip tested for 99 hr at 350℃ with 5×10^5 A/cm^2 current density [2]; and (c) two-dimensional conductor with grain boundaries and intersections [2].

	Melting point (K)	373K/T_m	Diffusivities at 373K (cm^2/sec)
Cu	1356	0.275	Surface $D_s = 10^{-12}$
Al	933	0.40	Grain boundary $D_{gb} = 6 \times 10^{-11}$
Pb	600	0.62	Lattice $D_l = 6 \times 10^{-13}$
Eutectic SnPb	456	0.82	Lattice $D_l = 2 \times 10^{-9}$ to 2×10^{-10}

Table 1-1 Melting temperatures, diffusivities, and diffusion mechanisms for Cu, Al, Pb, and SnPb solder [2].

1.4. Current Crowding Effect

Within a metal line, as soon as the EM-induced forms are present or as long as geometric non-uniformity exists, current density also becomes non-uniform. When voids or cracks grow, the non-uniformity of the current density over a conductor line increases. Since Joule heating is proportional to the square of current density, the local temperature will also increase rapidly. The current crowding effect therefore plays dual roles: both elevated local density and temperature accelerate the EM process. Thus, obtaining an accurate current crowding density distribution is necessary for determining the flux divergence [6].

Current crowding phenomenon is an even more serious issue in flip-chip solder joints [29]. However, current distribution and current crowding cannot be observed. The two-dimensional simulation of current crowding effect in flip-chip solder joints has been reported by Yeh *et al.*, as shown in Figure 1-4 [13, 16, 30]. It was found that the maximum current density in a solder bump can be much higher than the average one previously projected. It locates itself near the solder/UBM interface. Current crowding occurs in solder joints because the current flow experiences a dramatic geometrical and resistance transition from the thin on-chip metal line to the solder bump. Because the cross-section of the Al trace on the chip side is about two orders smaller than that of the solder joints, the majority of the current tends to gather near the Al-to-UBM entrance point to enter the solder bump instead of spreading uniformly across the opening before entering the bump. The current distribution tends to balance the effects of the shortest route and the largest effected area. The materials near the entrance point experience a current density of about one order of magnitude higher than the average value.

In previous research, Shao *et al* studied the current density distribution in a

solder joint using three-dimensional simulation [31-32]. Figure 1-5 (a) illustrates the typical three-dimensional current density distribution. From the cross-sectional view along the Al trace of the whole bump, as shown in Figure 1-5 (b), the current crowds in the solder bump near the entrance point of the Al trace. Moreover, this study obtained the current density distributions across six positions of the solder bump. The current density distribution of six layers, namely the UBM layer, IMC layer, top layer of solder, middle layer of solder, necking layer of solder are illustrated. Figure 1-5 (c) to (h) gives a clear picture of current distribution inside the solder joints. The high current region for each layer is close to the left-hand side, which is the current entrance point. In other words, the current goes from the Al trace and through the shortest path in the solder joint, leaving finally through the Cu line. Of note is that the direction of the current is opposite to that of the electron charge flow.

In addition, it is worth mentioning that current crowding effect leads to non-uniform current distribution inside a solder joint, thus resulting in non-uniformity in drift velocity. The drift velocity is proportional to the current density and non-uniform temperature distribution inside a solder joint due to the local Joule heating effect [16]. As a result, EM-induced damage occurs near the contact between the on-chip line and the bump; void is formed for the bumps with electrons migrating downward; and hillock or whisker is formed in the bumps with electrons migrating upward. Therefore, current crowding effect plays a crucial role in flip-chip solder joints under EM.

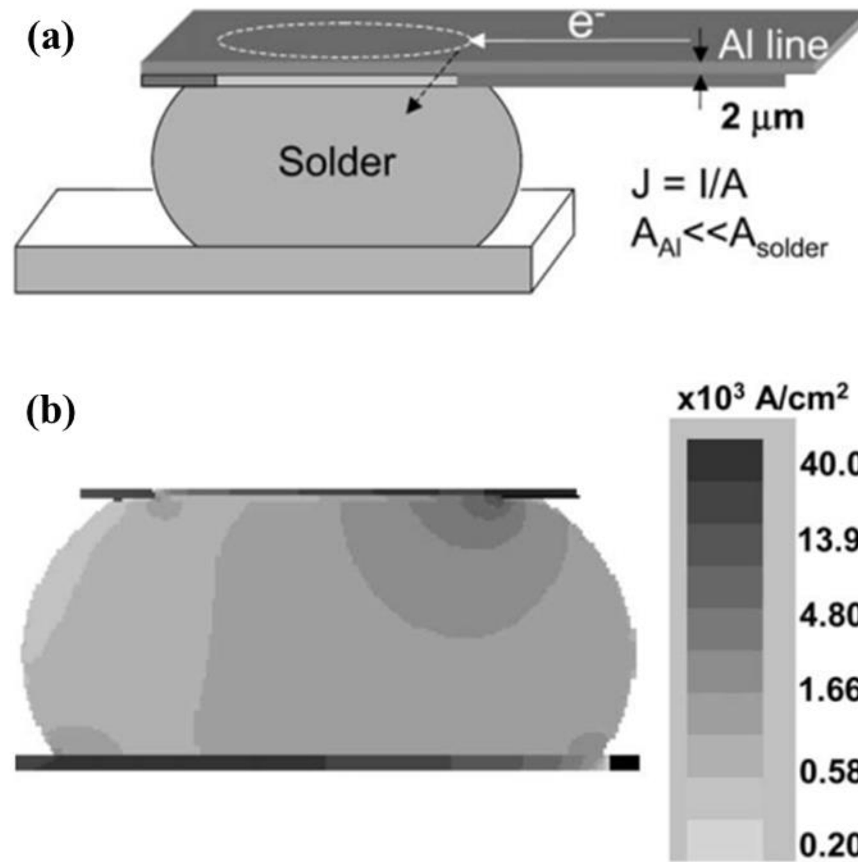


Figure 1-4 (a) Line-to-bump geometry of a flip-chip solder bump joining an interconnect line on the chip side (top) and a conduction trace on the board side (bottom) [13]; and (b) two-dimensional simulation of current distribution in a solder joint [13].

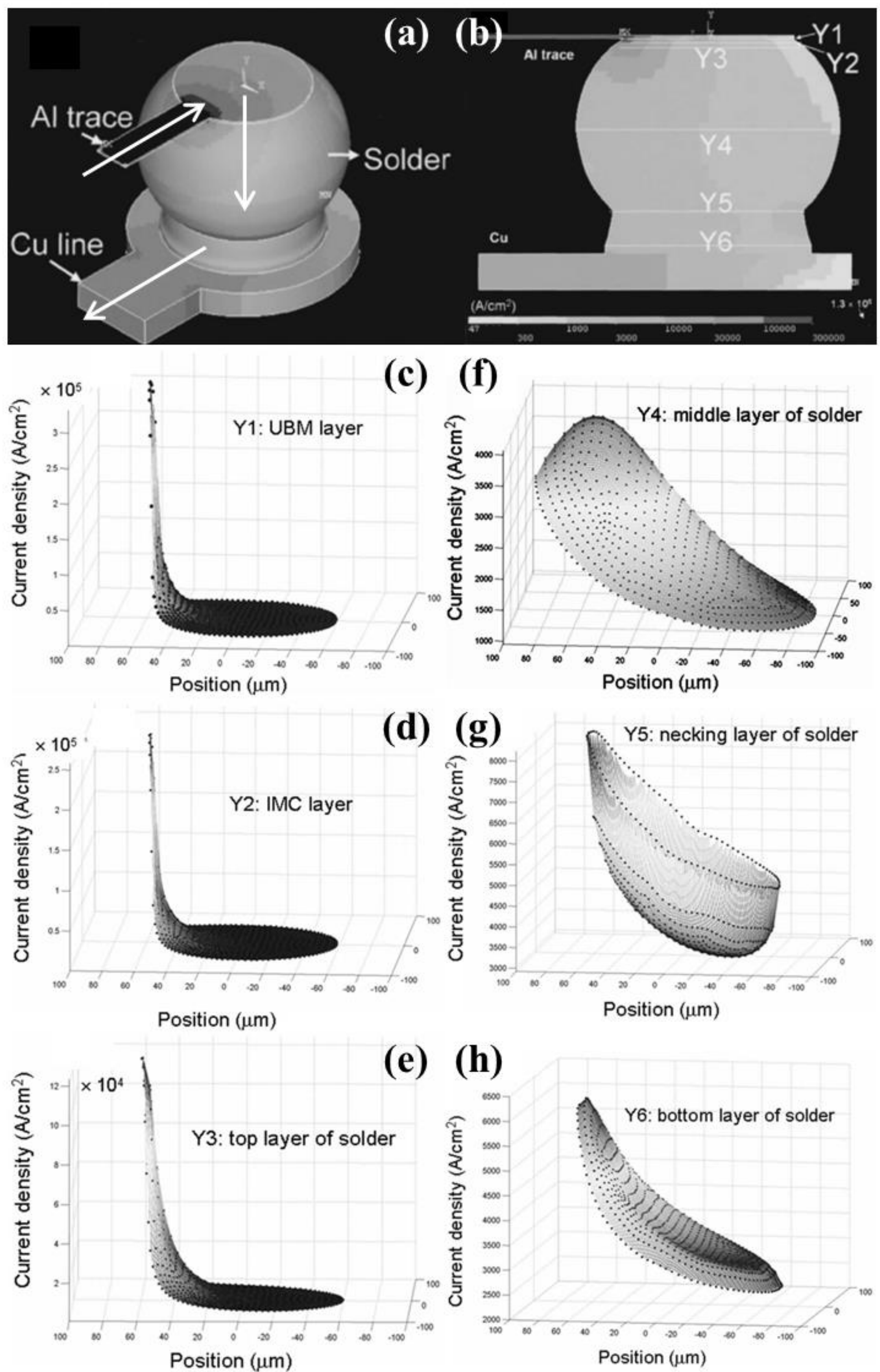


Figure 1-5 (a) Oblique current density distribution in a solder joint with Ti/CrCu/Cu thin-film UBM [31]; (b) cross-sectional current density distribution [31]; 3D current density distribution at the cross-section of (c) Y1, (d) Y2, (e) Y3, (f) Y4, (g) Y5, and (h) Y6 [31].

1.5. Failure Mechanisms of Solder Joints under Electromigration

There were two main failure mechanisms observed in previous studies: void formation and UBM dissolution. The failure mechanism during EM testing was determined by many factors including applied current density, testing temperature, designed structure, and dimensions. These two mechanisms usually occurred at the same time, with one of them dominating the failure behavior. On the one hand, void formation described the behaviors of void formation and propagation along the interface between the IMC and the solder. The void was formed at the interface because the IMC acted as a diffusion barrier, which blocks the diffusion of atoms in the UBM. The interface between the IMC and the solder therefore became a diffusion divergence for the void to nucleate. After a period of testing, the propagating void caused the joint to open and fail. On the other hand, UBM dissolution often happened when the Pb-free solder joined the high-wettability UBM, Cu for example. Owing to high wettability, the Cu dissolved quickly into the Pb-free solder. The rapid diffusion of UBM atoms caused the position of the original UBM to become the void. After the UBM dissolved completely into the solder, the short supplement of UBM atoms caused the solder joint to open. In addition, the void formed, whether at the interface between the IMC and the solder or in the UBM, caused the joint to melt at the end stage of EM testing. The melting made the failure mechanism difficult to identify. This should be prevented from happening in our testing.

In 2002, Yeh first reported the EM failure in flip-chip solder joints with eutectic SnPb [16]. In his research, the following interesting observations were made. (1) The current density inducing EM failure in the solder joints is two orders of magnitude lower than that in the Al; (2) the failure mode in the cathode end is pancake-type void

formation [33]; and (3) the redistribution of Pb-rich and Sn-rich phases was observed. Figure 1-6 (a) to (c) displays the SEM images of eutectic SnPb after EM [16]. After aging for 40 hr at 125℃ and 2.25×10^4 A/cm^2, voids were seen in the upper-left corner since electron flow entered the bump from the upper-left corner of the joint. Similar phenomena were also observed in 95.5Sn4.0Ag0.5Cu Pb-free solder joints of flip-chip solder joints when the cathode is on the chip side as shown in Figure 1-6 (d) [29]. With increase in current stressing time, pancake-type voids propagate across the top of solder joints, resulting in open failure. Since then, a lot of researches have been conducted to study void formation between the IMC and the solder [13, 34-44].

The second failure mechanism found was the rapid UBM dissolution into the solder. The mechanism was first investigated in 2003 by Nah and shown in Figure 1-7 [17]. It was observed that failure occurred in joints in a downward electron flow (from chip to substrate), while those joints having the opposite current polarity showed only minor changes. During EM, current crowding was observed inside the UBM and it enhanced the phase transformation of Cu to Cu_3Sn and to Cu_6Sn_5 at the UBM/solder interface. The Cu UBM was rapidly consumed, resulting in void formation-induced failure at the cathode side. Moreover, many studies also found this phenomenon. For example, in-situ method was employed to observe the solder joint with thick Cu UBM current stressed at room temperature by 4×10^4 A/cm^2 [45-46]. Not only was the cathode-side Cu UBM quickly dissolved, but also the thick Cu trace. Some other studies showed the same kind of failure mechanism [47-52].

Besides these two mechanisms, the microstructure evolution sometimes caused the solder joint to melt at the end stage of EM testing as shown in Figure 1-8 [53-55]. Figure 1-8 (a) to (d) diplays the results after EM testing at 150℃ by 1.6×10^4 A/cm^2 for 30 min, 60 min, 100 min, and 120 min respectively; representing the different

stages of void propagation from the right to the left along the interface between the IMC and the solder. Previous research showed that the current crowding effect was enhanced because the remaining contact area became smaller. The consequent local Joule heating effect was enhanced, thus generating a very high temperature [54-56]. Figure 1-8 (f) shows the relation between the maximum temperature of bumps and resistance change of the Al line. The solder was therefore melted as shown in Figure 1-8 (e). The melted solder led to the phase re-distribution and the rapid UBM dissolution, thus starting again the microstructure evolution. Therefore, such melting of solder should be prevented as much as possible in EM testing.

Nowadays, to meet the higher demand for device performance, the I/O count is expected to increase while the dimension of each individual joint should shrink. To date, each bump measures ≤ 100 μm of less in diameter. The design rule of packaging dictates that each bump is likely to carry a current of 0.2 to 0.4 A. Under this requirement, carry-on current density in solder bumps must be increased to exceed 1×10^4 A/cm^2, thus rendering EM a daunting reliability issue in flip-chip solder joints under such high current density. Consequently, the method for studying the microstructure evolution becomes very important [29].

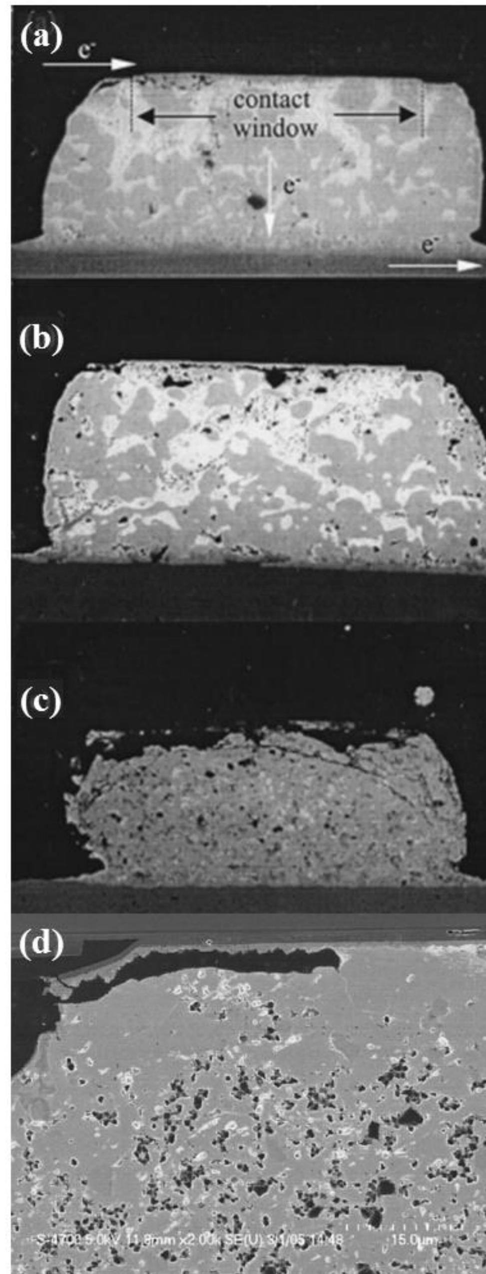


Figure 1-6 SEM images of void formation and propagation in a flip-chip E-SnPb solder bump stressed at 125℃ by 2.25×10^4 A/cm^2 for (a) 38 hr, (b) 40 hr, and (c) 43 hr [16]; and (d) SEM image of void formation in a flip-chip 95.5Sn4.0Ag0.5Cu solder bump stressed at 146℃ by 3.67×10^4 A/cm^2 [29, 33].

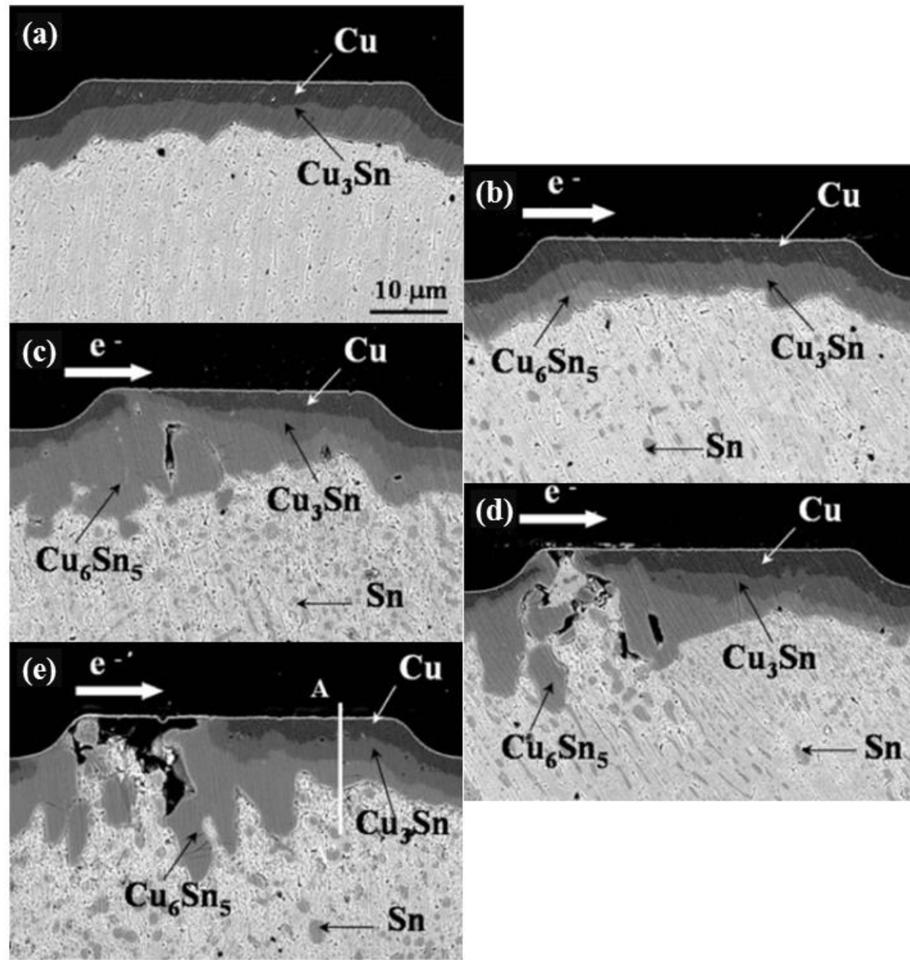


Figure 1-7 Solder joints current stressed at 140℃ by 2.55 × 10^4 A/cm^2 for (a) 0 hr, (b) 3 hr, (c) 12 hr, (d) 18 hr, and (e) 20 hr [17].

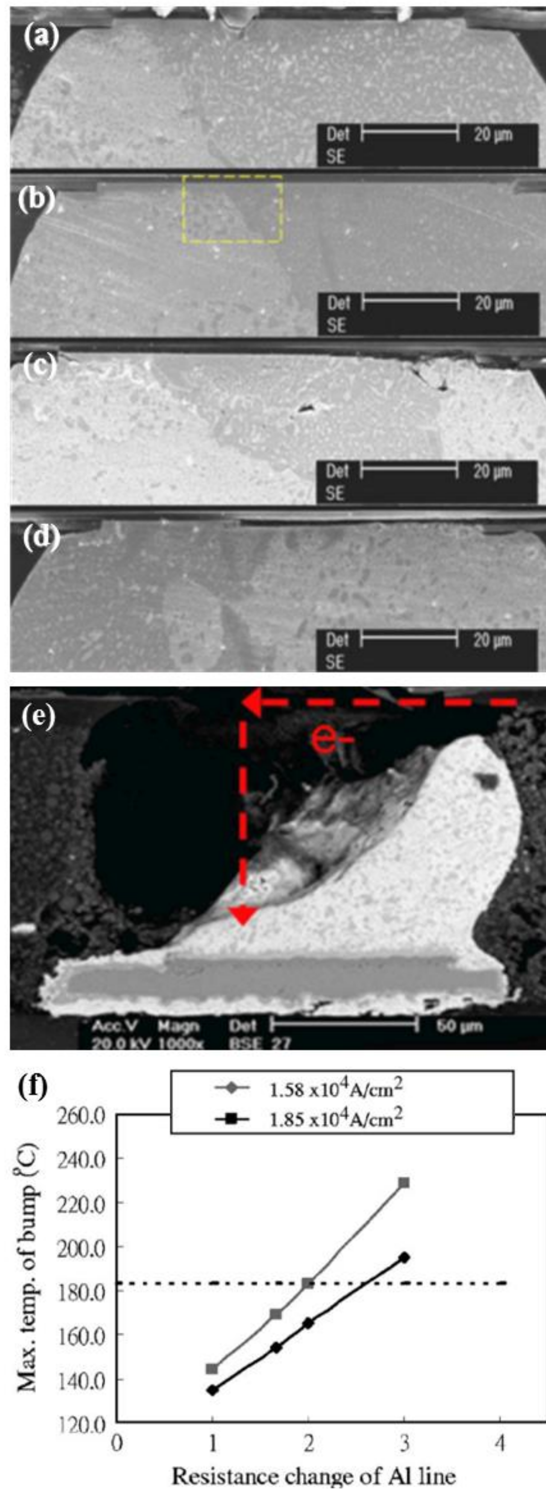


Figure 1-8 Top region of a solder bump after current stressing of 1.6×10^4 A/cm^2 at 150℃ for (a) 30 min, (b) 60 min, (c) 100 min, and (d) 120 min [53]; (e) melted solder joint due to large Joule heating before an open circuit [53]; and (f) relationship between maximum temperature of bumps and resistance change of Al line [54].

1.6. Interfacial Reaction

Solder is widely employed to connect chips to their packaging substrates in flip-chip technology as well as in ball-grid-array (BGA) technology [29]. In the last 50 years, the electronics industry has relied mainly on one type of solder (Sn-Pb solder) in product manufacture [57]. With the discovery of Pb as a hazardous material both to the environment and to human health, new developments have been made to steer away from the use of Sn-Pb solder [58-59]. In 2000, the National Electronics Manufacturing Initiative (NEMI) recommended replacing eutectic Sn-Pb solder with eutectic Sn-Ag-Cu solder in reflow processing and eutectic Sn-Cu in wave soldering [29]

A reliable solder joint can be formed by metallurgical reactions between molten solders and under-bump-metallization (UBM) on a chip or metallization on the substrate, which produces stable intermetallic compounds (IMCs) at joint interfaces [60]. During the soldering process, the formation of IMCs between solder alloys and the metallization layer is inevitable. The growth of these IMCs can strongly affect the mechanical reliability of the solder joints [61-63]. As a result, selection of appropriate UBM plays an important role in developing a reliable flip-chip joint, especially the adoption of Pb-free solders due to environmental concerns.

Copper is the most widely used UBM and substrate metallization for flip-chip and BGA applications. It is known that at the Cu/solder interface, Sn reacts rapidly with Cu to form Cu-Sn IMC, which weakens the solder joints due to its brittle nature [64]. Therefore, Ni is often used as a diffusion barrier layer to prevent the rapid interfacial reaction between solder and Cu layer in electronic devices.

In recent years, the reaction between solder and Ni has received much attention because the reaction rate is about two orders of magnitude slower than that of Cu.

Hence, the effect of IMC spalling on thin-film Ni is less serious and Ni can also serve as the diffusion barrier. The reason why the reaction rate between Ni and solder is much slower than that between Cu and solder has been an interesting kinetic question. The answer remains unclear but is likely to be caused by the much slower supply of Ni to the reaction than Cu. The supply may depend on the diffusion of Ni along the interface between Ni_3Sn_4 and Ni and also the solubility of Ni in the molten solder [65].

1.7. Kelvin Sensing

Kelvin sensing is named after William Thomson, Lord Kelvin, who invented the Kelvin bridge in 1861. It is also called four-terminal sensing, 4-wire sensing, or 4-point probe method. It is an electrical impedance measuring technique that uses separate pairs of current-carrying and voltage-sensing electrodes to make more accurate measurement than the traditional two-terminal sensing. This technique is very suitable for measuring low resistances because of two reasons: (1) diminished effect of wire resistances and contact resistances are diminished; and (2) measurement obtainable at specific positions for certain length.

Figure 1-9 (a) and (b) illustrates the 2-wire and Kelvin (4-wire) sensing method respectively. In Figure 1-9 (a), some problems arise when the resistance of some components is located at a significant distance away from the ohmmeter because an ohmmeter measures all resistances in the circuit loop, including the resistance of the wires (R_{wire}) connecting the ohmmeter to the measured component ($R_{subject}$). That is, the total resistance (R_{total}) can be expressed as:

$$R_{total} = R_{subject} + 2R_{wire} \qquad \text{Equation 1-5}$$

Usually, the wire resistance is very small (only a few ohms per hundreds of feet, depending primarily on the size of the wire), but if the connecting wires are very long,

and/or the component to be measured has a very low resistance, the measurement error due to wire resistance will be substantial.

An ingenious method of measuring subject resistance in a situation like this involves the use of both an ammeter and a voltmeter as shown in Figure 1-9 (b). It is known from Ohm's Law that resistance is equal to voltage divided by current (R = V/I). Thus, the resistance of the subject component can be determined if the current going through it and the voltage dropped across it are obtained. Current is the same at all points in the circuit, because it is a series loop. Because only the voltage drop across the subject resistance is measured, the calculated resistance is indicative of the resistance of the subject component ($R_{subject}$) alone.

However, the goal is to measure this $R_{subject}$ from a distance, so the voltmeter must be located somewhere near the ammeter, connected across the subject component by another pair of wires. At first it appears that all advantages of measuring resistance are lost this way because the voltmeter now has to measure voltage through a pair of long wires. Actually, nothing is lost at all because the wires of the voltmeter carry miniscule current. Thus, these wires of long length connecting the voltmeter across the subject component will drop insignificant amounts of voltage, resulting in a voltmeter indication that is almost the same as if it were connected directly across the subject component. Therefore, this measurement method avoids errors caused by wire resistance.

This technique is generally used in the industry to obtain the precise resistance of a specific component (via or contact) as shown in Figure 1-9 (c) and (d) [66-67]. In real cases, the Kelvin sensing structure is design as two L-shape circuits connected to one another by the turning corner. With the four wires, the resistance of the subject component (via or contact) can be obtained.

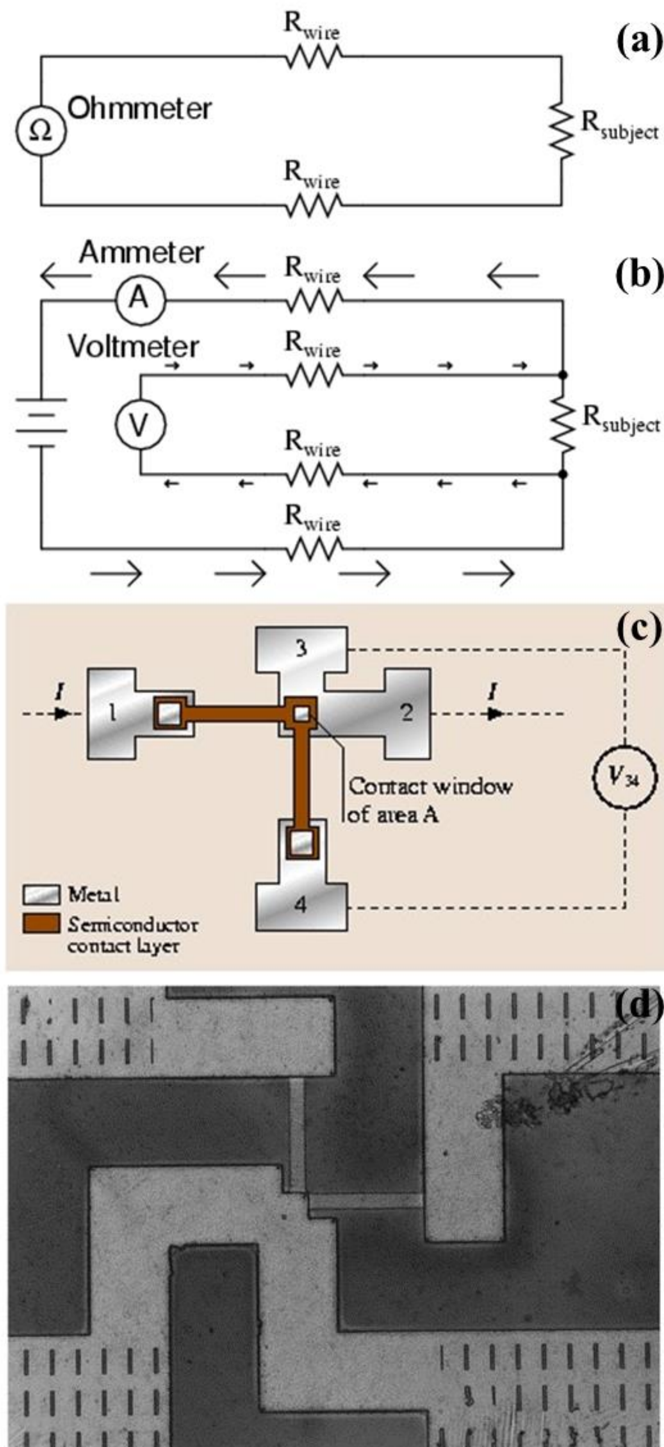


Figure 1-9 (a) Two-wire sensing; (b) Kelvin sensing (4-wire sensing); (c) schematic of Kelvin sensing structure applied in semiconductor fabrication industry [66]; and (d) Kelvin sensing structure fabricated [67].

1.8. Finite-Element Method

Modern technological advances challenge engineers to carry out increasingly complex and costly projects, which are subject to severe reliability and safety constraints [68]. These projects cover domains such as space travel, aeronautics and nuclear application, where reliability and safety are of crucial importance. Other projects are related to environmental protection, such as control of thermal, acoustic or chemical pollution, water course management, management of groundwater and weather forecasting. To obatin proper understanding, analysts need mathematical models that enable them to simulate the behavior of complex physical systems. These models are then used during the design phase of the projects. The finite-element method has become one of the most frequently used methods for solving such models.

Finite element method (FEM) is a numerical technique for finding approximate solutions to boundary value problems. It uses variational methods (the calculus of variations) to minimize an error function and produce a stable solution. Analogous to the idea that connecting many tiny straight lines can approximate a larger circle, FEM encompasses all the methods for connecting many simple element equations over many small subdomains, called finite elements, to approximate a more complex equation over a larger domain. It is difficult to quote on which FEM was invented. FEM was developed out of the need to solve complex elasticity and structural analysis problems in civil and aeronautical engineering. Nowadays, FEM requires intensive use of a computer, and can be employed to solve almost all problems encountered in practice: steady or transient problems in linear and nonlinear regions for one-, two-, and three-dimensional domains. FEM uses a simple approximation of unknown variables to transform partial differential equations into algebraic equations.

Today, ANSYS is one of the most popular and general commercial software

developed using both FEM and computer-aided engineering. ANSYS offers engineering simulation solution sets in engineering simulation that a design process requires. Companies in a wide variety of industries use ANSYS software. The tools put a virtual product through a rigorous testing procedure before it becomes a physical object [69].

1.9. Motivation

Since the current that a solder bump carries increases continuously, EM becomes one of the most important reliability issues [29]. A lot of studies have been done to examine the failure mechanisms during EM testing [13, 16, 33-52]. It is found that failure of solder bumps under EM involves two main mechanisms: void propagation and rapid UBM dissolution. Most of previous studies were conducted using two methods. One was to observe the microstructure evolution by mechanical polishing and SEM after the circuit resistance reached a certain value. The other one was to polish the solder bump before current stressing, followed by in-situ monitoring of the microstructure evolution throughout EM testing. However, these two methods have their own disadvantages.

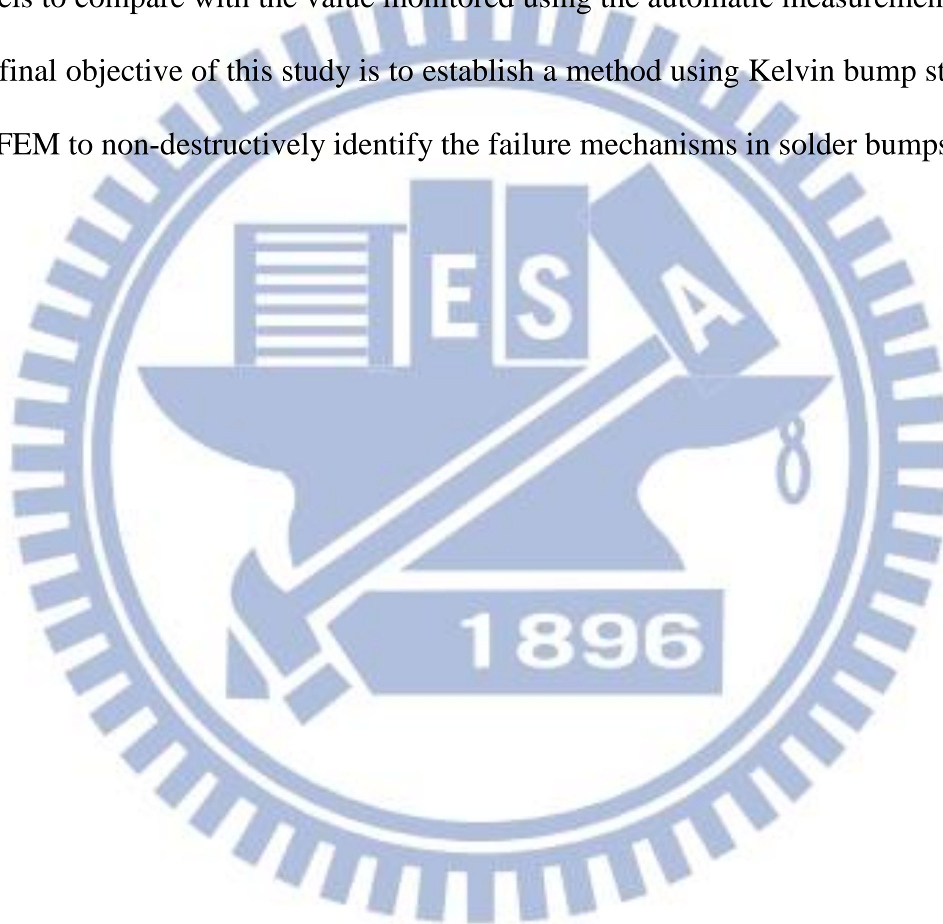
When observing the microstructure evolution by mechanical polishing and SEM, the failure time is determined by circuit resistance, but the resistance of a single solder bump is much lower than that of the entire circuit [70-71]. The bump resistance usually ranges from 1 mΩ to 10 mΩ depending on the dimensions, but the circuit resistance usually ranges around several ohms because it contains the resistance of external circuits. Once the increase in circuit resistance becomes large enough to identify, the magnitude of increase is already much larger than the bump resistance. Owing to this characteristic, the circuit resistance can only be employed to demonstrate the final stage of failure. It is not suitable for studying the detailed

procedure of failure under EM testing.

Polishing the sample before current stressing in order to in-situ observe the cross-sectional microstructure evolution caused the solder bump to come in direct contact with air, which can be viewed as the infinite vacancy source and sink. The system was transformed from a close system confined by chip, substrate, and underfill into an open system. This might seriously change the failure mechanism because the infinite vacancy source and sink, air, caused easy formation of void (at the cathode side) and the hillock (at the anode side). In addition, polishing also turned the surface of solder bump into a new heat sink because the air beside by the solder bump acted as a detour of convention. Hence, some non-destructive methods should be investigated.

In view of the above, both Kelvin sensing structure and FEM were employed to study the EM failure mechanisms in three types of solder bump. Therefore, not only were the failure mechanisms in solder bumps identified, but also was the size effect on the failure mechanism was also observed. In each type of bump, a Kelvin sensing structure was designed and combined with the bumps because the Kelvin bump structures detected only the bump resistance of the desired bumps. During EM testing, the bump resistances were continuously monitored for the same duration of time by an automatic measurement system. The automatic measurement system was self-developed using a computer, LabVIEW, high-precision programmable direct current (DC) sources, and multi-channel data acquisition instruments [72]. Multi-channel data acquisition instruments were employed to obtain the voltage drop across the specific portions. The measurement system monitored continuously the bump resistances and terminated the EM test when the bump resistances reached the specific levels such as 1.03, 1.1, 1.2, and 1.5 times that of the initial bump resistance.

Then the samples were first examined using the plan-view X-ray and then carefully polished to observe the cross-sectional microstructures. The microstructures at different stages of increase in bump resistance revealed the microstructure evolution over time. Some finite-element models were built according to the microstructures obtained to discuss the influence of current distribution on microstructure evolution, and the corresponding bump resistances were also obtained using finite-element models to compare with the value monitored using the automatic measurement system. The final objective of this study is to establish a method using Kelvin bump structures and FEM to non-destructively identify the failure mechanisms in solder bumps.



Chapter 2. Experimental

In order to study the relation between the electromigration failure mechanism and the behaviors of bump resistance obtained using Kelvin bump structures, three types of sample were fabricated: flip-chip solder bumps, 6-μm microbumps, and 10-μm microbumps. Because the fabrication process required much higher precession than that achievable in our laboratory, the samples were all made by some industrial companies on collaboration with us and then fabricated by the companies which maintained cooperation with us. Though, they were all designed under the cooperation between our laboratory members and the companies. Neverthless, all tests, measurements, and observations upon these samples were executed in our laboratory.

2.1. Flip-Chip Solder Bumps

2.1.1. Sample Structure

To reduce cost, the chip-on-substrate technology was employed to fabricate the flip-chip solder bump samples, as shown in Figure 2-1 (a). The Si chip was 6.35 mm × 4.35 mm × 0.3 mm, while that of the FR4 substrate was 26.0 mm × 26.0 mm × 1.0 mm. A total of 34 flip-chip solder bumps were made in the Si chip using lithography process, but only four of them were designed as Kelvin bump structures for measuring the bump resistance. The pitch between bumps was 800 μm. After the flip and the proper alignment between the chip and the substrate, the chip was bonded onto the substrate by 1-min reflow. After that, the underfill was heated to 75℃ to increase the fluidity, injected into the space between those solder bumps, and then fixed it by cooling it down to room temperature.

The schematic plot of a single flip-chip solder bump is shown in Figure 2-1 (b).

On the Si chip were 1.5-μm thick Al traces deposited by sputtering. The width of the Al traces was 100.0 μm, and the diameter of the Al pad was 140.0 μm. The diameter of the passivation opening and the UBM opening were 85.0 μm and 120.0 μm respectively. On the sputtered Ti/Cu seed layer (3000 Å in thickness), the 5.0-μm Cu/ 3.0-μm Ni UBM was electroplated. Because the passivation opening was confined by a 3.0-μm thick polyimide layer, the shape of the UBM looked like a cap. The eutectic SnPb (E-SnPb) solder was electroplated as well; after the electroplating, the solder was reflowed for 1 min. The reflow caused the formation of the intermetallic compound (IMC), Ni_3Sn_4, which is a chemical attachment and enhances the bonding between UBM and E-SnPb solder. Next, the entire structure was flipped upside-down and reflowed for 1 min to construct the bonding between the solder and the metallization on the substrate, which was electroplated 25.0-μm Cu/5.0-μm Ni. The IMC on the surface of substrate metallization was 1.0-μm Ni_3Sn_4, and the diameter of the substrate metallization is 280.0 μm. It was much larger than that of the UBM opening (120.0 μm) and caused the solder to spread out, thus forming a solder of very low height. The height of solder is only 25.0 μm. The 100.0-μm wide traces on the substrate and the pads were made using Cu.

The cross-sectional scanning electron microscope (SEM) image of the flip-chip solder bump is shown in Figure 2-1 (c). As can be seen, the bump was well aligned and the Pb-rich phase dispersed uniformly in the Sn matrix. Moreover, there was no void found in the solder. The fabrication process was very stable.

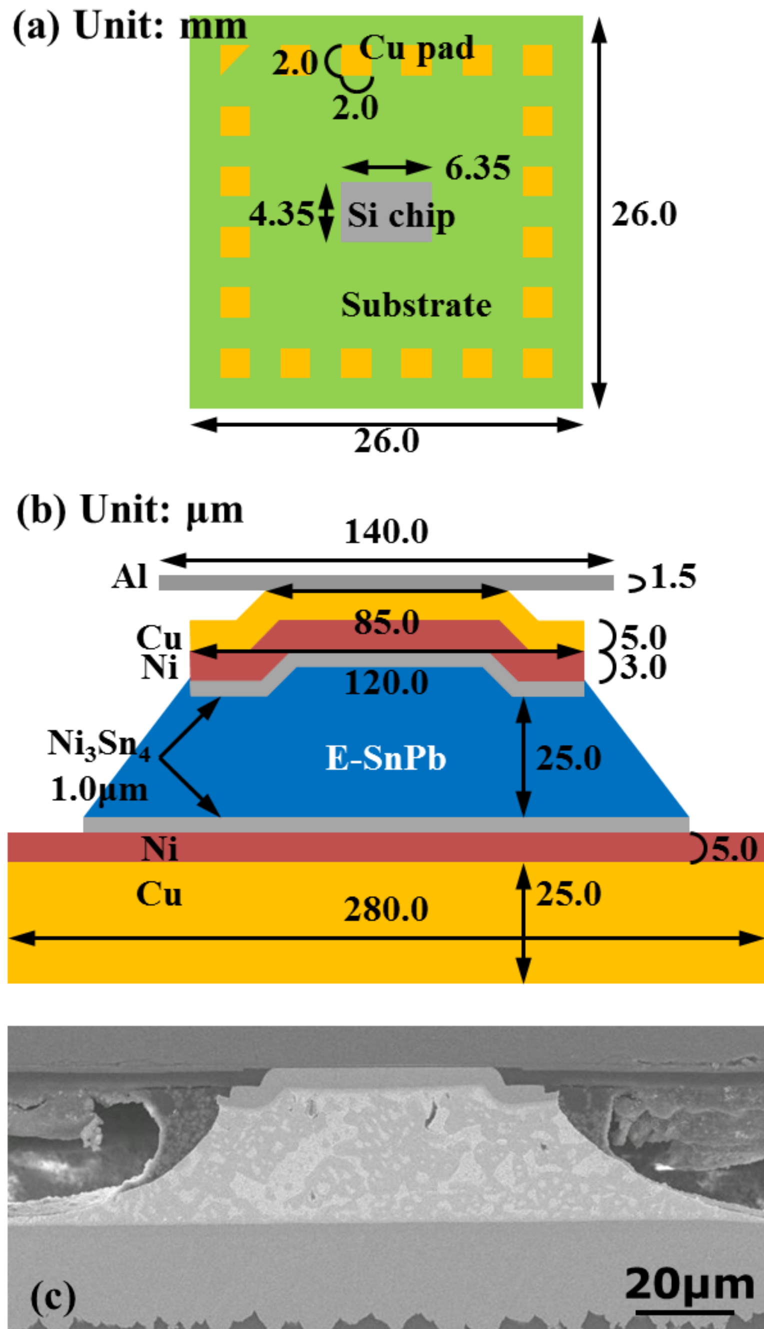


Figure 2-1 (a) Schematic illustration in plan-view of an entire flip-chip sample; (b) schematic illustration of the flip-chip solder bump; and (c) cross-sectional SEM image of a flip-chip solder bump.

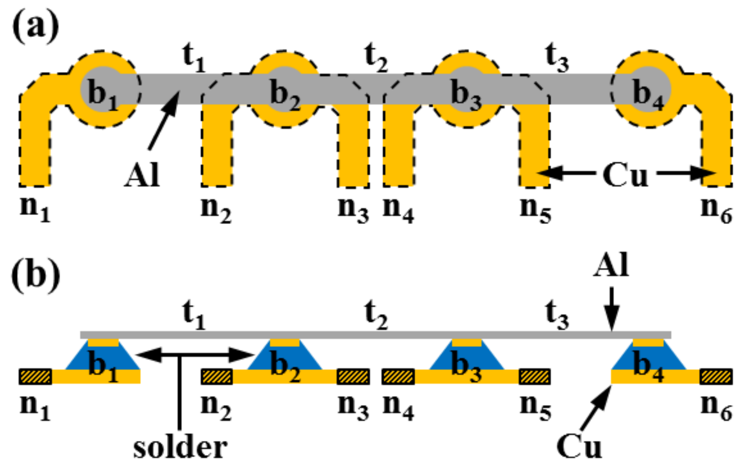
2.1.2. Kelvin Bump Structures and Experimental Procedures

In order to measure the bump resistance of a single bump, a Kelvin bump structure is necessary. As mentioned in section 2.1.1, only four of the bumps were designed as Kelvin bump structures, which are shown in Figure 2-2. Figure 2-2 (a) shows the plan view of the Kelvin bump structures while Figure 2-2 (b) shows the front-side cross-sectional view. In this figure, the gray-colored region indicat the Al traces and pads on the Si chip; the yellow-colored regions within black dashed lines indicate the Cu traces and pads on the substrate; and the four bumps between Al pads and Cu pads were marked b_1 to b_4. On the one hand, there were three Al traces, marked as t_1, t_2, and t_3, placed between the bumps to connect them. On the other hand, six Cu traces marked n_1, n_2 … to n_6 were also connected to those four bumps. With this setup of Kelvin bump structures, the resistance of b_2, b_3, and t_2 can be obtaied.

In Kelvin bump structures, if n_3 and n_4 are connected to the negative end and the positive end of a DC source respectively, the current will flow through the following paths: n_4, b_3, t_2, b_2, and n_3. The bump resistance of b2 and b3 can be obtained by measuring the voltage drop across b_2 and b_3. The bump resistance equals the value of voltage drop over the applied current. In this circumstance, the electron flows upward (from the substrate to the Si chip) in b_2 and downward (from the Si chip to the substrate) in b_3. Therefore, the bump resistance of the bumps with both upward and downward electron flow can be monitored at the same time, and so can the resistance of the entire circuit and t_2. The detailed measurement setup is shown in Table 2-1. When the current was applied from n_4 to n_3, the voltage drop across b_3 can be obtained from n_5 and n_6; the one across b_2 can be obtained from n_1 and n_2; and the one across t_2 can be obtained from n_6 and n_1. In this study, all the resistance of b_2, b_3, and t_2 were simultaneously measured during all the tests.

The tests were performed on a 150℃ hot plate. The applied current was 0.8 A, and the corresponding current density were 7.1×10^3 A/cm^2. Although the resistance of b_2, b_3, and t_2 were all monitored during the tests, only the bump resistance of b3 was analyzed in detail and discussed in this study since the flip-chip bump loaded by downward electron flow was usually the weakest spot in the entire structure. [13, 16, 31, 70, 73-74] Testing would continue until the bump resistance of b3 reached 1.03, 1.10, 1.20, 1.50, and 10.0 times that of the initial resistance value. Those samples reaching the above specific bump resistance values were marked as stages 1, 2, 3, 4, and 5, respectively. Moreover, the initial sample without current stressing was marked as stage 0 or initial stage, and the sample behaving as a fully open circuit was called the final stage.

After testing, the samples were first scanned by a two-dimensional X-ray imaging system to roughly observe the distribution of voids caused by current stressing. Next, the sample of different stages were carefully polished to the central cross-section of the tested bumps, and then observed by SEM. The composition of IMC was confirmed by energy dispersive X-ray spectrometer (EDX). Finally, the growth rate of void at different stages was also analyzed.



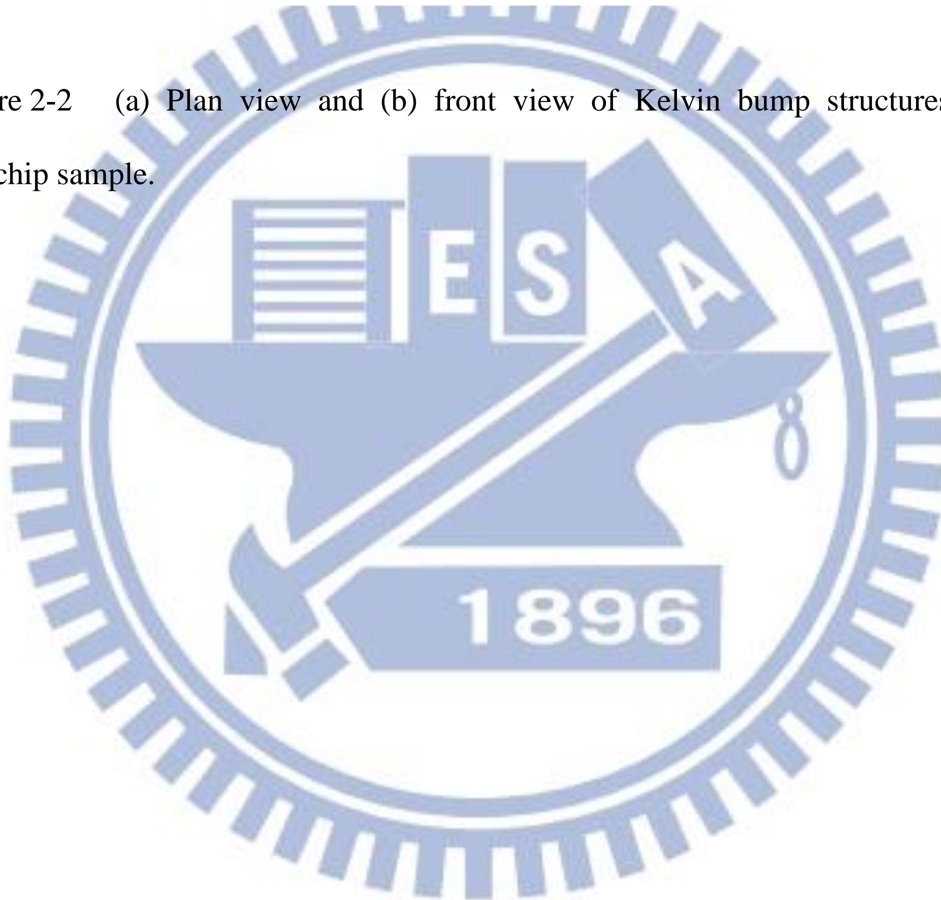


Figure 2-2 (a) Plan view and (b) front view of Kelvin bump structures in the flip-chip sample.

Voltage drop	Direction of electron flow	Measurement nodes	
		High voltage	Low voltage
ΔV_{total}	n_3-b_2-t_2-b_3-n_4	n_4	n_3
ΔV_{b2}	upward (substrate to chip)	n_1	n_2
ΔV_{b3}	downward (chip to substrate)	n_5	n_6
ΔV_{t2}	from b_2 to b_3	n_6	n_1

Table 2-1 Nodes used for measuring bump resistances of a flip-chip bump with current applied from n_4 to n_3.

Stage	**Bump resistance of b_3**
0 (or Initial)	R_i
1	$1.03 \times R_i$
2	$1.10 \times R_i$
3	$1.20 \times R_i$
4	$1.50 \times R_i$
5	$10.00 \times R_i$
Final	Open
R_i: the initial bump resistance of b_3	

Table 2-2 Bump resistance values at the different stages.

2.2. Six-Micro-Meter Microbumps

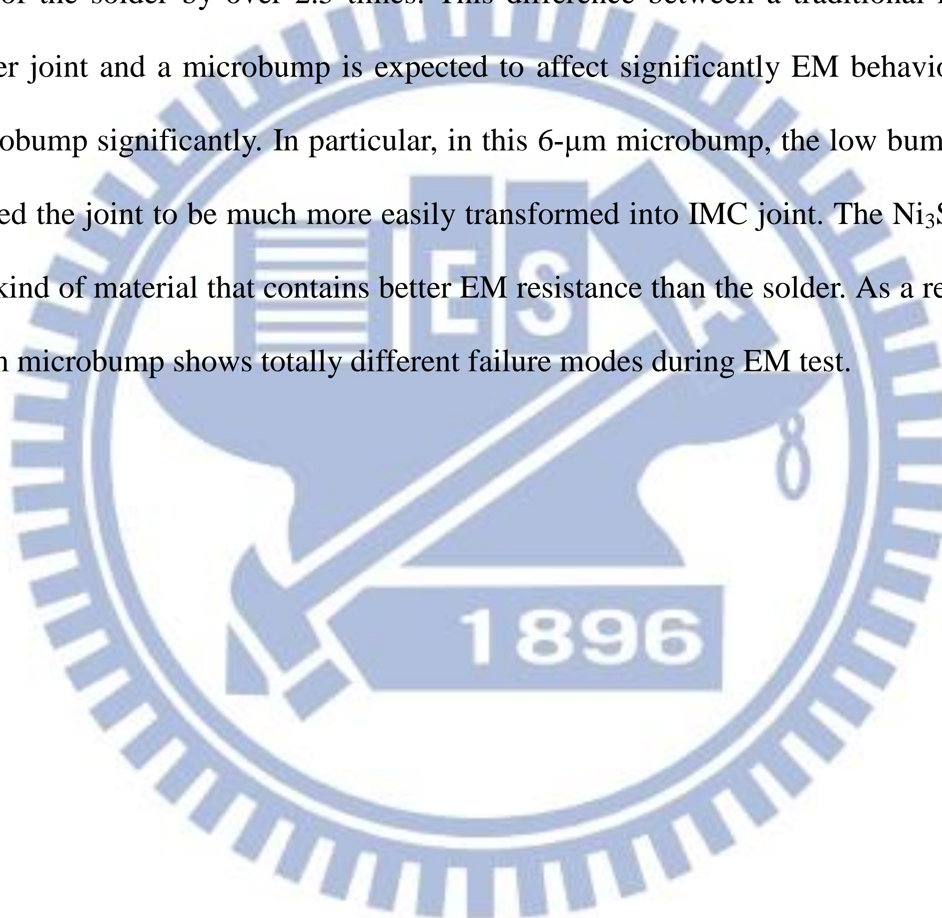
In order to study different EM failure modes using Kelvin bump structures, 6-μm microbumps and 10-μm microbumps were applied in this study. The 6-μm microbumps are introduced in section 2.2 while the 10-μm microbumps are described in section 2.3 to be introduced. The measurements of "6 μm" and "10 μm" indicate the solder height in the microbumps. In the 6-μm microbump, the height of solder ranged from 6 μm to 8 μm; in the 10μm microbump, the height of solder ranged from 10 μm to 12 μm.

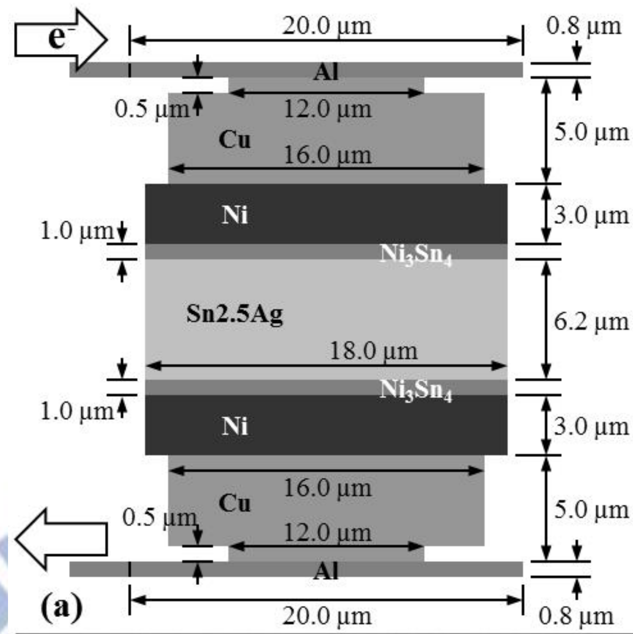
2.2.1. Sample Structure

Microbumps of Sn2.5Ag with Cu/Ni UBM were selected for EM tests. Since the size of a microbump was much smaller than that of a flip-chip bump, precise alignment during bonding was required. Therefore, the chip-on-chip (COC) technology was used. The Si of a smaller area and on top of the microbump was still called "Si chip" or "chip," while the bottom Si of a larger area was called "Si interposer" or "interposer." The thickness of both Si chip and Si interposer were 760.0 μm. The area of the Si chip is 4.5 mm×4.5 mm; that of the Si interposer is 16.0 mm×16.0 mm. The UBM comprised a 100-nm thick Ti adhesion layer, a 300-nm thick Cu seed layer, a 5.0-μm thick electroplated Cu layer and a 3.0-μm thick electroplated Ni layer on both Si chip and Si interposer sides as shown schematically in Figure 2-3 (a). The Al traces deposited by sputtering on both sides were 10 μm wide and 0.8 μm thick. The diameter of the microbump and Al pads were 18 μm and 20 μm, respectively; and the pitch was 60 μm. The diameter of Cu UBM was slightly smaller than that of Ni UBM due to the undercut during the fabrication process. On the Si chip side, Sn2.5Ag solder was electroplated on the Ni UBM, and the chip was bonded

to a Si interposer by thermo-compression at 260℃.

As shown in Figure 2-3 (b), the fabricated microbump has a solder height of 6.2μm, and the Ni_3Sn_4 IMC of about 1.0 μm thick is formed on both top and bottom interfaces between the UBM and the solder. Furthermore, some small precipitated Ag_3Sn particles can be found dispersed in the Sn2.5Ag solder. The total thickness of the UBM layers is approximately 16.0 μm; thus, the volume of the UBM is larger than that of the solder by over 2.5 times. This difference between a traditional flip chip solder joint and a microbump is expected to affect significantly EM behavior in the microbump significantly. In particular, in this 6-μm microbump, the low bump height caused the joint to be much more easily transformed into IMC joint. The Ni_3Sn_4 IMC is a kind of material that contains better EM resistance than the solder. As a result, the 6-μm microbump shows totally different failure modes during EM test.





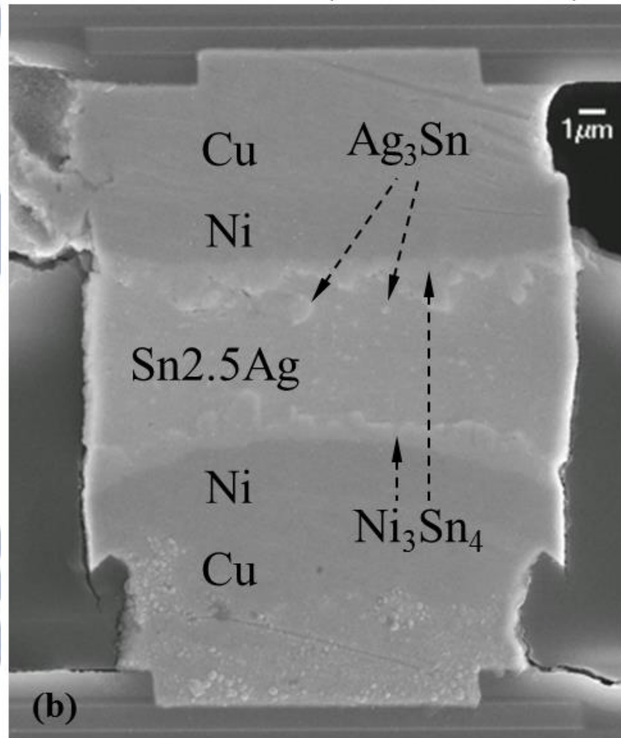


Figure 2-3 (a) Schematic illustration and (b) cross-sectional SEM image of a 6-μm microbump.

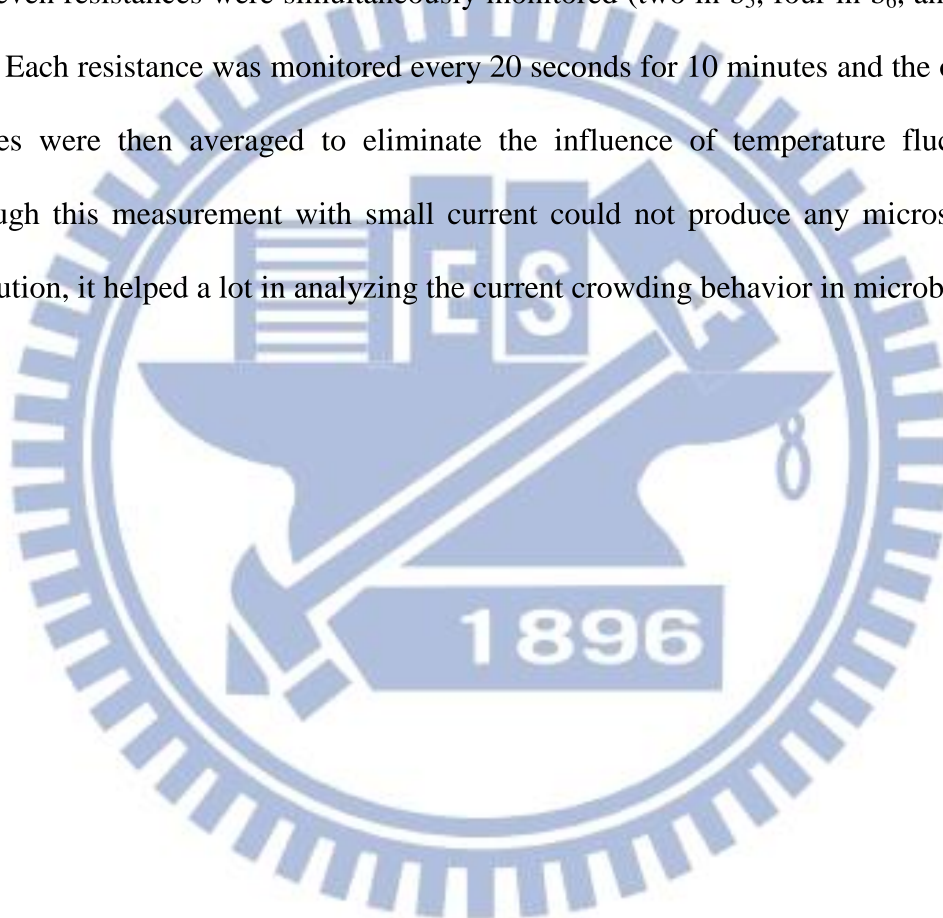
2.2.2. Kelvin Bump Structures and Experimental Procedures

Figure 2-4 is the plane view of Kelvin bump structures in the low-bump-height microbump samples. The solid lines represent the layout of Al traces on the Si chip, and the gray-colored regions represent the traces on the Si interposer. In this structure, 16 nodes were marked as n_1, n_2 … to n_{16}, and 9 microbumps were marked as b_1, b_2 ... to b_9. There were also three traces forming a direct links between b_4 and b_7 and marked as $t_{4\text{-}5}$, $t_{5\text{-}6}$, and $t_{6\text{-}7}$. With this Kelvin bump structure, the bump resistance of microbumps, b_5 and b_6, can be in-situ monitored during various kinds of reliability tests. In addition, the bump resistances at different angles of b_6 can also be obtained.

If a current was applied from n10 to n7, the electron flows through n7, b5, t5-6, b6, and finally n10. The direction of electron flow is upward (interposer to chip) in b5 and downward (chip to interposer) in b6. The methods for measuring the microbump resistances of b5 and b6 are listed in Table 2 3. The basics of measurement for the 6-μm microbump sample were quite similar to those for the flip-chip bump sample, but the bump resistance at different angles provided more information about the behavior of current crowding in the microbumps. In these samples, the 0° position is defined as the location that the trace-conducting current contacts the Al pad. The angle becomes larger with increasing distance of the edge of Al pad from the entrance of electron flow. That is, the 180° position is located at the opposite position across the Al pad.

Two different currents, 0.12 A and 0.24 A, were applied to a pair of microbumps placed on a hot plate maintained at 150℃. The corresponding current density were 4.6 × 10^4 A/cm^2 and 9.2 × 10^4 A/cm^2. The bump resistance of b_5 and b_6 at 0° and 180° were simultaneously monitored throughout the test. After the resistance reached some certain values, current stressing was terminated and the samples were polished for

microstructure analysis using a scanning electron microscope (SEM). Compositional analysis was performed by energy dispersive spectroscopy (EDS). However, before applying a high current density in the EM test, a small current, 2 mA, was employed to measure the bump resistance at all different angles. The corresponding current density is 7.86 A/cm^2, and the test with small current was also conducted on a 150℃ hot plate. The small current could prevent the occurrence of Joule heating. In this case, all seven resistances were simultaneously monitored (two in b_5, four in b_6, and one in $t_{5\text{-}6}$). Each resistance was monitored every 20 seconds for 10 minutes and the obtained values were then averaged to eliminate the influence of temperature fluctuation. Though this measurement with small current could not produce any microstructure evolution, it helped a lot in analyzing the current crowding behavior in microbumps.



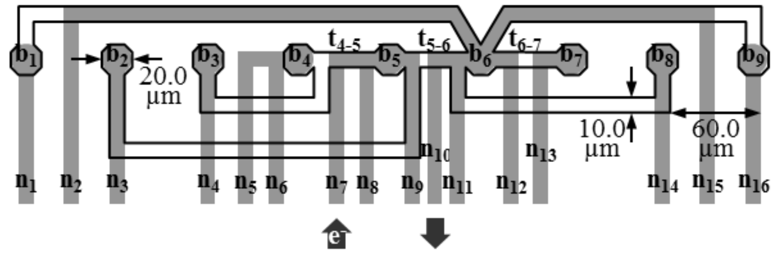


Figure 2-4 Kelvin bump structures in a 6-μm microbump.

Angle (°)	b_5 (e^- ↑) 0	b_5 (e^- ↑) 180	$t_{5\text{-}6}$	b_6 (e^- ↓) 0	b_6 (e^- ↓) 60	b_6 (e^- ↓) 120	b_6 (e^- ↓) 180
V^+ (node)	3	5	14	11	2	15	12
V^- (node)	6	9	3	14	1	16	13

Table 2-3 Nodes used for measuring resistances of a 6-μm microbump with current applied from n_{10} to n_7.

2.3. Ten-Micro-Meter Microbumps

2.3.1. Sample Structure

Figure 2-5 (a) shows the schematic structure of 10-μm microbump samples manufactured also using the COC technology. The dimensions of the Si chip and the Si interposer were 8. mm × 8. mm × 0.7 mm and 21.5 mm × 21.5 mm × 0.7mm, respectively. To prevent failure from happening in the traces, the electroplated Cu trace on both the Si chip and the interposer was thickened to 3 μm. Their width was 24 μm, same as the diameter of the Cu pads. The UBM on the chip side was made first by sputtering 1000 Å Ti/3000 Å Cu, followed by electroplating 15-μm Cu/2-μm Ni. The diameter of the UBM opening was 24 μm, and that of the passivation opening was defined as 12 μm. Ten-μm Sn2.0Ag that was electroplated on top of the chip-side UBM. After that, the Si chip was flipped and thermal-compressed onto the Si interposer. The UBM on the Si interposer was 2-μm Ni with the 1000 Å Ti/3000 Å Cu seed layer; and the diameter of the UBM opening and passivation opening were 24 μm and 10 μm, respectively. On both of the interfaces between the solder and the chip-side/bottom-side UBM, 1-μm Ni_3Sn_4 IMCs were observed. The height of the solder ranged from 10 μm to 12 μm, so this type of sample was called 10-μm microbump. Figure 2-5 (b) is the cross-sectional SEM image of a 10-μm microbump, showing well-controlled bonding. Moreover, a 6-μm-long Ag_3Sn particle can be observed on the top-right side of the solder. This was rarely found in the solder joints of a hypo-eutectic composition, which may have significant influence on the failure mode during EM tests.

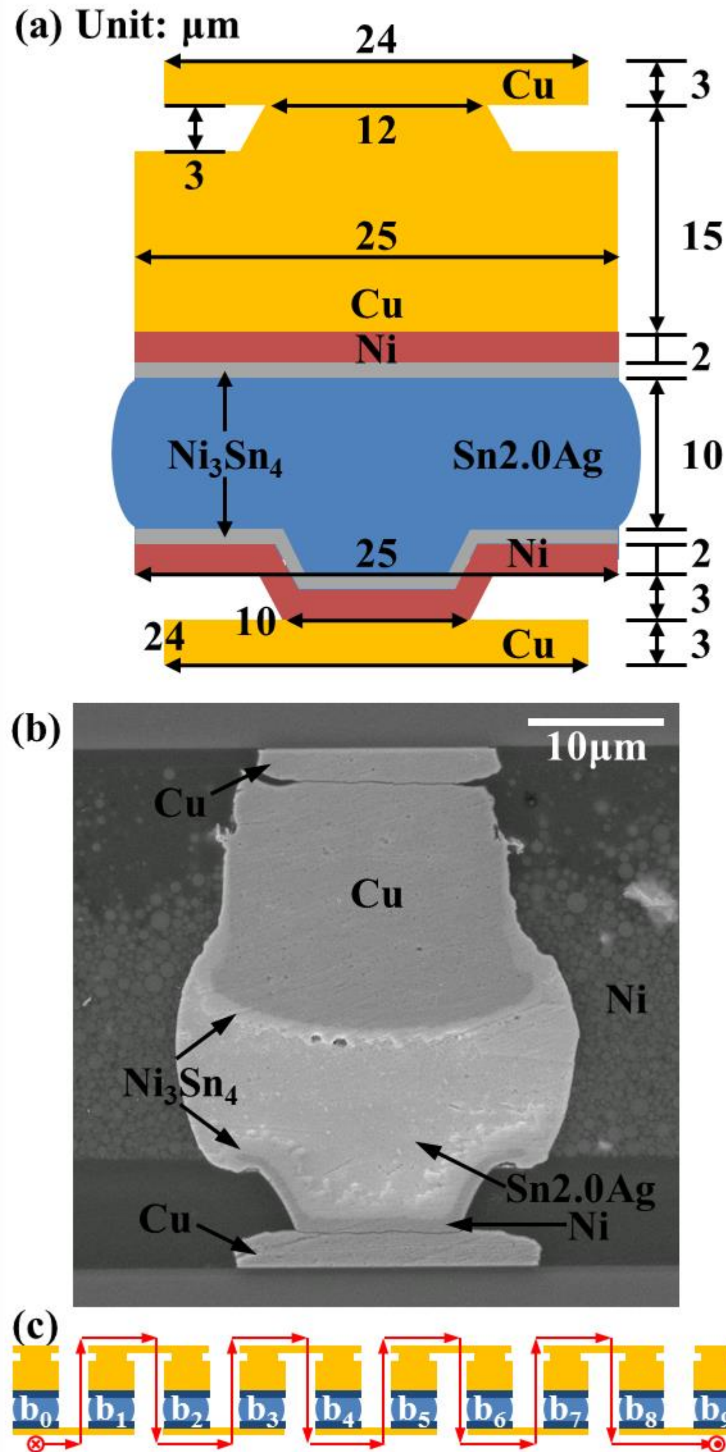


Figure 2-5 (a) Schematic plot and (b) cross-sectional SEM image of a 10-μm microbump; (c) 10-μm microbump structure tested.

2.3.2. Kelvin Bump Structures and Electromigration Stressing Conditions

The 10-μm microbump structure to be tested was schematically shown in Figure 2-5 (c). In this structure, a total of eight bumps, b_1 to b_8, were current stressed, while two dummy bumps, b_0 and b_9, were not current stressed. The current was conducted through the interposer-side pad of b_9 to that of b_0. That is, the electron flow is upward (interposer to chip) in b_1, b_3, b_5, and b_7 but downward (chip to interposer) in b_2, b_4, b_6, and b_8. The total bump resistance of the eight bumps was monitored throughout the test. The applied currents were 0.45 A, 0.36 A, and 0.27 A; while the corresponding current densities were 1×10^5 A/cm^2, 8×10^4 A/cm^2, and 6×10^4 A/cm^2. Unlike those described in previous sections, the tests of 10-μm microbumps were performed in ovens of 150℃ and 170℃

Contrary to the symmetrical structure in the 6-μm microbump, the structure of the 10-μm microbump is non-symmetrical in the vertical direction. Therefore, the polarity effect may be more obvious in 10-μm microbumps than in 6-μm microbumps. Moreover, the 2-μm Ni on the interposer side is too thin to prevent the current crowding effect from taking place in the solder. [16, 31-32], thus affecting significantly the consequent failure mode in 10-μm microbumps.

2.4. Procedures of Finite-Element Modeling

The commercial software, ANSYS, was employed to obtain the electric simulation in various bump structures. [69] ANSYS adopts the FEM for the thermal, electric, structural, and coupling analyses. For the FEM, the model needs to be meshed to form a lot of nodes and elements. According to the type of elements contained, the equations in the elements are employed to solve the analysis.

The complete procedure of a basic finite-element modeling includes three parts: preprocess, solution, and postprocess. In the first part, element types and materials properties were assigned, and the three-dimensional solid model was then constructed and meshed into an element model. Next, the loadings and the boundary conditions (BC) were added, and the model was solved. Finally, the results were generated in the postprocess. Since the pre-process is the most complicated part, it was introduced in two separate sections. Section 2.4.1 explains why the element was selected and how the material properties were determined; and section 2.4.2 describes the detailed solid modeling procedures and how it was transformed into the elemental model for simulation.

2.4.1. Element Type and Materials Properties

The element type of SOLID69 was used in these simulation models. It was suitable for the 8-node hexahedral and 6-node prism, and 4-node tetragonal thermo-electrical coupling elements, as shown in Figure 2-6. This type of element is very useful for mixed meshization process. For SOLID69, the physical calculations involved included heat generation, thermal gradient, thermal flux, electric fields, current density, Joule heating generation per unit volume, temperature, and heat flow. However, only electrical distributions such as electric fields and current density were simulated in this study. SOLID69 was chosen because it is the most convenient element type for achieving pure electrical simulation. Only the resistivity of materials has to be inputted but not temperature coefficient of resistivity (TCR), thermal conductivity (k), and feedback coefficient. Then the software will automatically define the simulation as a pure electrical problem. Consequently, only the results of voltage distribution and current density were generated after the solution.

The materials properties assigned in this study are listed in Table 2 4. The

resistivity of bulk Al is 2.7 μΩ-cm, but the value seen in Table 2 4 is 3.2 because the Al trace was deposited by sputtering. The sputtered Al was usually not as condensed as a bulk Al, so the resistivity of Al applied was slightly higher than 2.7 μΩ-cm. For Cu and Ni, the properties of the electroplated materials are usually affected by the additives during electroplating, but there were few studies describing clearly the relations between additives and resistivity. Accordingly, the resistivity of electroplated Cu (EP-Cu) and Ni (EP-Ni) were assumed to be the same as the resistivity of bulk Cu and bulk Ni. However, the electroless electroplated Ni (electroless-Ni) usually contains high composition of P atoms. The resistivity of electroless-Ni was 70 μΩ-cm, much higher than that of EP-Ni.

The solder comprised Sn, which is a kind of anisotropic materials. The resistivity along the c-axis is lower than that along the a-axis and b-axis [75-76]. However, the grain orientation of the solder could not be controlled during the reflow process, so the resistivity of E-SnPb, Sn2.0Ag, and Sn2.5Ag were set to be the same as the resistivity of the bulks. After the reflow process, the IMC, Ni3Sn4, was formed at the interfaces between the solder and Ni UBM. Apart from the electroless-Ni, Ni3Sn4 has the highest resistivity in the test structures. The resistivity of Ni3Sn4 is 4.2, 2, and 2.2 times higher than that of EP-Ni, E-SnPb, and Sn2.5Ag, respectively. The large difference between them has significant effect on microbump resistance.

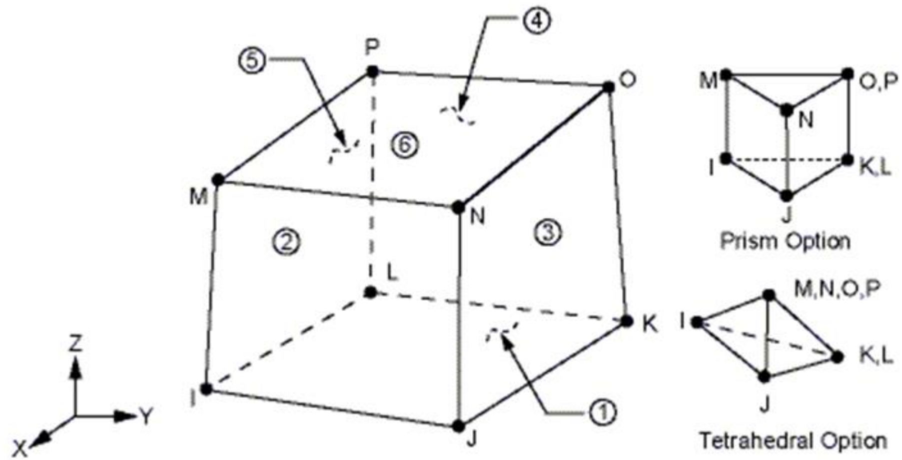


Figure 2-6 SOLID69 Geometry.

Materials	Resistivity (μΩ·cm)	Note
Al	3.2	Sputtered
Cu	1.7	Electroplated (EP)
Ni	6.8	EP
Electroless Ni	70.0	Electroless EP
E-SnPb	14.6	EP and reflowed
Sn2.0Ag	13.5	EP and reflowed
Sn2.5Ag	13.0	EP and reflowed
Ni_3Sn_4	28.5	Reflowed

Table 2-4 Materials properties used in this study.

2.4.2. Model Construction and Meshization

The two well-known standard solid construction methods in ANSYS are described in the following.

1. Bottom-up method:

The points that define the vertices of a model are called keypoints and are the "lowest-order" solid model entities. In building the solid model, keypoints are first created and then used to define the "higher-order" solid model entities, which include lines, areas, and volumes. This method is said to be model building "from bottom up." Since all the entities can be specifically defined, this method is more suitable for building a complicated model.

2. Top-down method:

The ANSYS program allows users to assemble the model using geometric primitives, which are fully defined lines, areas, and volumes. After a primitive is created, the program creates automatically all the "lower" entities associated with it. If the model construction begins with the "higher" primitive entities, the method is said to be model building "from top down." Moreover, the Booleans operations have to be performed to adjust the model details. This method is more suitable for building a simple model compared with the bottom-up method.

The bottom-up method was the main model construction approach adopted in this study because the model shapes were quite complicated. The top-down method was used only to adjust some model details. Figure 2-7 shows the model construction process, which involves the following steps:

Figure 2-7 (a): Build a half cross-section of the solder joints on the xy-plane.

Figure 2-7 (b): Rotate the areas by 90° along the y-axis to create volumes, and then divide the volumes by 45°.

Figure 2-7 (c): Mirror the volume across the y(-z)-plane.

Figure 2-7 (d): Extrude both top and bottom areas to form the traces and delete the assisting volumes.

Figure 2-7 (e): Assign the material properties onto the volumes.

Figure 2-7 (f): Mesh properly the solid model into the element model

To overcome the difficulties during model construction, both needle- and the scallop-shaped IMCs were simplified into plate-shaped. The effect of this simplification was analyzed by the "model of non-plate intermetallic compound," which will be introduced in section 2.5.3. Moreover, unlike that of Ni_3Sn_4, the resistivity of Ag_3Sn did not significantly affect the current distribution, so no Ag_3Sn was included in the models. Some of the volumes were divided into small pieces for the mapped mesh process in the meshization step. The size of elements created during meshization was well controlled to approach the appropriated convergence of solution.

2.4.3. Boundary Conditions and Solution

The steps of adding BC and solving the model are described as follows.

Figure 2-7 (f): Add an excitation load as the current on the top-left area and set the BC for the voltage to be 0 on the bottom-right area.

Figure 2-7 (g): Solve the problem by the built-in solver in ANSYS.

Figure 2-7 (h): Adjust the results.

Since the calculation of the degree-of-freedom (DOF), voltage, requires a reference point, the BC for the voltage to be 0 on the bottom-right area is necessary.

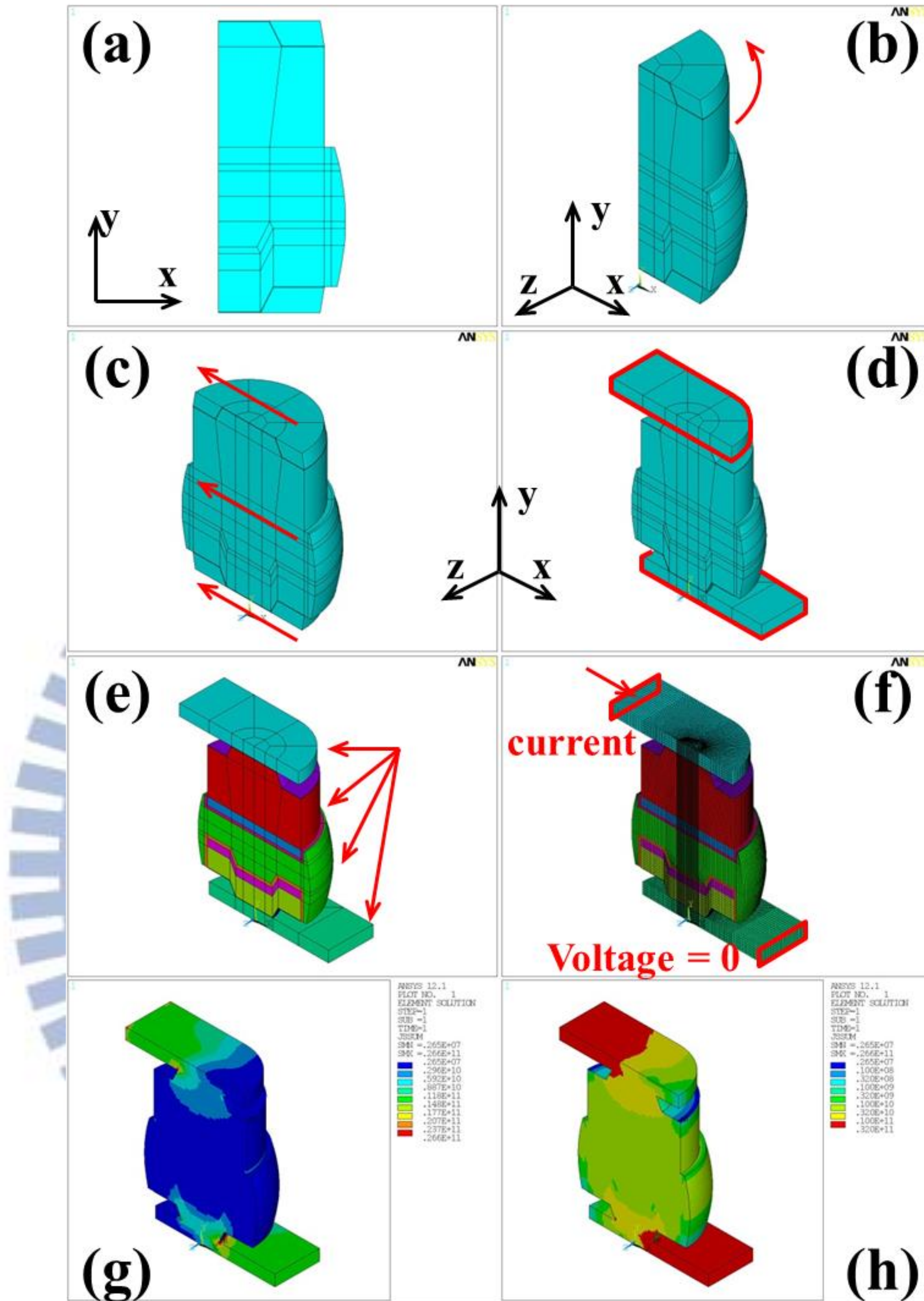


Figure 2-7 Procedures for building and solving a model.

2.4.4. Post-processing

In the final step of simulation, the postprocessor in ANSYS was employed to save the contour pictures of the current density and voltage distribution. In the solder, the position and value of maximum current density were analyzed because it usually caused early formation of void or the spot of fast IMC growth. Moreover, the crowding ratio (CR) that equals the maximum current density over the average one was also analyzed because it was the index of current crowding. On the one hand, CR = 1 means no current crowding. On the other hand, the larger the CR obtained, the more severe the current crowding was.

2.5. Models

The models corresponding to the real sample structures are introduced in this section. Besides the original models, a series of models were also built to enhance the failure mode analysis during EM tests.

2.5.1. Model of Flip-Chip bumps

The model of the flip-chip bump is shown in Figure 2-8. Since the height of the solder was only 25 μm, the solder height in the model was set as high as that of the real sample. Besides the original model, a series of models with void of different sizes were built to understand the changes in current density with void nucleation and growth due to EM. The different stages relative to the microstructure evolution during EM test are illustrated in Figure 2-9.

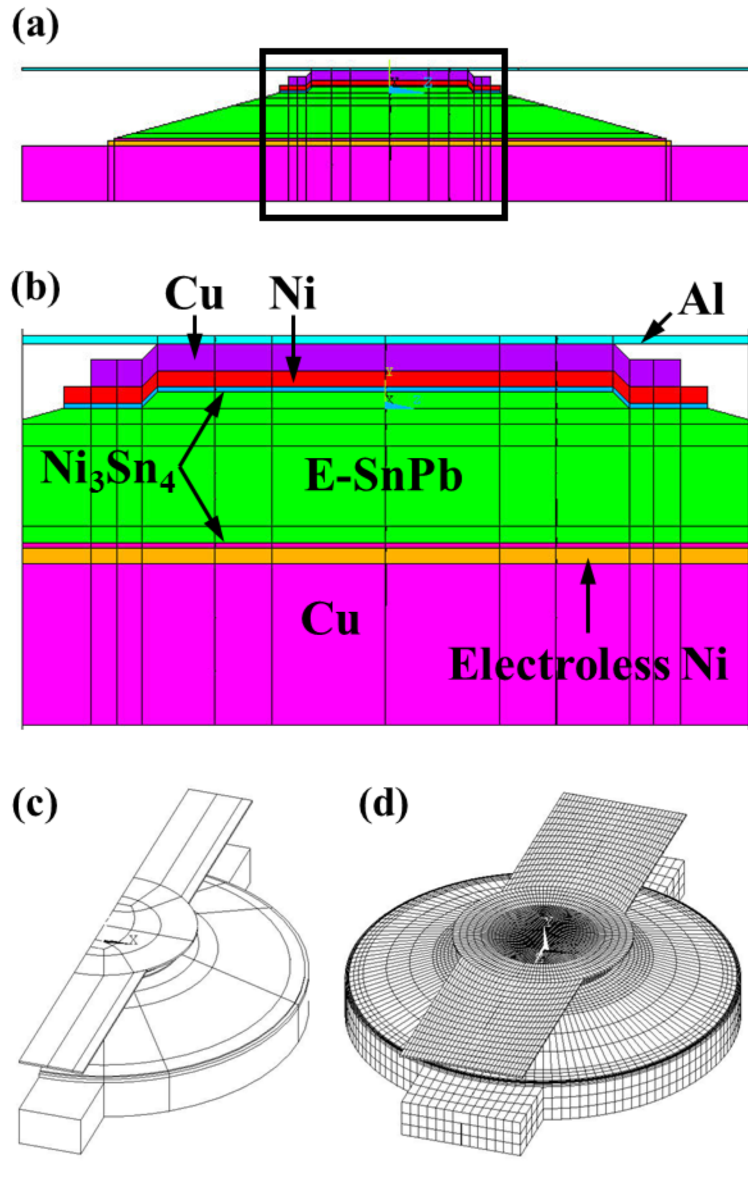


Figure 2-8 (a) Solid model cross-section of a flip-chip bump; (b) enlarged image of the black-line region in (a); (c) oblique view of the solid model; and (d) element model of a flip-chip bump.

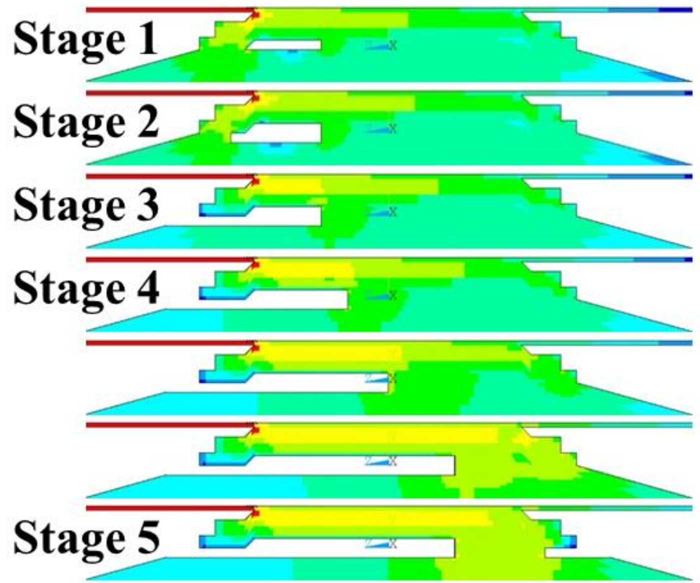


Figure 2-9 Different stages of void nucleation and propagation during EM test.

2.5.2. Model of Microbumps

The model constructed to simulate the voltage and current density distribution is shown in Figure 2-10. Figure 2-10 (a) is the cross-sectional view of the solid model, and Figure 2-10 (b) is the oblique view of the element model. In this model, the current flowed through two bumps. Since the bump structure was symmetric, the distribution in these two bumps did not show obvious difference. The bump resistances at different angles were also obtained in this model for comparison with the measurement from the Kelvin bump structures in the 6-μm microbump. A series of models with IMC of different thicknesses were built to examine the effect of IMC thickness on bump resistance. These models are shown in Figure 2-10 (c). The model on the left is the initial model with 1-μm Ni_3Sn_4 on both sides, while the one on the right was the model with over 95% of solder transformed into IMC.

Figure 2-11 shows the model of the 10-μm microbump. Figure 2-11 (a) and (b) are the cross-sectional and oblique view of the solid model, respectively; and Figure 2-11 (c) is the oblique view of element model. In this model, both the adhesive and the seed layers were also built.

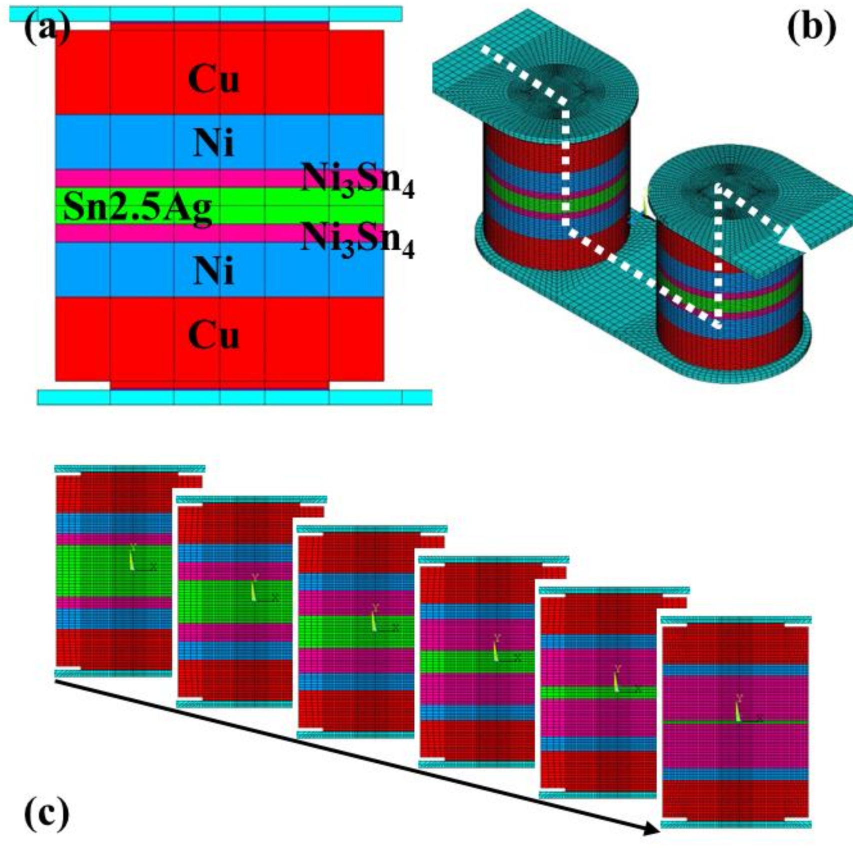


Figure 2-10 (a) Cross-section of solid model of a 6-μm microbump; (b) oblique view of element model; and (c) a series of models with IMC of different thicknesses

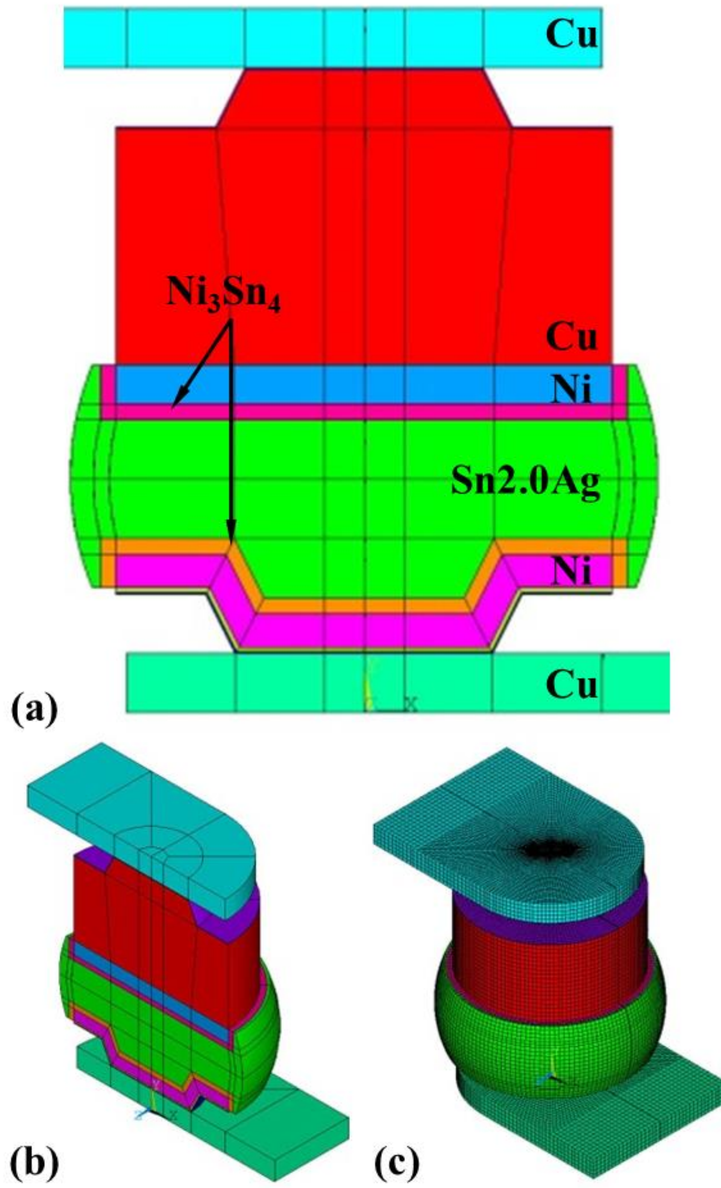


Figure 2-11 (a) Cross-sectional view of solid model, (b) oblique view of solid model, and (c) oblique view of element model of a 10-μm microbump.

2.5.3. Model of Scallop Intermetallic Compounds

A model of scallop IMCs was built to discuss the influence of simplifying the IMC into the plate shape. It was mentioned in section 2.4.2 that the IMCs between the solder and the metallization were simplified into plate shape to reduce the difficulties of model construction. Since the interfaces between the IMCs may be a divergent point of atomic flux, the shape of IMC may have significant influence. However, the shape of scallop IMCs was too complicated for direct construction in the solid model. Hence, the method of direct modification of nodes and elements in the element model had to be used. To use this method, no elements of IMC were constructed, and the elements of the solder near the UBM were first meshed. Next, because the nodes cannot be adjusted, the correlations between elements and nodes were rewritten into a correlation table. Then the elements were deleted to adjust slightly the position of nodes. Finally, the elements were reconstructed according to the correlation table and the material properties of IMCs were reassigned. Apart from these steps, the remaining simulation steps followed those described in section 2.4. The results of this model (with scallop IMC at the interfaces) were compared with the models with plate IMC. The cross-sectional view of this model is shown in Figure 2-12.

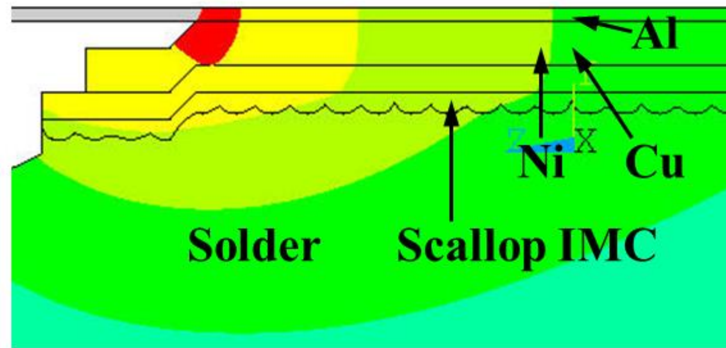
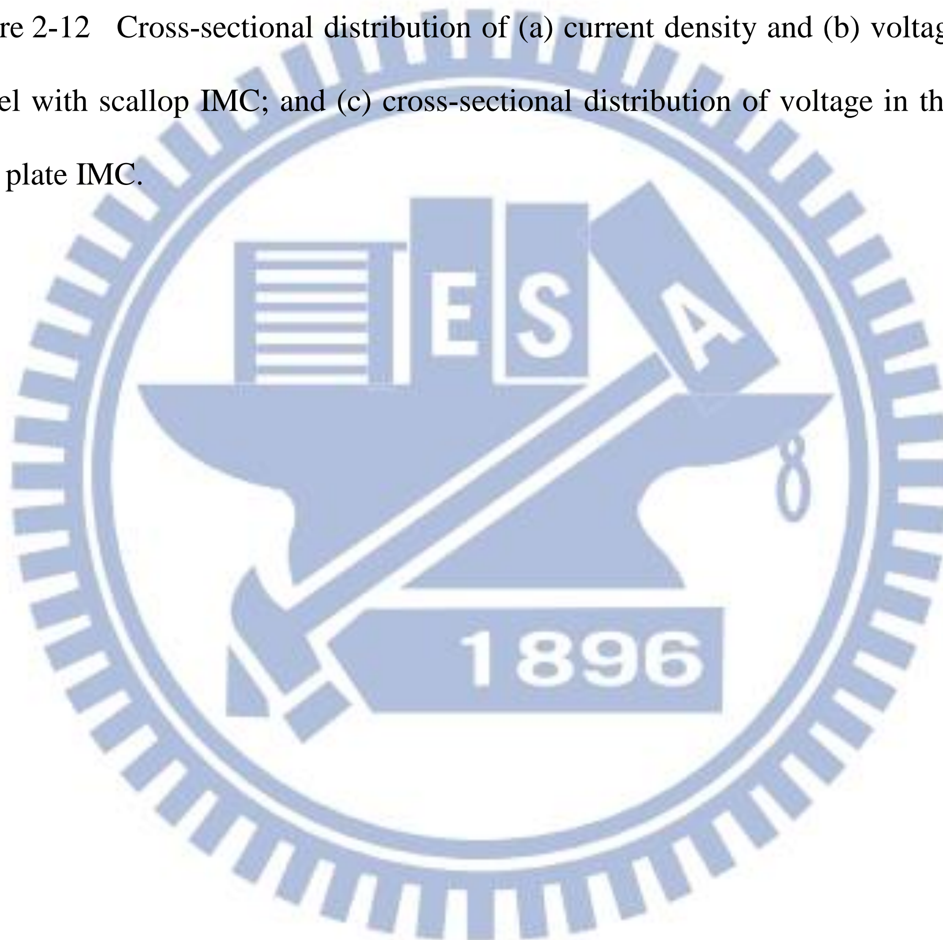


Figure 2-12 Cross-sectional distribution of (a) current density and (b) voltage in the model with scallop IMC; and (c) cross-sectional distribution of voltage in the model with plate IMC.



2.6. Numerical Modeling of Current Crowding Effect

In order to explain the relationship between current distribution in the microbump and microbump resistance, a simplified numerical model was created in this study. In this numerical model, the microbump solder joint was viewed as a resistance network, and the joint was divided into n parts vertically. The current on the left-hand side is larger than that on the right-hand side because of shorter conducting path. Since the current enters from the top-left-hand corner and exits through the bottom-left-hand corner, the model can also be employed to describe the current crowding phenomenon in microbumps.

The parameters are marked in Figure 2-13 (a), and the corresponding resistance network is shown in Figure 2-13 (b). To simplify the calculation process, both UBM and IMC were eliminated and the structure was treated as a rectangular solid. The height of Al trace and solder joint are denoted as H_1 and H_2, respectively. The thickness and the width of the microbump are marked as D and T, respectively. The resistivity of Al trace and solder joint are assigned as ρ_1 and ρ_2, respectively. The two-dimensional resistance network is assumed to comprise horizontal and vertical resistances, R_x and R_y, as a parallel circuit. Therefore, the microbump resistance can be obtained by calculating the effective resistance of the entire resistance network. The k-th effective resistance could be viewed as the parallel connection of the k-th R_y and the (k-1)-th effective resistance and the series of the effective resistance can be written as follows:

$$R_1 = R_y$$

$$\frac{1}{R_2} = \frac{1}{R_y} + \frac{1}{2R_x + R_1}$$

$$\vdots$$

$$\frac{1}{R_{n-1}} = \frac{1}{R_y} + \frac{1}{2R_x + R_{n-2}}$$

$$\frac{1}{R_n} = \frac{1}{R_y} + \frac{1}{2R_x + R_{n-1}} \qquad \text{Equation 2-1}$$

As a result, the relationship between R_n and R_{n-1} could be written in the following form.

$$R_n = \frac{R_y(2R_x + R_{n-1})}{R_y + 2R_x + R_{n-1}} \qquad \text{Equation 2-2}$$

R_n was assumed to be convergent, that is

$$\lim_{n\to\infty} R_{n-1} = \lim_{n\to\infty} R_n \qquad \text{Equation 2-3}$$

With Equation 2-3, Equation 2-2 is transformed into

$$0 = \lim_{n\to\infty} {R_n}^2 + 2R_x \lim_{n\to\infty} R_n - 2R_xR_y \qquad \text{Equation 2-4}$$

Equation 2-4 is solved as

$$\lim_{n\to\infty} R_n = R_x + \sqrt{{R_x}^2 + 2R_xR_y} \qquad \text{Equation 2-5}$$

R_x and R_y are the resistances of a little segment of $\overline{R_x}$ and $\overline{R_y}$, respectively. $\overline{R_x}$ is the total horizontal resistance and $\overline{R_y}$ is the total vertical resistance of the solder joint. The relationship therefore becomes

$$R_x = \frac{\overline{R_x}}{n}, R_y = n\overline{R_y} \qquad \text{Equation 2-6}$$

Consequently, Equation 2-5 can be written as

$$\lim_{n\to\infty} R_n = \frac{\overline{R_x}}{n} + \sqrt{\left(\frac{\overline{R_x}}{n}\right)^2 + 2\frac{\overline{R_x}}{n} \cdot n\overline{R_y}}$$

$$\lim_{n\to\infty} R_n = \sqrt{2\overline{R_x} \cdot \overline{R_y}} \qquad \text{Equation 2-7}$$

Finally, CR can be obtained. As mentioned in section 2.4.4, CR is defined as the maximum current density divided by the average value for a specific horizontal layer of solder. It is a very important parameter in EM of solder joint and represents the non-uniformity of current density. A higher CR indicates a higher non-uniform

distribution of current density. Therefore, with $n \lim_{n\to\infty} R_n \times I_{total} = R_y \times I_{max}$ coming from the equal-potential law, the CR can be simplified to

$$\mathrm{C.R.} = \frac{J_{max}}{J_{avg}} = \frac{I_{max}/\frac{DT}{n}}{I_{total}/DT} = \frac{nI_{max}}{I_{total}}$$

$$= \frac{n \lim_{n\to\infty} R_n}{R_y} = \frac{n \lim_{n\to\infty} R_n}{n\overline{R_y}} = \sqrt{2\overline{R_x}/\overline{R_y}} \qquad \text{Equation 2-8}$$

To verify the result, some critical conditions should be taken into consideration, and Equation 2-1 should be sensitive to the following conditions. First, for the condition of $R_x \to 0$ or $R_y \to \infty$, Equation 2-1 becomes invalid. However, these two conditions indicate that current can easily flow horizontally through the Al trace and the pad, but to flow vertically through the solder is difficult. Therefore, the current tends to distribute uniformly in the Al trace and the pad before flowing into the solder. As a result, the total effective resistance, $\lim_{n\to\infty} R_n$, approaches $\overline{R_y}$ while R_x becomes smaller or R_y becomes larger. Next, the condition of $R_x \to \infty$ or $R_y \to 0$ means that current crowding is severe because the high trace resistance, $\overline{R_x}$, will force the current to quickly flow downward through the solder. As a result, the total effective resistance, $\lim_{n\to\infty} R_n$, reaches $\overline{R_y}$. Furthermore, although the contributions from the UBM and the IMC were eliminated in the assumption, they can still be recovered by treating UBM and IMC as rectangular solids to modify $\overline{R_y}$.

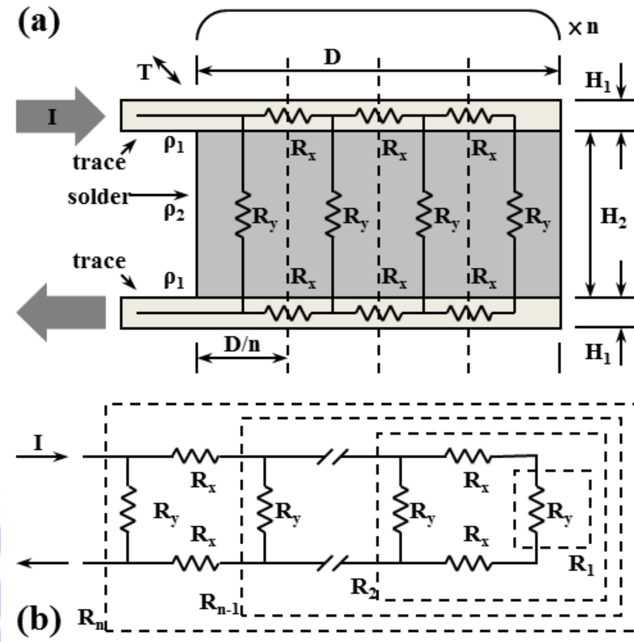


Figure 2-13 (a) Schematic plot of numerical model for calculating the resistance of a microbump; and (b) the corresponding resistance network diagram.

Chapter 3. Results

In this Chapter, the results of flip-chip bumps, 6-μm microbumps, and 10-μm microbumps are reported respectively in sections 3.1, 3.1.3, and 0. In each section, the bump resistance curves and the corresponding microstructure evolutions are presented. Furthermore, secondary information such as void growth rate and bump resistance at different angles were also investigated. In section 0, the results of finite-element analysis with the different structures were examined. The distribution of current density demonstrates clearly how current density distribution, which could not be observed, affected the failure mechanisms during EM tests.

3.1. Electromigration Test Results of Flip-Chip Bumps

3.1.1. Bump Resistance of Flip-Chip Bumps

A typical bump resistance of the flip-chip bump behaved as a concave-up curve, as shown in Figure 3-1. Figure 3-1 (b) shows the enlarged plot of the dashed square region in Figure 3-1 (a). The horizontal axis is the time normalized to the total test duration, which is 756.6 hr. The initial bump resistance of the flip-chip bump was 0.45 mΩ, and all the bump resistances obtained were normalized according to the initial value. The left vertical axis in Figure 3-1 denotes the original bump resistance value, and the right vertical axis, the normalized value. In the following discussion, the normalized bump resistance was used more often because the initial bump resistance was not the same every time. Therefore, the normalized bump resistance indicating the change brought by the microstructure evolution was more useful than the original value.

In Figure 3-1, the initial bump resistance was 0.45 mΩ, and the EM testing lasted

756.6 hr until the circuit opened. The rate of increase in bump resistance could be divided into three stages. In the first stage, the normalized bump resistance took around 0.05 (5%) of the normalized time to reach 1.03, which corresponded to the first stage of failure introduced in section 3.1.2. After that, the bump resistance increased slowly and gradually to 2.5 of the normalized bump resistance until the normalized time reached 0.5. Then the rate of increase rose significantly in the second stage. From 0.5 to 0.8 of the normalized time, the normalized bump resistance increased from 2.5 to 11.5. The magnitude of increase in bump resistance was more than 9 times the initial value in 30% of total stressing period. Compared with the rate of increase before 0.5 of the normalized time, the rate of increase in bump resistance was around 10 times ($\frac{(11.5-2.5)/(0.8-0.5)}{(2.5-1.0)/(0.5-0)}$) higher. Finally, in the third stage, the bump resistance grew even faster than that in the second stage, and became very unstable. The corresponding microstructure is also shown in the next section. After the bump resistance increased rapidly to exceed 100 mΩ, the tested flip-chip failed, and the circuit opened. The tests were stopped and different stages were marked according to the increase in bump resistance. The specific increases and the corresponding stages of failure have been defined in section 2.1.2.

Figure 3-1 (c) shows the bump resistance obtained from a daisy chain, which was generally employed to study the EM. The difference between Figure 3-1 (b) and Figure 3-1 (c) tells that the widely used daisy-chain structure was not precise enough to detect the change in bump resistance caused by microstructure evolution. The resistance obtained by the daisy chain did not change although the resistance from the Kelvin bump structures already showed obvious increases. Therefore, the Kelvin bump structures are more suitable for in-situ monitoring of microstructure evolution.

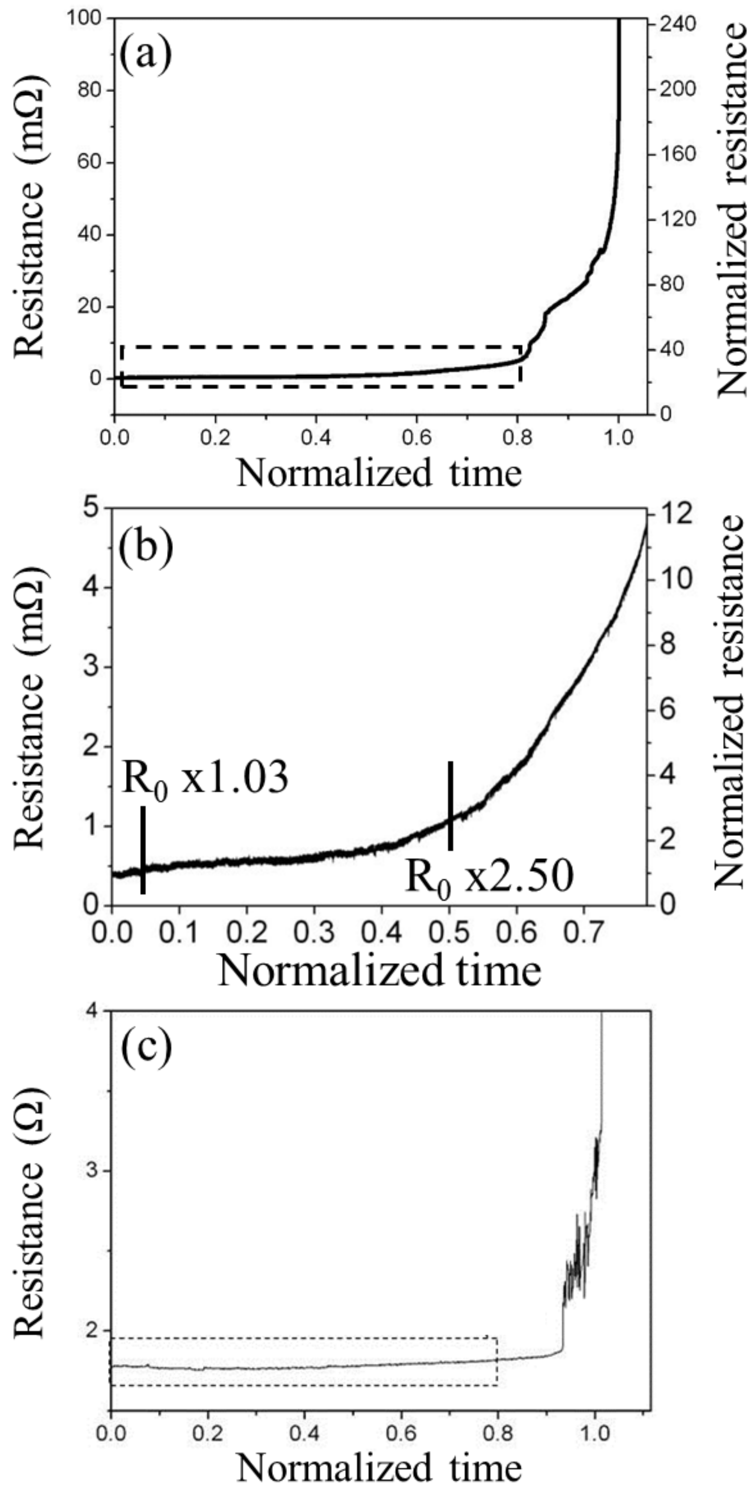


Figure 3-1 (a) Bump resistance curve of a flip-chip bump during EM test; (b) enlarged bump resistance curve of the dashed square in (a); and (c) resistance of entire circuit in the flip-chip sample.

3.1.2. Microstructure Evolution in Flip-Chip Bumps

With the pre-designed Kelvin bump structures, the different stages of failure in flip-chip bumps during EM tests can be well clarified. Figure 3-2 shows the cross-sectional interface between the E-SnPb and the IMC (and UBM) in the solder bump stressed by the downward (chip-side to substrate-side) electron flow. Accordingly, the main failure mechanism in the flip-chip solder bumps involved void nucleation and propagation at the interface between IMC and solder.

The series of cross-sectional SEM images demonstrate clearly the entire progress of failure caused by EM testing. Figure 3-2 (a) represents stage 0, which is also the initial stage without current stressing. There was no void found in this stage. After current stressing for 29.8 hr, the failure reached stage 1. The bump resistance increased by only 3%, and void nucleation at the interface between the IMC and the solder could be observed. The void nucleation site was located near the entrance point of the electron flow, which was also the spot of current crowding and the maximum atomic flux divergence. Since the void (air) was non-conducting, it acted as a block, thus forcing the current (electron flow) to reroute along the edge of the void, which became the new spots of void formation. The void therefore grew and propagated along the interface of the IMC and the solder, as shown in Figure 3-2 (c) and (d). The bump resistance reached 1.1 (stage 2 in Figure 3-2 (c)) and 1.2 (stage 3 in Figure 3-2 (d)) of the normalized value after current stressing for 101.5 hr and 140 hr, respectively.

However, the void did not continue growing after reaching the center of the interface (stage 3). Secondary void formation occurred at the spot far away from the initial current crowding region, as shown in Figure 3-2 (e) and (f). The two voids grew after the split, occupied completely the area of the cross-section, and caused

joint failure. It took 155.3 hr and 383 hr for the joint to reach stage 4 and stage 5, respectively. In these two stages, the remaining contact area between the IMC and the solder was small. That is, the current crowded in the small area, and the corresponding current density was actually very large. In this situation, the failure time would be shortened since the EM flux is proportional to the current density (see section 1.3). However, the testing lasted more than 300 hr before failure according to the microstructure evolution and 0.25 of normalized failure time according to the bump resistance curves in Figure 3-1 (a) and (b). This phenomenon may be attributed to phase coarsening. Obvious phase coarsening was observed in stages 4 and 5. Both Sn-rich and Pb-rich grains became very large. In the Pb-rich phase (Figure 3-3), the composition of Pb is about 90wt%, which is very close to the composition in the high-Pb solder (95wt%). The melting temperature of Pb, 327℃, is much higher than that of Sn, 232℃; and the low-Sn phase retards the reaction between UBM and solder. Once the Pb-rich got coarsened near the remaining area, the high-EM-resistance Ph-rich phase enhanced the EM resistance, thus lengthening the EM failure time.

The detailed test duration at different stages are listed in Table 3-1, and the plan-view X-ray images of different stages shown in Figure 3-4 illustrate void nucleation and propagation. Since the high-atomic-weight atoms block and absorb more X-ray, the dark region denotes the remaining E-SnPb solder, and the bright region surrounded by the dark region denotes the void. The white dashed lines indicate the Al trace, passivation opening, and the UBM opening. The X-ray image of different stages demonstrated void nucleation on the left side near the spot of current crowding, which then propagated toward the right side. The circular void surrounded the remaining solder; creating an image of the void like splitting into two parts, as seen in the cross-sectional SEM image.

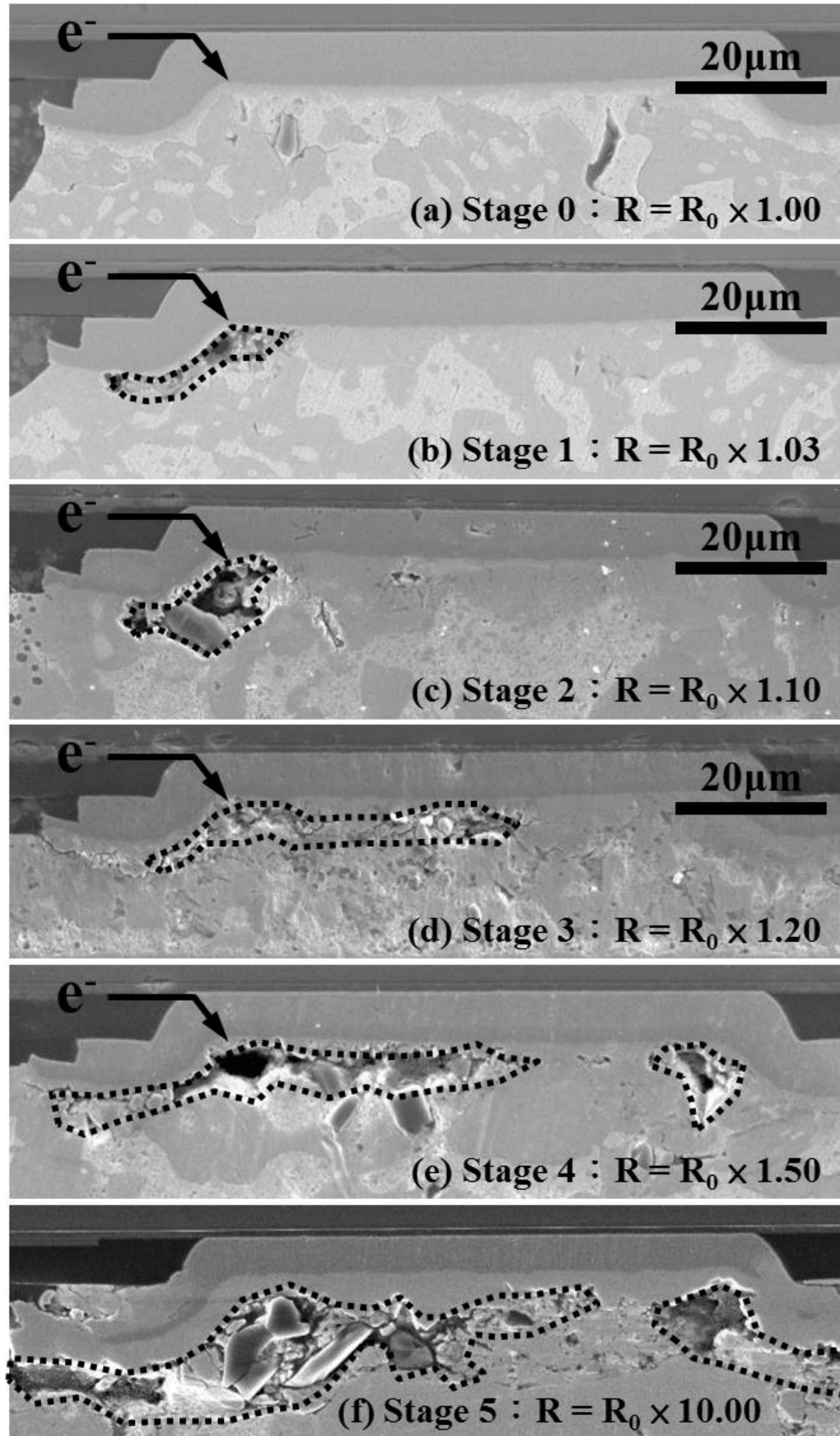


Figure 3-2 (a) Stage 0 (initial stage), (b) stage 1, (c) stage 2, (d) stage 3, (e) stage 4, and (f) stage 5 of the failure caused by EM test.

Stage	Normalized bump resistance	Real time (hr)	Normalized time ($\times 10^{-2}$)
0	1.00	0.0	0.0
1	1.03	29.8	3.9
2	1.10	101.5	13.4
3	1.20	140.0	18.5
4	1.50	155.3	20.5
5	10.00	383.0	50.6
Final	open	756.6	100.0

Table 3-1 Current stressing time at different stages.

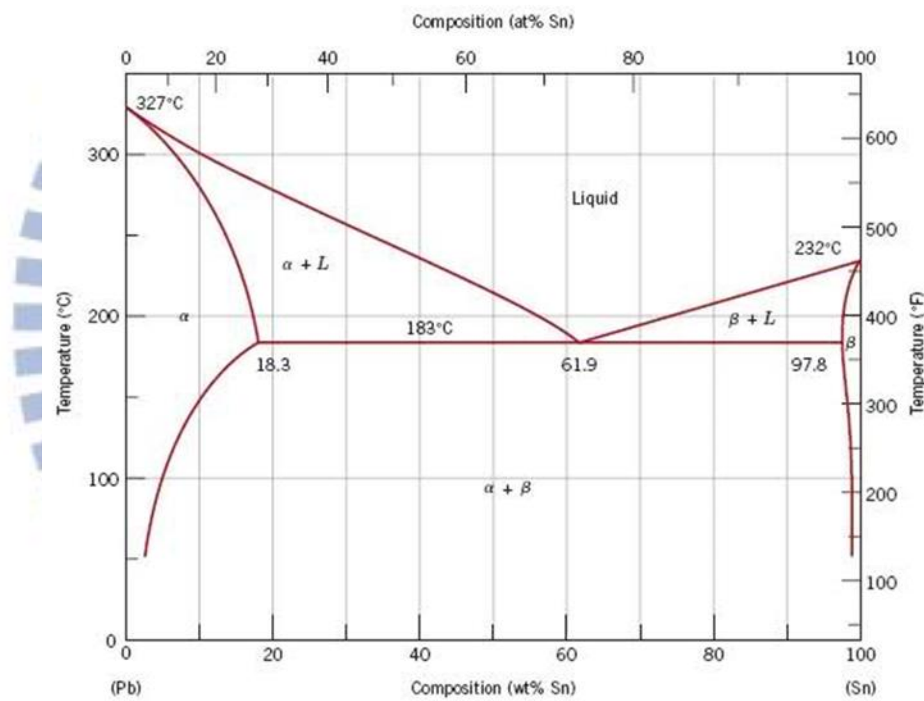


Figure 3-3 Binary Pb-Sn phase diagram.

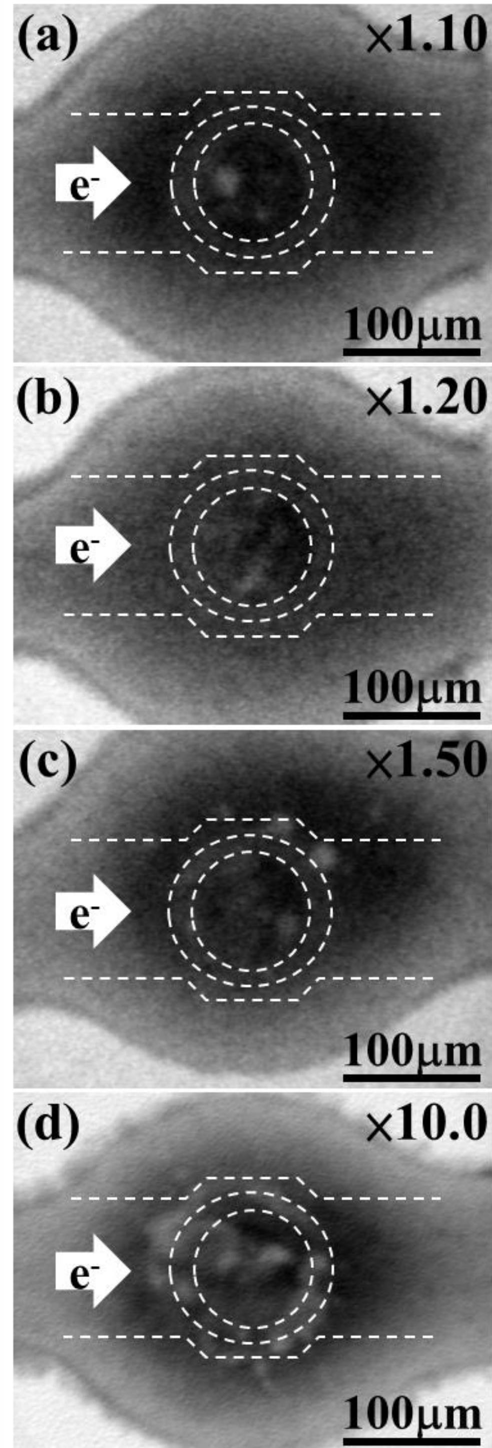


Figure 3-4 Plan-view X-ray image of (a) stage 2, (b) stage 3, (c) stage 4, and (d) stage 5.

3.1.3. Void Growth Rate in Flip-Chip Bumps

The 2D X-ray images were also employed to calculate the void area and the void depletion rate at different stages. The void depletion rate is defined as the horizontal length of the void divided by the current stressing time, as shown in Figure 3-5. Figure 3-5 (a) shows the relation between void depletion area and current stressing time, and the number in brackets after the stage number is the percentage of void depletion on the area of UBM opening. Figure 3-5 (b) shows the void depletion velocity along the interface between the IMC and the solder. As can be seen, the initial void depletion velocity was 1.27 μm/hr and reached the maximum of 1.84 μm/hr at stage 2. At stage 3, the depletion velocity dropped dramatically to 0.65 μm/hr, which was only one third of that at stage 2. Thereafter, the depletion velocity continued decreasing until the end of EM testing.

The depletion velocity did not reach the maximum because the void took some incubation time to nucleate. Therefore, the initial depletion velocity was not so large. After void nucleation, the spot of current crowding spread from a point to the surrounding edge of the void, and the maximum current density caused by current crowding consequently decreased. With the combined effect of phase coarsening mentioned in section 3.1.2, the depletion velocity dropped dramatically.

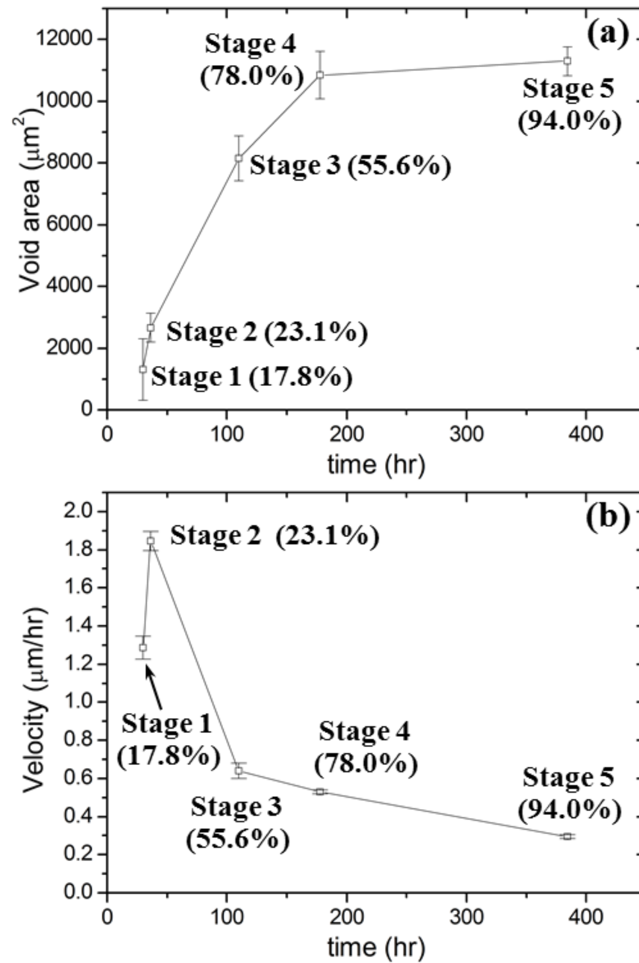


Figure 3-5 (a) Void depletion area at different stages during EM testing; and (b) void depletion velocity along the interface at different stages during EM testing.

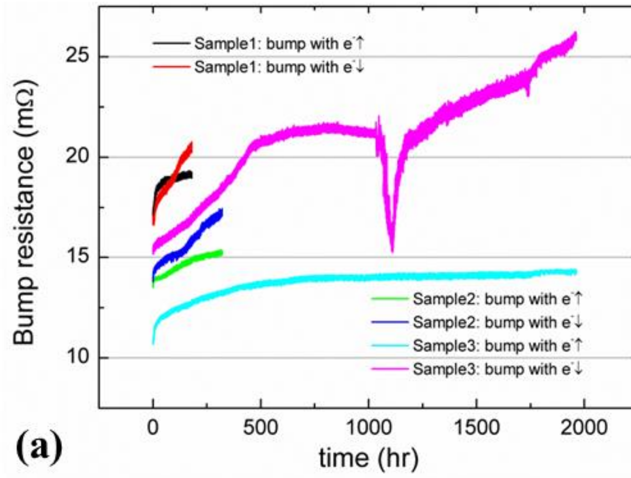
3.2. Electromigration Test Results of Six-Micro-Meter Microbumps

3.2.1. Bump Resistance of Six-Micro-Meter Microbumps

Contrary to the concave-up curve behavior shown by the bump resistance of flip-chip bump, the bump resistance curves of 6-μm microbumps are concave-down, as shown in Figure 3-6. Figure 3-6 (a) shows the bump resistances obtained from the Kelvin bump structures in 6-μm microbump samples. Since the microbump in 3D-IC is still a new topic in this decade, the fabrication technique is still developing. The fabrication technique of microbump bonding was not as stable as that of the flip-chip bonding. Moreover, the low bump height and ultra-fine pitch made the bonding of 6-μm microbump tough to achieve. As a result, the initial bump resistance of 6-μm microbumps ranged very widely from 11 mΩ to 17 mΩ. To observe only the increase in bump resistances, all the values were subtracted by the average of the data in the first 10 min, and the increases obtained are shown in Figure 3-6 (b). In Figure 3-6, the concave-down curve means that bump resistance took almost no incubation time to increase for a period and then remained at a certain level for a long time. The curves of 6-μm microbumps differing from those of flip-chip bumps indicate different microstructure evolutions in 6-μm microbumps. In flip-chip bumps, void nucleation and propagation was observed at the interface between IMC and solder, thus yielding a concave-up bump resistance curve. On the contrary, the low-height microbump resistance remaining constant after a period of increase might denote a transformation from the original microbumps into some kinds of structures with high EM resistance. According to the references cited in section 1.3, such high-EM-resistance structure was very likely the IMC, Ni_3Sn_4, produced through the reaction between Ni and Sn.

Owing to its higher melting point and higher tensile modulus, the EM resistance of Ni_3Sn_4 should be much higher than that of Sn2.5Ag. After the Ni_3Sn_4 growth during initial testing, the 6-μm microbumps were transformed into micro IMC bumps. Owing to such transformation, the bump resistance remained at a certain level.

However, the magnitude of current (density) may significantly change the microstructure evolution as shown in Figure 3-7. Figure 3-7 (a) shows the bump resistance of 6-μm microbumps tested by 0.24 A (9.2×10^4 A/cm^2) on the 150℃ hot plate, and Figure 3-7 (b) shows increase in bump resistance. As can be seen, both concave-up and concave-down bump resistance curves were obtained, showing that microstructure evolution in 6-μm microbumps is dependent on the magnitude of current (density) applied in the test. Under low current density, 4.6×10^4 A/cm^2, IMC growth dominated the microstructure evolution; while under high current density, 9.2×10^4 A/cm^2, void formation became the main characteristic of 6-μm microbumps, similar to that in flip-chip bumps. In Figure 3-7, both the microbumps in sample 4 and the microbump tested by downward electron flow in sample 5 produced concave-up curves, while the microbump tested by upward electron flow in sample 5 generated the concave-down curve. Moreover, the rates of increase in bump resistances tested under 9.2×10^4 A/cm^2 were much higher than those tested under 4.6×10^4 A/cm^2, thus resulting in shorter time to failure.



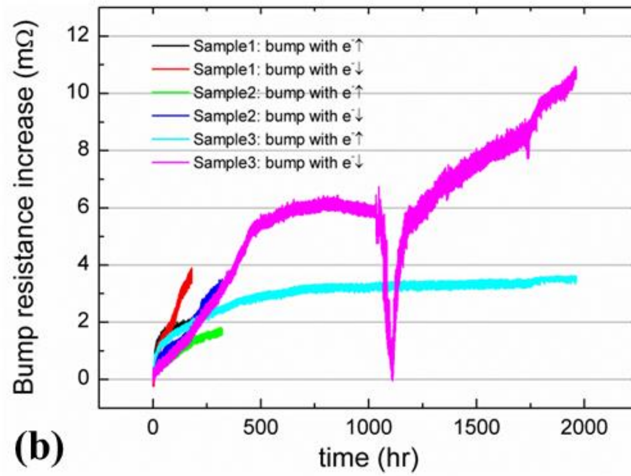


Figure 3-6 (a) Bump resistances and (b) increase in bump resistances of 6-μm microbumps after current stressing by 0.12 A (4.6×10^4 A/cm^2) on 150℃ hot plate for different durations.

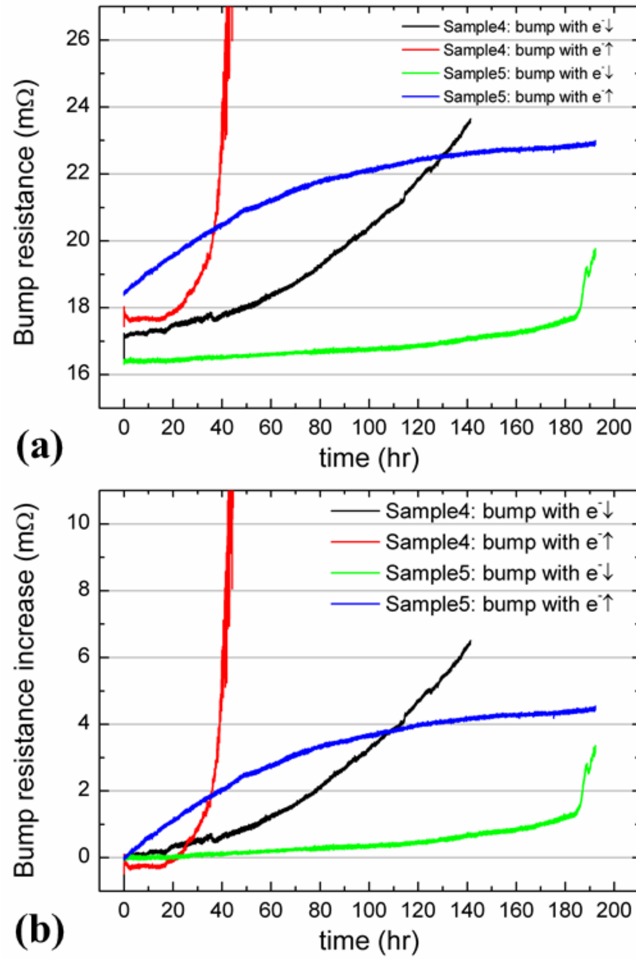


Figure 3-7 (a) Bump resistances and (b) increase in bump resistances of 6-μm microbumps after current stressing by 0.24 A (9.2×10^4 A/cm^2) on 150℃ hot plate for different durations.

3.2.2. Microstructure Evolution in Six-Micro-Meter Microbumps

In the previous section, the concave-down curve indicates the formation of high-EM-resistance structure in 6-μm microbumps, which is very likely the IMC, Ni_3Sn_4. This inference could be proven by the SEM images (the cross-sectional view of the microbumps tested under 4.6×10^4 A/cm^2 on the 150℃ hot plate) in Figure 3-8. As can be seen, the images are marked as a1 to a3, b1 to b3, and c1 to c3, with the letter referring to the sample and the number denoting the microbump tested. Samples "a," "b," and "c" were 6-μm microbumps tested for 49.8 hr, 321.6 hr, and 1961.8 hr, respectively; while microbumps "1," "2," and "3" were tested under no current stressing, upward electron flow, and downward electron flow, respectively. After EM testing, all the images obtained showed obvious Ni_3Sn_4 growth, which corresponded with the inference stated in section 3.2.1. The formation of Ni_3Sn_4 was a very important issue. The electrical resistivity of Ni_3Sn_4 is 28.5 μΩ-cm, which is the highest resistivity in the Cu-Ni-Sn reaction system. It is 2 times higher than that of Sn2.5Ag, 13.0 μΩ-cm, 4 times higher than that of Ni, 6.8 μΩ-cm, and almost 17 times higher than that of Cu, 1.7 μΩ-cm. Besides having high resistivity, Ni_3Sn_4 was also brittle, so the transformation may lower the reliability under structural testing. Although the concave-down bump resistance curve revealed clearly the formation of high-EM-resistance structures, there were some unique phenomena worth mentioning.

After EM testing for 49.8 hr, some Sn2.5Ag was found in the microbump without current stressing, as shown in Figure 3-8 (a1). Ni UBMs on both chip side and interposer side were not seriously consumed, and the initial scallop-shaped Ni_3Sn_4 between solder and Ni became plate-shaped [2]. Unlike the non-stressed one, microbumps tested by the upward and downward electron flow showed obvious polarity effect. The cathode-side UBMs driven by EM were quickly dissolved into the

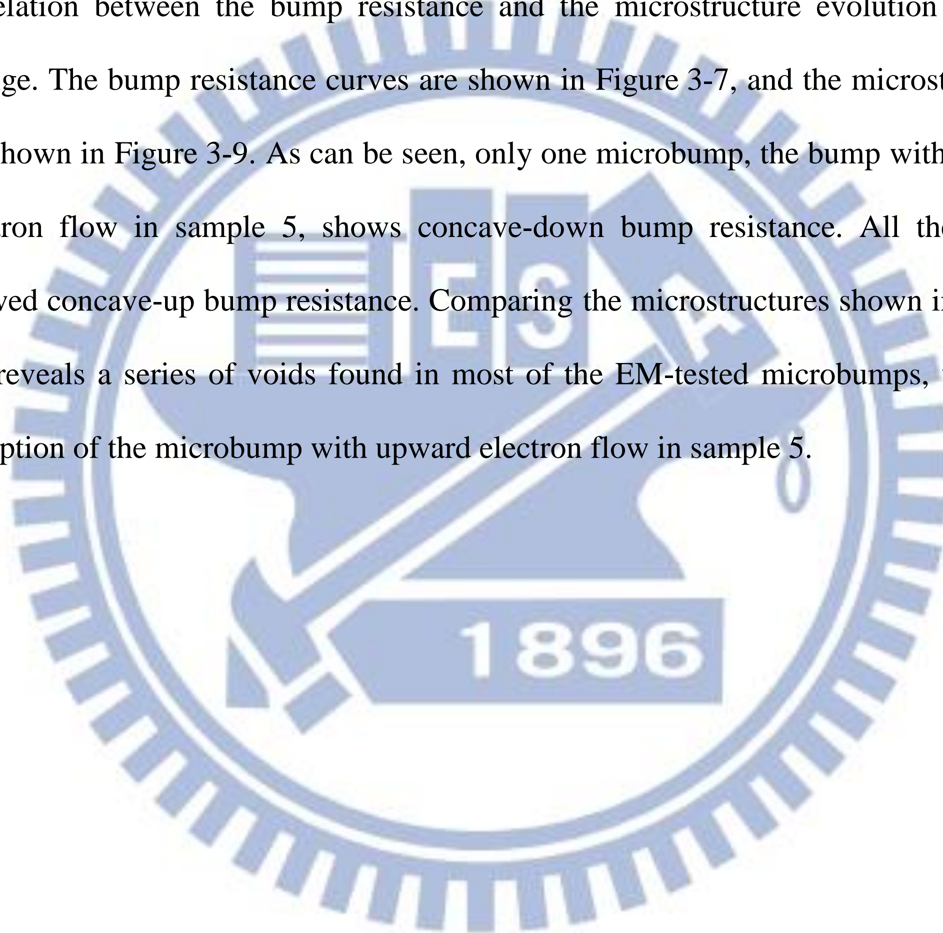
solder and formed IMC. In Figure 3-8 (a2) and (a3), over 80% of the solder was transformed into Ni_3Sn_4, which possessed higher EM resistance than the solder. However, the bump resistances in Figure 3-6 took almost 500 hr to reach the long-time constant value, implying that the transformation from solder to Ni_3Sn_4 took around 500 hr to complete. It seemed that these two results, the fast phase transformation and the slow bump resistance increase, went against each other. However, such was actually possible for two reasons. First, the distribution of Ni_3Sn_4 affects the increase in bump resistance; and second, the Sn grain orientation has a significant impact on the diffusivity of Ni in Sn. In Figure 3-8 (a2) and (a3), Ni_3Sn_4 was not found to be of plate-shaped. Some residual Sn2.5Ag was dispersed in the Ni_3Sn_4, preventing the bump resistance of 6-μm microbumps from immediate increase [77]. The bump resistance stopped increasing when the transformation completed. The Sn grain orientation affects more the diffusivity of Ni in Sn than the distribution of Ni_3Sn_4 [78]. At room temperature, the diffusivity of Ni in Sn with parallel grain orientation is 2.04×10^6 times higher than that with perpendicular grain orientation ($D_{\parallel, RT} = 1.41 \times 10^{-5}$ cm^2/sec and $D_{\perp, RT} = 6.91 \times 10^{-12}$ cm^2/sec). At 100℃, the difference is still 1.20×10^5 times ($D_{\parallel, RT} = 5.84 \times 10^{-5}$ cm^2/sec and $D_{\perp, RT} = 4.85 \times 10^{-10}$ cm^2/sec). In microbump samples, the pitch was lowered to 30 μm to increase the I/O density, so the diameter was only 18 μm. In this circumstance, only one to two grains could be found in a microbump. Therefore, the difference in diffusivity caused by Sn grain orientation affected the Ni diffusion in Sn and the consequent Ni_3Sn_4 growth.

Figure 3-8 (b) shows the microbumps tested for 321.6 hr. In Figure 3-8 (b2) and (b3), no residual Sn2.5Ag was observed in the microbumps at this stage of EM testing. Similar to the polarity effect found in Figure 3-8(a2) and (a3), the cathode UBM

became non-uniform. The Ni atoms were driven by EM to the anode side so the anode-side IMC was thicker than the cathode-side, and the crack formed near the anode side. This phenomenon was also found in the sample tested for 1961.8 hr. Whether the microbumps have upward or downward electron flow, cracks were observed between the IMC. However, the crack did not expand smoothly because the crack was not caused by external stresses. Instead, they were caused by the reaction between Ni and Sn. The molecular volume of Ni_3Sn_4 was smaller than the sum of Ni and Sn. The volume shrank by 10.5% after the reaction between Ni and Sn [79]. In view of the previous observations, it can be concluded that the microstructure evolution of 6-μm microbumps under EM testing involved the following four changes. (1) In the initial stage of testing, the Ni atoms driven by EM quickly diffused into Sn2.5Ag and formed Ni_3Sn_4. The fast-growing Ni_3Sn_4 on the chip side and on the interposer side then came into contact, and the residual Sn2.5Ag dispersed between IMCs. (2) The residual Sn2.5Ag continued reacting with the Ni atoms and then formed voids between the chip-side IMC and the interposer-side IMC. Once several voids became connected, they looked like a crack between the IMCs. (3) Owing to the high EM resistance of Ni_3Sn_4, such status remained for a long time until the Ni cathode-side Ni ran out. (4) After Ni became insufficient, the cathode-side Cu joined the reaction and turned Ni_3Sn_4 into $(Ni, Cu)_3Sn_4$, $(Cu, Ni)_6Sn_5$, and Cu_3Sn. The resistivity of Cu_6Sn_5 and Cu_3Sn are only 16.5 μΩ-cm and 8.5 μΩ-cm, which are only two-thirds and one-third that of Ni_3Sn_4, respectively. As a result, the bump resistance of sample 3 showed an obvious drop after being tested for 1000 hr. The volume shrinkage during Ni_3Sn_4 formation caused not only the crack between IMCs but also the big void beside the joint. Ouyang *et al*. reported some very similar results in 2012 [80]. In their study, some microbumps, after transforming into IMC bumps, lasted for

over 4000 hr under 8×10^4 A/cm^2 at 150°C. However, they did not use Kelvin bump structures to monitor the bump resistance, so they did not observe the correlation between the concave-down bump resistance curve and the microstructure evolution under EM testing. This difference shows the power of Kelvin bump structures and the importance of monitoring the bump resistance of a single bump.

Under severe stressing condition, 9.2×10^4 A/cm^2 on the 150°C hot plate, the correlation between the bump resistance and the microstructure evolution did not change. The bump resistance curves are shown in Figure 3-7, and the microstructures are shown in Figure 3-9. As can be seen, only one microbump, the bump with upward electron flow in sample 5, shows concave-down bump resistance. All the others showed concave-up bump resistance. Comparing the microstructures shown in Figure 3-9 reveals a series of voids found in most of the EM-tested microbumps, with the exception of the microbump with upward electron flow in sample 5.



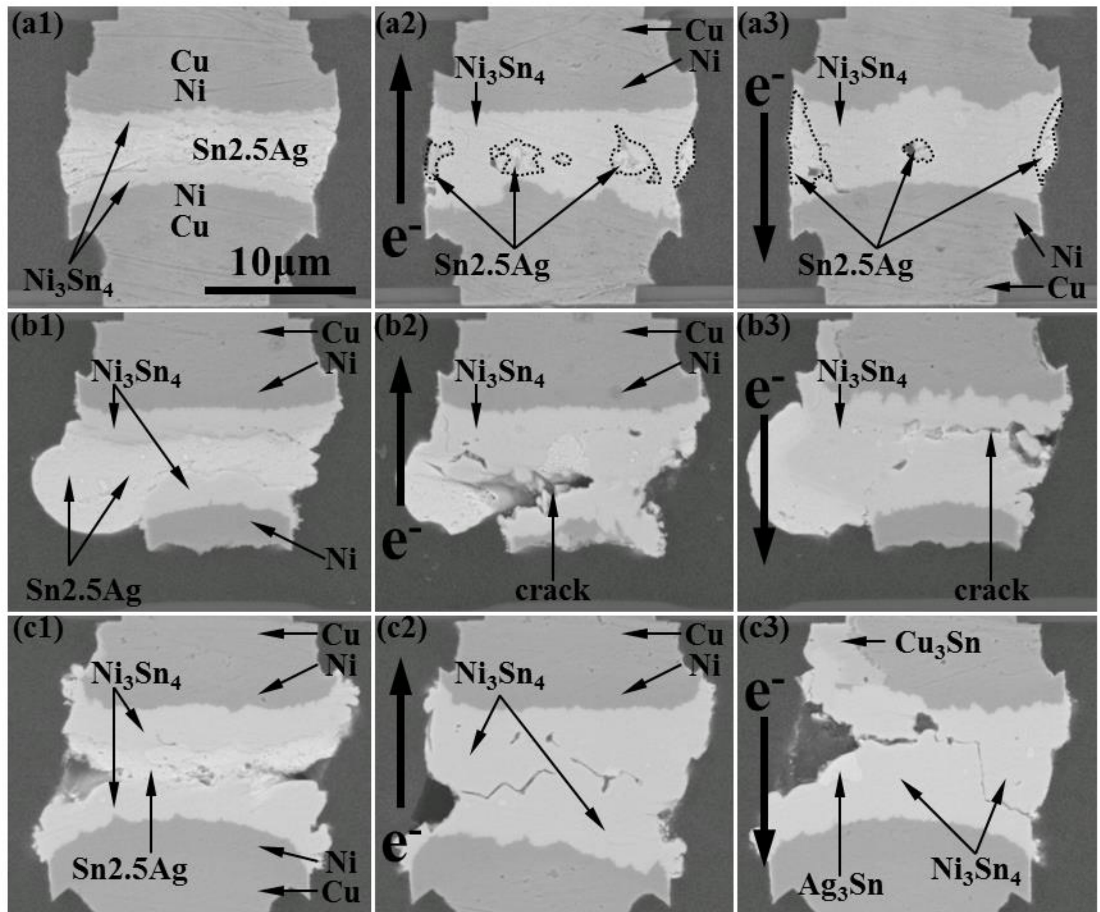
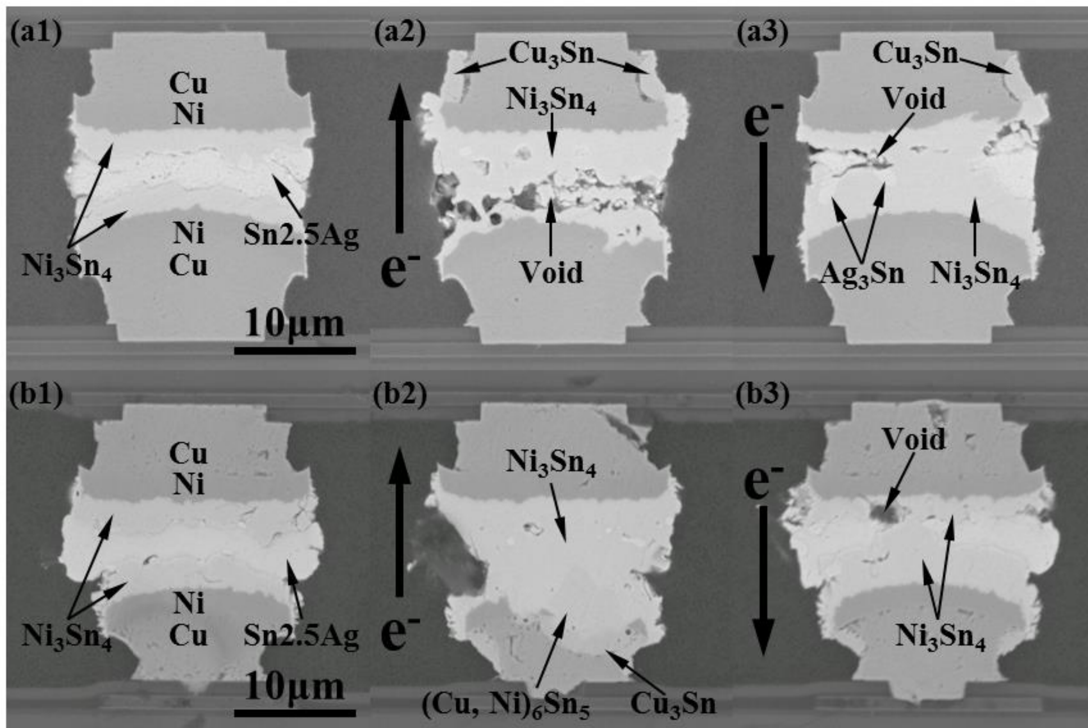


Figure 3-8 6-μm microbumps in samples EM tested for (a) 49.8 hr, (b) 321.6 hr, and (c) 1961.8 hr by 0.12 A (4.6×10^4 A/cm^2) on 150°C hot plate.



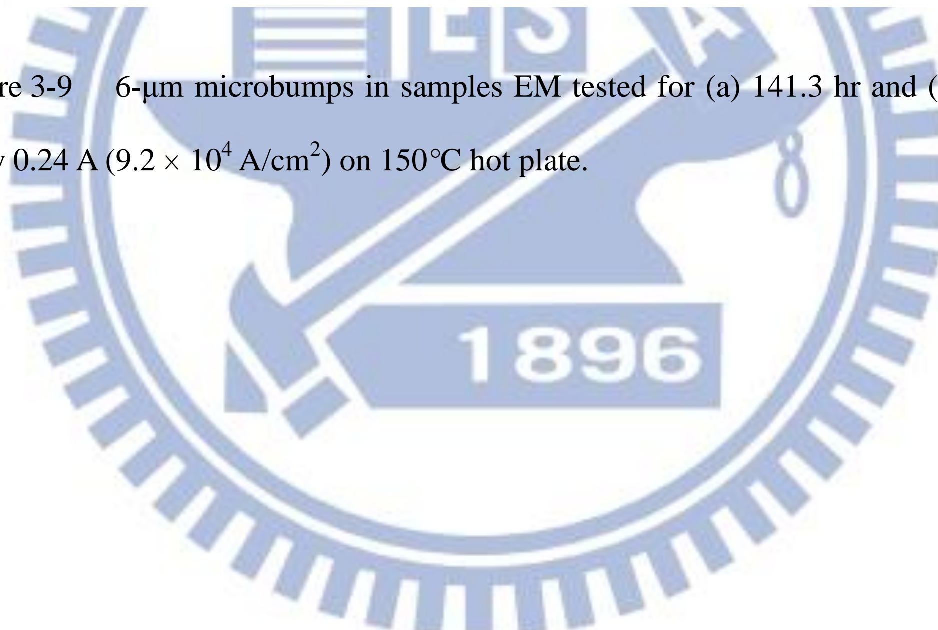


Figure 3-9 6-μm microbumps in samples EM tested for (a) 141.3 hr and (b) 192.3 hr by 0.24 A (9.2×10^4 A/cm^2) on 150℃ hot plate.

3.2.3. Bump Resistance at Different angles in Six-Micro-Meter Microbumps

The microbump resistance measured at 0°, 60°, 120°, and 180° are 114.7 mΩ, 45.9 mΩ, 14.6 mΩ, and 13.7 mΩ, respectively; as shown in Table 3-2 and Figure 3-10. However, the resistance is only 13.5 mΩ if a microbump is viewed as an ideal stack of circular metal disks when the current is uniformly distributed in every layer of metal disks. The microbump resistance at 0° monitored by Kelvin bump structures exceeded 100 milliohms, which is seven to nine times larger than 13.5 mΩ. If the solder joint is defined to include Al pads, UBM materials, IMCs, and the solder, the microbump resistance obtained at 0° is closest to the actual microbump resistance because this measurement contains the full voltage drop across the entire solder joint system. The large microbump resistance consequently arouses concern because RC delays can significantly change heat distribution caused by Joule heating. Therefore, understanding the cause of the unexpected large microbump resistance is the first step to improving electrical performance.

With increase in measurement angle, the microbump resistance decreases due to the current crowding effect. That is, when the current changes its flow direction, in order to reduce the total resistance in the microbump, a non-uniform current flows through a small area resulting in current crowding. Under this circumstance, the measurement position at high angle is too far to detect the full voltage drop along the solder joint [81]. Therefore, the microbump resistance decreases significantly with increasing measurement angle.

Sample	b_5 (e^- ↑)		t_{5-6}	b_6 (e^- ↓)			
	0°	180°		0°	60°	120°	180°
No.1	113.5	14.2	139.8	118.3	47.4	14.5	13.4
No.2	110.3	18.9	141.2	111.0	44.3	14.7	11.9
No.3	115.7	13.9	143.7	113.5	—	—	13.6
No.4	115.1	13.2	142.3	116.0	—	—	15.7
Average	113.7	15.1	141.8	114.7	45.9	14.6	13.7

Table 3-2 Bump resistance of 6-μm microbumps at different angles and trace resistance of t_{5-6}.

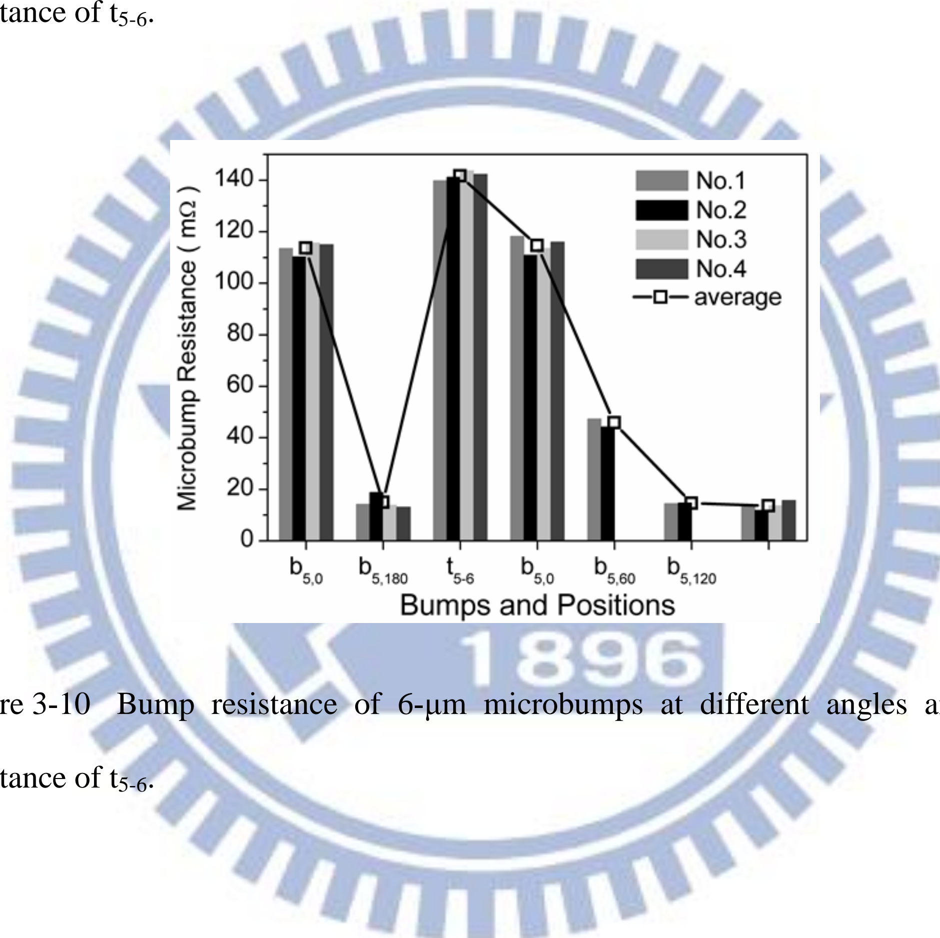


Figure 3-10 Bump resistance of 6-μm microbumps at different angles and trace resistance of t_{5-6}.

3.3. Electromigration Test Results of Ten-Micro-Meter Microbumps

3.3.1. Resistance of Ten-Micro-Meter Microbumps

The resistance of 10-μm microbumps show two curve behaviors in combination, as shown in Figure 3-11. That is, the first half of the curve was concave-down while the second half of the curve was concave-up, implying a change in failure mechanism from UBM dissolution (IMC growth) to void formation during EM testing. According to the rate of increase in resistance, EM testing could be divided into three stages. In the first stage, the resistance rose very rapidly and then slowed down gradually, meaning that the rate of increase was initially large, followed by a decrease. In the second stage, the rate of increase in resistance remained constant; and finally rose again in the third stage.

The shape of the resistance curves of 10-μm microbump samples were very regular because the resistance obtained included that of eight microbumps, while the resistance for the 6-μm microbumps included the resistance of only one sample. With more samples included, the differences between bumps were diminished. Therefore, the effect of grain orientation mentioned in section 3.2.2 becomes less significant, and the regularity of 10-μm microbump samples consequently becomes better than the 6-μm ones. Moreover, the resistance curves obtained under various testing conditions showed the same shape (concave-down initially and then concave-up), indicating very stable failure mechanism under these testing conditions.

Although the resistance curve of 10-μm microbumps in the first stage behaved concave-down, same as the bump resistance of 6-μm microbumps, there was a critical difference between them. That is, the bump resistance of 6-μm microbumps reached a

constant value, but the resistance of 10-μm microbumps did not, implying complete transformation from solder into IMC not found in 10-μm microbump samples, possibly due to the larger solder volume (bump height). The volume ratio of reaction between Ni and Sn is 1:3.26 [79]. That is, 1.00-μm Ni dissolving into Sn consumes 3.26-μm Sn. Because EM retarded the anode-side reaction, only one-side dissolution was considered. In 10-μm microbump samples, the Ni thickness on both chip side and interposer side were 2 μm, meaning 6.52-μm Sn consumption. In 10-μm microbump samples, the height of solder is nearly 12 μm. For the 10-μm microbumps stressed by downward electron flow, the cathode-side UBM (15-μm Cu/2-μm Ni) was sufficient for reaction. However, the cathode-side UBM of the bump tested by upward electron flow (2-μm Ni) was going to exhaust and form voids after a period of testing. The height was crucial for the bump resistance to reach constant value.

After the resistance grew by a constant rate for a period of time (stage 2), the void nucleated and propagated at the interface between IMC and solder. Same as the void formation and propagation observed in flip-chip bumps, the voids reduced the area conducting current and caused the bump resistance to increase rapidly again.

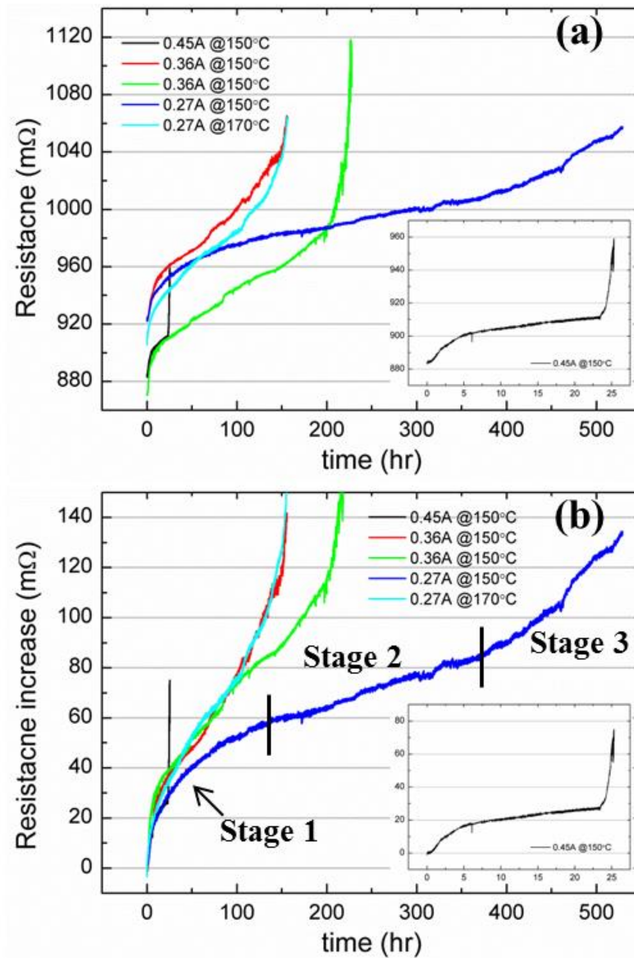


Figure 3-11 (a) Bump resistance and (b) increase in bump resistance of 10-μm microbumps during EM testing.

3.3.2. Microstructure Evolution in TenMicro-Meter Microbumps

The microstructures of samples after EM testing are shown in Figure 3-12. Figure 3-12 (a) to (d) show the samples tested for 25.3 hr by 0.45 A (1×10^5 A/cm^2) in a 150℃ oven, for 227.9 hr by 0.36 A (8×10^4 A/cm^2) in a 150℃ oven, for 529.1 hr by 0.27 A (6×10^4 A/cm^2) in a 150℃ oven, and for 194.3 hr by 0.27 A in a 170℃ oven, respectively. Generally speaking, the failure mechanisms in these samples were very regular.

In microbumps stressed by upward electron flow, the cathode-side (interposer-side) UBM was quickly dissolved and driven to the anode side by EM. The surface of the adhesive layer, Ti, then became the nucleation point of void. Furthermore, the Ti layer was depleted by EM in Figure 3-12 (c2) and (d2). The Cu in the interposer-side trace was therefore depleted, too. Moreover, the void was formed not only at the position of the cathode-side UBM, but also at the center of the microbumps. In section 3.2.1, Ni_3Sn_4 was introduced as a material of high EM resistance. Once the migration of Ni driven by EM was not fast enough to reach the anode side, the Ni_3Sn_4 tended to form at the anode side, which further blocked the subsequent Ni migration, thus making the interface between the solder and IMC the new void nucleation site.

On the contrary, voids were observed at the interface between the cathode-side (chip-side) IMC and the solder. For the samples tested for longer durations and at higher temperatures, Figure 3-12 (c3) and (d3) shows more obvious voids, but they seemed not so obvious in Figure 3-12 (a3) and (b3). Such difference was caused by the sample preparation. To eliminate such discrepancy, the focused ion beam (FIB) was applied. Figure 3-13 shows the microbumps tested by 8×10^4 A/cm^2 in the 150℃ oven, with Figure 3-13 (a) and (b) illustrating microbumps with downward and

upward electron flow, respectively. The void could be found at the interface between the IMC and the solder in Figure 3-13 (a) and at the position that was originally the Ni UBM in Figure 3-13 (b). Though the voids in Figure 3-12 (a3) and (b3) were not clear, the FIB images indicated that void formation still dominated the bump resistance of the microbumps.

In addition, the residual of solder in all of the EM-tested microbumps corresponded with the resistance behavior observed in section 3.3.1.

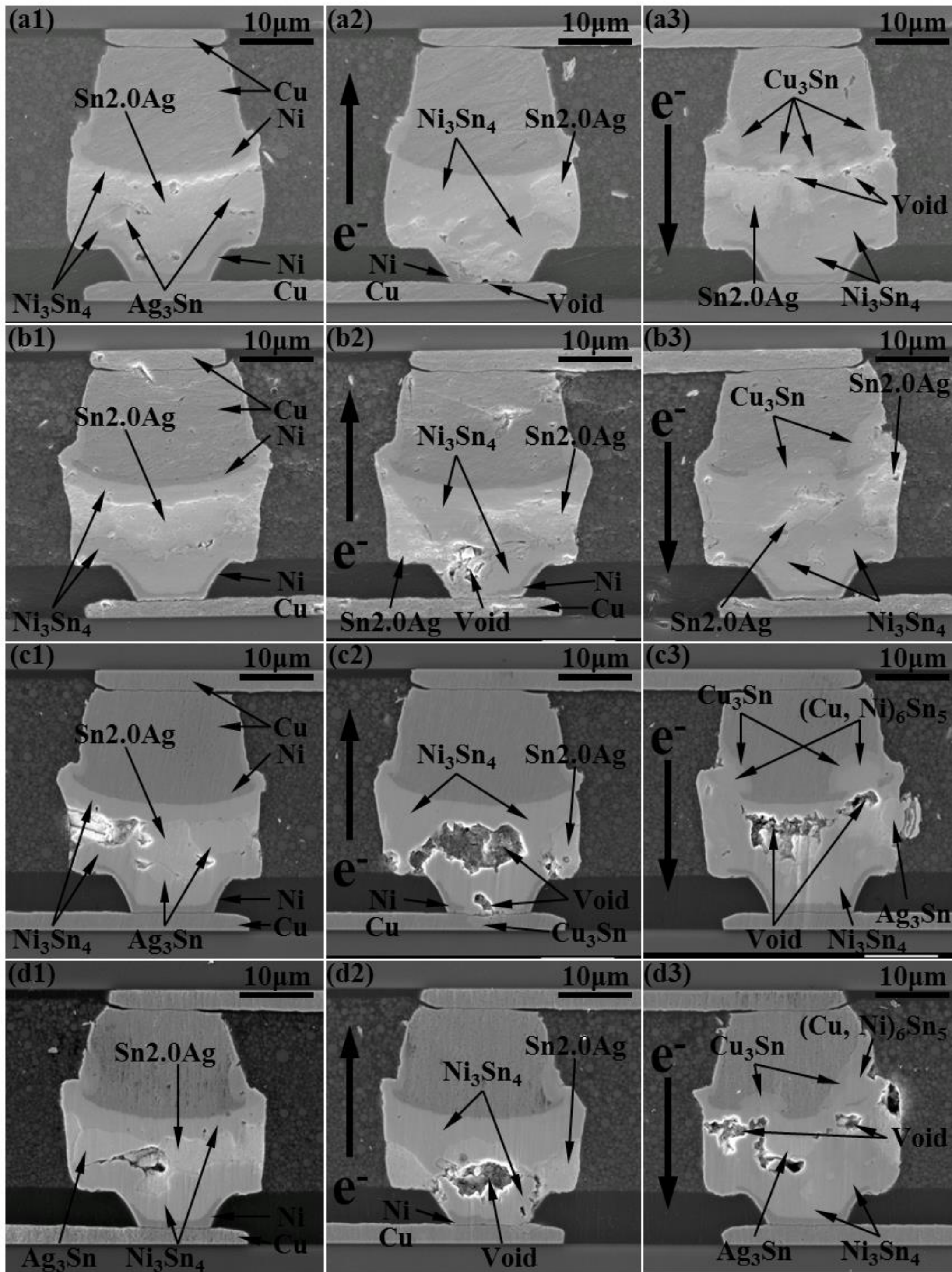


Figure 3-12 10-μm microbump samples EM tested (a) for 25.3 hr by 0.45 A (1×10^5 A/cm^2) in 150℃ oven, (b) for 227.9 hr by 0.36 A (8×10^4 A/cm^2) in 150℃ oven, (c) for 529.1 hr by 0.27 A (6×10^4 A/cm^2) in 150℃ oven, and (d) for 194.3 hr by 0.27 A in 170℃ oven.

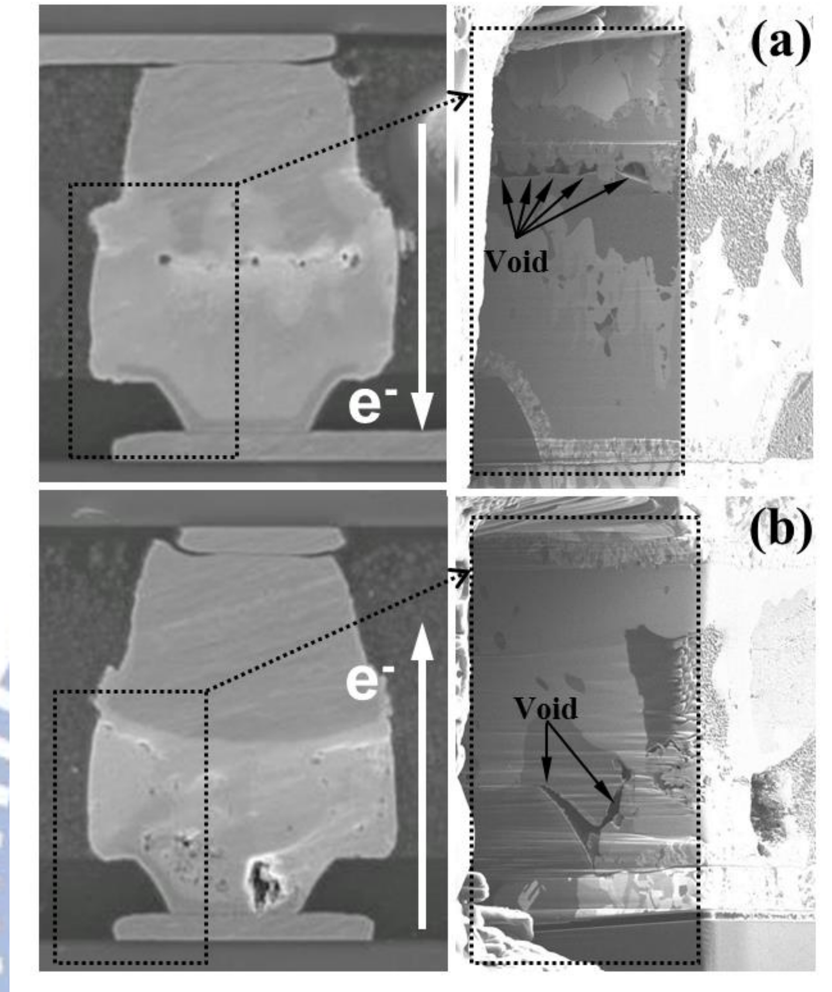


Figure 3-13 The cross-sectional focused ion beam (FIB) image of the bump stressed by (a) downward electron flow and (b) upward electron flow.

3.4. Results of Finite-Element Analysis

3.4.1. Finite-Element Analysis of Scallop Intermetallic Compounds

To decrease the difficulty of model construction and reduce solution time, the scallop IMCs were all assumed to be of plate shape. The effect of such simplification must be made clear before the other finite-element analyses.

Figure 3-14 shows the results of the scallop IMC model. Figure 3-14 (a) is the cross-sectional view of the entire model. Only the chip-side IMC became scallop shape because the thin Al trace at the chip side usually intensified the current crowding effect. The substrate-side IMC was maintained to be of plate shape. Figure 3-14 (b) and (c) displays the enlarged plots of the current density distribution and the voltage distribution near the current-crowding region. As seen in Figure 3-14 (b), high current density appeared in the valleys between the scallop IMCs since the resistivity of the solder is lower than that of IMCs. According to the kinetics analysis, the valley region between scallop IMCs acted as the short cut for atoms to diffuse [2]. Therefore, the high current density at the valley regions tended to enhance this effect, thus flattening the IMCs. The non-uniform current density distribution caused by the scallop IMCs was actually diminished also by the scallop shape. In terms of voltage, the voltage distribution in the scallop IMC model did not differ much from that in the plate IMC model, as seen in Figure 3-15. To conclude, simplifying scallop IMCs into plate IMCs did not significantly affect the EM failure mechanism.

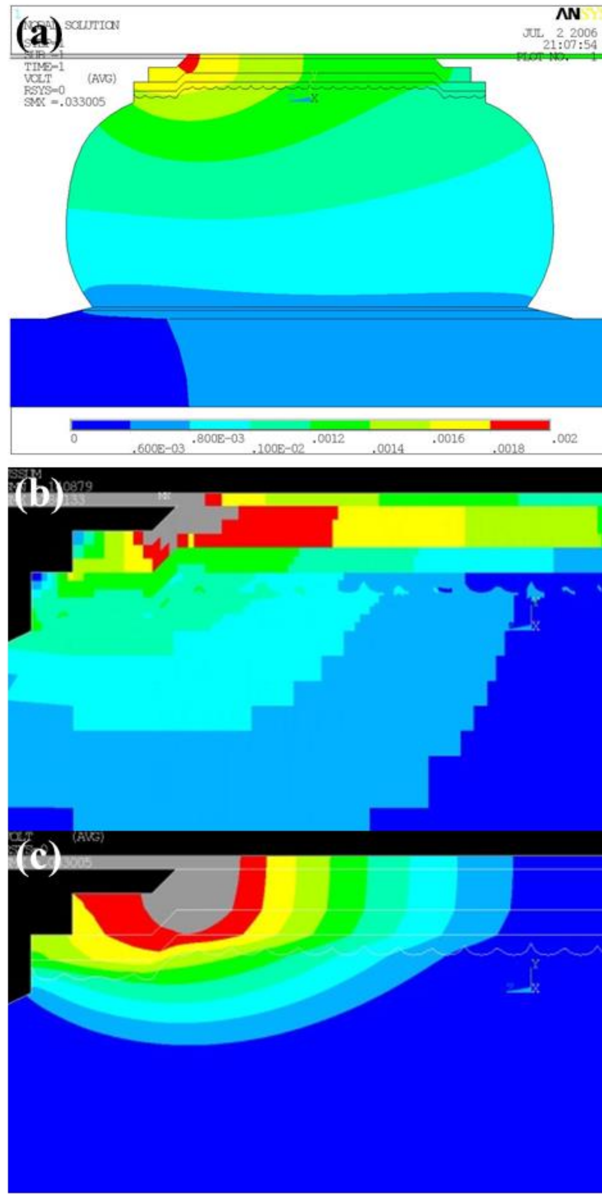


Figure 3-14 (a) Cross-sectional view of scallop IMC model; (b) current density distribution and (c) voltage distribution of current crowding region in the scallop IMC model.

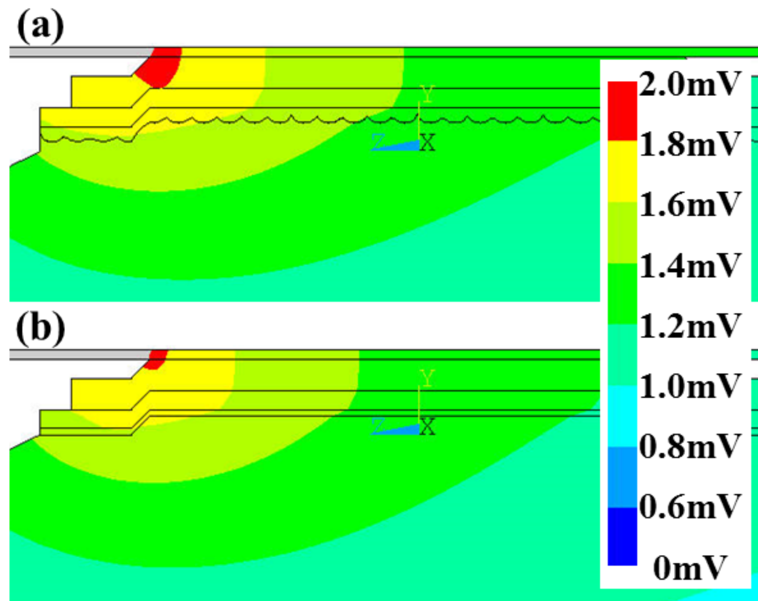


Figure 3-15 Voltage distribution of (a) scallop IMC model and (b) uniform-thickness IMC model.

3.4.2. Finite-Element Analysis of Flip-Chip Bumps

Figure 3-16 displays the results of FEM. Figure 3-16 (a) and (b) shows the oblique and the cross-sectional current density and voltage distributions, respectively; Figure 3-16 (c) and (d) shows the current density distributions at the planes marked “c” and “d” in (b), respectively. The maximum was located in the Al trace because of the minimum cross-sectional area. After the current reached the UBM, the thick UBM (5-μm Cu/3-μm Ni) relieved the current crowding effect and lowered the maximum current density inside the solder. The maximum current density in the solder was 2.36 $\times 10^4$ A/cm^2, and the crowding ratio (CR) was 3.34. The high-current-density region had a moon shape, as seen in Figure 3-16 (c1) because the Al pad was wider than the passivation opening and tended to conduct the current to the two wings.

To simulate how the current density distribution was affected by void formation, a series of models with voids were built by replacing the elements of solder containing high current density with nonconductive elements. The results of the series of models are shown in Figure 3-17. In the beginning, the high-current-density region was located at the left side near the current-crowding site. The void was first growing to the left side and then to the right side. During the procedure, the high-current-density region was driven to the right side by the growing void. Another interesting phenomenon was that the low-resistivity UBM conducted the current to the right as a short cut. As a result, the high-current-density region was divided into two parts at the end stage of void propagation.

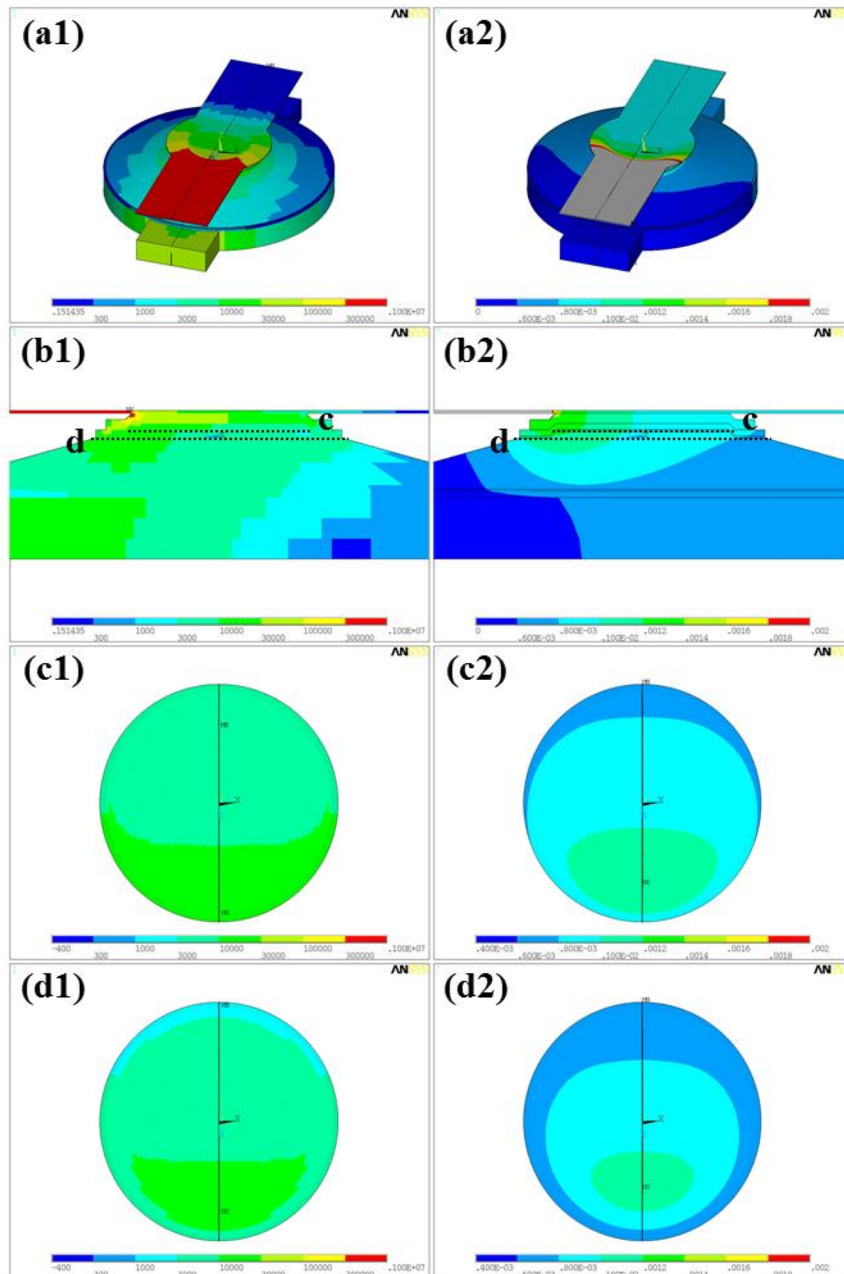


Figure 3-16 (a) Oblique view and (b) cross-sectional view of the entire flip-chip bump model; (c) plan-view distribution of the plane marked as “c” in (b); and (d) plan-view distribution of the plane marked as “d” in (b).

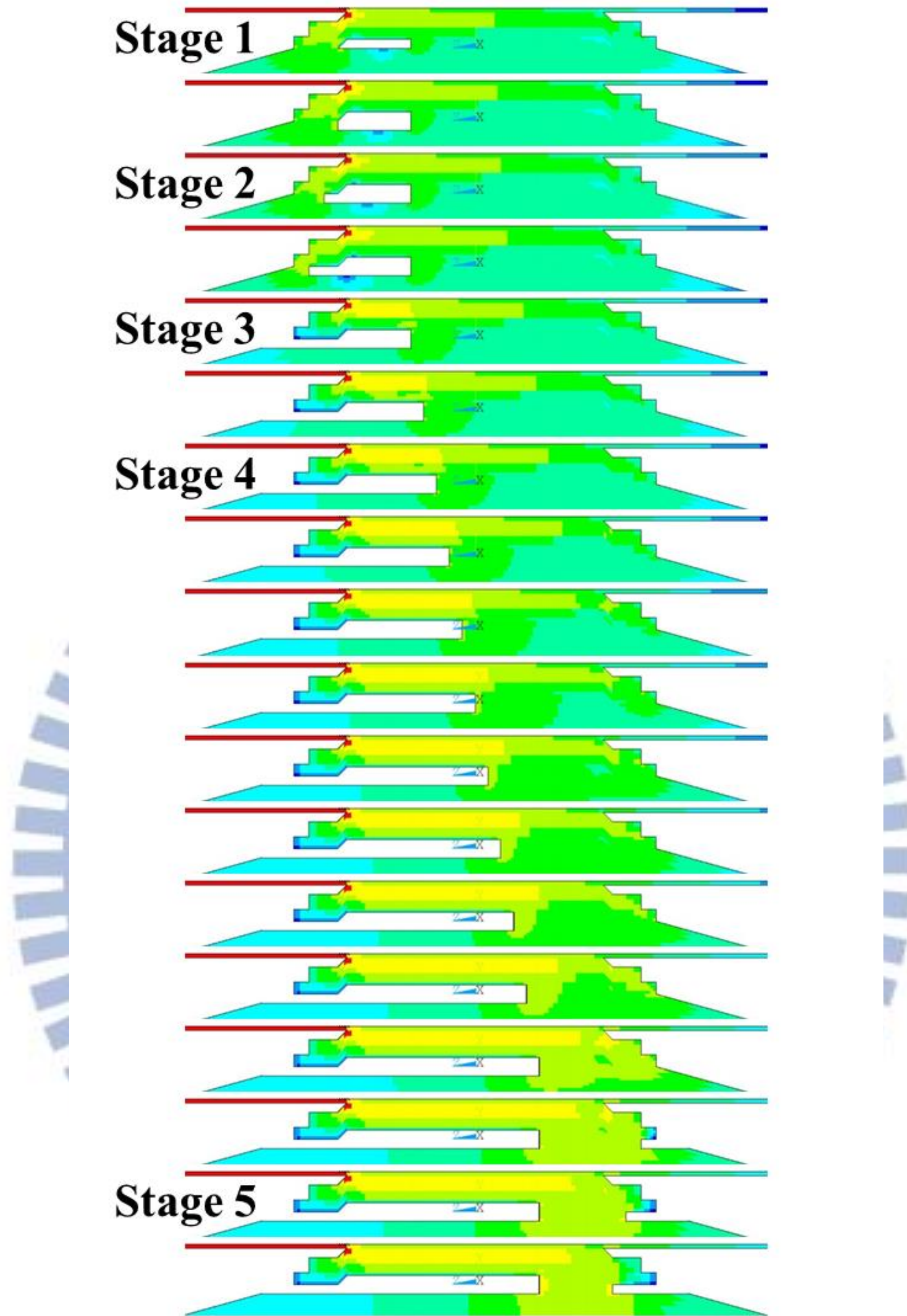


Figure 3-17 Current density distribution near current-crowding region of different stages during void propagation caused by EM.

3.4.3. Finite-Element Analysis of Six-Micro-Meter Microbumps

The FEM results of 6-μm microbumps are shown in Figure 3-18. Figure 3-18 (a) displays the oblique view of the element model with the white dashed line illustrating the direction of current flow (the reverse direction of electron flow). Figure 3-18 (b) and (c) shows the oblique and cross-sectional view of current density distribution, respectively. It was the Al traces that conducted the highest current density (denoted by red color) because of the smallest cross-section. Once the current got into the Cu UBM, the serious current crowding took place at the entrance point of the current. Owing to the change in direction of current, the maximum current reached 1.19×10^6 A/cm^2, and the CR was 25.5. However, the 5-μm Cu/3-μm Ni relieved the current crowding and reduced the maximum current density in solder to 4.80×10^4 A/cm^2. The CR in the solder was only 1.02, and the current density shown in Figure 3-18 (d) was almost uniform. Though the UBM thickness used in the flip-chip samples was the same as that in 6-μm microbumps, the 5-μm Cu/3-μm Ni in the flip-chip samples did not relieve the current crowding to this level (the CR in the flip-chip samples was 3.34). The reason will be discussed in the next chapter. Such difference pointed out the influence of volume shrinkage. Even the thickness of UBM in both flip-chip bumps and microbumps were the same, the consequent current density distribution could be totally different and caused different failure mechanisms, void formation in flip-chip bumps and IMC growth in 6-μm microbumps.

The microbump resistances at different angles were obtained for comparison with the measurement results. The resistances at 0°, 60°, 120°, and 180° obtained from the FEM were 91.7 mΩ, 52.6 mΩ, 11.6 mΩ, and 12.1 mΩ, respectively; and the trace resistance was 83.7 mΩ. Generally speaking, the values obtained using FEM were slightly lower than the measured results, but they showed the same trend. The

microbump resistance became smaller with increase in angle. The resistance at 0°, 91.7 mΩ, was 7.6 times higher than the value at 180°, 12.1 mΩ, because of the current crowding effect. The measurement angles, 120° and 180°, were relatively further away from the current-crowding spot than the other angles. As a result, the value at 120° and 180° was much smaller than the other values. The values obtained using FEM were smaller than those measured because of the Joule heating effect. To reduce the noise and the error caused by temperature variations, the microbump resistance measurements were performed on a 150°C hot plate, but FEM did not include the effect of temperature coefficient of resistance (TCR). Therefore, the microbump resistances obtained from the measurements were slightly larger than those obtained using FEM.

Furthermore, FEMs with different parts of solder transformed into IMC were built to examine the influence of IMC growth, and the result is shown in Figure 3-19. In Figure 3-19, the x-axis was the percentage of transformation. The percentage equal 100% means complete transformation of the solder into IMC. Without the current crowding effect (relieved by the UBM), the increase in microbump resistance at all angles were found to be linearly related to the IMC transformation percentage, and the magnitudes of increase were very similar. This result indicated the IMC growth did not influence the current density distribution near the current-crowding region. When the transformation percentage approached 100%, the increase in microbump resistance at all angles ranged between 5 mΩ and 6 mΩ. This magnitude fitted the result obtained in the long-time EM testing, which was between 3.5 mΩ and 5 mΩ. Since the increase in microbump resistance was affected by the control of bump height during fabrication, this range was quite reasonable.

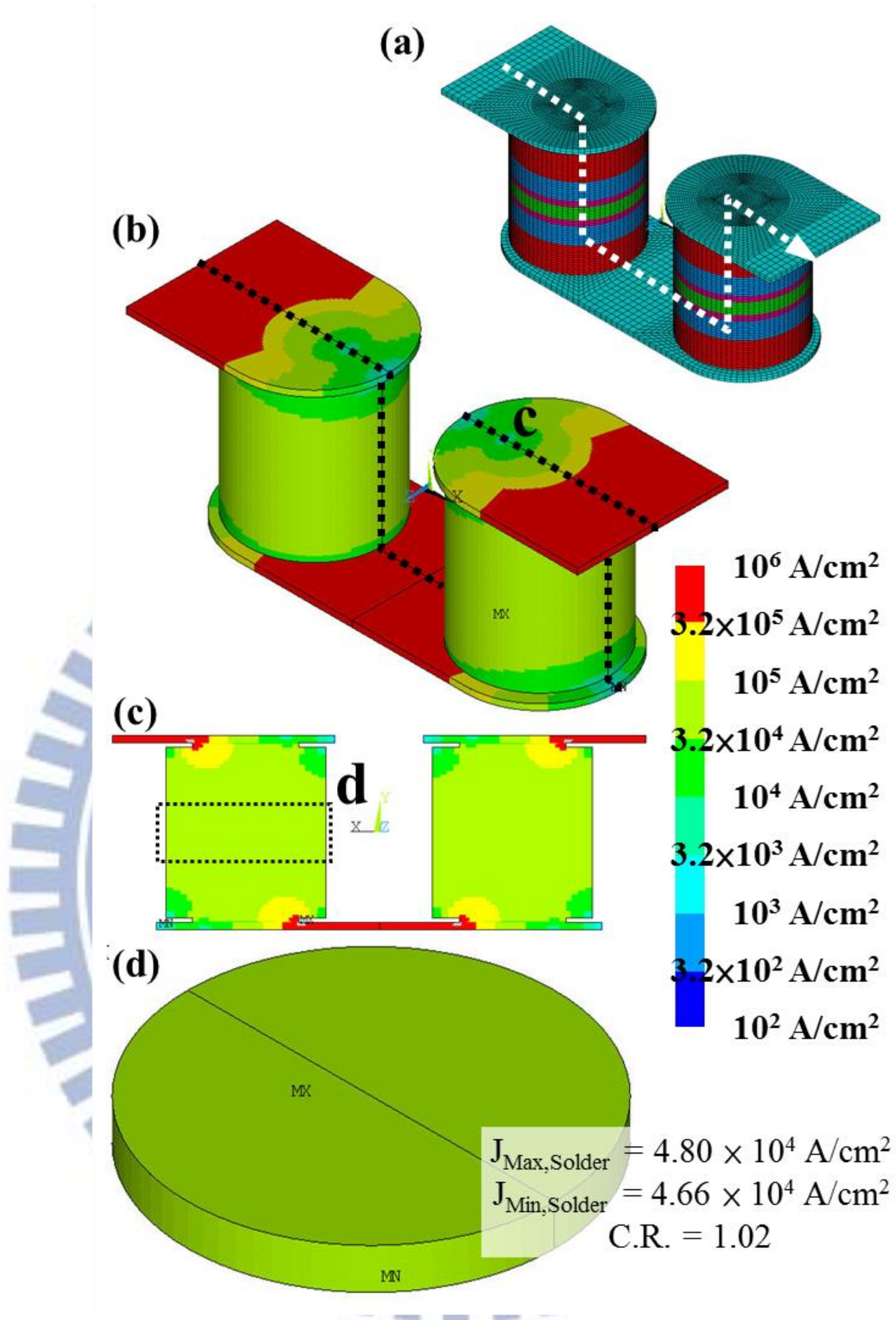


Figure 3-18 (a) Oblique view of entire model and (b) oblique view of current density distribution of 6-μm microbumps; (c) current density distribution of cross-section marked as “c” in (b); and (d) oblique current density distribution of cross-section marked as “d” in (c).

$R_{Al\ trace}$	$R_{b,0}$	$R_{b,60}$	$R_{b,120}$	$R_{b,180}$
83.7 mΩ	91.7 mΩ	52.6 mΩ	11.6 mΩ	12.1 mΩ

Table 3-3 Trace resistance and the bump resistances at different angles of a 6-μm microbump obtained using FEM.

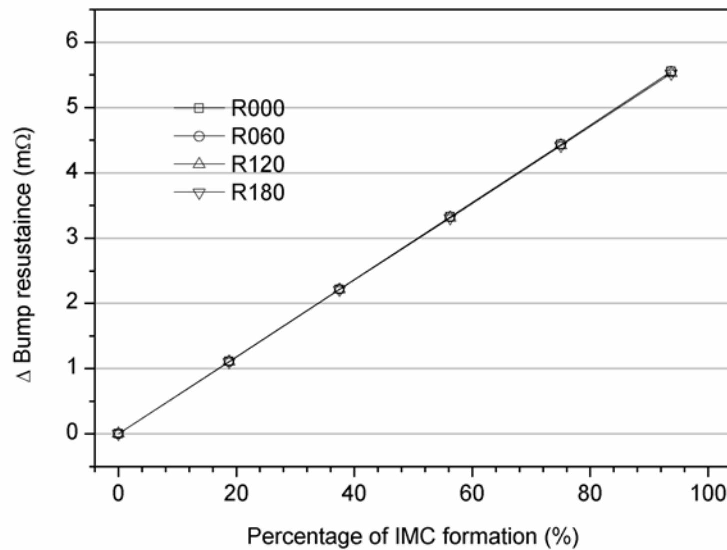


Figure 3-19 Bump resistance of a 6-μm microbump at different angles during uniform growth of IMC.

3.4.4. Finite-Element Analysis of Ten-Micro-Meter Microbumps

The cross-sectional current density distribution in 10-μm microbumps is shown in Figure 3-20. Figure 3-20 (a) and (b) displays the cross-section of the entire model and only the solder part, respectively. Unlike that of a 6-μm microbump, the structure of a 10-μm microbump was non-symmetric, and the interposer-side UBM was only 2-μm Ni. Though the chip-side UBM was ultra-thick 15-μm Cu/2-μm Ni, the thin interposer-side 2-μm Ni could not fully relieve the current crowding effect. The maximum current density appearing near the interposer side and was 3.50×10^5 A/cm^2. The CR was 3.50 (the average current density was 10^5 A/cm^2). From the result, it was obvious that the reliability under EM testing would be highly promoted when thickening the interposer-side UBM.

Moreover, the current density distribution verified the observation in the EM test results of 10-μm microbumps. In the microbump tested by the upward electron flow, the high current density near the interposer side caused the 2-μm Ni quickly to dissolve into the solder and form IMC. In the microbump tested by the downward electron flow, the current density was relieved, thus causing relatively slighter damage to the microbump.

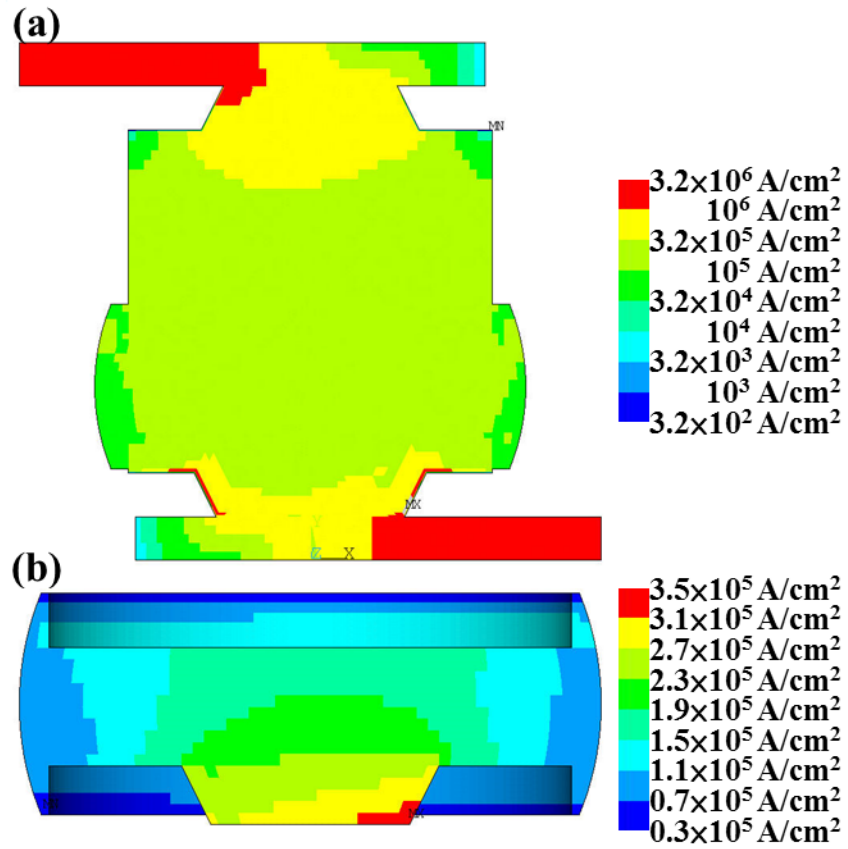


Figure 3-20 Cross-sectional current density distribution of (a) entire model and (b) solder part in 10-μm microbump.

Chapter 4. Discussion

4.1. Bump Resistance of Flip-Chip Bumps

According to the results obtained in sections 3.1.1 and 3.1.2, the void depletion area and the bump resistance of flip-chip bumps could be schematically shown as Figure 4-1. The resistance equals to the resistivity multiplied by the length and divided by the conducting area, which is R = ρL/A. In the initial stage, there was no void, so the R0 could be expressed as follows:

$$R_0 = \frac{\rho L}{A_{ubm}} \qquad \text{Equation 4-1}$$

During EM testing, the void grew gradually and finally occupied the entire UBM opening, so the maximum void depletion area equals the area of UBM. In the process, the depletion area could be expressed as

$$A = A_{ubm} - \exp[-(t - t_0)] \qquad \text{Equation 4-2}$$

Moreover, the un-depleted area was defined as $\bar{A}$, which equaled

$$\bar{A} = A_{ubm} - A \qquad \text{Equation 4-3}$$

With Equation 4-3, the bump resistance became $R(\bar{A})$, and $R(\bar{A})$ equaled

$$R(\bar{A}) = \frac{\rho L}{\bar{A}} = \frac{\rho L}{A_{umb} - A} = \frac{\rho L}{A_{umb}}\left(\frac{A_{umb}}{A_{umb} - A}\right) \qquad \text{Equation 4-4}$$

From Equation 4-4, $R(\bar{A})$ became

$$R(\bar{A}) = R_0\left(\frac{1}{1 - \frac{A}{A_{umb}}}\right) \qquad \text{Equation 4-5}$$

With Equation 4-2, Equation 4-5 was transformed into

$$\frac{R(\bar{A})}{R_0} = \frac{1}{1 - \frac{1}{A_{ubm}}\left[A_{ubm} - e^{-(t-t_0)}\right]}$$

$$\frac{R(\bar{A})}{R_0} = A_{ubm}\exp(t - t_0) \qquad \text{Equation 4-6}$$

There was a boundary condition. For time, t, equaled 0, $R(\bar{A}) = R_0$. With this boundary condition, Equation 4-6 became

$$1 = A_{ubm} \exp(-t_0)$$

$$t_0 = \ln A_{ubm} \qquad \text{Equation 4-7}$$

From Equation 4-7, the void depletion area and the bump resistance became

$$A = A_{ubm} - \exp[-(t - \ln A_{ubm})] \qquad \text{Equation 4-8}$$

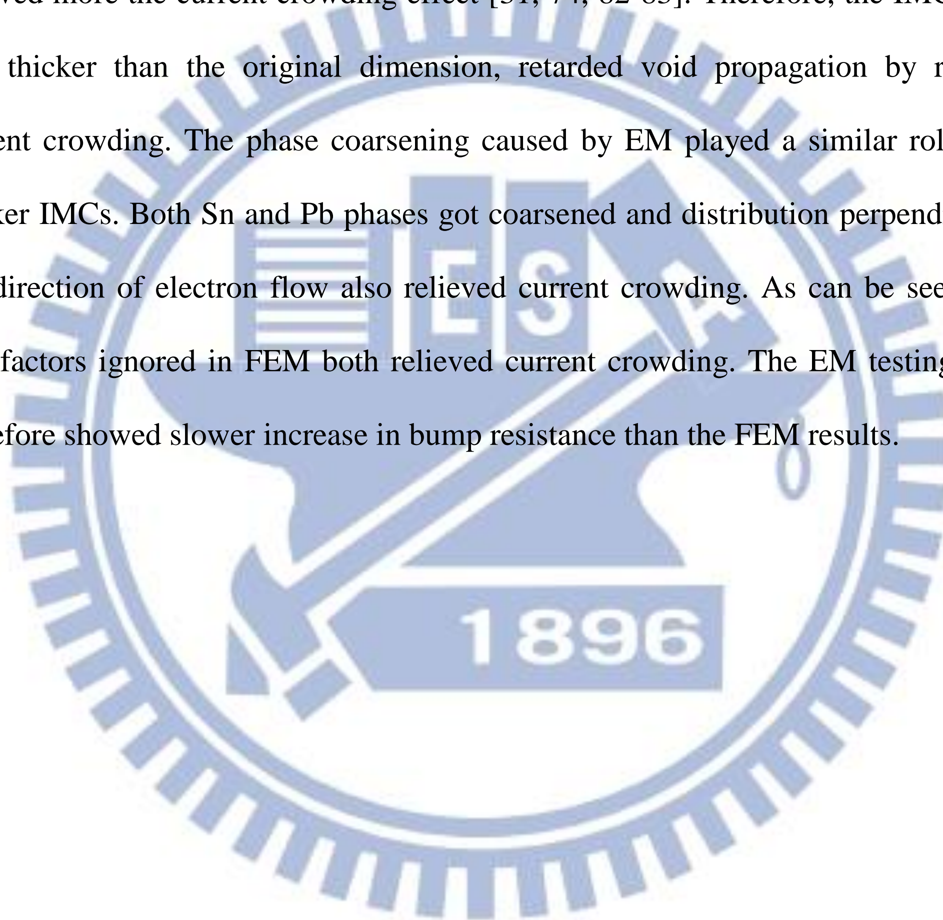
$$R(\bar{A}) = \rho L \exp(t - \ln A_{ubm}) \qquad \text{Equation 4-9}$$

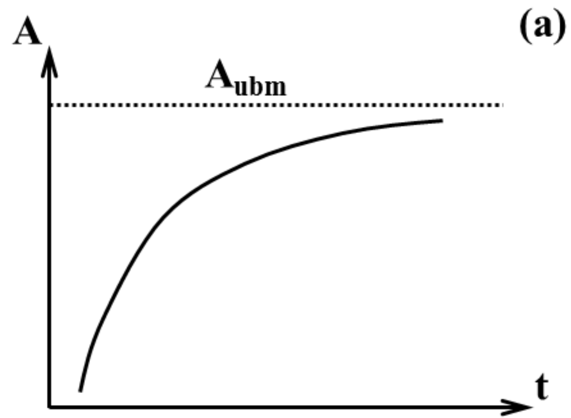
Equation 4-9 fitted the behavior shown in Figure 4-1 (a). The entire derivation indicated the relation between void depletion and increase in bump resistance. The void depleted during EM testing and confined the area conducting current. Although the phase coarsening at the end stage did delay the EM failure, as shown in section 3.1.2, the relation between the remaining contact area and increase in bump resistance was obvious.

Moreover, a lot of previous studies used resistance to monitor the samples [13, 16, 34, 37, 39, 41-44, 47, 49, 51]. However, the circuit resistance was not able to correctly reflect the microstructure evolution during EM testing. It was said that void nucleation happened near the end stage according to the increase in circuit resistance. In this study, it was found that the resistance caused by void nucleation was actually only a few milli-ohms, which could not be detected by circuit resistance. Therefore, the Kelvin bump structures proved to be very helpful and necessary in the subsequent research on flip-chip bumps.

Furthermore, void nucleated at a very early stage during EM testing. In this study, the void took only 5% of the total testing time to nucleate. The rest 95% of time was for the void to propagate, which was significantly different from previously reported. As a result, to enhance EM reliability involved not only preventing void nucleation but also retarding void propagation.

Comparison of bump resistances obtained by FEM and EM testing showed the same trend, though increase in resistance obtained from the Kelvin bump structures was slower than that yielded by FEM. The reason for such difference was that FEM ignored two very important factors: simultaneous IMC growth and phase coarsening during EM testing. In FEM, the IMC thickness remained constant throughout the process. However, the thickness in fact kept increasing. The thicker UBMs and IMCs relieved more the current crowding effect [31, 74, 82-83]. Therefore, the IMC, which was thicker than the original dimension, retarded void propagation by relieving current crowding. The phase coarsening caused by EM played a similar role as the thicker IMCs. Both Sn and Pb phases got coarsened and distribution perpendicular to the direction of electron flow also relieved current crowding. As can be seen, these two factors ignored in FEM both relieved current crowding. The EM testing results therefore showed slower increase in bump resistance than the FEM results.





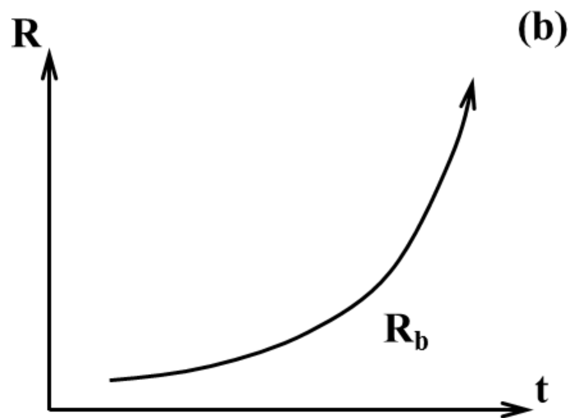


Figure 4-1 (a) Schematic void depletion area of flip-chip bumps; and (b) schematic bump resistance of flip-chip bumps.

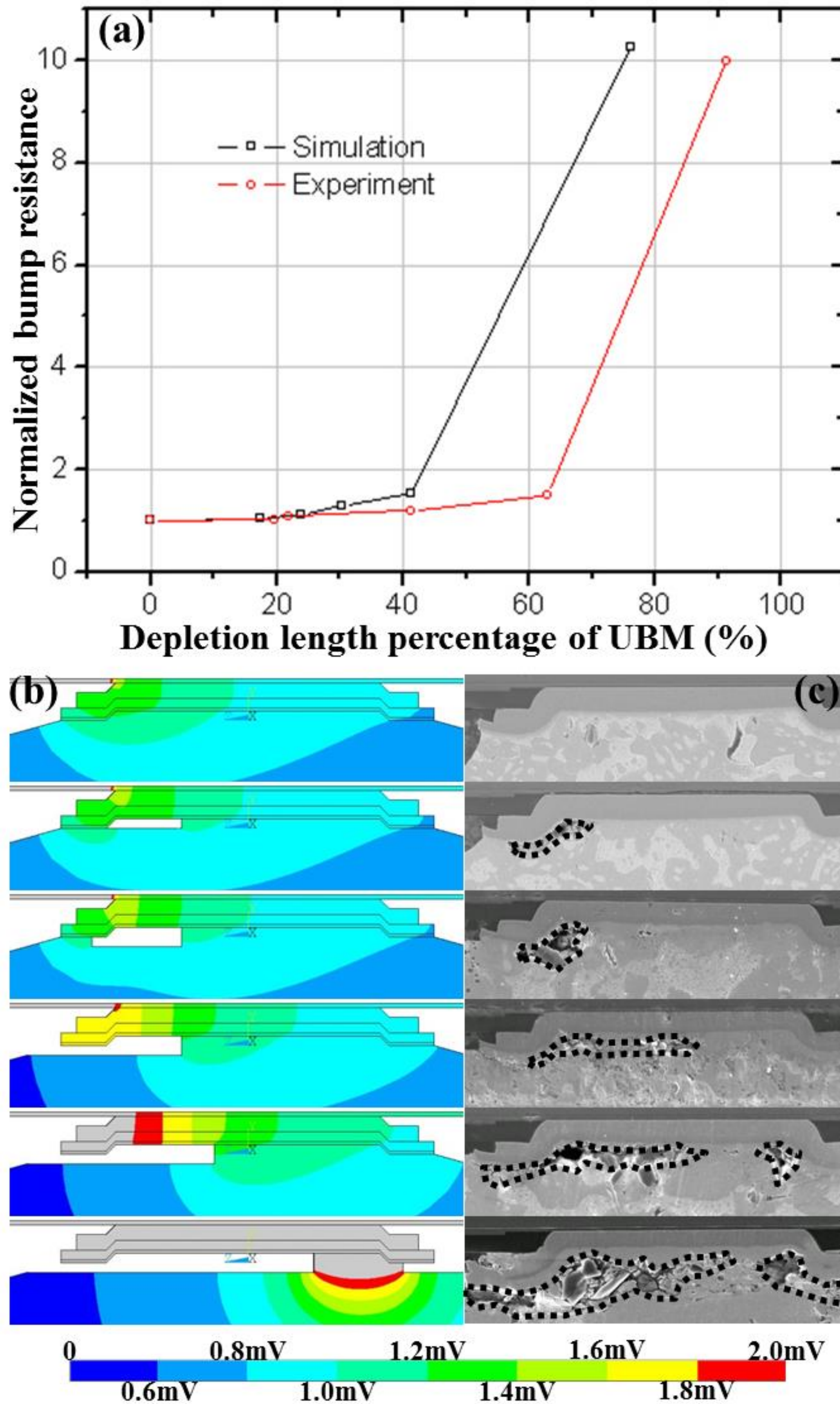


Figure 4-2 (a) Bump resistance curves obtained from FEM and Kelvin bump structures; (b) cross-sectional voltage distribution in FEM; and (c) cross-sectional microstructure at different stages of void propagation.

4.2. Secondary Void Formation near End Stage of Electromigration Testing

Another interesting phenomenon found in flip-chip bumps during EM testing was secondary void formation near the end stage of testing. As shown in Figure 4-2 (c), secondary void formation looked abnormal at the first glance but was actually reasonable according to the X-ray images and the FEM results. The X-ray images showed the void (white region in the UBM opening) first generated near the entrance point of electron flow, which was also the current-crowding spot. Then the void expanded toward the low-current-density region from the two wings. Near the end stage of testing, the two wings overlapped, and the high-current-density regions, the green part in Figure 4-3 (c1) and the light green part in Figure 4-3 (d1), surrounded the remaining contact area. Once the samples were polished along the vertical central line as shown in Figure 4-3 (a1), (b1), (c1), and (d1), the circular voids crossing the central line by two points looked like two split voids in the cross-section. There were two reasons causing this phenomenon: the shape of solder bumps and the relation between the Al trace and the UBM.

Owing to surface tension, the solder bumps usually looked like a ball. The diameter and the area in the center of the solder were larger than those of the UBM opening. Once the current flowed through the IMC and got into the solder, the current tended to spread out more because of the larger area in the center. The current density near the surrounding edge became larger than that in the center. Therefore, the shape of the high-current-density region, the green part in Figure 4-3 (b1), appeared like a pair of horns. This combined with the reason discussed below caused the split of void at the end stage of EM testing.

During sample fabrication, the area of Al pad had to be larger than that of the

passivation opening to prevent direct contact of the Cu UBM with the Si chip. Once Cu diffused into the Si chip, Cu silicide was formed, thus affecting the properties of the internal electric devices. Usually it was a very important design rule that the Al pad should be larger than the passivation opening, and the passivation opening should be within the range of Al pad. Because of this design, the edge of Al pad provided extra routes for electron flow rather than directly getting into the solder bump, as shown in Figure 4-4. The extra routes helped relieve current crowding by spreading the entrance from a point to a range and caused the circular void as well. This effect was enhanced when the thickness increased, or the gap between the Al pad and the passivation became larger.

Since the design rule is a must and surface tension cannot be avoided, the split of void always occurs near the end stage of EM testing. This phenomenon may mislead the estimation of void depletion rate because the growth rate becomes nonlinear in the cross-section. The plan-view X-ray images can be a very important tool for analyzing the behavior of void growth.

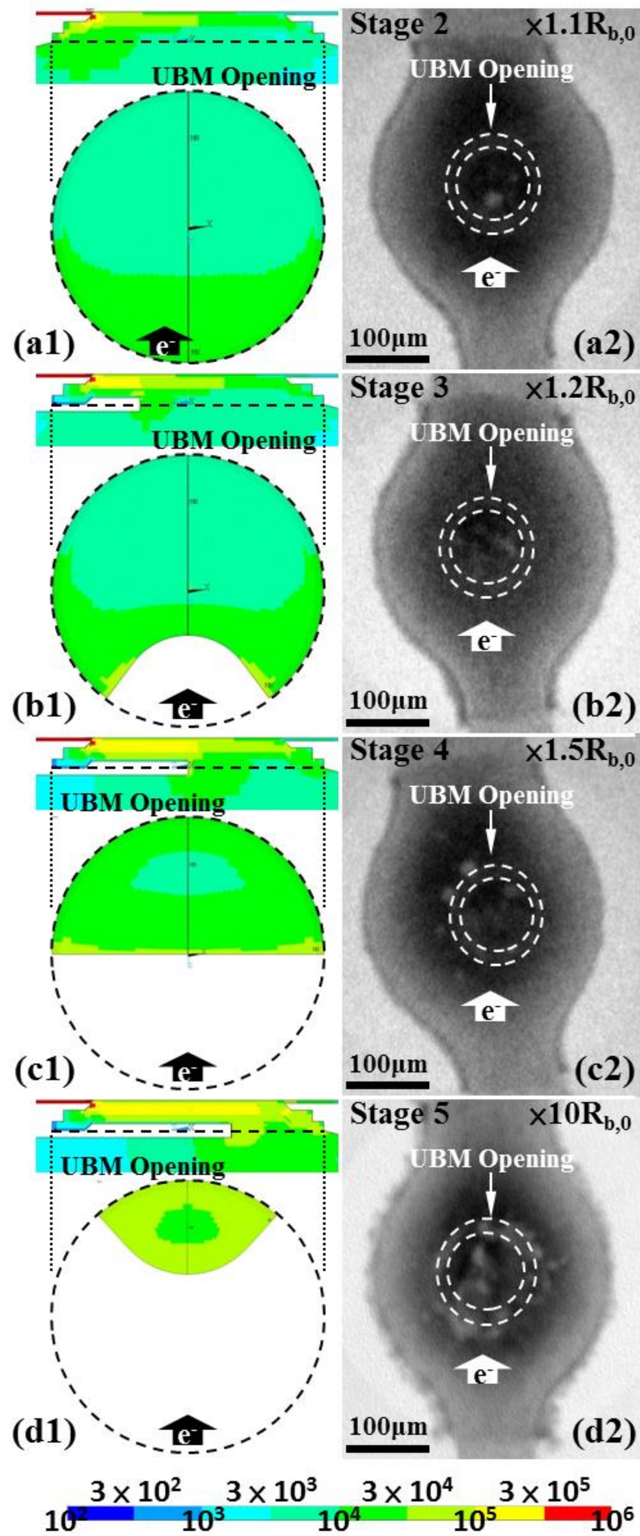


Figure 4-3 Plan-view current density distribution of UBM opening and plan-view X-ray images at (a) stage 2, (b) stage 3, (c) stage 4, and (d) stage 5 during EM testing.

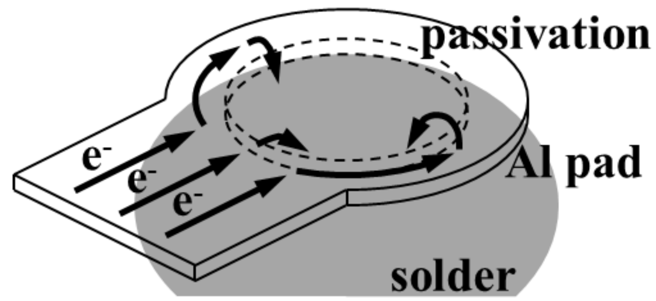
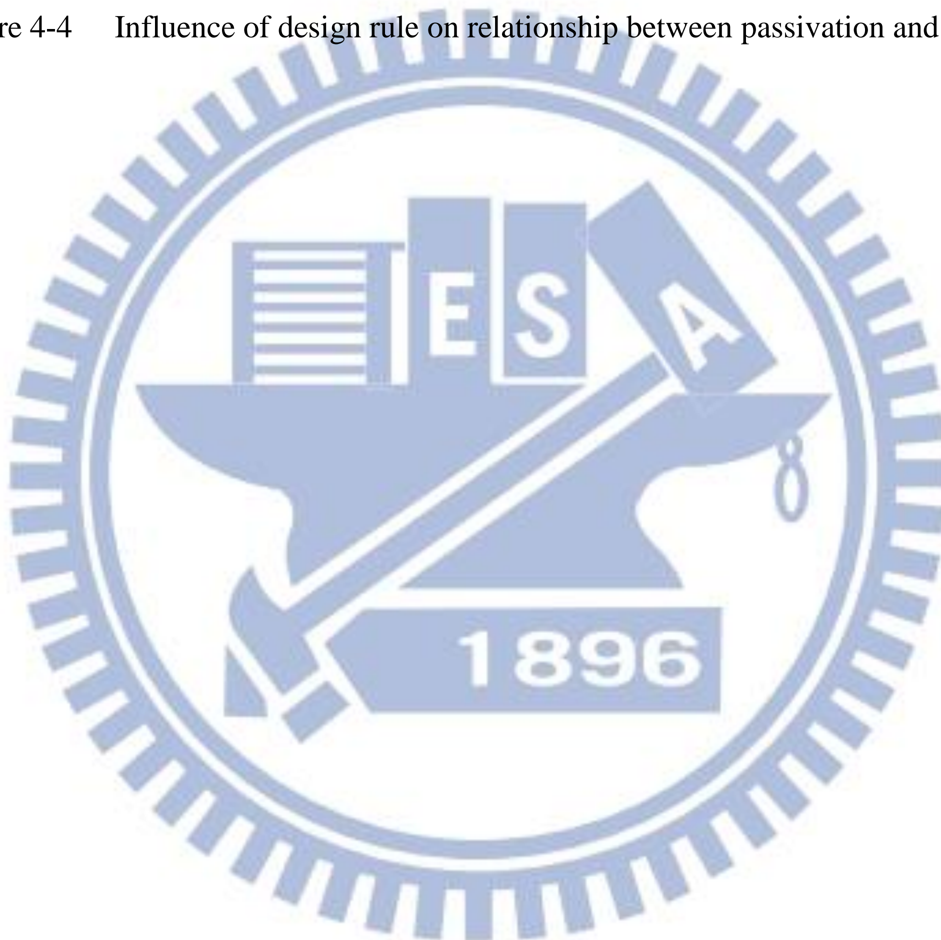


Figure 4-4 Influence of design rule on relationship between passivation and Al pad.



4.3. Bump Resistance of Six-Micro-Meter Microbumps

For simplicity of description on the bump resistance of 6-μm microbumps, a numerical model was derived section in 2.6. The bump resistance and the CR were simplified as $\sqrt{2\overline{R_x} \cdot \overline{R_y}}$ and $\sqrt{2\,\overline{R_x}/\overline{R_y}}$, respectively. On the one hand, in terms of bump resistance, the increase in both $\overline{R_x}$ and $\overline{R_y}$ brought about the increase in bump resistance. On the other hand, in terms of CR, the increase in $\overline{R_x}$ and the decrease in $\overline{R_y}$ caused the current to get directly into the solder rather than spread first.

The microbump resistances with different Al trace thicknesses obtained using Kelvin bump structures, FEM, and the numerical model are shown in Figure 4-5. The results of the numerical model matched the trends of Kelvin bump structures and FEM results. Nevertheless, these results all show that a microbump with a thicker Al trace has a lower resistance. When the thickness of Al trace was increased from 0.8 μm to 3 μm, the calculated microbump resistance decreased from 90 mΩ to 30 mΩ. The curves of FEM and the numerical model overlap when the thickness of Al trace is less than 0.8 μm, but split when the Al trace is thicker than 0.8 μm. The difference between FEM and the numerical model becomes more significant when the Al trace becomes thicker. Such difference is due to the assumption of the existence of serious current crowding at the interface of the traces and the solder joint.

The numerical model included two important assumptions. First, once the current gets into the solder, it does not redistribute anymore, but it does in the real case. This assumption makes the model imprecise when the current density redistribution is obvious in the solder. Usually this occurs in the case with very high solder. On the contrary, the numerical model works excellent when the solder height is low. The same is true for the thin Al trace. Second, the numerical model assumes the structure

to be vertically symmetrical, which is rare in flip-chip samples. However, this is the case for the 6-μm microbump samples in this study. During microbump fabrication, the COC process became very general due to the requirement for high precision. The symmetrical structure is going to be more common in COC because this can simplify the process. Although the model was not useful in the studies of flip-chip bumps, it could be useful when studying microbump samples. In addition, the numerical model gave a general idea on how the structure affected bump resistance and CR.

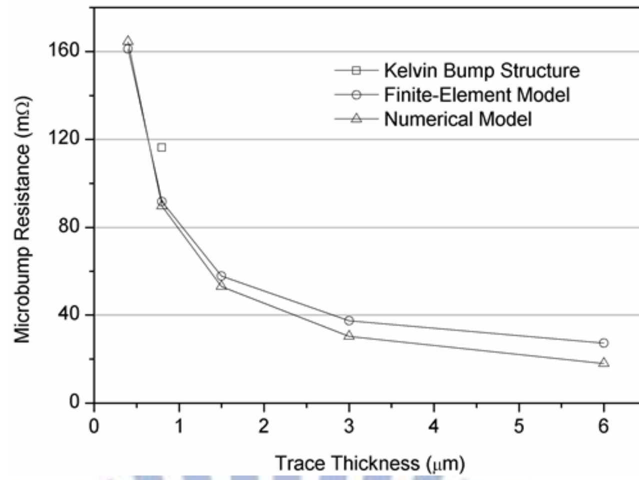
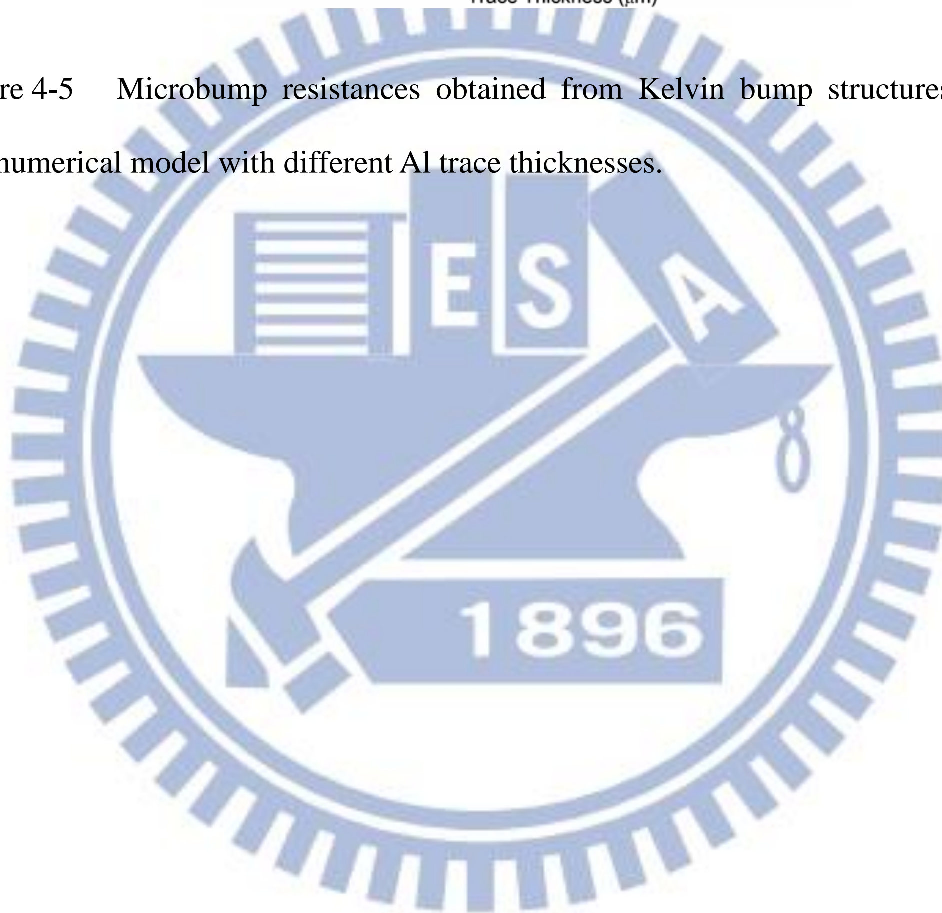


Figure 4-5 Microbump resistances obtained from Kelvin bump structures, FEM, and numerical model with different Al trace thicknesses.



4.4. Relation between Bump Resistance Behavior and Microstructure Evolution

There were three kinds of bump resistance behaviors introduced in sections 3.1.1, 3.2.1, and 3.3.1. They were the concave-up curve, concave-down curve, and concave-down-then-up curve. The corresponding microstructures were void propagation, IMC growth, and IMC growth followed by void formation.

The concave-up bump resistance curve refers to the microstructure evolution of remaining contact area confined by void propagation. The bump resistance is described as a function of remaining contact area obtained in section 4.1, $R(\overline{A}) = \rho L \exp(t - \ln A_{ubm})$. On the contrary, the concave-down bump resistance curve refers to the microstructure evolution involving formation of high-EM-resistance materials, which are usually the IMCs in the Sn-Cu-Ni system. The volume (height) ratio between UBM and the solder governs whether the concave-down resistance curve reaches the constant value. During EM testing, the reaction is usually enhanced at the cathode side but retarded at the anode side. Once the solder volume becomes too big for the cathode-side UBM to consume, IMC formation cannot reach a point for the reaction to stop. In this case, the corresponding bump resistance cannot become a constant, and vice versa. If the solder volume is too small, the entire solder bump will be transformed into IMC bumps. Then the EM failure time of the IMC bumps gets extremely prolonged. If the solder consumes the entire cathode-side UBM, the void forms at the original position of cathode-side UBM and causes the concave-up resistance curve to appear again. The relation between bump resistance curve behaviors and microstructure evolutions thus becomes clear.

What was the failure mechanism in the microbump with low solder volume (height)? Owing to high EM resistance, failure would occur in the traces instead of the

IMC [80]. Even in microbumps, the cross-sectional area of the trace was still smaller than that of bumps by 14 times. If the current density in the microbump reached 10^5 A/cm^2, the one in the trace reached 1.4×10^5 A/cm^2. For Al, this current density was large enough to cause EM. The study of Ouyang et al. observed clearly this EM failure in the trace. Therefore, it becomes necessary to thicken the trace in the 6-µm microbump case. Thickening the trace not only reduces the current density within but also relieves current crowding at the interface between the trace and the UBM.

4.5. Effect of Solder Height on Microstructure Evolution

From the results presented in Chapter 3, solder height affected significantly microstructure evolution during EM in the bumps by controlling the linkage between IMCs. In the case of flip-chip bumps in this study, the solder height was around 25 µm. According to the microstructures in Figure 3-2, the IMC grew during EM testing, but the solder was too high for the chip-side and the substrate-side IMCs to come in contact with each other. At the same time, void nucleated at the IMC-solder interface, which becomes a flux divergence site. Overall, the EM failure mechanism in flip-chip bumps involved void nucleation and then propagation because the IMC growth was relatively not obvious. The corresponding bump resistance curve behaved concave-up as a result.

When the solder height decreased to 10 µm, which was an intermediate height, the EM failure mechanism changed into a mixture of IMC growth and void propagation. Figure 3-12 illustrates this mixed EM failure mechanism in 10-µm microbumps. Since the IMC, Ni_3Sn_4, was of scallop shape, some of the IMCs on the chip-side and the interposer-side came into contact with each other even when the solder was not yet fully transformed into IMC. The IMC is a high-EM-resistance material. Once the IMC linkage between the chip-side and the interposer-side was

formed, the rate of increase in bump resistance became a constant. However, the interposer-side Ni UBM was only 2 μm thick. The 10-μm solder was taller than the critical solder height, 6.52 μm, of 2-μm Ni [79]. Therefore, the void still formed after the interposer-side Ni was fully consumed. This mixed EM failure mechanism in 10-μm microbumps caused the corresponding microbump resistance curve to behave concave-down in the beginning and then concave-up toward the end of testing.

Furthermore, when the solder height decreased to only 6 μm, the EM failure mechanism changed to IMC growth. In the case of 6-μm microbumps, the chip-side and the interposer-side Ni UBM were both 3 μm thick, and the corresponding critical solder height was 9.78 μm. Because the critical height exceeded the solder height, the cathode-side Ni could completely consume the solder and transform the solder bumps into IMC bumps, as shown in Figure 3-8. Owing to the high EM resistance in the IMC, the microstructure did not significantly change after the bumps were transformed into IMC bumps. Therefore, the microbump resistance increased markedly in the beginning and then maintained at a constant value after a period of testing.

Since the Ni layer was often viewed as a diffusion barrier between Cu and solder, the thickness of Ni could not be too thick. The most common thickness was around 2 μm to 3 μm, and the corresponding critical solder height ranged from 6.52 μm to 9.78 μm. Therefore, this range could also be thought as a critical of the EM failure mechanism. When the solder height was obviously greater than 10 μm, the EM failure mechanism of the solder bump involved both void nucleation and propagation. Once the solder height decreased to 10 μm, the mechanism gradually changed involving both void propagation and IMC growth instead. The IMC grew in the beginning and the void formed at the interface between IMC and solder near the end stage of testing. If the solder height was smaller than 6 μm, the cathode-side Ni completely consumed

the solder. IMC growth and UBM dissolution dominated the EM failure mechanism. These different EM failure mechanisms corresponded with different bump resistance curve behaviors.

4.6. Effect of Magnitude of Applied Current on Microstructure Evolution

Along with the solder height, the different applied currents also caused different failure mechanisms, as shown in Figure 3-8 and Figure 3-9. When low current (4.6×10^4 A/cm^2) was applied, IMC growth was the main EM failure mechanism. On the contrary, the void formation became the main EM failure mechanism under the application of high current (9.2×10^4 A/cm^2). The same trends were also observed in some previous studies [84]. The changing of EM failure mechanism came from two driving forces: EM and interfacial reaction. When the current was doubled, the flux from the interfacial reaction maintained the same, but the magnitude of flux from the EM also doubled, thus changing the EM failure mechanism, which merits further discussion and exploration.

4.7. Integration between Kelvin Bump structures and Daisy Chain Structure

From the analyses in the previous chapters, it was found that both Kelvin bump structures and bump resistance curves were very important. Moreover, the Kelvin bump structures were totally comparable to the daisy chain structure, which has been applied for a long time in the research on EM [85]. In the process this study, our group applied for a patent about combining the Kelvin bump structures and the daisy chain structure. Since the high-precision automatic measurement system was established,

the resistance of daisy chain can be viewed as a pair of monitoring nodes, thus enabling easy monitoring. The results shown in Figure 3-1 demonstrate this advantage. The bump resistance in Figure 3-1 (a) and the daisy chain resistance in Figure 3-1 (c) could be obtained simultaneously.

Chapter 5. Conclusions

In this study, three types of solder bump samples within pre-designed Kelvin bump structures were applied to monitor non-destructively the microstructure evolution inside the bumps during EM testing.

The first type of sample was flip-chip bumps. The bump resistance was found to be less than 1 mΩ and increase as a concave-up curve. After the bump resistance increased to more than 10 times its initial value, it started to rapidly grow and then fail. The corresponding microstructure was void nucleation and propagation. The void was first formed near the current-crowding spot and then grew along the interface between the IMC and the solder. At the end stage of EM testing, phase coarsening caused by EM retarded the failure, and the void split into two parts as seen in the cross-sectional SEM images. The split was due to the spherical shape of the solder and design rule of Al pad, causing the high-current-density region to surround the low-current-density one. The void therefore became circular and was found split when the samples were polished to the center. The relation between the remaining contact area and the bump resistance could be expressed as $R(\overline{A}) = \rho L \exp(t - \ln A_{ubm})$, where ρ is the resistivity, L is the effective bump height, t is the stressing time, and the A_{ubm} is the area of UBM opening.

The second type of sample was 6-μm microbumps sample. The microbump resistance behaved concave-down, starting between 11 mΩ and 17 mΩ, increasing rapidly in the beginning, then slowing down, and finally reaching a constant value after 400 hr of testing. The increase in the early stage of testing ranged between 3.5 mΩ and 5.0 mΩ, which was reasonable when compared with the FEM results. The bump resistance reached the constant value and behaved concave-down because the

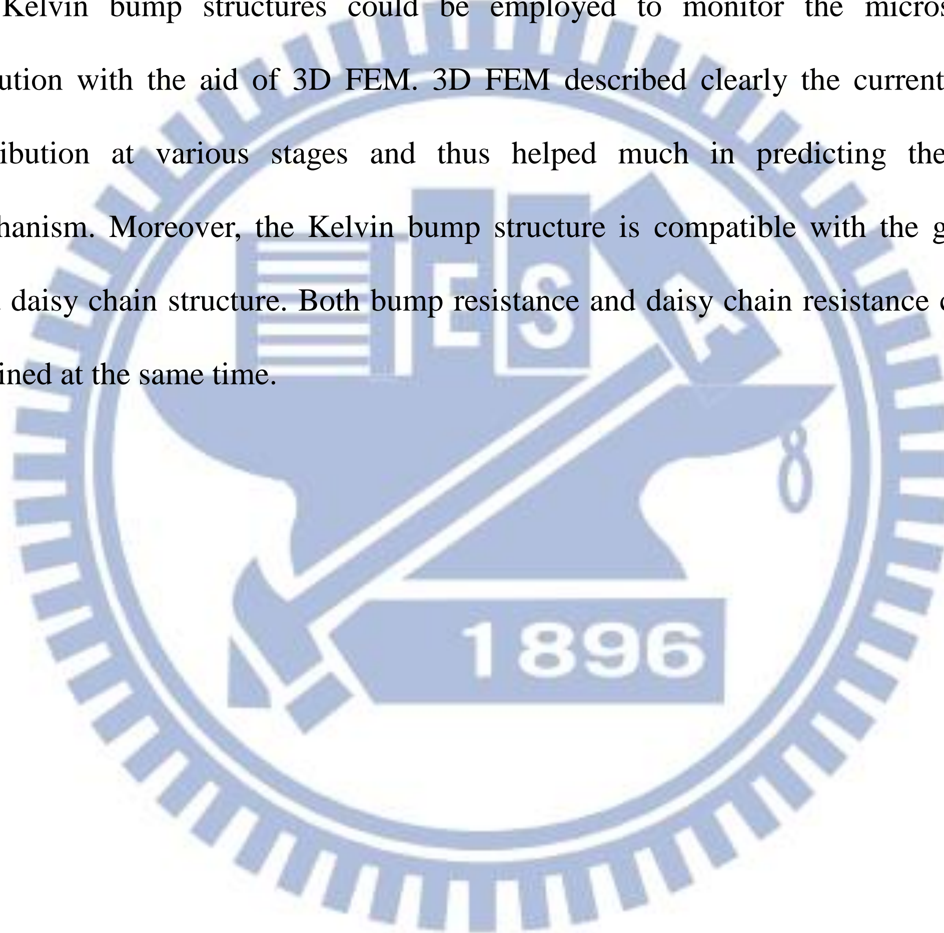
volume (height) was too low. During EM testing, the cathode-side UBM reacted with the solder and transformed the entire microbump into Ni_3Sn_4, which has better EM resistance than the solder. Once the entire solder got transformed into IMC, the reaction approached the stopping point and caused the bump resistance to remain constant. The bump resistances at different angles indicated current crowding still taking place, but in the Cu UBM and not in the solder. The complete voltage drop across the microbump was the value obtained at 0°. However, the bump resistance obtained at 0° was 7 times larger than that at 180°. That is, the RC delay caused by microbump is actually very large. For simplicity of description on the relation between microbump resistance, crowding ratio, and structural dimensions, a numerical model was built. The microbump resistance and the crowding ratio were $\sqrt{2\overline{R_x}\cdot\overline{R_y}}$ and $\sqrt{2\,\overline{R_x}/\overline{R_y}}$ respectively. It was suitable for a vertically symmetrical structure with low bump height and thin trace, which was the 6-μm microbump used in this study.

The last type of sample was 10-μm microbumps. The resistance behaved first concave-down and then concave-up because the solder height was too high for the interposer-side UBM to consume. In the beginning, the concave-down curve was observed for the same reason as the low-bump-height case. However, the volume (height) of solder was around 10 μm, which was too high for the interposer-sider UBM to react with. When the electron flow upward (from interposer to chip), the interposer-side UBM, 2-μm Ni, was the cathode side. Driven by EM, the 2-μm Ni quickly dissolved into the solder. After the 2-μm Ni ran out, the void was formed, causing the bump resistance curve to behave concave-up again.

The solder height affected significantly the failure mechanism. In flip-chip bumps, the solder height was around 25 μm. The solder height was obviously larger than the

critical reaction height, so void nucleation and propagation constituted the main failure mechanisms. When the solder height decreased to 10 μm, the mechanism became the mixture of void propagation and IMC growth because 10 μm was close to the critical reaction height. When the solder height was decreased to 6 μm, it became smaller than the critical value, and the failure mechanism changed to IMC growth.

According to the obtained results, the behaviors of bump resistances obtained by the Kelvin bump structures could be employed to monitor the microstructure evolution with the aid of 3D FEM. 3D FEM described clearly the current density distribution at various stages and thus helped much in predicting the failure mechanism. Moreover, the Kelvin bump structure is compatible with the generally used daisy chain structure. Both bump resistance and daisy chain resistance could be obtained at the same time.



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Chapter 7. Publication List

A. Journal as first author

A.1 **Y. W. Chang**, S. H. Chiu, Chih Chen, and D. J. Yao, "Effect of Si-die dimensions on electromigration failure time of flip-chip solder joints." *Materials Chemistry and Physics* 127.1 (2011): 85-90.

A.2 **Y. W. Chang**, S. H. Chiu, and Chih Chen, "Investigation of Void Nucleation and Propagation in the Joule Heating Effect During Electromigration in Flip-Chip Solder Joints." *Journal of electronic materials* 39.11 (2010): 2489-2494.

A.3 **Y. W. Chang**, H. Y. Peng, R. W. Yang, Chih Chen, T. C. Chang, C. J. Zhan, J. Y. Juang, and Annie T. Huang, "Analysis of bump resistance and current distribution of ultra-fine-pitch microbumps." *Microelectronics Reliability* (2012).

B. Conference Paper as first author

B.1 **Y. W. Chang** and Chih Chen, "Design of Al pad geometry for reducing current crowding effect in flip-chip solder joint using finite-element analysis." *Thermal, Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE), 2010 11th International Conference on*. IEEE, 2010.

B.2 **Y. W. Chang** and Chih Chen, "Optimal design of passivation/UBM openings for reducing current crowding effect under electromigration of flip-chip solder joint." *Electronics Packaging Technology Conference, 2009. EPTC'09. 11th*. IEEE, 2009.

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C. Journal (and Patent)

C.1 Hsiao-Yun Chen, Han-Wen Lin, Chien-Min Liu, **Yuan-Wei Chang**, Annie T. Huang, and Chih Chen, "Thermomigration of Ti in flip-chip solder joints." *Scripta Materialia* 66.9 (2012): 694-697.

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C.4 Chih Chen, Hsiang-Yao Hsiao, **Yuan-Wei Chang**, Fanyi Ouyang, and K.N. Tu, "Thermomigration in solder joints." *Materials Science and Engineering: R: Reports* (2012).

C.5 Chih Chen, and **Yuan-wei Chang**, "STRUCTURE FOR MEASURING BUMP RESISTANCE AND PACKAGE SUBSTRATE COMPRISING THE SAME." U.S. Patent No. 20,120,268,147. 25 Oct. 2012. (Patent)

D. Conference

D.1 C. C. Wei, C. H. Yu, C. H. Tung, R. Y. Huang, C. C. Hsieh, C. C. Chiu, H. Y.

Hsiao, **Y. W. Chang**, C. K. Lin, Y. C. Liang, C. Chen, T. C. Yeh, L. C. Lin, and D. C. H. Yu, "Comparison of the electromigration behaviors between micro-bumps and C4 solder bumps." *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*. IEEE, 2011.

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D.3 Ruo-Wei Yang, **Yuan-Wei Chang**, Chih Chen, Tao-Chih Chang, Chau-Jie Zhan, and Jin-Ye Juang, "Agglomeration of Ag_3Sn compounds in microbumps during reflow for 3D-IC packaging." *Microsystems Packaging Assembly and Circuits Technology Conference (IMPACT), 2010 5th International*. IEEE, 2010.

D.4 Ruo-Wei Yang, **Yuan-Wei Chang**, Chih Chen, Tao-Chih Chang, Chau-Jie Zhan, and Jin-Ye Juang "Microstructure evolution in microbumps for 3D-IC packaging." *Microsystems Packaging Assembly and Circuits Technology Conference (IMPACT), 2010 5th International*. IEEE, 2010.