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鎳鍺化物接觸之N^+-P鍺淺接面及接觸電阻之研究

A Study on the Nickel Germanide Contacted N^+-P Germanium Shallow Junction and Contact Resistance

研 究 生： 施哲儒

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中華民國一0二年九月

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國立交通大學

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摘要

在過去幾十年內，提升矽半導體元件的特性的研究已經越來越完整。但是隨著元件快速的微縮，以矽做為半導體材料的金氧半場效電晶體很快就會因為物理極限的限制而越來越難繼續微縮下去。因此，當前的課題就是發展其他可能方法來解決這個問題。鍺由於本身的較高的載子遷移率以及和矽製程有較大的相容性而被視為能取代矽基板做為未來半導體的材料。但是N型參雜在鍺基板裡面會快速地擴散，所以好的鍺淺接面特性不容易達成，此外，由於N型鍺與金屬界面上，費米能階會被鎖定在接近價帶的位置，會產生很大的蕭基位能障而導致較大的接觸組抗。本論文主要探討利用鎳鍺化物接面來形成較淺的接面，並同時降低對N型鍺的接觸阻抗。

由於鎳鍺化物的電阻係數較其他金屬鍺化物來的低，且形成溫度也相對較低，所以選用鎳鍺化物當作接面金屬。此外，本論文中使用了兩種製程來研究接面特性，其一是形成鍺化物之前打入參雜使參雜的離子堆積在界面，另一種是形成鍺化物之後打入參雜，接著再退火使參雜離子能夠在界面離析出來。

經過形成鍺化物之前打入參雜的製程後，在濃度較高的鍺基板上植入較淺較高濃度的參雜所形成的鎳鍺接面特性並不好，主要是因為鎳原子擴散到接面的邊緣，造成大量的漏電流。然而在形成鎳鍺化物之前植入氟離子卻能夠有效的抑制

鎳原子的擴散而改善漏電流。另一方面來說，若在濃度較高的鍺基板上植入較深較低濃度的參雜，其所形成的鎳鍺接面特性較好，漏電流比前述之鎳鍺接面來的低。但是若在形成鎳鍺化物之前植入氟離子反而增進鎳原子的擴散進而造成漏電流增加。推測鎳原子的擴散深淺主要是靠植入的參雜濃度所產生的缺陷來決定。但在濃度較低的鍺基板上植入較淺較高濃度的參雜所形成的鎳鍺接面都會有好的特性，主要是因為接面深度較深而抑制鎳擴散所造成的破壞。而且就形成鎳鍺化物跟未形成鎳鍺化物的接面來比較，形成鎳鍺化物之後的接面，其順向電流都有明顯的增加，是因為在形成鎳鍺化物時，參雜的離子大量堆積在鎳鍺化物與鍺基板的界面，進而降低接觸阻抗。不論是磷參雜還是砷參雜都能看見此現象。

但在只經過形成鍺化物之後打入參雜的製程後，由於離析出來的接面深度太淺，受到鎳擴散的影響而造成大量的漏電流。因此結合以上這兩種製程，先做形成鍺化物之前打入參雜的製程然後再打入參雜後退火，能觀察到好的鎳鍺接面特性，且能同時提高順向電流。最後藉由量測接觸電阻來驗證此鎳鍺接面所觀察到的電流特性。在單純經過形成鍺化物之前打入參雜的製程的接面，其接觸電阻為 $2x10^{-5}$ 歐姆-平方公分 ； 而再打入參雜後退火的接面能使接觸電阻降到 $2x10^{-6}$ 歐姆-平方公分。

總而言之，與當今發表過的研究相比，本論文利用兩種使參雜堆積的製程來達到低接觸阻抗、低接面深度、以及好的接面特性。這個結果預期能夠改善 N 型鍺基板金氧半場效電晶體的特性。

A Study on the Nickel Germanide Contacted N^+-P Germanium Shallow Junction and Contact Resistance

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Abstract

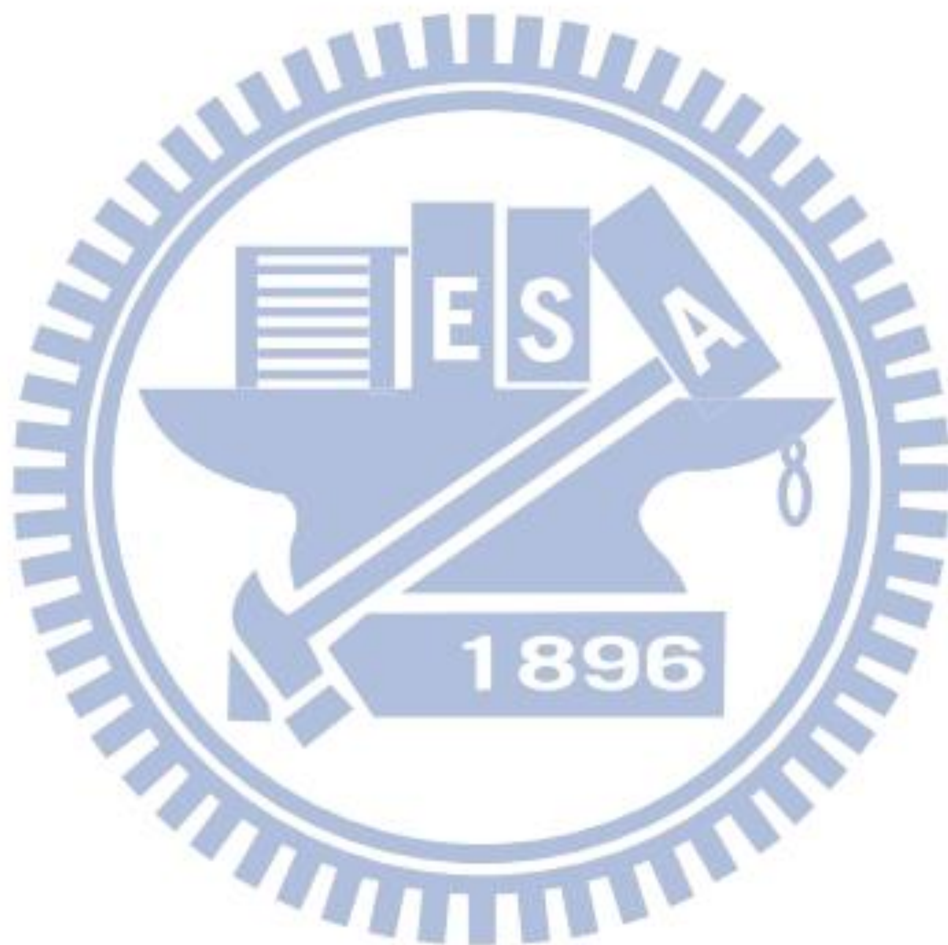
In the past several decades, the research on Si-based devices progresses very fast. Furthermore, the Si-based MOSFETs have been successfully scaled down to 20 nm regime. However, scaling down the devices becomes more and more difficult and reaches the physics limits soon. Therefore, developing another ways to promote the device performance is necessary. Using new semiconducting materials is a way to improve performance. Because germanium has higher mobility and process compatibility for MOSFET fabrication process, germanium is considered to replace Si as the channel material in the future. Nevertheless, the n-type dopant diffusion in germanium is fast so that it is not easy to form shallow n^+/p junction, and the high Schottky barrier height at the metal/n-Ge interface causes a high contact resistance due to the Fermi level pinning near the Ge valance band at the interface between metal and germanium. Therefore, the thesis would focus on the forming of shallow n^+/p-Ge junction and low resistance metal/n-Ge contact.

Because NiGe has the lowest resistivity and low temperature formation, NiGe is selected as the contact metal. The implantation before germanide (IBG) process

means ion implantation is performed before germanide formation, and the implantation after germanide (IAG) process means ion implantation is performed after germanide formation.

For the IBG junctions fabricated on heavily-doped substrate, very poor junction characteristic is observed by high dose phosphorous ion implantation due to the fast diffusion of Ni by virtue of defects which are generated by ion implantation. Fluorine ion implantation before NiGe formation could effectively suppress Ni diffusion and reduce the leakage current. Moreover, better junction characteristic can be obtained by low dose ion implantation due to the less defects resulting in less Ni diffusion. However, fluorine implantation before NiGe formation would enhance the Ni diffusion to degrade junction characteristic because the fluorine ion implantation induces extra defects. Next, on the lightly-doped substrate, good junction characteristic is more easily to be obtained than on heavily-doped substrate because the deeper junction depth on lightly-doped substrate so that the Ni diffusion would not destroy the junctions. In particular, after NiGe formation, the forward current obviously increases owing to the dopant segregation at the NiGe/Ge interface. Furthermore, either phosphorous or arsenic n^+/p junction would have the dopant segregation effect. The arsenic n^+/p junctions have relatively low activation concentration inferred by the I-V characteristic. Finally, because the IAG junctions have poor junction characteristic due to the segregated n^+ layer is too thin to maintain good n-p junction and the Ni fast diffusion induces large leakage current, the IBG+IAG process is proposed. The IBG+IAG junction could achieve shallow junction depth and raise the forward current at the same time. Furthermore, the measured contact resistance of the IBG junction is about $2x10^{-5}$ Ω-cm^2 and the lowest contact resistance of IBG+IAG junction is $2x10^{-6}$ Ω-cm^2.Therefore, this thesis has formed a junction with shallower junction depth, lower leakage current, and lower

contact resistance in comparison with previous studies. This achievement is expected to improve the performance of Ge nMOSFETs.



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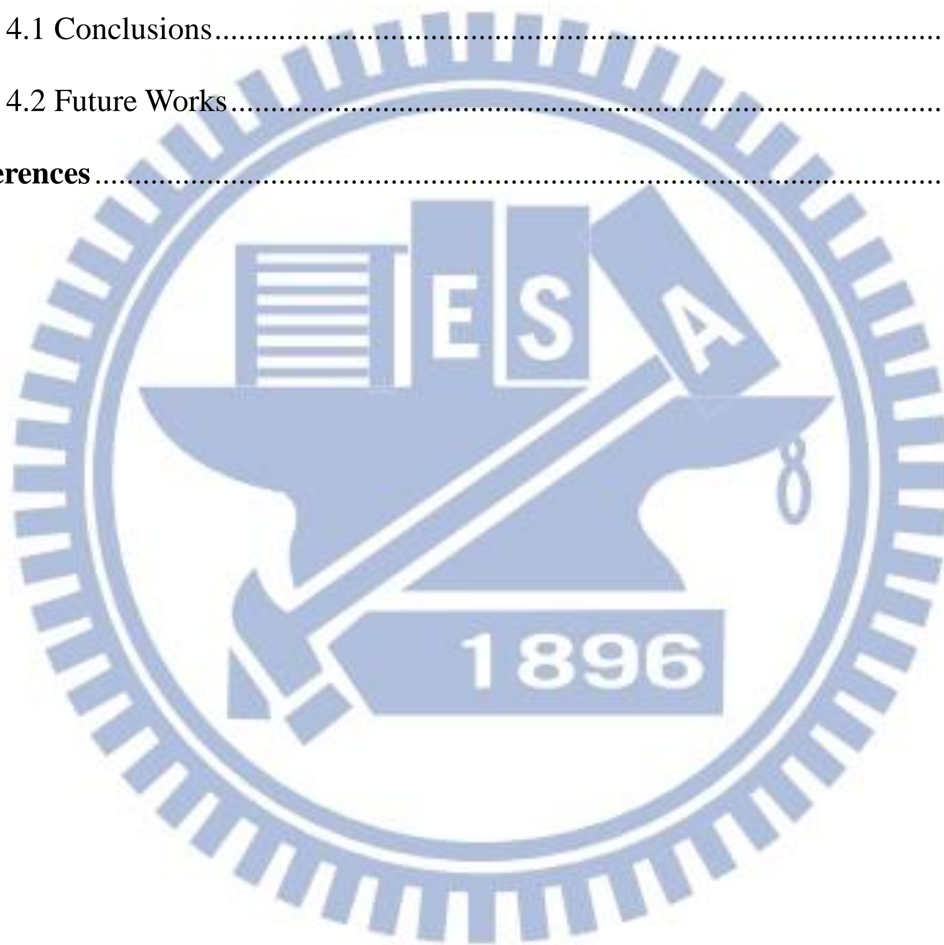

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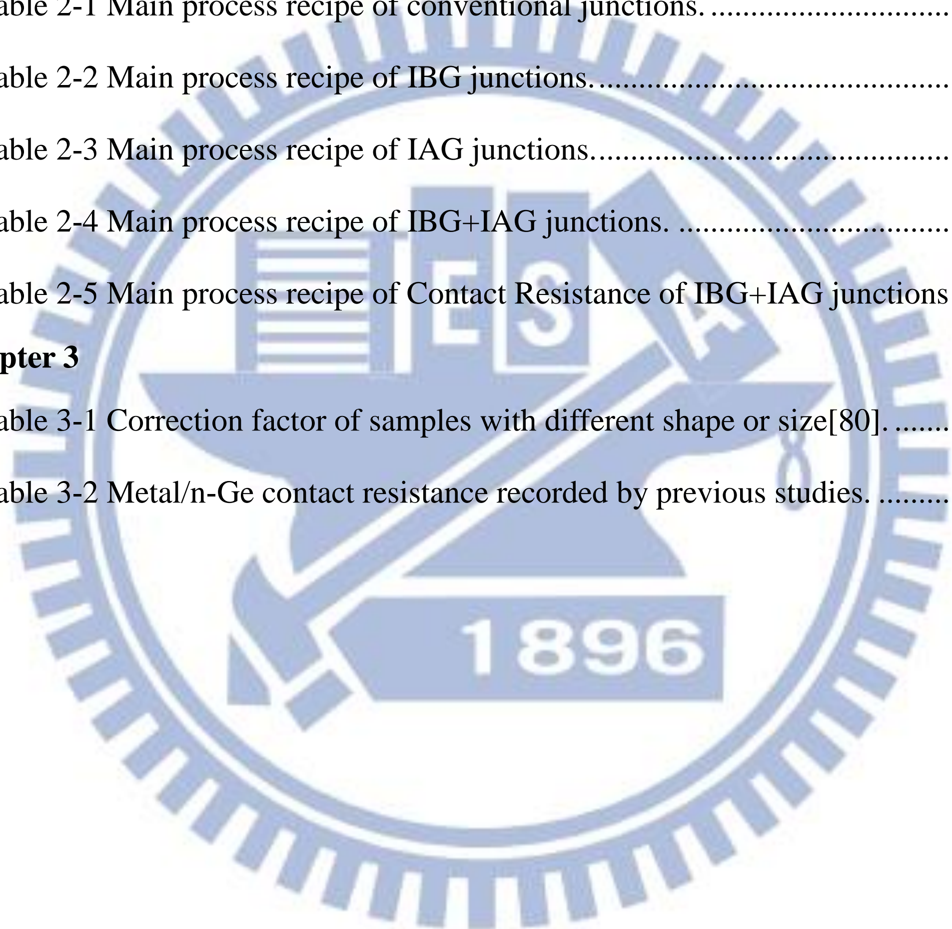

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Chapter 1
Introduction

1.1 Background of Studying Germanium

Germanium is one of the semiconducting materials in all elements. In particular, germanium is the material used to fabricate the first transistor in the world. It can be traced back to 1947, John Bardeen and Walter Brattain succeeded in inventing first transistor using bulk germanium in Bell Laboratories, and they were awarded the Nobel Prize in Physics with William Shockley in 1956. After that moment, germanium had become the principal material for solid-state devices from the 1950s to the early 1960s. However, as the development of Silicon, another semiconducting material, is gradually mature, silicon quickly replaced germanium to be the predominant semiconducting material from the late 1960s. One of the reasons for this evolution is that the wider band gap of silicon (~1.12eV) leads to lower leakage current in comparison with germanium (~0.67eV) [1]. Another reason is that silicon dioxide is physically and chemically stable but germanium oxide is water-soluble [1] so that silicon dioxide is more appropriate to form device isolation. The other reason is the low cost of silicon than germanium. For these reasons, silicon is generally used to fabricate semiconductor devices from the 1970s to the present [1].

In the past several decades, the development of semiconductor industry follows Moore's law which indicates that the number of transistors on integrated circuits doubles approximately every two years [2]. At first, the gate dielectric of silicon dioxide is replaced by high dielectric constant oxide like HfO_2. By applying high dielectric constant (high-k) materials, the thickness of gate dielectric could be

thicker than the thickness of silicon dioxide resulting in lower gate leakage current. Secondly, source and drain silicidation can lower the parasitic resistance and enhance the driving current. Therefore, the research of applying high-k materials and silicidation process has been conducted for many years. However, scaling down the devices becomes more and more difficult and reaches the physics limits soon. Therefore, developing another ways to promote the device performance is necessary. Using new semiconducting materials is the way to improve performance. Because germanium has the higher electron and hole mobility (μ_e=3900 and μ_h=1900 $cm^2 V^{-1}s^{-1}$) compared with silicon (μ_e=1400 and μ_h=450 $cm^2 V^{-1}s^{-1}$), germanium is considered to be a potential channel material in the next generation [1]. Consequently, conducting complete research of germanium MOSFET is important and it is anticipated that germanium can replace silicon to improve the device performance in the future.

Although germanium has higher mobility and process compatibility for MOSFET fabrication process, some problems are still inevitable. First of all, germanium lacks suitable clean process. RCA clean is a standard clean process for silicon. However, germanium is not suited to RCA clean because germanium oxidized fast and the germanium oxide is water-soluble so that germanium would be consumed fast in the RCA clean process. In general, HF/H_2O and HCl/H_2O are used in germanium clean process because germanium would hardly be etched by these solutions [1]. Secondly, the small band gap of germanium would induce higher junction leakage current and gate induced drain leakage (GIDL) current. Third, very high density of surface states (D_{it}) exists at the interface between gate dielectric and germanium substrate [3-5]. These surface states would induce severe Coulomb scattering and decrease the electron/hole mobility. In addition, the unstable germanium oxide is also a cause of surface states [6-8]. Furthermore, n-type dopants

diffuse fast in germanium [9-13] and the metal/n-Ge contact exhibits high contact resistance due to Fermi level pinning effect [14-16]. Dopants in germanium actually have low solid-state solubility resulting in low doping concentration [17]. For n-type dopant, the dopant diffusion is fast so that it is not easy to form shallow n^+/p junction, on the contrary, p-type dopants hardly diffuse at high temperature in germanium [18, 19]. Besides, in order to reduce parasitic resistance, metal germanide is used to form source/drain contact. However, the Fermi level is strongly pinned near the Ge valance band at the interface between metal and germanium, so the high Schottky barrier height of metal/n-Ge causes a high contact resistance.

In summary, despite the advantage of high carrier mobility in germanium, there is still some research need to be conducted for germanium MOSFET. In addition, NMOSFET has confronted more difficulties than PMOSFET [20, 21], so how to improve the germanium NMOSFET is of the first importance. To the present, some research has been conducted to reduce the surface states at the gate oxide and germanium interface, for example, germanium oxidation before gate dielectric deposition [22] and plasma recovery of interface states [23]. Furthermore, the effective oxide thickness (EOT) is also reduced to lower than 1 nm by depositing different high-k materials [24]. Table 1-1 lists the D_{it} and EOT reported in some literatures. On the other hand, the researches about the n+/p-Ge shallow junction and the contact resistance of metal/n-Ge contact are not complete [25-27]. Therefore, the thesis would focus on the forming shallow n^+/p-Ge junction and low resistance metal/n-Ge contact.

1.2 Metal and Semiconductor Contact

When metal contacts with semiconductor, either Schottky contact or ohmic contact forms. The metal work function (φ_m) is defined as the energy difference between vacuum level and Fermi level of metal; the semiconductor work function (φ_s) is defined as the energy difference between vacuum level and Fermi level of semiconductor, and χ is electron affinity. As soon as the metal and semiconductor contact intimately, according to the Einstein relation, the Fermi levels should be connected horizontally and continuous in electrostatic equilibrium. Whether it is a Schottky contact or ohmic contact is decided by the work function difference and dopants type of semiconductor. Take metal/n-type Si as an example; in the case of $\varphi_m > \varphi_s$, the Fermi level of semiconductor is higher than the Fermi level of metal. It means that the electrons in semiconductor near the interface would diffuse to metal after the two Fermi levels are aligned so that a potential barrier and a depletion region would be formed near the junction. Therefore, the Schottky barrier height can be expressed as $\varphi_{bn}=\varphi_m - \chi$. It is called a Schottky contact or rectifying contact. However, in the condition of $\varphi_m < \varphi_s$, the Fermi level of semiconductor is lower than the Fermi level of metal. After the two Fermi levels are aligned, the barrier between metal and semiconductor is small and the barrier is easily overcome by a small electrostatic potential energy. It is called an ohmic contact.

Schottky contact is like a rectifying junction and ohmic contact can be regarded as a very small resistor. What kind of contact should be formed is based on the purpose of the device. Furthermore, whether it is Schottky contact or ohmic contact can be controlled by the work function difference and the dopants type of semiconductor.

1.2.1 Metal Germanide

In 1966, silicide formation was first confirmed to be practical to form ohmic and Schottky contact. Because of high melting point, high thermal stability, and low resistivity, silicide has been widely used in the state-of-the–art VLSI process technology. In order to reduce the parasitic resistance, self-aligned metal silicide (salicide) process was introduced in 1981 [28-30]. Salicide is the process that sputtering a metal film after the gate and source/drain diffusion region formation, then annealing by rapid thermal annealing (RTA) to let metal reacts with silicon to form metal silicide. After silicide formation, selected wet etching is used to remove unreacted metal. By the salicide process, silicide is only formed on the silicon exposed regions. In brief, salicide has plenty of advantages not only reducing parasitic resistance and contact resistance but also the self-aligned feature.

In germanium devices, germanide is also used for the purpose similar to the silicide in silicon devices. In the germanidation process, the germanide must have the following characteristics: low resistivity, less germanium consumption, and good thermal stability. There were many kinds of metals have been examined for germanidation such as Fe, Co, Ni, Pd, Pt, and Cu [31]. Among them, NiGe and PdGe are considered to be the candidate due to the lower resistivity, but nickel is the most appropriate metal to form germanide for four reasons. At first, NiGe has the lowest resistivity ($< 22\ \mu\Omega.cm$) [31-33]. Secondly, NiGe forms at low temperature [34]. Some research showed that NiGe can be formed at $275^{o}C$. Third, unreacted nickel can be easily removed by HCl or hot H_3PO_4 [35]. Lastly, it is thermodynamically stable with no Ge-rich phase nickel germanide [31, 36, 37]. Furthermore, nickel controls the diffusion in germanidation, and Ni_2Ge forms in the beginning then transit to NiGe. Therefore, for the four reasons, NiGe has been studied intensively. However, NiGe

has two disadvantages in application. One of the disadvantages is germanium out diffusion during germanidation [38]. Research showed that germanide overgrows over the SiO_2 isolation by one-step formation (330^oC) and germanium voids left around the corner of isolation, but no overgrowth appears by two-step formation process (270^oC/330^oC). In addition, a method has been proposed to solve this problem, oxidation to form thin GeO_2 between nickel and germanium before germanidation [39], but whether it is effective is necessary to be proved. The other disadvantage is that NiGe is thermally unstable. The sheet resistance of NiGe increases sharply above 500^oC, ascribed to NiGe agglomeration [40]. When some metals are added to form germanide between nickel and germanium such as Pt [41] and Ti [42], the thermal stability could be improved.

1.2.2 Fermi Level Pinning

In ideal case, as metal contacts with semiconductor to form Schottky contact, the Schottky barrier height might changes with different kinds of metals due to different work functions following the relationship of $\varphi_{bn}=\varphi_m-\chi$. However, in the metal/germanium contact, the Schottky barrier height almost would not changes with different metals. It is just like the Fermi level is pinned at a fixed position resulting in the Schottky barrier height unchanged; this phenomenon is called the Fermi level pinning. There is a formula to express the Fermi level pinning, $\varphi_{bn}=S(\varphi_m-\varphi_{CNL})+(\varphi_{CNL}-\chi)$, where φ_{bn} is Schottky barrier height, φ_m is metal work function, φ_{CNL} is charge neutrality level, χ is electron affinity, and S is pinning factor. The pinning factor can be used to judge whether Fermi level pinning exists. If S approaches to 1, it means Schottky barrier height changed with metal work function, so Fermi level pinning effect hardly exists. On the contrary, If S approaches to 0, it

means Schottky barrier height unchanged with metal work function. Therefore, by sketching the relation of φ_{bn} and φ_m, the slope gives the pinning factor S and that the extent of Fermi level pinning is obtained.

In general, the causes of Fermi level pinning effect could be attributed to interface state. The interface state stems from Metal Induced Gap States (MIGS) [14] and dangling bonds. MIGS is the fact that when metal contacts with semiconductor, metal electron wave function would penetrate into semiconductor band gap. In addition, the other cause is the dangling bonds existing at semiconductor surface. However, the research of Fermi level depinning by insertion of a dielectric layer [43] or a doping segregation layer [44] would not completely support these two causes of Fermi level pinning, so the reasons of Fermi level pinning is not quite clear now. Charge neutrality level (CNL)[45] then comes into existence by virtue of surface states interaction. Furthermore, Fermi level is usually pinned at the charge neutrality level. For germanium, the Fermi level is pinned at 0.1eV above the valence band and the pinning factor S = 0.05 [16]. As a result, the metal/n-germanium Schottky barrier height is high.

1.2.3 Method for Fermi Level Depinning

Due to the Fermi level pinning effect mentioned above, the barrier height between metal and semiconductor could not change with metal work function. In addition, Fermi level is always pinned at near valence band on germanium so it is difficult to form ohmic contact on n-type germanium. Therefore, some methods have been presented to relax the Fermi level pining effect and/or modify the Schottky barrier height [43, 46, 47]. Surface passivation is a kind of the way by using solution immersion, ion implantation, or plasma treatment to relax the Fermi level pinning

effect. By these techniques, the dangling bond would be reduced by means of surface passivation so that the Fermi level pinning effect would be alleviated. Research show that $(NH_4)S$ solution immersion, sulfur implantation into germanium, and CF_4 plasma treatment can effectively alleviate Fermi level pinning [44, 47, 48]. The other method is insertion of thin dielectric film. Several researches have different idea to explain the mechanism about Fermi level depinning. Some research showed that the dipole would exist at the interface to cause shift of the pinning position [49-51] and other research indicated many fixed oxide charges in the dielectric to cause band bending [52]. In addition, there are many research discussing about Fermi level depinning by insertion of TiO_2[46], Al_2O_3[46], Si_3N_4, Si[53], and Ge_3N_4[54]. However, insertion of dielectric film would cause the additional tunneling resistance to reduce on-current. The tunneling resistance is determined by the thickness of dielectric and the conduction band offset (CBO) of dielectric to germanium. On the one hand, the thinner dielectric would get lower resistance but the dielectric may be not enough to block metal electron wave function penetration. Therefore, it is critical to determine the thickness of dielectric film. On the other hand, conduction band offset can also affect the tunneling resistance. For example, conduction band offset of TiO_2 is nearly zero to germanium so that there is nearly no tunneling resistance or barrier. Consequently, the thickness of TiO_2 would not affect the contact resistance a lot.

In short, there are many kinds of methods for Fermi level depinning such as surface passivation and insertion of dielectric film. Furthermore, Fermi level depinning is exactly an important issue to form ohmic contact or get lower contact resistance.

1.3 Dopants activation in germanium

As the devices scale down generation by generation, the dimension of transistor becomes smaller and smaller and the device structure become more and more complicate as well. When the channel length decreases, short channel effect then occurs. Short channel effect is an effect that the depletion width of source/drain is too large to affect the gate threshold voltage, and it usually happens on small devices. Therefore, forming ultra-shallow junction is the best way to relax this effect. However, forming ultra-shallow n^+/p-Ge junction is difficult.

In advanced CMOS process, ion implantation is the prevalent way to form source/drain doping. Nevertheless, ion implantation would produce lots of defects in the implantation region. The defects may affect device performance and enhance dopant diffusion, but high temperature annealing could recover these defects. In germanium, n-type dopants diffuse fast at high temperature [9-13] and dopants are difficult to activate to obtain high carrier concentration because of low solid-state solubility [17]. Because activation of n-type dopants needs higher than 500°C thermal annealing [55, 56] but shallow junction needs low temperature process, it is hard to form n-type high-concentration and ultra-shallow junction by ion implantation. Besides, phosphorous has lower diffusion coefficient and higher solid-state solubility than the other n-type dopants. On the contrary, p-type dopants behave totally different from n-type dopants [18]. P-type dopants have higher activation concentration (Boron: $6x10^{20}cm^{-3}$ versus Phosphorous: $2x10^{20}cm^{-3}$) and hardly diffuse even at high temperature [19].

In the past, many methods were raised to increase activation concentration and retard the dopant diffusion. One of the methods is using laser annealing to activate dopant, which could obtain high activation concentration because of high temperature

and short dopant diffusion because of transient annealing [57-59]. Another one is co-implantation, for example, antimony and phosphorous co-implantation due to local strain compensation between antimony and phosphorous [60, 61] or phosphorous and fluorine co-implantation because fluorine passivation of the defects in Ge to increase the activation concentration [62]. ;. The other one is spin-on dopant which is free from ion damage [63].

1.4 Contact Resistance

As devices scale down, the parasitic resistance becomes more and more critical for high performance devices. Parasitic resistance is composed of source/drain extension (SDE) to gate overlap resistance R_{ov}, SDE resistance R_{ext}, deep S/D resistance R_{dp}, and silicide-diffusion contact resistance R_c as shown in Fig.1-1 [64]. Every factor would affect device performance greatly. However, for the smaller devices, the contact resistance plays the predominant role to affect the parasitic resistance as shown in Fig.1-2 [65]. Therefore, it is important to pay more attention on reducing metal/semiconductor contact resistance.

The contact resistance (Ω) issue is always discussed in another criterion, specific contact resistance (ρ_c) without the influence of contact size. Specific contact resistance is defined as the reciprocal of deviation of current density to voltage at zero voltage.

$$\rho_c \equiv \left(\frac{\partial J}{\partial V}\right)_{V=0}^{-1} \ (\Omega \cdot \mathrm{cm}^2),$$

where J is current density (A/ cm^2) and V is voltage (V).

For the low doping concentration metal/semiconductor contact, the thermionic emission mechanism leads the current transportation. Therefore, ρ_c can be expressed

by

$$\rho_c(TE) = \frac{k}{qA^*T}\exp(\frac{q\phi_B}{kT}),$$

where k is Boltzmann constant, q is the charge of an electron, A* is Richardson constant, T is absolute temperature, and Φ_B is Schottky barrier height. As a result, reducing the Schottky barrier height could get lower specific contact resistance.

Furthermore, for the high doping concentration metal/semiconductor contact, the tunneling mechanism would lead the current transportation. Therefore, ρ_c can be expressed by

$$\rho_c(FE) \propto \exp\left[\frac{2\sqrt{\epsilon_s m^*}}{\hbar}\left(\frac{\phi_B}{\sqrt{N_d}}\right)\right],$$

where ε_s is dielectric constant, m* is electron mobility, and N_d is doping concentration. Consequently, in order to reduce specific contact resistance, increasing the doping concentration and reducing the Schottky barrier height are necessary.

As a result, the specific contact resistance should be reduced in metal/n-Ge having Fermi-level pinning effect. In addition, there have been already some research not only increasing the doping concentration but also reducing the Schottky barrier height to reduce metal/n-Ge specific contact resistance [25, 66-70].

1.5 Dopant Segregation Method

Dopant segregation method can be used to increase doping concentration and modulate the effective Schottky barrier height in order to reduce contact resistance. The dopant segregation junction depends on very high doping concentration that leads to a strong band bending at the interface between metal and semiconductor, so the carriers could tunnel through the barrier easier. There are two kinds of ways to form the Ge dopant segregation junction, implantation after germanidation and

implantation before germanidation. Implantation after germanidation is the way implanting dopants into the metal germanide after metal germanide formation, then annealing at medium temperature to let the dopants diffuse out and segregate at the interface [71]. Since ion implantation is performed after germanide formation, we call it the implantation after germanidation (IAG) process. With different segregation coefficient of varied dopants, the effect of segregation would be different. On the other hand, dopant segregation is the way dopants implantation first followed by metal germanide formation. During germanidation, the dopants segregate in front of the forming germanide front because of the snowplow effect of the dopants [72]. Since the ion implantation is performed before germanide formation, we call it the implantation before germanidation (IBG) process. Research showed that sulfur and selenium could reduce effective Schottky barrier height [47, 73]. In brief, no matter what kind of processes is used to form the dopant segregation junction, the purpose is utilizing dopant segregation to form high doping concentration region at the interface. As a result, dopant segregation junction formation could change the Schottky contact with high Schottky barrier to ohmic contact for reduction of metal/Ge contact resistance.

1.6 Motivation

In order to reduce the parasitic resistance, metal germanide would be selected to form S/D contact due to its low resistivity. NiGe is selected to be the germanide due to its low resistivity and low formation temperature. In addition, because of fast diffusion of n-type dopants and low activation concentration in germanium, the general high temperature RTA activation would form a deep junction and is hard to form shallow junction. In this thesis, IBG process and IAG process are introduced to

form shallow junction. The doping concentration may be high due to segregation, and the junction depth may be shallow.

Moreover, because the Fermi level is pinned near the germanium valence band, the high Schottky barrier exists on the NiGe/n-Ge contact and the contact resistance would be high. On the contrary, the specific contact resistance on NiGe/p-Ge would be as low as $2x10^{-7}$ Ω・cm^2 [32]. Previous studies showed that contact resistance was reduced by laser annealing [25], which is a high temperature process, and some other papers [25, 26, 66, 68] also showed low contact resistance in Table 1-2. However, in this thesis, IBG+IAG process and dielectric insertion are introduced to get low contact resistivity without high temperature annealing. At first, the high n-type doping is formed by implantation and RTA. Secondly, NiGe formation can let the dopant segregate at the NiGe/n-Ge interface. Next, n-type dopants are implanted into the NiGe. Finally, annealing by RTA let the dopants diffuse out to segregate again. Due to the dual-segregation, high doping concentration is expected. Furthermore, the effective Schottky barrier height is also reduced because the band bending in high doping concentration causes carrier tunneling. According to ρ_c formula of high doping concentration, ρ_c would be reduced by high doping concentration and low Schottky barrier height.

In summary, the thesis is focused on forming shallow n^+/p junction and reducing the contact resistivity by dopant segregation method and dielectric insertion method. It is anticipated to improve the performance of S/D junction on germanium NMOSFET in next generation.

1.7 Organization

Chapter 1 includes the introduction of germanium characteristics and the encountered problems in metal contact and n^+/p-Ge junction. In addition, the contact resistance and dopant segregation method are also introduced in the chapter. Chapter 2 describes the fabrication process of samples. Material and electrical analysis are introduced as well.

Chapter 3 focused on the IBG junction. The conventional junctions of different implantation dosage are first discussed, then forming NiGe, which named IBG junction, is done to compare the electrical characteristics with conventional junctions. Furthermore, studying IBG junction on different concentration substrates and the effect of Ni diffusion is also included. Finally, the contact resistance of the IBG+IAG junctions are also showed, the results are proved by material analysis as well.

Finally, Chapter 4 summarizes the experiment results and makes some conclusions. The future works are suggested as well.

Table 1- 1 Interface trap density (D_{it}) and effective oxide thickness (EOT) recorded by previous studies in Ge capacitor.

Gate stack	Treatment	D_{it} ($cm^{-2} eV^{-1}$)	EOT (nm)	Source
$Ge/GeO_x/Al_2O_3$	O_2 plasma and PDA in N_2 at 400°C, 30 min	$1x10^{11}$	~1	[23]
$Ge/GeO_x/ Al_2O_3/HfO_2$	N.A.	$5x10^{11}$	0.76	[24]
Ge/GeON/HfTiON	PDA in NH_3 ambient at 500°C, 300s	$2.3x10^{11}$	0.96	[74]
Ge/GeON/HfTiON	PDA in wet NO at 500°C, 300s	$1.2x10^{11}$	1.02	[74]
Ge/GeON/TaON/ HfTiON	PDA in wet NO at 500°C, 40s	$5.4x10^{11}$	0.91	[75]
Ge/GeON/TaON/ HfTiON	PDA in NH_3 ambient at 500°C, 40s	$6.8x10^{11}$	0.86	[75]
$Ge/AlN/HfO_2$	N.A.	$1 x10^{12}$	0.82	[76]

Table 1- 2 Metal/n-Ge contact resistance recorded by previous studies.

Contact	Doping	Activation	Test Structure	Contact Resistivity (Ω-cm^2)	Junction Depth (nm)	Source
NiGe	P+Sb IBG	500°C/RTA	CTLM	5.5x10^{-7}	200	[27]
NiGe	As IBG	900°C/LSA	CTLM	1.4x10^{-6}	N.A.	[25]
NiGe	As IBG	800°C/LSA	CTLM	5.0x10^{-5}	30	[25]
NiGe	P IBG	500°C/FA	TLM	8.8x10^{-5}	N.A.	[68]
NiGe$_x$	P IBG	500°C/FA	TLM	3.5x10^{-6}	N.A.	[68]
Al	P-epi	None	CTLM	4.6x10^{-5}	N.A.	[25]
Ti	As I/I	600°C/RTA	CTLM	1.0x10^{-3}	N.A.	[25]
Ti	P I/I	650°C/N.A.	CTLM	4.9x10^{-5}	N.A.	[66]
TaN	P I/I	650°C/N.A.	CTLM	2.7x10^{-5}	300	[26]

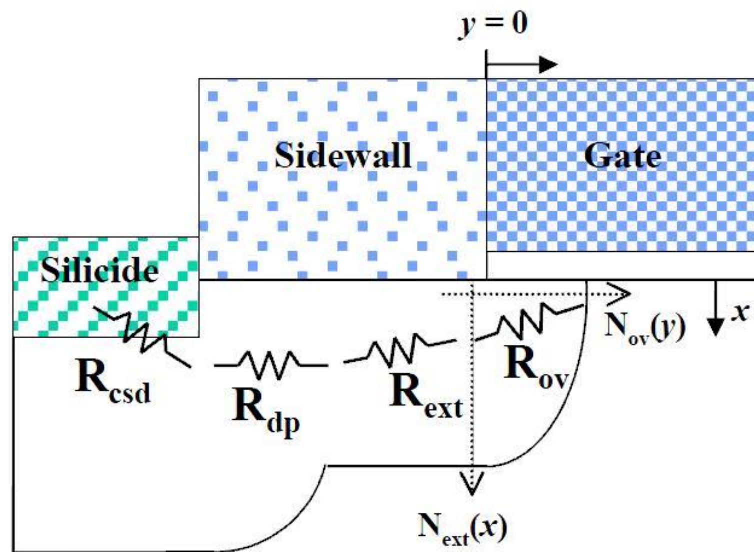
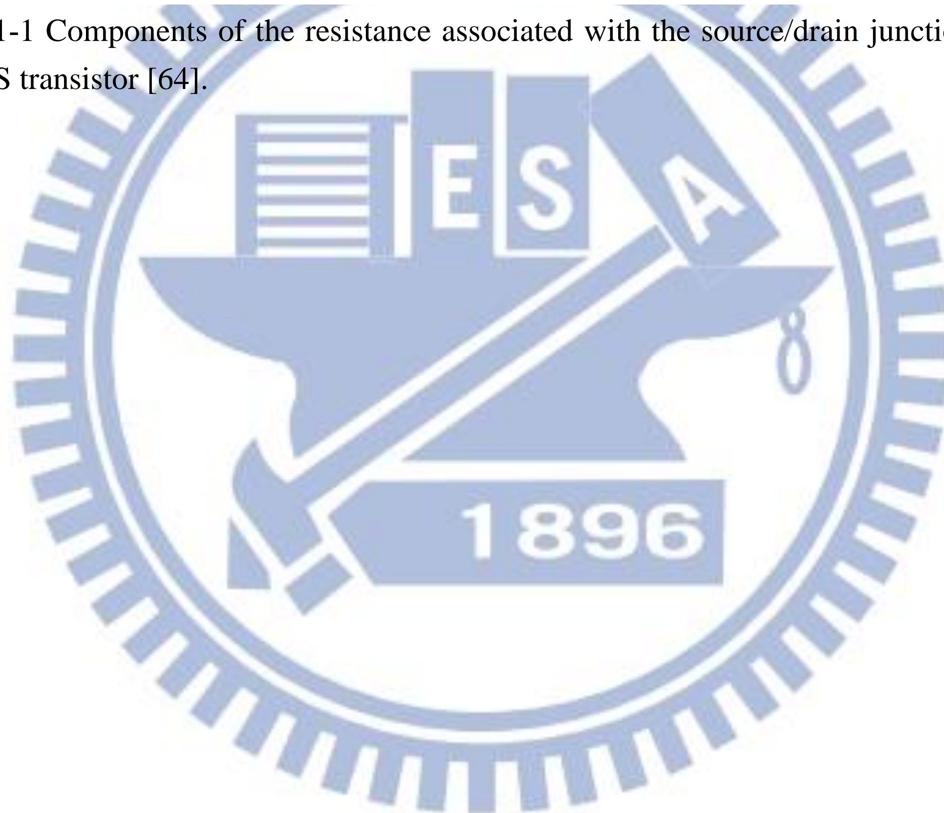
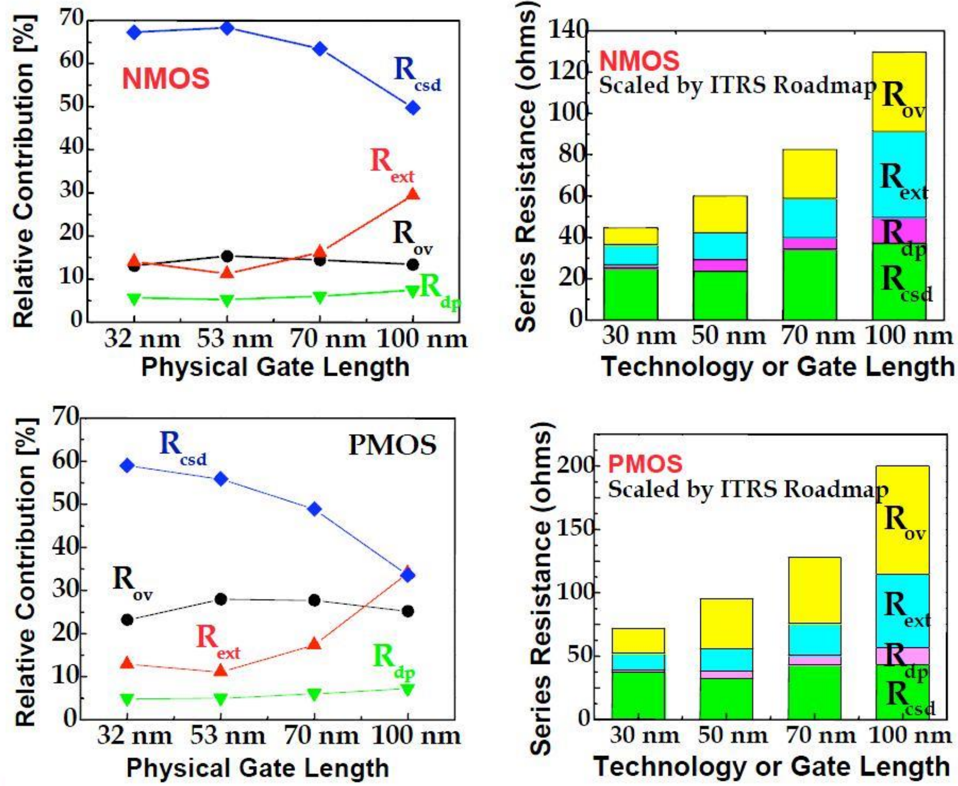


Fig.1-1 Components of the resistance associated with the source/drain junctions of a MOS transistor [64].





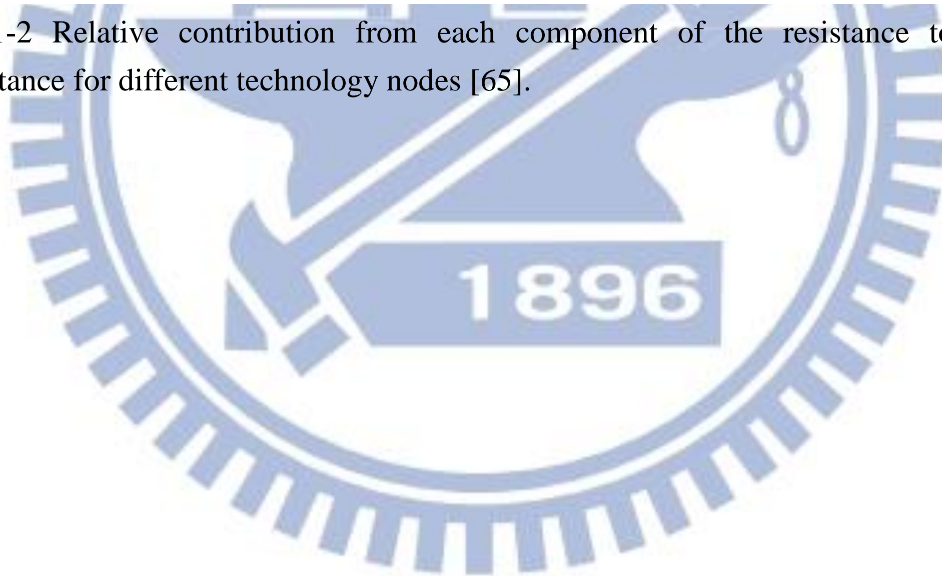


Fig.1-2 Relative contribution from each component of the resistance to series resistance for different technology nodes [65].

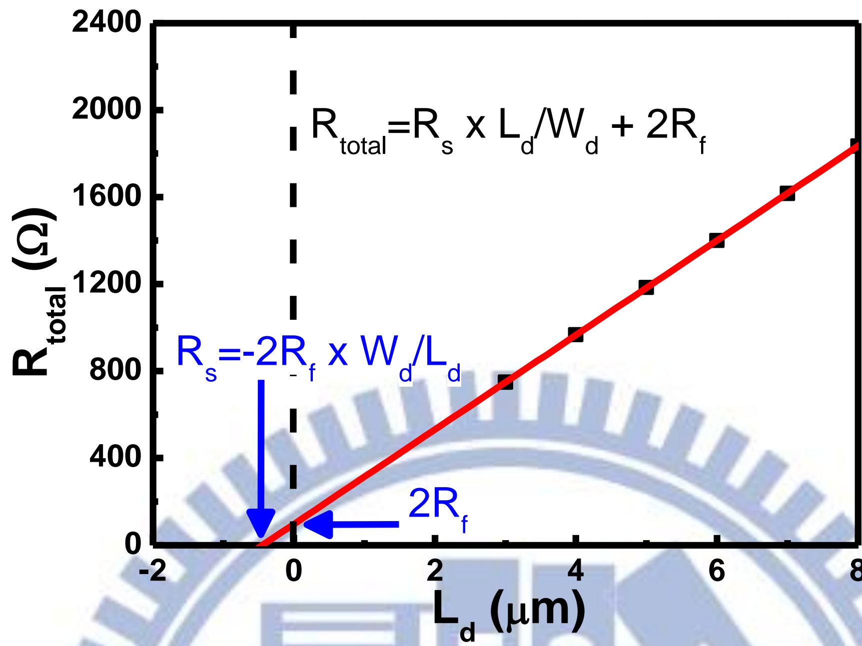


Fig.1-3 Extraction of the front resistance (R_f) from the R_{total}-L_d plot.

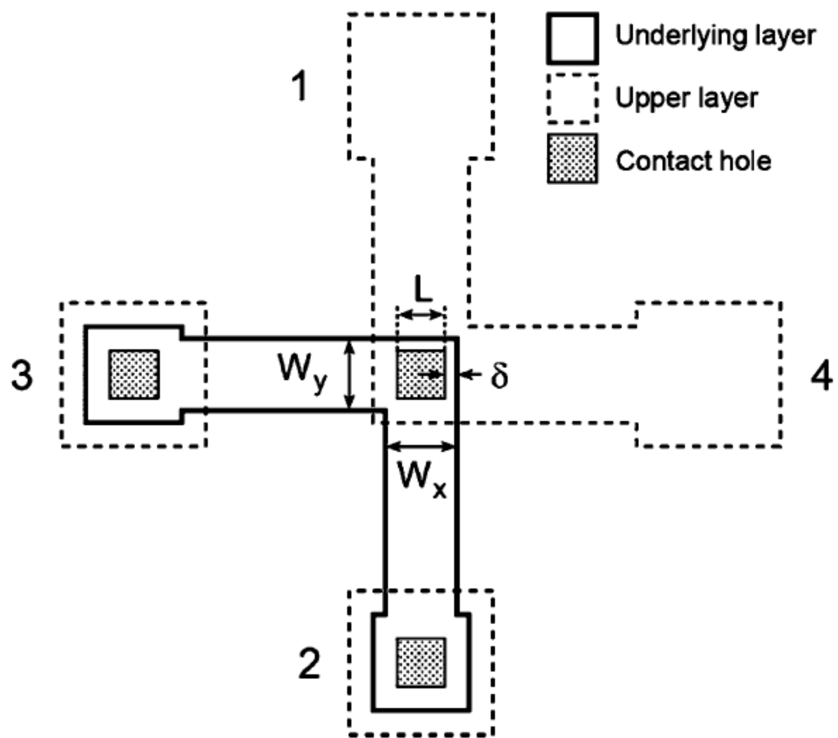
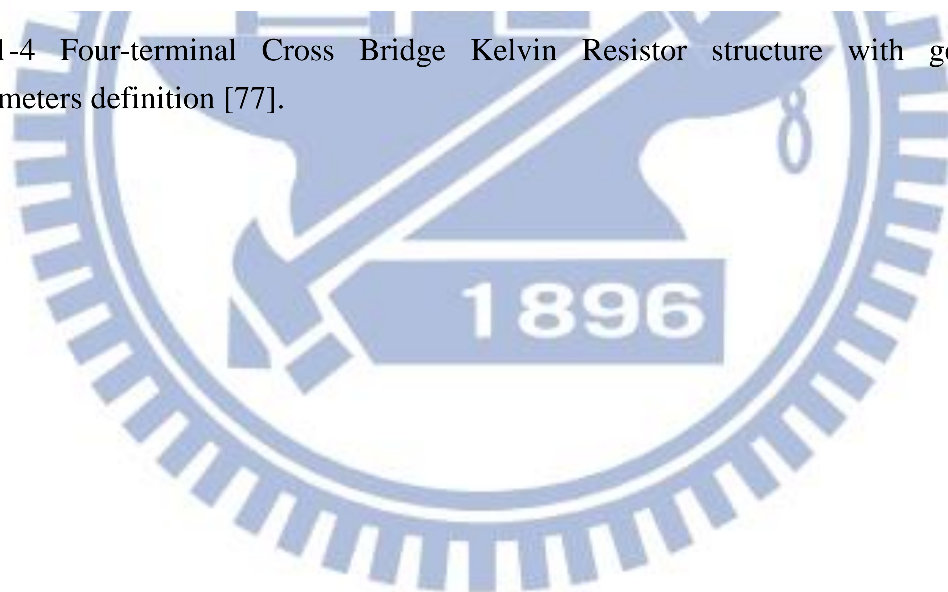


Fig.1-4 Four-terminal Cross Bridge Kelvin Resistor structure with geometry parameters definition [77].



Chapter 2
Experiments

2.1 Devices Fabrications

In this section, the fabrication processes of devices used in this thesis are described in detail. Two kinds of Ge substrate were used. They are Ga-doped (100)-oriented Ge wafer with resistivity 0.01~0.05 ohm-cm and Ga-doped (100)-oriented Ge wafer with resistivity 1~10 ohm-cm. The former one is called heavily doped substrate and the later one is called the lightly doped substrate.

2.1.1 IBG + IAG Junction Formation

All the samples were dipped in diluted HF solution ($HF:H_2O=1:50$) for 2 minutes and rinsed by DI water for 5 minutes to clean the surface at first. Then, 300-nm-thick Tetraethyl orthosilicate (TEOS) SiO_2 was deposited by a plasma enhanced chemical vapor deposition (PECVD) system at 350°C as field oxide. Active regions were patterned by typical lithography process and the field oxide was etched by buffered oxide etchant (BOE) for 90 seconds. The residual photo-resist was removed by acetone in ultrasonic cleaner for 1 minute.

The samples on the heavily-doped Ge substrate were implanted by Phosphorus at 20 keV to a dose of $1x10^{15}$ cm^{-2} and at 50keV to a dose of $5x10^{13}$ cm^{-2}. Furthermore, the samples on the lightly-doped Ge substrate were implanted by Phosphorus at 50 keV to a dose of $1x10^{15}$, $5x10^{13}$, $1x10^{13}$, or $5x10^{12}$ cm^{-2} and Arsenic at 50 keV to a dose of $1x10^{15}$, $5x10^{13}$, or $1x10^{13}$ cm^{-2}. All samples were annealed at 600 ^{o}C for 60

seconds in N_2 ambient by a rapid thermal annealing (RTA) system to activate the dopants, and the N^+/P-Ge junctions formed.

Before Ni deposition, some heavily-doped samples were implanted by Fluorine at 10keV to a dose of $1x10^{15}$ cm^{-2} to study the effect of fluorine on the Ni diffusion. Moreover, the samples were dipped in diluted HF solution ($HF:H_2O$=1:100) for 2 minutes and rinsed by DI water for 5 minutes to clean the surface. After that, Ni was deposited to 10-nm-thick to form germanide and TiN was deposited to 15-nm-thick to passivate Ni surface by a co-sputtering system. The Ni deposition was performed under the condition of Ar with 100 sccm and 300W at the rate about 0.5nm/sec, moreover, the TiN deposition was performed under the condition of Ar/N_2 with 100/10 sccm and 800W at the rate about 0.68nm/sec. The Ni-deposited samples were annealed at 350°C for 5 minutes by a backend vacuum annealing furnace to form NiGe. The process is called IBG process.

After forming NiGe, the unreacted metal was selectively etched by hot H_3PO_4 at 150°C for 5 minutes and the NiGe formation is finished. Samples were implanted again by Arsenic at 10 keV to a dose of $1x10^{15}$ cm^{-2} and annealed at 500/550/600°C for 10 seconds in N_2 ambient by rapid thermal annealing (RTA) to segregate the dopants at the interface. The process is called IAG process.

Finally, a 300-nm-thick Al was deposited by a thermal coater to act as the contact metal. The Al layer was patterned by the typical lithography process and high density plasma - reactive ion etching (HDP-RIE) with Cl_2 and BCl_3 as the reacting gas, and the residual photo-resist was removed by acetone in ultrasonic cleaner for 1 minute. A 300-nm-thick Al was deposited again by a thermal coater at wafer backside to form backside contact.

First, the conventional junctions were fabricated by the IBG process flow but skipping the NiGe related process steps and the main process conditions are

summarized in Table 2-1. Secondly, the IBG junctions are only fabricated by IBG process and the main process conditions are summarized in Table 2-2. Next, the IAG junctions are only fabricated by IAG process and the main process conditions are summarized in Table 2-3. Finally, the IBG+IAG junctions are fabricated by IBG and IAG process and the main process conditions are summarized in Table 2-4. In addition, the process flow of IBG+IAG junctions is depicted in Fig. 2-1.

2.1.2 Contact Resistance of IBG+IAG junctions

Lightly doped Ge substrate was used in this experiment. The process flow is identical to the IBG+IAG junction. However, after activation annealing, 300-nm-thick TEOS SiO_2 was deposited again; then, contact regions were patterned and the oxide was etched by BOE for 90 seconds. The main process conditions of the contact resistance of IBG+IAG junctions are summarized in Table 2-5. Also, the process flow is depicted in Fig. 2-2.

The contact resistance were extracted by six-terminal D-type CBKR structure shown in Fig.2-3. The contact area values of the CBKR structures used in this thesis are designed in 3x3 μm^2, 5x5 μm^2, and 10x10 μm^2. The widths of current arms and voltage arms are designed to be the same values as the contact widths. The process tolerances are considered with 3μm.

2.2 Material Analysis and Electrical Measurement

The Current-voltage (I-V) characteristics of devices were measured by a semiconductor analyzer of model Agilent 4156C. The contact resistance was also measured by the same semiconductor analyzer. Sheet resistance was measured by a

four point probe system. Furthermore, the samples were analyzed by different kinds of material analysis instrument in order to compare with the results of electrical measurement, for example, X-ray Diffraction (XRD), Transmission Electron Microscopy (TEM), Scanning Electron Microscopy (SEM), and Secondary Ion Mass Spectrometer (SIMS).

XRD was used to analyze the crystallized orientation of NiGe. When X-ray goes through the crystallized structure, the constructive interference occurs. According the Bragg's Law ($n\lambda=2d\sin\theta$), the constructive interference only occurs for certain θ correlating to a (h k l) plane. Therefore, the crystallized (h k l) plane of NiGe can be inferred. TEM was used to observe the microstructure of NiGe film. TEM depends on electrons beam transmitted through an ultra-thin specimen and the electrons beam interacts with the specimen as it passes through to form the image. The image is magnified and focused on the imaging device with high resolution. Therefore, the quality of NiGe film can be clearly observed. In addition, SEM is used to observe the surface of NiGe film. SEM produces images by means of scanning the samples with electrons beam and the electrons interact with atoms in the samples to detect the signal and show the samples' surface topography. SIMS was used to analyze the distribution of elements in the samples, such as P, As, and Ni. SIMS analysis relies on sputtering the surface of the samples with a focused ion beam and analyzing the ejected secondary ions from the surface. The kind of elements could be determined by mass/charge ratios of these secondary ions. Moreover, the amount and depth distribution of the elements could also be detected at the same time.

In brief, all the material analysis plays the role of assistant to prove the measured electrical characteristics. As long as the results are consistent, the inference or conclusion would be more convinced.

Table 2-1 Main process recipe of conventional junctions.

Implantation Recipe	Annealing Recipe	Substrate
P, 50keV, $5x10^{12}$ cm^{-2}	600^oC, 60s	Lightly
P, 50keV, $1x10^{13}$ cm^{-2}		
P, 50keV, $5x10^{13}$ cm^{-2}		
P, 50keV, $1x10^{15}$ cm^{-2}		
As, 30keV, $1x10^{13}$ cm^{-2}	600^oC, 60s	Lightly
As, 30keV, $5x10^{13}$ cm^{-2}		
As, 30keV, $1x10^{15}$ cm^{-2}		
P, 50keV, $5x10^{13}$ cm^{-2}	600^oC, 60s	Heavily
P, 50keV, $1x10^{15}$ cm^{-2}		

Table 2-2 Main process recipe of IBG junctions.

Implantation Recipe	Annealing Recipe	NiGe formation	Substrate
P, 50keV, $5x10^{12}$ cm^{-2}	600^oC, 60s	350^oC, 5min	Lightly
P, 50keV, $1x10^{13}$ cm^{-2}			
P, 50keV, $5x10^{13}$ cm^{-2}			
P, 50keV, $1x10^{15}$ cm^{-2}			
As, 30keV, $1x10^{13}$ cm^{-2}	600^oC, 60s	350^oC, 5min	Lightly
As, 30keV, $5x10^{13}$ cm^{-2}			
As, 30keV, $1x10^{15}$ cm^{-2}			
P, 50keV, $5x10^{13}$ cm^{-2}	600^oC, 60s	300/325/350/400/450^oC, 5min	Heavily
P, 50keV, $5x10^{13}$ cm^{-2}		325/350/400^oC, 5min with F Implantation (10keV, $1x10^{15}$ cm^{-2})	
P, 50keV, $1x10^{15}$ cm^{-2}		350/400/450^oC, 5min with F Implantation (10keV, $1x10^{15}$ cm^{-2})	

Table 2-3 Main process recipe of IAG junctions.

NiGe	Implantation Recipe	Annealing Recipe	Substrate
350°C, 5min	As, 10keV, $1x10^{15}$ cm^{-2}	500°C, 10s 550°C, 10s 600°C, 10s	Heavily

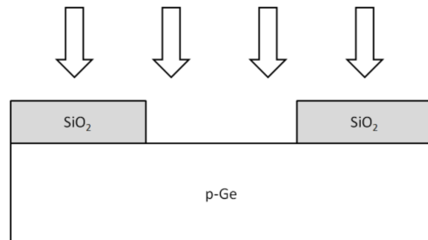
Table 2-4 Main process recipe of IBG+IAG junctions.

Implantation Recipe 1st	Annealing Recipe 1st	NiGe	Implantation Recipe 2nd	Annealing Recipe 2nd	Substrate
P, 20keV, $1x10^{15}$ cm^{-2}	600°C, 10s	350°C, 5min	As, 10keV, $1x10^{15}$ cm^{-2}	500°C, 10s	Lightly

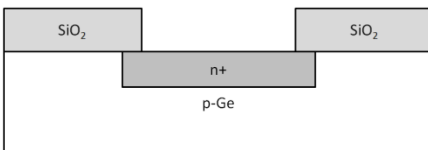
Table 2-5 Main process recipe of Contact Resistance of IBG+IAG junctions

Implantation Recipe	Annealing Recipe 1st	NiGe	Implantation Recipe	Annealing Recipe 2nd	Substrate
P, 20keV, $1x10^{15}$ cm^{-2}	600°C, 10s	X	X	X	Lightly
P, 20keV, $1x10^{15}$ cm^{-2}	600°C, 10s	350°C, 5min	X	X	Lightly
P, 20keV, $1x10^{15}$ cm^{-2}	600°C, 10s	350°C, 5min	As, 10keV, $1x10^{15}$ cm^{-2}	500°C, 10s	Lightly
P, 20keV, $1x10^{15}$ cm^{-2}	600°C, 10s	350°C, 5min (with F Imp)	As, 10keV, $1x10^{15}$ cm^{-2}	500°C, 10s	Lightly

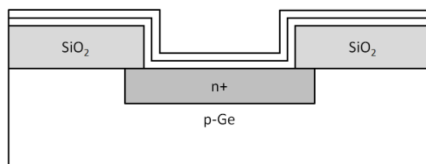
1. HF clean
2. 300nm SiO_2 deposition
3. Active area defined by lithography process
4. SiO_2 etching by BOE
5. Remove PR by ACE



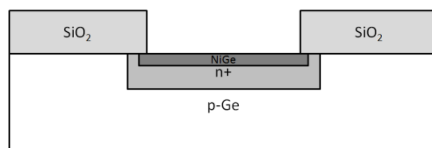
6. P or As implantation



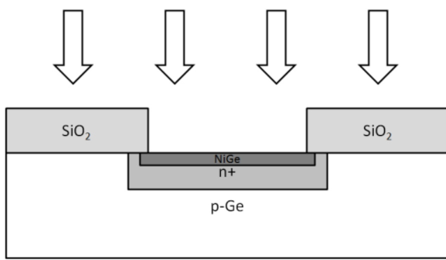
7. Dopant activation ($600^{o}C$,60s)



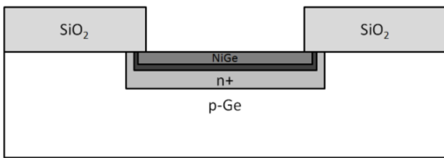
8. Ni(10nm)/TiN(15nm) deposition by Sputter system



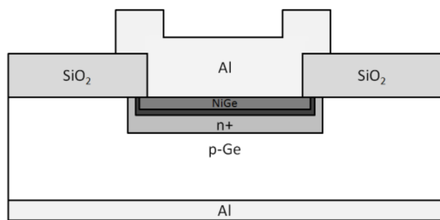
9. NiGe formation
10. Unreacted-Ni and TiN were etched by hot H_3PO_4



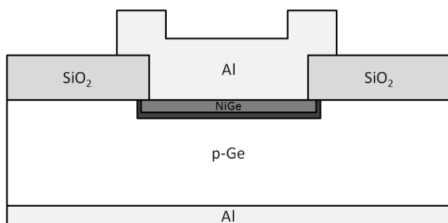
11. As implantation



12. Dopant activation

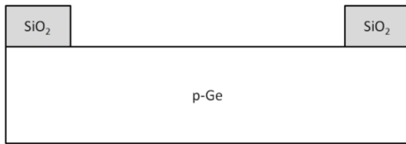


13. Al contact defined by lithography process
14. Al etching by HDPRIE
15. Al backside contact

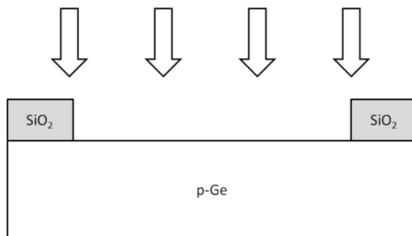


IAG junctions without first implantation

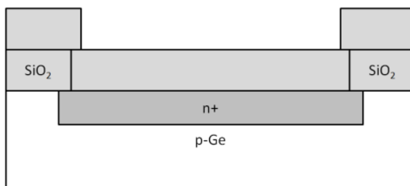
Fig.2-1 Process flow of IBG+IAG junctions.



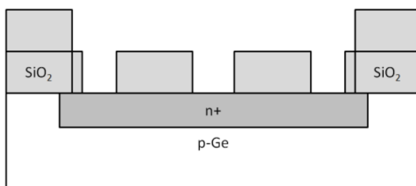
1. HF clean
2. 300nm SiO_2 deposition
3. Diffusion region defined by lithography process
4. SiO_2 etching by BOE
5. Remove PR by ACE



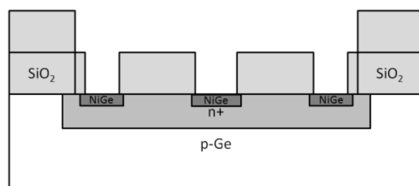
6. Implantation:
   P, 20keV, $1x10^{15}$ cm^{-2}
7. Dopant activation
   (600^oC,10s)



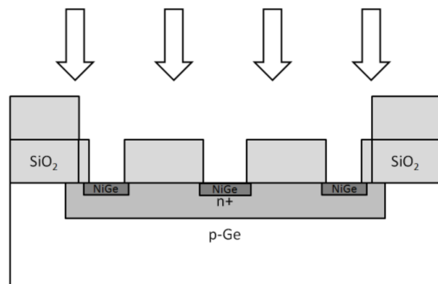
8. 300nm SiO_2 deposition



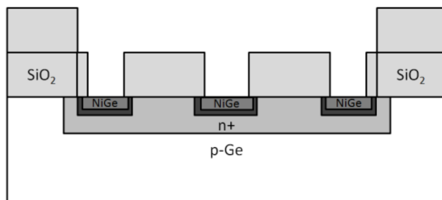
9. Active region lithography
10. SiO_2 etching by BOE
11. Remove PR by ACE



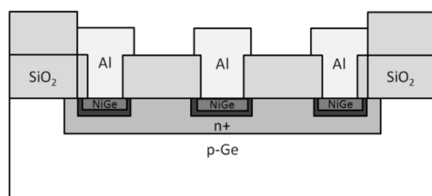
12. Ni(10nm)/TiN(15nm) deposition by Sputter system
13. NiGe formation (350^oC, 5min)
14. Unreacted-Ni and TiN were etched by hot H_3PO_4



15. Implantation :
    As, 10keV, 1×10^{15} cm^{-2}



16. Dopant activation



17. Al contact defined by lithography process
18. Al etching by HDPRIE
19. Al backside contact

Fig.2-2 Process flow of Contact Resistance of IBG+IAG junctions.

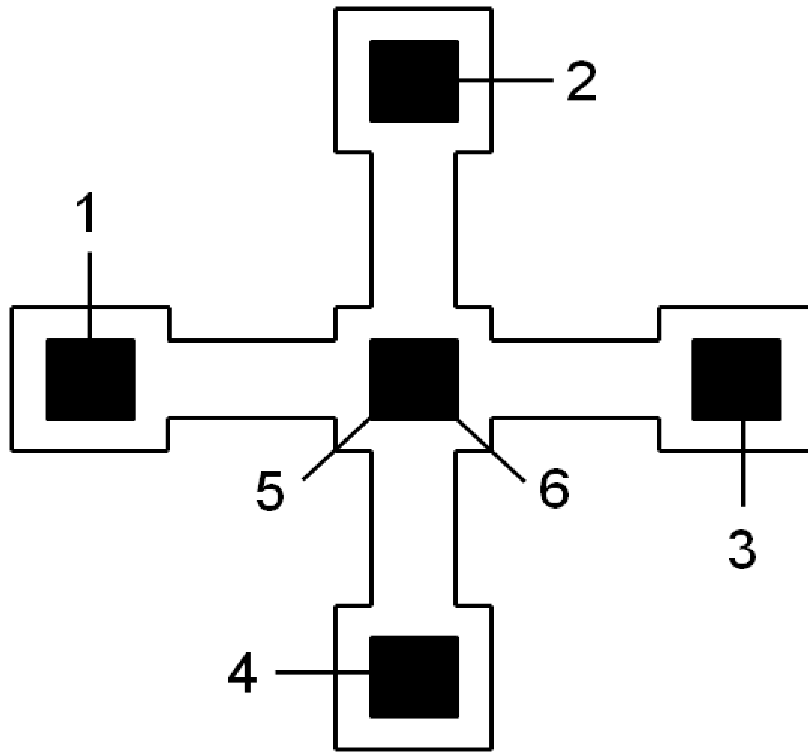


Fig.2-3 Schematic layout of six-terminal Cross Bridge Kelvin Resistor (CBKR) structure.

Chapter 3
IBG and IAG junctions

3.1 NiGe formation

In order to find out the lowest thermal budget for NiGe formation, the sheet resistance of the NiGe film formed at different thermal budgets was measured and shown in Fig.3-1 and Fig.3-2. According to Fig.3-1, the sheet resistance of NiGe decreases from 73 Ω/□ after 300 ^{o}C annealing to 20 Ω/□ after 325 ^{o}C annealing for 5 minutes and still keeps low after 400°C annealing. In addition, in Fig.3-2, the sheet resistance of NiGe decreases from 80 Ω/□ for 3 minutes annealing to 20 Ω/□ for 5 minutes annealing at 325 ^{o}C. According to the change of sheet resistance shown above, NiGe starts to growth at 325°C but the growth rate is slow so that at least a 5 minutes annealing is necessary. In the thesis, NiGe formation was performed at 350 ^{o}C for 5 minutes to ensure that NiGe could completely form if not specified. According to the formula of the sheet resistance R_{sh}=V/I x CF, where CF is correction factor determined by the value of d/s, where d is the distance of the probe to the sample edge and the s is the distance between the probes, the sheet resistance of NiGe measured by the four point probe system is under the condition of infinitely large samples and the correction factor is 4.5324. However, the samples' size used in the thesis is nearly 0.5x0.5 cm^2 and the value of d/s is about 3. Therefore, the correction factor is about 2.4575 based on the Table 3-1 and the thickness of NiGe is 20 nm (Fig.3-15); then, the resistivity of NiGe is calculated to be 22.04×10^{-6} Ω-cm. In addition, XRD diffraction analysis on the NiGe/Ge structure formed by 350°C annealing shows polycrystalline NiGe phases as shown in Fig. 3-3. The main NiGe crystal orientations

are (2 1 0), (1 1 2), and (1 1 1).

3.2 Conventional N^+/P Junctions

At first, the I-V curves of the conventional junctions with phosphorus ion implantation at 20 keV to a dose of $1x10^{15}$ cm^{-2} and 50 keV to a dose of $5x10^{13}$ cm^{-2} on heavily-doped substrate are shown in Fig.3-4. After dopant activation at 600 ^oC for 60 seconds, the junctions with phosphorus ion implantation at 20 keV to a dose of $1x10^{15}$ cm^{-2} has a relatively higher forward current and lower reverse current due to the higher doping concentration. The forward and reverse bias current ratio is about 5 orders of magnitude. In addition, the band-to-band tunneling can also be observed when the reverse bias exceeds 0.5 V. Because the high n^+ concentration and heavily-doped substrate cause high electric field at the junction edge, the electrons would easily tunnel through the band to the other side as the reverse bias is applied.

Next, the I-V curves of conventional junctions with phosphorus ion implantation at 50 keV to different doses of $1x10^{15}$, $5x10^{13}$, $1x10^{13}$, $5x10^{12}$ cm^{-2} on lightly-doped substrate are shown in Fig. 3-5. After annealing at 600 ^oC for 60 seconds, the forward current increases with the increase of the ion implantation dose and the junction with the highest dose of $1x10^{15}$ cm^{-2} has the highest forward current. The reason is that more dopants could be activated to form higher concentration of n^+ region so that the electron diffusion current increases and the NiGe/Ge contact resistance could be reduced. Moreover, the reverse bias current slightly increases with the increase of dose because higher ion implantation dose may induce more defects to raise leakage current. Therefore, the forward/reverse current ratio also increases with the increase of dose and the current ratio of the junction with a dose of $1x10^{15}$ cm^{-2} is about 10^3.

According to the depletion width formula of a p-n junction, $W = \left[\frac{2\varepsilon V_0}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)\right]^{\frac{1}{2}}$, where ε is permittivity, q is electronic charge, V_0 is build-in potential, N_a is concentration of acceptor, and N_d is concentration of donor. In other words, the depletion width is proportional to $\left(\frac{1}{N_a} + \frac{1}{N_d}\right)^{\frac{1}{2}}$. In addition, the reverse bias current is directly proportional to the depletion width when the generation current within the depletion region dominates the reverse bias current. Now, N_a is the concentration of substrate and N_d is the concentration of the n^+ region. If the concentration of n^+ region is the same, the concentration of substrate would dominate the reverse bias current. The lower concentration of substrate would cause the wider depletion width, and the wider depletion width would cause the higher reverse bias current. Comparing the I-V curves of the conventional junctions with phosphorus ion implantation at 50 keV to a dose of $5x10^{13}$ cm^{-2} on lightly-doped and heavily-doped substrate, e.g. Fig.3-4 and Fig.3-5, respectively, it is the reason why the reverse bias current on lightly-doped substrate is larger than that on heavily-doped substrate.

Thirdly, the I-V curves of conventional junctions with arsenic ion implantation at 50 keV to a dose of $1x10^{15}$, $5x10^{13}$, $1x10^{13}$ cm^{-2} on lightly-doped substrate are shown in Fig. 3-6. After dopants activation at 600 ^oC for 60 seconds, the junction with arsenic ion implantation to a dose of $1x10^{15}$ cm^{-2} shows the highest forward current and the lowest reverse current; the forward/reverse current ratio is about 300. However, the junctions with dose of $5x10^{13}$ and $1x10^{13}$ cm^{-2} show poor junction characteristics. The reason is that the doping concentration is not high enough so that the arsenic doped layer is depleted.

Comparing the I-V curves of conventional junctions of implantation by phosphorus and arsenic at 50 keV to a dose of $5x10^{13}$ cm^{-2} on lightly-doped substrate, the reverse bias current of the arsenic implanted junction is higher than that of the

phosphorus implanted junction because the activation ratio of arsenic is relatively lower than that of phosphorus so that the junction depth of the arsenic implanted junction is inferred to be shallower. Furthermore, the heavier arsenic atom would generate more defects than the lighter phosphorous atom. Therefore, the reverse bias current of the arsenic implanted junction is higher as shown in Fig. 3-5 and Fig. 3-6.

3.3 NiGe on Conventional N^+/P Junctions (IBG junctions)

In this session, we examine the effect of NiGe formation on the preformed N^+/P junctions, i.e the IBG junctions. Fig.3-7 shows the I-V curves of the IBG junctions with different NiGe formation temperatures. The preformed junction is implanted by phosphorus at 20 keV to a dose of $1x10^{15}$ cm^{-2} on heavily-doped substrate. All junctions show high reverse bias current and the electrical characteristics are nearly ohmic behavior. The junction with NiGe formation at 300^oC for 5 minutes shows lower current and slightly rectifying characteristic due to incomplete NiGe formation. From Fig.3-1, the sheet resistance is higher than 70 Ω/□ which implies that Ni_2Ge formed but not NiGe formed. Other junctions have the same high forward current about 10^2 A/ cm^2 as a result of complete NiGe formation.

Compared with the conventional junctions, before the NiGe formation, the reverse bias current is about 10^{-4} A/ cm^2; however, the reverse bias current rises apparently after NiGe formation and the current increases with the increase of the NiGe formation temperature. It means NiGe formation causes something happened to destroy the preformed junction. According to the temperature dependence, a possible reason may be the fast diffusion of Ni. Fig. 3-8 shows the diffusivity of elements in Ge, Ni has the second high diffusivity among these elements [78]. If Ni atoms enter the depletion region of the junction, they act as generation-recombination center and

destroy the junction. Therefore, finding some methods to suppress Ni diffusion is important.

A method of fluorine implantation before silicide formation had been proposed to solve the problem of large leakage current caused by Ni diffusion [79]. Hence, fluorine implantation before NiGe formation was performed in this thesis in order to solve the Ni diffusion problem. Fig.3-9 shows the I-V curves of the fluorine implanted junctions with different NiGe formation temperatures. The preformed conventional junction is formed by phosphorus ion implantation at 20 keV to a dose of $1x10^{15}$ cm^{-2} on heavily-doped substrate. It is observed that fluorine ion implantation reduces both forward current and reverse current. This result confirms that fluorine implantation could suppress the Ni diffusion but affect the NiGe formation at the same time. The reverse bias current of the junction with NiGe formation at 325 ^{o}C is reduced by nearly 3 orders of magnitude. But the reverse bias current still increases with the increase of the NiGe formation temperature.

The junctions with deeper junction depth were fabricated to examine whether the fast diffusion of Ni still damages the junction characteristic. The deep junction was formed by phosphorus ion implantation at 50 keV to a dose of $5x10^{13}$ cm^{-2} on heavily-doped substrate. The I-V curves are shown in Fig. 3-10. The forward current is about 10^{2} A/ cm^{2} and is nearly the same with the forward current of the IBG junctions. Furthermore, the reverse bias current is nearly 10^{-2} A/ cm^{2} and is lower than that of the IBG junction with phosphorus ion implantation at 20 keV to a dose of $1x10^{15}$ cm^{-2}. It could be inferred that high ion implantation dose may cause more defects than low ion implantation dose does, and more defects may let Ni diffuse faster so that the reverse bias current increases. Fig.3-10 also shows the I-V curves of the IBG junctions with fluorine ion implantation. In particular, the reverse bias current of the fluorine implanted junction is higher than that of the junction without fluorine

implantation and also increases with the increase of the NiGe formation temperature. It could be inferred that fluorine implantation causes additional defects than phosphorous implantation and these defects enhance Ni diffusion.

Next, the IBG junctions are also fabricated on lightly-doped substrate to observe whether the junction is still destroyed by Ni diffusion. Because different implantation doses might induce different amount of defects, the IBG junctions with different implantation doses were designed to observe the effect of Ni diffusion. Fig.3-11 shows the IBG junctions formed with phosphorus implantation at 20 keV to different doses on lightly-doped substrate. The forward current of the four IBG junctions increases with the increase of the ion implantation dose due to the different activated concentrations. However, the reverse bias current of the four IBG junctions are all about 10^{-1} A/cm^2 and do not increase with the ion implantation dose. This observation is not consistent with the IBG junctions on heavily-doped substrate. The cause could be inferred that the junction depth on lightly-doped substrate is deeper than that on heavily-doped substrate with the same ion implantation and activation conditions. The Ni diffusion is deep enough to destroy the IBG junction on heavily-doped substrate, but it is not deep enough to destroy the IBG junction on lightly-doped substrate. In addition, the forward current increases after NiGe formation due to the dopant segregation at the NiGe/Ge interface in comparison with Fig.3-5.

First-principle calculations were introduced to discuss the behaviors of the n-type dopant around the NiGe/Ge interface [81]. First, the realistic polycrystalline phases NiGe/Ge contact is built by including NiGe(112) phase only, so the NiGe/Ge contact is simulated by a supercell connecting 8 NiGe(112) layers, 16 Ge(001) layers, and 12Å -vacuum where the dangling bonds of the Ge surface are saturated by H atoms. Before exploring whether the n-type dopant such as P and As can be segregated and pile-up at the NiGe/Ge interface or not, the implanted dopant is assumed to be

activated and migrate into the substitutional sites. Therefore, one at a time of the Ge atoms around the interface is replaced by a doping atom in the NiGe/Ge interfacial structure and then the doped interfacial structure is relaxed by the DFT-LDA calculations until the forces are less than 0.01eV/Å for atoms within 9 Å from the interface, where the atoms beyond this region approach their corresponding bulk positions. The total energy of the system with one Ge atom being substituted for a P and As are shown in Fig. 3-12(a) and (b), respectively. The P and As dopant concentration here is equivalent to 8.34 x 10^{20} cm^{-3}.

The result in Fig. 3-12(a) shows that the P doping occurs most stably at the positions labeled as MG3 and SG1a. It implies that the P dopant can be segregated around the NiGe/Ge interface and piled up on the NiGe side. Nevertheless, the As atom prefers to stay on the Ge side near the interface as shown in Fig. 3-12(b) since the Ge-side doping of As is more stable than the NiGe-side. The most stable substitutional site for the As dopant is labeled as SG1c. To sum up, although both P and As dopants can be segregated around the NiGe/Ge interface in our calculations, the former prefer to pile up on the NiGe side but the latter like to stay on the Ge side around the interface.

Finally, IBG junctions formed by arsenic ion implantation at 30keV to a dose of $1x10^{13}$, $5x10^{13}$, and $1x10^{15}$ cm^{-2} on lightly-doped substrate are fabricated and the I-V curves are shown in Fig. 3-13. The poor junction characteristic is observed as the As dose is $1x10^{13}$ cm^{-2} because the activated dose cannot form good N^{+}/P junction. The IBG junctions formed with arsenic ion implantation to a dose of $5x10^{13}$ and $1x10^{15}$ cm^{-2} have better junction characteristic. The forward current also increases after NiGe formation due to dopant segregation. Therefore, the dopant segregation effect could be observed by As implantation as well, and the forward current is slightly lower than the IBG junctions formed by P implantation due to the low activation rate of As.

3.4 NiGe Dopant Segregation Junctions

Fig. 3-14 shows the I-V curves of the IAG junctions with different annealing temperatures. Very poor junction characteristics are observed on all IAG junctions. One reason may be the segregated n^+ layer is too thin to maintain good N^+/P junction. The other possible reason is that because Ni diffuses much faster than arsenic, the distribution of Ni would be much deeper than arsenic. Therefore, using IAG process to get a good shallow junction is very difficult. In addition, cross-sectional TEM micrographs of the NiGe/Ge structure with IAG process after annealing at 500°C and 550°C for 10 sec are shown in Fig.3-15. The highest sustainable temperature of the NiGe/Ni structure is 500 °C. This temperature is also the highest allowable temperature for the IAG process.

In order to maintain good junction characteristic, a low energy phosphorus ion implantation was performed before NiGe formation followed by the IAG process. It is called the IBG+IAG junction. The I-V curve of the IBG+IAG junction with 500 °C annealing is shown in Fig. 3-16. Comparing the IBG+IAG junction and the Al-contacted conventional junction, the IBG process steps form a good 100-nm-deep shallow junction (Fig. 3-18) while the IAG process improves the turn-on characteristic. Furthermore, the NiGe formation process does not degrade leakage current.

3.5 Contact resistance of IBG+IAG junctions

First-principles calculations were used to calculate the total energy of the NiGe/Ge structure. Replacing Ge atom by P or As atom, Fig. 3-12 shows the total energy of the NiGe/Ge structure as a function of the dopant position. Either P or As

atom may segregate at the NiGe/Ge interface, however, the most stable segregation position for P is at the NiGe side and the most stable segregation position for As is at the germanium side. These results imply that NiGe formation would reduce the contact resistance on the P- doped and As-doped junctions (IBG process) while As would be a better choice for the implantation after NiGe process (IAG process). Therefore, IBG process is preferred for the P-doped junction due to P has higher activation concentration than As and IAG process is preferred for the As-doped junction due to the lowest total energy at the interface. The contact resistance would reduce by virtue of the two times dopants segregation.

Cumulative distribution of contact resistivity extracted by the CBKR structure is shown in Fig.3-17. The contact resistivity of the Al-contacted conventional junction is as high as 10^{-4} Ω-cm^2, because the Fermi-level pinning near valance band at the interface. In addition, the SIMS analysis shows the junction depth is about 125 nm in Fig. 3-18. After the IBG process, the contact resistivity is reduced to $2x10^{-5}$ Ω-cm^2. According to the SIMS analysis shown in Fig. 3-19, there is a peak concentration at the NiGe/Ge interface as a result of P segregation. This observation is consistent with first-principle calculations and also consistent with the I-V characteristics shownin Chapter 3. In order to further reduce the contact resistance, IAG process is perfromed following the IBG process. Similar to the P segegation at the interface in the IBG process, As atoms in NiGe also prefer to segregate at the interface in the IAG process and the pile-up of the dopant concentration can reduce contact resistance. According to Fig.3-17, the lowest contact resistance is $2x10^{-6}$ Ω-cm^2. However, the SIMS depth profile shown in Fig.3-20 does not reveal peak concentration of As at theNiGe/Ge interface, because the NiGe film is a little rough to affect the analysis of SIMS. In addition, the contact resistance of IBG+IAG junction with fluorine implantation before NiGe formation is also shown in Fig.3-17. The contact resistance has tighter

distribution than that of the IBG+IAG junctions without flourine implantation. According to the previous study, the roughness of NiGe film can be obviously improved using the AFP method. Therefore, the tighter distribution could be attributed to the better roughness of the NiGe/Ge interface with fluorine implantation before NiGe formation. Furthermore, the junction depth increased to 150 nm due to the second high temperature annealing. In addition, according to the I-V curve in Fig. 3-16, the IBG+IAG junction would have lower leakage current and keep origin junction characteristics. Therefore, compared with previous studies in Table 3-1, the IBG+IAG process could achieve lower contact resistance, lower leakage current, and shallower junction depth.

3.6 Summary of IBG and IAG junctions

At first, in order to reduce thermal budget, NiGe formation temperature and time are tested by measuring the sheet resistance. The most appropriate recipe is formation at 350 ^{o}C for 5 minutes.

Next, the IBG junctions are discussed. On heavily-doped substrate, very poor junction characteristic is observed by high dose phosphorous ion implantation due to the fast diffusion of Ni by virtue of defects which are generated by ion implantation. Fluorine ion implantation before NiGe formation could effectively suppress Ni diffusion and reduce the leakage current. Moreover, better junction characteristic was observed by ion implantation to a low dose due to the less defects resulting in less Ni diffusion. However, fluorine implantation before NiGe formation would enhance the Ni diffusion to degrade junction characteristic because the fluorine ion implantation induces extra defects.

On lightly-doped substrate, good junction characteristic is more easily to be

obtained than on heavily-doped substrate because the deeper junction depth on lightly-doped substrate so that the Ni diffusion would not destroy the junctions. In particular, after NiGe formation, the forward current obvious increases owing to the dopant segregation at the NiGe/Ge interface. Furthermore, either phosphorous or arsenic n^+/p junction would have the dopant segregation effect. And the arsenic n^+/p junctions have relatively low activation concentration inferred by the I-V characteristic.

Finally, because the IAG junctions have poor junction characteristic due to the segregated n^+ layer is too thin to maintain good n-p junction and the Ni fast diffusion induces large leakage current, the IBG+IAG junctions were fabricated. The IBG+IAG junction could achieve shallow junction depth and raise the forward current at the same time.

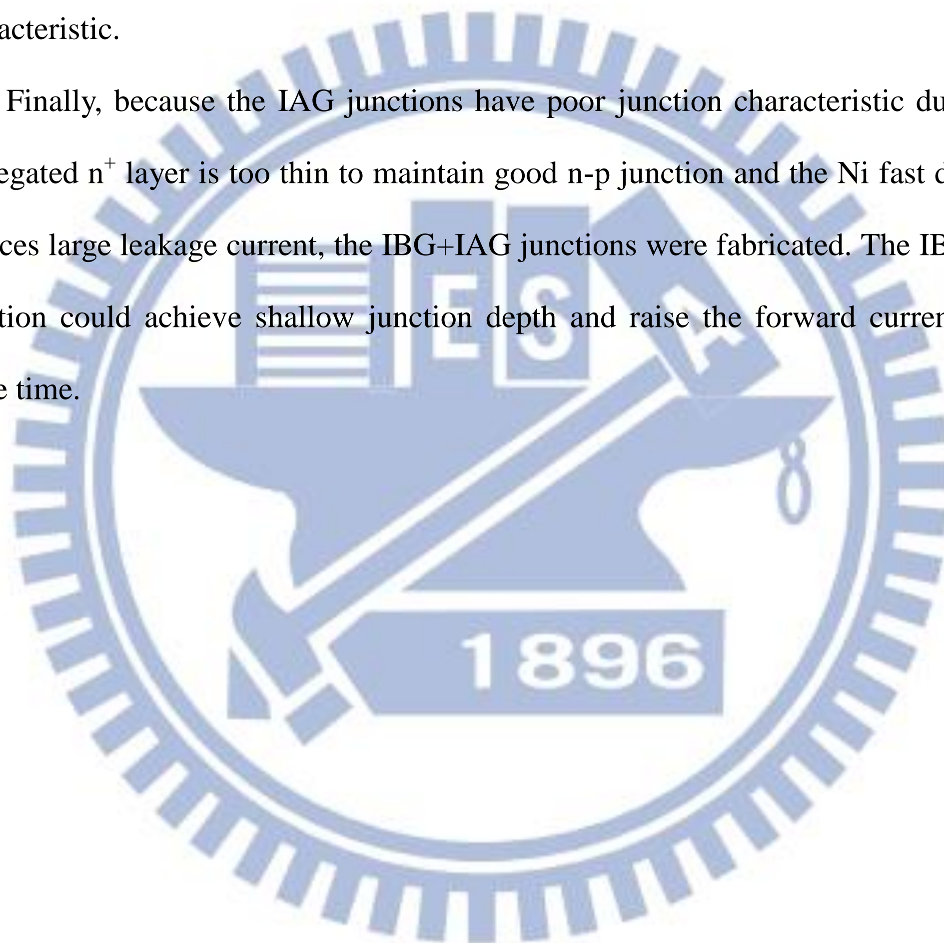


Table 3-1 Correction factor of samples with different shape or size[80].

CF1(d/s)	Circle	Square	Rectangle L/W=2	Rectangle L/W=3	Rectangle L/W=4
1.0				0.9988	0.9904
1.25				1.2467	1.2248
1.5			1.4788	1.4893	1.4893
1.75			1.7196	1.7238	1.7238
2.0			1.9475	1.9475	1.9475
2.5			2.3532	2.3541	2.3541
3.0	2.2662	2.4575	2.7000	2.7005	2.7005
4.0	2.9289	3.1127	3.2246	3.2248	3.2248
5.0	3.3625	3.5098	3.5749	3.5750	3.5750
7.5	3.9273	4.0095	4.0361	4.0362	4.0362
10.0	4.1716	4.2209	4.2357	4.2357	4.2357
15.0	4.3646	4.3882	4.3947	4.3947	4.3947
20.0	4.4364	4.4516	4.4553	4.4553	4.4553
32.0	4.4791	4.4878	4.4899	4.4899	4.4899
40.0	4.5076	4.5120	4.5129	4.5129	4.5129
Infinity	4.5324	4.5324	4.5324	4.5324	4.5324

Table 3-2 Metal/n-Ge contact resistance recorded by previous studies.

Contact	Doping	Activation	Test Structure	Contact Resistivity (Ω-cm^2)	Junction Depth (nm)	Source
NiGe	P+Sb IBG	500°C/RTA	CTLM	$5.5x10^{-7}$	200	[27]
NiGe	As IBG	900°C/LSA	CTLM	$1.4x10^{-6}$	N.A.	[25]
NiGe	As IBG	800°C/LSA	CTLM	$5.0x10^{-5}$	30	[25]
NiGe	P IBG	500°C/FA	TLM	$8.8x10^{-5}$	N.A.	[68]
$NiGe_x$	P IBG	500°C/FA	TLM	$3.5x10^{-6}$	N.A.	[68]
Al	P-epi	None	CTLM	$4.6x10^{-5}$	N.A.	[25]
Ti	As I/I	600°C/RTA	CTLM	$1.0x10^{-3}$	N.A.	[25]
Ti	P I/I	650°C/N.A.	CTLM	$4.9x10^{-5}$	N.A.	[66]
TaN	P I/I	650°C/N.A.	CTLM	$2.7x10^{-5}$	300	[26]
NiGe	**P IBG + As IAG**	**500°C/RTA**	**CBKR**	**$2x10^{-6}$**	**150**	**This work**

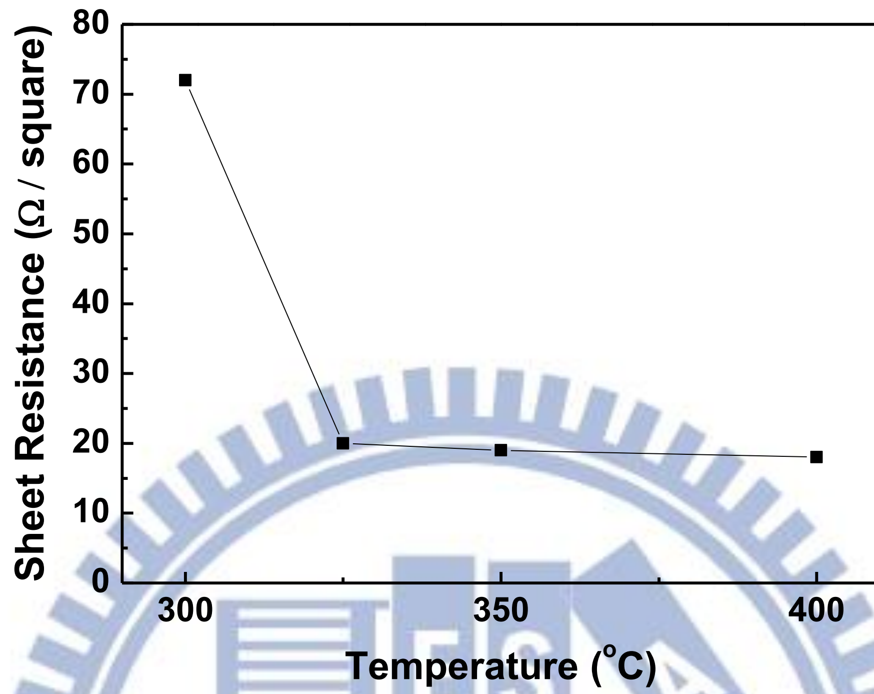


Fig.3-1 Sheet resistance as a function of annealing temperatures for 5 minutes of NiGe formation.

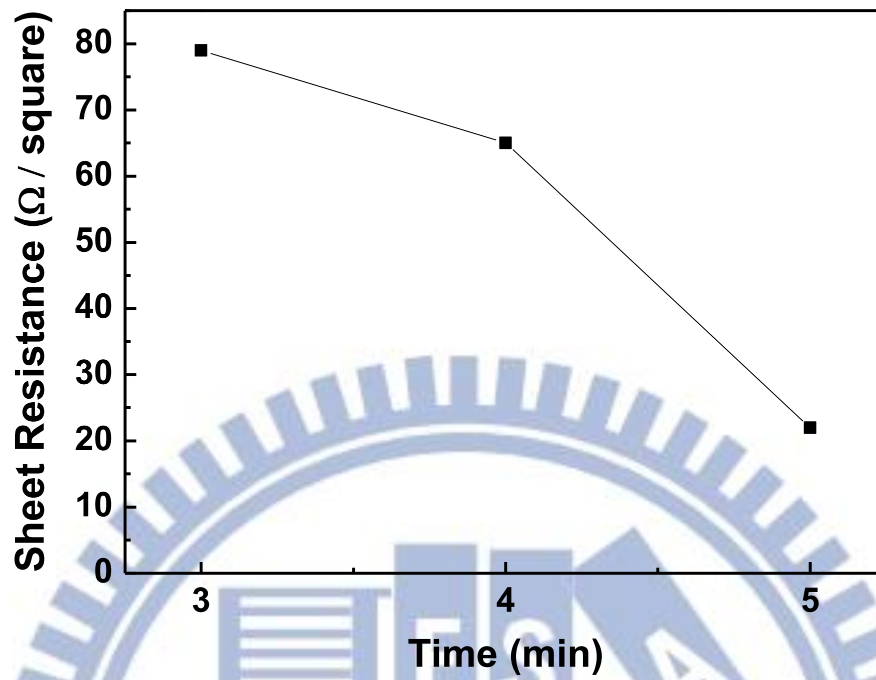


Fig.3-2 Sheet resistance as a function of annealing times at 350°C of NiGe formation.

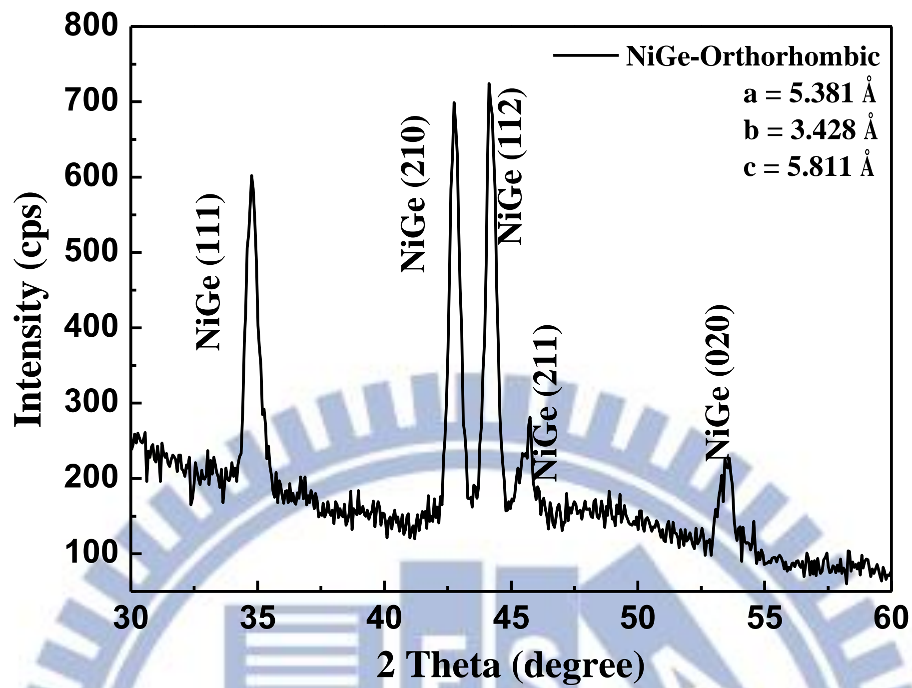


Fig.3-3 X-ray diffraction spectrum of the NiGe/Ge structure formed by 350°C annealing shows polycrystal NiGe phases.

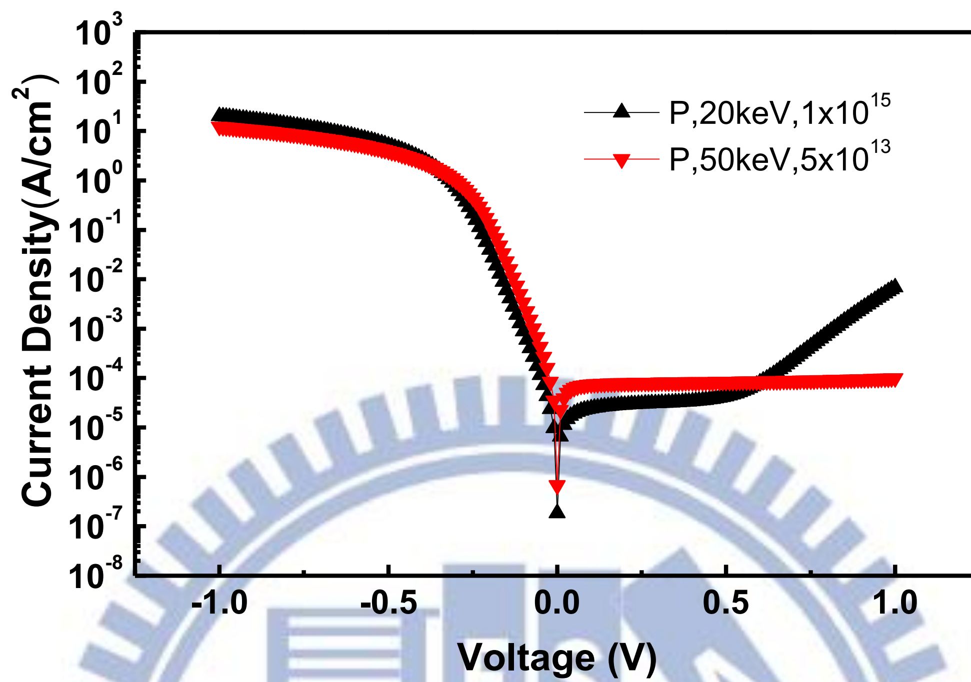


Fig.3-4 Current-voltage curve of conventional junctions of implantation by phosphorus at 20keV to a dose of $1x10^{15}$ cm^{-2} and 50keV to a dose of $5x10^{13}$ cm^{-2} and activation at 600^oC for 60 seconds on heavily-doped substrate.

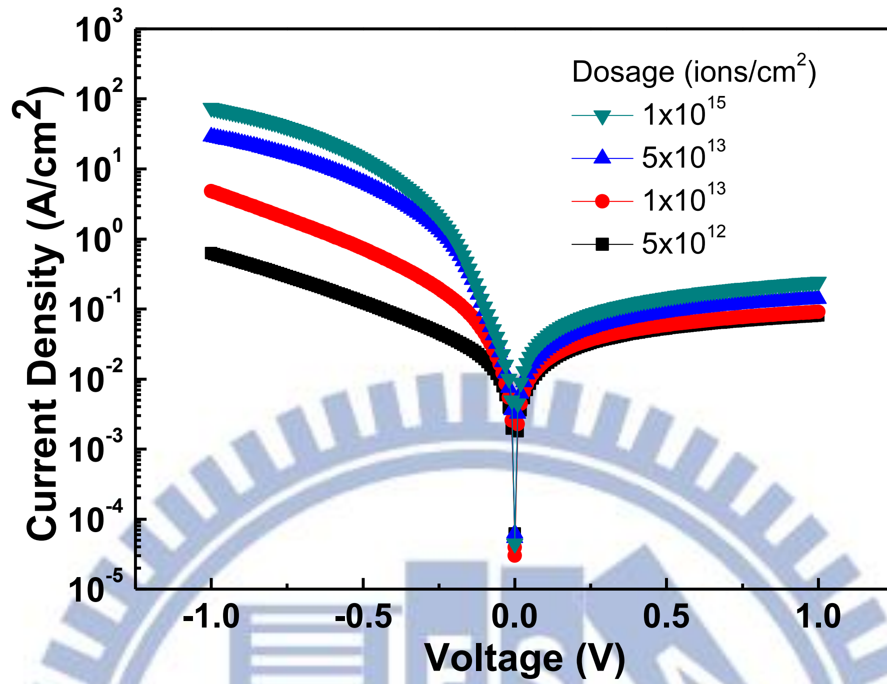


Fig.3-5 Current-voltage curve of conventional junctions of implantation by phosphorus at 50keV to a dose of $1x10^{15}$, $5x10^{13}$, $1x10^{13}$, $5x10^{12}$ cm^{-2} and activation at 600°C for 60 seconds in lightly-doped substrate.

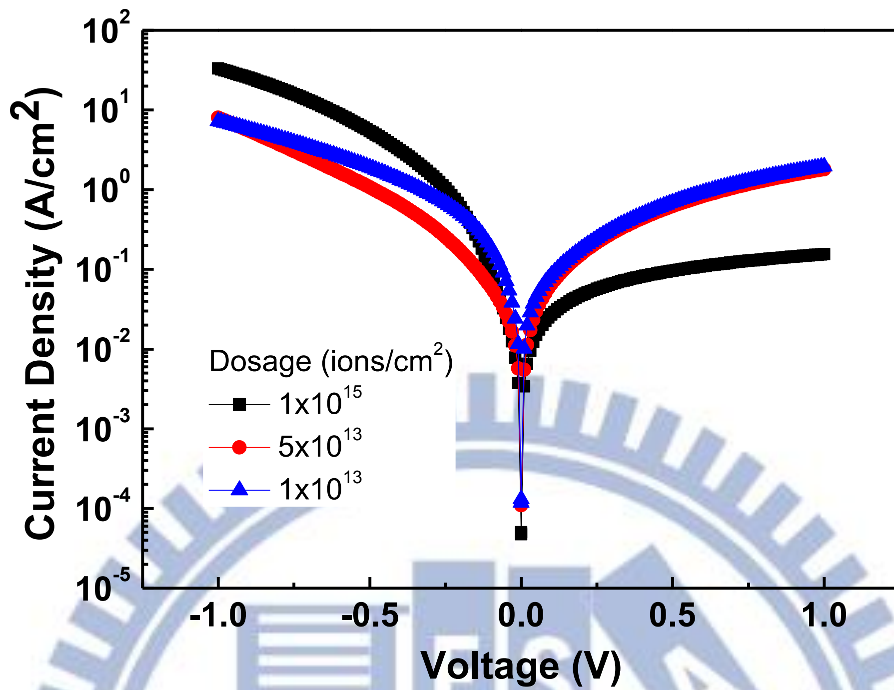


Fig.3-6 Current-voltage of conventional junctions of implantation by arsenic at 30keV to a dose of $1x10^{15}$, $5x10^{13}$, $1x10^{13}$ cm^{-2} and activation at 600°C for 60 seconds in lightly-doped substrate.

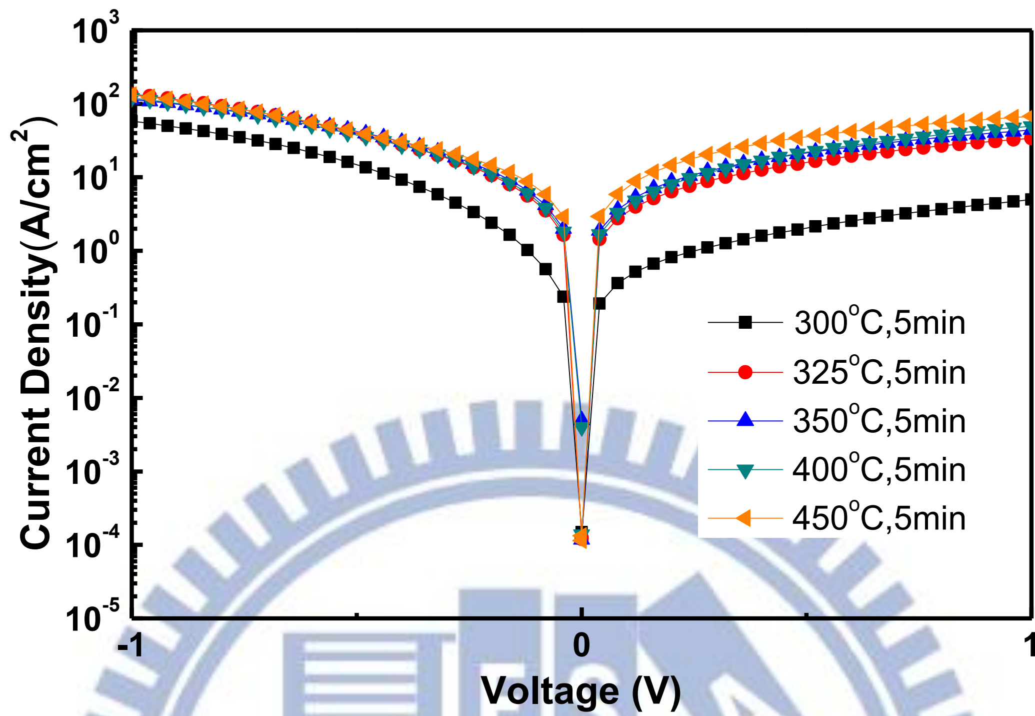


Fig.3-7 Current-voltage curves of IBG junctions forming with different formation temperature of implantation by phosphorus at 20keV to a dose of $1x10^{15}$ cm^{-2} and activation at 600°C for 60 seconds on heavily-doped substrate.

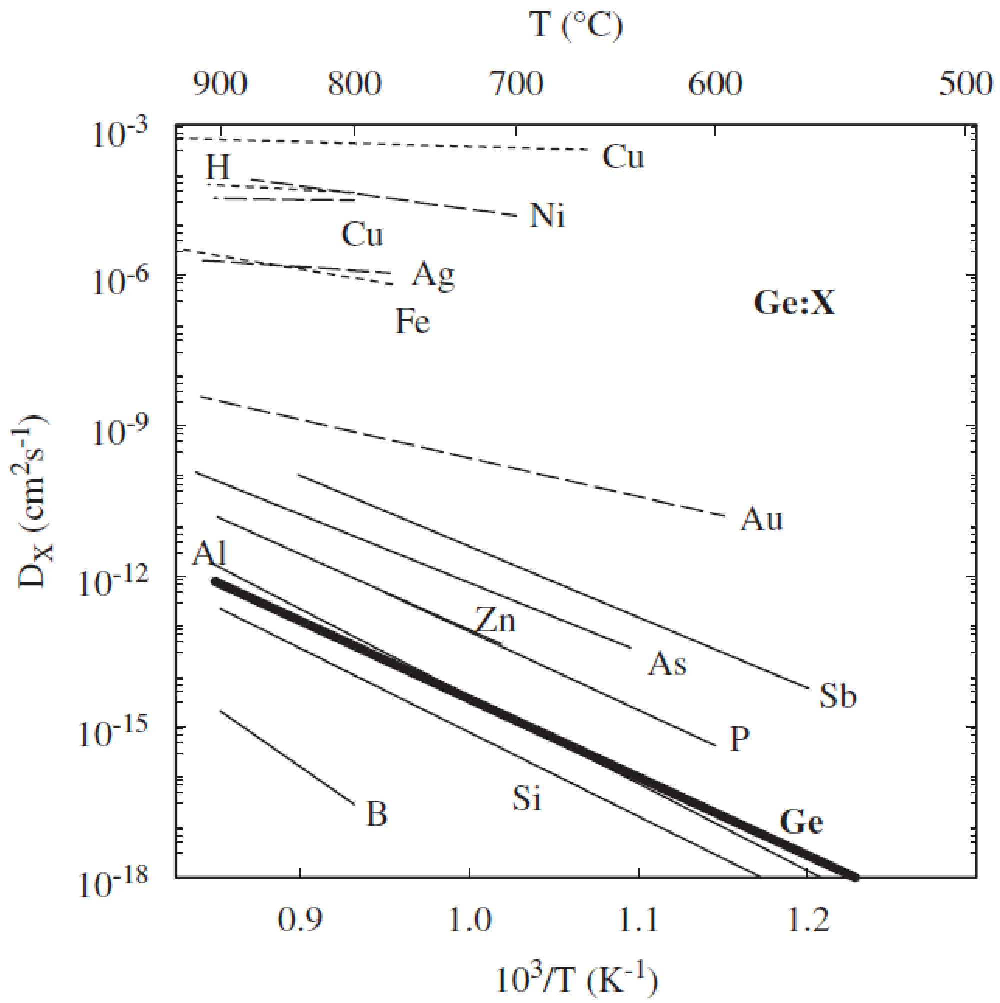


Fig.3-8 Diffusivity of elements in Ge [78].

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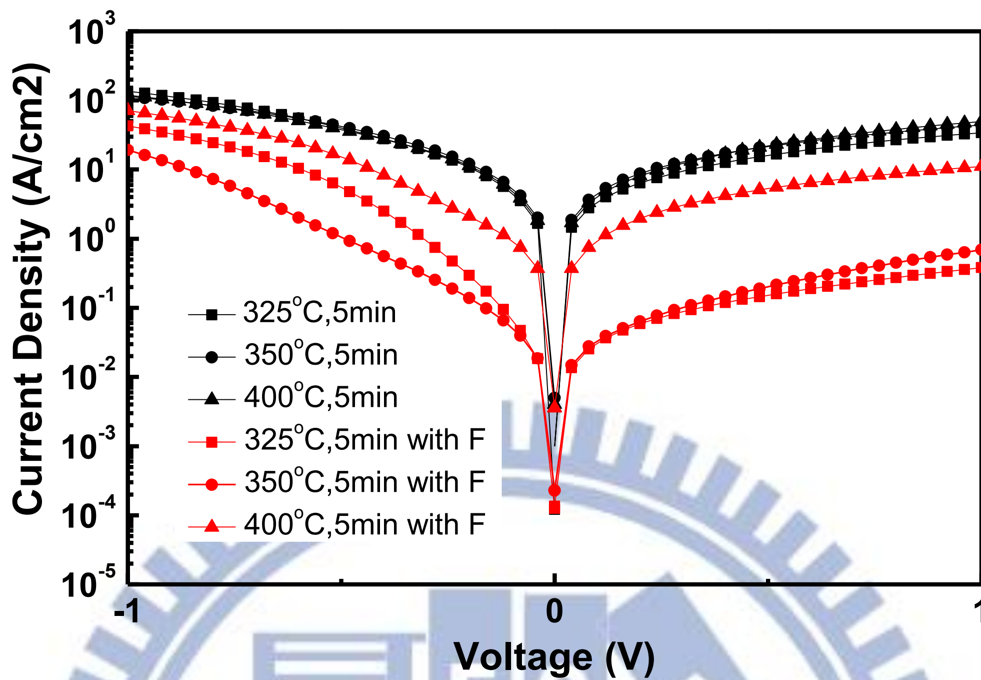


Fig.3-9 Current-voltage curves of fluorine implantation before NiGe formation and IBG junctions with different formation temperature of implantation by phosphorus at 20keV to a dose of $1x10^{15}$ cm^{-2} and activation at $600^{o}C$ for 60 seconds in heavily-doped substrate. The fluorine implantation is at 10keV to a dose of $1x10^{15}$ cm^{-2}.

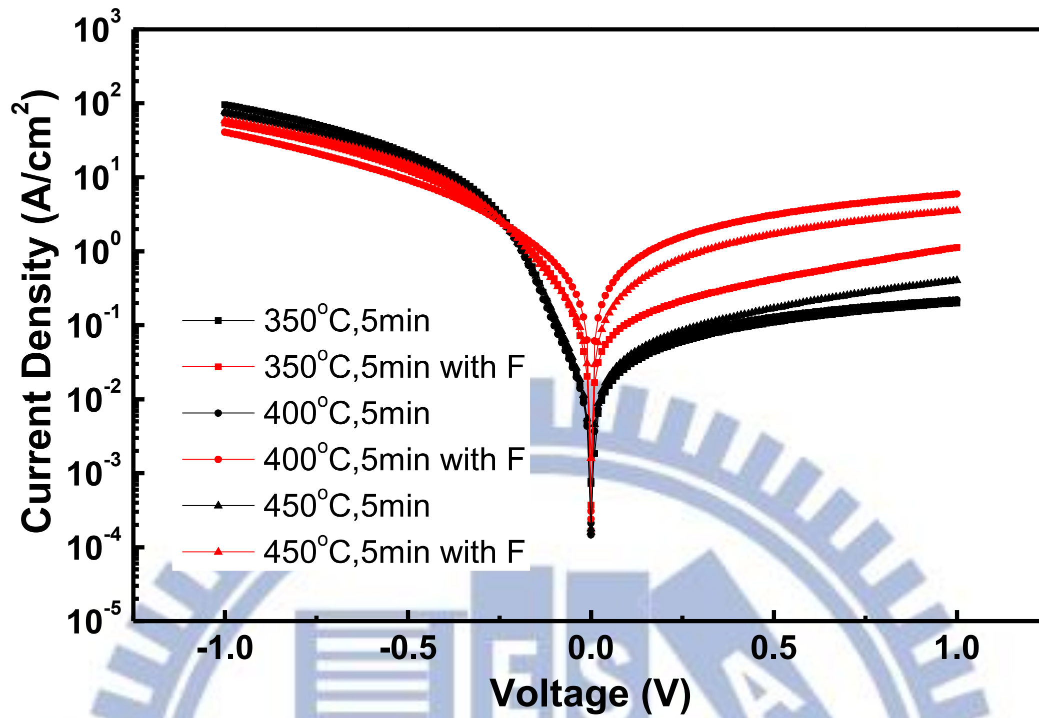


Fig.3-10 Current-voltage curves of fluorine implantation before NiGe formation and IBG junctions with different formation temperature implantation by phosphorus at 50keV to a dose of $5x10^{13}$ cm^{-2} and activation at 600^oC for 60 seconds in heavily-doped substrate. The fluorine implantation is at 10keV to a dose of $1x10^{15}$ cm^{-2}.

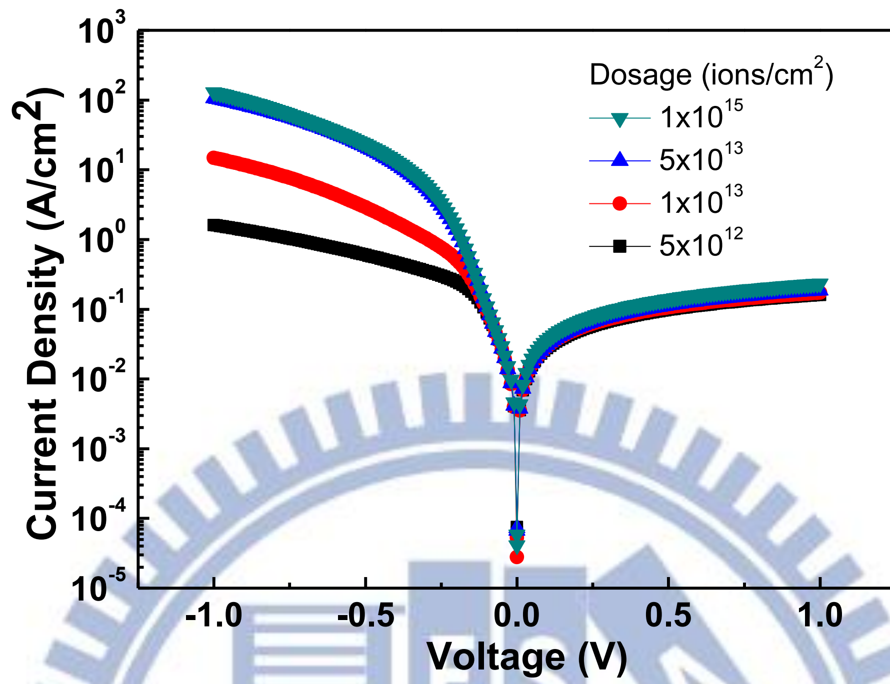
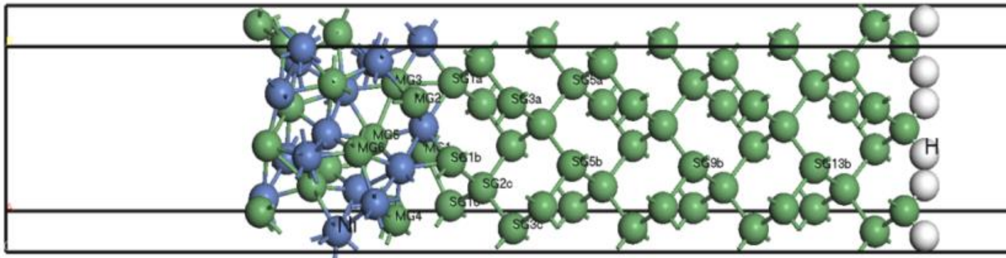
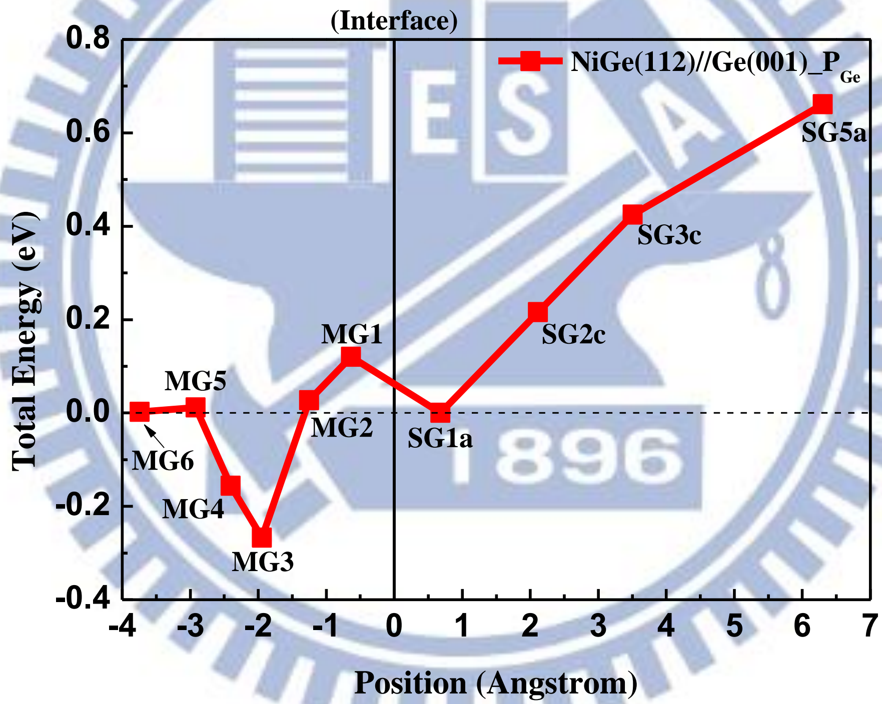
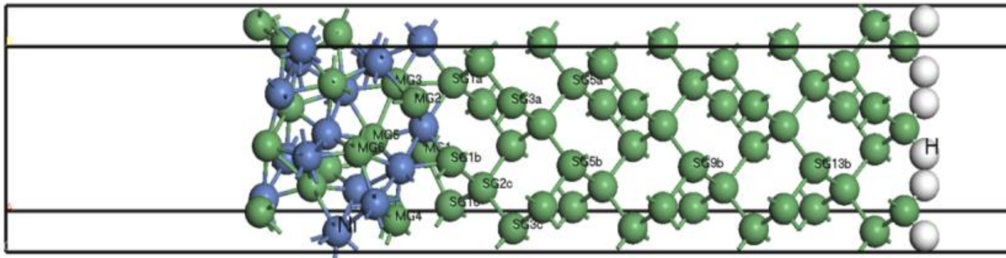


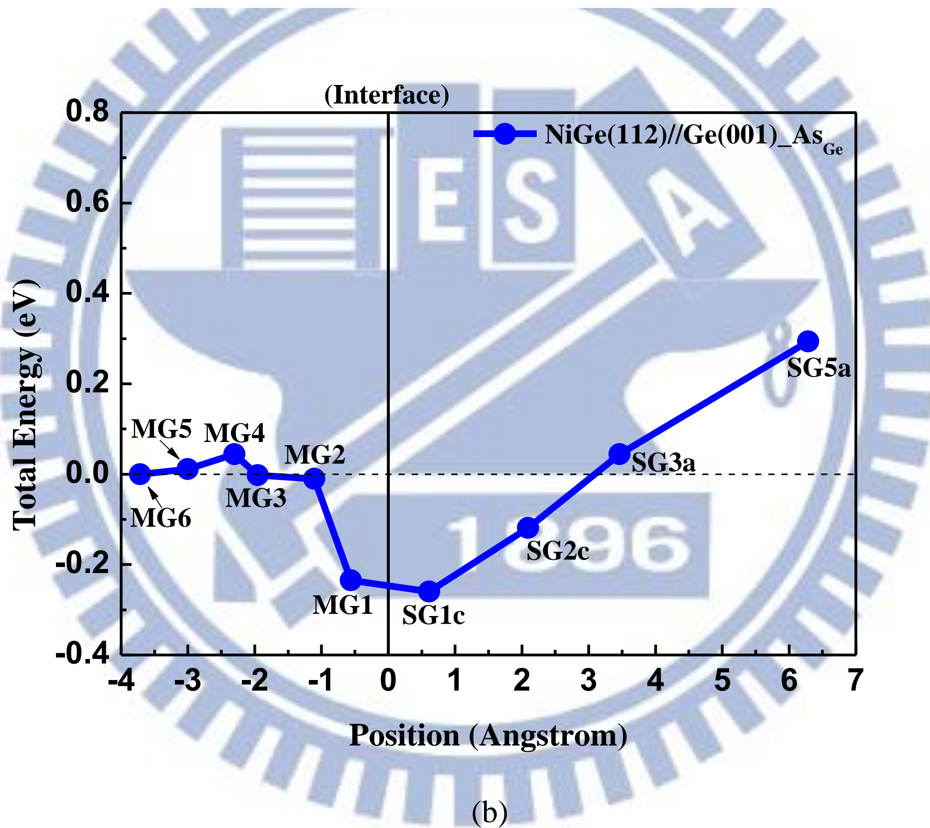
Fig.3-11 Current-voltage curve of IBG junctions of implantation by phosphorus at 50keV to a dose of $1x10^{15}$, $5x10^{13}$, $1x10^{13}$, $5x10^{12}$ cm^{-2} and activation at 600°C for 60 seconds in lightly-doped substrate.





(a)





(b)

Fig.3-12 Total energy of the interfacial structure as a function of the dopant position. One of the Ge atoms is replaced by (a) P atom and (b) As atom.

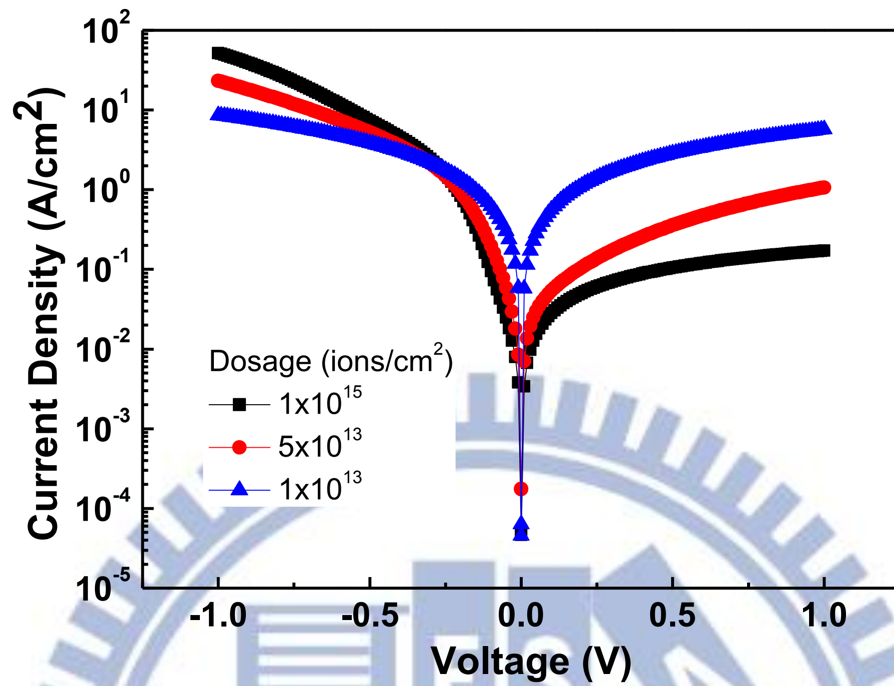


Fig.3-13 Current-voltage curves of IBG junctions forming with implantation by arsenic at 30keV to different dose and activation at 600°C for 60 seconds on lightly-doped substrate.

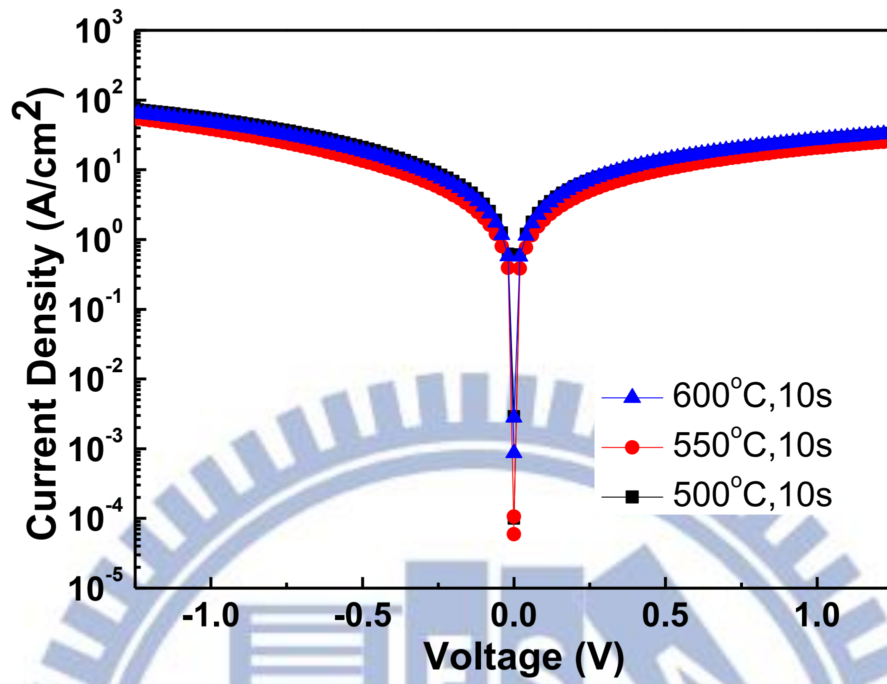
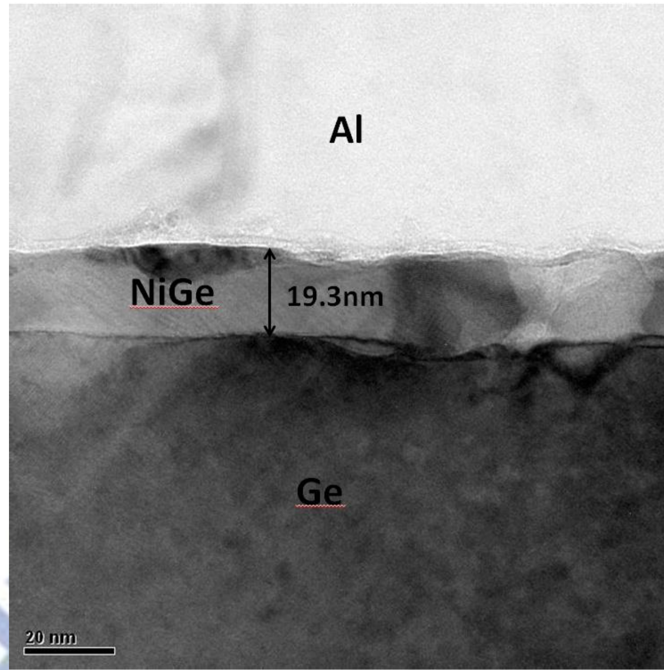
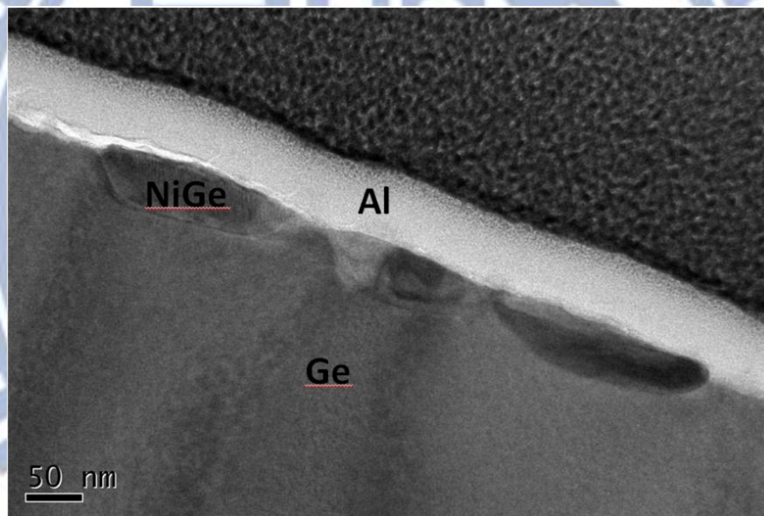


Fig.3-14 Current-voltage curves of IAG junctions with implantation by arsenic at 10keV to a dose of $1x10^{15}$ cm^{-2} with different annealing temperature.



(a)



(b)

Fig.3-15 Cross-sectional TEM micrography of the NiGe/Ge structure with IAG process after annealing at (a) 500°C and (b) 550°C for 10 sec.

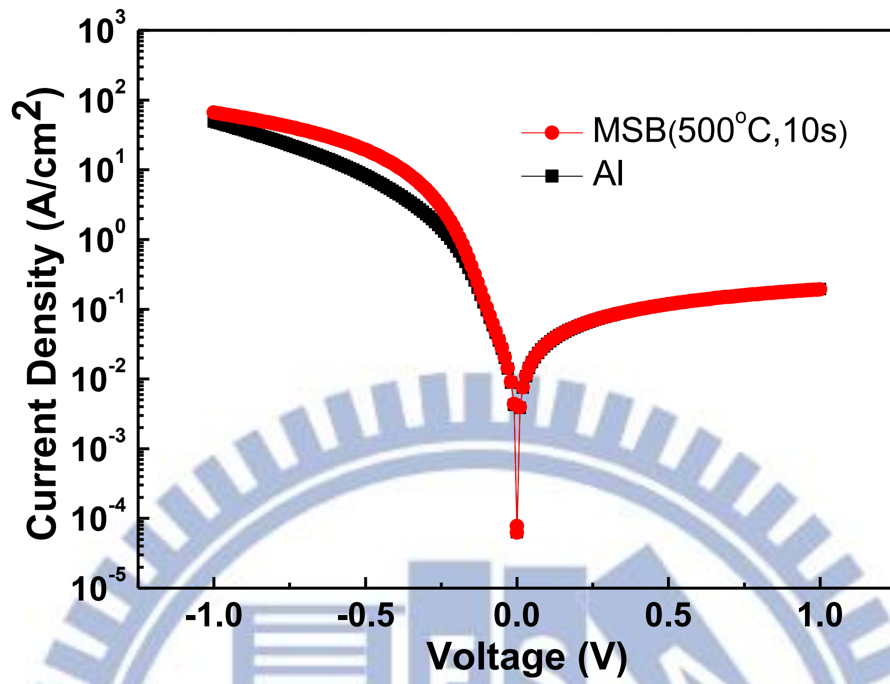


Fig.3-16 Current-voltage curve of IBG (phosphorus at 20keV to a dose of $1x10^{15}$ cm^{-2} and activation at 600°C for 10 seconds) + IAG(arsenic at 10keV to a dose of $1x10^{15}$ cm^{-2}) junction with 500°C for 10 seconds annealing.

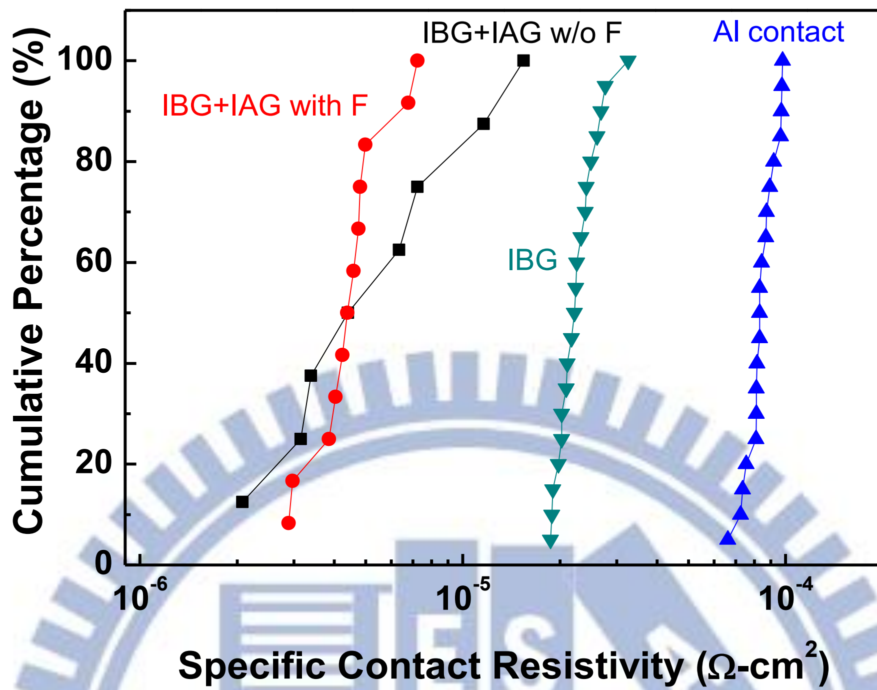


Fig.3-17 Cumulative distribution of contact resistivity extracted by the CBKR structure. The contact areas are 10x10, 5x5 and 3x3 um^2.

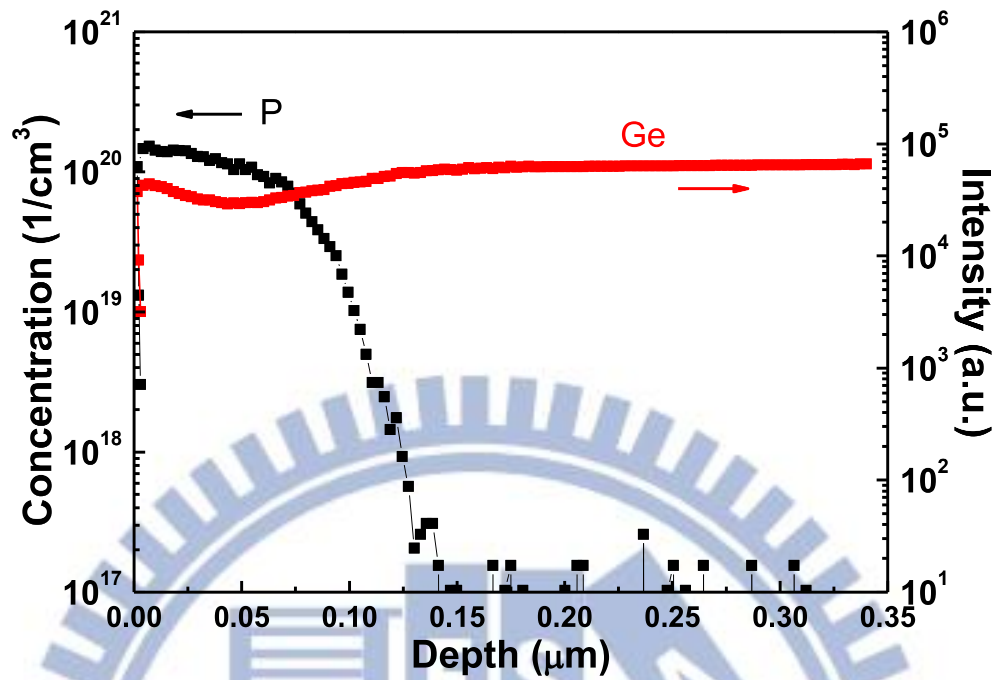


Fig.3-18 Secondary ion mass spectrometer depth profiles of the conventional junction of implantation by phosphorus at 20keV to a dose of $1x10^{15}$ cm^{-2} and activation at 600^oC for 10 seconds on lightly-doped substrate.

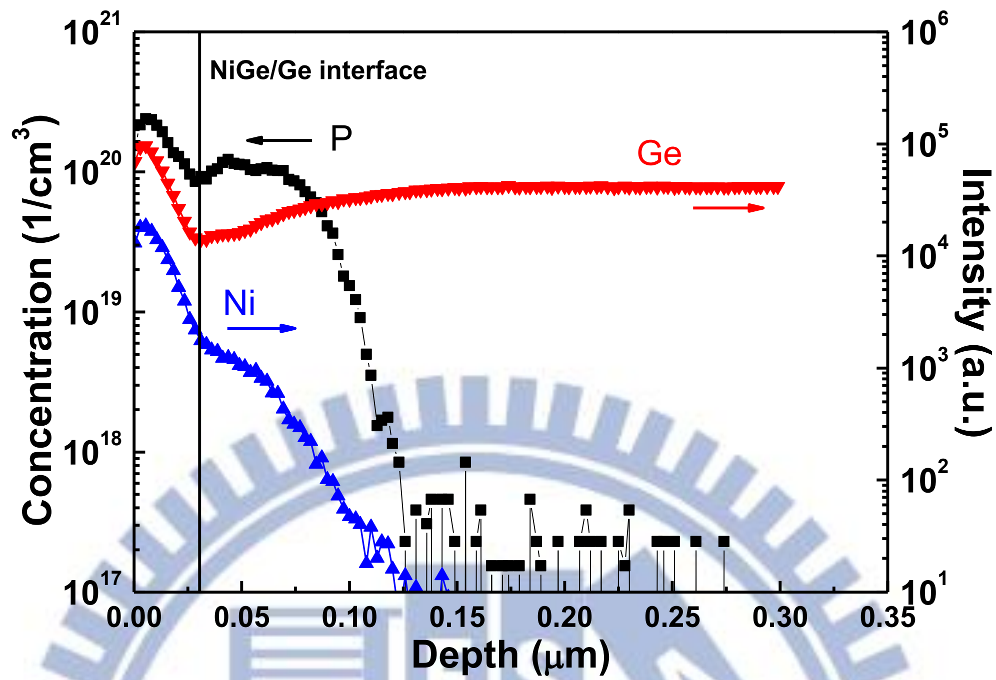


Fig.3-19 Secondary ion mass spectrometer depth profiles of the NiGe-contacted junction formed by the IBG process of implantation by phosphorus at 20keV to a dose of $1x10^{15}$ cm^{-2} and activation at $600^{o}C$ for 10 seconds on lightly-doped substrate.

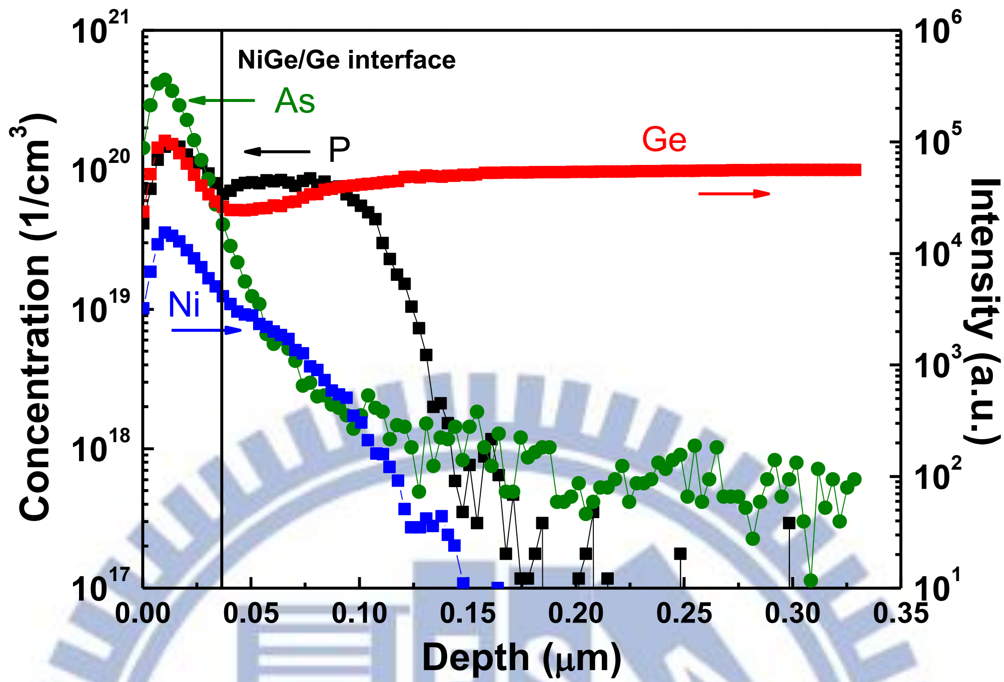


Fig.3-20 Secondary ion mass spectrometer depth profiles of the NiGe-contacted junction formed by the IBG (implantation by phosphorus at 20keV to a dose of $1x10^{15}$ cm^{-2} and activation at 600°C for 10 seconds) + IAG (implantation by arsenic at 10keV to a dose of $1x10^{15}$ cm^{-2} and annealing at 500°C and 10 seconds).

Chapter 4
Conclusions and Future Works

4.1 Conclusions

In the thesis, the thermal budget for NiGe formation is studied firstly. It is concluded that a 350 ^{o}C annealing for 5 minutes ensures that NiGe could completely form. The highest process temperature is limited to 500 °C. Beyond that, agglomeration of the NiGe film occurs. In additon, the main NiGe crystal orientations are (2 1 0), (1 1 2), and (1 1 1) identified by XRD diffraction.

For the Al-contacted conventional junctions, good junction characteristic can be achieved on either heavily-doped or lightly-doped substrate. In particular, band-to-band tunneling can also be observed on the high doping concentration N^+/P junction on heavily-doped substrate. Because the lower concentration of substrate would cause the wider depletion width, and the wider depletion width would cause the higher reverse bias current, therefore, the reverse bias current on lightly-doped substrate is higher than that on heavily-doped substrate. Besides, the reverse bias current of the arsenic implanted junction is higher than that of the phosphorus implanted junction because the activation ratio of arsenic is relatively lower than that of phosphorus so that the junction depth of the arsenic implanted junction is shallower. Furthermore, the heavier arsenic atom would generate more defects than the lighter phosphorous atom. Therefore, the reverse bias current of the arsenic implanted junction is higher.

To evaluate the feasibility of the self-aligned metal germanide process, NiGe-contacted junctions are investigated. On heavily-doped substrate, very poor

junction characteristic is observed by high dose phosphorous ion implantation due to the fast diffusion of Ni by virtue of defects which are generated by ion implantation. Fluorine ion implantation before NiGe formation could effectively suppress Ni diffusion and reduce the leakage current. Better junction characteristic is observed by ion implantation to a lower dose due to less defects resulting in less Ni diffusion. However, fluorine implantation before NiGe formation would enhance the Ni diffusion to degrade junction characteristic because the fluorine ion implantation induces extra defects. On the other hand, good junction characteristic is more easily to be obtained on lightly-doped substrate than on heavily-doped substrate because the deeper junction depth on lightly-doped substrate so that the Ni diffusion would not destroy the junctions. In particular, after NiGe formation, the forward current increases obviously, in comparison with the Al-contacted junction, owing to the dopant segregation at the NiGe/Ge interface. The IBG junction with ion implantation to a lower dose has a higher degree of forward current improvement. Furthermore, either phosphorous or arsenic n^+/p junction would have the dopant segregation effect, and the arsenic n^+/p junctions have relatively low activation concentration inferred by the I-V characteristic.

The IAG junctions have poor junction characteristic due to the segregated n^+ layer is too thin to maintain good n-p junction and the Ni fast diffusion induces large leakage current. The IBG+IAG junction could achieve shallow junction depth and raise the forward current at the same time. On the bases of first-principles calculations, NiGe formation would reduce the contact resistance on the P- doped and As-doped junctions (IBG process) while As would be a better choice for the implantation after NiGe process (IAG process). The measured NiGe/n-Ge contact resistance of the IBG process is about $2\text{x}10^{-5}$ Ω-cm^2 and the lowest contact resistance of the IBG+IAG process is $2\text{x}10^{-6}$ Ω-cm^2.

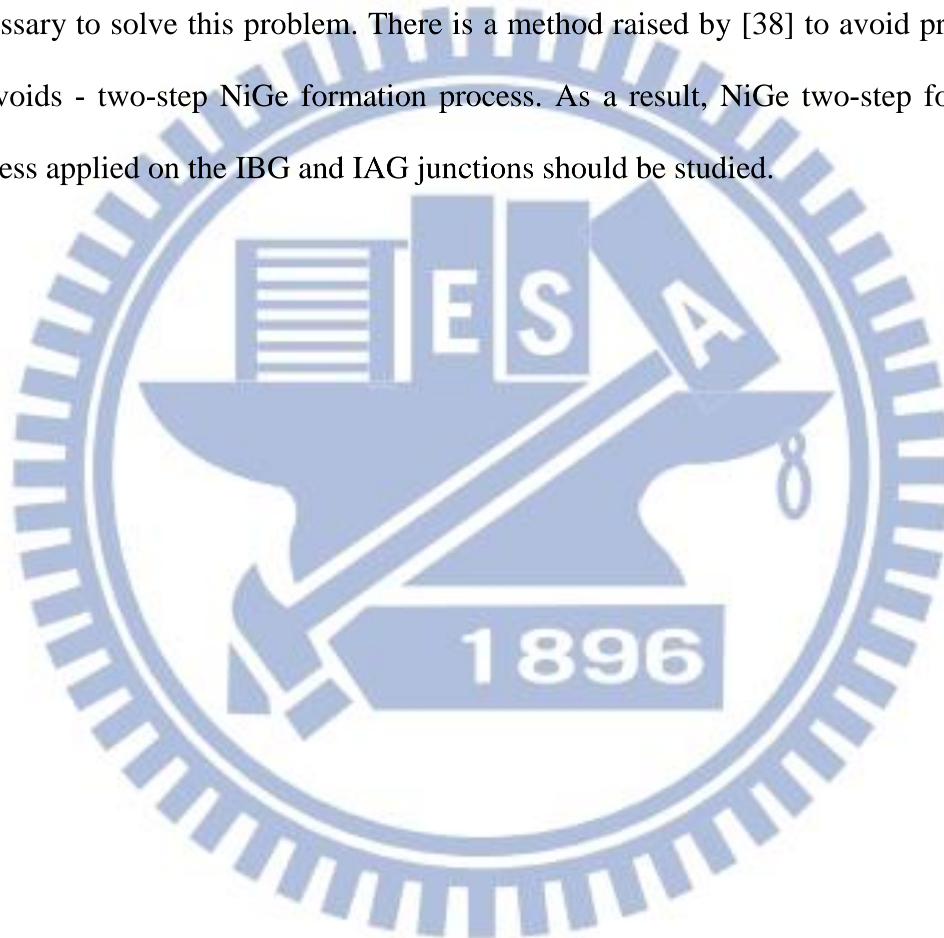
To sum up, the thesis proposed that the IBG junctions would be destroyed by Ni fast diffusion which depends on the amount of defects, and the dopant segregation effect could reduce the contact resistance. The IBG+IAG process can form a junction with shallower junction depth, lower leakage current, and lower contact resistance in comparison with previous studies.

4.2 Future Works

In this thesis, dopant diffusion, dopant diffusion due to defects, Ni diffusion, and Ni diffusion due to defects and the mechanism of Ni diffusion are all necessary to be proved by SIMS analysis or other material analysis. Dopant diffusion model in Ge should be investigated thoroughly. Furthermore, the XRD analysis of NiGe after IBG and IAG process and the interaction between Ni and F to affect Ni diffusion also need to be done. Because F implantation may cause additional defects, CF_4 plasma treatment could be studied to suppress Ni diffusion without implantation damage. In addition, although a low contact resistance has been achieved by IBG+IAG process, the contact resistance may be further reduced by improving the processes. At first, the implantation dosage of the IAG process can be raised to $3x10^{15}$ or $5x10^{15}$ to observe whether more dopants can segregate at the interface to form a higher concentration n^+ layer to achieve lower contact resistance. Secondly, increasing the annealing time of the IAG process may also be another way to let more dopants segregate. Thirdly, whether forming other metal germanide or implanting other dopants could segregate more at the interface to reduce contact resistance need to be studied. Furthermore, improving the thermal stability of NiGe to enhance the segregation effect should also be studied. After all the processes are optimized, short channel Ge NMOSFET integrated the IBG+IAG S/D junctions should be fabricated in order to verify the

improvement on real MOSFETs.

However, previous research [38] shows that germanide overgrows over the SiO_2 isolation by one-step high temperature annealing (330^oC) and germanium voids left around the corner of isolation. This phenomenon could also be observed in the thesis as shown in Fig. 4-1. If the junctions are applied on Ge MOSFET, the voids would interrupt the connection between S/D and the inverted channel. Therefore, it is necessary to solve this problem. There is a method raised by [38] to avoid producing the voids - two-step NiGe formation process. As a result, NiGe two-step formation process applied on the IBG and IAG junctions should be studied.



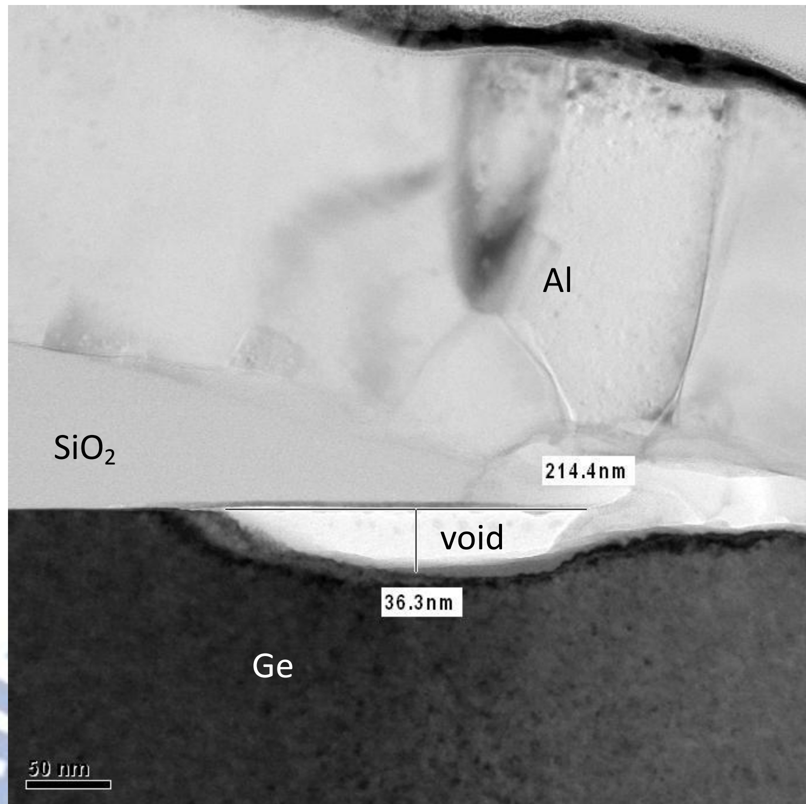


Fig.4-1 Cross-sectional TEM micrography of the NiGe/Ge structure at the junction edge.

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