1-V Linear CMOS Transconductor with -65 dB THD in Nano-Scale CMOS Technology

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Abstract—**This paper presents a high linearity MOSFET-only transconductor based on differential structures. The linearity is improved by mobility compensation techniques as the device size is scaled down in the nano-scale CMOS technology. Transconductance tuning could be achieved by transistors operating in the linear region. The simulated total harmonic distortion (THD) under 1-V power supply voltage shows 12 dB improvement of the proposed version, and -65 dB THD can be achieved for a 1 MHz 700 mV$_{pp}$ differential input. Monte-Carlo simulation over the corner variation and transistor mismatch guarantees the shown performance. The static power consumption is 130 μW. Simulation results demonstrate the agreement with theoretical analyses.**

I. INTRODUCTION

The transconductor is an important building block in the analog signal processing circuits, such as analog filters, data converters, voltage controlled oscillators, and multipliers [1-5]. The main function of the transconductor is to convert the voltage applied to the input terminals into current at output nodes, and the building block is generally referred as a V-I converter [6]. Usually, the linearity of the voltage-to-current conversion should be maintained. This is because that the linearity of the transconductor would determine the linearity of the overall system. However, this feature is hard to achieve, especially in the low supply voltage. In addition, the other requirement of the transconductor is the electronically tuning ability to resist the variation of the fabrication process and temperature.

In recent years, numerous of linearization techniques have been designed and reported [7]. The passive resistor, which is often implemented by the poly-silicon in the CMOS process, would be used in the high linearity transconductor circuit. Unfortunately, the use of passive resistors would cost more area, and it would also be affected by fabrication and temperature variation. The lack of electronically tuning ability of the passive resistor can be solved by using the resistor array, but it would encounter the accuracy problem while costing excessive areas and parasitic capacitors. Therefore, the transconductors with MOSFET-only configuration was developed and reported [8]. In such a configuration, the linearity of such an architecture is limited
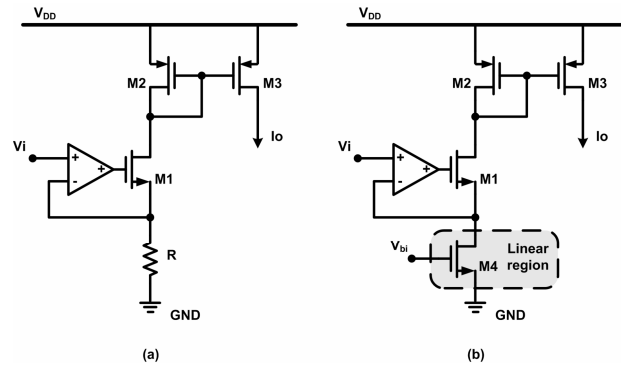

Figure 1. (a) The conventional transconductor. (b) The MOSFET-only transconductor.

to below 50dB owing to the non-ideal characteristic of the active device. Moreover, the degradation of linearity happens for small feature sizes of MOS transistors due to the influence of second-order effects, like velocity saturation and mobility reduction, under nano-scale CMOS technology.

In the paper, the design of a low distortion and low supply voltage transconductor is presented. The proposed high linearity transconductor by using mobility compensation techniques in the differential structure is discussed in Section II. In Section III, the simulation results of the proposed transconductor are discussed. Some final conclusions are presented in Section IV.

II. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Figure 1(a) shows the conventional transconductor, where the voltage-to-current conversion is obtained by using an operational amplifier through a passive resistor. The current is then sensed and mirrored to the output node. However, the variation of resistor due to fabrication and temperature would provide an undesired transconductance value. Thus, a single transistor under linear region operation shown in Figure 1(b) is used to replace the passive resistor [9]. By using the linear region transistor, the equivalent resistance can be continuously tuned by adjusting the gate voltage of transistor M4. When the NMOS operating in the

linear region, the drain current can be given, and the voltage-to-current relationship shown in Figure 1(b) can be obtained as follows

$$I_{D,lin} = K_{lin}(V_{GS} - V_{thn})V_{DS} - \frac{1}{2}K_{lin}V_{DS}^2 \qquad (1)$$

where $K_{lin} = \mu_n C_{ox}(W/L)$, W and L are the width and length of the device, respectively, C_{ox} is the oxide capacitance per unit channel area, μ_n is the low-field mobility, and V_{thn} is the NMOS threshold voltage. V_{GS} and V_{DS} are the gate-to-source and drain-to-source voltage, respectively.

We can find that the output current would not hold a linear relationship to the input voltage owing to the additional second term in equation (1), which thus degrades the linearity of the transconductor. In order to increase the linearity of the transconductor, previous research reports that another transistor could be added to cancel out the second term in equation (1) based on the large signal square-law equation in the saturation region, and the -40 dB total harmonic distortion (THD) was achieved [10]. However, the technique needs extra operation amplifiers, which implies much more power consumption. Besides, it would not work well in the modern nano-scale CMOS technology owing to that the short channel effect would largely affect the ideal characteristic of the square-law behavior.

Although the technique reported in [10] is not suitable to provide the high linearity and low power transconductor in modern nano-scale CMOS process, we can take the circuit in Figure 1(b) to become the differential version in our design. Therefore, the second term in equation (1) can be cancelled out by inherent differential structure, and the linear relationship would be given by

$$I_{out} = \frac{K_{lin}(V_{GS} - V_{thn})}{1 + \theta(V_{GS} - V_{thn})}V_{in} \qquad (2)$$

where θ is the mobility reduction coefficient. The equation shows that the linear voltage-to-current conversion could be obtained by taking short channel effects into consideration. Furthermore, high order nonlinearity components still occur in the conversion because equation (1) is resulted from the
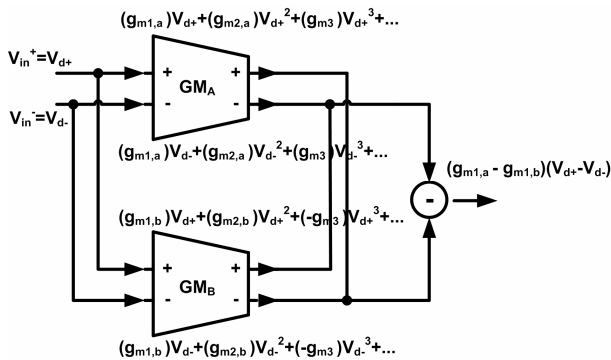
analysis of an approximation. To deal with the drain current of the linear region transistor in more details, a precise LEVEL 54 BSIM4 transistor model is expressed as [11]

$$I_{D,lin} = K_{lin}\left[\frac{(V_{GS} - V_{thn})V_{DS} - \frac{1}{2}V_{DS}^2}{1 + \theta(V_{cm} - V_{thn})}\right] \times$$
$$\left\{1 + \frac{K_{lin}}{V_{DS}}\left[\frac{(V_{GS} - V_{thn})V_{DS} - \frac{1}{2}V_{DS}^2}{1 + \theta(V_{cm} - V_{thn})}\right]\right\}^{-1} \qquad (3)$$

To analyze the linearity of the V_{DS} voltage against the drain current, a Tayler series expansion is used and than the relationship would be expressed by

$$I_{D,lin} = a_{0,lin} + a_{1,lin}V_{DS} + a_{2,lin}V_{DS}^2 + a_{3,lin}V_{DS}^3 + a_{4,lin}V_{DS}^4 + \cdots \qquad (4)$$

where
$$a_{1,lin} = \frac{K_{lin}(V_{GS} - V_{thn})}{[1 + (K_{lin} + \theta)(V_{GS} - V_{thn})]}$$
$$a_{3,lin} = \frac{-K_{lin}^2[1 + \theta(V_{GS} - V_{thn})]}{4[1 + (K_{lin} + \theta)(V_{GS} - V_{thn})]^3}$$

In the equation, the even-order harmonic term can be cancelled out by the differential structure and thus the third-order harmonic distortion would become the dominant component.

In our proposed transconductor, the other saturated transistors based on the differential structure are used to compensate the third-order harmonic distortion. Fig. 2 shows the block diagram of the proposed approach. Two voltage-to-current converters with the opposite third-order signs are provided in the transconductor. Therefore, the nonlinearity term of the transconductor can be reduced. The concept of the topology comes from that the output current of the saturated transconductor in the differential pair also suffers the problems of channel length modulation and short channel effects as the feature size of the transistors is chosen to be small, and thus the output current is given by

$$I_{D,sat} = \frac{K_{sat}(V_{GS} - V_{thn})^2}{2[1 + \theta(V_{GS} - V_{thn})]} \qquad (5)$$

where K_{sat} is the device parameter of saturated transistors. Again, a Tayler series expansion is introduced and then the voltage-to-current relationship would be expressed by

$$I_{D,sat} = a_{0,sat} + a_{1,sat}V_{GS} + a_{2,sat}V_{GS}^2 + a_{3,sat}V_{GS}^3 + a_{4,sat}V_{GS}^4 + \cdots \qquad (6)$$

Figure 2. Nolinearity cancellation mechanism.

$$\text{where} \quad a_{1,sat} = \frac{K_{sat} V_{thn} [2 + 3\theta]}{2[1 - \theta V_{thn}]^2}$$

$$a_{3,sat} = -\frac{K_{sat} \theta}{2[1 - \theta V_{thn}]^4}$$

We can find that the dominant distortion of the saturated transistor occurs due to the short channel effects in the third-order harmonic component under the topology of the differential structure.

The introduced transistor in the saturation region seems to provide another distortion term. However, although the third-order harmonic terms of equations 4 and 6 have the same signs, we can put the output node of saturated transistors in the opposite position as corresponding to the linear region transistors. Thus, when fixed values of parameters are given, the aspect ratio of compensated transistor can be found by solving the following equation to achieve a highly linear voltage-to-current conversion.

$$a_{3,lin} - a_{3,sat} = 0 \tag{7}$$

Figure 3(a) shows the proposed transconductor circuit. The simple operational amplifiers are formed by transistors M1 to M2, M3 to M4, and two level shifter circuits. On one hand, transistors M7 and M8 operate in the linear region, and thus the input voltage variation can be passed down to the source of transistor M5 and M6, and converted by transistors M7 and M8 for one voltage-to-current conversion path. On the other hand, the input voltage applied to the gate of the saturated transistors M9 and M10 composes another voltage-to-current conversion path. Finally, the output common-mode node is adjusted by a CMFB circuit through the gate voltage of transistors M11 and M12. In the proposed transconductor, the overall differential current is given by

$$I_O = (I_1 - I_2) + (I_3 - I_4) \tag{8}$$

Thus, the transconductance of the transconductor would be

$$Gm = \frac{I_O}{V_{in}} = \frac{K_{7,8}(V_{tune} - V_{thn})}{[1 + (K_{lin} + \theta)(V_{tune} - V_{thn})]} - \frac{K_{9,10} V_{thn} [2 + 3\theta]}{2[1 - \theta V_{thn}]^2} \tag{9}$$

Figure 3(b) shows the level shifter circuit in our transconductor. The circuit, which is called the flipped voltage follower, is composed by a shunt feedback to enhance the follower ability [12].

III. SIMULATION RESULTS

The chip was simulated in TSMC 180-nm Deep N-WELL CMOS process. A supply voltage of 1-V was employed in the simulation and the nominal static power consumption of the transconductor is 120 μW. Large signal simulation shows the function of differential input voltage to transconductance variation in Figure 4. By comparing with a simple differential transconductor, the proposed differential transconductor with mobility compensation techniques achieves much higher linearity, but with smaller transconductance value as expected. Fig. 5 shows THD with relation to 1MHz sinusoid differential input swing ranges. -65 dB THD can be achieved in a 0.7 V_{pp} input swing, and 12 dB improvement of the proposed version is shown. The distribution of linearity is shown in Figure 6 by Monte-Carlo simulation over the corner variation and transistor mismatch. The result shows 70% of 180 samples range the performance of -64 to -68 dB in 1MHz 0.7 V_{pp} input signal. Finally, the simulated input referred noise spectral density at 1 MHz is 32 nV/$\sqrt{}$ Hz.
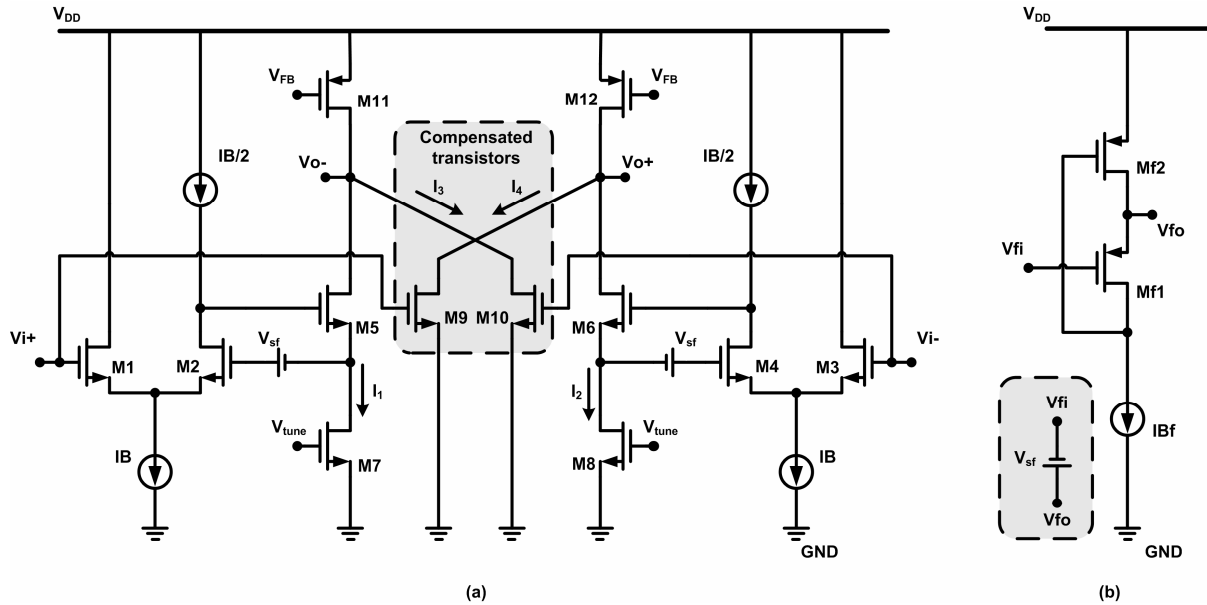

Figure 3. (a) Proposed transconductor circuit. (b) The level shifter circuit.

Figure 4. G$_m$ variation of transconductors.

Figure 5. Simulated THD with input differential voltage.

Figure 6. Monte Carlo simulation results of THD for 0.6V$_{pp}$ input differential voltage.

IV. CONCLUSIONS

A novel differential transconductor under nano-scale CMOS technology has been reported. It is based on the principle that the third-order harmonic distortion term could be cancelled by the addition of the two drain current, one in the linear region and the other in the saturation region, to improve the linearity. The technique employed leads to a significant improvement of the linearity performance in the voltage-to-current conversion in the MOSFET-only topology. The simulation results show that less than -65 dB THD at 0.7 V$_{pp}$ input signal could be achieved under 1-V power supply voltage. We can conclude that the low voltage transconductor could be provided as a high linearity building block in analog VLSI applications.

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[12] R. G. Carvajal, J. Ramirez-Angulo, A. J. Lopez-Martin, A. Torralba, J. A. G. Galan, A. Carlosena, and F. M. Chavero,"The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design," *IEEE Trans. Circuits Syst. I: Regular Paper*, vol. 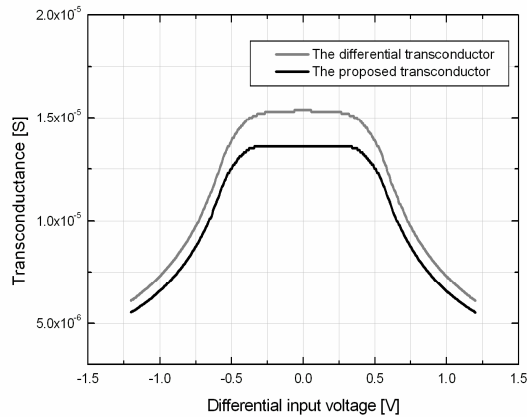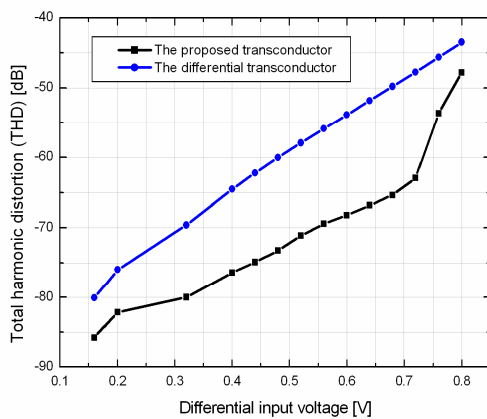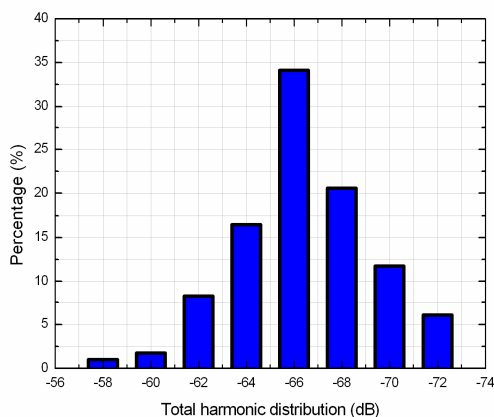52, no. 7, pp. 1276-1291, Jul. 2005.