

# 國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

原子層沉積二氧化鋯/三氧化二鋁於砷化銦鎵金氧半  
電容之電性與表面化性分析的研究

**Investigation of Electrical and Interfacial Chemistry  
Analyses for Atomic-Layer-Deposition  
ZrO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs**

研究生：張邦聖

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# 原子層沉積二氧化鋁/三氧化二鋁於砷化銦鎵金 氧半電容之電性與表面化性分析的研究

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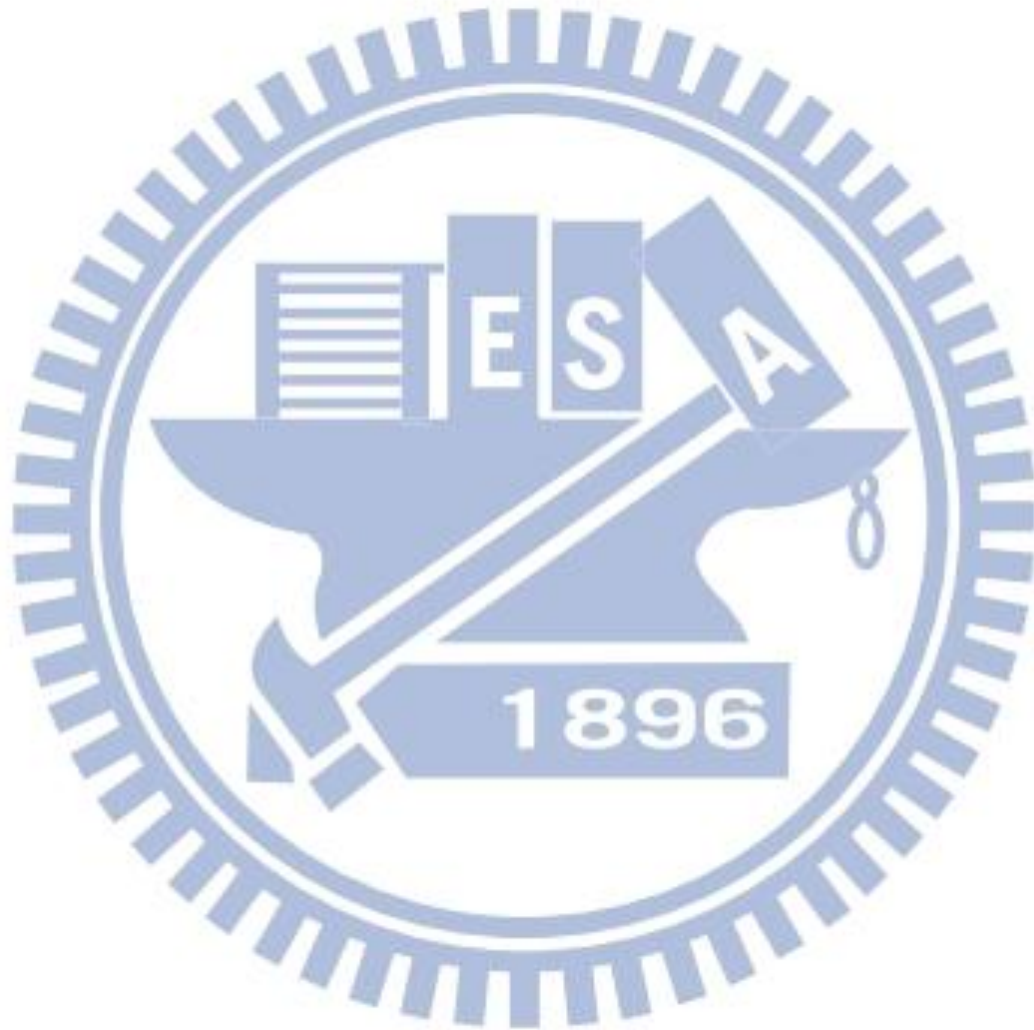
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## 摘要

在此篇論文初，我們研究了利用原子層沉積系統的前驅物做表面的預處理，像是 TMA 以及 TEMAZ。然而，與 TEMAZ 相比，我們發現 TMA 表面處理可以有效地抑制聚積區的頻率分散與空乏區的介面缺陷電荷。為了更進一步探討二氧化鋁/砷化銦鎵的介面與閘極氧化層的特性，我們使用了不同的後沉積退火溫度及氮氫混合氣體退火。此外，藉由 TMA 預處理，我們在二氧化鋁與砷化銦鎵的介面併入數層的三氧化二鋁，並且討論其表面特性。從數據分析上指出電容在每個不同的三氧化二鋁層條件下，後沉積退火溫度 300 度及氮氫混合氣體退火展現最好的電性。另外，我們利用電導法來萃取介面缺陷電荷密度；仍然可以觀察到在 PDA 溫度 300 度及 FGA 下能隙深處 (midgap) 的缺陷電荷是最低的。在 XPS 分析的證明下，我們推測這個結果可能是在電容介面上有較高的  $As^{2+}/As_2O_5$ 、 $As_2O_3/As_2O_5$ 、 $In_2O_3/InAsO_4$ 。此外，從電性與表面化學特性來看，我們可以證實較厚的三氧化二鋁夾層可以改善介面品質。

最後，我們建立了一個分佈模型來解釋操作在聚積區之半導體表面與閘極氧化層內缺陷的穿隧機制。然後我們利用模型與實驗數據做媒合並且定量地萃取閘極介電層內的缺陷密度。而與前面的結果相比有很好的 consistency。





# **Investigation of Electrical and Interfacial Chemistry Analyses for Atomic-Layer-Deposition ZrO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs**

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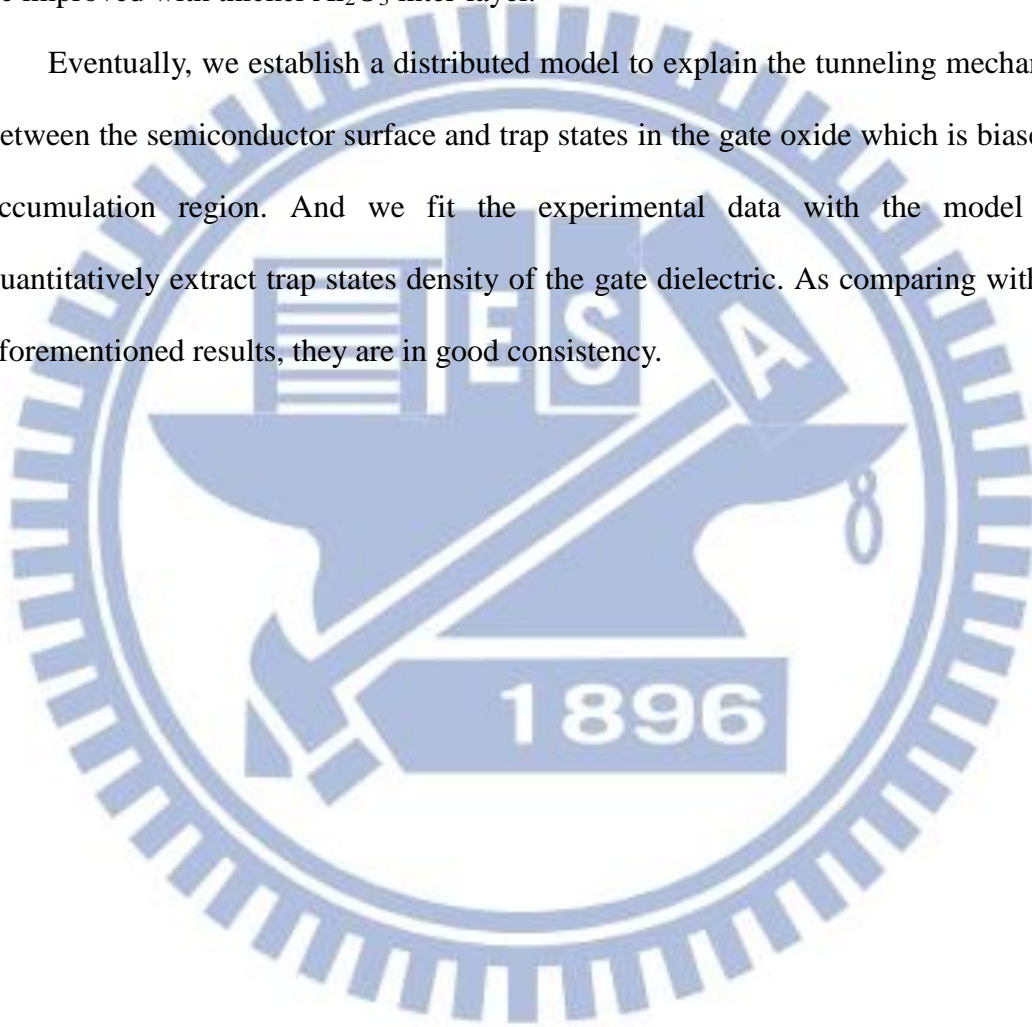
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## ***ABSTRACT***

In the beginning of this thesis, we have investigated the surface pretreatment before depositing gate dielectric by using the precursors of ALD system, such as TMA and TEMAZ. However, compared to TEMAZ, we find the TMA surface treatment is effective to suppress the frequency dispersion and interface states in accumulation and depletion region. In order to further discuss the interface and gate oxide property of ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs, we apply various post-deposition annealing temperatures with forming gas annealing (FGA). Moreover, by TMA pretreatment, we incorporate several Al<sub>2</sub>O<sub>3</sub> inter-layers with the interface of ZrO<sub>2</sub> and In<sub>0.53</sub>Ga<sub>0.47</sub>As and discuss their interface properties. It is noted that the MOSCAPs under PDA 300 °C with FGA show the best electrical characteristics at each Al<sub>2</sub>O<sub>3</sub> inter-layer conditions. In addition, we utilize the conductance method to extract the density of

interface states and still observe that the  $D_{it}$  exists near midgap is the lowest at PDA 300 °C with FGA. With the evidence of XPS analysis, we suppose that the result might be caused by higher amounts of the  $As^{2+}/As_2O_5$ ,  $As_2O_3/As_2O_5$ , and  $In_2O_3/InAsO_4$  at the MOSCAPs interface. Furthermore, from the electrical and interfacial chemistry characteristics, we demonstrate that the interface quality could be improved with thicker  $Al_2O_3$  inter-layer.

Eventually, we establish a distributed model to explain the tunneling mechanism between the semiconductor surface and trap states in the gate oxide which is biased in accumulation region. And we fit the experimental data with the model and quantitatively extract trap states density of the gate dielectric. As comparing with the aforementioned results, they are in good consistency.



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學生生涯終究還是結束了。回想起這兩年多的碩士生活，不禁覺得時間真的過得很快，有種淡淡的哀傷。在研所期間遇到的人事物現在回想起來依然歷歷在目，首先要感謝我的指導教授簡昭欣老師，謝謝您總是在研究方面給予我們支持與協助，更提供很好的學習與實驗環境，讓我們能確實的學習到專業知識，在待人處事上也常提醒我們哪些地方是該注意並改進的，使我們在前進職場的道路上能懂得應對得體。很高興能在研究所期間選擇老師指導，使我在未來的人生道路上提前學到了不少寶貴經驗。

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於新竹交通大學

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# Chapter 1

## *Introduction*

### 1.1 General Background

Recently, in order to maintain the performance of silicon-based metal oxide semiconductor field-effect-transistors (MOSFETs) and scale the size of transistors at the same time, the gate dielectric thickness and channel length have been reduced to support this criterion. However, when the reduction of device dimensions is approaching physical limitation, high- $k$  materials and high mobility channel substrates have been developed to remain or improve the performance. Therefore, several bulk materials, such as Ge, GaAs, InGaAs, and InAs [1] have attracted much attention as the potential candidates due to their higher electron mobility than Si, as shown in **Table 1.1**. From **Fig. 1.1**, we can find various integration and applications of Ge/ III-V channel materials on Si platform [2]. The CMOS device fabricated on the non-Si channel materials which accord with the More Moore approach are pursuing for the high driving current. As a result, III-V materials are used to be n-channel MOSFETs, and Ge is proper for n- or p-channel MOSFETs. Furthermore, if III-V p-channel MOSFETs are expanded as practical structures, III-V or Ge CMOS might be appropriate development in the future. In addition, high- $k$  materials have been regarded as replaceable gate dielectrics for scaling problems and insulator leakage issues of conventional SiO<sub>2</sub>. With comparing to silicon dioxide, high- $k$  materials can provide the higher capacitance without reducing oxide thickness and increasing gate leakage current. So far, there are numerous literature demonstrate that the MOSFETs developed as the potential devices, such



as Ge [3], InGaAs [4,5] channels by using high- $k$  gate dielectrics. Nevertheless, the interface characteristics between gate oxide and III-V semiconductors still exist important issues, such as Fermi-level pinning and an amount of interface states. Thus, there are several solutions have demonstrated to passivate the interface and prevent Fermi-level pinning [4,6-9]. With solving these problems, high- $k$ /III-V MOSFETs will be one of the promising structures in the future.

## 1.2 Motivation

To understand III-V compound semiconductors used to fabricate MOSFETs, there are many technological challenges need to be conquered. One of the main obstacles is the gate dielectrics which lack high oxide quality, thermodynamic stabilization, low leakage current, high breakdown fields, and excellent native oxide like SiO<sub>2</sub> on Si naturally. Moreover, III-V surface exists such as vacancies, defects, or incomplete dimerization which cause unsaturated bonds and form electrically active traps [10,11]. Thus, high interface trap densities might give rise to insufficient Fermi-level response, preventing control over the charge carriers in the channel [12], the degradation of the drive current, and the subthreshold swing. For that reason, the interfacial control in III-V gate stack is strongly needed for realizing low  $D_{it}$ . To develop appropriate gate dielectrics and better interface properties, forming a stable interface with suitable thermal budget and how to reduce the density of interface states ( $D_{it}$ ) are the important issues. In particular, fabricating good interface qualities between III-V and high- $k$  dielectrics are extremely challenging. Here, we will use In<sub>0.53</sub>Ga<sub>0.47</sub>As as our substrates, Al<sub>2</sub>O<sub>3</sub> and ZrO<sub>2</sub> as gate oxide to study their interface and oxide characteristics.

## 1.3 Organization of the Thesis

In **Chapter 1**, an introduction of the background and the main challenges has been realized. We also describe the problems of gate dielectric quality and interface state issues.

In **Chapter 2**, in order to investigate the property of the  $\text{ZrO}_2$  oxide quality and the high- $k$ /III-V interface, the frequency dispersion at accumulation region, the hysteresis, and conductance method are extracted from the measured  $C$ - $V$  electrical characteristics and the XPS analysis to confer the interfacial chemistry. First, we utilize the various pretreatment to passivate the high- $k$ / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  interface before depositing gate dielectrics. Then, incorporating several  $\text{Al}_2\text{O}_3$  as inter-layer between  $\text{ZrO}_2$  and  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  is demonstrated. Furthermore, we discuss the influence of various PDA conditions with FGA.

In **Chapter 3**, we apply the distributed border traps model to quantitatively determine the density of bulk-oxide traps extracted from our measured capacitance and conductance data. And we compare these  $N_{\text{bt}}$  values with the frequency dispersion  $\Delta C$  in **Chapter 2**.

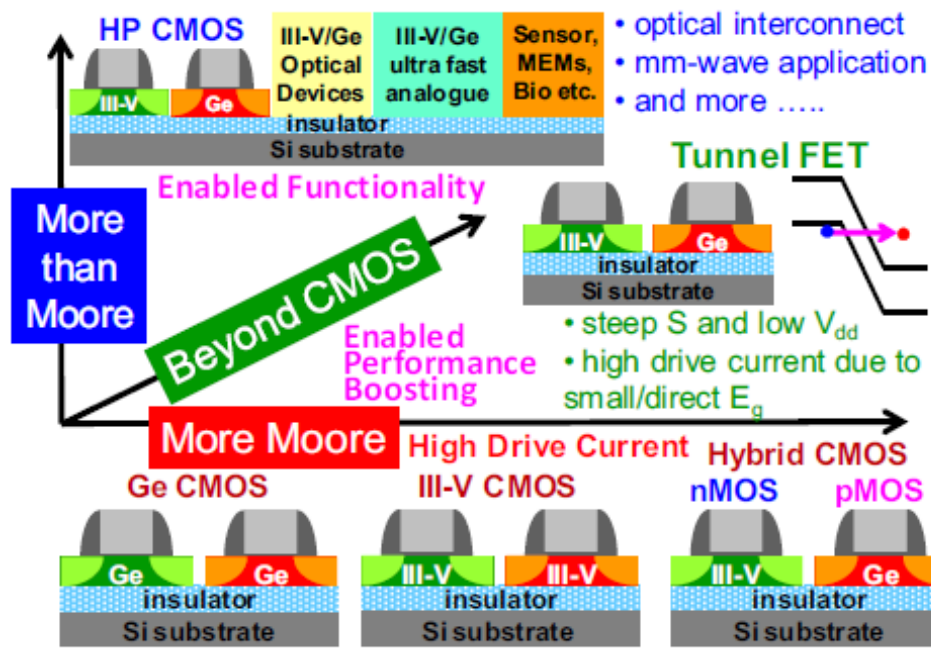
In **Chapter 4**, we make a conclusion as the aforementioned results and give some suggestions for future works.

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**Fig. 1.1** Possible evolution scenario for III-V/Ge devices on Si platform through heterogeneous integration

	Si	Ge	GaAs	In <sub>0.53</sub> Ga <sub>0.47</sub> As	InAs
Lattice constant (Å)	5.431	5.646	5.653	5.869	6.058
Band gap (eV)	1.12	0.66	1.42	0.74	0.36
Intrinsic carrier conc. (cm <sup>-3</sup> )	9.6×10 <sup>9</sup>	2.4×10 <sup>13</sup>	2.2×10 <sup>6</sup>	6.3×10 <sup>11</sup>	1×10 <sup>15</sup>
Effective conduction band density of states (cm <sup>-3</sup> )	2.8×10 <sup>19</sup>	1.04×10 <sup>19</sup>	4×10 <sup>17</sup>	2.2×10 <sup>17</sup>	8.7×10 <sup>16</sup>
Effective valence band density of states (cm <sup>-3</sup> )	1.04×10 <sup>19</sup>	6×10 <sup>18</sup>	9.7×10 <sup>18</sup>	7.8×10 <sup>18</sup>	6.6×10 <sup>18</sup>
Electron mob. (cm <sup>2</sup> /Vs)	1600	3900	9200	12000	40000
Electron effective mass (/m <sub>0</sub> )	m <sub>t</sub> : 0.19 m <sub>l</sub> : 0.916	m <sub>t</sub> : 0.082 m <sub>l</sub> : 1.467	0.067	0.043	0.023
Hole mob. (cm <sup>2</sup> /Vs)	430	1900	400	300	500

**Table 1.1** Material properties of bulk Si, Ge, GaAs, In<sub>0.53</sub>Ga<sub>0.47</sub>As, and InAs at 300K

# Chapter 2

## *Studies of $ZrO_2/Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs with Electrical Characteristics and Interfacial Chemistry*

### 2.1 Introduction

Recent research shows III-V compound semiconductor has been actively investigated to replace the Si-based CMOS technology for pursuing higher device performance and lower power consumption due to their high electron mobility, high saturation velocity, and small electron effective mass [1-3]. However, the obstacle for the implementation of III-V semiconductors is the high density of interface states ( $D_{it}$ ) which has caused Fermi level pinning between gate dielectric and III-V interface [4]. To improve the device performance, it's important to reduce the  $D_{it}$  at the III-V interface, which results in increasing gate leakage current, lower drive current and sub-threshold swing [5-6]. Several researches such as combination of high- $k$  dielectric materials, crystal orientations, appropriate deposition conditions, and various passivation techniques have shown in recently [7-10]. Moreover, previous publication revealed that in order to reduce the native oxide on III-V surface and improve electrical characteristics, there have developed various treatment or passivation methods such as ammonium sulfide passivation before oxide deposition [11], effect of hydroxylation on the interface [12]. In addition, depositing gate dielectric by atomic-layer-deposited (ALD) can also reduce native oxide and interface states because of the “self-cleaning” effect by ALD precursors on III-V semiconductors such as GaAs [13-14], InGaAs [15-17].

With continuous downscaling of gate dielectrics, developing high- $k$  materials such as  $\text{Al}_2\text{O}_3$  [18], and  $\text{HfO}_2$  [19],  $\text{ZrO}_2$  [20-23] with low interfacial density of states and low gate leakage current is important for III-V semiconductors as a high mobility channel material.  $\text{Al}_2\text{O}_3/\text{InGaAs}$  MOS interfaces formed by using ALD are known to have the better quality, but the dielectric constant is still not enough to provide the high performance devices [5]. On the other hand,  $\text{HfO}_2$  and  $\text{ZrO}_2$  [24-27] have attracted much attention as promising gate dielectrics of III-V semiconductors because of the high permittivity. In addition,  $\text{ZrO}_2$  dielectric constant value is higher than  $\text{HfO}_2$  [28] as shown in **Fig. 2.1** but lower band offset shown in **Table 2.1**. However, the high- $k$ /III-V interfacial property is complicated due to the more number of elements present at the interface when compared to the  $\text{Si}/\text{SiO}_2$ . When exposure to the air, the native oxides of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  influence the high- $k$ /III-V interface by increasing the leakage current and density of interface states between the gate dielectrics and the III-V substrate [29]. Therefore, there were some efforts show that the Trimethylaluminium (TMA,  $\text{Al}(\text{CH}_3)_3$ ) of ALD precursors can be used to remove native oxides on III-V surface [14,30], but the influence of Tetrakis(ethylmethylamino) zirconium [TEMAZ,  $\text{Zr}(\text{N}(\text{C}_2\text{H}_5)(\text{CH}_3))_4$ ] of the ALD precursors as pre-deposition treatment hasn't been studied.

In our work, we will use the TEMAZ and TMA precursor to be pre-deposition treatment before depositing  $\text{ZrO}_2$ . Nevertheless, compared with the aforementioned pretreatment, the  $\text{ZrO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  interfaces still have worse properties. For this reason, we will insert  $\text{Al}_2\text{O}_3$  inter-layer to improve the  $\text{ZrO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  interface quality. Besides, there is several researches show that annealing with hydrogen could reduce the oxide charge and interface states and the presence of thermal energy can reconstruct the bonds and passivate dangling bond all over the gate oxide [31, 32]. On behalf of further improving oxide interface quality, various post-deposition annealing conditions with FGA have been implemented. Finally, we will discuss the influence of the various pretreatment and inserting  $\text{Al}_2\text{O}_3$  inter-layers by electrical characteristics and interfacial chemistry.



In this chapter, capacitance-Voltage ( $C-V$ ) and conductance-voltage ( $G-V$ ) characteristics were measured by HP4284A  $LCR$  meter at the temperature of 300K.

## 2.2 Experimental Procedures of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAPs

### 2.2.1 Various Surface Pretreatment and Capacitor Fabrication

The MOS capacitor substrates prepared in this thesis were p-type InP (100) wafers with Zn-doped and doping concentration of ca.  $1 \times 10^{18} \text{ cm}^{-3}$  as the bulk substrates. Then, growing thickness of 300 nm p-type  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  (100) with Zn-doped and doping concentration of ca.  $1 \times 10^{18} \text{ cm}^{-3}$  as a buffer layer and 60-nm p-type  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  (100) with Zn-doped and doping concentration of ca.  $1 \times 10^{16} \text{ cm}^{-3}$  as a channel layer. Before depositing gate dielectric, there must be a thin native oxide layer on the wafer's surface. In order to remove this, there were three clean steps prior to gate dielectric deposition. At first, the sample was rinsed in acetone (ACE) for 5 minutes. Next, rinsing in isopropanol (IPA) for 5 minutes, followed by dipping in deionized water ( D.I. water ). Finally, rinsing in dilute HCl solution (HCl :  $\text{H}_2\text{O}=1:10$ ) for 2 minutes. Then the samples were loaded into ALD chamber. Tetrakis(ethylmethylamino) zirconium [TEMAZ,  $\text{Zr}(\text{N}(\text{C}_2\text{H}_5)(\text{CH}_3))_4$ ] or trimethylaluminum [TMA,  $\text{Al}(\text{CH}_3)_3$ ] precursor pulses were performed for 10 cycles as surface pretreatment. After that, the treated  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  surfaces were *in-situ* grown the  $\text{ZrO}_2$  thin film for 80 cycles by atomic-layer-deposition (ALD) system at 250 °C. After depositing, different annealing conditions such as 300 °C, 400 °C, and 500 °C for 120 s in  $\text{N}_2$  ambience have been tested. Then, we defined the capacitor area by photolithography and patterning gate electrode by sputter system of 100 Å of Ti and 500 Å of Pt. The capacitor area of gate electrode was ca.  $1 \times 10^{-4} \text{ cm}^2$  by optical microscopy. Backside contacts were also formed by sputter system

(Ti/Pt : 100 Å/500 Å). Finally, all of the samples were prepared by forming gas annealing (FGA) at 250 °C for 30 min in a 10% H<sub>2</sub>/90% N<sub>2</sub> ambience.

The process flow and structure are shown in **Fig. 2.2** and **Fig. 2.3**.

## **2.2.2 Incorporating Several Cycles of Al<sub>2</sub>O<sub>3</sub> with ALD-TMA /ZrO<sub>2</sub> Growth and Capacitor Fabrication**

The MOS capacitor substrates prepared in this thesis were p-type InP (100) wafers with Zn-doped and doping concentration of ca.  $1 \times 10^{18} \text{ cm}^{-3}$  as the bulk substrates. Then, growing thickness of 300 nm p-type In<sub>0.53</sub>Ga<sub>0.47</sub>As (100) with Zn-doped and doping concentration of ca.  $1 \times 10^{18} \text{ cm}^{-3}$  as a buffer layer and 60-nm p-type In<sub>0.53</sub>Ga<sub>0.47</sub>As (100) with Zn-doped and doping concentration of ca.  $1 \times 10^{16} \text{ cm}^{-3}$  as a channel layer. Before depositing gate dielectric, there must be a thin native oxide layer on the wafer's surface. In order to remove this, there were three clean steps prior to gate dielectric deposition. At first, the sample was rinsed in acetone (ACE) for 5 minutes. Next, rinsing in isopropanol (IPA) for 5 minutes, followed by dipping in deionized water ( D.I. water ). Finally, rinsing in dilute HCl solution (HCl:H<sub>2</sub>O=1:10) for 2 minutes. Then the samples were loaded into ALD chamber. Trimethylaluminum [TMA, Al(CH<sub>3</sub>)<sub>3</sub>] precursor pulses were performed for 10 cycles as surface pretreatment. After that, the different cycles (1, 5, 10 cycles) of Al<sub>2</sub>O<sub>3</sub> and 80 cycles ZrO<sub>2</sub> thin film were grown by atomic-layer-deposition (ALD) system at 250 °C. After depositing, different annealing conditions such as as-deposited, and 300 °C, 400 °C, and 500 °C for 120 s in N<sub>2</sub> ambience have been tested. Then, we defined the capacitor area by photolithography and patterning gate electrode by sputter system of 100 Å for Ti and 500 Å for Pt. The capacitor area of gate electrode was ca.  $1 \times 10^{-4} \text{ cm}^2$  by optical microscopy. Backside contacts were also formed by sputter system (Ti/Pt : 100 Å/500 Å). Finally, all of

the samples were prepared by forming gas annealing (FGA) at 250 °C for 30 min in a 10% H<sub>2</sub> / 90% N<sub>2</sub> ambience.

The process flow and structure are shown in **Fig. 2.4** and **Fig. 2.5**. The cross-sectional TEM image of as-deposited TMA/Al<sub>2</sub>O<sub>3</sub> 10 cycle/ZrO<sub>2</sub> on In<sub>0.53</sub>Ga<sub>0.47</sub>As channel layer with FGA is shown in **Fig. 2.6**.

## 2.3 Capacitor Characteristics and Interfacial Chemistry of ALD-ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs with Various Pretreatments

In the multi-frequency *C-V* curves, we can see the dispersion among different frequencies at the accumulation and depletion region, respectively. Consequently, we quantitatively define the frequency dispersion ratio  $\Delta C$  at the accumulation region as follows:

$$\Delta C (@V_g = -2 \text{ V}) \equiv \{ [C(@100\text{Hz}) - C(@100\text{kHz})] / C(@100\text{kHz}) \} \times 100\% \quad (2.1)$$

Here,  $\Delta C$  is the frequency dispersion of the capacitance measured in 100 kHz and 100 Hz at  $V_g = -2$  V. The overviews of all the samples in capacitance frequency dispersion are shown in **Table 2.2**.

The hysteresis curve in *C-V* measurement is observed at 100 kHz with two sweep directions; one is from the accumulation to inversion region and the other one is opposite. Therefore, we determine  $V_{FB}$  experimentally by plotting  $(1/C_{hf})^2$  versus  $V_g$ , respectively. Then differentiating these two curves and finding the sharply peaked curves whose peaks mean the flatband voltage  $V_{FB}$  (not shown). The different values between these two peaks are about  $V_{FB}$  shift or hysteresis. The overviews of all the samples in hysteresis (V) are shown in **Table 2.3**.



### 2.3.1 $C$ - $V$ and $G$ - $V$ properties of MOSCAPs under Various Post-Deposition Annealing Conditions w/FGA

**Fig. 2.7 (a) (b) (c)** and **Fig. 2.9 (a) (b) (c)** show the multi-frequency  $C$ - $V$  curves of  $p$ -type  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  MOSCAPs with  $\text{ZrO}_2$  gate dielectric for TEMAZ or TMA pretreatment with FGA under different PDA conditions, respectively. For TEMAZ treatment, the thermal condition with PDA 300 °C for 120s demonstrates the best  $C$ - $V$  electrical characteristics than the others. Though the capacitance at  $V_g = -2$  V is the lowest (**Fig. 2.7 (a)**), the frequency dispersion near accumulation region with PDA 300 °C ( $\Delta C = 99.4\%$ ) is better than the others ( $\Delta C = 160.9\%$  at 400 °C and  $\Delta C = 129.5\%$  at 500 °C), are shown in **Table 2.2**. The huge hump at all the samples from  $V_g = -0.5$  V to  $V_g = 0.5$  V indicate the response of interface states. Then, from **Fig. 2.8 (a) (b) (c)**, we can find the color variation of conductance maps from  $V_g = -1$  V to  $V_g = -2$  V is becoming dramatic when above PDA 400 °C from low toward high frequency. We suppose this phenomenon to the border traps response of gate dielectrics. Catching more attention to these maps, we can observe the concentric circles between  $V_g = -1$  V and  $V_g = 0$  V. It might indicate the movement of Fermi level from high positive gate voltage to this region and pinned between 1 kHz and 10 kHz. Then toward high negative gate voltage, the voltage will drop on the gate dielectrics. Besides, there is an additional signal at high frequency with high negative gate voltage as the increasing temperature of PDA, this might be the energy loss. And a distinct map signal exists from  $V_g = 1$  V to  $V_g = 2$  V at low frequency region might be the interface traps response accompanying with minority carrier signal, especially at PDA 500 °C.

Moreover, for TMA treatment from **Fig. 2.9 (a) (b) (c)**, we can also observe the frequency dispersion near accumulation region with PDA 300 °C ( $\Delta C = 42.7\%$ ) is better than the others ( $\Delta C = 84.3\%$  at 400 °C and  $\Delta C = 75.9\%$  at 500 °C), also shown in **Table 2.2**. The hump from  $V_g = -0.5$  V to  $V_g = 0.5$  V indicate the density of interface states is lowest at PDA



300 °C. Furthermore, we extract the hysteresis from the difference of  $V_{FB}$  and find PDA 300 °C with FGA has the lowest oxide traps or interface states, are shown in **Table 2.3**. And then, from **Fig. 2.10 (a) (b) (c)**, there is obvious variation of contours from  $V_g = -1$  V to  $V_g = -2$  V as the increasing temperature of PDA and these might be the presence of oxide traps. As well Fermi level pinning also occur between  $V_g = -1$  V and  $V_g = 0$  V among 1 kHz and 10 kHz. In addition, the energy loss exists at high frequency with high negative gate voltage when the temperature of PDA increases. Similarly, the response of interface states and minority carrier also exists at gate voltage between 1 and 2 volts, especially at PDA 500 °C.

### 2.3.2 Comparison of Various Pretreatments on Electrical and Interfacial Chemistry Characteristics

From **Fig. 2.7** to **Fig. 2.10**, we can notice that the frequency dispersion near accumulation region of TMA treatment is much weaker and the hysteresis is smaller than TEMAZ, especially at PDA 300 °C, which reveals the high-k dielectrics and interface quality are improved. In general, the frequency dispersion and the hysteresis of the *C-V* curves are mainly caused by the existence of border traps and interface states. Therefore, we infer that the interface between gate dielectric and substrate might be repaired by TMA pretreatment. This phenomenon means TMA treatment is better than TEMAZ. In order to further interpret the interface property, we select specific condition to analyze the discrepancy of chemical characteristics as follows.

The top two graphs of **Fig. 2.36 (a) (b) (c)** show X-ray photoelectron spectroscopy of ALD-TEMAZ or TMA 10 cycle /ZrO<sub>2</sub> 10 cycles on p-type In<sub>0.53</sub>Ga<sub>0.47</sub>As with FGA at PDA 300 °C. XPS spectra were taken by Ga 2*p*<sub>3/2</sub>, In 3*d*<sub>5/2</sub>, and As 2*p*<sub>3/2</sub> core levels. From **Fig. 2.36 (a)**, there is no obvious variation in Ga 2*p*<sub>3/2</sub> spectra. However, the In 3*d*<sub>5/2</sub> and As 2*p*<sub>3/2</sub> spectra, shown in **Fig. 2.36 (b) (c)**, indicate the existence of In- and As-oxide in both

samples. **Table 2.6** shows the ratio of the fitted area such as  $\text{In}_2\text{O}_3$  to  $\text{InAsO}_4$  from  $\text{In } 3d_{5/2}$  spectra,  $\text{As}^{2+}$  to  $\text{As}_2\text{O}_5$  and  $\text{As}_2\text{O}_3$  to  $\text{As}_2\text{O}_5$  from  $\text{As } 2p_{3/2}$  spectra. From the area ratio, we can demonstrate that the higher ratio value is, the better electrical characteristic is, which is consistent with aforementioned conclusion. This finding confirms the TMA treatment might prevent or reduce the presence of inferior substrate native oxides at the interface before depositing gate dielectric [33].

## 2.4 Capacitor Characteristics of ALD- $\text{ZrO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAPs with inserting $\text{Al}_2\text{O}_3$ Inter-layer

The foregoing section indicated that using TMA precursor has a self-cleaning effect before depositing  $\text{ZrO}_2$ . However, from above electrical and interface chemical characteristics, the  $\text{ZrO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  interfaces still have inferior quality than  $\text{Al}_2\text{O}_3$  or  $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  [34]. For the purpose, we will incorporate several  $\text{Al}_2\text{O}_3$  inter-layers with ALD-TMA/ $\text{ZrO}_2$  to confer its interface property.

### 2.4.1 C-V and G-V properties of MOSCAPs under Various Post-Deposition Annealing Conditions w/FGA

At first, we desire to discuss inserting  $\text{Al}_2\text{O}_3$  for 1 cycle into ALD-TMA/ $\text{ZrO}_2$  interface to confer the oxide and  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  interfacial electrical property with FGA under various PDA conditions. From **Fig. 2.11 (a) (b)**, comparing the samples with or without PDA 300 °C condition after FGA, we can find that both samples have not reached strong accumulation, which may indicate high interface states close to the valence band edge. From the frequency dispersion in **Table 2.2** and the hysteresis in **Table 2.3**, the PDA 300 °C ( $\Delta C=41.7\%$ ,

$\Delta V=0.44$  V) is both smaller than as-deposited one ( $\Delta C=43.4\%$ ,  $\Delta V=0.49$  V). Then, from **Fig. 2.11 (b) (c) (d)**, **Table 2.2**, and **Table 2.3**, also display the PDA 300 °C have better properties than the others. Moreover, the C-V characteristics show that the hump between  $V_g = -0.5$  V and  $V_g = 0.5$  V is getting larger as the PDA temperature increase, which may exhibit more response of  $D_{it}$ . Therefore, we can speculate that the superior temperature of post deposition annealing might be 300 °C for our substrates. The conductance contour from **Fig. 2.12 (a) (b) (c) (d)** at low frequency, it might indicate the existence of border traps with high negative  $V_g$ . And the color variation around 0 V to high positive  $V_g$  are becoming noticeable above PDA 400 °C, we suppose that these might be interface traps accompanying with minority carrier signal rather than only minority carrier response [35].

Continued from the preceding paragraph, the quality of ALD-TMA/ $Al_2O_3$  1cycle / $ZrO_2$  interface is still not good enough. Consequently, we raise  $Al_2O_3$  to 5 cycles for improving the properties. From **Fig. 2.13 (a) (b)**, we can't observe the difference between the as-deposited one and the PDA 300 °C one by the naked eye. But from **Table 2.2** and **Table 2.3**, we still find PDA 300 °C is slightly better than the as-deposited one. And From **Fig. 2.13 (b) (c) (d)**, although the capacitance value at  $V_g = -2$  volts with PDA 500 °C is the largest, the frequency dispersion and the hysteresis of all the samples with PDA 300 °C still display the best. This indicates that the samples through appropriate annealing process might be getting better. After that, from **Fig. 2.14 (a) (b) (c) (d)**, the conductance maps from negative to positive gate voltage and from high to low frequency, the variation of contours are more conspicuous especially at PDA 500 °C, which reveal the interface states may mix up with minority carrier response and getting worse. Particularly, there is a distinct variation at low frequency with high negative gate voltage from **Fig. 2.14 (c) (d)**, which might show the border trap response of high-k dielectrics.

Furthermore, from **Fig. 2.15 (a) (b)**, the accumulation, depletion, and inversion region of the MOSCAPs of the as-deposited one and PDA 300 °C one are the same in substance. The



frequency dispersion and hysteresis are demonstrated that the as-deposited one ( $\Delta C=25.0\%$ ,  $\Delta V=0.31$  V) is slightly worse than PDA 300 °C ( $\Delta C=24.4\%$ ,  $\Delta V=0.29$  V), are shown in **Table 2.2** and **Table 2.3**. Then from **Fig. 2.15 (b) (c) (d)**, even if we see the capacitance at accumulation region get larger as increasing PDA temperature, the electrical characteristics are still worse. This might be the oxide trap capacitance induced and interact with the accumulation capacitance. Moreover, the conductance maps at low frequency around 0V to high  $V_g$  of all the samples show that PDA 500 °C has a high distribution of interface traps response, and the position of Fermi-level pinning is moved from 10 kHz to around 100 kHz by the location of the concentric circles, are shown in **Fig. 2.16 (a) (b) (c) (d)**. Besides, we conjecture the energy loss signal around  $V_g = 2$  volts is mainly due to gate leakage.

#### **2.4.2 Comparison of Various $Al_2O_3$ cycles as Inter-layer of ALD-TMA/ $ZrO_2$ on Electrical Characteristics**

From **Fig. 2.17** to **Fig. 2.20**, we notice that the higher  $Al_2O_3$  cycles inserting in ALD-TMA/ $ZrO_2$  is, the optimum capacitor performance is. These results indicate that the more  $Al_2O_3$  inter-layer is effective to passivate the substrate surface and significantly to reduce frequency dispersion and hysteresis at the  $ZrO_2/In_{0.53}Ga_{0.47}As$  interfaces. In addition, we already know that incorporating several cycles of  $Al_2O_3$  can improve the oxide and interface quality from  $C-V$  and  $G-V$  characteristics, which is demonstrated experimentally with aforementioned section, but still not realize the quantitative density of interface trap states. In next section, we will introduce conductance method to extract  $D_{it}$  and compare the different conditions.



## 2.5 Conductance Method

Impedance measurements of MOSCAPs as a function of voltage, frequency, and temperature of high- $k$ /semiconductor interfaces contain contributions from  $D_{it}$  that can be extracted in different ways [36]. The conductance method, established by Nicollian and Goetzberger in 1967, is one of the sensitive methods to quantify  $D_{it}$  [37]. It is the most complete method, because it yields  $D_{it}$  in the depletion and weak inversion portion of the band gap and the capture cross-sections for majority carriers. Although Berglund, Terman and high-low frequency extracted methods could determine interface states, they might overestimate the  $D_{it}$  value on low band gap III-V semiconductor because the signal may induce by minority carrier response. **Fig 2.21 (a)** shows energy band diagram of  $n$ -type MOSCAP in depletion region. A dc gate bias is applied to the gate which superimposes on a small amplitude ( $\sim 25$  mV) ac signal with frequency  $f$  (typically between 1 MHz and 100 Hz). Besides, it displays an arbitrary interface states density distribution, the Fermi level  $E_F$  and the intrinsic level  $E_I$ . The gate voltage  $V_g$  which determines the Fermi level position at the interface induces a space charge and band bending. The ac signal causes a periodic change in band bending and the gate bias determines the energy level position where the Fermi level oscillates at the interface. The traps with energy levels near the Fermi level are capable of changing their occupancy. The conductance is representing the loss mechanism due to interface trap capture and emission of carriers. The equivalent circuit of MOSCAP with interface states in depletion region appropriate for the conductance method is simplified as shown in **Fig. 2.21 (b)**. It consists of the gate oxide capacitance,  $C_{ox}$ , the semiconductor capacitance,  $C_{dos}(\omega, \psi_s)$ , the interface trap capacitance,  $C_{it}(\omega, \psi_s)$ , equivalent parallel conductance,  $G_p(\omega, \psi_s)$  and a series resistance,  $R_s$ . The simplified circuit model supposes the minority carrier response is negligible. The equivalent circuit of impedance analyzer with the

measured capacitance  $C_m$  and conductance  $G_m$  is shown in **Fig. 2.21 (c)**. The frequency dependence is related with the characteristic trap response time,  $\tau=2\pi/ \omega$ , where  $\omega$  is the angular frequency (  $f$  is measured frequency).

The interface trap capacitance which is induced by the interface state density is

$C_{it} = qD_{it}$ , where  $q$  is the elemental charge. The trap response time for hole is given by Shockley-Read-Hall statistics of capture and emission rate:

$$\tau_h = (\sigma v_{th,h} N_v)^{-1} \exp \left[ \frac{E_t - E_v}{k_B T} \right] \quad (2.2)$$

where  $E_t$  is the trap energy level in the band gap,  $\sigma$  is the capture cross section,  $v_{th,h}$  is the average thermal velocity of majority carriers (hole),  $N_v$  is the effective DOS of the majority carrier (hole) band,  $k_B$  is the Boltzmann constant, and  $T$  is the temperature.

The conductance method is the way of analyzing the loss that is caused by the variation in the trap level charge state. In fact, interface trap are continuously distributed all over the band gap rather than single energy level. Capture and emission occurs chiefly by traps located within a few  $kT/q$  above and below the Fermi level, giving rise to a time constant dispersion and indicating the normalized conductance as follows:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln \left[ 1 + (\omega\tau_{it})^2 \right] \quad (2.3)$$

The circuit from **Fig. 2.21 (b)** to **(c)** gives  $G_p/\omega$  in terms of the oxide capacitance  $C_{ox}$ , the measured capacitance  $C_m$ , and the measured conductance  $G_m$ , are shown as follows:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (2.4)$$

An approximate expression given the interface trap density in terms of the measured maximum conductance is:

$$D_{it} \approx \frac{2.5}{Aq} \left( \frac{G_p}{\omega} \right)_{\max} \quad \text{as } \omega\tau_{it} \approx 2 \quad (2.5)$$

where  $A$  is the device area. In addition,  $E_t$  can be determined at the specific frequency from  $(G_p/\omega)_{max}$  and applying **Eq. (2.2)**. **Fig. 2.22** shows the behavior of the interface trap time constant at room temperature as a function of capture cross section, which determines the part of interface traps in the band gap observable in the MOS admittance characteristic. **Fig. 2.23** shows trap level position calculated from **Eq. (2.2)** using the values for the average thermal velocity and the density of state band for  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  and a capture cross section  $\sigma = 1 \times 10^{-17} \text{ cm}^2$ , which chosen from **Fig. 2.22**. The trap characteristic frequency as a function of temperature determines the part of interface traps in the band gap conspicuously in the MOS admittance characteristic. Because of the representative measurement frequency between 100 Hz and 1 MHz, it's difficult to extract the interface state density over the whole band gap at room temperature. Nevertheless, the  $D_{it}$  of whole band gap profiles can be extracted by measuring in the various temperatures. For  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ , the traps near midgap could be observed at room temperatures. However, if we want to determine the traps which close to the band edges, we have to measure the impedance at lower temperature because of the increasing of the trap response time. Next section, we extract  $D_{it}$  at room temperature and compare the influence of the interface state with various PDA conditions in same  $\text{Al}_2\text{O}_3$  inter-layer and various  $\text{Al}_2\text{O}_3$  cycles at same PDA conditions. As well correspond to XPS interfacial chemical properties.

### 2.5.1 MOSCAPs with FGA under Various PDA Conditions

**Fig 2.24 (a) (b) (c) (d)** show parallel conductance maps of  $p$ -type Pt/Ti/TMA+ $\text{Al}_2\text{O}_3$  1cycle+ $\text{ZrO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  MOSCAPs with FGA under different PDA conditions, at temperature 300K. The  $D_{it}$  is estimated by the multiple peak values of the curves, which indicate the maximum of  $[(G_p/\omega)/Aq]$  with a factor of 2.5[see **Eq. 2.5**]. In **Fig 2.24**, all maps



show distinct signal at the gate voltage between -1 and -2 volts and lower frequency. We speculate that these responses might be the bulk oxide traps or slow traps, resulting in high frequency dispersion at  $V_g = -2$  volts, which is consistent with aforementioned section. Among these plots, we can find the color variation in this region is more indistinct with PDA 300 °C. However, because of a great deal of slow traps signal at accumulation region, the response of  $D_{it}$  at depletion region is suppressed and results in more invisible signal. Therefore, the  $[(G_p/\omega)/Aq]-f$  curves from **Fig. 2.25** are demonstrated here, and the interface states can be acquired with the factor of 2.5. From these curves, we can find that the peak value is getting larger as increasing PDA temperature. From **Fig. 2.30 (a)** and **Table 2.4**, it is observed that the  $D_{it}$  of PDA 300 °C is slightly smaller than the as-deposited one, but mostly better than PDA 400 °C and 500 °C. Accordingly, higher PDA temperature should be avoided so as to prevent the inferior native oxide and interface quality which might degrade electrical characteristics.

Furthermore, the parallel conductance maps of  $Al_2O_3$  5 cycles inter-layer are shown in **Fig. 2.26** and the  $[(G_p/\omega)/Aq]$  curves in **Fig. 2.27** with FGA under various PDA condition. These contour maps also show the slow traps at the high negative gate voltage, especially at PDA 500 °C. Because of the signal between  $V_g = -1$  and -2 volts at lower frequency is much stronger than the response of interface states, we can't see more obviously about the  $D_{it}$  signal. Then, we define the interface state quantitatively by **Fig. 2.27** and show in **Fig. 2.30 (b)** and **Table 2.4**. Compare to these values with various PDA temperatures, we demonstrate that the  $D_{it}$  at PDA 300 °C is much lower than others.

Moreover, from **Fig. 2.28** and **Fig. 2.29**, for  $Al_2O_3$  10cycles inter-layer, the signal of PDA 500 °C in accumulation region is apparent and the peak of the  $[(G_p/\omega)/Aq]$  curves is more seriously. Then, from **Fig. 2.30 (c)** and **Table 2.4**, these values indicate that the PDA 300 °C one is the best case of all the samples.

In order to be convinced of the conclusion which the PDA 300 °C is the best one of all the conditions and to prevent more  $Al_2O_3$  inter-layer from interfering with the signal between



ALD-TMA/Al<sub>2</sub>O<sub>3</sub> and Al<sub>2</sub>O<sub>3</sub>/ZrO<sub>2</sub> interface, we analyze the interfacial chemistry characteristics of ALD-TMA/Al<sub>2</sub>O<sub>3</sub> 1 cycle/ZrO<sub>2</sub> on p-type In<sub>0.53</sub>Ga<sub>0.47</sub>As with FGA under different PDA conditions.

XPS spectra were taken by Ga 2p<sub>3/2</sub>, In 3d<sub>5/2</sub>, and As 2p<sub>3/2</sub> core levels in **Fig. 2.35 (a) (b)**, and **(c)**. Deconvolution of XPS lines involves Shirley baseline removal and Lorentzian-Gaussian doublets as fitting components [38-40]. From **Fig. 2.35 (a)**, there is no significant variation in Ga 2p<sub>3/2</sub> spectra. Nevertheless, the In 3d<sub>5/2</sub> and As 2p<sub>3/2</sub> spectra show the presence of In- and As-oxide in both samples, are shown in **Fig. 2.35 (b) (c)**. Upon different annealing temperatures, it is possible that there are some oxygen bonds transfer processes from one oxidation to another. In other words, the As<sup>5+</sup> oxidation state is seen to undergo an oxygen transfer to the As<sup>3+</sup> with the small As<sup>2+</sup> state related component after specific annealing conditions. The As<sub>2</sub>O<sub>5</sub> portion of the native oxide decreases with the As<sub>2</sub>O<sub>3</sub> increases; this suggests that the arsenic oxides undergo a bond conversion from one form of arsenic oxide to another. However, the In<sup>3+</sup> and the InAsO<sub>4</sub> oxides are seen to increase, whereas there is an unobvious signal in the gallium oxide states suggesting this signal takes place as a result of oxygen bond transfers from gallium to indium. The **Table 2.5** shows the ratio of the fitted area such as In<sub>2</sub>O<sub>3</sub> to InAsO<sub>4</sub> from In 3d<sub>5/2</sub> spectra, As<sup>2+</sup> to As<sub>2</sub>O<sub>5</sub> and As<sub>2</sub>O<sub>3</sub> to As<sub>2</sub>O<sub>5</sub> from As 2p<sub>3/2</sub> spectra. With evidence in **Fig. 2.37 (a)**, these area ratio were compared to the electrical characteristics, we can illustrate that the better interface property is caused by the higher ratio values of the superior oxide. This phenomenon may be caused by the passivation of the trivalent oxides or lower valence As on the interface. Therefore, we can demonstrate that the PDA 300 °C is the best condition in our samples.

## 2.5.2 Comparison of Various Al<sub>2</sub>O<sub>3</sub> cycles with same PDA Conditions

**Fig. 2.31** shows the comparison of D<sub>it</sub> profiles of ALD-TMA/ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As

MOSCAPs with various Al<sub>2</sub>O<sub>3</sub> inter-layers at the same PDA conditions, which are measured at 300K. These diagrams show that incorporating more Al<sub>2</sub>O<sub>3</sub> inter-layers with ALD-TMA/ZrO<sub>2</sub>, the oxide and interface quality will be more improvable, especially at PDA 300 °C. It indicates that the interface could be passivated within Al<sub>2</sub>O<sub>3</sub>. Therefore, we further compare the electrical properties of ALD-TMA/ZrO<sub>2</sub> case which means Al<sub>2</sub>O<sub>3</sub> 0cycle inter-layer [see **Fig. 2.32**] and the ALD-TMA/Al<sub>2</sub>O<sub>3</sub> case which means all of the gate dielectric is composed of Al<sub>2</sub>O<sub>3</sub> [see **Fig. 2.33**] with Al<sub>2</sub>O<sub>3</sub> 1,5, and 10 cycles inter-layer under PDA 300 °C/120s, w/FGA. From **Fig. 2.34** and **Table 2.4**, we notice that thicker Al<sub>2</sub>O<sub>3</sub> might passivate the In<sub>0.53</sub>Ga<sub>0.47</sub>As surface, the oxide and interface quality might be improved [41]. In addition, we will analyze the interfacial chemistry characteristics of ALD-TMA/ZrO<sub>2</sub> with various Al<sub>2</sub>O<sub>3</sub> inter-layers under PDA 300 °C to prove the aforementioned results.

The Ga 2*p*<sub>3/2</sub>, In 3*d*<sub>5/2</sub>, and As 2*p*<sub>3/2</sub> core levels of XPS spectra are reported in **Fig. 2.36 (a)**, **(b)**, and **(c)** for ALD-TMA/Al<sub>2</sub>O<sub>3</sub> 0, 1, 5, 10cycle/ZrO<sub>2</sub> 10cycle on p-type In<sub>0.53</sub>Ga<sub>0.47</sub>As, respectively, except the top one. It is found that the signal of Ga 2*p*<sub>3/2</sub> spectra hardly depends on the various Al<sub>2</sub>O<sub>3</sub> inter-layer. However, we can notice the variation at the In 3*d*<sub>5/2</sub> and As 2*p*<sub>3/2</sub> spectra. When increasing Al<sub>2</sub>O<sub>3</sub> inter-layers, the As<sub>2</sub>O<sub>5</sub> decreases with the As<sub>2</sub>O<sub>3</sub> and As<sup>2+</sup> increase. It indicates that the more Al<sub>2</sub>O<sub>3</sub> layer tend to displace the As<sup>5+</sup> oxidation state to the As<sup>3+</sup> and As<sup>2+</sup>. From **Table 2.6**, we can see that the area ratio of In<sub>2</sub>O<sub>3</sub> to InAsO<sub>4</sub>, As<sup>2+</sup> to As<sub>2</sub>O<sub>5</sub>, and As<sub>2</sub>O<sub>3</sub> to As<sub>2</sub>O<sub>5</sub> increase when inserting Al<sub>2</sub>O<sub>3</sub> 10cycles between the ZrO<sub>2</sub> and the In<sub>0.53</sub>Ga<sub>0.47</sub>As interface. To further demonstrate the connection between electrical and chemical characteristics of the interface, we combine the density of interface state with the area ratio in the profile. From **Fig. 2.37 (b)**, it shows that the interface can be effectively passivated by trivalent oxides such as Al<sub>2</sub>O<sub>3</sub> and As<sub>2</sub>O<sub>3</sub> without generating a large amount of dangling bonds [42]. Consequently, we show that the Al<sub>2</sub>O<sub>3</sub> 10cycles inter-layer condition is better than other conditions.

## 2.6 Summary

In the past, poor gate dielectric quality and interface among oxide/semiconductor could results in frequency dispersion, hysteresis, and inferior interface property. Therefore, first of all, we demonstrate the TMA precursor of ALD can achieve more self-cleaning capability than TEMAZ at the oxide/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  interface. Furthermore, various  $\text{Al}_2\text{O}_3$  inter-layers with FGA under different PDA conditions have been conferred. According to the electrical characteristics of frequency dispersion and hysteresis, the capacitor under PDA 300 °C with FGA displays the better property than other temperatures. This result indicates that proper temperature of PDA is important due to the higher temperature might produce inferior native oxide like  $\text{As}_2\text{O}_5$  or  $\text{InAsO}_4$  from XPS analysis which gives rise to higher  $D_{it}$  existed in midgap from the extraction of the conductance method. In addition, more  $\text{Al}_2\text{O}_3$  cycles inserting among ALD-TMA/ $\text{ZrO}_2$  show the optimum electrical performance. It is observed that the interface of  $\text{ZrO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  is effectively passivated by trivalent oxides such as  $\text{Al}_2\text{O}_3$  and  $\text{As}_2\text{O}_3$  without generating a large amount of dangling bonds and demonstrate that the interface have better quality.



## Reference (Chapter 2)

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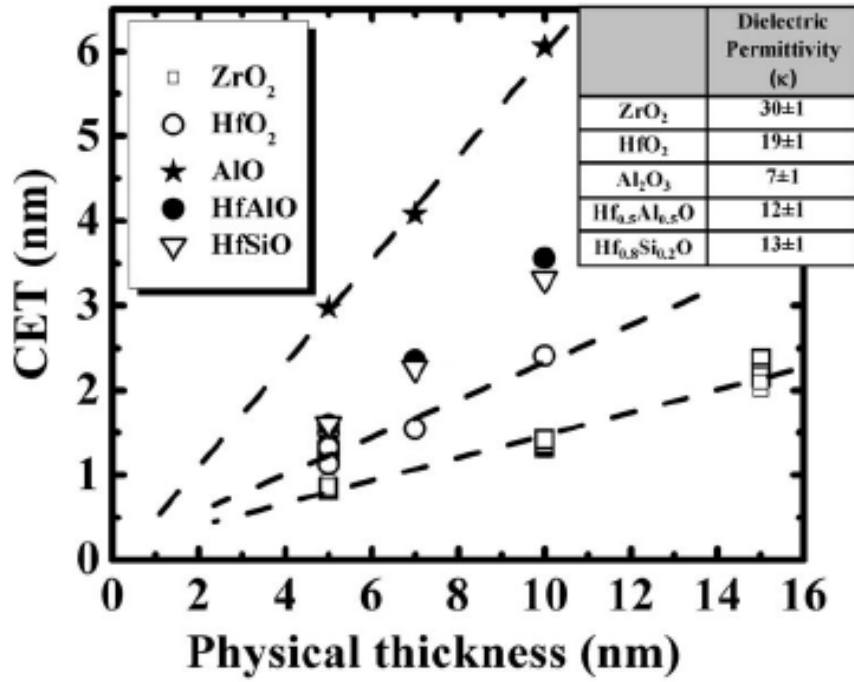
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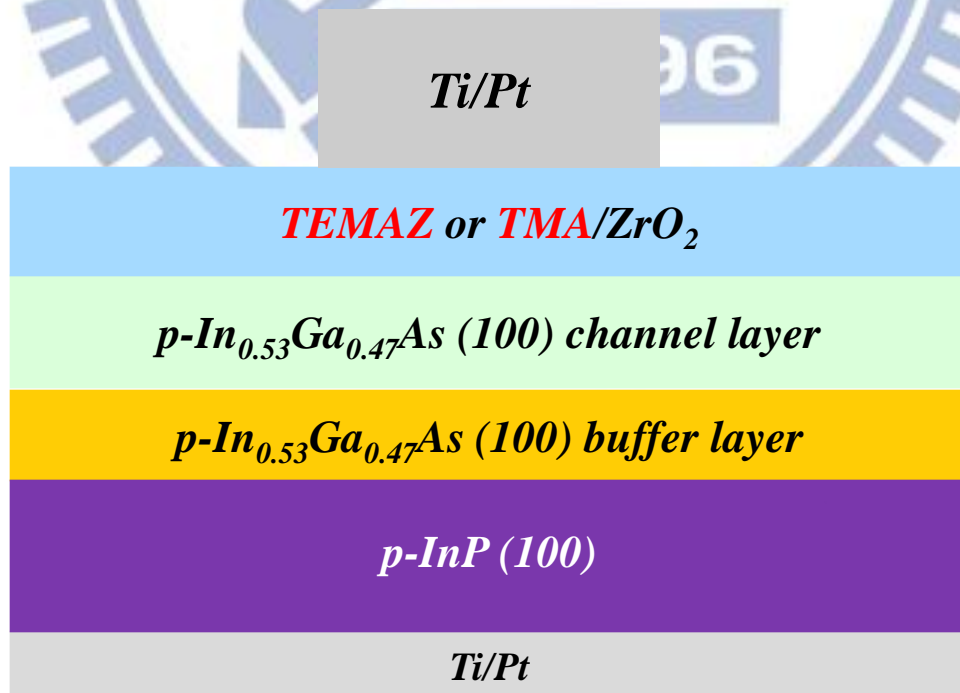
**Fig. 2.1** Capacitive equivalent thickness (CET) vs. physical thickness as measured in a MOSCAPs for various ALD dielectrics on In<sub>0.53</sub>Ga<sub>0.47</sub>As.

Gate dielectric(ALD)	$\Delta E_v$ (eV)	$\Delta E_c$ (eV)	$E_g$ (eV)
ZrO <sub>2</sub>	2.63±0.1	2.13±0.3	5.5±0.2
HfO <sub>2</sub>	3.04±0.1	1.8±0.3	5.6±0.2
Al <sub>2</sub> O <sub>3</sub>	4.09±0.1	2.8±0.3	7.65±0.2

**Table 2.1** Band offsets of various dielectrics with respect to In<sub>0.53</sub>Ga<sub>0.47</sub>As as measured by synchrotron radiation photoelectron spectroscopy.

- **Surface pretreatment**
  - Acetone (5min)
  - Isopropanol (5min)
  - HCl : H<sub>2</sub>O = 1:10 (2min)
- **Deposited by ALD at 250 °C**
  - **TEMAZ or TMA** 10cycles pretreatment
  - ZrO<sub>2</sub> 80 cycles.
- **Annealing condition**
  - PDA (300.400.500°C/120s)
- **Gate electrode patterning and formation(Ti/Pt)**
- **Backside-contact deposition (Ti/Pt)**
- **FGA 10% H<sub>2</sub>+90% N<sub>2</sub> (250°C/30min.)**

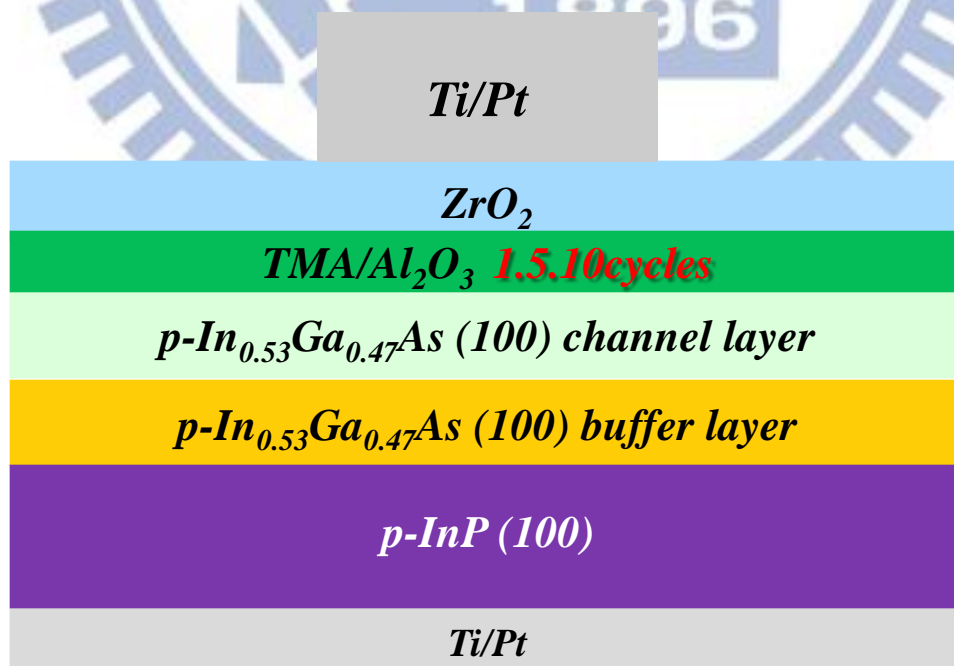
**Fig. 2.2** Process flow of MOSCAPs with different surface pretreatments.



**Fig. 2.3** MOSCAPs structure with ALD-TEMAZ or TMA/ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As.

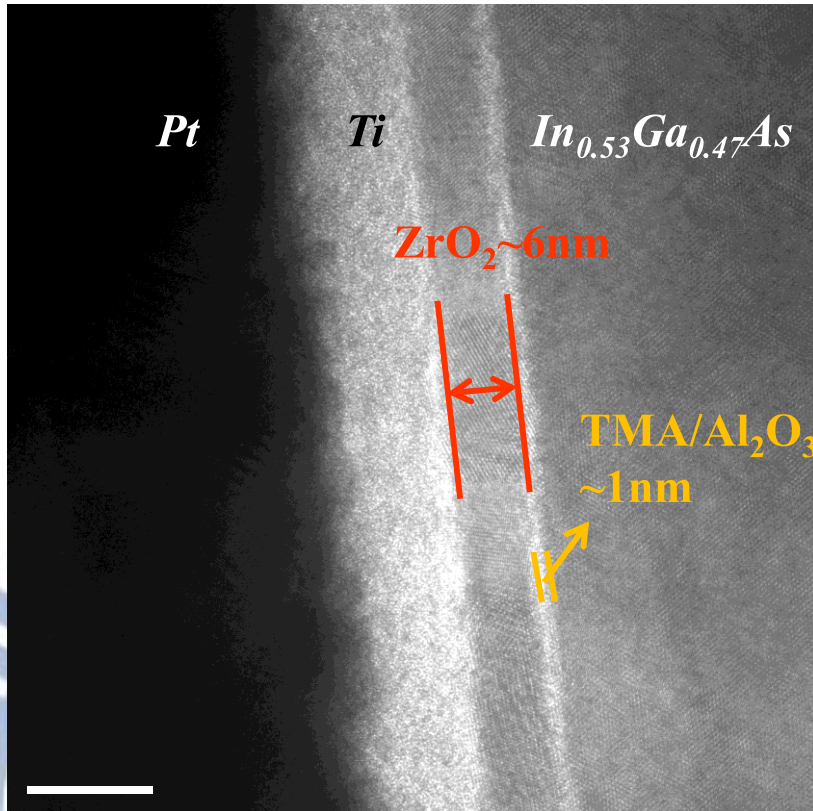
- **Surface pretreatment**
  - Acetone (5min)
  - Isopropanol (5min)
  - HCl : H<sub>2</sub>O = 1:10 (2min)
- **Deposited by ALD at 250 °C**
  - TMA 10cycles
  - Al<sub>2</sub>O<sub>3</sub> **1.5.10** cycles
  - ZrO<sub>2</sub> 80 cycles.
- **Annealing condition**
  - as-deposited or PDA (300.400.500 °C/120s)
- **Gate electrode patterning and formation(Ti/Pt)**
- **Backside-contact deposition (Ti/Pt)**
- **FGA 10% H<sub>2</sub>+90% N<sub>2</sub> (250°C/30min.)**

**Fig. 2.4** Process flow of the MOSCAPs with several cycles of Al<sub>2</sub>O<sub>3</sub>.

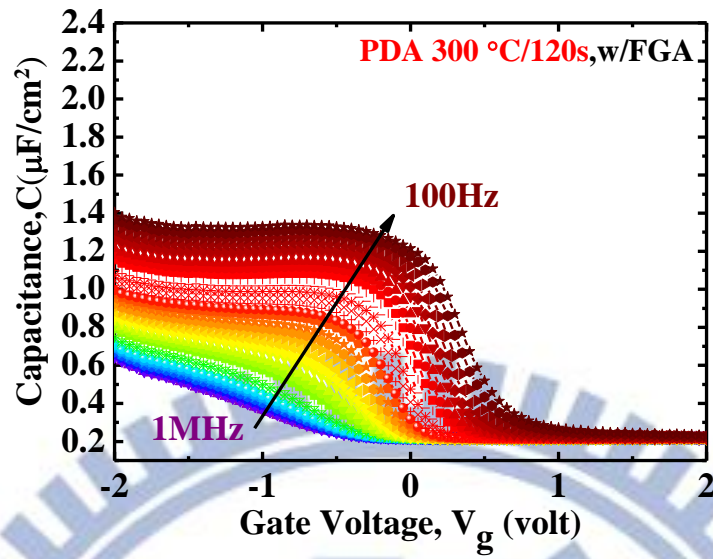


**Fig. 2.5** MOSCAPs structure with ALD-TMA/Al<sub>2</sub>O<sub>3</sub>/ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As.

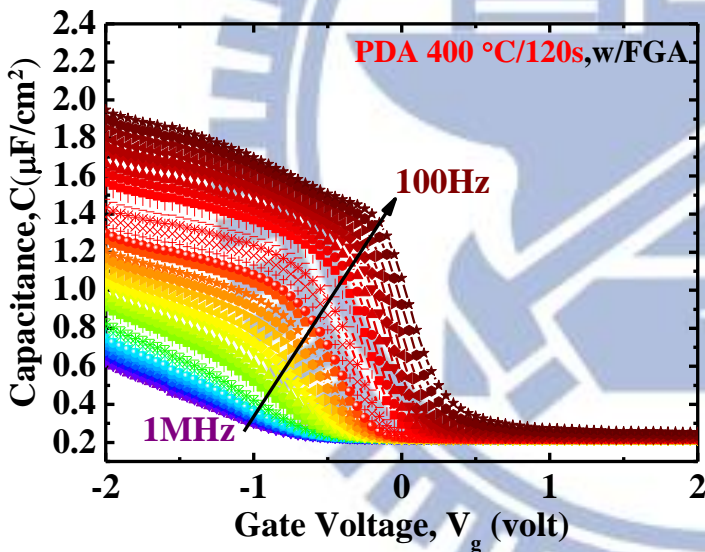




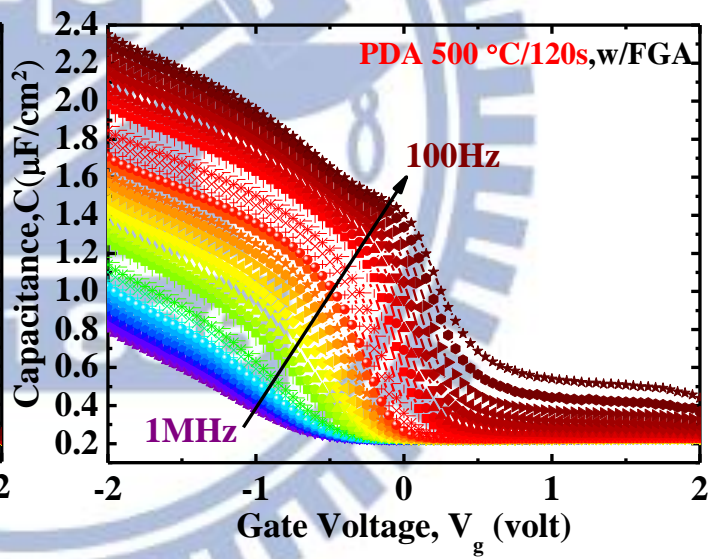
**Fig. 2.6** TEM image of the as-deposited ALD-TMA/ $Al_2O_3$  10 cycle/ $ZrO_2$  on  $In_{0.53}Ga_{0.47}As$  with FGA.



(a)

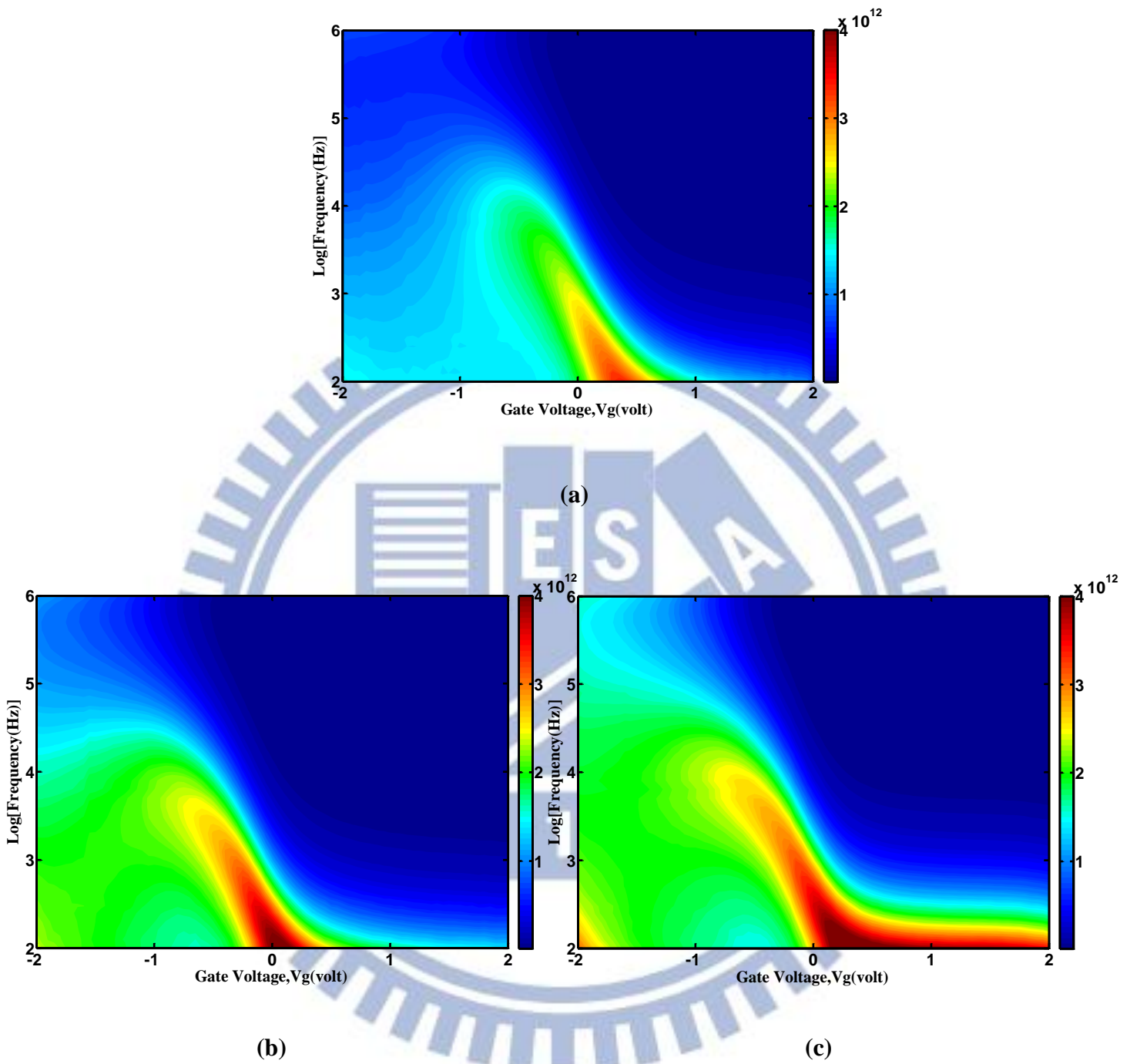


(b)

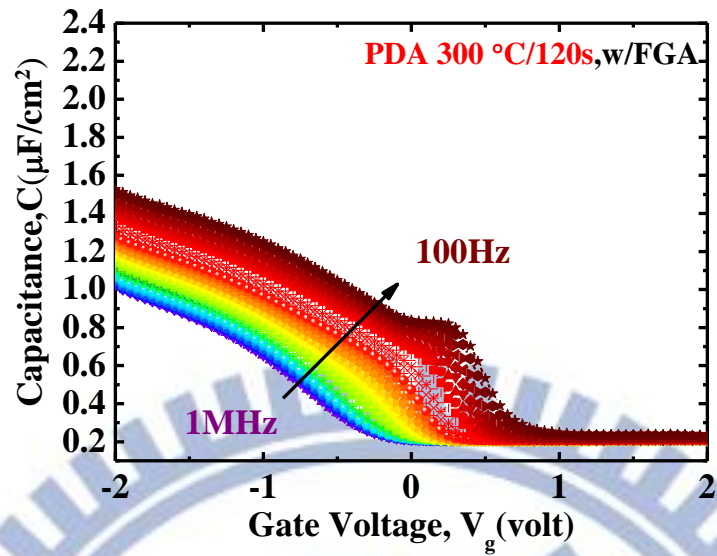


(c)

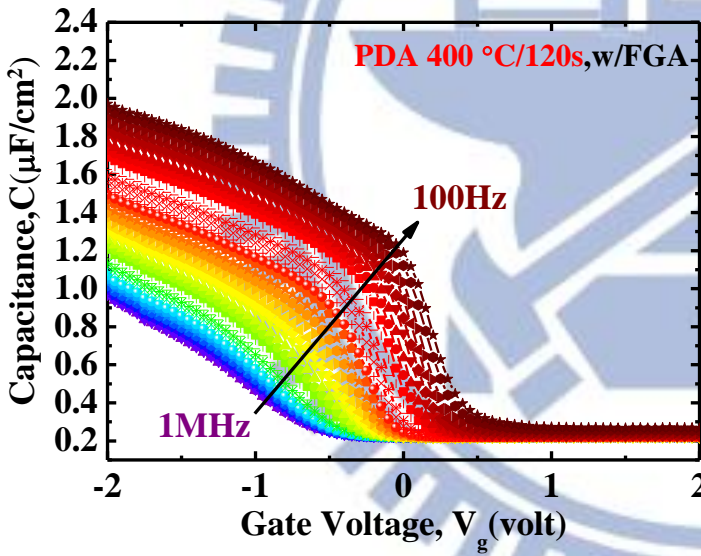
**Fig. 2.7** Multi-frequency  $C$ - $V$  curves for  $p$ -type Pt/Ti/TEMAZr+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in N<sub>2</sub> ambience for 120 s (a) 300 °C (b) 400 °C (c) 500 °C



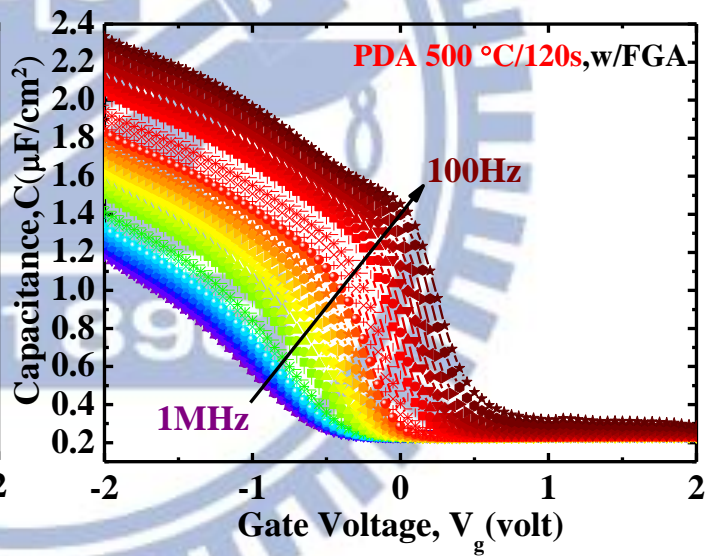
**Fig. 2.8** Map of normalized conductance  $G/A\omega q$  ( $\text{eV}^{-1}\text{cm}^{-2}$ ) vs.  $V_g$  (volt) for *p*-type Pt/Ti/TEMAZr+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in N<sub>2</sub> ambience for 120 s (a) 300 °C (b) 400 °C (c) 500 °C



(a)



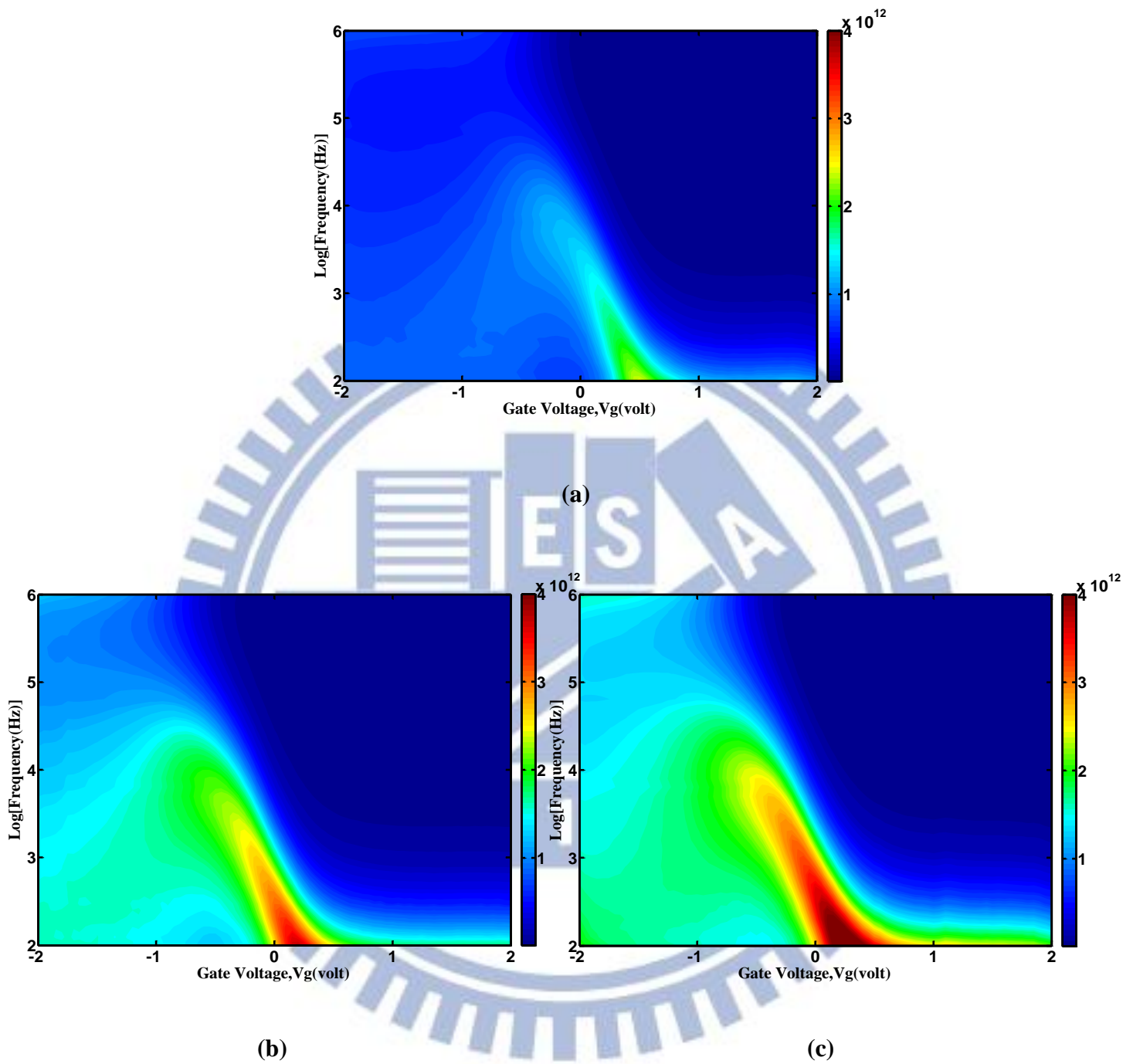
(b)



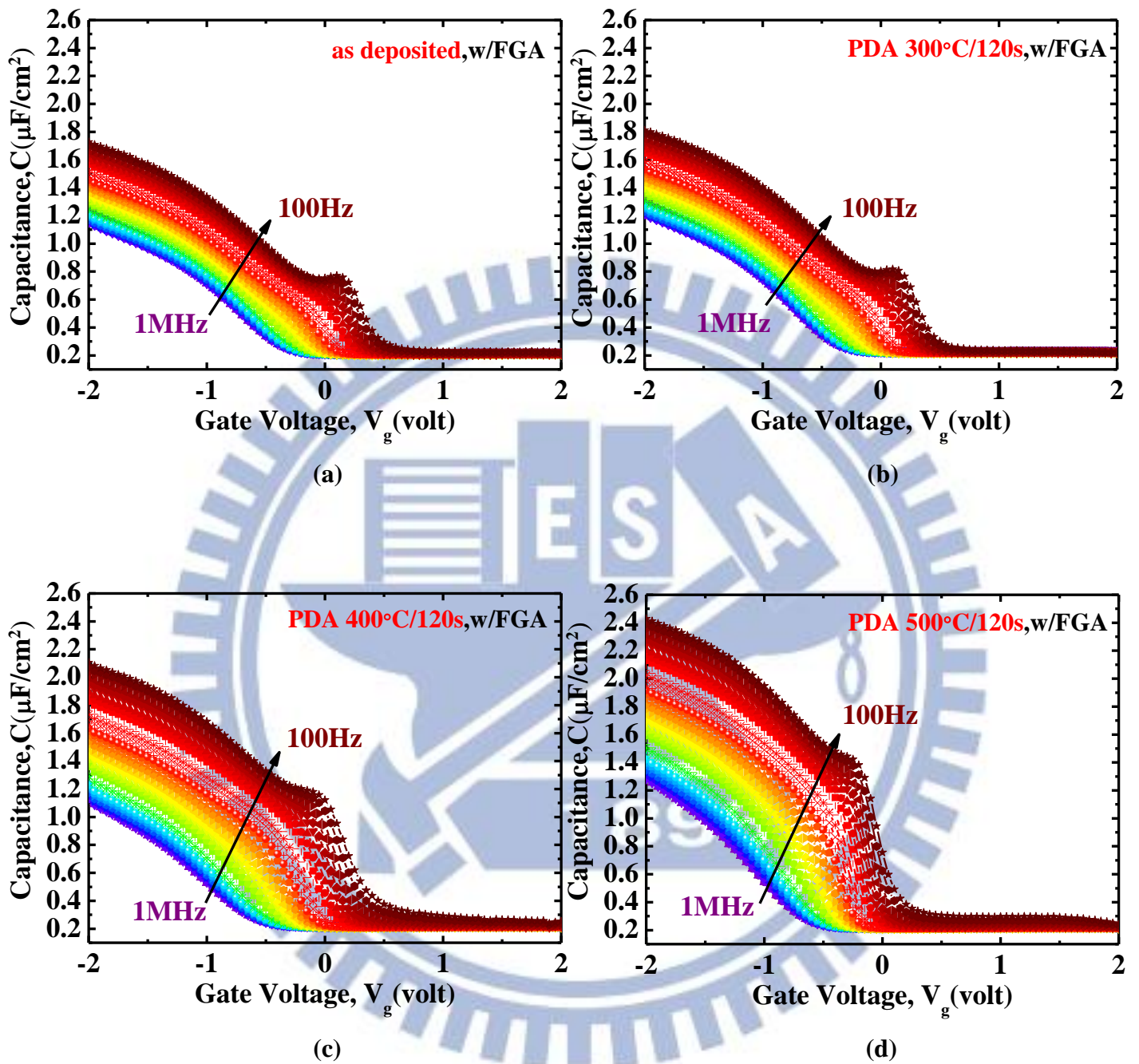
(c)

**Fig. 2.9** Multi-frequency  $C$ - $V$  curves for  $p$ -type Pt/Ti/TMA+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in N<sub>2</sub> ambience for 120 s (a) 300 °C (b) 400 °C (c) 500 °C.

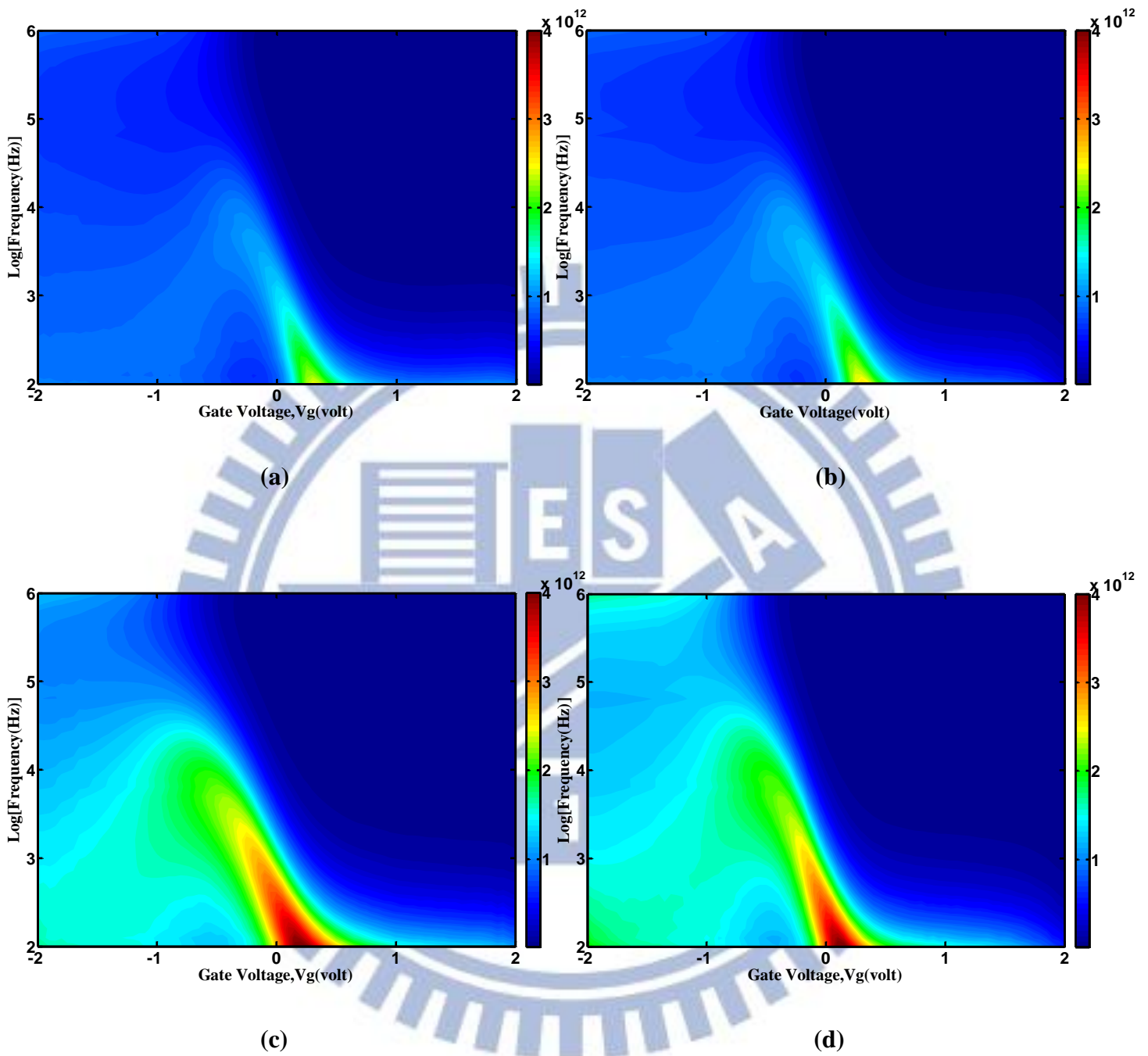




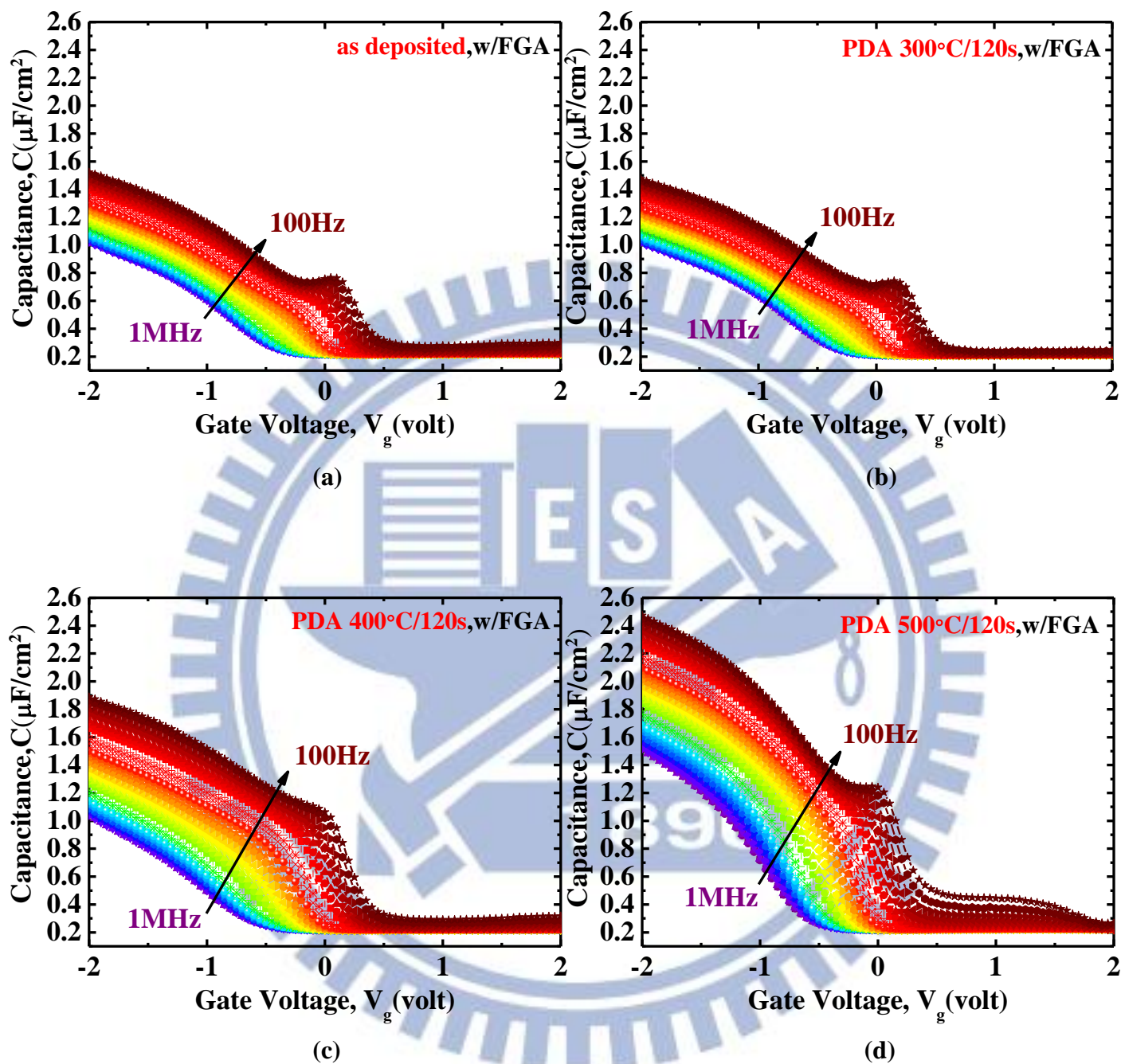
**Fig. 2.10** Map of normalized conductance  $G/A\omega q$  ( $\text{eV}^{-1}\text{cm}^{-2}$ ) vs.  $V_g$  (volt) for *p*-type Pt/Ti/TMA+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in N<sub>2</sub> ambience for 120 s (a) 300 °C (b) 400 °C (c) 500 °C



**Fig. 2.11** Multi-frequency  $C$ - $V$  curves for  $p$ -type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 1 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>-As MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in N<sub>2</sub> ambience for 120 s (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.

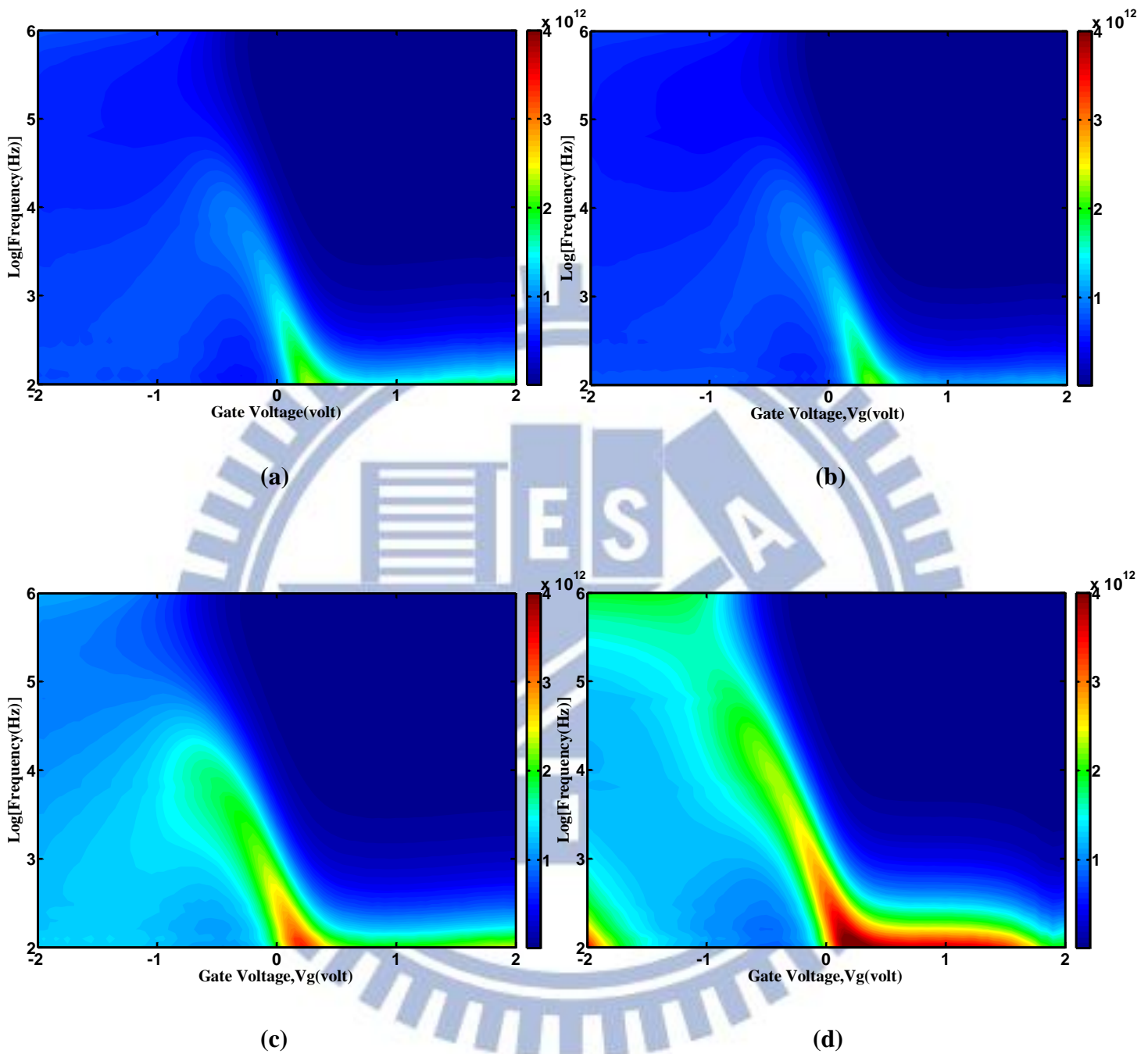


**Fig. 2.12** Map of normalized conductance  $G/A\omega q$  ( $\text{eV}^{-1}\text{cm}^{-2}$ ) vs.  $V_g$  (volt) for  $p$ -type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 1 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in N<sub>2</sub> ambience for 120 s (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.

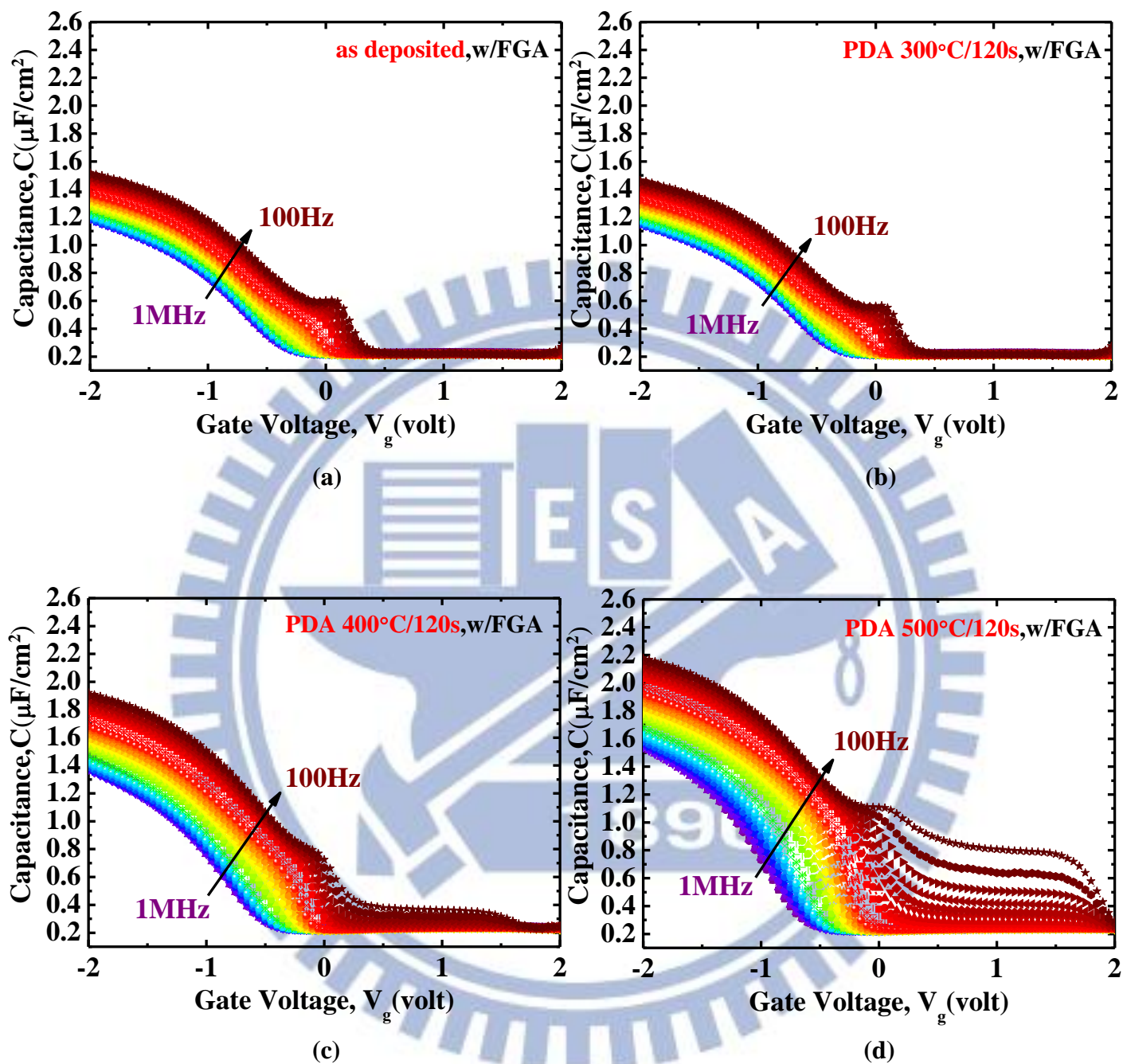


**Fig. 2.13** Multi-frequency  $C-V$  curves for  $p$ -type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 5 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>-As MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in N<sub>2</sub> ambience for 120 s (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.

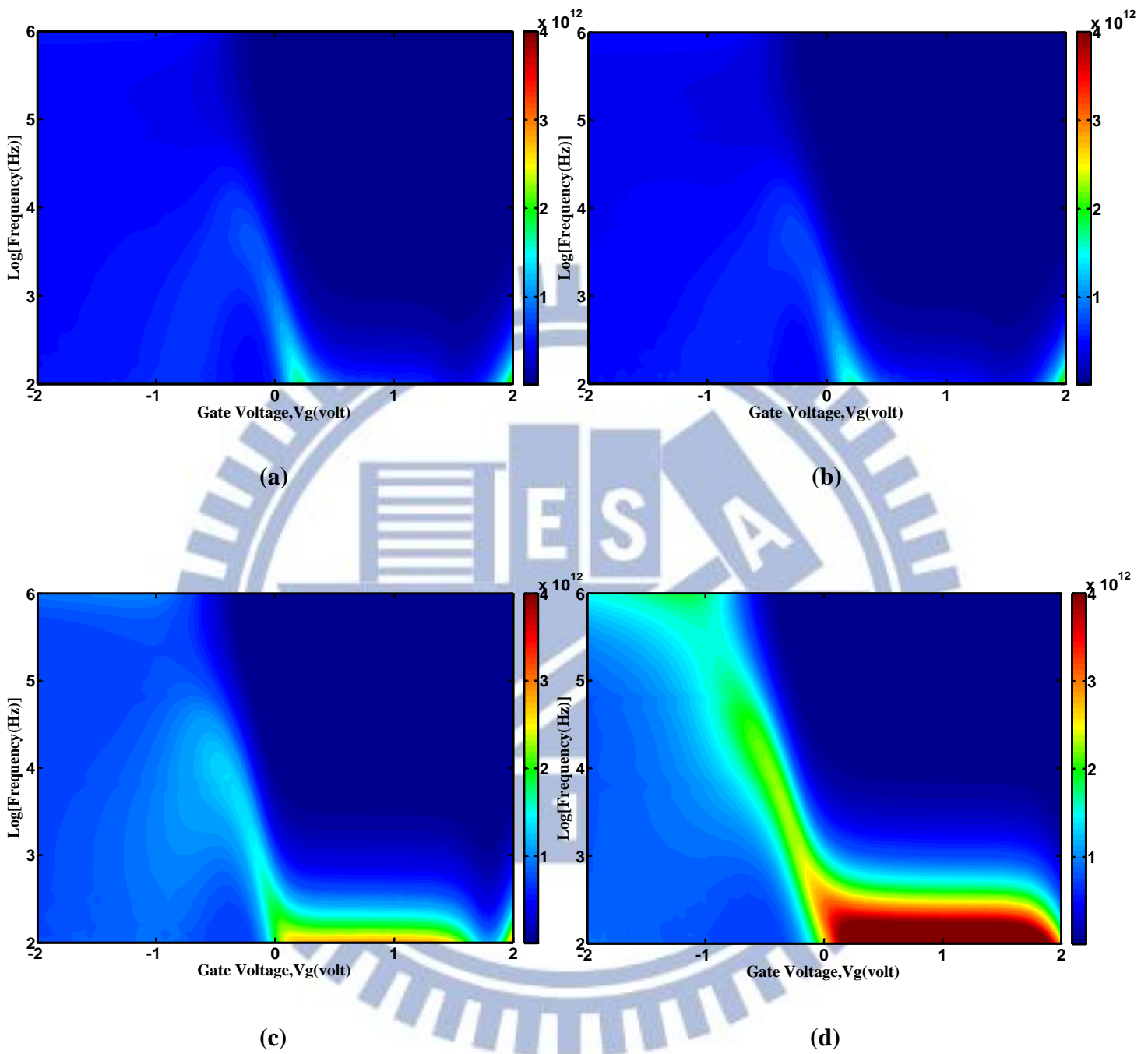




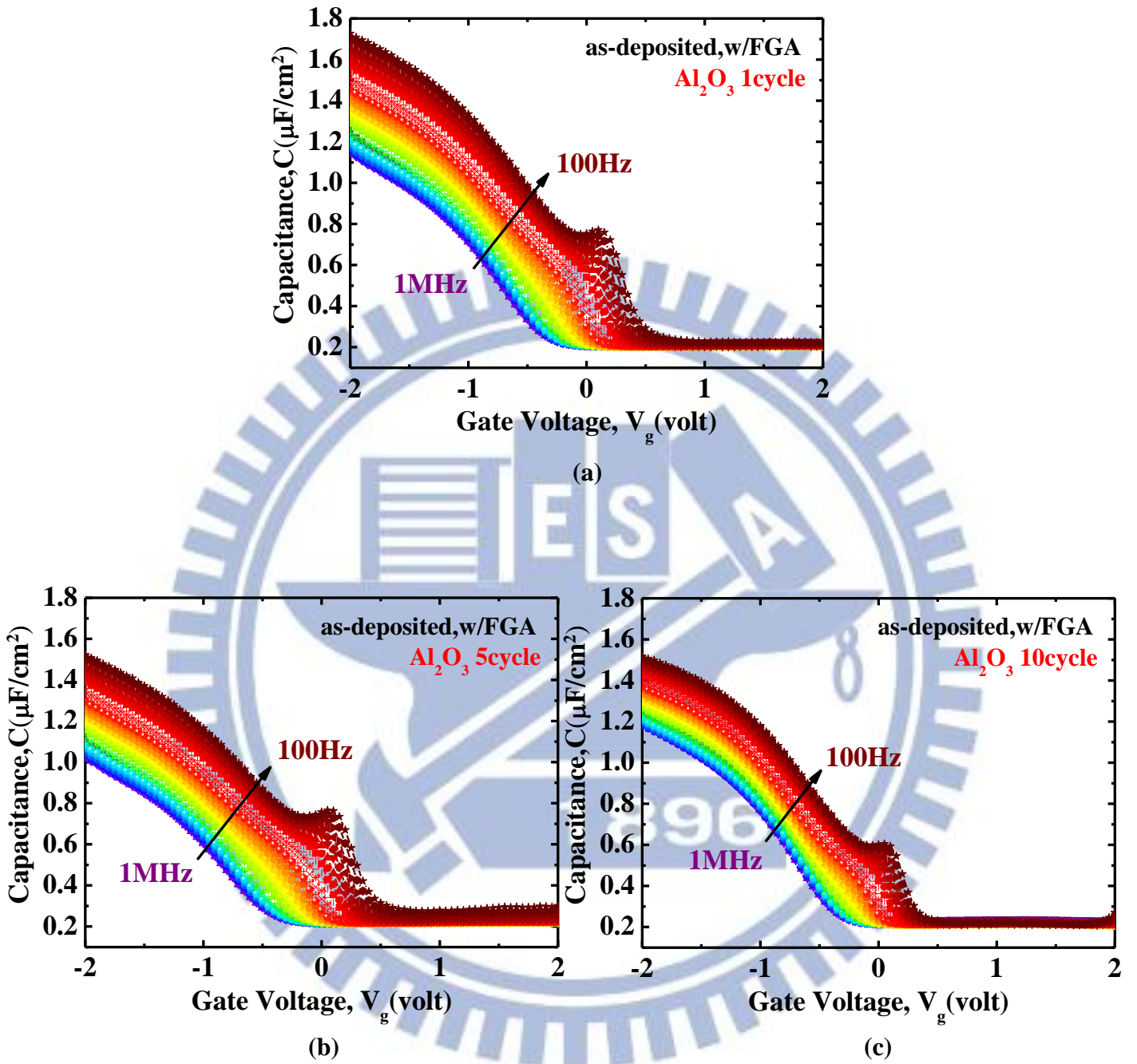
**Fig. 2.14** Map of normalized conductance  $G/A\omega q$  ( $eV^{-1}cm^{-2}$ ) vs.  $V_g$  (volt) for  $p$ -type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 5 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in N<sub>2</sub> ambience for 120 s (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.



**Fig. 2.15** Multi-frequency  $C$ - $V$  curves for  $p$ -type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 10 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga-<sub>0.47</sub>As MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in N<sub>2</sub> ambience for 120 s (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.

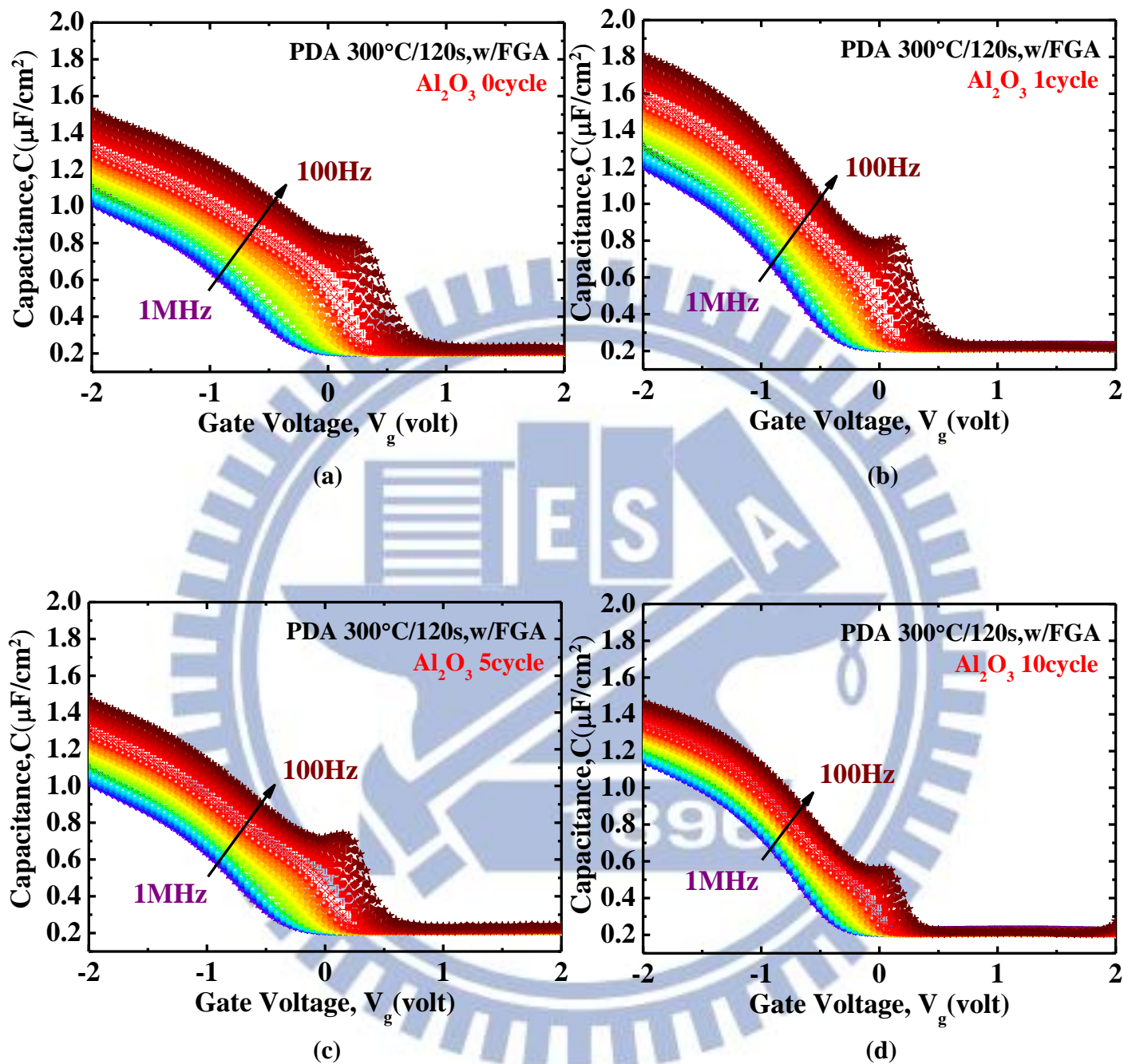


**Fig. 2.16** Map of normalized conductance  $G/A\omega q$  ( $eV^{-1}cm^{-2}$ ) vs.  $V_g$  (volt) for *p*-type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 10 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in N<sub>2</sub> ambience for 120 s (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.

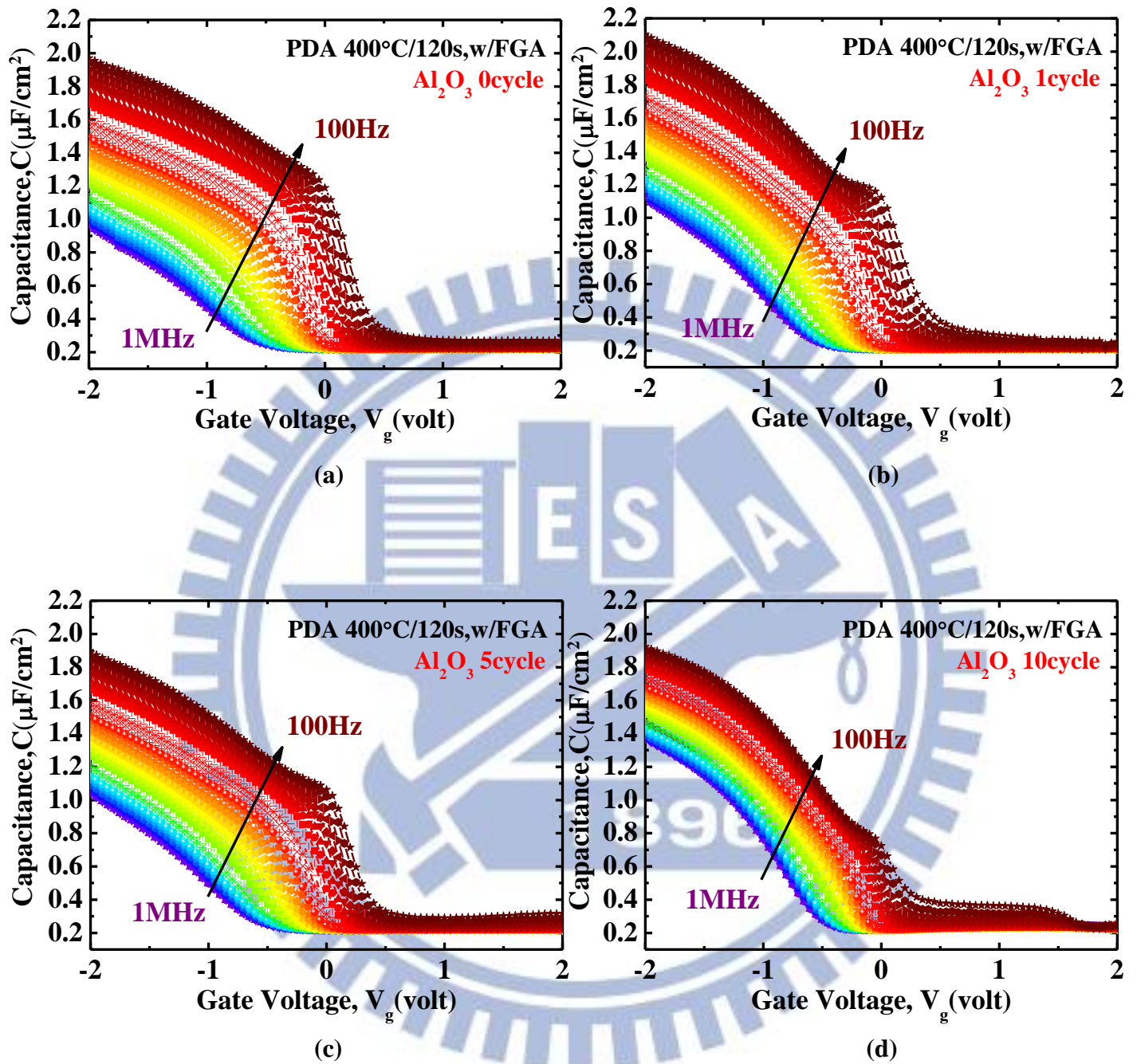


**Fig. 2.17** Multi-frequency C-V curves for various Al<sub>2</sub>O<sub>3</sub> cycles measured from 1 MHz to 100 Hz after FGA under as-deposited (a) Al<sub>2</sub>O<sub>3</sub> 1 cycle (b) Al<sub>2</sub>O<sub>3</sub> 5 cycle (c) Al<sub>2</sub>O<sub>3</sub> 10 cycle.

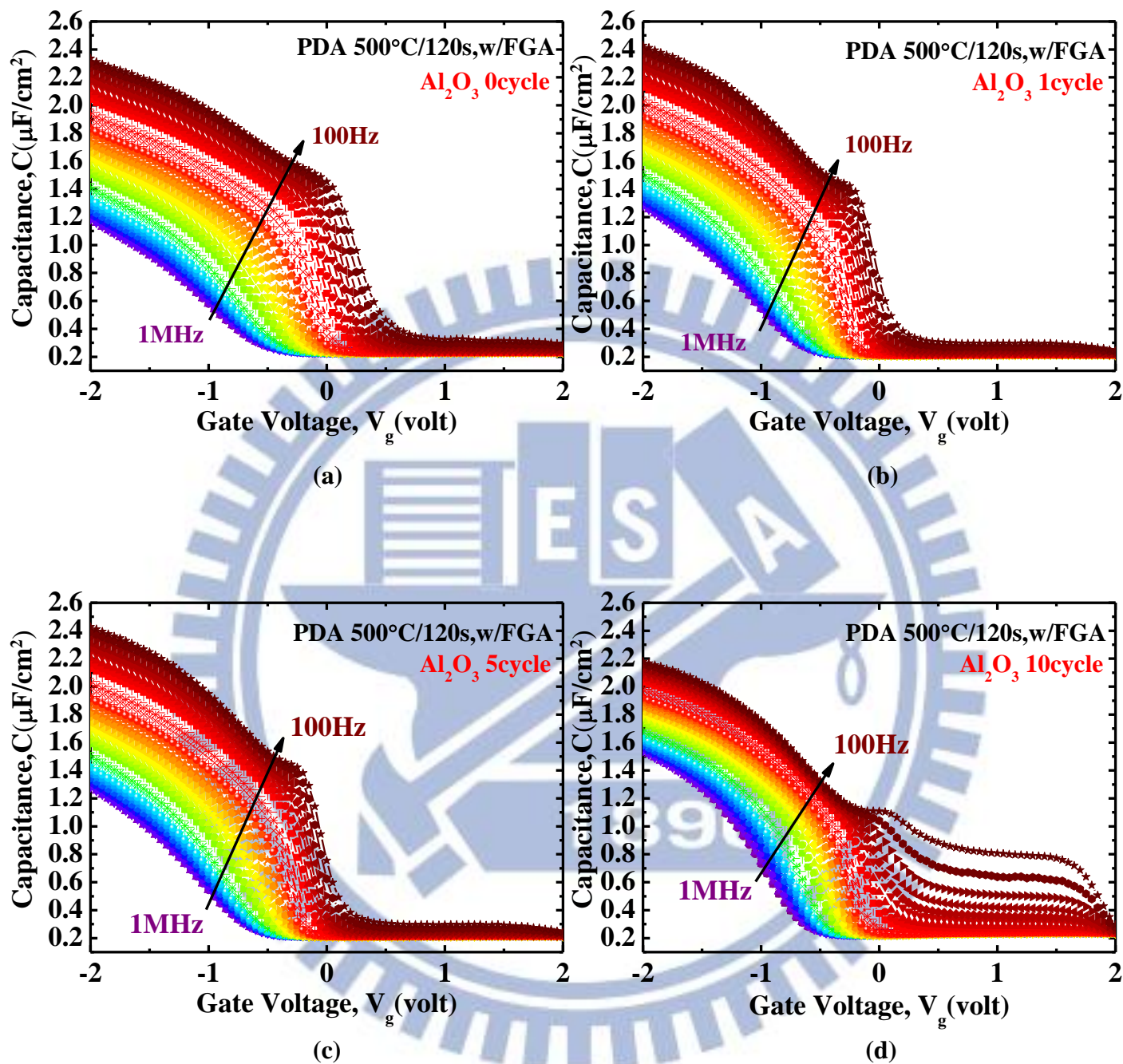




**Fig. 2.18** Multi-frequency  $C$ - $V$  curves for various  $\text{Al}_2\text{O}_3$  cycles measured from 1 MHz to 100 Hz after FGA under PDA 300 °C /120 s (a) TMA pretreatment ( $\text{Al}_2\text{O}_3$  0 cycle) (b)  $\text{Al}_2\text{O}_3$  1 cycle (c)  $\text{Al}_2\text{O}_3$  5 cycle (d)  $\text{Al}_2\text{O}_3$  10 cycle.



**Fig. 2.19** Multi-frequency C-V curves for various  $\text{Al}_2\text{O}_3$  cycles measured from 1 MHz to 100 Hz after FGA under PDA 400 °C /120 s (a) TMA pretreatment ( $\text{Al}_2\text{O}_3$  0 cycle) (b)  $\text{Al}_2\text{O}_3$  1 cycle (c)  $\text{Al}_2\text{O}_3$  5 cycle (d)  $\text{Al}_2\text{O}_3$  10 cycle.



**Fig. 2.20** Multi-frequency C-V curves for various  $\text{Al}_2\text{O}_3$  cycles measured from 1 MHz to 100 Hz after FGA under PDA 500 °C /120 s (a) TMA pretreatment( $\text{Al}_2\text{O}_3$  0 cycle) (b)  $\text{Al}_2\text{O}_3$  1cycle (c)  $\text{Al}_2\text{O}_3$  5 cycle (d)  $\text{Al}_2\text{O}_3$  10 cycle.



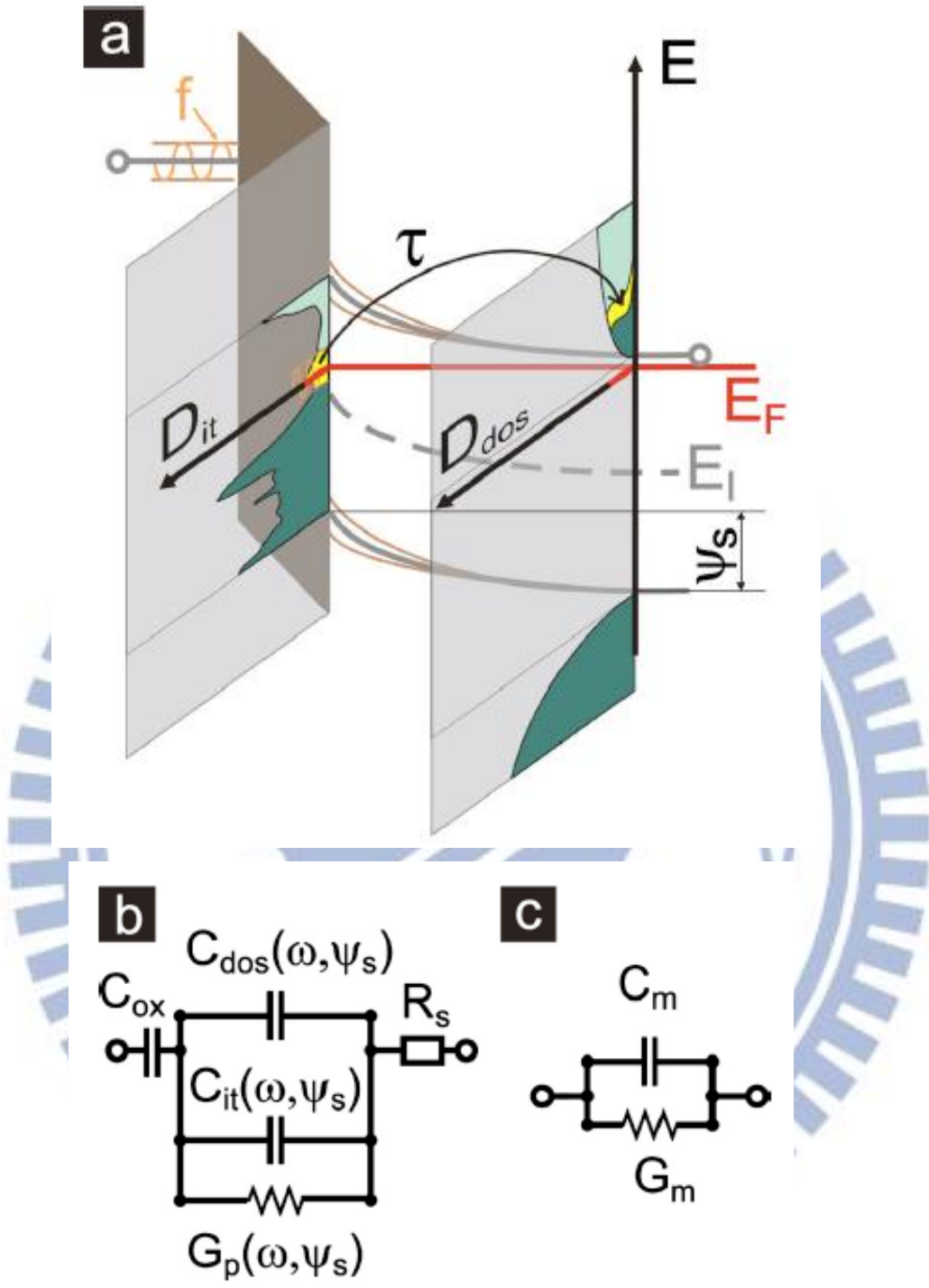
$\Delta C$ (@ $V_g = -2$ V) (w/FGA)	as-deposited	PDA 300 °C /120 s	PDA 400 °C /120 s	PDA 500 °C /120 s
TEMAZ		99.4%	160.9%	129.5%
TMA		42.7%	84.3%	75.9%
Al <sub>2</sub> O <sub>3</sub> 1cyc.	43.4%	41.7%	79.4%	55.7%
Al <sub>2</sub> O <sub>3</sub> 5cyc.	40.9%	37.8%	65.3%	46.7%
Al <sub>2</sub> O <sub>3</sub> 10cyc.	25.0%	24.4%	34.8%	33.6%

**Table 2.2** Overview of frequency dispersion  $\Delta C$  of various pretreatments and several Al<sub>2</sub>O<sub>3</sub> cycles with FGA under various PDA conditions at  $V_g = -2$  V.

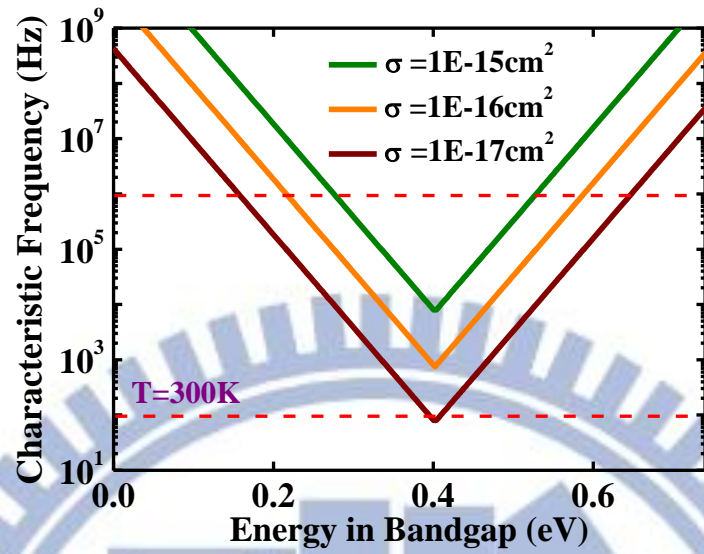
Hysteresis (V) (w/FGA)	as-deposited	PDA 300 °C /120 s	PDA 400 °C /120 s	PDA 500 °C /120 s
TEMAZ		0.96	0.76	0.61
TMA		0.59	0.74	0.66
Al <sub>2</sub> O <sub>3</sub> 1cyc.	0.49	0.44	0.70	0.54
Al <sub>2</sub> O <sub>3</sub> 5cyc.	0.48	0.43	0.62	0.46
Al <sub>2</sub> O <sub>3</sub> 10cyc.	0.31	0.29	0.43	0.37

**Table 2.3** Overview of hysteresis (V) of various pretreatments and several Al<sub>2</sub>O<sub>3</sub> cycles with FGA under various PDA conditions.

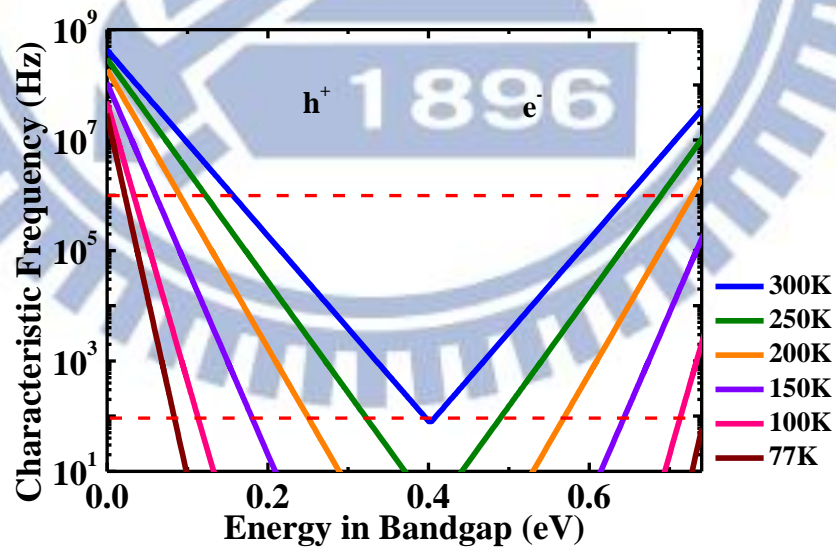




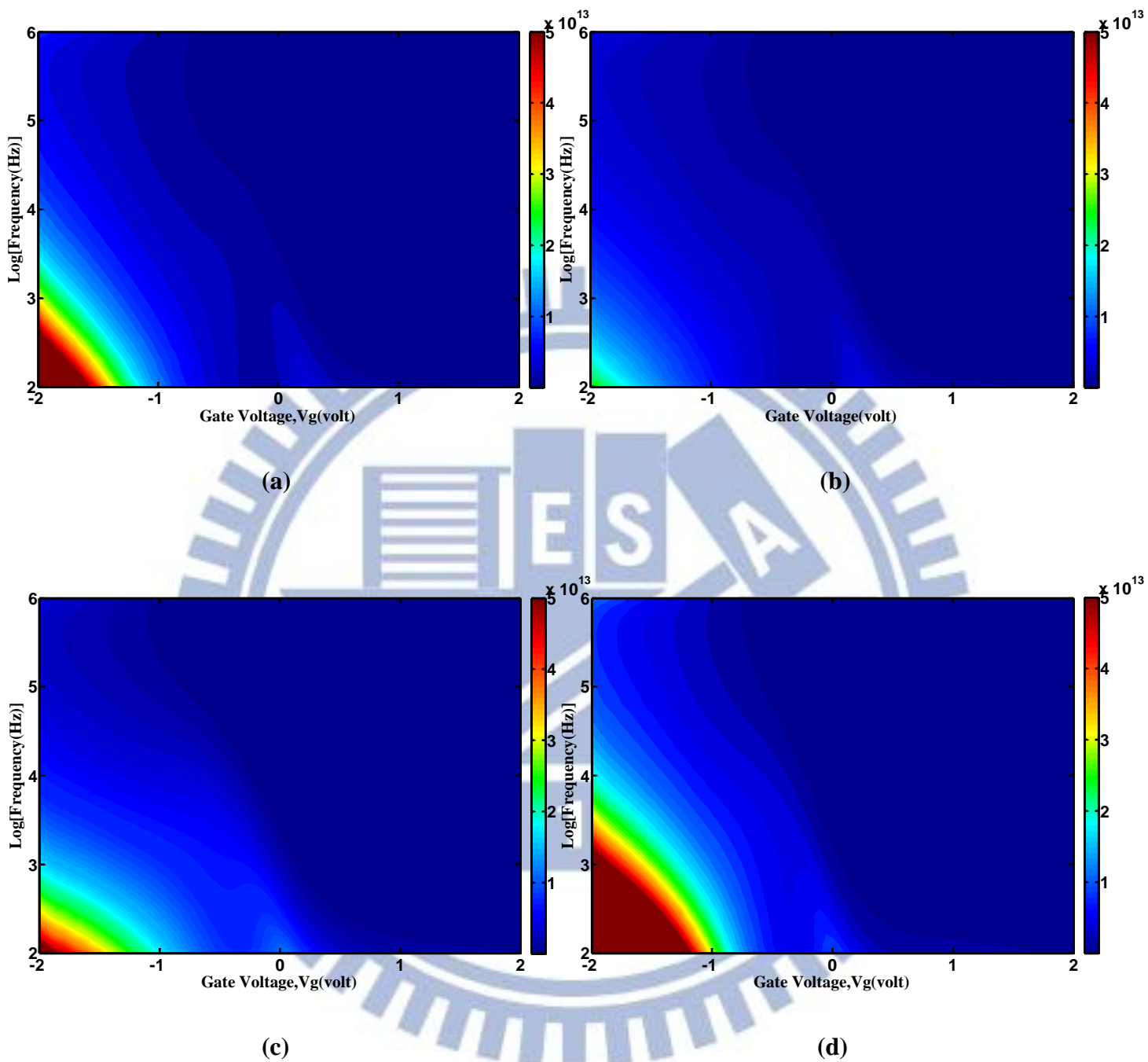
**Fig. 2.21** Energy band diagram of a  $n$ -type MOSCAPs in depletion region is shown in (a). A dc gate bias  $V_g$  with a small ac signal of frequency  $f$  are applied, causing a band bending  $\psi_s$  in the semiconductor and interface trap response with time constant  $\tau$ . (b) Equivalent circuit of MOSCAPs in depletion region. (c) Measured capacitance  $C_m$  and conductance  $G_m$ .



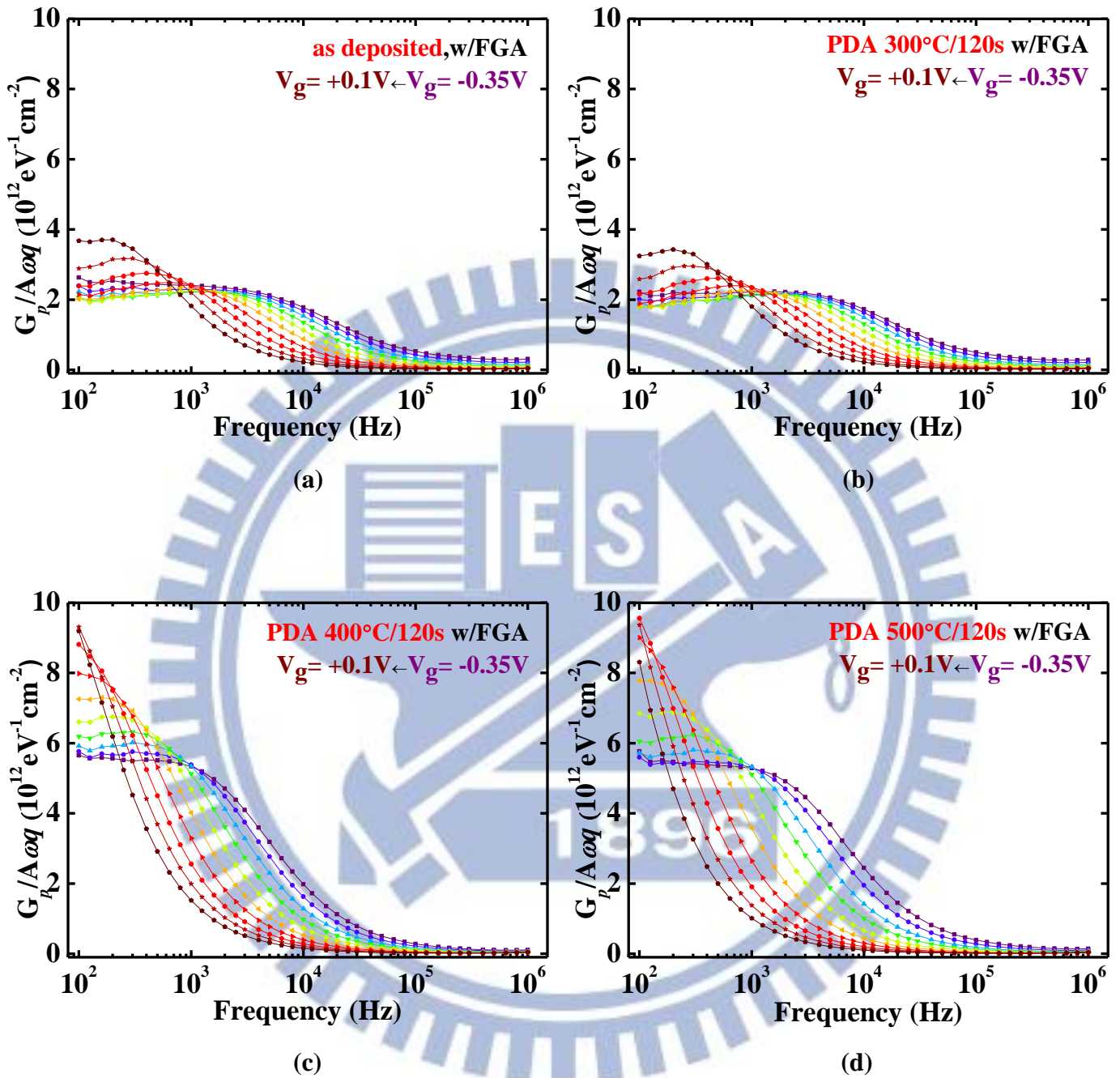
**Fig. 2.22** Behavior of the interface trap time constant at room temperature as a function of capture cross section determines the part of interface traps in the band gap observable in the MOS admittance characteristics.



**Fig. 2.23** The trapped charge characteristics for  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  under different temperature and corresponding measurement window from 1 MHz to 100 Hz C-V measurement frequency.

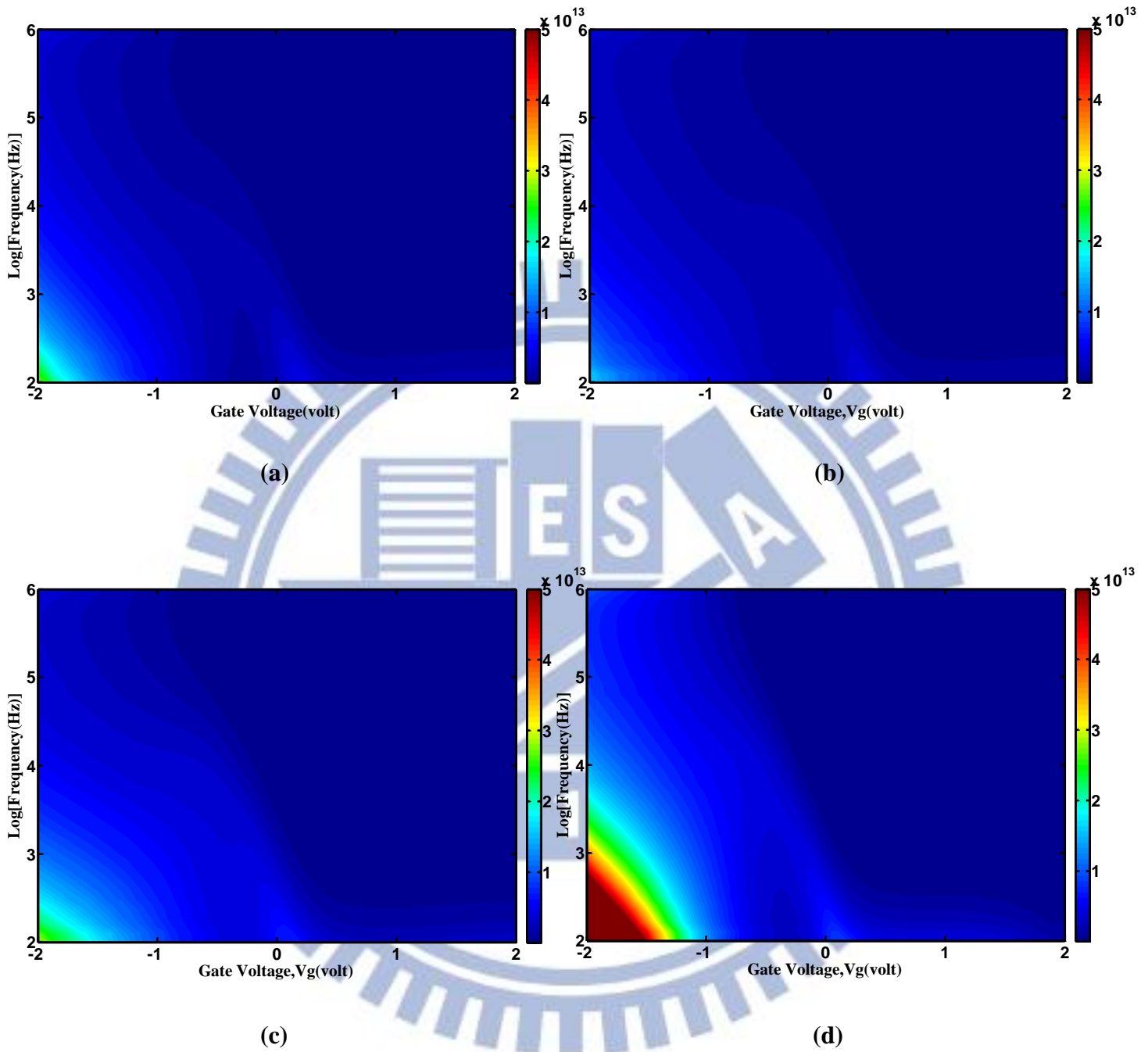


**Fig. 2.24** Map of normalized parallel conductance,  $(G_p/\omega)/Aq$  ( $\text{eV}^{-1}\text{cm}^{-2}$ ) vs.  $V_g$  (volt) for  $p$ -type Pt/Ti/TMA+ $\text{Al}_2\text{O}_3$  1 cycle+ $\text{ZrO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in  $\text{N}_2$  ambience for 120 s (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.

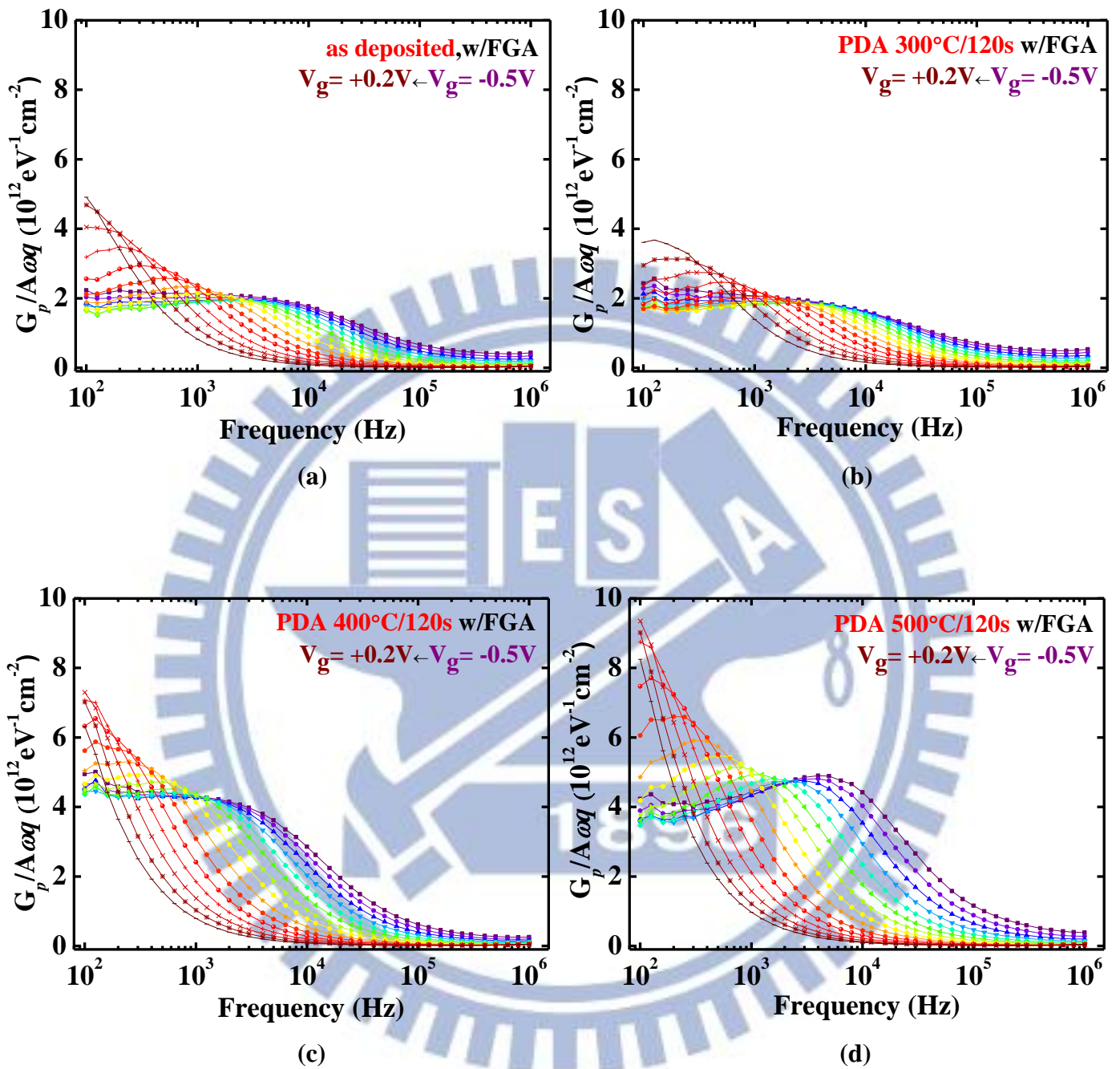


**Fig. 2.25** Parallel conductance curves of for *p*-type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 1 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs after FGA under different PDA conditions from  $V_g = -0.35$  to  $+0.1$  volts (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.

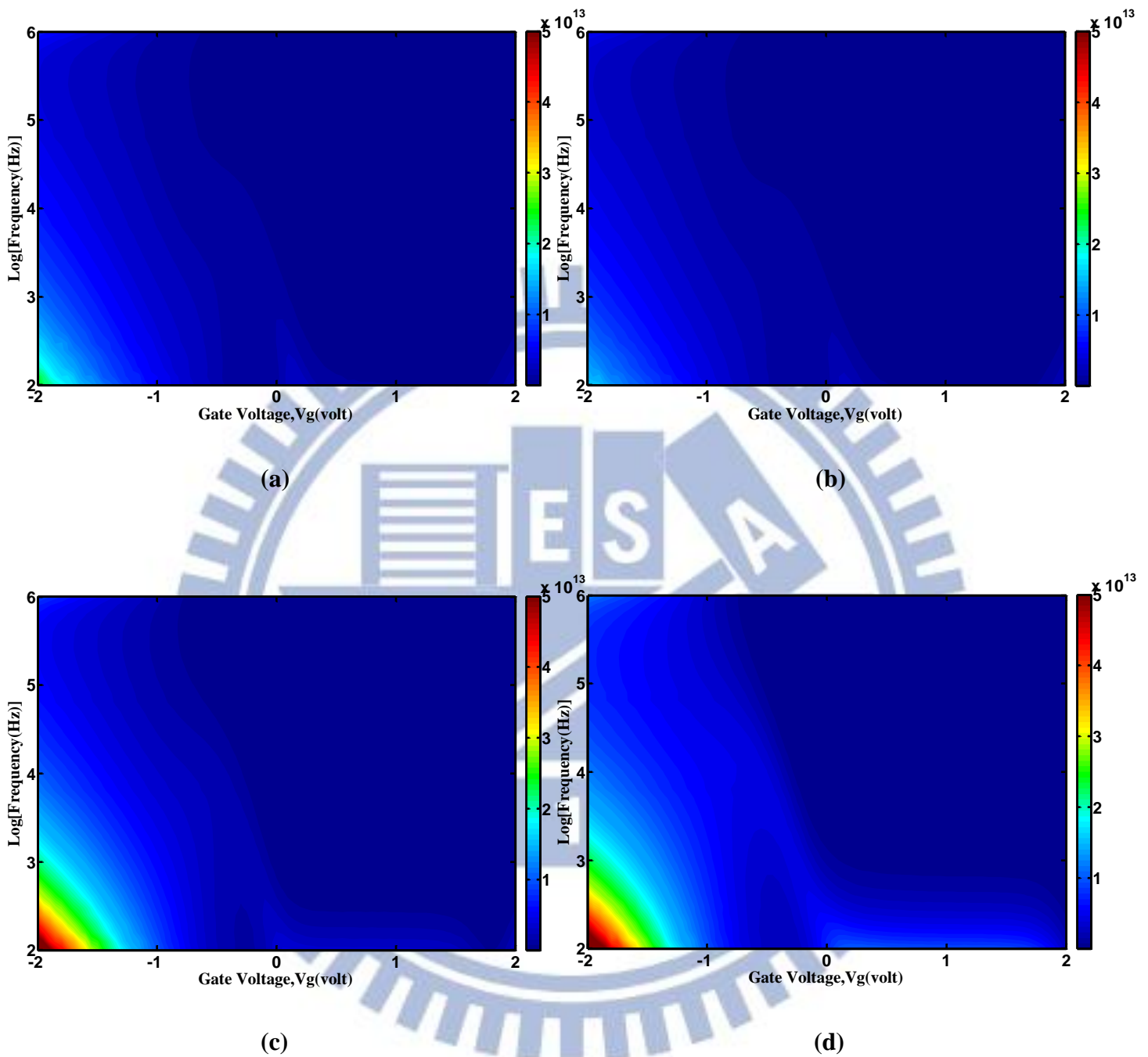




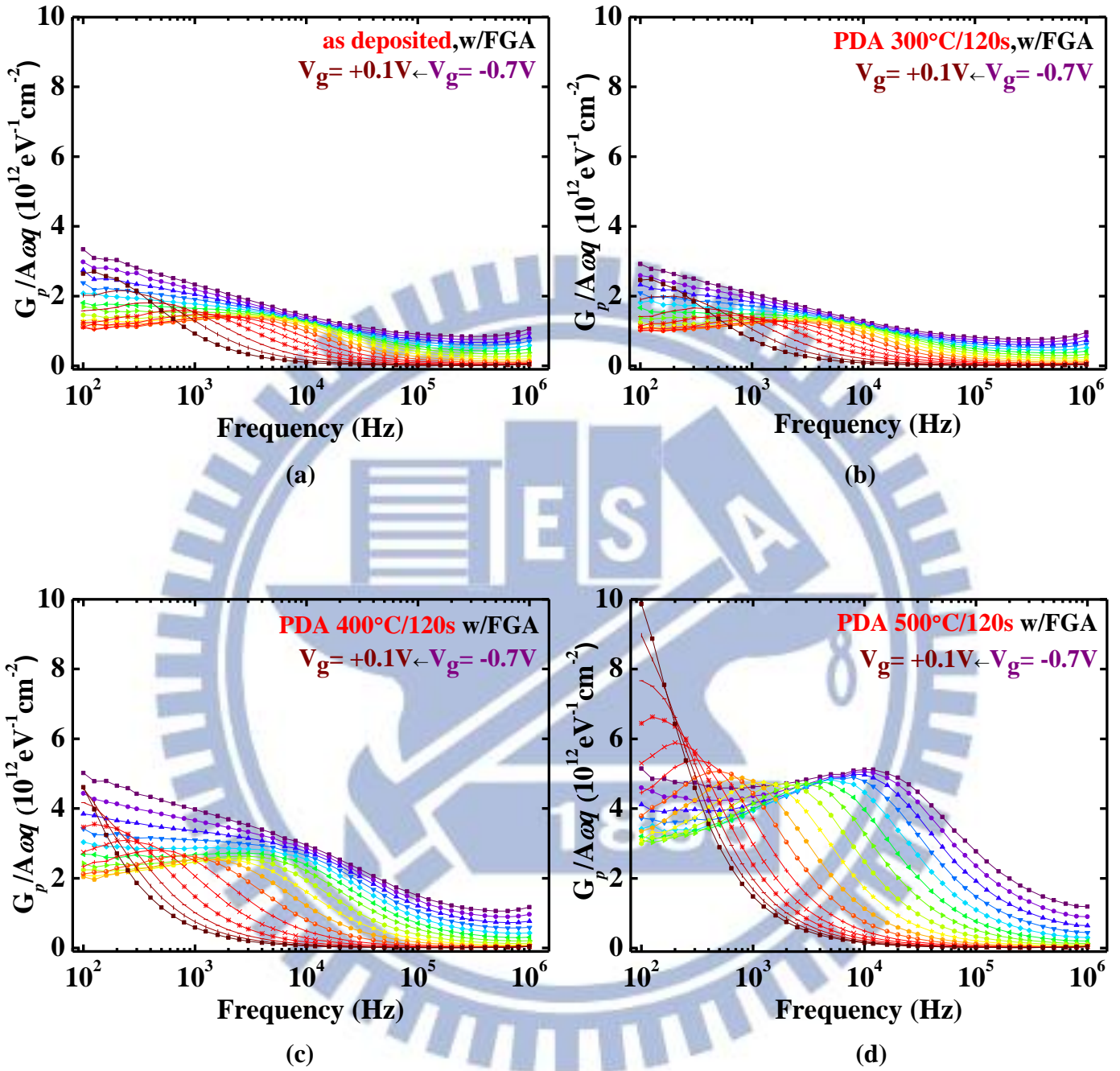
**Fig. 2.26** Map of normalized parallel conductance,  $(G_p/\omega)/Aq$  (eV<sup>-1</sup>cm<sup>-2</sup>) vs.  $V_g$  (volt) for *p*-type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 5 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in N<sub>2</sub> ambience for 120 s (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.



**Fig. 2.27** Parallel conductance curves of for *p*-type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 5 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs after FGA under different PDA conditions from  $V_g = -0.5$  to  $+0.2$  volts (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.

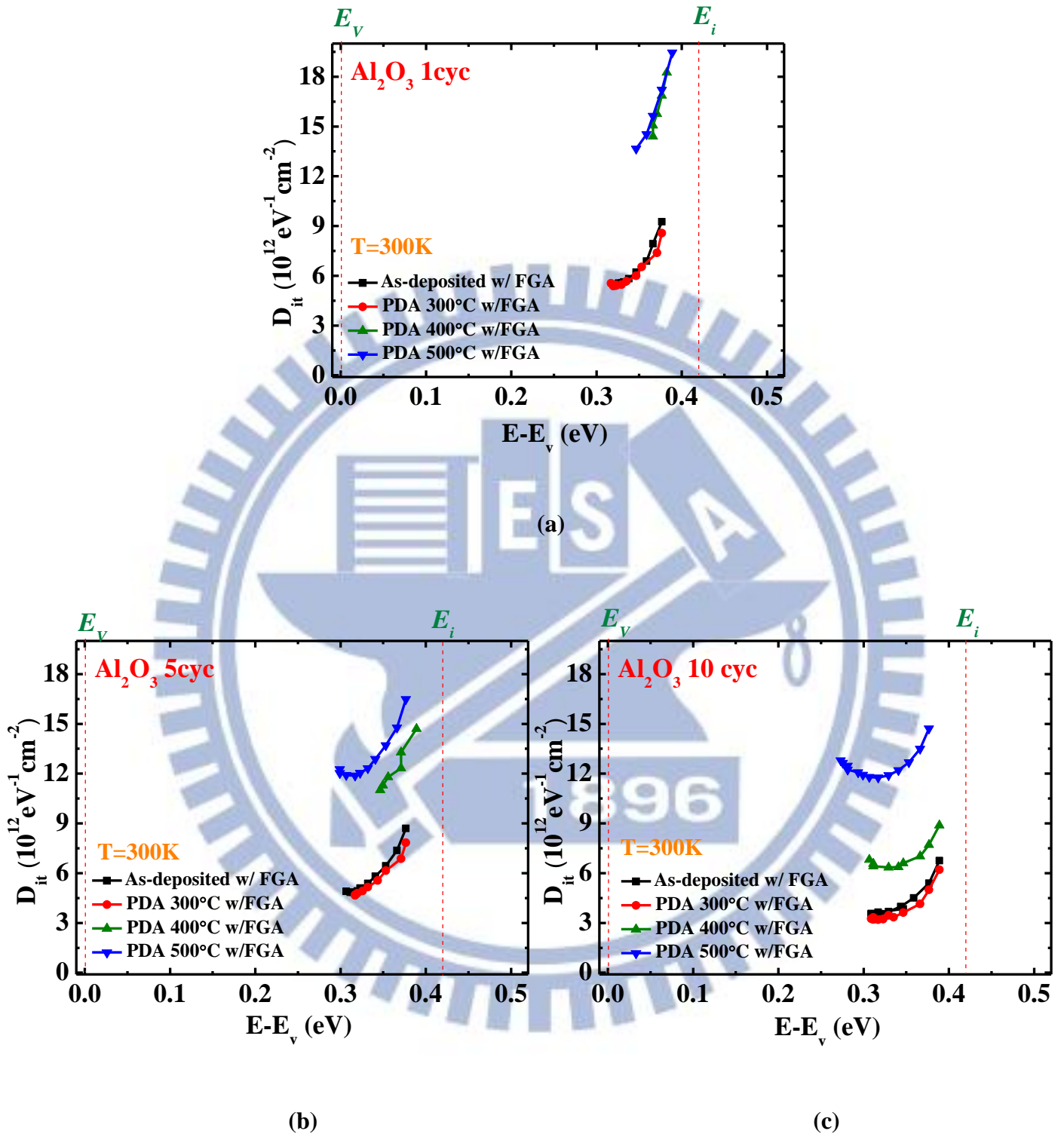


**Fig. 2.28** Map of normalized parallel conductance,  $(G_p/\omega)/Aq$  (eV<sup>-1</sup>cm<sup>-2</sup>) vs.  $V_g$  (volt) for *p*-type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 10 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs measured from 1 MHz to 100 Hz after FGA under different PDA conditions in N<sub>2</sub> ambience for 120 s (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.

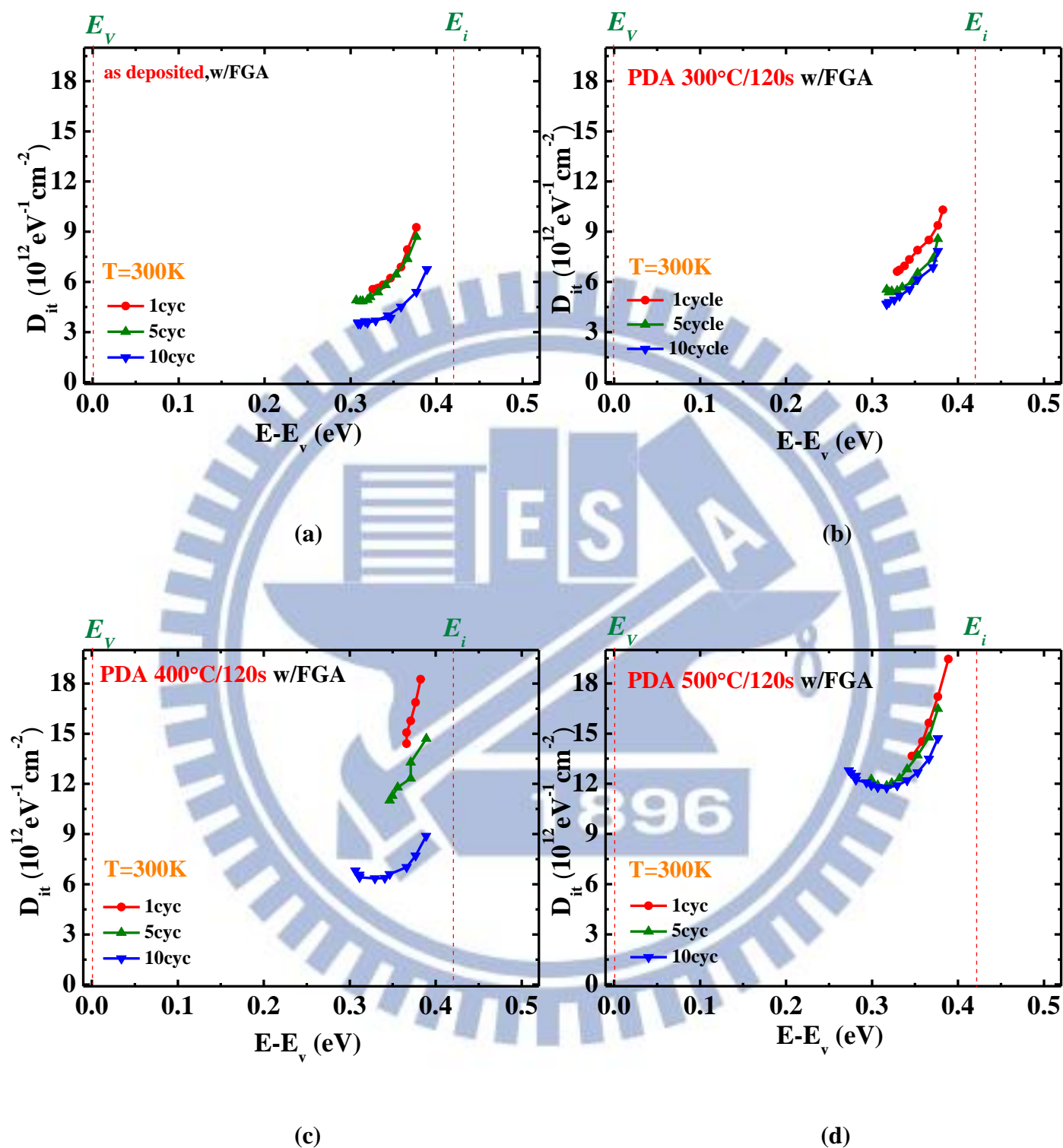


**Fig. 2.29** Parallel conductance curves of for  $p$ -type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 10 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>-Ga<sub>0.47</sub>As MOSCAPs after FGA under different PDA conditions from  $V_g = -0.7$  to +0.1 volts (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.

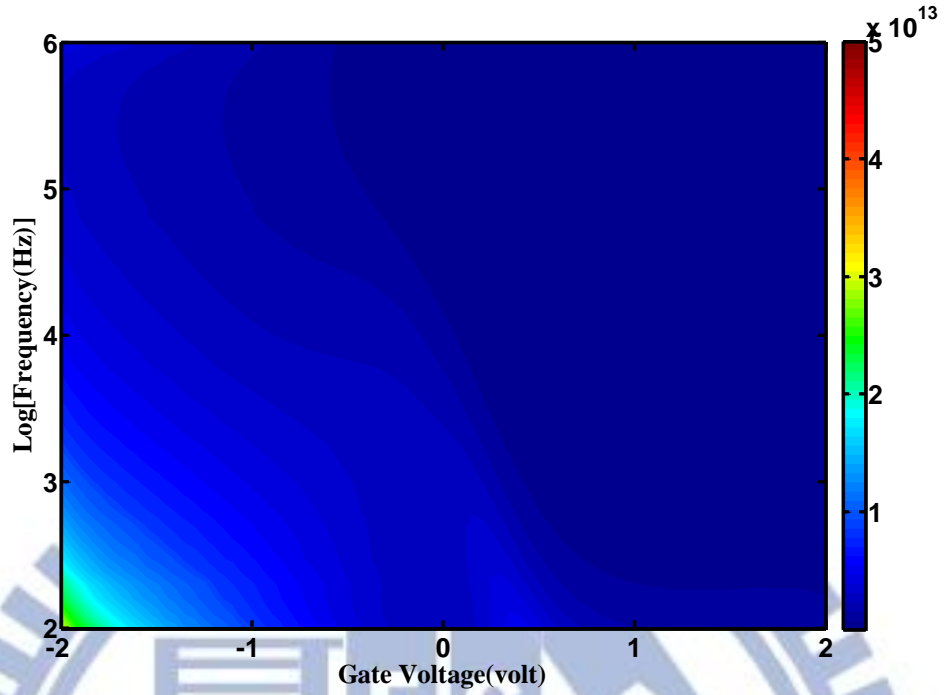




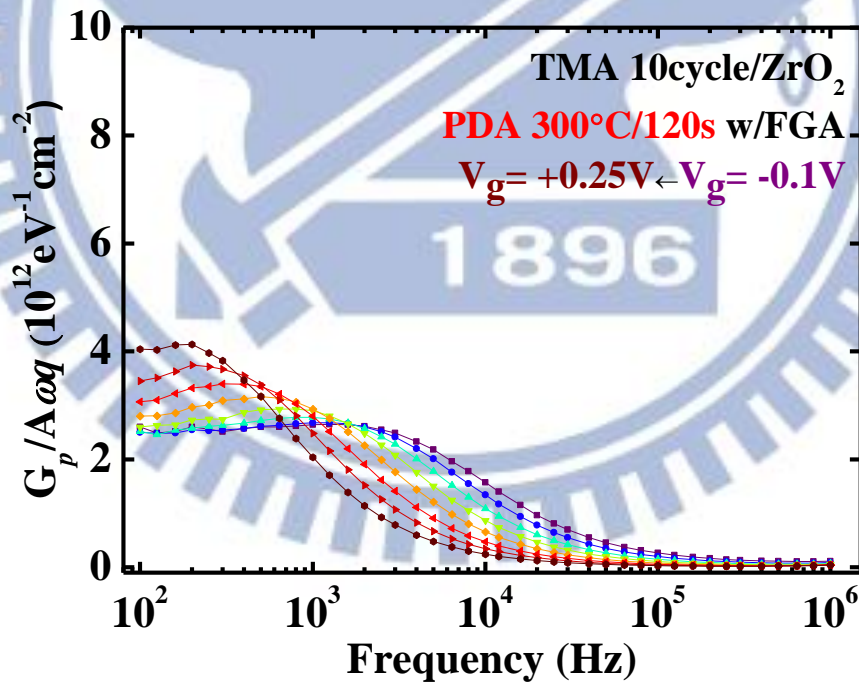
**Fig. 2.30** Comparison of  $D_{it}$  profiles of ALD-TMA/ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs under different PDA conditions with various Al<sub>2</sub>O<sub>3</sub> inter-layer (a) 1cycle (b) 5cycle (c) 10cycle.



**Fig. 2.31** Comparison of  $D_{it}$  profiles of ALD-TMA/ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs with various Al<sub>2</sub>O<sub>3</sub> inter-layers under different PDA conditions (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.

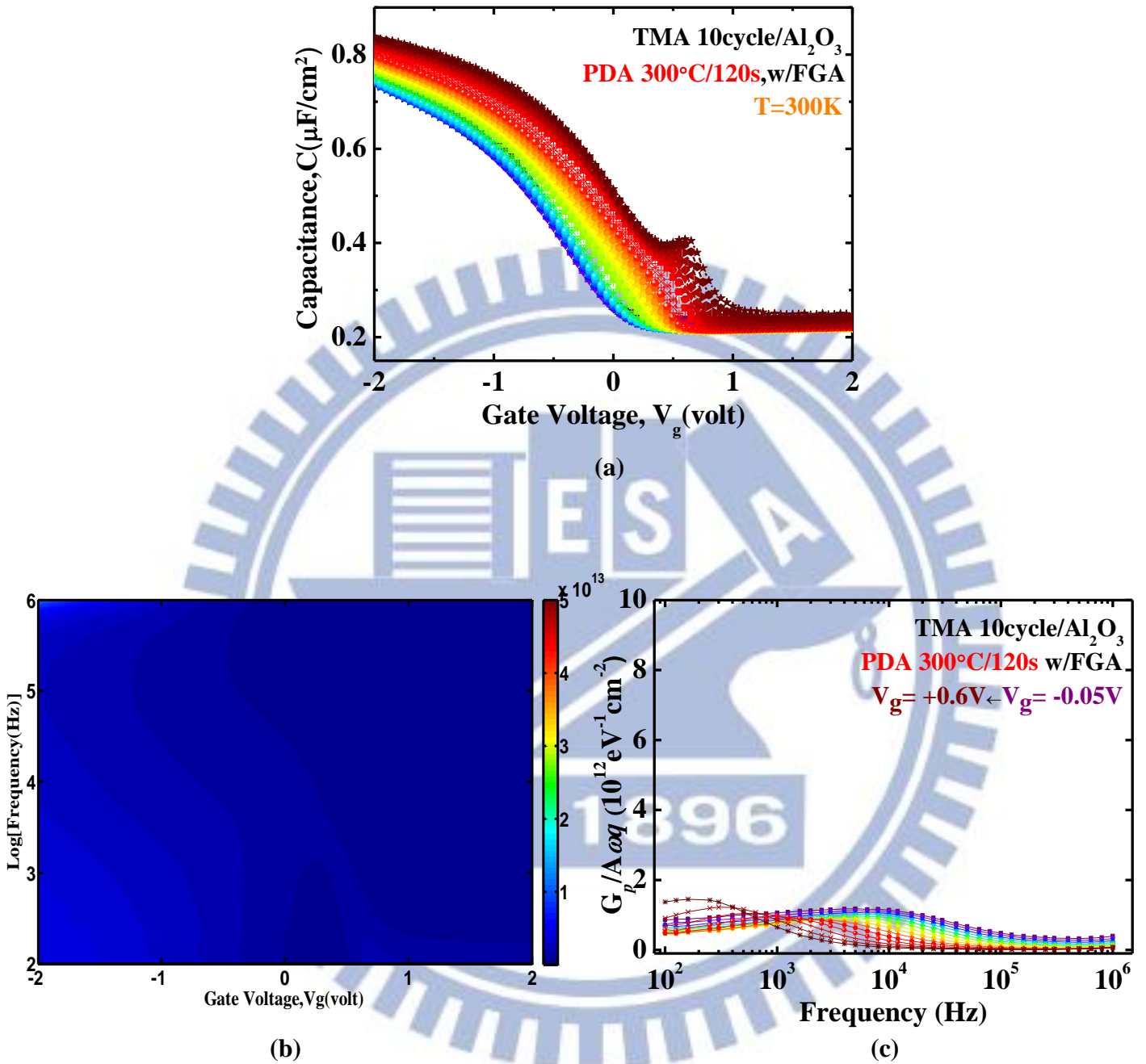


(a)



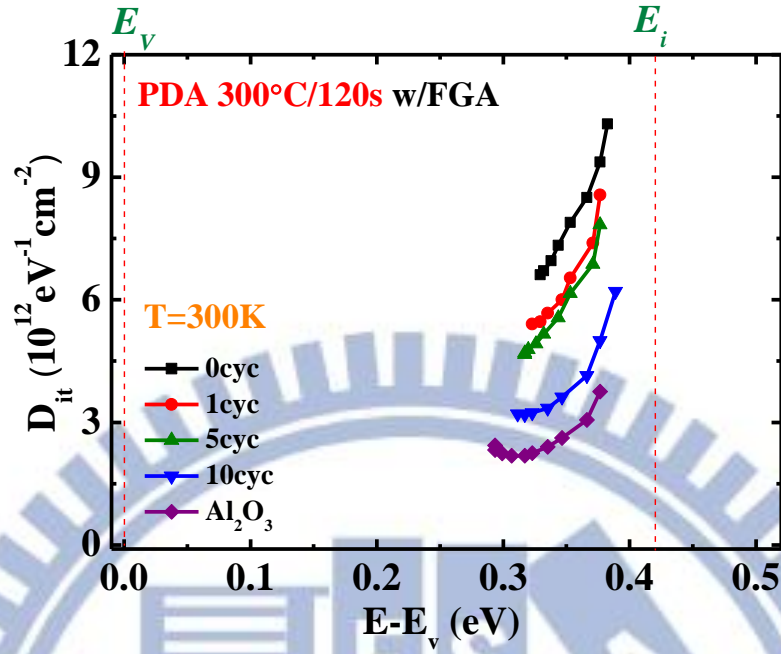
(b)

**Fig. 2.32(a)(b)** The map of normalized parallel conductance,  $(G_p/\omega)/Aq$  ( $\text{eV}^{-1} \text{cm}^{-2}$ ) vs.  $V_g$  (volt) and the curves for  $p$ -type Pt/Ti/TMA+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs from  $V_g = -0.25$  to  $+0.1$  volts under PDA 300 °C/120 s, w/FGA



**Fig. 2.33** (a)(b)(c) The capacitance curve, the map of normalized parallel conductance, and  $(G_p/\omega)/Aq$  ( $\text{eV}^{-1}\text{cm}^{-2}$ ) vs.  $V_g$  (volt) and the  $[(G_p/\omega)/Aq]$  curves for *p*-type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs from  $V_g = -0.05$  to  $+0.6$  volts under PDA 300 °C/120 s, w/FGA

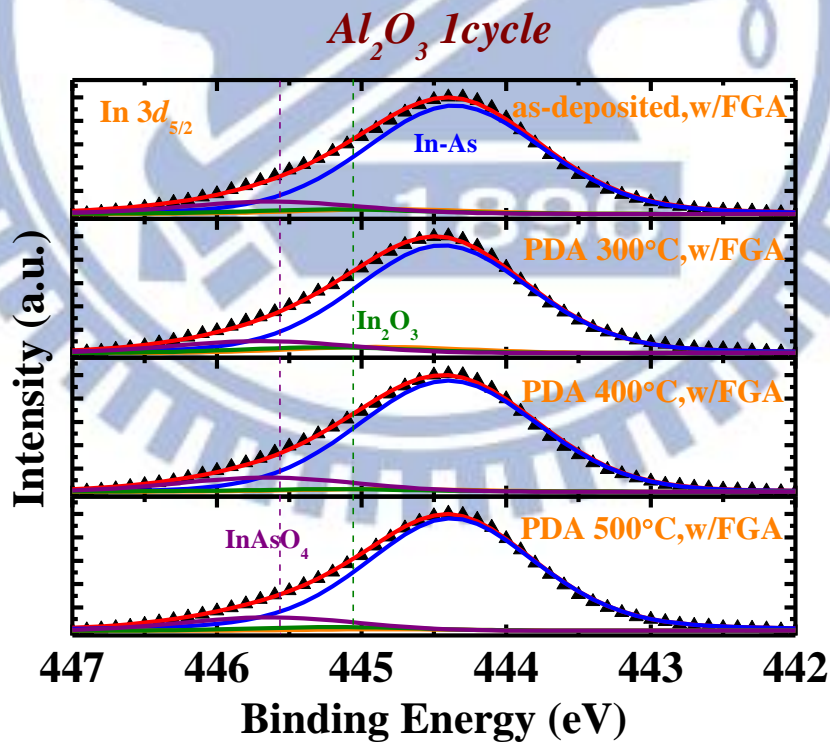
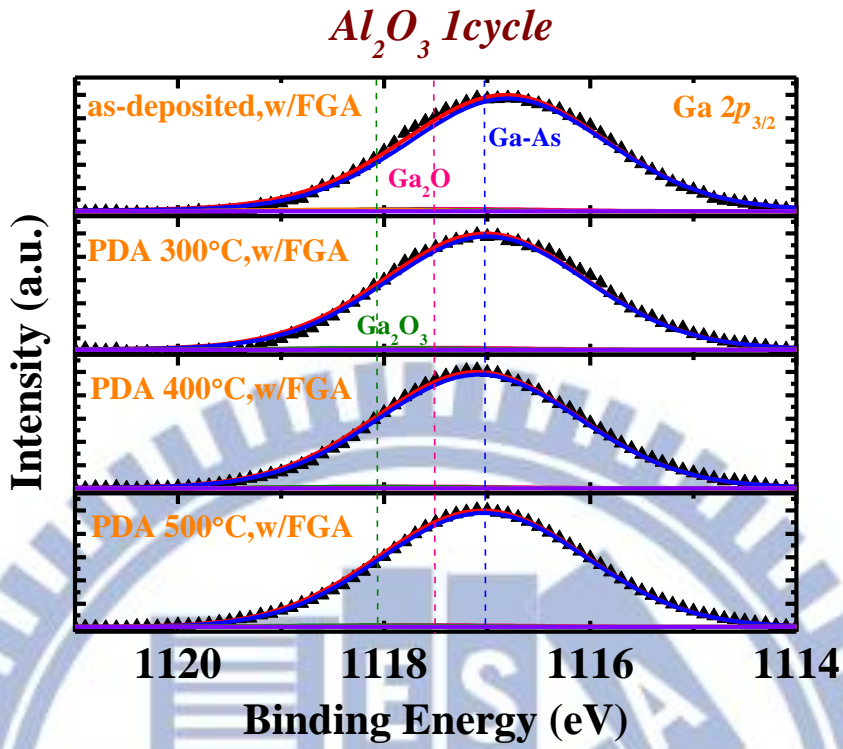


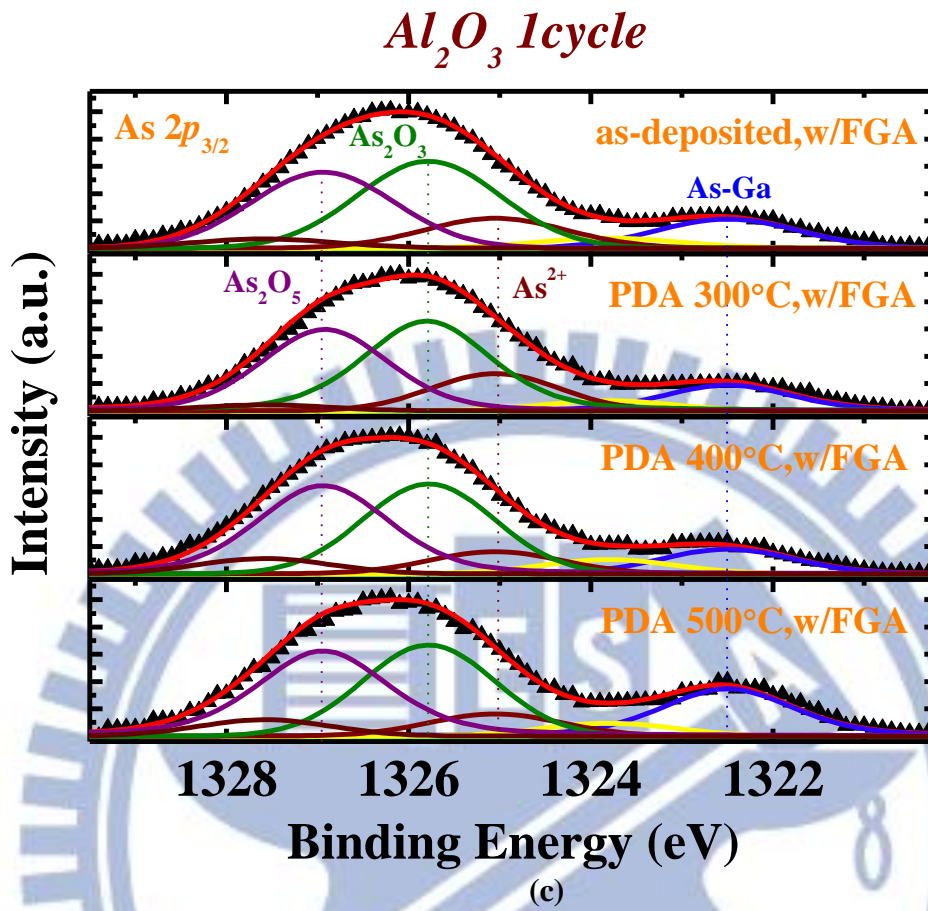


**Fig. 2.34** Comparison of  $D_{it}$  profiles of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  MOSCAPs with various  $\text{Al}_2\text{O}_3$  cycle inter-layer and ALD- $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  MOSCAPs under PDA 300 °C/120 s, w/FGA.

$D_{it} (10^{12} \text{eV}^{-1} \text{cm}^{-2})$	0cyc	1cyc	5cyc	10cyc	$\text{Al}_2\text{O}_3$
As-deposited+FGA		9.26	8.70	5.40	
<b>PDA 300 °C+FGA</b>	<b>9.37</b>	<b>8.57</b>	<b>7.83</b>	<b>4.99</b>	<b>3.75</b>
PDA 400 °C+FGA		16.87	14.0	7.71	
PDA 500 °C+FGA		17.21	16.49	14.71	

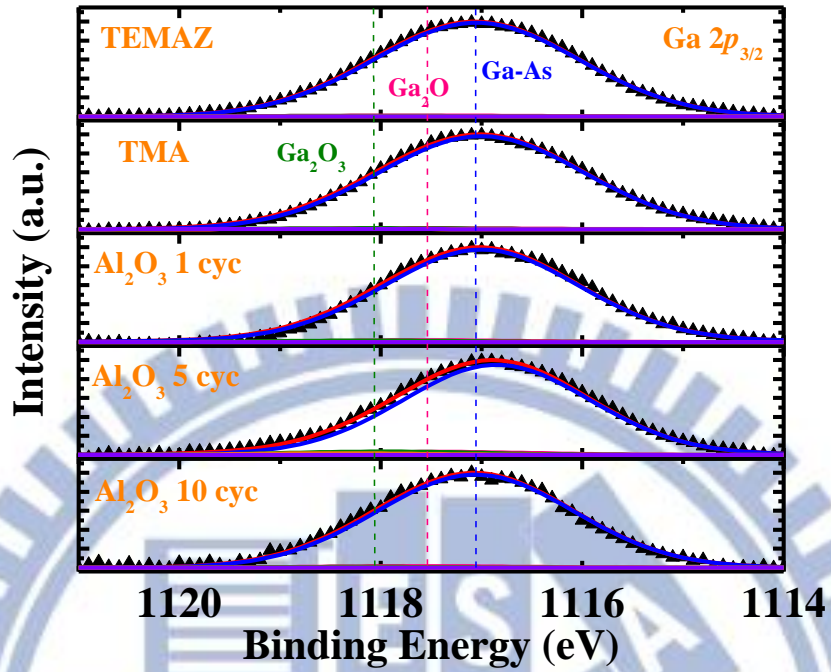
**Table 2.4** Overview of  $D_{it}$  at trap energy  $E_t=0.377\text{eV}$  of ALD-TMA/ $\text{ZrO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  under different thermal conditions and  $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  MOSCAPs at PDA 300 °C/120 s, w/FGA.



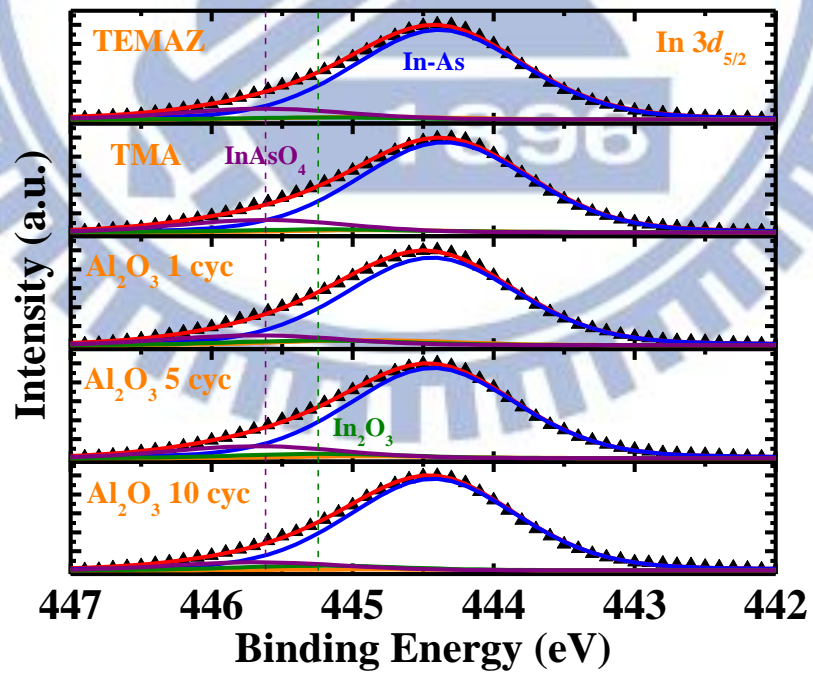


**Fig. 2.35** X-ray photoelectron spectroscopy for *p*-type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 1 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>-Ga<sub>0.47</sub>As MOSCAPs after FGA under various PDA conditions (a) Ga 2*p*<sub>3/2</sub> (b) In 3*d*<sub>5/2</sub> (c) As 2*p*<sub>3/2</sub>.

*PDA 300 °C/120s,w/FGA*

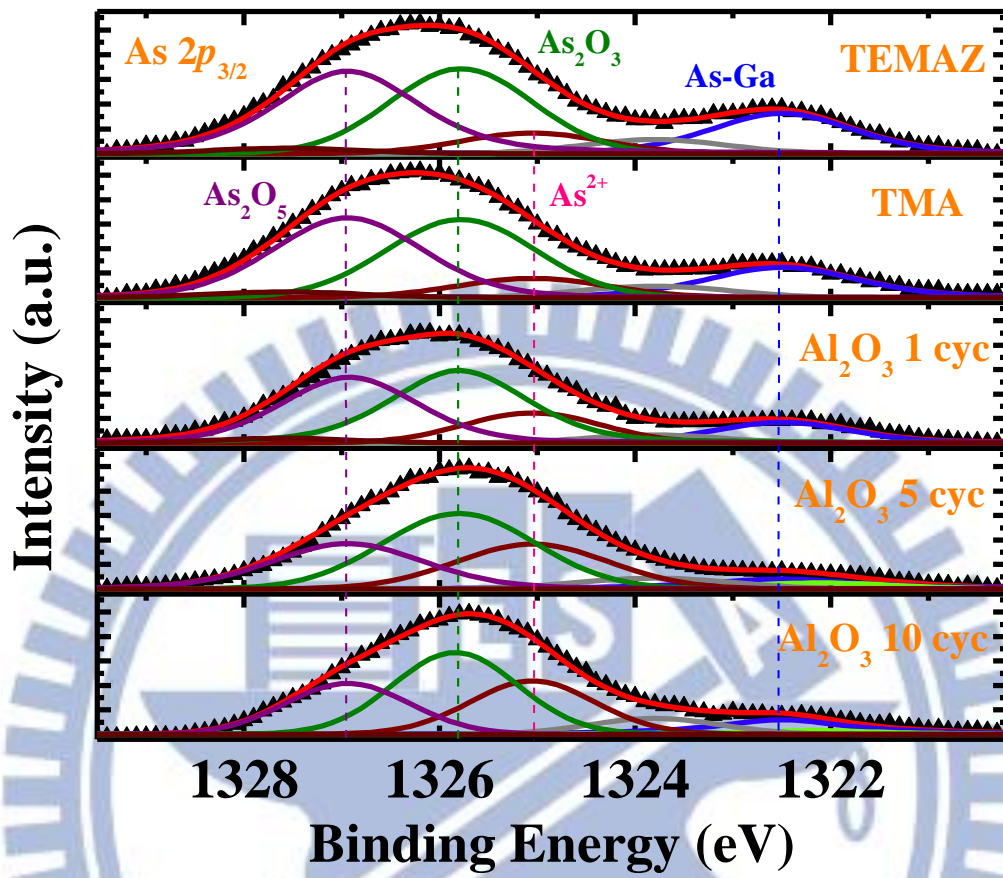


*PDA 300 °C/120s,w/FGA*





*PDA 300 °C/120s,w/FGA*



(c)

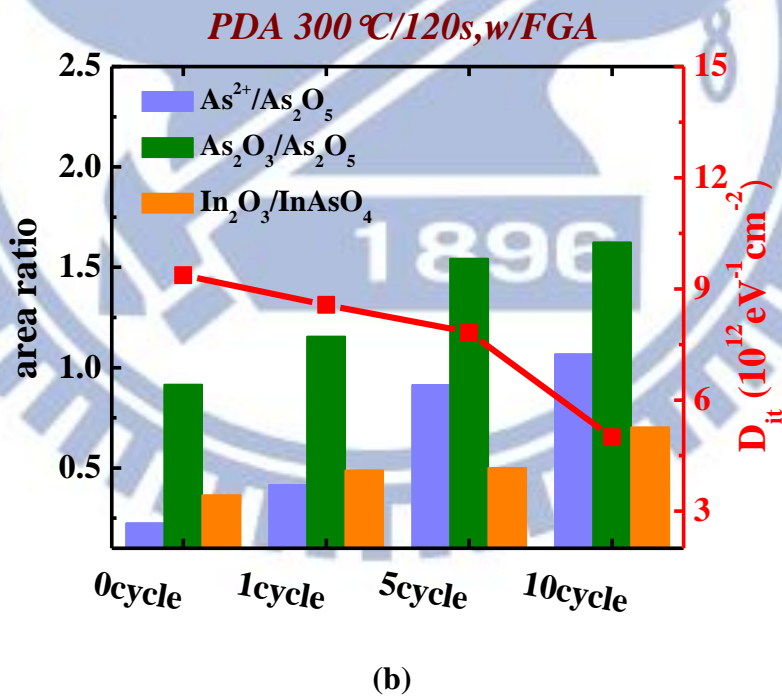
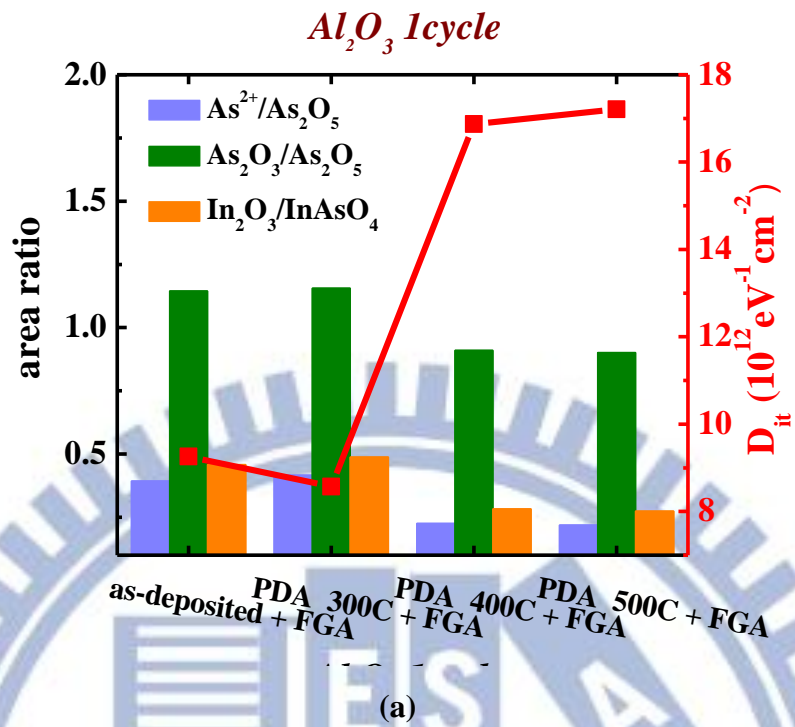
**Fig. 2.36** X-ray photoelectron spectroscopy of various pretreatment and several Al<sub>2</sub>O<sub>3</sub> cycles after FGA under PDA 300 °C /120 s (a) Ga 2p<sub>3/2</sub> (b) In 3d<sub>5/2</sub> (c) As 2p<sub>3/2</sub>

<b>Al<sub>2</sub>O<sub>3</sub> 1cycle</b>	<b>As<sup>2+</sup> /As<sub>2</sub>O<sub>5</sub></b>	<b>As<sub>2</sub>O<sub>3</sub>/As<sub>2</sub>O<sub>5</sub></b>	<b>In<sub>2</sub>O<sub>3</sub>/InAsO<sub>4</sub></b>
<b>As-deposited+FGA</b>	<b>0.393</b>	<b>1.145</b>	<b>0.458</b>
<b>PDA 300 °C /120 s+FGA</b>	<b>0.417</b>	<b>1.156</b>	<b>0.488</b>
<b>PDA 400 °C /120 s+FGA</b>	<b>0.225</b>	<b>0.910</b>	<b>0.283</b>
<b>PDA 500 °C /120 s+FGA</b>	<b>0.219</b>	<b>0.902</b>	<b>0.274</b>

**Table 2.5** Ratio of the fitted area from the As 2p<sub>3/2</sub> and In 3d<sub>5/2</sub> spectra for *p*-type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 1 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs after FGA under various PDA conditions.

<b>PDA 300 °C/120 s w/FGA</b>	<b>As<sup>2+</sup> /As<sub>2</sub>O<sub>5</sub></b>	<b>As<sub>2</sub>O<sub>3</sub>/As<sub>2</sub>O<sub>5</sub></b>	<b>In<sub>2</sub>O<sub>3</sub>/InAsO<sub>4</sub></b>
<b>TEMAZ</b>	<b>0.210</b>	<b>0.867</b>	<b>0.228</b>
<b>TMA</b>	<b>0.225</b>	<b>0.916</b>	<b>0.364</b>
<b>Al<sub>2</sub>O<sub>3</sub> 1cyc.</b>	<b>0.417</b>	<b>1.156</b>	<b>0.488</b>
<b>Al<sub>2</sub>O<sub>3</sub> 5cyc.</b>	<b>0.915</b>	<b>1.543</b>	<b>0.501</b>
<b>Al<sub>2</sub>O<sub>3</sub> 10cyc.</b>	<b>1.068</b>	<b>1.624</b>	<b>0.703</b>

**Table 2.6** Ratio of the fitted area from the As 2p<sub>3/2</sub> and In 3d<sub>5/2</sub> spectra at various pretreatment and several Al<sub>2</sub>O<sub>3</sub> cycles after FGA under PDA 300 °C/120 s.



**Fig. 2.37** Comparison of  $D_{it}$  and ratio of the fitted area from the As  $2p_{3/2}$  and In  $3d_{5/2}$  spectra profiles of ALD-TMA/ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs (a) with Al<sub>2</sub>O<sub>3</sub> 1 cycle inter-layer (b) with PDA 300 °C /120 s, w/FGA.

# Chapter 3

## *The Extraction of Border Traps for $ZrO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs by a Distributed Bulk-Oxide Traps Model*

### 3.1 Introduction

The concept of border traps has been introduced by Dan Fleetwood in 1992 [1] to define traps in the gate dielectrics of high- $k$ /III-V MOS devices, which result in frequency dispersion at the accumulation region. The traps have been attributed to trapped-holes [2] or to oxygen deficiency defects [3]. As a rule, the density of border traps increases when the quality of the oxide decreases, due to poor stoichiometry or the presence of strained bonds at the interface [4]. However, the conventional interface states whose time constant in such bias regions is far shorter than the period of typical measurement frequencies can't be used to explain this dispersion phenomenon. On the other hand, the trap states reside the high- $\kappa$  dielectric, which are called border traps or slow oxide traps, have long time constants when they exchange charge with the channel [5]. Furthermore, the frequency dispersion of conductance doesn't follow the renowned peak deoprtment when the conventional conductance method [6] for the interface states is applied to the high to low transition (the maximum slope) of the  $C-V$  data. In addition, comparing the experimental  $C-V$  curve with the ideal case demonstrates that the density of interface state far surpass which is extracted from the dispersion in that region. Such variance can be resolved by a border trap model in which the low frequency portion give rise to the stretch-out  $C-V$  curve is stronger than the high-frequency portion for the dispersion.

In this chapter, the distributed border traps model is completed by adding integration of



the trap density with respect to energy for calculating the equivalent admittance. A differential equation is derived and numerically solved to produce frequency-dependent capacitance and conductance of the MOS devices. The model is validated and calibrated by the experimental data of p-type ALD- ZrO<sub>2</sub>/ Al<sub>2</sub>O<sub>3</sub> /In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs in accumulation region.

### 3.2 A Distributed Model for determining Border Traps

In general, the bulk oxide traps can interchange charge with mobile carriers in the semiconductor bands by tunneling mechanism in devices. Hence, **Fig. 3.1** schematically exhibits the mechanism between bulk-oxide traps and valence band of the p-type MOS devices in the accumulation gate bias. The time constant connected with charge exchange between bulk-oxide traps and semiconductor is regulated by tunneling mechanism that has exponential dependence on the trap distance  $x$  from the interface of oxide/semiconductor [5, 7-10] as follows:

$$\tau(x) = (1 - f_0)\tau_0 e^{2\kappa x} \quad (3.1)$$

Here,  $\tau_0$  is the time constant of the interface trap which equals  $1/(n_s \sigma v_{th})$  with  $\sigma$  being the trap cross-sectional area, and  $v_{th}$  is the thermal velocity of hole. Other parameters in **Eq.(3.1)** are as follows:  $f_0$  is the Fermi-Dirac function which a trap occupied by an electron at energy  $E$ , and  $\kappa$  is the attenuation coefficient for an energy  $E$  wavefunction of an hole decaying due to an energy barrier  $E_{v,ox} > E$ .

$$\kappa = \sqrt{2m^*(E_{v,ox} - E)/\hbar} \quad (3.2)$$

$m^*$  is the hole effective mass of the gate dielectric, and  $E_{v,ox}$  is the bottom energy of the gate insulator band (tunneling barrier), as shown in **Fig. 3.1**.

The bulk-oxide traps at a specific depth  $x$  and energy  $E$  change occupancy with respond to a small-signal ac modulation for a given dc bias. The border traps at energy about  $E \sim E_f$

are most responsible for the small-signal capacitance. In the other words, we assume the border traps located within certain distance from the interface maintain a Fermi level the same as the semiconductor. Then, we can find that the influences of the bulk-oxide traps at certain depth  $x$  and energy  $E$  can be modeled by a series of connecting capacitance and conductance on the small-signal MOS admittance. The bulk-oxide traps in an incremental depth  $\Delta x$  at  $x$  and incremental energy  $\Delta E$  at  $E$  are symbolized by the incremental capacitance  $\Delta C_{bt}(E, x)$  and the incremental conductance  $\Delta G_{bt}(E, x)$  which are connected in series. If the density per volume per energy of bulk-oxide traps is  $N_{bt}$  in units of  $\text{eV}^{-1}\text{cm}^{-3}$ , then [5-6] the equation of  $\Delta C_{bt}$  will indicate:

$$\Delta C_{bt}(E, x) = \frac{f_0(1-f_0)q^2 N_{bt}}{kT} \Delta E \Delta x \quad (3.3)$$

And the  $\Delta C_{bt}(E, x)$  and  $\Delta G_{bt}(E, x)$  have the relationship in time constant  $\tau(x)$

$$\frac{\Delta C_{bt}(E, x)}{\Delta G_{bt}(E, x)} = \tau(x) = (1 - f_0)\tau_0 e^{2\kappa x} \quad (3.4)$$

In order to integrate with the continuous energy distribution of bulk-oxide traps, the  $\Delta C_{bt}(E, x)$  and  $\Delta G_{bt}(E, x)$  in serial combination have to be transfer to a parallel connection of the incremental admittance  $\Delta Y_{bt}(E, x)$ . Due to the factor  $f_0(1-f_0)$  has pointy peak at  $E = E_f$ , the attenuation coefficient  $k$  in **Eq.(3.2)** is determined as a constant with  $E = E_f$  in the integration. Therefore, the total incremental admittance at certain depth  $x$  and energy  $E$  is indicated for

$$\Delta Y_{bt}(x) = \int_E \frac{1}{\frac{1}{j\omega\Delta C_{bt}(E, x)} + \frac{1}{\Delta G_{bt}(E, x)}} = \frac{q^2 N_{bt} \ln(1 + j\omega\tau_0 e^{2\kappa x})}{\tau_0 e^{2\kappa x}} \Delta x \quad (3.5)$$

Because of a continuous energy distribution of the border trap all over the gate oxide thickness, an equivalent circuit of the distributed model in the MOS device is illustrated in **Fig. 3.2**, where the oxide capacitance is separated into an infinite number of serial slices with branches of  $\Delta Y_{bt}(x)$ , which is linked in different depth. Here,  $\epsilon_{ox}$  is the permittivity of the gate dielectric and  $C_s$  is the semiconductor capacitance.

Consequently, if we define  $Y(x)$  to be the equivalent admittance at the point  $x$  looking into the semiconductor in **Fig. 3.2**, the recursive nature of the circuit will give the admittance

of the next point  $x + \Delta x$  as

$$Y(x + \Delta x) = \Delta Y_{bt}(x) + \frac{1}{\frac{\Delta x}{j\omega\epsilon_{ox}} + \frac{1}{Y(x)}} \quad (3.6)$$

Then, substituting **Eq.(3.5)** for  $\Delta Y_{bt}(x)$ , the first order terms in  $\Delta x$  will yield a differential equation for  $Y(x)$

$$\frac{dY}{dx} = -\frac{Y^2}{j\omega\epsilon_{ox}} + \frac{q^2 N_{bt} \ln(1 + j\omega\tau_0 e^{2\kappa x})}{\tau_0 e^{2\kappa x}} \quad (3.7)$$

There are two equations as boundary conditions as follows:

$$Y(x = 0) = j\omega C_s + j\omega C_{it} + G_{it} \quad (3.8)$$

where  $C_s$  is the semiconductor capacitance and  $C_{it}$  and  $G_{it}$  are contributions from interface traps and given in [6] as

$$C_{it} = q^2 D_{it} \arctan(\omega\tau_{it}) / (\omega\tau_{it}) \quad (3.9)$$

$$G_{it} = q^2 D_{it} \ln[1 + (\omega\tau_{it})^2] / 2\tau_{it} \quad (3.10)$$

where  $D_{it}$  ( $\text{eV}^{-1} \cdot \text{cm}^{-2}$ ) is the interface trap density.

Moreover, **Eq.(3.7)** need to be numerically solved to obtain the total admittance looked into semiconductor by gate

$$Y(x = t_{ox}) \equiv G_{tot} + j\omega C_{tot} \quad (3.11)$$

For the typical measured frequency limit of 1 kHz - 1 MHz,  $1.4 \cdot 10^{-6} < \omega\tau_0 < 1.4 \cdot 10^{-3}$ , the bulk-oxide traps can't respond to the ac signal and  $C_{tot}$  is equal to  $C_{ox}$  in series with  $C_s$ , so the  $C_{tot}$  varies with  $\ln(1/\omega)$  linearly, and  $G_{tot}$  varies with  $\omega$ , that is to say,  $G_{tot} / \omega \sim \text{constant}$ . For a given bias, the constant  $G_{tot} / \omega$  shows that the response of the border traps causes wide frequency dispersion because of their various depth distribution, in other words, an obvious distinction from conventional interface traps [6]. Then, for a given frequency of  $\omega < 1/\tau_0$ , the depth of the slow traps that respond to the small-signal can be estimated by making the factor  $\omega\tau_0 e^{2\kappa x}$  in **Eq.(3.7)** equal unity, as the exhibition  $x \sim (2\kappa)^{-1} \ln(1/\omega\tau_0)$ , which is in the range of 0.1~1nm.

When  $\omega = 0$  or in dc condition, the circuit of **Fig. 3.2** becomes a purely capacitive



circuit model, and **Eq.(3.7)** is simplified to a real equation for  $C(x)$  as follows:

$$\frac{dC}{dx} = -\frac{C^2}{\epsilon_{ox}} + q^2 N_{bt} \quad (3.12)$$

The capacitance boundary condition at  $x=0$  is  $C_s$ . For the uniform distribution of  $N_{bt}$ , **Eq.(3.12)** can be analytically resolved to produce

$$C(x) = C_0 \frac{(C_s + C_0) \exp\left(2qx \sqrt{\frac{N_{bt}}{\epsilon_{ox}}}\right) + (C_s - C_0)}{(C_s + C_0) \exp\left(2qx \sqrt{\frac{N_{bt}}{\epsilon_{ox}}}\right) - (C_s - C_0)} \quad (3.13)$$

Here,  $C_0 = q\sqrt{\epsilon_{ox}N_{bt}}$ . If  $2qx\sqrt{\epsilon_{ox}N_{bt}} \gg 1$ , then  $C(x = t_{ox}) \approx \sqrt{q^2\epsilon_{ox}N_{bt}}$ , which is insensitive to  $C_s$ . Certainly, this is only a matter of theoretical interest, nevertheless, it would take much longer than the age of the universe to charge up all the border traps in the gate dielectric.

Besides, the  $C_s$  in accumulation region of the case is very high. From **Eq.(3.13)**,  $C_{tot}(dc) \approx C_0 \coth(C_0/C_{ox})$ , is larger than  $C_{ox}$ . This result is in contrast to the interface states or lumped-circuit bulk-oxide traps model, which don't yield dispersion when shorted out by large  $C_s$ . Consequently, frequency dispersion in accumulation region is a good indicator of distributed bulk-oxide traps. Moreover, the model should be applicable to any oxide/semiconductor interface with border traps since the derivation isn't depend on material. However, some parameters, such as  $v_{th}$  and  $\kappa$ , are material dependent and need to be calculated compatibly [11].

Furthermore, the time constant  $\tau_0$  is gate-voltage dependent which is assumed to submit standard SRH theory for advanced devices, one should account for inversion layer quantization and its impact on the carrier recombination at the interface. A final factor which must be carefully investigated is that most of the oxide traps show inelastic tunneling transitions, while by default, elastic tunneling is assumed in many cases [4].



### 3.3 The Relationship between the Model and the measured Multi-frequency $C-V$ and $G-V$ Electrical property in Accumulation region

To further discuss the effect of bulk-oxide traps in gate dielectrics at accumulation region and extract  $N_{bt}$  quantitatively, we have fitted the experimental capacitance and conductance data for the ALD-TMA/ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs under different PDA conditions with several Al<sub>2</sub>O<sub>3</sub> layers at the gate voltage range from -2 to -1 volts which are correlated with the distributed model. There are several parameters of the model, such as  $N_{bt}$ ,  $\tau_0$ ,  $C_s$ ,  $\epsilon_{ox}$ , and  $k$ , need to be given an initial supposed values and be matched between the measured data and the oxide traps model from 1 kHz to 100 kHz. Part of the parameters like gate oxide thickness  $t_{ox}$  is determined by TEM image, the semiconductor capacitance  $C_s$  is selected which gives  $C_{tot}$  slightly below the capacitance value of 1 MHz at  $V_g = -2$  V. Moreover, due to two kinds of gate dielectric layers in our sample, we have to assign different parameters, such as  $\epsilon_{ox}$ ,  $k$ , and  $t_{ox}$  for Al<sub>2</sub>O<sub>3</sub> and ZrO<sub>2</sub>, respectively. Pay more attention to the attenuation coefficient  $k$ , we find that Al<sub>2</sub>O<sub>3</sub> should be larger than ZrO<sub>2</sub> because of the difference between the valence band of gate oxide and the energy  $E$ . And  $\tau_0$  is given to probably achieve the frequency condition  $\omega\tau_0 \sim 1$ , which means the influence of bulk-traps has not existed on the capacitance and conductance characteristics. Finally, we can discover that the consequences of the model and the measured data are matched because of being sensitive to the initial supposed values.

**Fig 3.3, 3.5, 3.7, and 3.9** show the transferred  $C-V$  map of total experimental  $C-F$  data for the ALD-TMA/ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs under different PDA conditions with various Al<sub>2</sub>O<sub>3</sub> inter-layers at frequency from 1 kHz to 100 kHz, and **Fig 3.4, 3.6, 3.8, and 3.10** display

the converted  $G$ - $V$  map of total experimental  $G$ - $F$  data. With these figures of  $C$ - $V$  and  $G$ - $V$  maps, the values of  $N_{bt}$  are extracted as shown in **Table. 3.1** at  $C_s=0.75$  ( $\mu\text{F}/\text{cm}^2$ ), which indicate the surface band bending of semiconductor are in the same conditions. And this substrate capacitance corresponding to the energy  $E$  of band gap is above valence band about 0.15 eV.

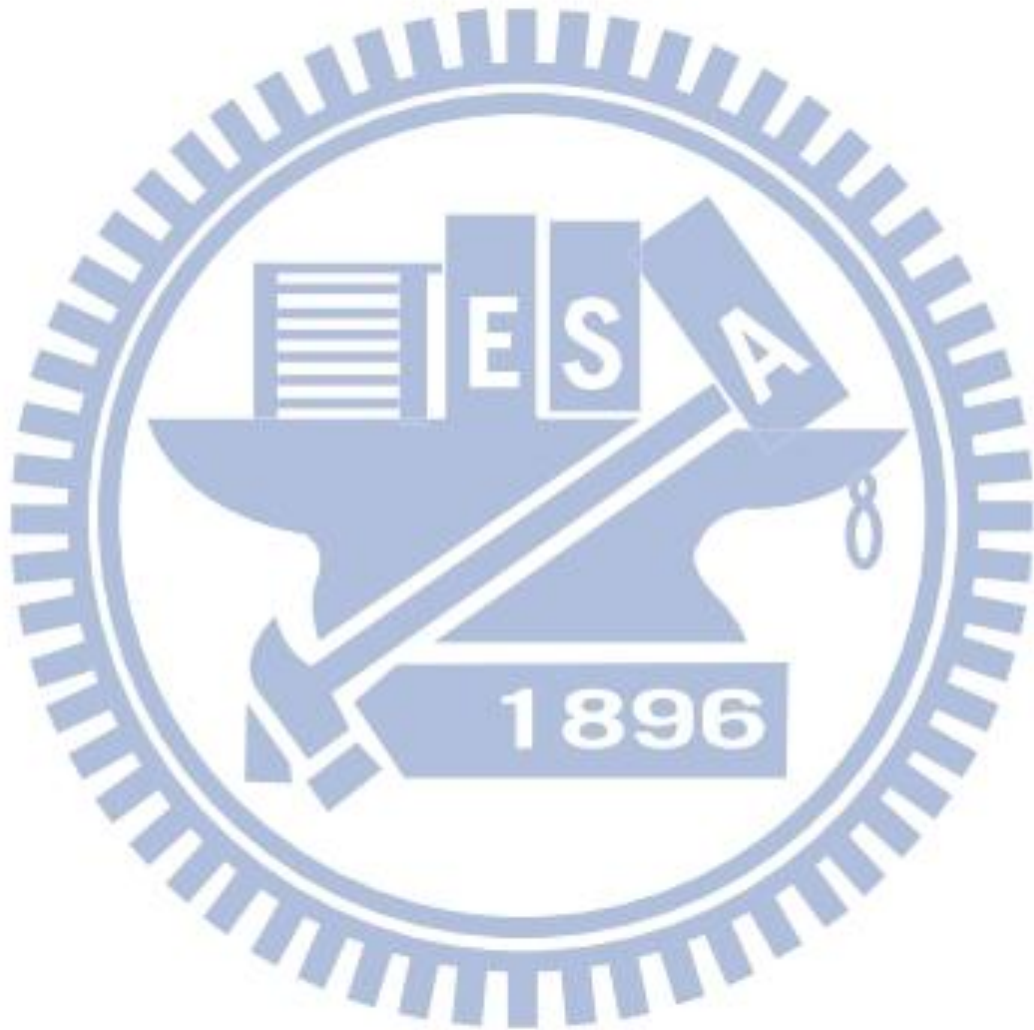
From **Fig 3.11** and **3.12**, both the slopes of  $C$ - $F$  and  $G$ - $F$  of different PDA conditions are sensitive to bulk-oxide trap density  $N_{bt}$  which demonstrate the frequency dispersion at accumulation region, and in contrast with **Table. 3.1**, the temperature of 300 °C has lower  $N_{bt}$  in each  $\text{Al}_2\text{O}_3$  inter-layer conditions except for  $\text{Al}_2\text{O}_3$  with 1cycle. This might be a slightly error of the extraction. Besides, we compare these results of  $N_{bt}$  with the frequency dispersion  $\Delta C$  in **Table. 2.2**, and have good consistency with the consequence. In addition, the  $\Delta C$  and  $N_{bt}$  of 400 °C and 500 °C have some mismatch; these might be the capacitance values at accumulation region of PDA 500 °C is much higher than 400 °C and result the  $\Delta C$  at PDA 500 °C in lower values.

Furthermore, from each post-deposition annealing conditions, we demonstrate that the bulk-oxide trap density  $N_{bt}$  of thicker  $\text{Al}_2\text{O}_3$  layers have lower values and low frequency dispersion, as shown in **Fig 3.13**, **3.14**, and **Table 3.1**. This might be the quality of gate dielectric  $\text{ZrO}_2$  is not good enough, and the  $\text{Al}_2\text{O}_3$  inter-layer can be used to improve the oxide and interface characteristics.

### 3.4 Summary

The distributed bulk-oxide traps model has been developed for the tunneling mechanism which indicate charging and discharging of the border traps between the  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  surface and trap states. Besides, due to the broad frequency spectrum of traps response, the model

differs from the usual interface state circuit. However, the model is demonstrated with the measured data in  $C-V$  and  $G-V$  curves. And the extraction of density  $N_{bt}$  of bulk-oxide traps has similar property which compared to the aforementioned chapter. By this distributed model, we could further demonstrate the consistency with the border traps from the quantitative analyses.



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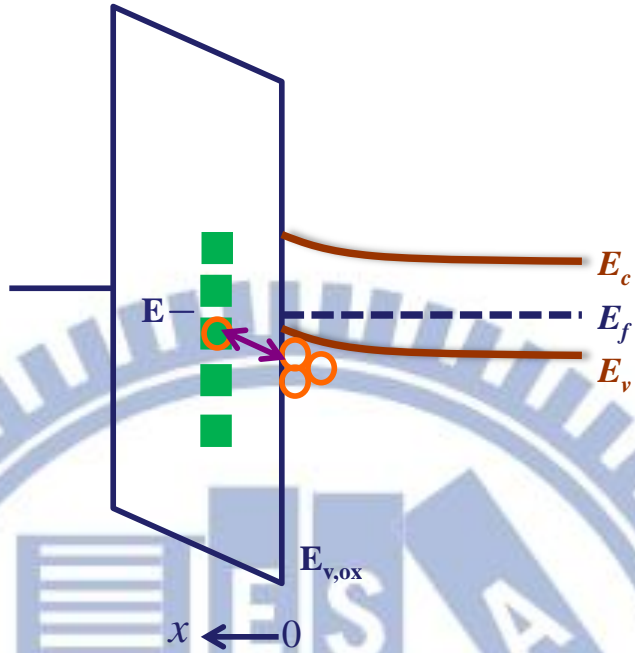


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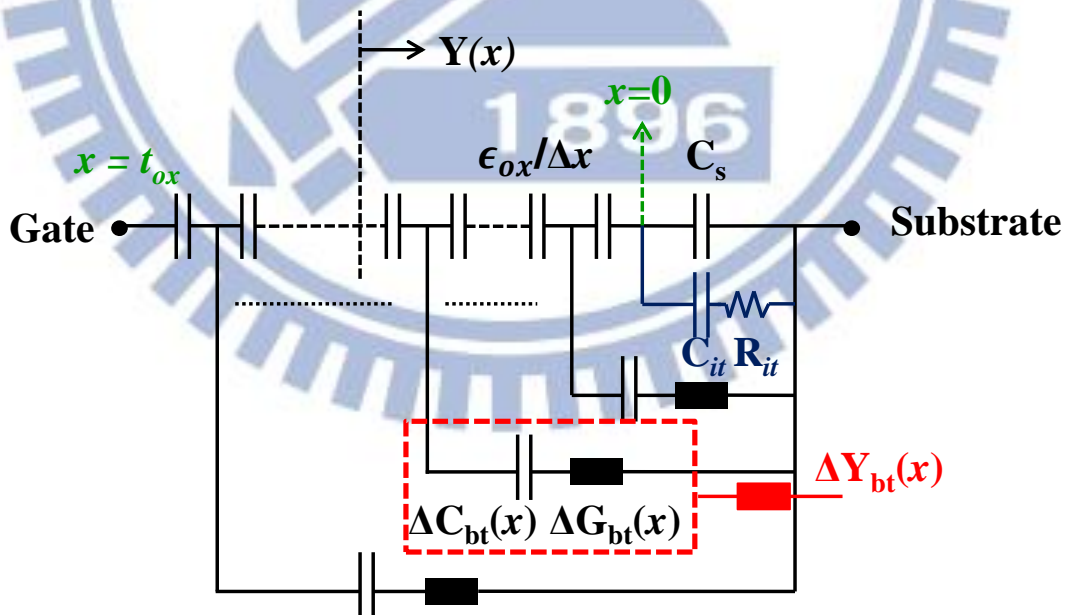
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Gate dielectric    Semiconductor

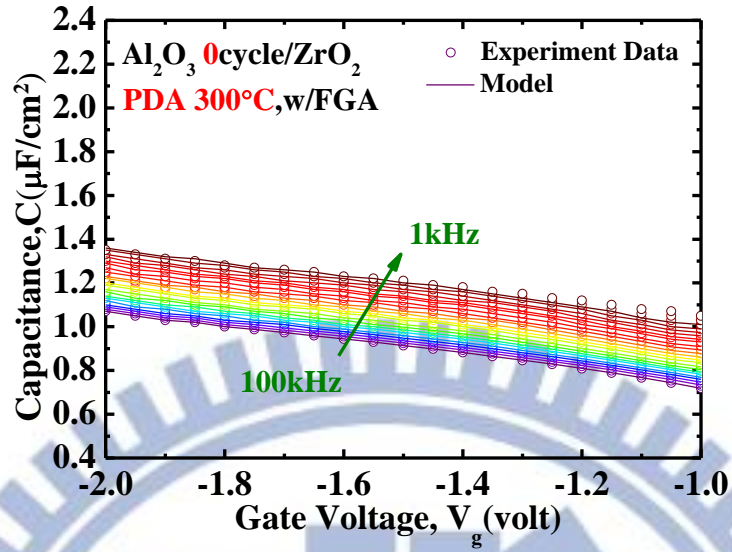


**Fig. 3.1** Band diagram of tunneling mechanism between bulk-oxide traps in the gate dielectric and valence band of the semiconductor.

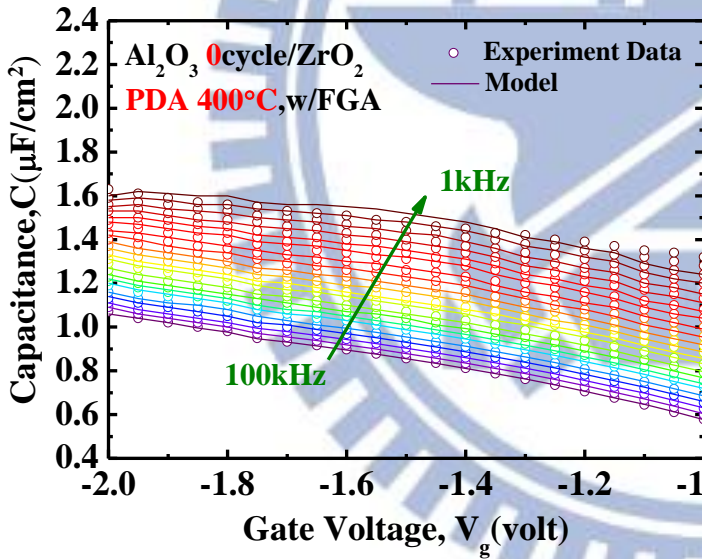


**Fig. 3.2** An equivalent circuit for border traps distributed over the depth  $x$  of the gate dielectrics.

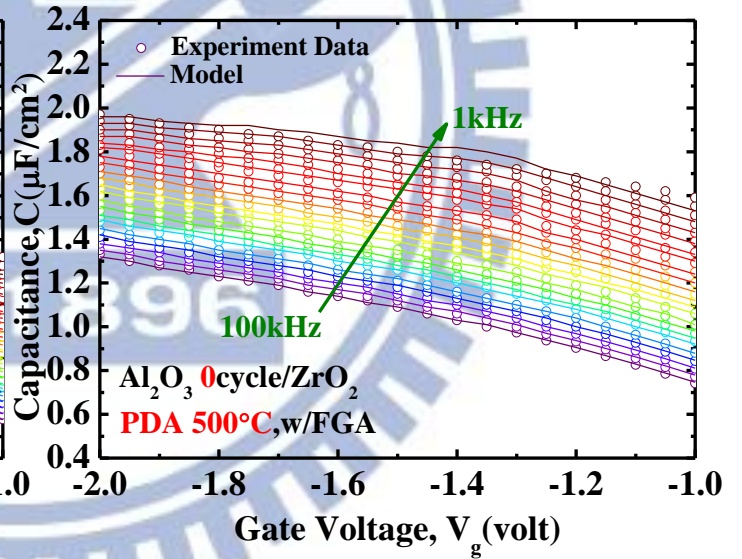
The semiconductor capacitance is represented by  $C_s$ , the interface trap capacitance is  $C_{it}$ , and the resistance  $R_{it}$  is a lossy process of  $D_{it}$ .



(a)

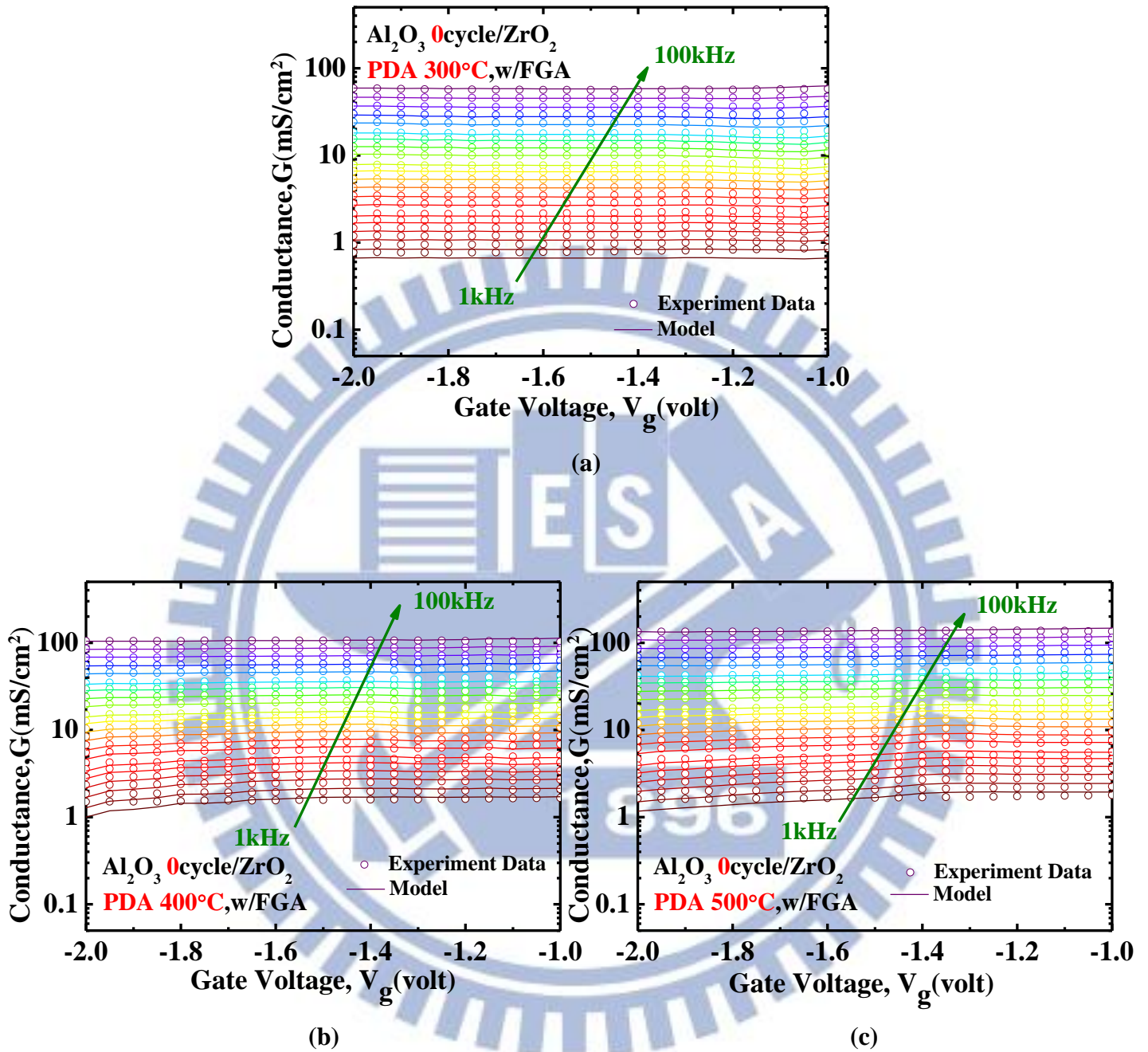


(b)



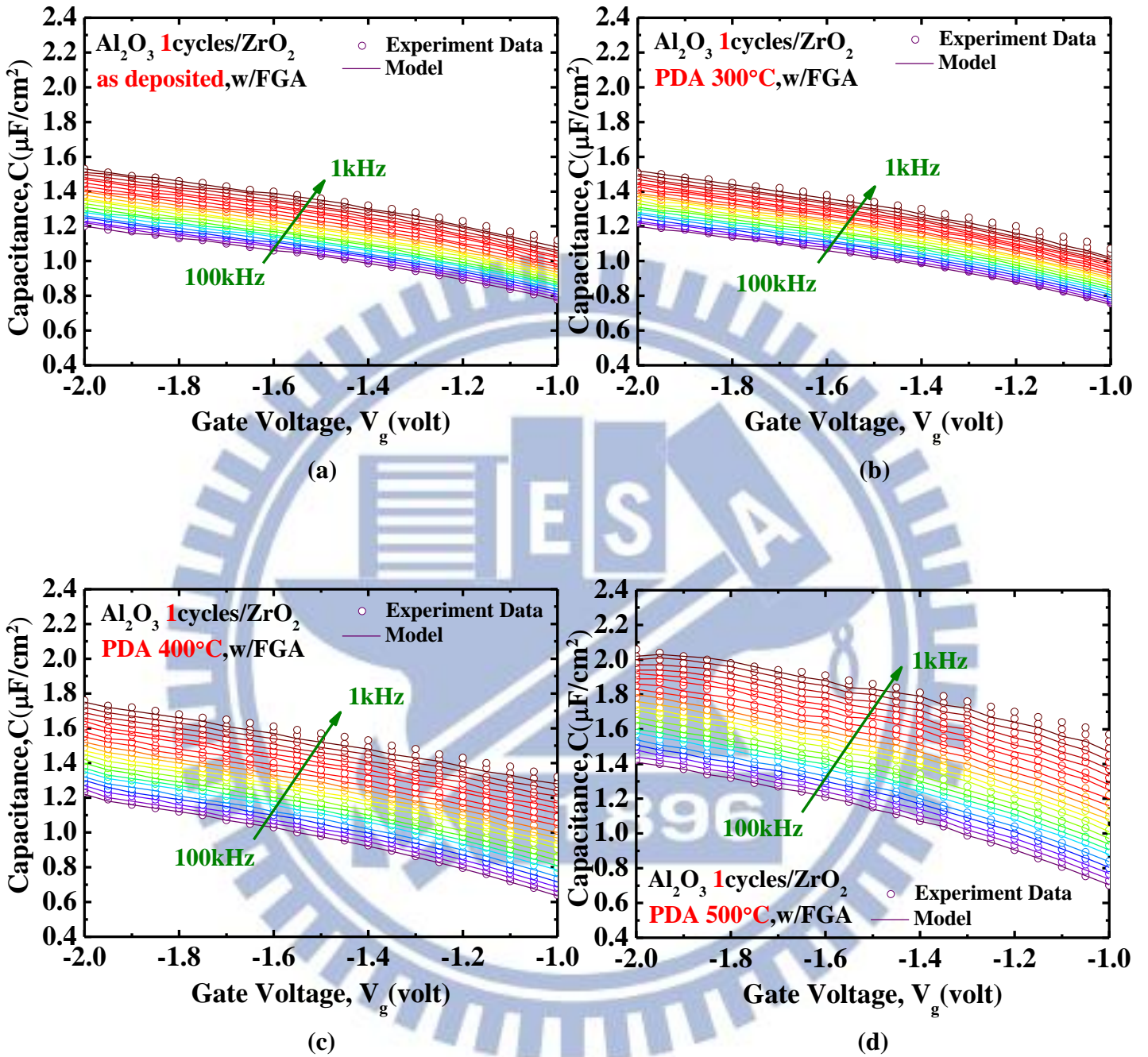
(c)

**Fig. 3.3** The transferred  $C$ - $V$  map of total experimental  $C$ - $F$  data for  $p$ -type Pt/Ti/TMA+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs at the frequency 1 kHz ~ 100 kHz from  $V_g = -1$  to  $-2$  volts at PDA (a) 300 °C (b) 400 °C (c) 500 °C , which compared from the distributed border trap model.

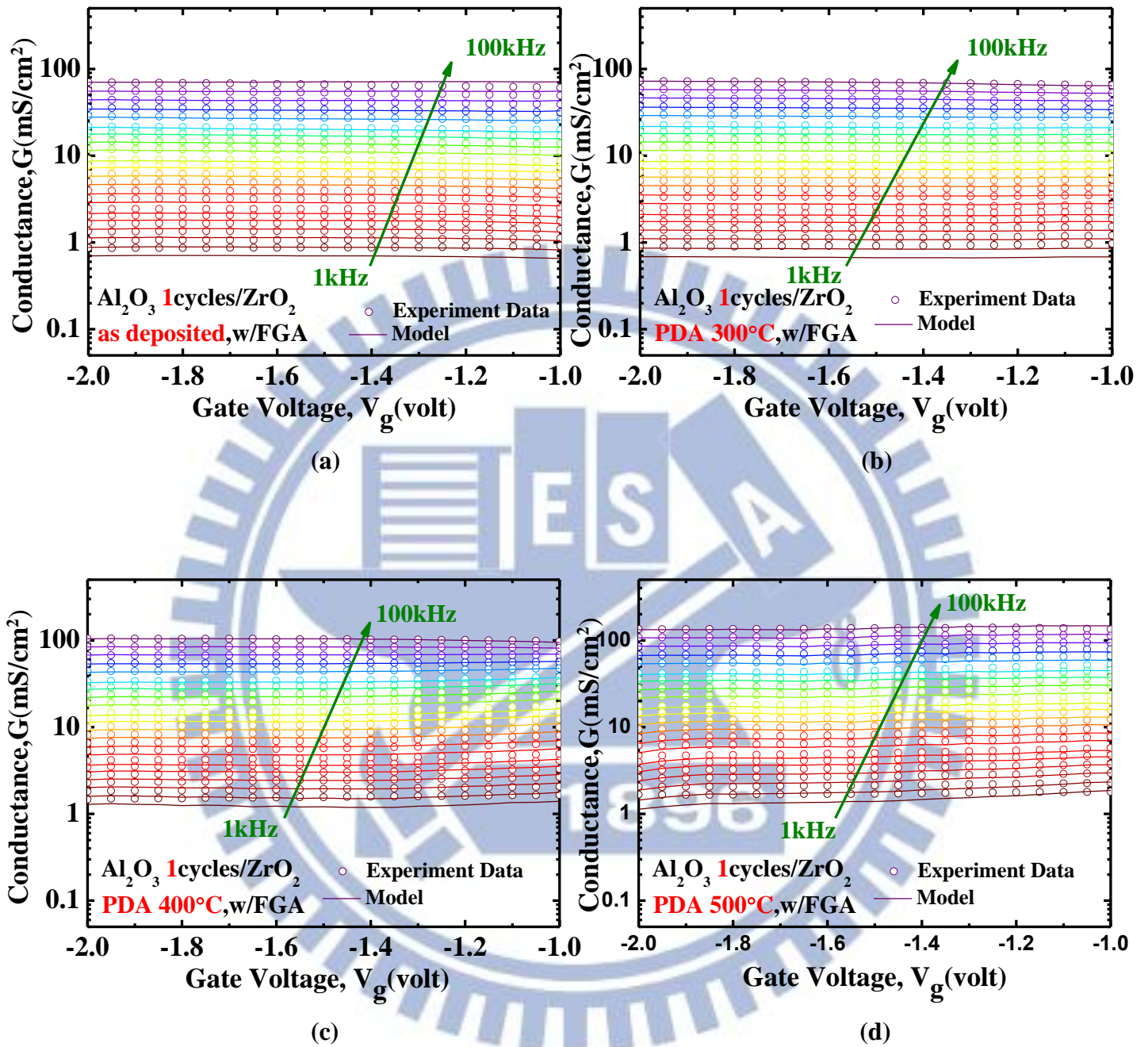


**Fig. 3.4** The transferred  $G$ - $V$  map of total experimental  $G$ - $F$  data for  $p$ -type Pt/Ti/TMA+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs at the frequency 1 kHz ~ 100 kHz from  $V_g = -1$  to  $-2$  volts at PDA (a) 300 °C (b) 400 °C (c) 500 °C , which compared from the distributed border trap model.

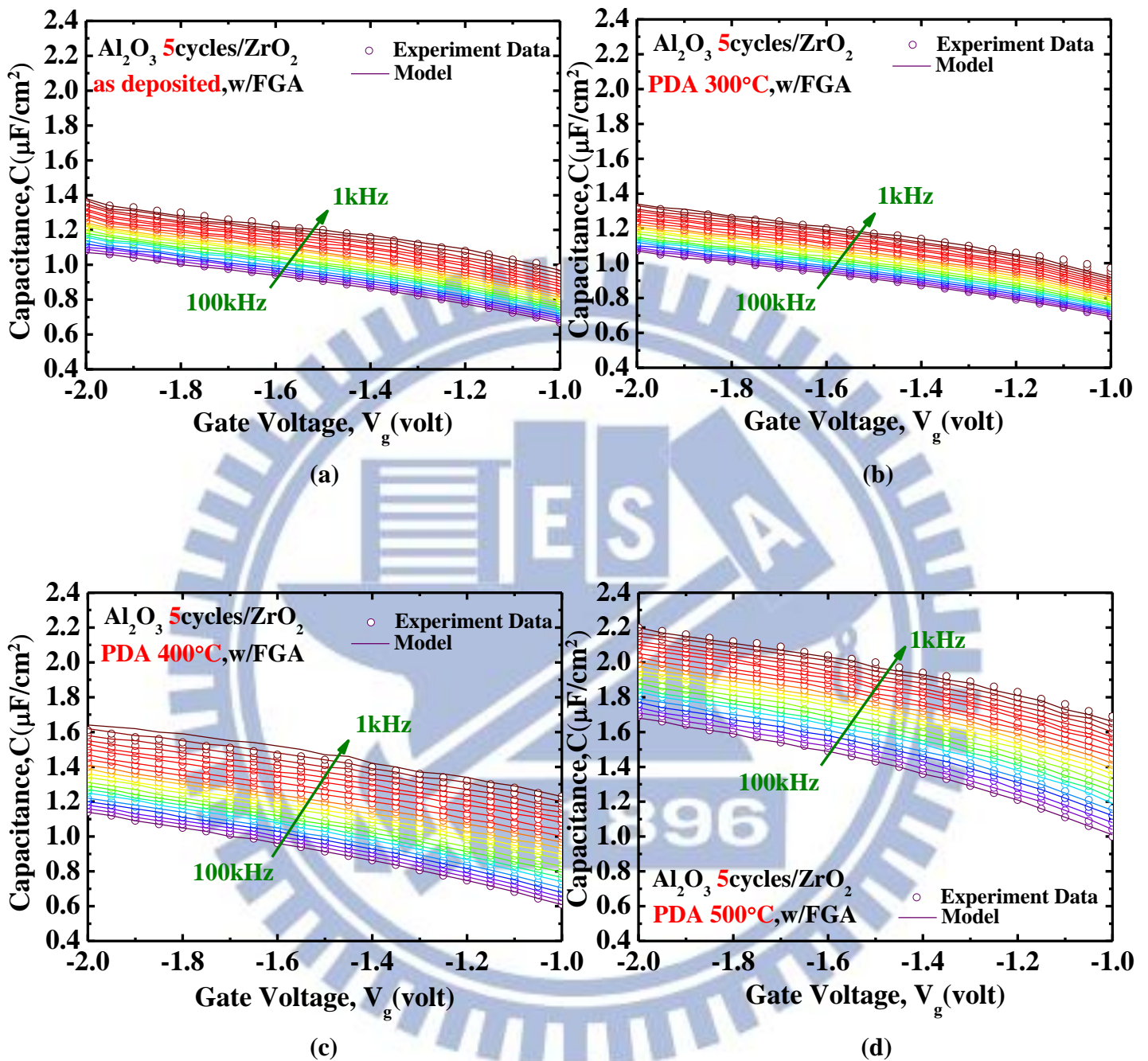




**Fig. 3.5** The transferred C-V map of total experimental C-F data for p-type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 1 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As at the frequency 1 kHz ~ 100 kHz from V<sub>g</sub>= -1 to -2 volts at (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C ,which compared from the distributed border trap model.

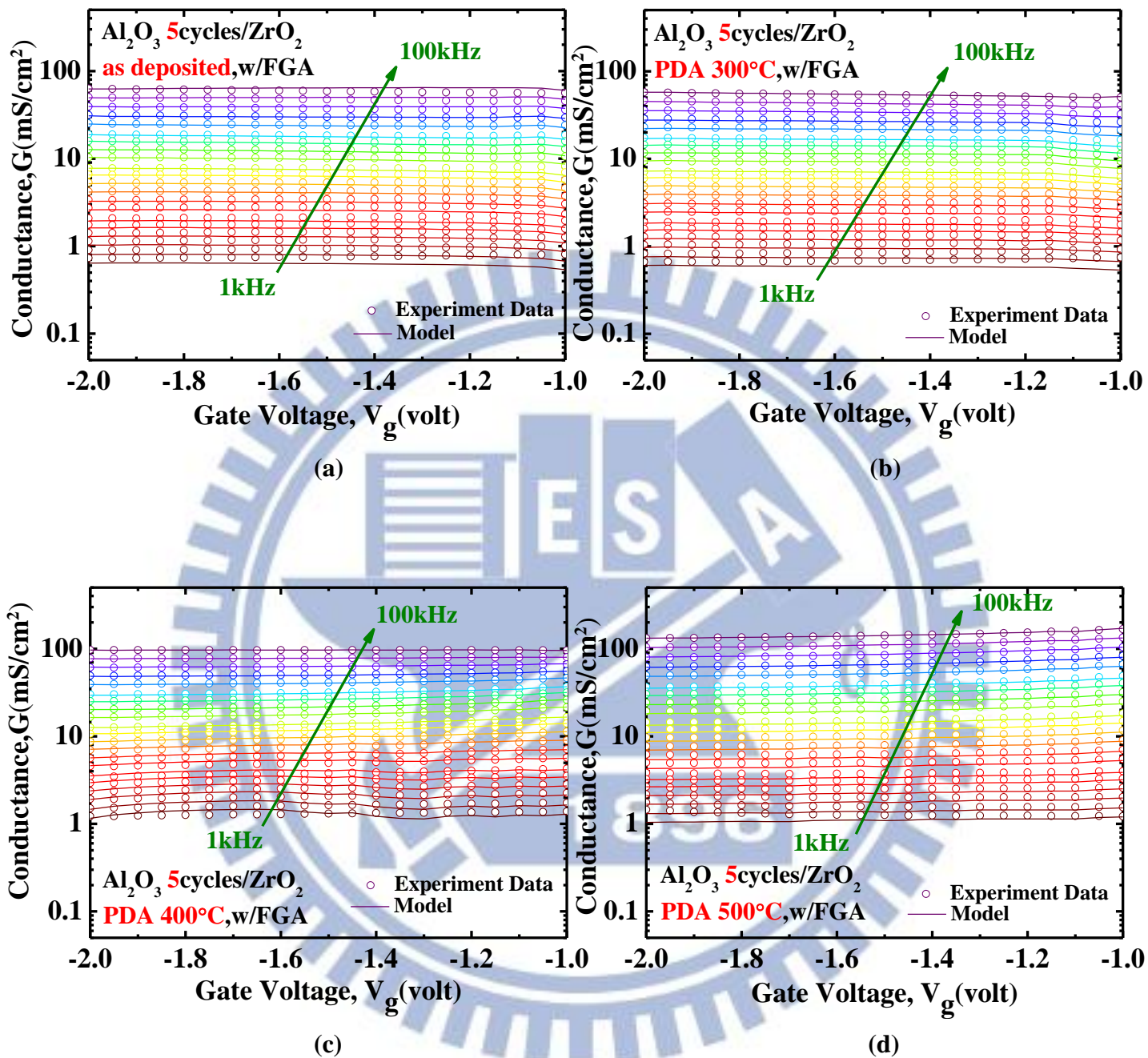


**Fig. 3.6** The transferred  $G$ - $V$  map of total experimental  $G$ - $F$  data for  $p$ -type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 1 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As at the frequency 1 kHz ~ 100 kHz from  $V_g = -1$  to  $-2$  volts at (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C , which compared from the distributed border trap model.



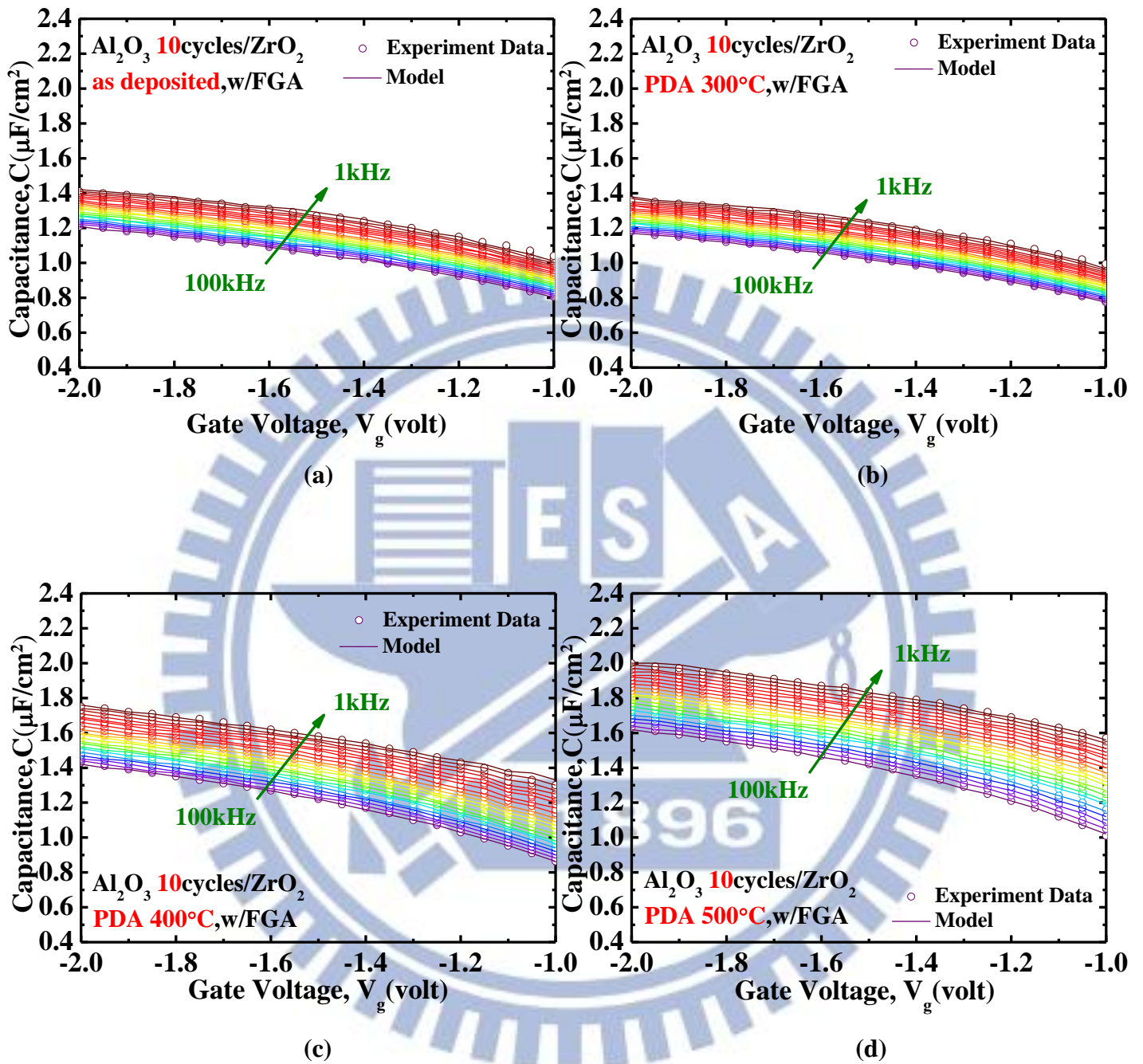
**Fig. 3.7** The transferred C-V map of total experimental C-F data for p-type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 5 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As at the frequency 1 kHz ~ 100 kHz from V<sub>g</sub>= -1 to -2 volts at (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C ,which compared from the distributed border trap model.



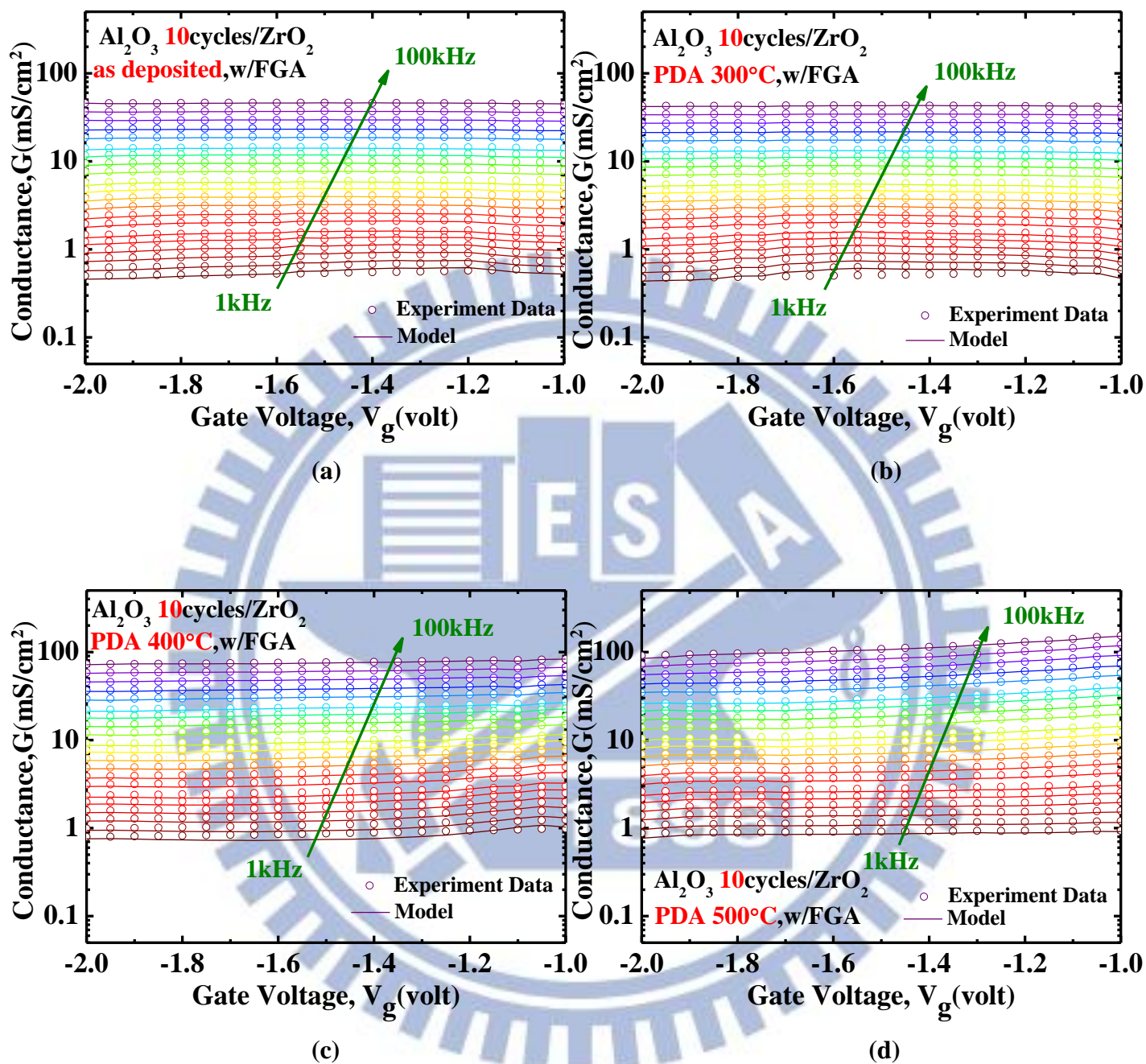


**Fig. 3.8** The transferred  $G$ - $V$  map of total experimental  $G$ - $F$  data for  $p$ -type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 5 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As at the frequency 1 kHz ~ 100 kHz from  $V_g = -1$  to  $-2$  volts at (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C , which compared from the distributed border trap model.

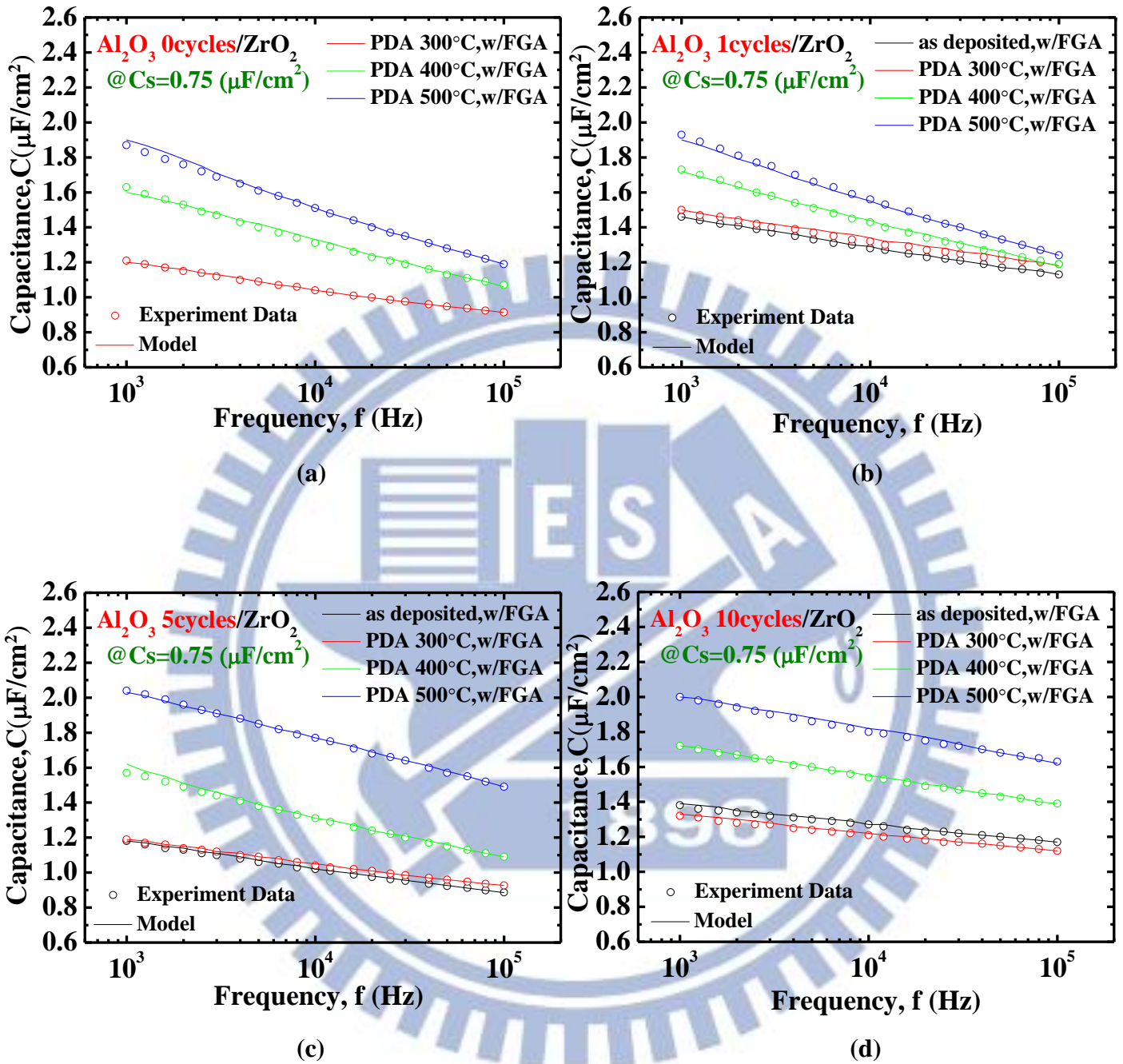




**Fig. 3.9** The transferred  $C$ - $V$  map of total experimental  $C$ - $F$  data for  $p$ -type Pt/Ti/TMA+ $\text{Al}_2\text{O}_3$  10 cycle+ $\text{ZrO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  at the frequency 1 kHz ~ 100 kHz from  $V_g = -1$  to  $-2$  volts at (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C , which compared from the distributed border trap model.

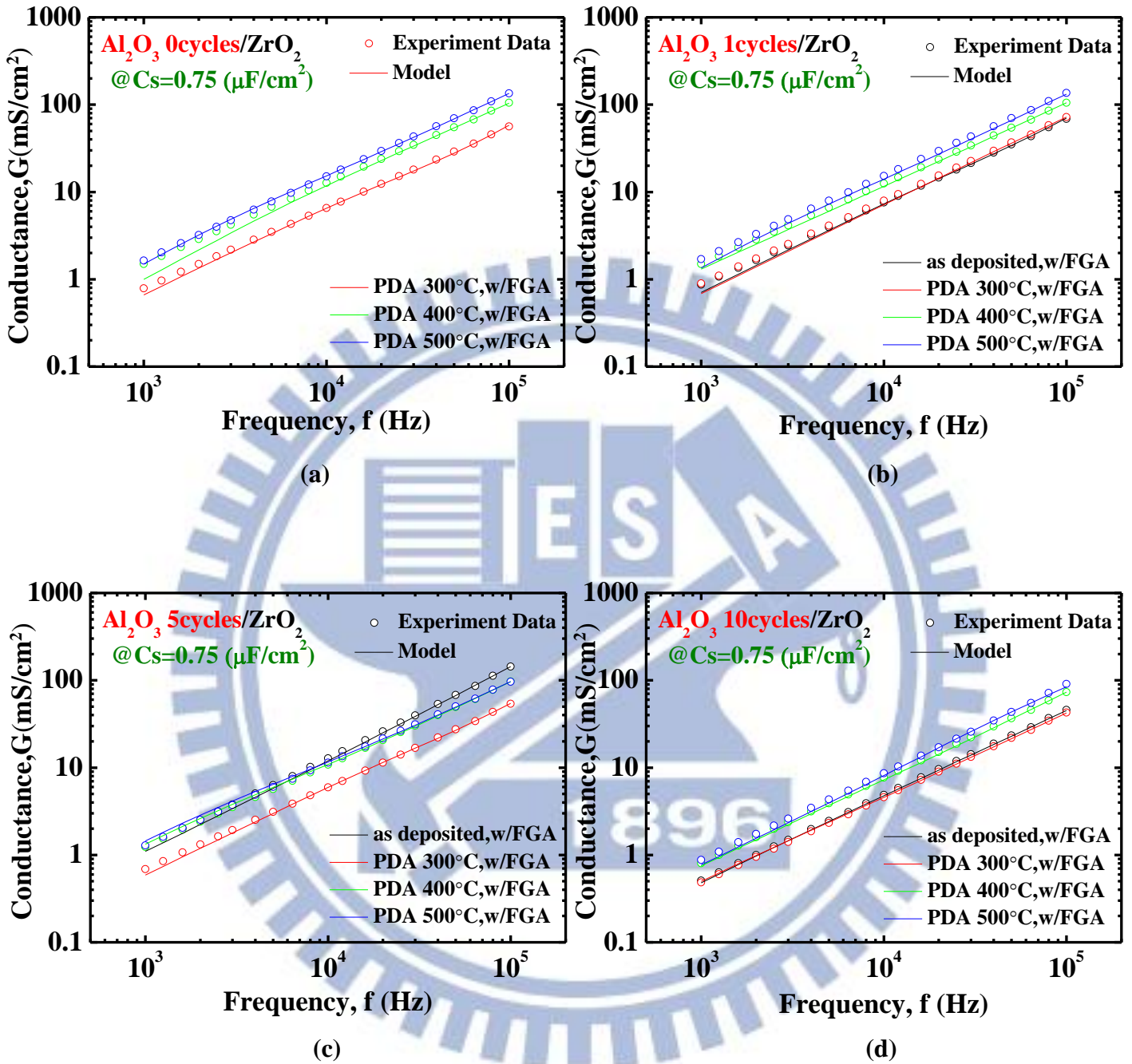


**Fig. 3.10** The transferred  $G$ - $V$  map of total experimental  $G$ - $F$  data for  $p$ -type Pt/Ti/TMA+Al<sub>2</sub>O<sub>3</sub> 10 cycle+ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As at the frequency 1 kHz ~ 100 kHz from  $V_g = -1$  to  $-2$  volts at (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C , which compared from the distributed border trap model.



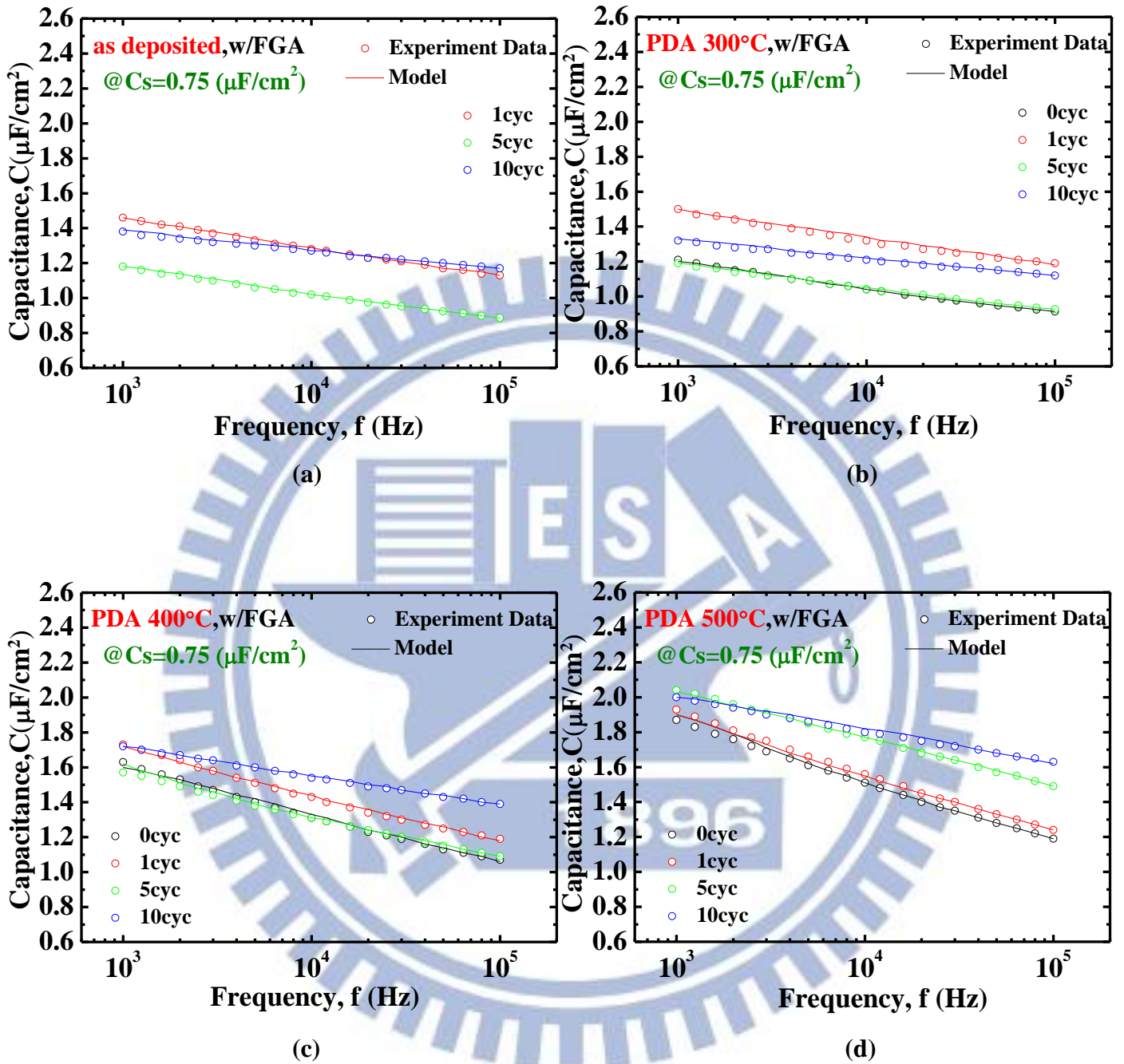
**Fig. 3.11** The frequency dispersion calculated by using the bulk-oxide traps model (line) and experimental data taken at  $C_s=0.75\mu\text{F}/\text{cm}^2$  (circle) of ALD-TMA/ $\text{ZrO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  MOSCAPs under different PDA conditions with various  $\text{Al}_2\text{O}_3$  inter-layer (a) 0 cycle (b) 1 cycle (c) 5 cycle (d) 10 cycle. Moreover, the color of black, red, green, and blue indicate as deposited, PDA 300 °C, 400 °C, 500 °C, respectively.



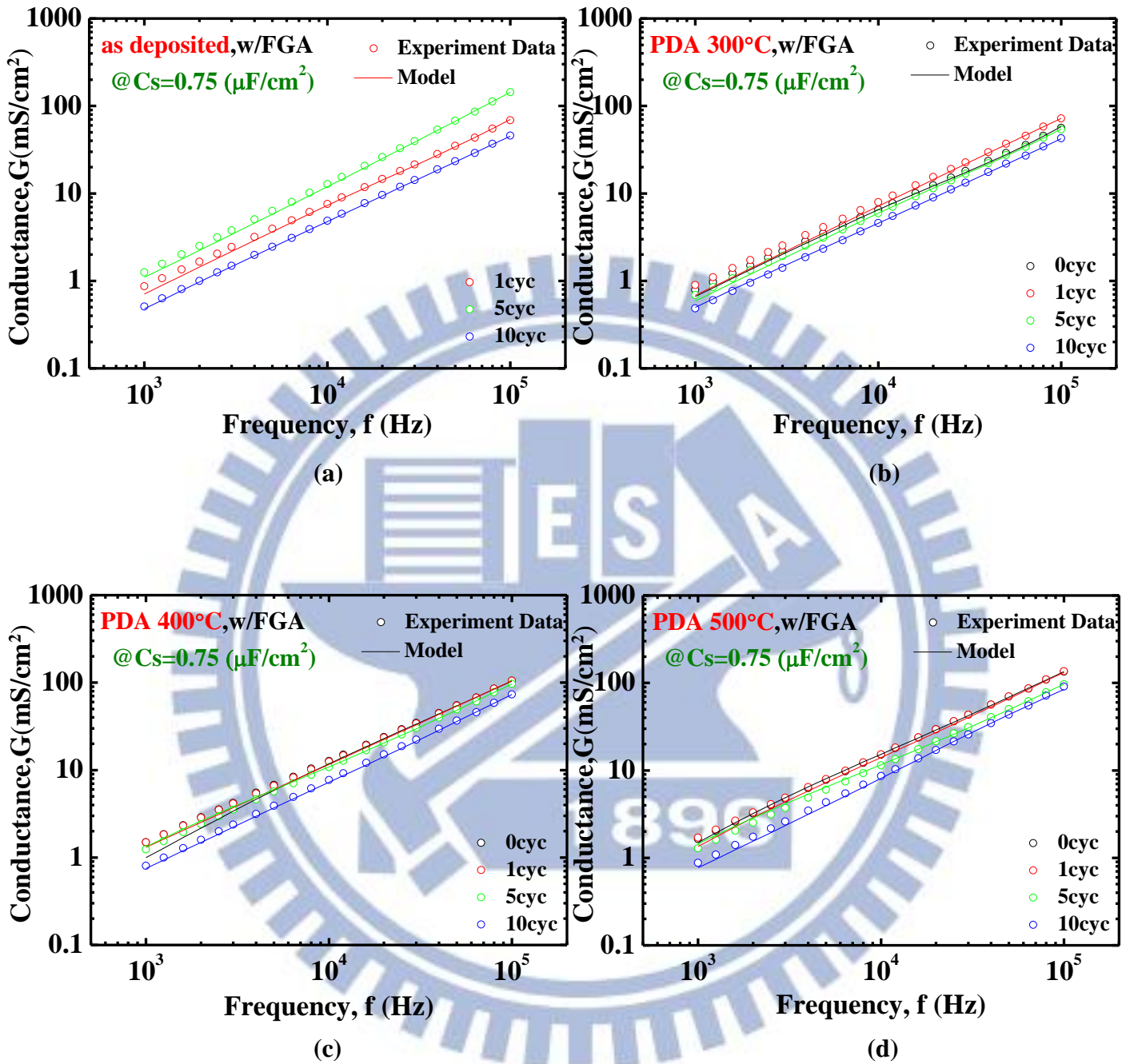


**Fig. 3.12** Comparison of the fitted  $G$ - $F$  map at  $C_s=0.75\mu\text{F}/\text{cm}^2$  of ALD-TMA/ $\text{ZrO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  MOSCAPs under different PDA conditions with various  $\text{Al}_2\text{O}_3$  inter-layer (a) 0 cycle (b) 1 cycle (c) 5 cycle (d) 10 cycle. Moreover, the color of black, red, green, and blue indicate as deposited, PDA 300 °C, 400 °C, 500 °C, respectively.





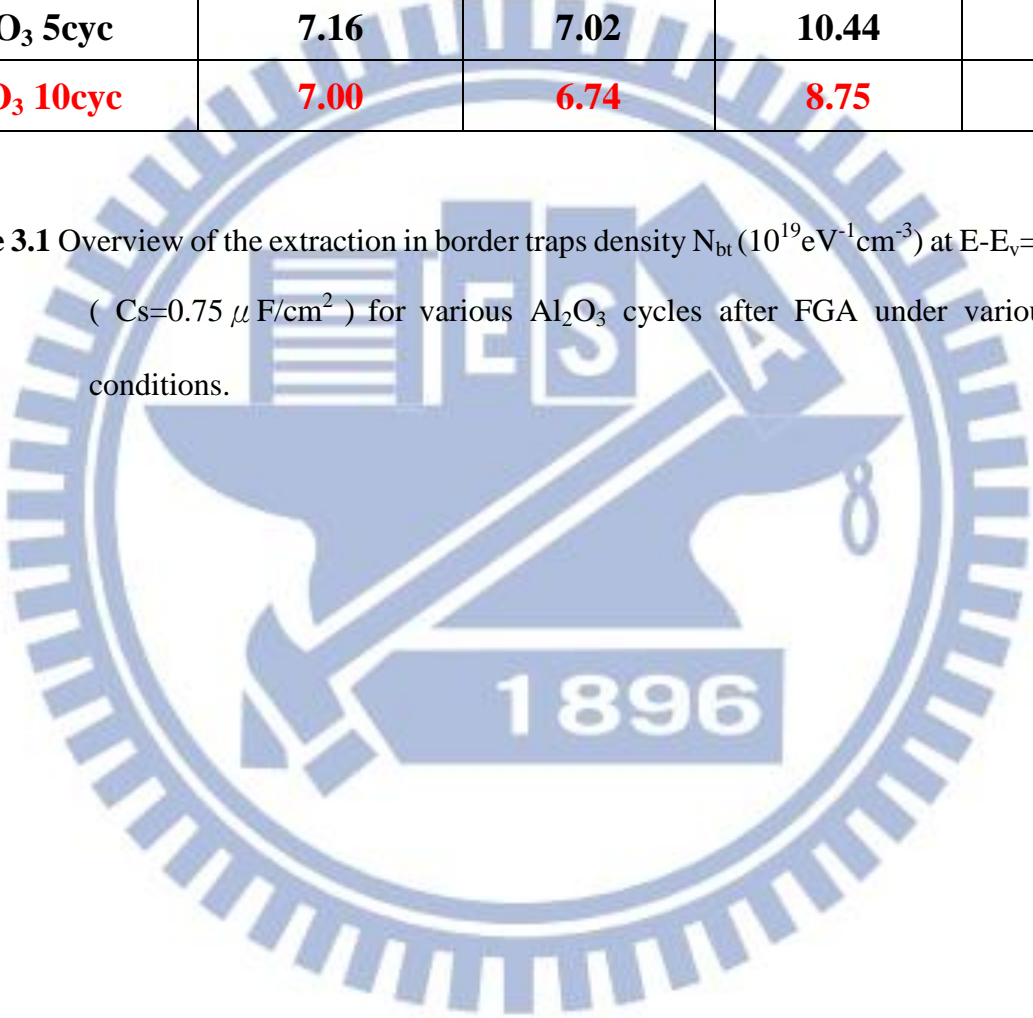
**Fig. 3.13** The frequency dispersion calculated by using the bulk-oxide traps model (line) and experimental data taken at  $C_s=0.75\mu\text{F}/\text{cm}^2$ (circle) of ALD-TMA/ZrO<sub>2</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSCAPs with various Al<sub>2</sub>O<sub>3</sub> inter-layer under different PDA conditions (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.



**Fig. 3.14** Comparison of the fitted  $G$ - $F$  map at  $C_s=0.75\mu\text{F}/\text{cm}^2$  of ALD-TMA/ $\text{ZrO}_2$ / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  MOSCAPs with various  $\text{Al}_2\text{O}_3$  inter-layer under different PDA conditions (a) as deposited (b) 300 °C (c) 400 °C (d) 500 °C.

$N_{bt} (10^{19} eV^{-1} cm^{-3})$	As-deposited	PDA 300 °C /120s	PDA 400 °C /120s	PDA 500 °C /120s
<b>Al<sub>2</sub>O<sub>3</sub> 0cyc</b>		<b>8.93</b>	<b>17.34</b>	<b>21.72</b>
<b>Al<sub>2</sub>O<sub>3</sub> 1cyc</b>	<b>8.34</b>	<b>8.39</b>	<b>14.29</b>	<b>15.62</b>
<b>Al<sub>2</sub>O<sub>3</sub> 5cyc</b>	<b>7.16</b>	<b>7.02</b>	<b>10.44</b>	<b>13.65</b>
<b>Al<sub>2</sub>O<sub>3</sub> 10cyc</b>	<b>7.00</b>	<b>6.74</b>	<b>8.75</b>	<b>12.37</b>

**Table 3.1** Overview of the extraction in border traps density  $N_{bt} (10^{19} eV^{-1} cm^{-3})$  at  $E-E_v=0.15$  eV ( $C_s=0.75 \mu F/cm^2$ ) for various Al<sub>2</sub>O<sub>3</sub> cycles after FGA under various PDA conditions.



# Chapter 4

## *Conclusion*

In this thesis, we have investigated the electrical characteristics and interfacial chemistry of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  MOSCAPs with  $\text{ZrO}_2$  gate dielectric. At first, we utilize the precursors of ALD, such as TMA or TEMAZ, to passivate the surface before depositing dielectrics. Then, the thermal treatments of various PDA conditions with FGA were employed to observe the effect of interface and oxide properties. From the frequency dispersion and hysteresis, we can find the TMA pretreatment is effective to improve the interface and oxide quality. Moreover, comparing to post-deposition temperatures, PDA 300 °C is the best one than the others. The XPS spectra also shows that the higher area ratio of  $\text{In}_2\text{O}_3$  to  $\text{InAsO}_4$ ,  $\text{As}^{2+}$  to  $\text{As}_2\text{O}_5$  and  $\text{As}_2\text{O}_3$  to  $\text{As}_2\text{O}_5$  indicate the passivation of the trivalent oxides or lower valence As on the interface and result in the better electrical characteristics.

However, the  $\text{ZrO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  interfaces still have inferior properties than  $\text{Al}_2\text{O}_3$  on  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ , so we incorporate several  $\text{Al}_2\text{O}_3$  inter-layers to discuss its interface property. From the electrical characteristics of the capacitors, we note that the interface and gate dielectric qualities were much improved by inserting thicker  $\text{Al}_2\text{O}_3$  inter-layer. The  $D_{it}$  at midgap also demonstrates the interface could be passivated within thick  $\text{Al}_2\text{O}_3$ . With the evidence of XPS spectra, we can clarify that the better interface property is caused by the higher ratio values of the  $\text{As}_2\text{O}_3$  and  $\text{In}_2\text{O}_3$  passivation. It might be the thicker  $\text{Al}_2\text{O}_3$  layers tend to displace the  $\text{As}^{5+}$  oxidation state to the  $\text{As}^{3+}$  and  $\text{As}^{2+}$ . Subsequently, we compare the different PDA conditions at each  $\text{Al}_2\text{O}_3$  inter-layer. It shows that PDA 300 °C with FGA demonstrates the best property than others under certain conditions like frequency dispersion, hysteresis, and the density of interface states. Furthermore, the XPS spectra also displays that



the area ratio becomes larger as the PDA temperature decreasing. Comparison of electrical characteristics, it indicates if interface exist more  $\text{As}_2\text{O}_3$  and  $\text{In}_2\text{O}_3$  components, the properties might be improved.

In addition, the influence of frequency dispersion at high negative gate voltage is caused by oxide traps. To further realize the phenomenon of accumulation region, a distributed border traps model between  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  and trap states in the gate dielectrics is developed. Then, we fitted the experimental data with the model and extracted density of trap states  $N_{bt}$  quantitatively. Finally, comparing with the aforementioned chapter, we can find it has good consistency with our experimental data.

In the future, we suggest that the double layer of gate dielectrics in our experiment can be replaced by depositing  $\text{ZrO}_2$  with  $\text{O}_2$ -plasma treatment during the process of atomic-layer deposition, which gate oxide quality may be further improved. Moreover, lower temperature of ALD down to  $200\text{ }^\circ\text{C}$  or less can be a promising method to suppress the interface states. Finally, we expect the improvable gate stacks on III-V substrates can be fabricated by self-aligned MOSFETs.

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碩士論文題目:

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與表面化性分析的研究

**Investigation of Electrical and Interfacial Chemistry Analyses for  
Atomic-Layer-Deposition  $ZrO_2/Al_2O_3/In_{0.53}Ga_{0.47}As$  MOSCAPs**