國 立 交 通 大 學

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碩 士 論 文

直流–直流降壓電源轉換器單晶片補償技術

ON-CHIP COMPENSATION TECHNIQUES FOR DC-DC BUCK CONVERTERS

研 究 生：李家鈞

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研 究 生：李家鈞　　Student：Jia-Jyun Lee

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摘 要

本文主要於較深入討論應用在直流-直流降壓電源轉換器的單晶片補償技術，其中直流-直流降壓電源轉換器的控制方法一般可以分為電壓模式控制及電流模式控制，一般而言，直流-直流降壓電源轉換器的補償電路都需要外掛元件如大電容得到期望的零點位置而使系統可以穩定。

關於電壓模式控制的直流-直流降壓電源轉換器，通常使用型式三的補償電路以增加迴路增益的交越頻率而得到較好的暫態響應，型式三的補償電路多半是由一個主動元件如運算放大器或者是運算電導放大器以及外接的大電容和電阻完成，對於型式三的補償電路的了解可以對於單晶片的比例積分微分控制器的設計提供很好的基礎，整合型的單晶片比例積分微分控制器使用四個運算電導放大器產生兩個零點以補償電壓模式控制的降壓電源轉換器產生的雙極點系統可以穩定，電路的結果證明單晶片的比例積分微分控制器和型式三的補償電路的表現是相同的。

至於電流模式控制的直流-直流降壓電源轉換器，其優點在於使用比例積分控制器即能使系統可以穩定，以補償的角度而言，這個好處是很明顯的，然而，比例積分控制器仍須使用外接的大電容，這還是在晶片整合上形成障礙，於是對單晶片的電流模式密勒補償及時間模式密勒補償電路有進一步的介紹、分析及實現，單晶片的電流模式密勒補償利用電流對可以整合在晶片上的小電容充放電的密勒效應而得到等效大電容值，單晶片的時間模式密勒補償則利用電路取樣原理在非常短時間內對誤差訊號作積分而得到整合在晶片上的小電容值等效放大，電路的結果證明單晶片的電流模式密勒補償及時間模式密勒補償的效能非常接近。

On-Chip Compensation Techniques for DC-DC Buck Converters

Student: Jia-Jyun Lee Advisor: Dr. Ke-Horng Chen

Department of Electrical and Control Engineering
National Chiao-Tung University

Abstract

This work is discussing the comprehensive concepts of on-chip compensation (OCC) techniques for DC-DC buck converters with voltage mode control and current mode control. In general, the compensator network of DC-DC buck converter needs the external components for the large value capacitors to place the zeros in desired location to stabilize the system. Thus, the compensation of the regular DC-DC converter is completed by an off-chip compensator.

Regarding DC-DC buck converter with voltage mode control, Type III compensator is usually employed to extend the loop gain crossover frequency for better transient response. Type III compensation is often implemented by a single active element such as an OPA or OTA with off-chip large capacitors and resistors, and its insight of compensation provides the fertile background to develop the counterpart PID OCC. The integrated PID OCC takes four OTAs for the creations of two zeros to compensate the double poles from buck converter with voltage mode control. The simulation results show that the performance of PID OCC is comparable to that of Type III off-chip compensation.

As to DC-DC buck converter with current mode control, the advantage is that PI compensator is sufficient to manage the stability issue. The simplicity is obvious from the compensation point of view. However, the large capacitor required for PI compensator remains the problem to its integration on chip. Current mode Miller (CMM) OCC and time mode Miller (TMM) OCC is therefore introduced, analysed, implemented and simulated. CMM OCC by definition utilizes current to charge and discharge the small on-chip capacitor achieving the Miller effect for the large equivalent capacitance. On the other hand, TMM OCC makes use of sampling and hold to integrate the error information within very short period of time, and thus the capacitance amplification of the small on-chip capacitor is obtained. According to simulation results, the performance of CMM OCC and TMM OCC is compatible with current mode control buck converter.

Acknowledgements

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Symbol and Abbreviation

OCC On-Chip Compensation

PID Proportional-Integral-Derivative

PI Proportional-Integral

CMM OCC Current Mode Miller On-Chip Compensation

TMM OCC Time Mode Miller On-Chip Compensation

OTA Operational Transconductance Amplifier

OPA Operational Amplifier

DCR DC Resistance of an inductor

ESR Equivalent Series Resistance of a capacitor

PWM Pulse Width Modulation

E.A. Error Amplifier

T.F. Transfer Function

CCM Continuous Conduction Mode

DCM Discontinuous Conduction Mode

D Duty Ratio

Q Quality Factor

R_O Output Resistance

R_{ON} On-resistance of MOSFET

MOSFET Metal-Oxide-Semiconductor Field Effect Transistor

C_{OX} Capacitance of Oxide layer

μ_n Mobility of N channel MOSFET

Chapter 1
Introduction

1.1 The Fundamentals of DC-DC Converter

An electronic circuit that converts a voltage with a dc level in a controllable manner without any energy loss is usually called an ideal DC-DC converter mainly to supply the regulated voltage and improve the power efficiency. As shown in Fig.1, the ideal DC-DC converter in the simplified diagram is controlled by the control parameter ß. For Vin, it could be such as battery, and Vo could be the applications such as CPU, Logic, Memory, or the portable electronic devices etc. When feedback path is applied as shown in Figure 1, the output voltage could be better regulated against the fluctuation in the input voltage or loading current. A vast majority of applications in the leading edge technology actually require an output voltage which is tightly regulated. To meet the demanding specification, the circuits in DC-DC converter including PWM modulation, controller design and its compensation, even the protection mechanisms are also turning complicated, and therefore are categorized in power management unit (PMU).[1]

As shown in Figure 2, the diagram of a practical DC-DC converter essentially has two sections. One is the power stage that is comprised of switch and LC filtering, and the other is the control section including modulator where PWM modulation is doing its work to control the duty ratio of the switch for correct output voltage level, and compensator whose purpose is to stabilize the loop and improve the frequency response for better transient performance. More detailed will be revisited in the following paragraphs.

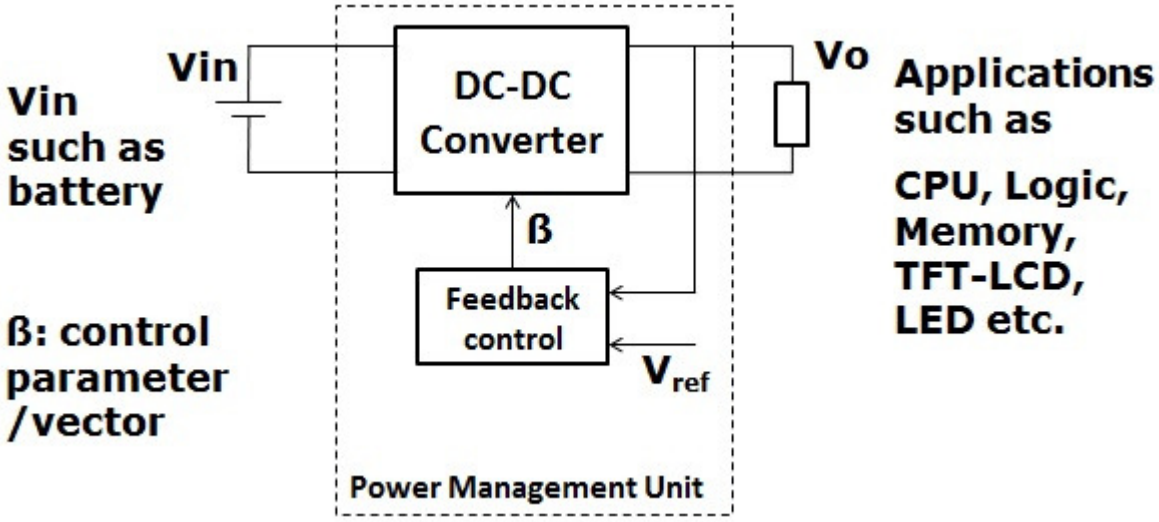


Figure 1 Simplified diagram of an ideal DC-DC converter

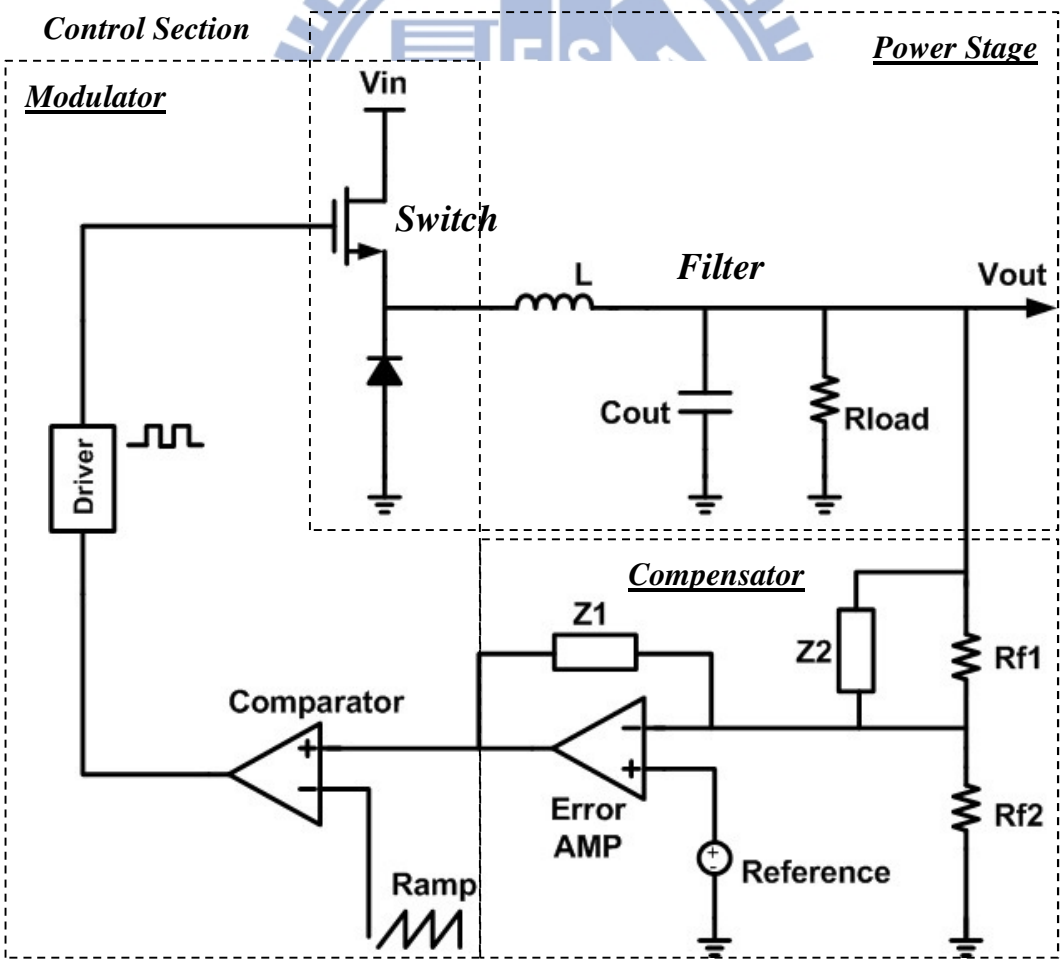


Figure 2 Diagram of a practical DC-DC converter

1.2 Converter Topology

This section is to briefly look at the three fundamental converter topologies as illustrated in Figure 3 including buck converter, boost converter, and buck-boost converter. As far as the scope of this thesis is concerned, the buck converter, aka step-down DC-DC converter, will be discussed in more details in the following portions of control schemes and compensations.

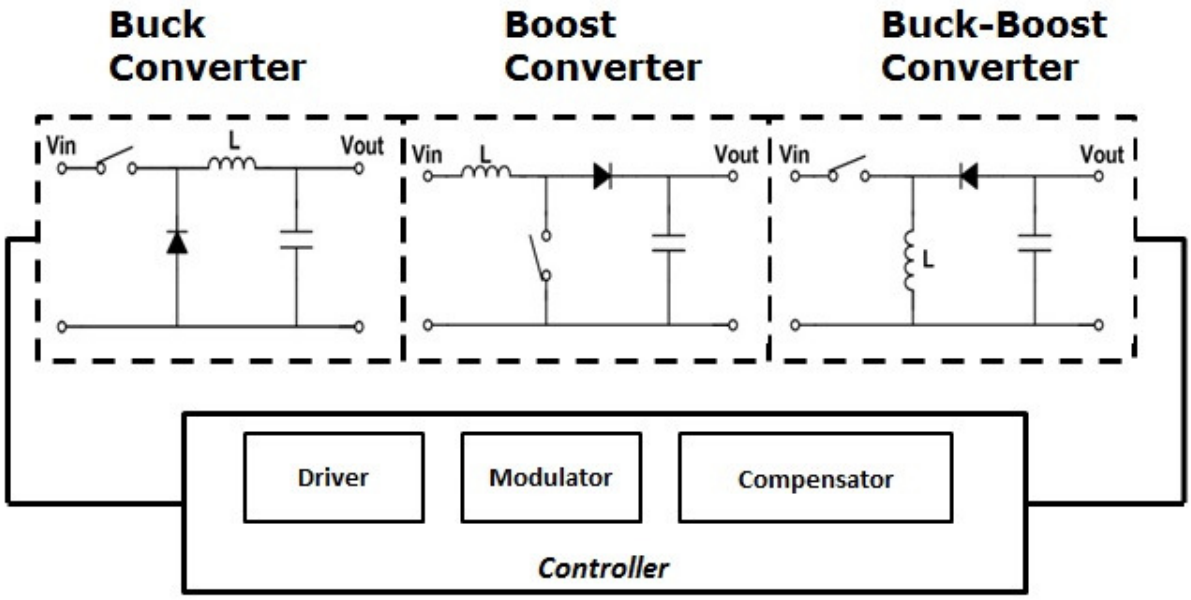


Figure 3 Converter topologies with controller embedded

The simplest way to lower the voltage of a DC supply is to use a linear regulator like a LDO, but linear regulator wastes too much energy dissipating power to heat. Buck converters, on the other hand, could easily have much higher efficiency (95% or above for integrated circuits), making them the converter of choice to convert the main voltage in an electronic system such as a desktop or a laptop down to the lower voltage provided to CUP, HD, or Display etc.

A boost converter that has the output voltage higher than the input voltage is also called a step-up converter because it “steps up” the input voltage. The converter topology of boost

differs from Buck in the position of switch if it separates inductor and capacitor. This circuit topology could be in the application of low power battery to have the ability of well using up the remaining energy in a battery. That energy otherwise is wasted as the low voltage of a nearly depleted battery makes it not capable for a normal loading.

A buck–boost converter that has an output voltage either higher or lower than the source voltage actually has two different topologies, the inverting and the non-inverting topology. For the inverting topology, the output voltage of buck-boost is of the opposite polarity to the input, and the circuitry has the similar topology to the boost converter and the buck converter. As for the non-inverting buck-boost, it is a buck followed by a boost, and the output voltage is thus the same polarity with the input. A non-inverting buck-boost is in favour of a single inductor that could be buck inductor and boost inductor depending on the controls of the switches.

1.2.1 Open Loop System

In Figure 4 it represents the basic building blocks of DC-DC buck converter system. Prior to the compensator is included for a closed loop system, a generic open loop system is as shown in Figure 5 and its Bode plot shown in Figure 6. For systems with low DCR and ESR parameters, the phase will experience a sharp slope downward at the double pole while the gain will have a rather high peak. Systems that have such resonant output filters will be more difficult to do the compensation, and typically need a Type III compensation, which will be discussed later in Chapter 2.[2]

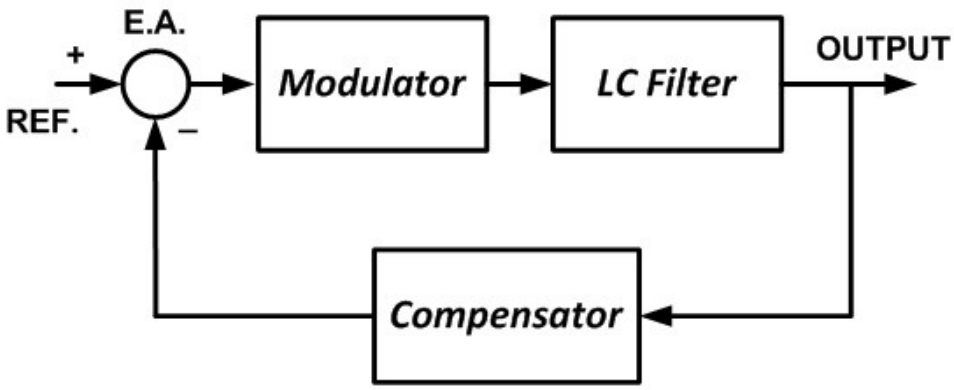


Figure 4 Basic Blocks of Buck converter

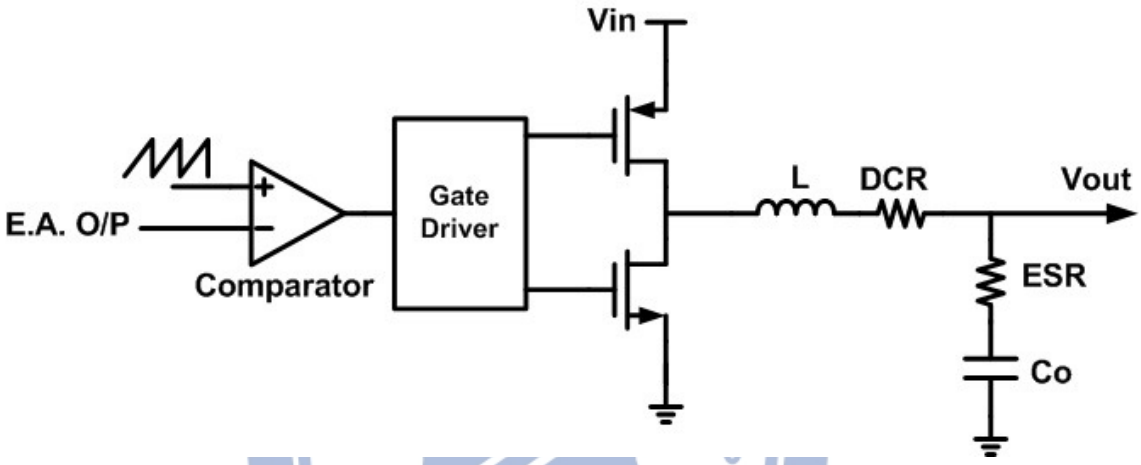


Figure 5 Open loop of Buck converter

$$GAIN_{OPENLOOP} = \frac{V_{IN}}{\Delta V_{OSC}} \frac{1 + s * ESR * C_O}{1 + s(ESR + DCR)C_O + s^2 L_O C_O}$$

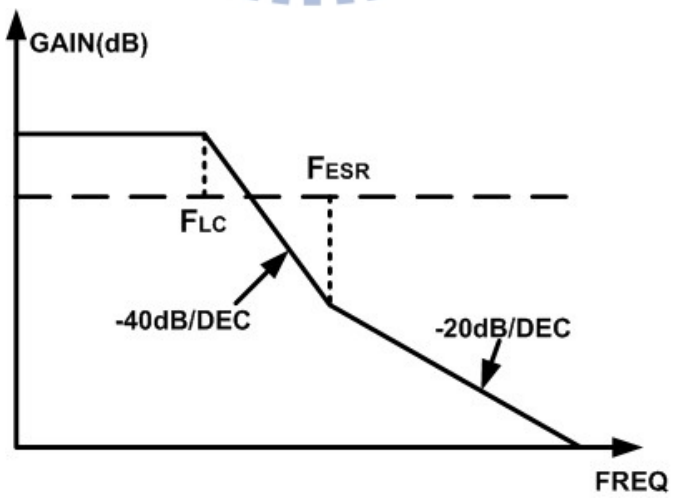


Figure 6 Bode plot of open loop Buck converter

1.3 Compensation Schemes

The criterion for a stable loop is that the total phase shift must be less than 360◦ at the cross over frequency as gain amplitude is 0 dB. This includes the necessary 180◦ negative feedback connection. The amount by which the total phase shift is less than 360◦ at the crossover frequency is called the phase margin. To ensure a stable loop under worst-case condition for a DC-DC converter, the most common practice is to design for 45◦ to 60◦ phase margin. As the compensation schemes shown in Table 1, the schematics and Bode plots are illustrated, and we would go over the more details in the following sections.[5]

1.3.1 Closing the Loop

As mentioned the compensation schemes are for closing the control loop that allows the regulator to adjust to load perturbations or changes in the input voltage which may adversely affect the output. Proper compensation of the system will allow for a predictable bandwidth with unconditional stability. In most cases, a Type II or Type III compensation network will properly compensate the system. The ideal Bode plot for the compensated system would be a gain that rolls off at a slope of -20dB/decade, crossing 0db at the desired bandwidth and a phase margin greater than 45° for all frequencies below the 0dB crossing. For synchronous and non-synchronous buck converters, the bandwidth should be between 20 to 30% of the switching frequency. In the next section, the compensation options and compensations design procedure will be introduced.

1.3.2 Compensation Guideline

To implement the desired loop gain with sufficient zero-cross over frequency and a safe phase margin, a sound compensation must be taken into consideration.

A guideline of practical procedure is as follows: [9]

First step - Follow the specification to collect system parameters such as input voltage, output voltage and switching frequency etc.

Second step - Locate the poles and zeros of open loop that is without compensation..

Third step - Determine the zero crossover frequency and compensation type. The compensation type is determined by the location of zero crossover frequency and characteristics of output capacitor.

Forth step - Calculate the designed locations of zeros and poles for the desired compensator.

Fifth step – Calculate the parameters of compensator components including resistor and capacitor of designed compensator from standard catalogue so that the parameters could be as close to calculated value as we could.

1.3.3 Type III Compensation

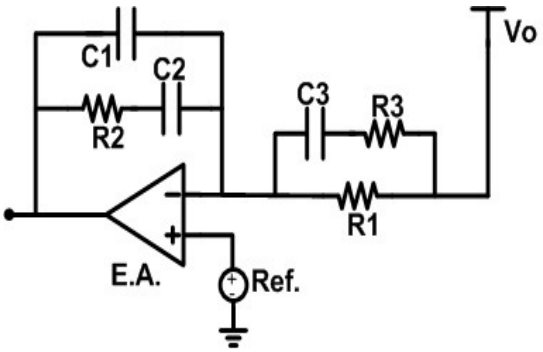
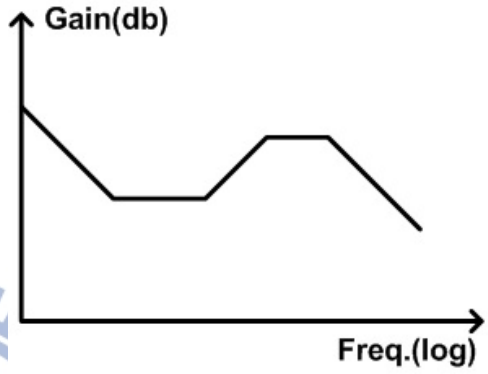
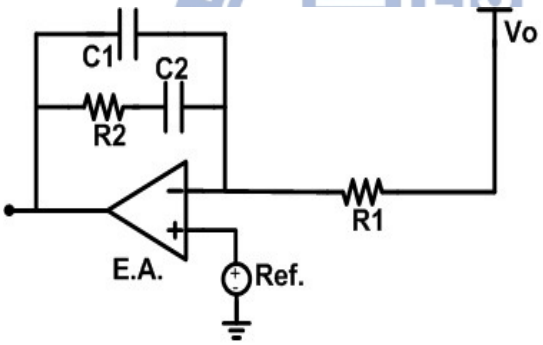
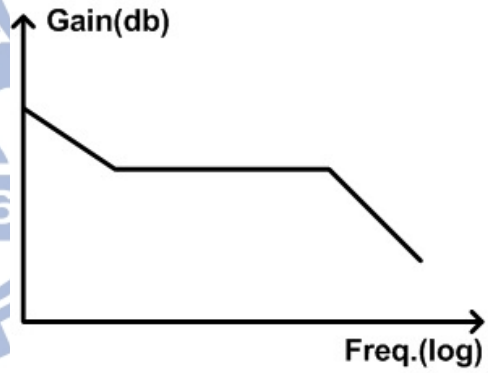
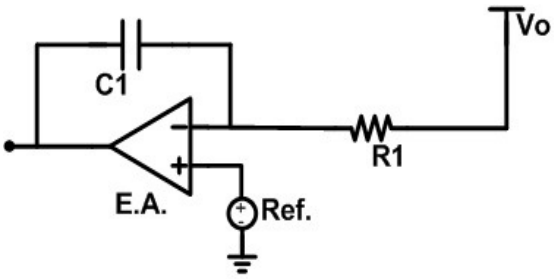
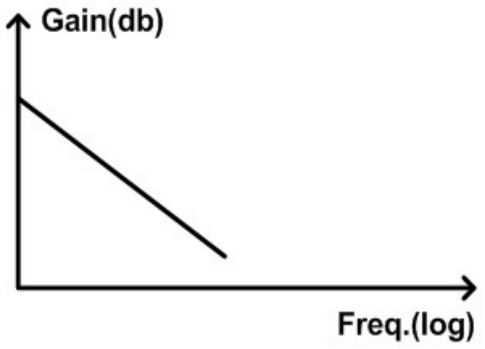
Three types of error amplifier compensation schemes are most often used called the Type I, Type II, and Type III in order of the complexity and flexibility as shown in Table 1. As a matter of fact, Type I and Type II are just the subsets of Type III compensator. The transfer function of a Type III error amplifier is given by [8]

$$\mathrm{A(s)} = \frac{\omega_{p0}}{s} \times \frac{(\frac{s}{\omega_{z1}} + 1)(\frac{s}{\omega_{z2}} + 1)}{(\frac{s}{\omega_{p1}} + 1)(\frac{s}{\omega_{p2}} + 1)}$$

1.3.4 Type I and II Compensation

As shown in the transfer function of Type III compensator, it actually provides one pole-at-zero and two poles and two zeros. Compared with Type III, they are less powerful for Type I which only provides one pole-at-zero, and Type II which provides one pole-at-zero and one pole and one zero.

Table 1 Compensation schemes

Scheme	Implementation	Bode plot
Type III		
Type II		
Type I		

1.4 Controller Alternatives

The output characteristics can be modified by means of the control of duty ratio. As a matter of fact, the feedback path will control duty ratio to maintain constant output voltage no matter what conditions of input and output. Generally, there are two major options to control the duty ratio in DC-DC converter, voltage mode and current mode. The following sections are therefore focused on how the duty ratio is well elaborated. [4]

1.4.1 Voltage Mode Control

For voltage mode, as its name implies the output voltage is the parameter feedback loop mainly controls. As illustrated in Figure 7 that is very typical buck converter with voltage mode controller, and it is not difficult to know that voltage mode is a single loop control. In voltage-mode control, a control signal is compared to a ramp wave to control the duty cycle of the power switch. The higher the error voltage, the longer the switch is on. And the error voltage is derived in the feedback loop from the error amplifier that amplifies the difference between the output voltage and the reference voltage. It is applying pulse width modulation (PWM) to regulate the output voltage as shown in Figure 8 how the switching signal is modulated by the control signal which is generated from error amplifier and then compared to a ramp wave.

Voltage mode is a direct duty cycle control as the control signal or error voltage directly drives the duty ratio, and consequently it has a wide range of duty ratio; however the bandwidth of voltage mode control would be limited by the compensation of LC resonant frequency, and then the performance of the transient characteristics is dramatically poor if the bandwidth is not wide enough. In the next chapter, the solution to this problem will be further studied with conventional off-chip and on-chip compensation.

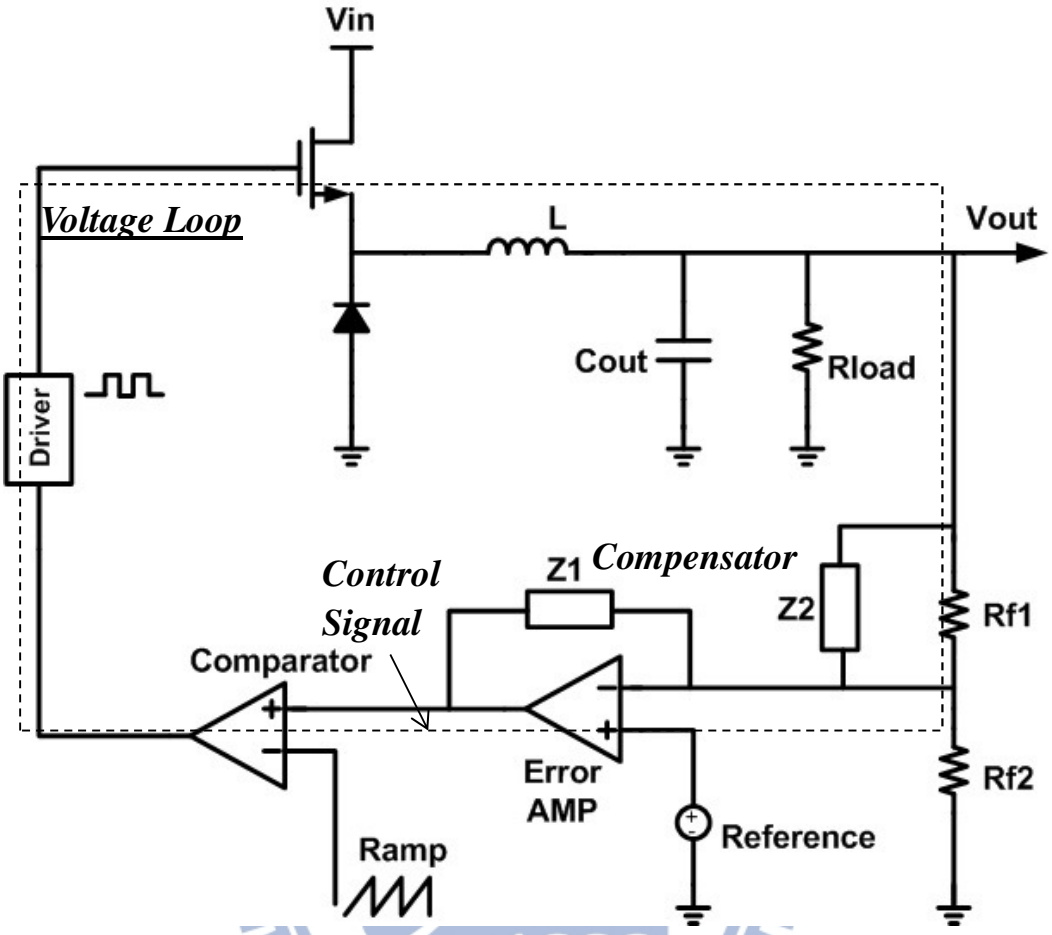


Figure 7 Voltage mode control buck converter

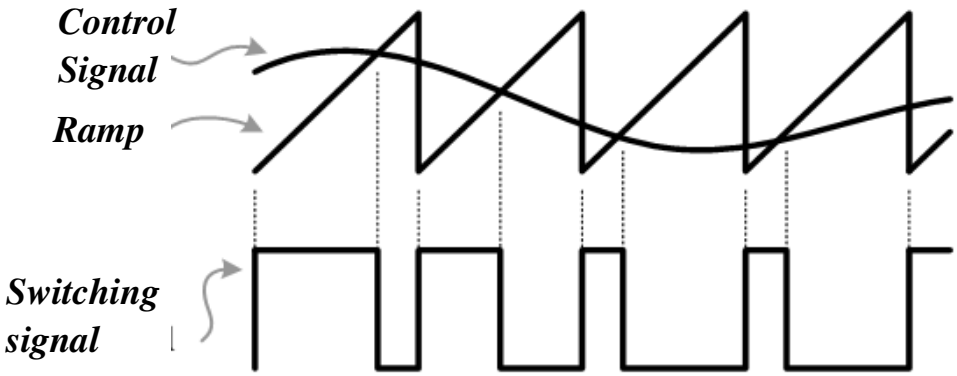


Figure 8 Voltage mode control duty ratio waveforms

1.4.2 Current Mode Control

Current mode control was formally introduced to the power electronics world in 1978 [10]. It was quickly accepted as the common approach to control power supplies. A standard implementation of current-mode control is shown in Figure 9 A general implementation of current mode control Figure 9. Compared to single loop in voltage mode, current mode control features a current loop or the inner loop in Figure 9 and a voltage loop or outer loop. The error voltage is used to directly control the peak of the switch current. (A sawtooth ramp is often used in most cases and is referred to as slope compensation in current mode control.) This dramatically changes the behavior of the DC-DC converter. From the mathematical point of view, the transfer function of voltage mode is the second order which is corresponding to LC double poles, and the control to output with current mode is the first order. The major pros and cons of current mode control are briefly summarized in Table 2.

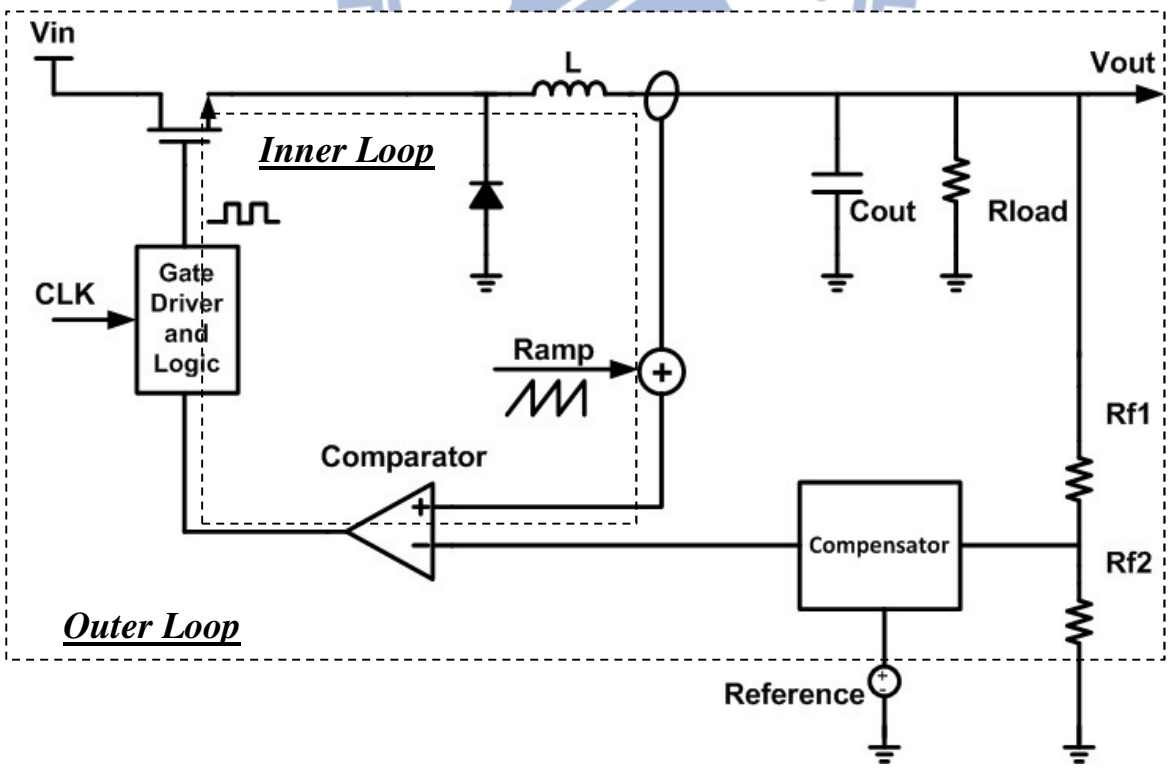


Figure 9 A general implementation of current mode control

Table 2 Pros and cons of current mode control [10]

Control to output T.F. of Voltage mode

$$\frac{V_o}{V_c} = K_v \frac{1 + sCR}{1 + \frac{s}{\omega_o Q} + \frac{s^2}{\omega_0^2}}$$

$$where\ \omega_0 = \frac{1}{\sqrt{LC}}\ and\ Q = \frac{R}{L}$$

Control to output T.F. of current mode

$$\frac{V_o}{V_c} = K_i \frac{1 + sCR}{1 + sCR_L} F_h(s)$$

$$where\ F_h\ is\ a\ 2nd\ order\ pair\ of\ poles\ at\ half\ the\ switching\ frequency$$

CONS	***PROS***
1.Current Sensing: It takes additional circuits to accurately sense either switch current or inductor current. The current sensing must be very wide band to correctly reconstruct the current signal. 2.Sub-harmonic Oscillation: Current mode control could be unstable as duty ratio larger than 50%. A compensation ramp is necessary to fix the issue, and this could introduce complication as well. 3.Signal to Noise Ratio The infamous problem in almost every current mode supply is noise on the current sense signal. In many power supplies there are simply not enough signals to control the converter smoothly over the full range of operation. Solution includes filtering the current wave form in different places for example in buck it would be the output side or leading edge blanking where the most noise in the initial part of the signal is ignored. Even with these approaches, which all increase circuitry complications, current mode control could be not working.	1.Easy Compensation: With voltage mode, the sharp phase drop requires a type III compensator to stabilize the system. Current mode control looks like a single pole system, and a type II compensator is adequate. 2.RHP Zero Converters: In a converter where the crossover frequency is restricted by the presence of an RHP zero. Although current mode control could not eliminate RHP zero, it makes the compensation easier. 3 CCM and DCM Operation When moving from CCM mode to DCM mode, the characteristics with voltage mode control are very different. It is difficult to design a compensator with voltage mode that provides good performance in the two regions. 4 Line Rejection Closing the current loop gives a lot of attenuation of noise. For buck, it can even be nulled under some specific conditions with proper compensation ramp.

As the pros mentioned in Table 2, the technique how to accurately sense the inductor current or switch current, and the proper slope compensation to prevent sub-harmonic oscillation instability are two major disadvantages for current mode control. The followings are to take a look at the techniques of current sensing and slope compensation.

1.4.3 Slope Compensation

Sub-harmonic oscillation is a well-known problem for current-mode switching converters when the duty ratio larger than 0.5 as shown in Figure 10. To avoid sub-harmonic oscillation, the slope compensation ramp is required to suppress the issue on as illustrated in Figure 10.[3]

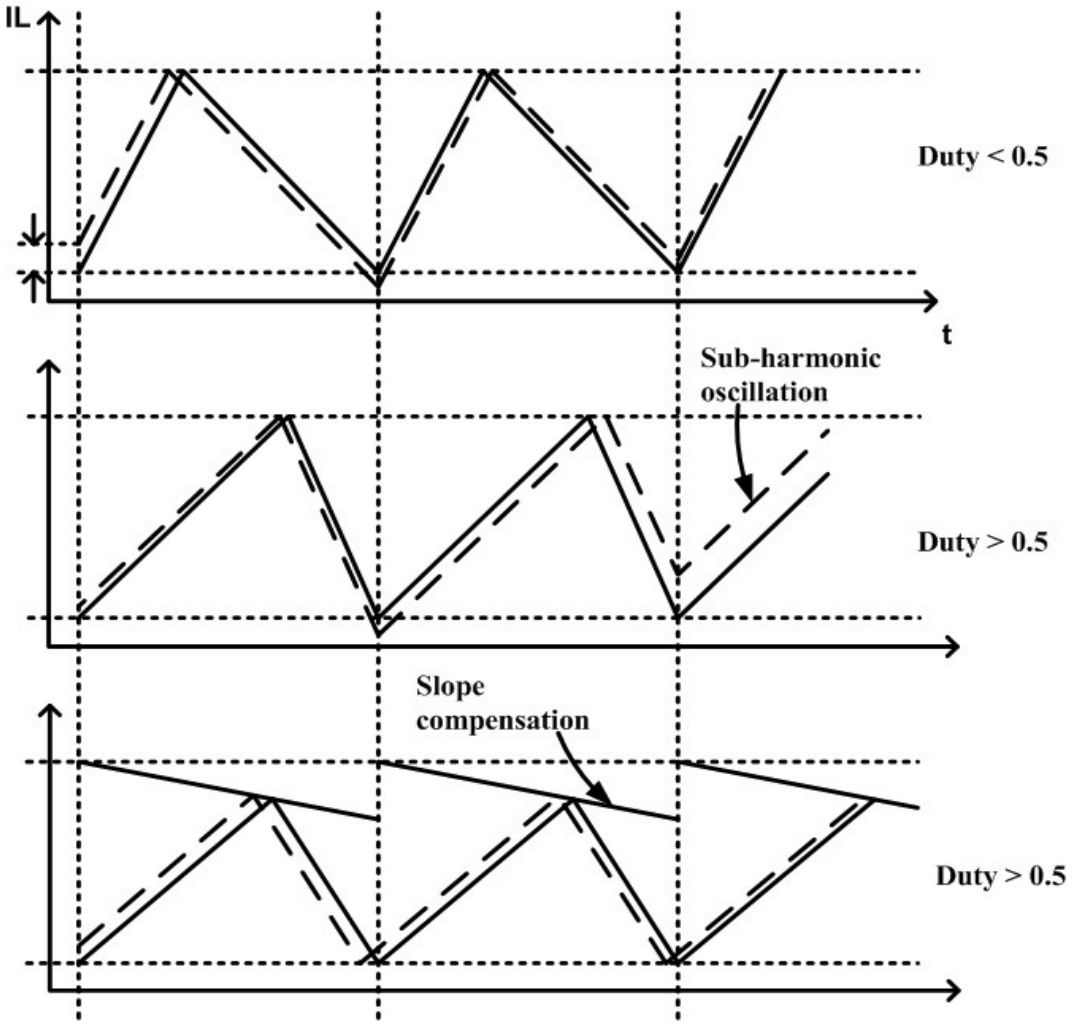


Figure 10 Sub-harmonic oscillation and slope compensation

1.4.4 Current Sensing

In Table 2, it also reveals that current sensing scheme is also playing a very key role for the converter with current mode control to precisely reconstruct the current signal of inductor. As shown in Table 3, it provides the reference of current sensing techniques for their advantages and the main concerns.

Table 3 Overview of current sensing techniques [13]

#	Technique	Advantage	Main Concern
1	External sensing resistor	High accuracy and common practice	High power dissipation as all the inductor current or drain current of the power transistor must pass through the sensing resistor. Not only suffer from low efficiency, but also require extra off-chip known resistor
2	Sensor less integrator	Claimed could be Lose-less	Complexity of design with different topologies, and The exact value of the inductor should also be known. Moreover, the accuracy of this current sensing scheme is influenced by different factors such as the time-constant value tolerance of the filter and manufacturing tolerances on the inductor.
3	On-resistance of power switch	Lose-less	Low accuracy due to that it is also sensed by a resistor, and the on-resistance of switch varies with temperature and different processes and thus affects accuracy.
4	Internal current sensing	Integrated on-chip	Increased the complication of circuit design for accuracy and variation from temperature, process and switch frequency.

1.5 Advantages of On-Chip Compensation (OCC)

As it is well known that the higher level of integration the better performance because it resulted from the reduction of parasitic component such as bonding wires, connections, or package. Unfortunately, off-chip inductors and capacitors take up significant area on PCBs, increase production cost, and make it difficult for system-on-chip (SoC) applications. To reduce the side effects of parasitic elements from wiring and power loss on them, it takes advantages to integrate the circuits on chip as many as we could. High integration is necessary to improve performance and have smaller footprint area. [15]

In Figure 11, the conventional compensation network contains a resistor and capacitors. After the integration of these passive components, pin out number can be minimized and the chip only needs the output filter which contains an inductor and a capacitor as shown in Figure 12. If the integration of the output filter into the chip is needed, the technique of system-in-package (SIP) can be used to implement the large off-chip output filter. For low cost and high integration, on-chip compensation techniques to implement a buck converter with minimized external pins and high performance are presented in the following chapters.

The difficulty of high integration in the design of dc-dc converters is due to the large off-chip capacitors for compensation. The compensator such as PI and PID controllers must generate poles and zeros to counteract the dominant pole or double poles and form a new suitable dominant pole for the desired bandwidth. However, large-valued capacitors needed for compensation would occupy a lot of space of layout if they are on-chip. By means of on-chip compensation techniques, zeros are generated by circuitry or large equivalent capacitance multiplied by current mode Miller compensation or time mode Miller compensation. It means that the minimization of capacitor size can alleviate the tradeoff between cost and performance to maximize the profit and cost down.

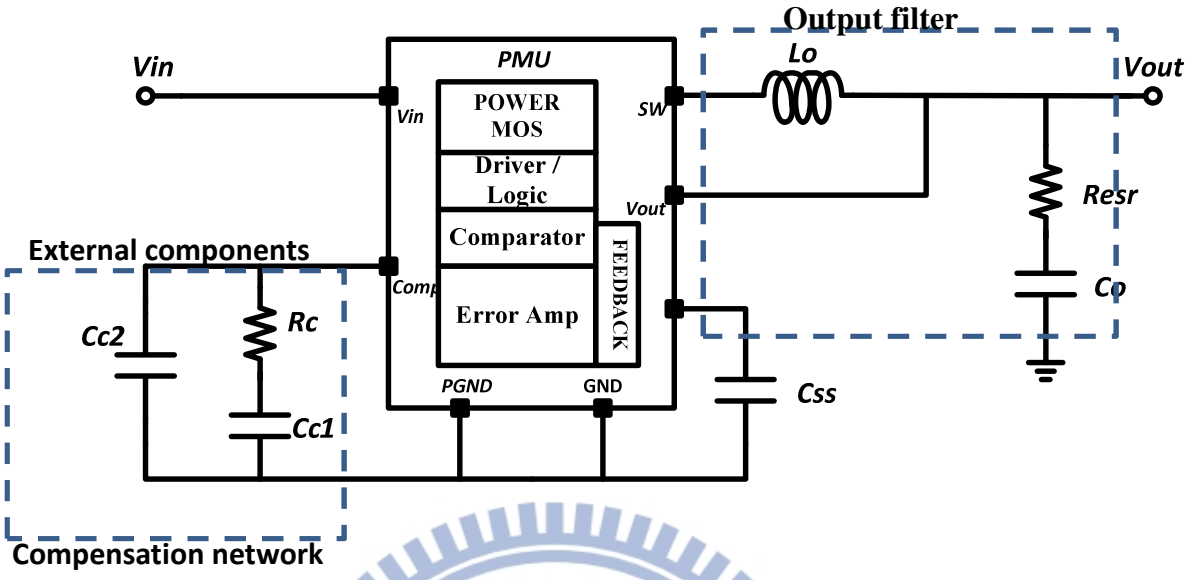


Figure 11 Conventional compensation network of power chip

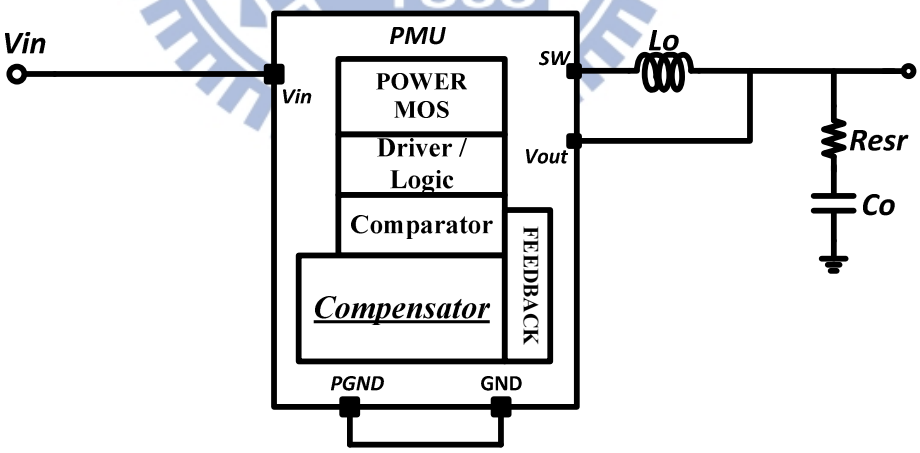


Figure 12 Lower pin counts after compensation network integrated on chip.[16]

1.6 Thesis Organization

This work is introducing the fundamentals of DC-DC converters in Chapter 1 which includes the basic converter topologies, control alternatives, compensation schemes, and the advantages of on-chip compensations. The on-chip compensation techniques such as PID on-chip compensation integrated for voltage mode buck converter, and current mode Miller (CMM) on-chip compensation as well as time mode Miller (TMM) on-chip compensation for current mode buck converter are playing the key roles in the Chapter 2 and Chapter 3. In Chapter 4, the circuit implementations and simulation results are therefore focused on the main building blocks used by CMM and TMM on-chip compensation techniques, following with the circuit level simulations to validate their characteristics and performances. The conclusions and future works are finally put in Chapter 5.

Chapter 2

OCC for Voltage Mode Buck Converter

This chapter focuses on compensation techniques for DC-DC buck converter with voltage mode control. First, generic type III compensator is reviewed in details including its transfer function, circuit schematics, frequency response, and practical design procedure etc. Contrary to type III off-chip compensation due to that it takes the large capacitors to position the desired zero as we would see in the next section, an integrated PID OCC in DC-DC buck converter is then the highlight of this chapter.

2.1 Type III Off-Chip Compensation

The Figure 13 shows a generic Type III compensation, its transfer function and asymptotic Bode plot. The Type III network helps to shape the profile of the gain with respect to frequency and also gives a 180° boost to the phase. This boost is necessary to counteract the effects of an under damped resonance of the output filter at the double pole.[22]

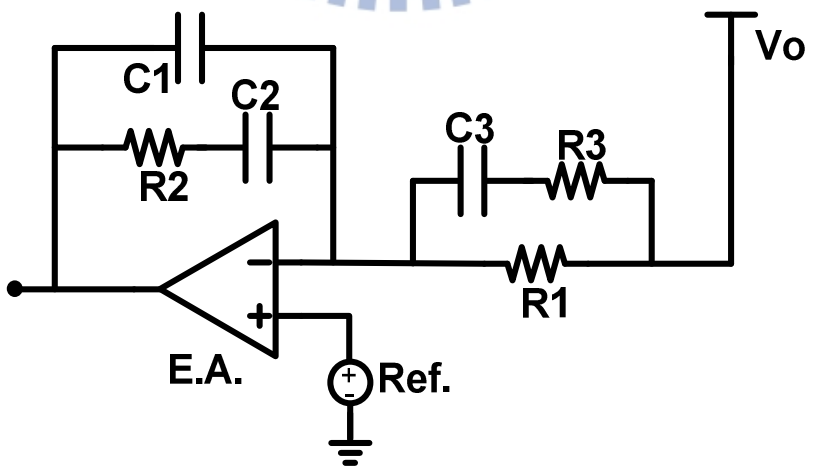


Figure 13 Generic Type III compensation

Type III Compensation Transfer Function,

$$GAIN_{TypeIII} = \frac{R1+R3}{R1*R3*C1}\frac{(s+\frac{1}{R2*C2})(s+\frac{1}{(R1+R3)*C3})}{s\left(s+\frac{C1+C2}{R2*C1*C2}\right)*(s+\frac{1}{R3*C3})} \quad (1)$$

where

$$Zero1 = \frac{1}{R2*C2},$$

$$Zero2 = \frac{1}{(R1+R3)C3}$$

$$Pole1 = \frac{1}{R2\left(\frac{C1C2}{C1+C2}\right)},$$

$$Pole2 = \frac{1}{R3C3}$$

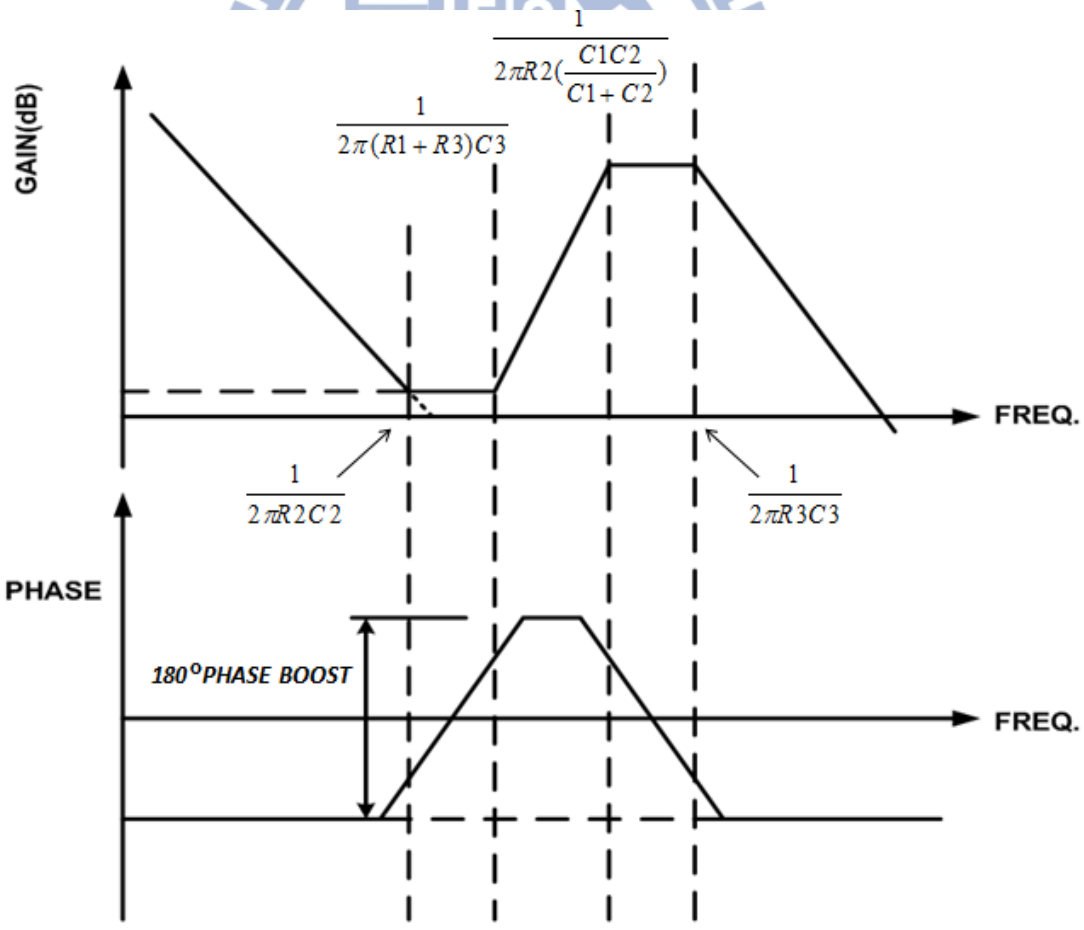


Figure 14 Generic Type III compensation [2]

2.1.1 Closed Loop with Type III Compensation

In Figure 15 shows a closed loop buck converter with Type III compensation network. Figure 16 depicts the asymptotic Bode gain plot for the close system with Type III compensation. For the transfer function of the compensated system, the gain and phase equation are also listed in the followings.

As with the Type III compensation network, it is recommended that the actual gain and phase plots be generated through the use of a commercially available analytical software package that has the capability to plot. In section 2.2 the general procedure of design flow is briefly described and demonstrated.[2][9]

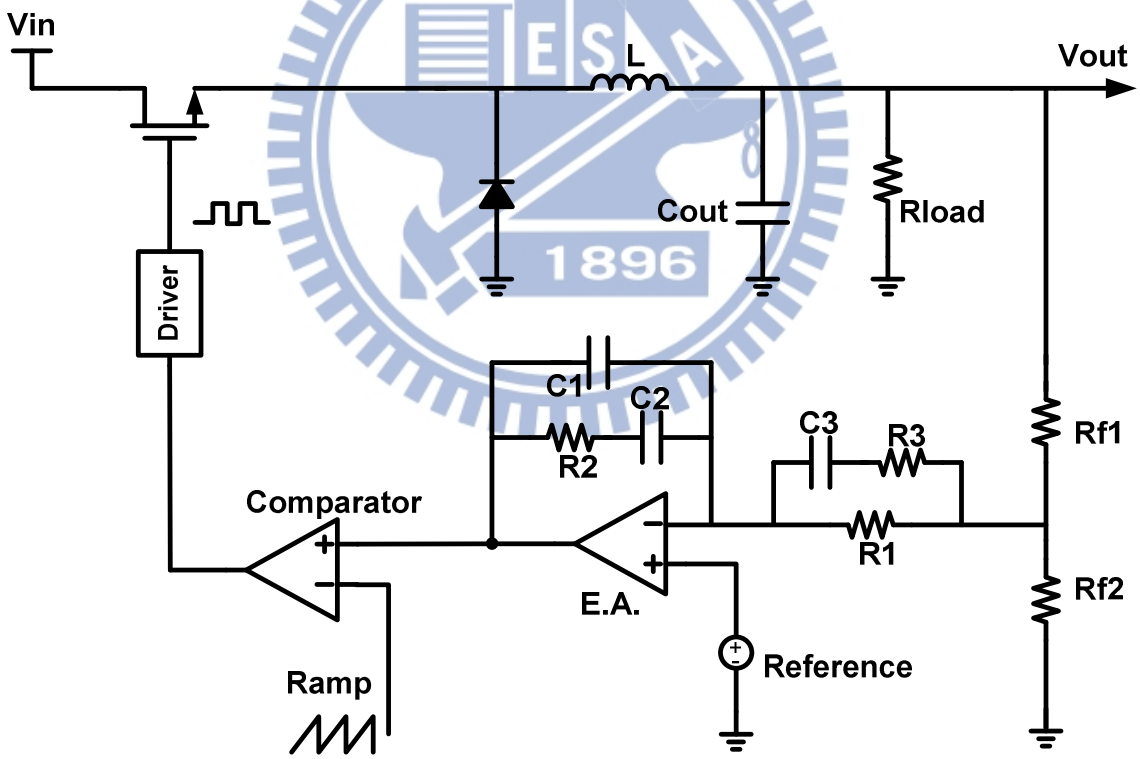


Figure 15 Closed loop buck converter with Type III compensation

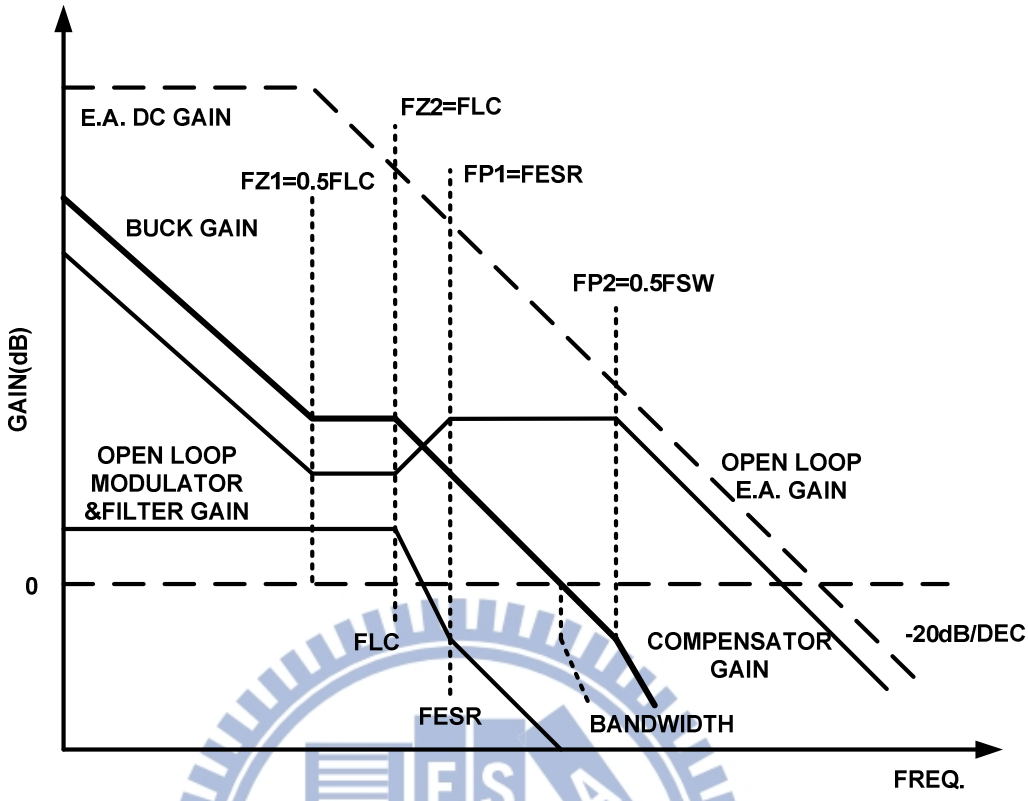


Figure 16 Buck converter with Type III compensation Bode plots

Buck with Type III compensation transfer functions are listed below,

$GAIN_{dB}(T) = GAIN_{MODULATOR} + GAIN_{FILTER} + GAIN_{TYPEIII}$

$\text{PHASE(T)} = PHASE_{MODULATOR} + PHASE_{FILTER} + PHASE_{TYPEIII}$

where: $GAIN_{MODULATOR} = 20\log\left(\frac{V_{IN}}{\Delta V_{OSC}}\right)$

$GAIN_{FILTER} = 10\log[1 + (\omega * ESR * C_o)^2] - 10\log[(1 - \omega^2 * L_O C_O)^2 + (\omega(ESR + DCR)^2]$

$GAIN_{TYPEIII} = 10\log[1 + (\omega R2C2)^2 - 20\log[\omega R1(C1 + C2)] - 10\log[1 + (\omega R2(\frac{C1C2}{C1 + C2}))^2$

$PHASE_{FILTER} = tan^{-1}[\omega * ESR * C_O] + tan^{-1}[\frac{\omega ESR + DCR * C_O}{\omega^2 L_O C_O^{-1}}]$

$PHASE_{TYPEIII} = -90° + tan^{-1}[\omega * R2 * C2] - tan^{-1}\left[\omega R2\frac{C1C2}{C1 + C2}\right] + tan^{-1}[\omega(R1 + R3)C3]$

$- tan^{-1}(\omega R3C3)$

2.1.2 Compensation Design Procedure

The systematic procedure will help calculate the poles and zeroes, and from those the component values to position the poles and zeroes for Type III compensation network. .

1. Choose a value for R1 usually between 2k and 5kohm
2. Pick a gain (R2/R1) that will shift open loop gain up to give the desired bandwidth. This will allow the 0dB crossover to occur in the frequency range where the Type III network has its second flat gain. The following equation will do calculation for an R2 that accomplish this given the system parameters and a chosen R1.

$$\mathrm{R2} = \frac{DBW\ \Delta V_{OSC}}{F_{LC}\ V_{in}} R1$$

3. Calculate C2 by placing the zero at 50% of the output filter double pole frequency.

$$\mathrm{C2} = \frac{1}{\pi * R2 * F_{LC}}$$

4. Calculate C1 by placing the first pole at the ESR zero frequency

$$\mathrm{C1} = \frac{C2}{2\pi R2 C2 F_{ESR} - 1}$$

5. Set the second pole at half switching frequency and also set the second zero at output filter double pole. This combination will yield the following component calculations.

$$\mathrm{R3} = \frac{R1}{\frac{F_{SW}}{2F_{LC}} - 1}$$

$$\mathrm{C3} = \frac{1}{\pi * R3 * F_{SW}}$$

The compensation gain must be compared to the open loop gain of the error amplifier. The compensation gain should not exceed the error amplifier open loop gain because this is the limiting factor of the compensation. Once the gain and phase plots are generated the system may need to be changed after it is analyzed. Adjust the poles and/or zeroes in order to shape the gain profile and make sure that the phase margin is larger than 45°or in between 45° to 60°.[9]

2.2 PID On-Chip Compensation Technique

This section presents a wide-band compensation that could be implemented by an on-chip integrated PID compensator for buck converter with voltage mode control. The details of the schematics and loop gain analysis will be discussed in the following sections.

The proportional-integral (PI) controller that is sufficient when the process dynamics is essentially first-order, proportional derivative (PD) controller and proportional integral derivative (PID) controller that has the advantages of PI and PD control are widely used in many industrial control systems. The traditional implementation of PID controller by OP-amps is as shown in Figure 17 and the transfer function of a general analog PID controller can be written as follows, [24]

$$\mathrm{T(s)} = \frac{V_o(s)}{V_i(s)} = K_P + \frac{K_I}{s} + sK_D$$

$$where\ \ K_P\ is\ the\ proportional\ gain,$$

$$K_I\ is\ the\ integral\ gain,$$

$$and\ K_D\ is\ the\ derivative\ gain$$

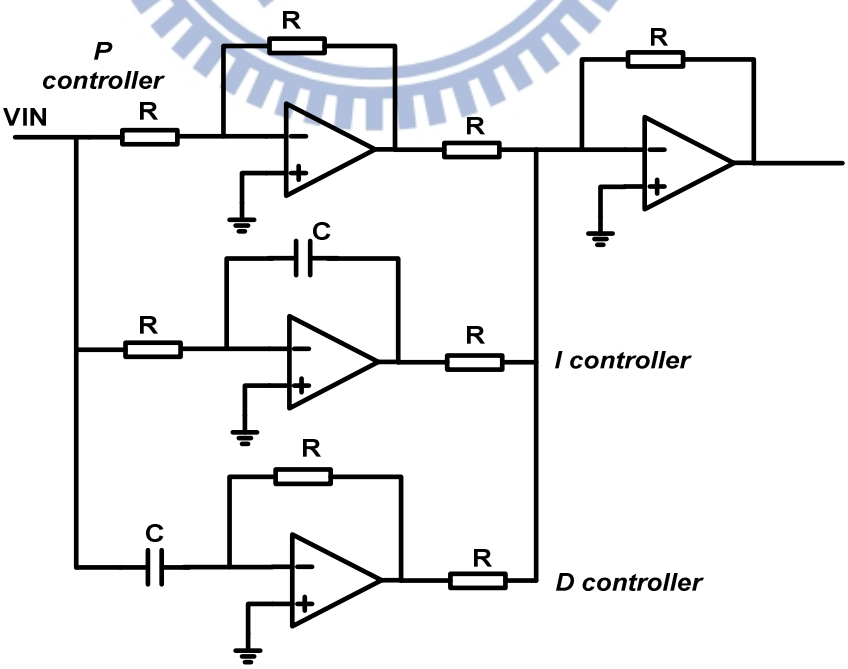


Figure 17. Traditional PID controller

Figure 18 shows block diagram of buck converter with PID compensation. The architecture of PID compensation will be presented in the next section. In addition to the voltage feedback, the current of inductor is sensed and summated with error amplifier as a part of compensator. It looks like there are two feedback paths compared to current control, but it is still a voltage mode control. [20] The current sensing network is also shown below.

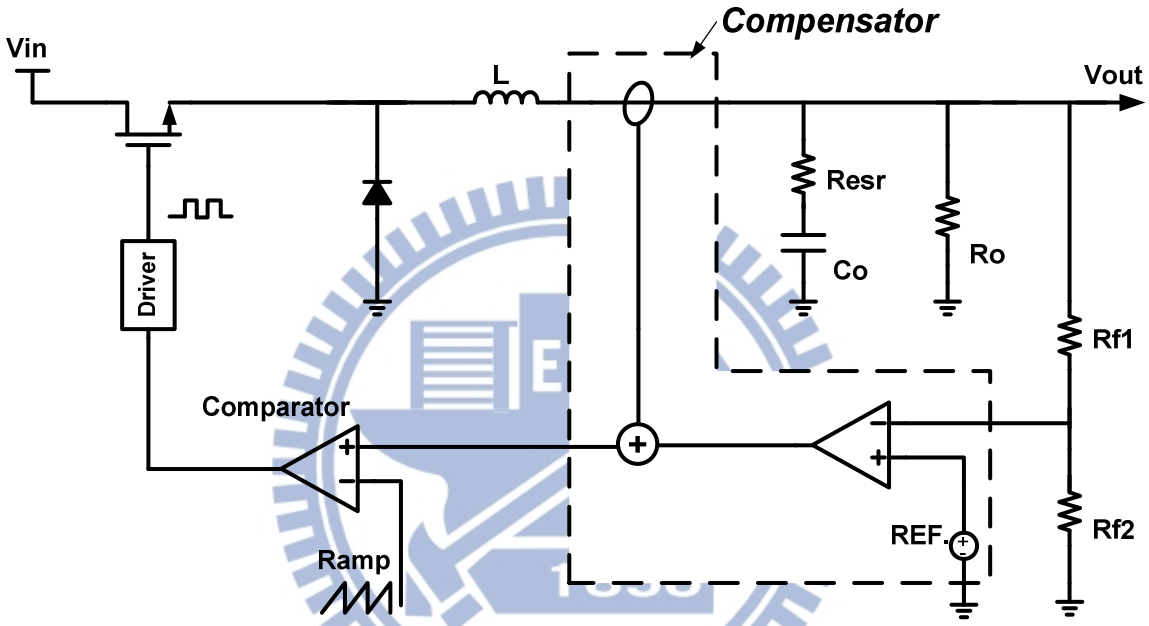


Figure 18 Block diagram of Buck converter with PID compensation

2.2.1 PID OCC Architecture

The buck converter as shown in the Figure 19 consists of a PID controller that is designed for fully integrated on the chip. The PID controller is including a differential controller, an integral controller and the proportional controller. The overall architecture is similar to the PID controller mentioned in section 2.2.

To meet the fast load transient response and achieve a bandwidth of 200 kHz with phase margin 60°, it needs PID controller for voltage mode control instead of using either dominant pole compensation or PI compensation. The P (proportional)-controller is composed of only

Operational Transconductance Amplifier circuits (OTA2 and OTA3) to avoid large resistors. An error amplifier (OTA1), known as I (integral)-controller, is designed with additional compensation capacitor Cz. The output voltage is differentiated by D controller using the ripple current of the inductor (I_{L_ac}) detected by integrating the voltage difference across the voltage of the inductor (V_L), which is given as

$$I_{L\_ac} = \frac{1}{L}\int V_L dt$$

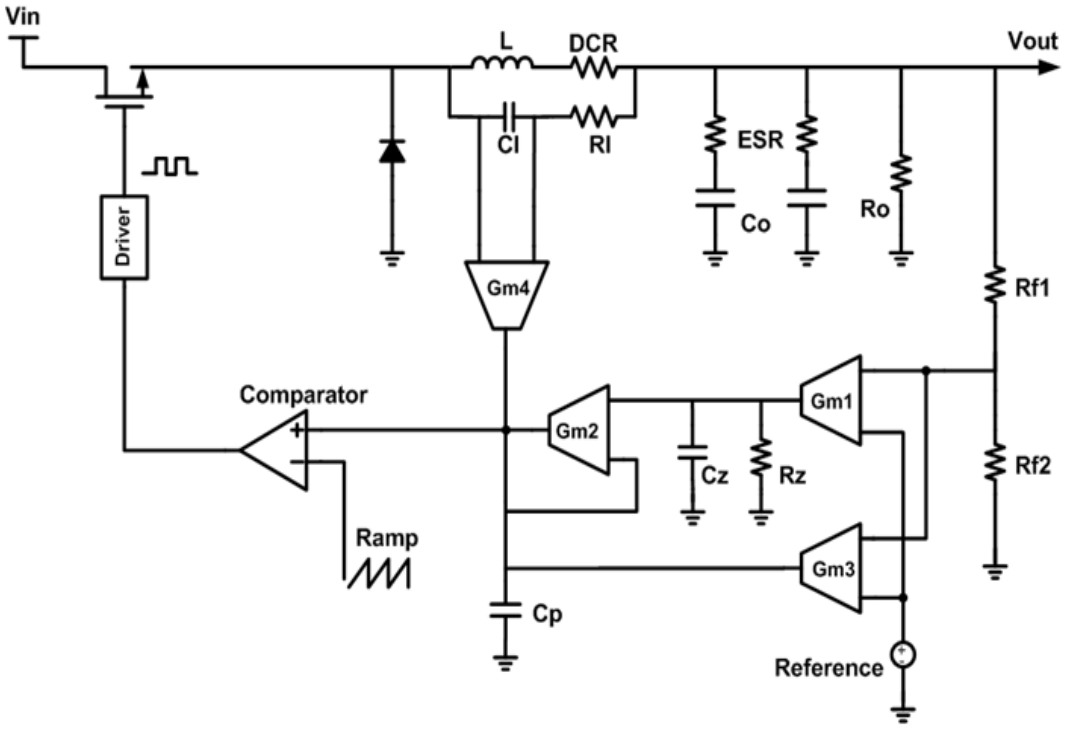


Figure 19 Buck converter with on-chip PID compensation

Therefore, the RC-series is connected to the inductor terminals. Then, the voltage across the capacitor (Cl) is detected by OTA4. This technique is an effective method for obtaining AC ripple current information. Current sensing network that senses AC ripple inductor current with passive devices only including one capacitor and one resistor as shown in Figure 20, and the correlation of sensed voltage and network components such as Cl and Rl is also attached below,

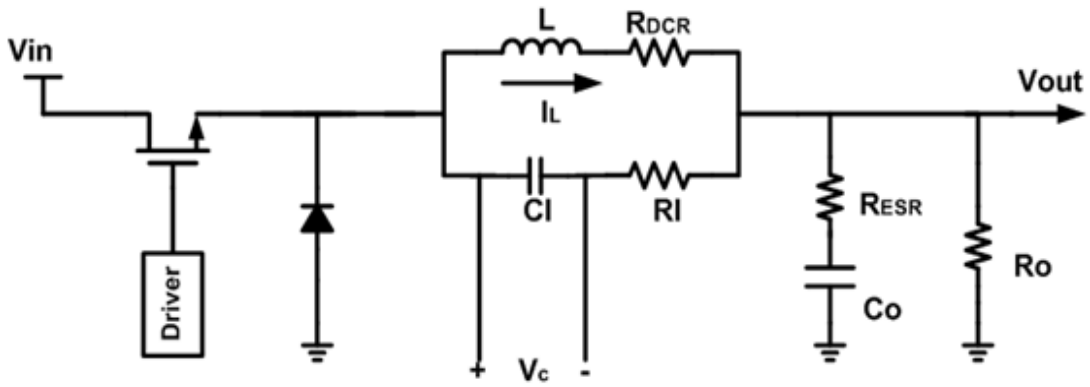


Figure 20 Current sensing network

As shown Figure 20 that is a RC low-pass filter to sense inductor current and the voltage across the inductor L is

$$v_L = (R_{DCR} + sL)i_L \ ,$$

And the voltage across capacitor Cl is

$$v_C = \frac{\frac{1}{sCl}}{Rl + \frac{1}{sCl}} v_L = \frac{1}{1 + sClRl} v_L = \frac{R_{DCR}(1 + \frac{sL}{R_{DCR}})}{1 + sClRl} i_L$$

$$\text{If } \frac{L}{R_{DCR}} = ClRl,$$

$$Then\ v_C = R_{DCR} * i_L$$

2.2.2 Loop Gain Analysis

The transfer function of the total loop gain of buck converter with PID compensator is derived in the following equations T(s), [20]

$$T(s) = -\frac{1}{V_M}\frac{V_{out}}{D}\frac{1}{\left(\frac{s}{\omega_0}\right)^2 + \left(\frac{s}{Q_0\omega_0}\right) + 1}\frac{R_{f1}}{R_{f1} + R_{f2}}(1 + sC_oR_{ESR})G_{CC}(s)\frac{1}{sC_p\frac{1}{G_{m2}} + 1}$$

$$\text{where } \ Q_0 = R_0\sqrt{\frac{C_o}{L}} \ , \ \ \omega_o = \frac{1}{\sqrt{LC_o}}$$

V_M *is the PWM gain,* D *is duty ratio,*

R_{ESR} *is the equivalent series resistance of output capacitor*

C_P *represents the parasitic capacitance*

The transfer function of PID compensation Gcc(s) as shown in fig

$$G_{CC}(\mathrm{s}) = \frac{G_{m3}}{G_{m2}} + G_{m1}R_{O1}\left(\frac{1}{sC_ZR_{O1}+1}\right) + \frac{G_{m4}}{G_{m2}}sL\left(\frac{sC_OR_O+1}{R_O}\right)\left(\frac{1}{sClRl+1}\right)\left(\frac{1}{1+sC_OR_{ESR}}\right)$$

$$where \quad \frac{G_{m3}}{G_{m2}} \quad P\ controller\ gain\ , \qquad G_{m1}R_{O1}\left(\frac{1}{sC_ZR_{O1}+1}\right)\ I\ controller\ gain$$

$$\frac{G_{m4}}{G_{m2}}sL\left(\frac{sC_OR_O+1}{R_O}\right)\left(\frac{1}{sClRl+1}\right)\left(\frac{1}{1+sC_OR_{ESR}}\right)\ D\ controller\ gain$$

$$Thus, transfer\ function\ of\ PID\ rewritten\ as \quad G_{CC}(\mathrm{s}) = K_P + \frac{K_I}{s} + sK_D$$

There are two following poles: one which is generated by the inductor current sensor, Rl and Cl, and the other which is generated by Co and RESR. Since 1/($Co \cdot R_{ESR}$) is a zero in terms of the control-to-output transfer function, it is canceled out in the total loop transfer function. The compensator contains two zeros as shown in fig. Zero1 is at the point where the magnitude line of I-control meets that of P-control. The zero1 location is calculated in the following equations,

$$\frac{\mathrm{G_{m3}}}{\mathrm{G_{m2}}} = \mathrm{G_{m1}R_{O1}}\left(\frac{1}{\mathrm{sC_ZR_{O1}}+1}\right)$$

$$\mathrm{Zero1} = \frac{G_{m1}}{C_Z} * \frac{G_{m2}}{G_{m3}}$$

The other zero, Zero2, exists at the point where the magnitude line of P-control meets that of D-control. Zero2 position will be known by solving the equations as shown below,

$$\frac{G_{m3}}{G_{m2}} = \frac{G_{m4}}{G_{m2}}sL\left(\frac{sC_OR_O+1}{R_O}\right)\left(\frac{1}{sClRl+1}\right)$$

$$\mathrm{Zero2} = \frac{G_{m3}}{G_{m4}} * \frac{ClRl}{LC_O}$$

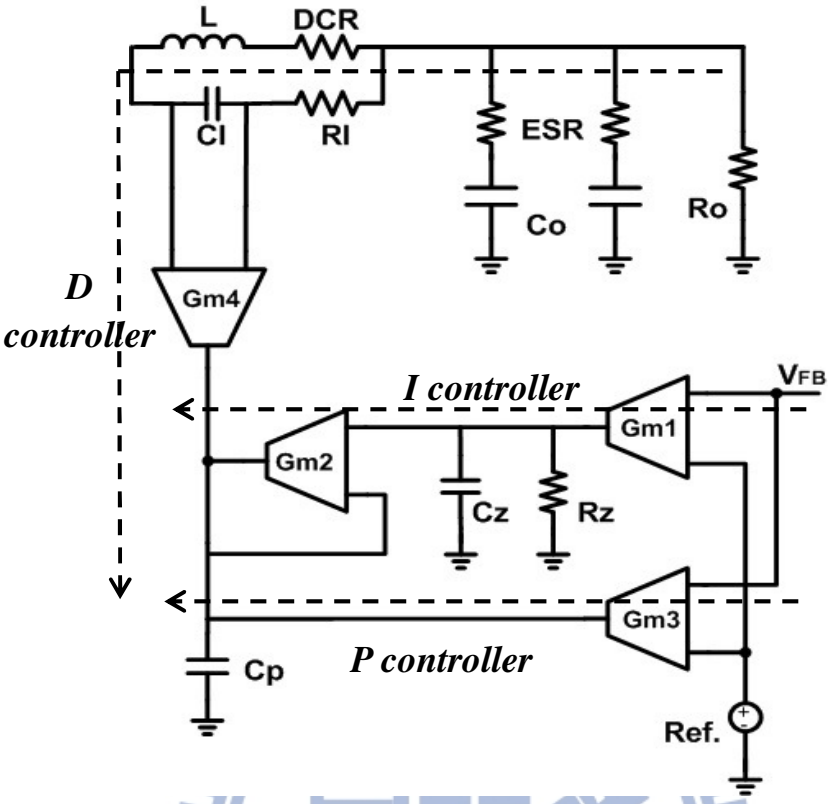


Figure 21 PID OCC schematics

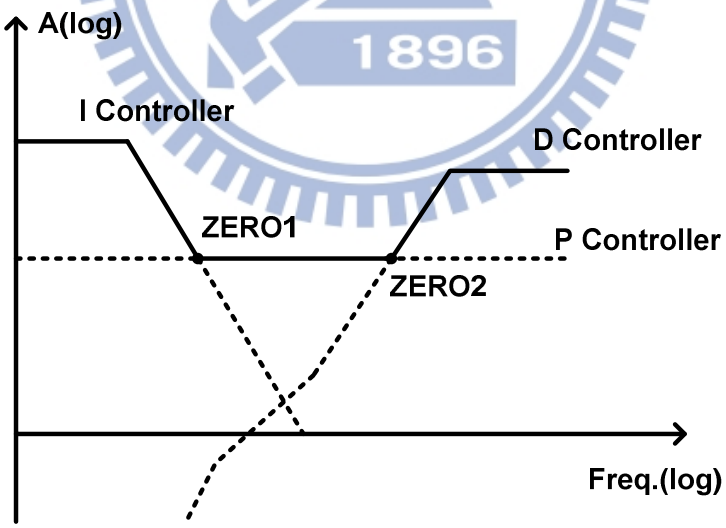


Figure 22 Bode plot of PID OCC

2.3 PSIM Implementation

2.3.1 Compensation Worksheets

As shown in Table 4 and Table 5, the worksheets of Type III off-chip compensation and PID OCC are to facilitate the calculations of poles and zeros, and are very helpful for the parameters tuning as running the simulations.

Table 4 Type III off-chip compensation worksheet

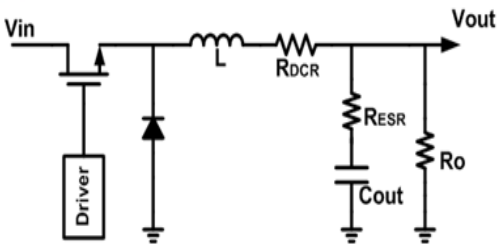
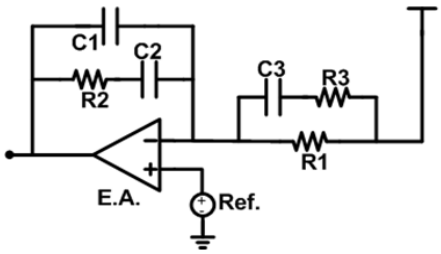
Converter Parameters Input Voltage: VIN 3.3V Output Voltage: VOUT 2.5V Output Current: 500mA Switching Frequency: F_{SW} 1MHz Total Output Capacitance: C_{OUT} 44µF Total ESR: R_{ESR} 8mΩ Inductor: L 2.2µH Inductor DCR: DCR 18mΩ Control scheme: Voltage mode Compensation : Off-chip Type III Reference Voltage: V_{REF} 1V Error Amp DC Gain 80dB Desired Bandwidth: DBW 200kHz Phase Margin: 60° R1= 7 kΩ R2= 70 kΩ R3= 100 Ω C1= 1 pF C2= 400 pF C3= 600 pF Zero1= 5.7 kHz Zero2= 37.4 kHz Pole1= 23 MHz Pole2= 2.65 MHz	Buck converter  Type III compensator  Poles and zeros positions, $\text{Zero1} = \frac{1}{2\pi * \text{R2} * \text{C2}}$ $\text{Zero2} = \frac{1}{2\pi * (\text{R1} + \text{R3})\text{C3}}$ $\text{Pole1} = \frac{1}{2\pi * \text{R2}\left(\frac{\text{C1C2}}{\text{C1} + \text{C2}}\right)}$ $\text{Pole2} = \frac{1}{2\pi * \text{R3} * \text{C3}}$

Table 5 PID OCC worksheet

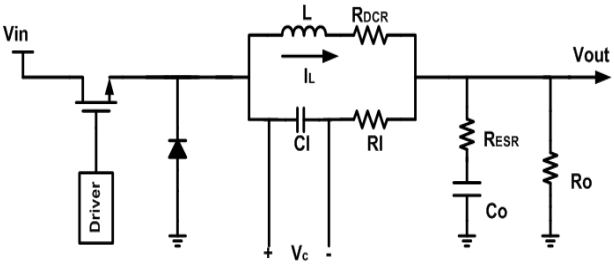
Converter Parameters

Input Voltage: VIN 3.6V
Output Voltage: VOUT 2.5V
Output Current: 500mA
Control scheme: Voltage mode
Compensation : On-chip PID
Reference Voltage: V_{REF} 1V
Switching Frequency: F_{SW} 1MHz
Total Output Capacitance: 44µF
C_{OUT} 44uF (22uF X2)
Total ESR: R_{ESR} 8mΩ
(16mohm // 16mohm)
Output Inductance: Lout 2.2uH
Inductor DCR: DCR 18m
Desired Bandwidth: DBW 200kHz(f_0)
Phase Margin: 60°

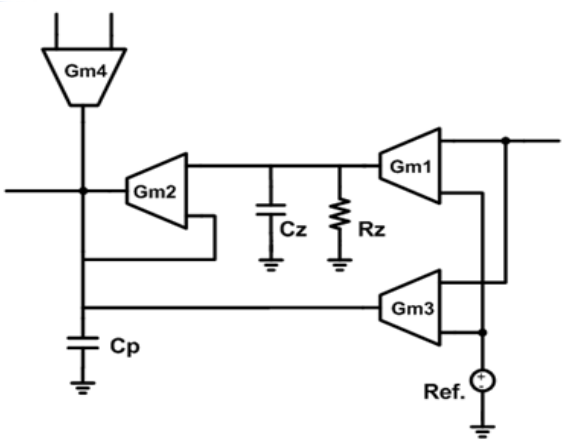
Gm1= 20µ A/V
Gm2= 20µ
Gm3= 400µ
Gm4= 20µ
Cz= 40 pF
Rz= 50 MΩ
Cl= 20 pF
Rl= 200 kΩ
Zero1= 4 kHz
Zero2= 820 kHz

ESR zero @ 452 kHz
LC double poles @ 16.2 kHz

Buck converter



PID OCC



Zeros positions

$$\text{Zero1} = \frac{G_{m1}}{C_Z} * \frac{G_{m2}}{G_{m3}}$$

$$\text{Zero2} = \frac{G_{m3}}{G_{m4}} * \frac{ClRl}{LC_O}$$

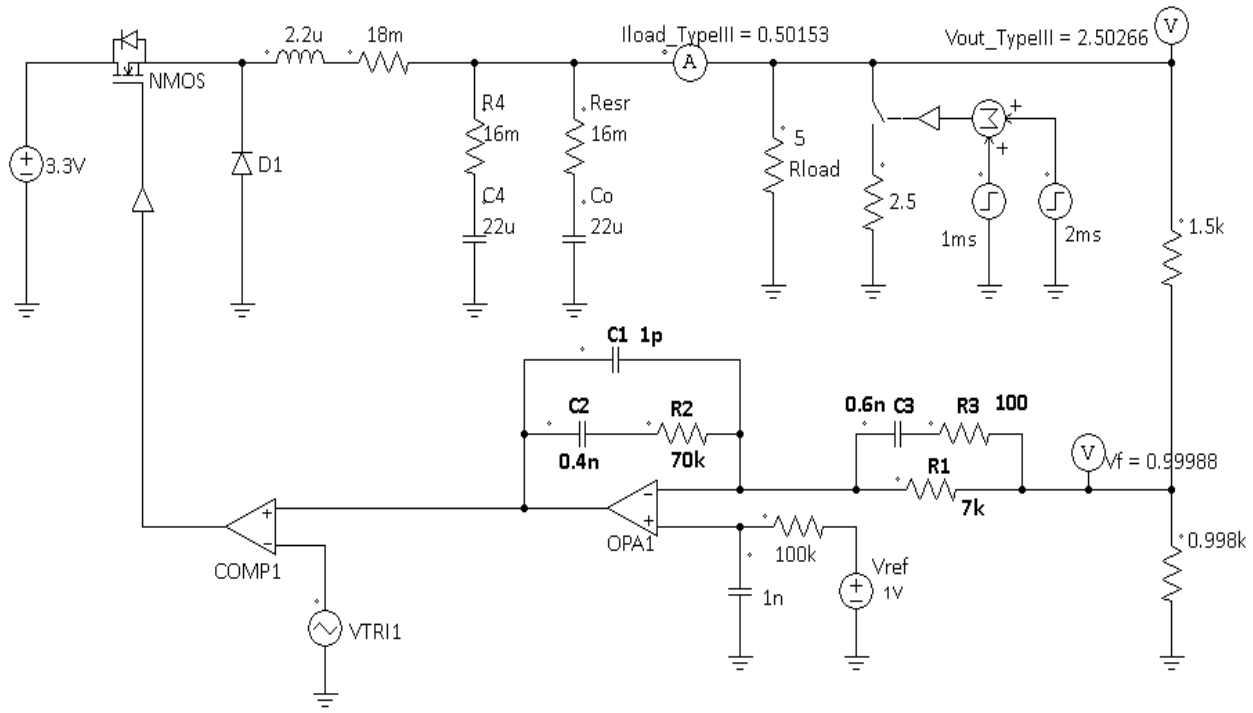


Figure 23 Buck converter with off-chip Type III compensation implemented by PSIM

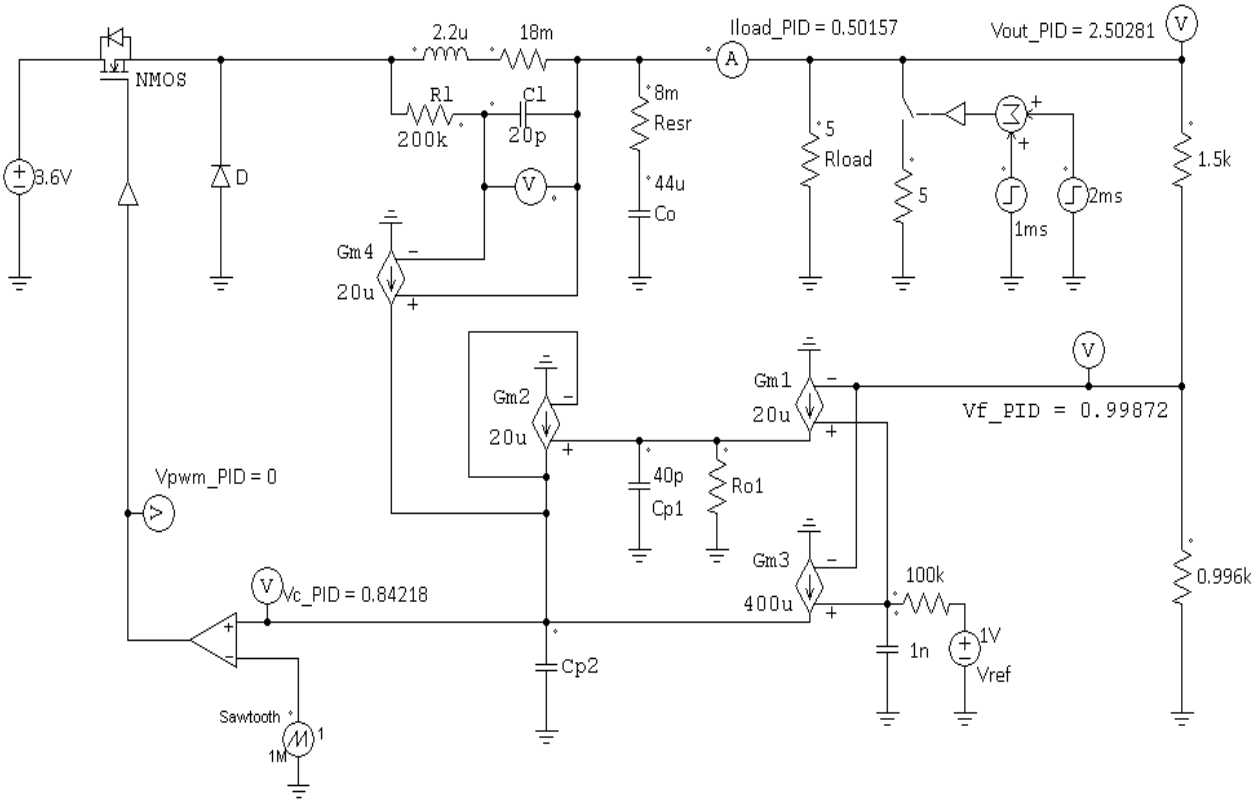


Figure 24 Buck converter with on-chip PID OCC implemented by PSIM

2.3.2 Frequency Response

As shown in Figure 23 and Figure 24 are buck converters with Type III and PID compensator implemented by PSIM. The total loop gain of buck converter with Type III is in the following Bode plots in Figure 25 showing that the system has phase margin 60°as cross over frequency is at 200 kHz.

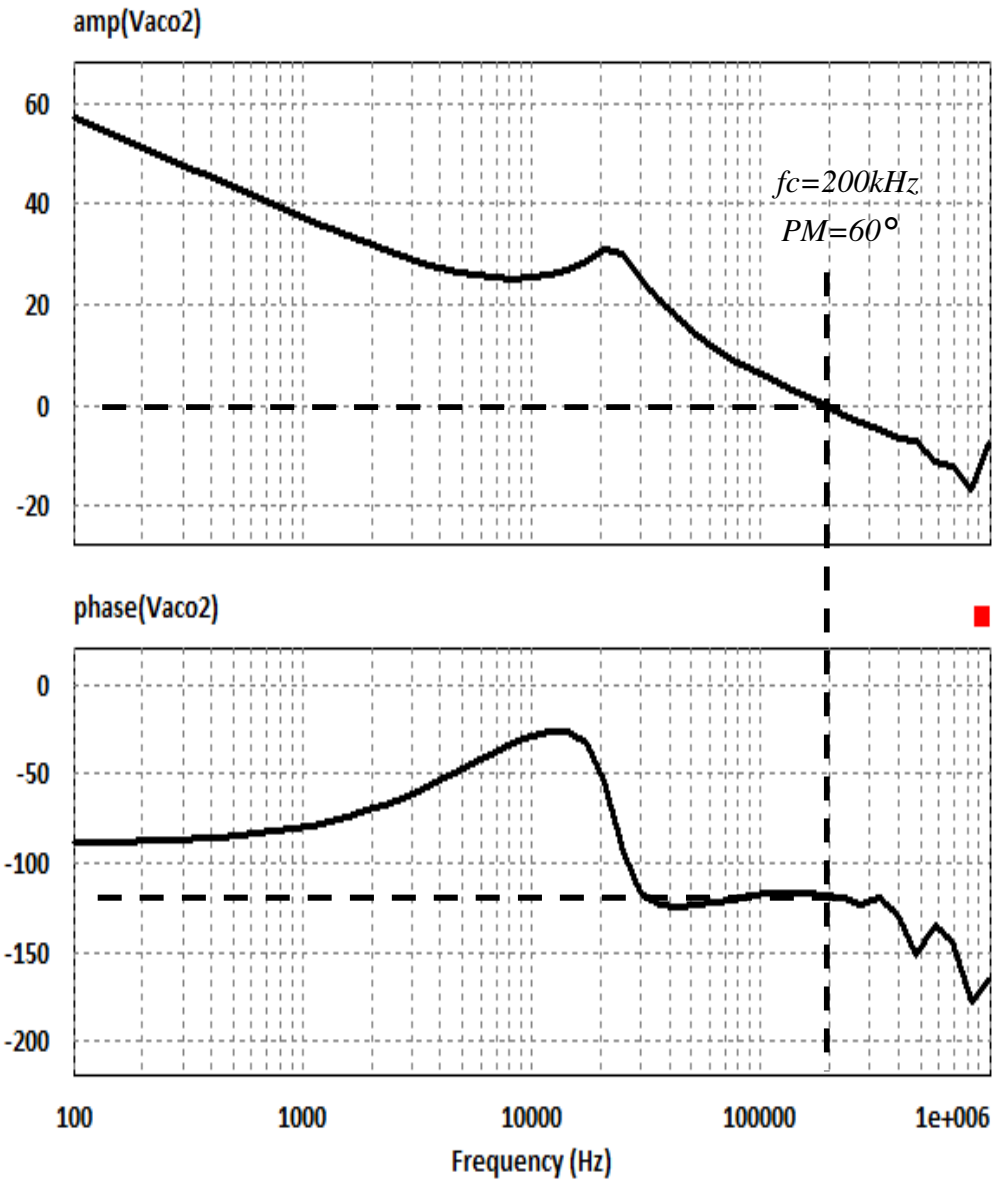


Figure 25 Buck converter with Type III Off-chip Compensation frequency response

The frequency response of buck with PID on-chip compensation is in Figure 26 for its loop gain amplitude and phase Bode plot. The phase margin and cross over frequency is the same as that of Type III off-chip compensator that requires the large compensation capacitors C2 equal to 400pF and C3 600pF to cope with the system stability.

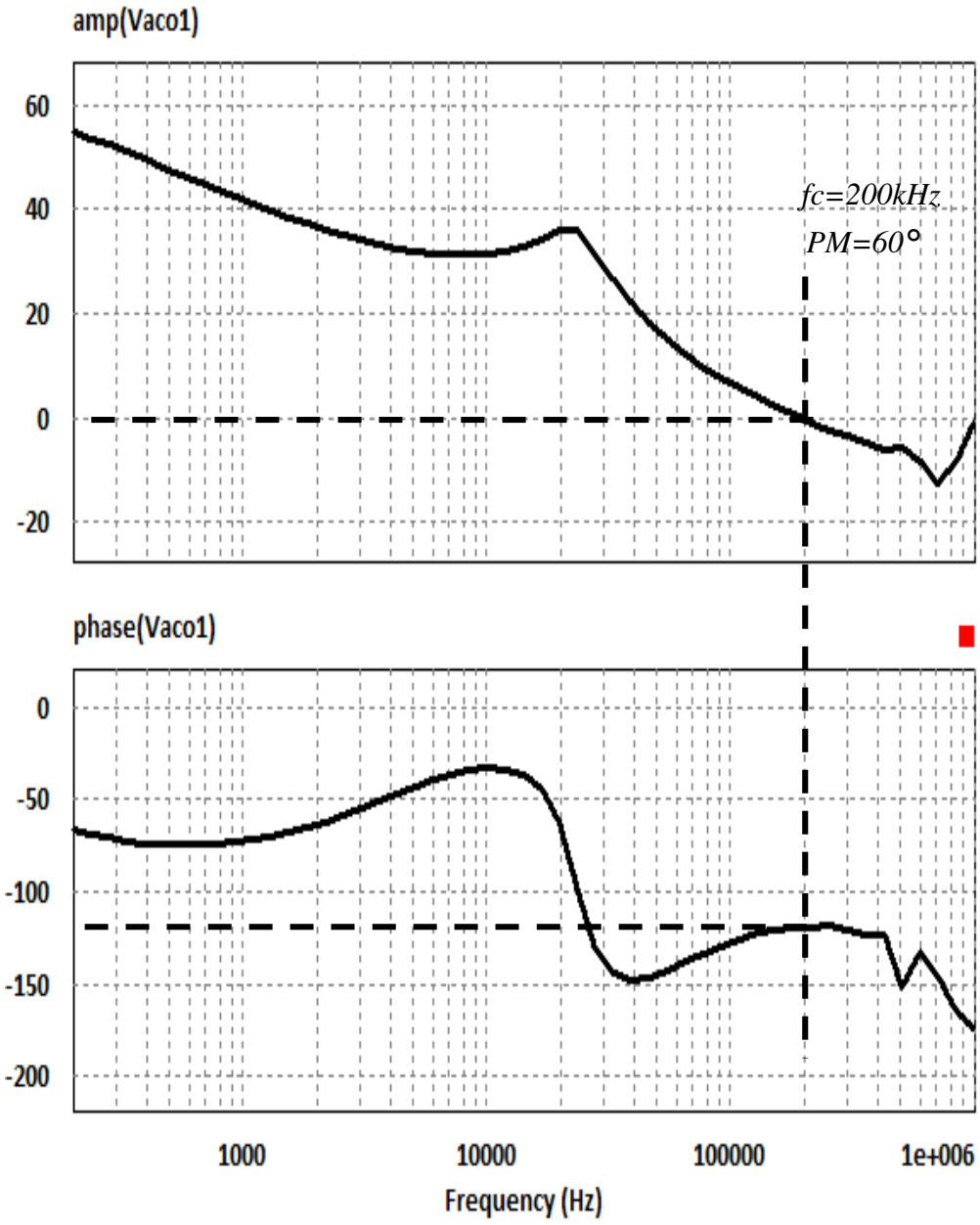
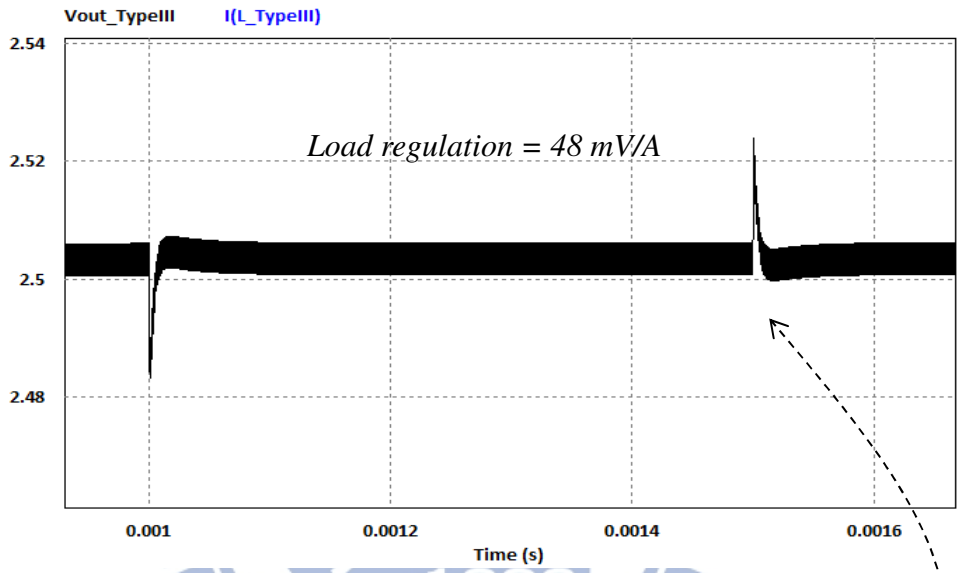


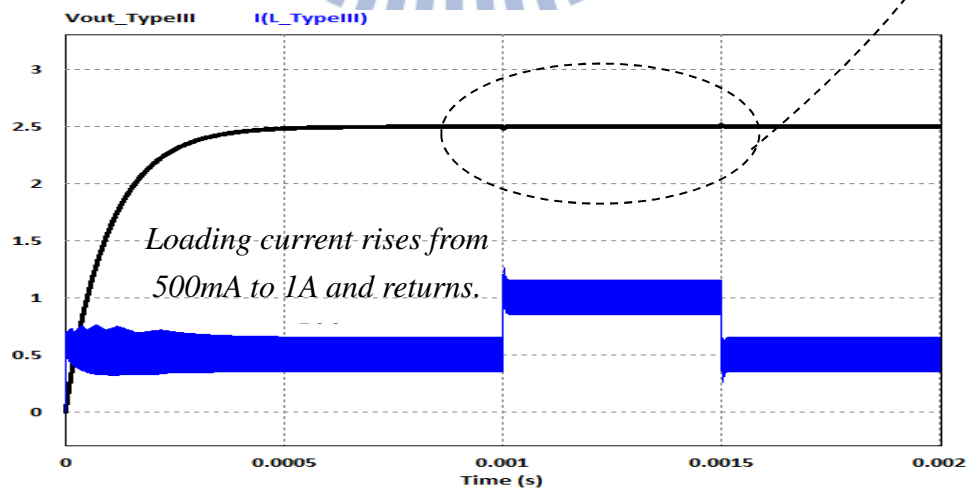
Figure 26 Buck converter with PID OCC frequency response

2.3.2 Load Regulation

The load regulation is defined as the percentage of steady state output voltage variation when the load current changes. The load regulation of buck with Type III compensator as loading current from 500mA to 1A within 1 μsec is 48 mV/A as shown in Figure 27 (a) and the enlarged view in (b), respectively.



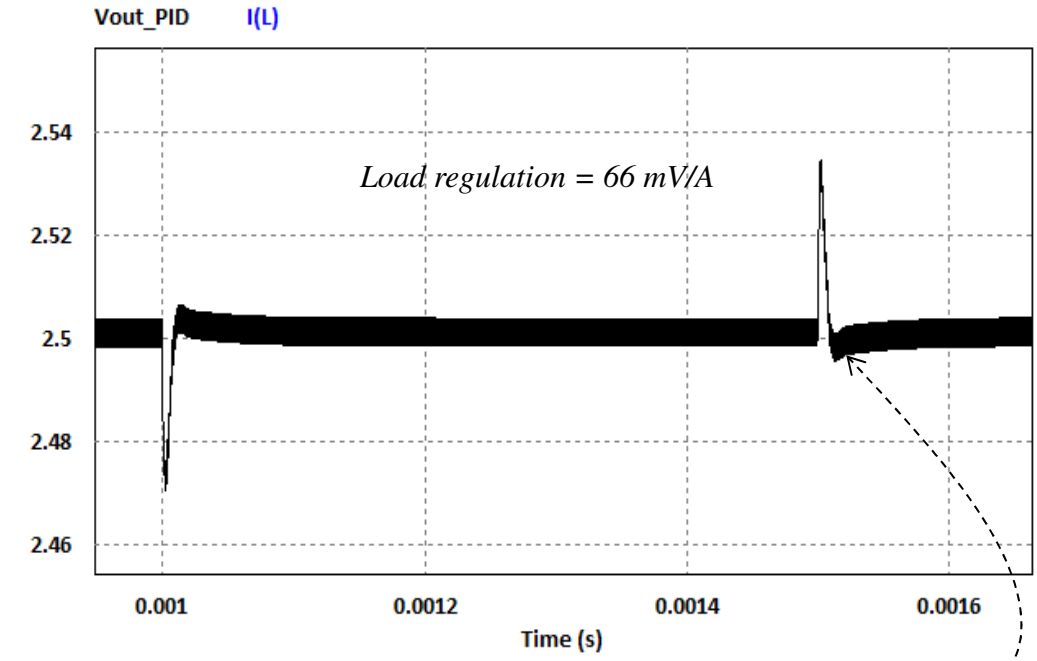
(a) Enlarged view of load regulation shown below



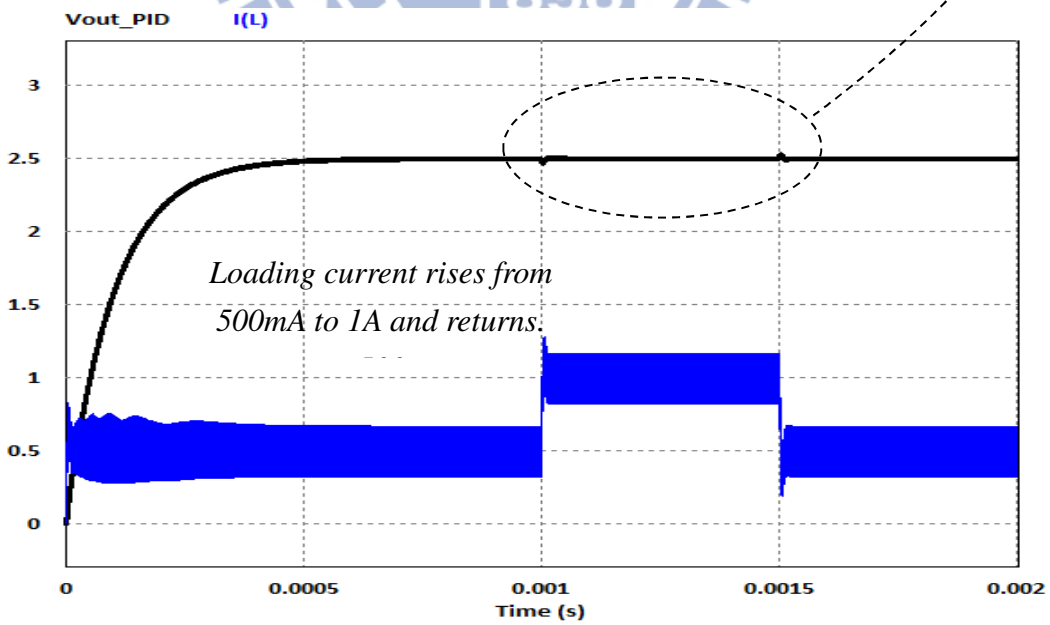
(b)

Figure 27 Load regulation of buck converter with Type III off-chip compensation

As shown in Figure 27 (a) and the enlarged view in (b) with the same condition loading current from 500mA to 1A within 1 μsec, the drop voltage is 33 mV and the load regulation of buck converter with PID compensator is 66 mV/A.



a. Enlarged view of load regulation shown below

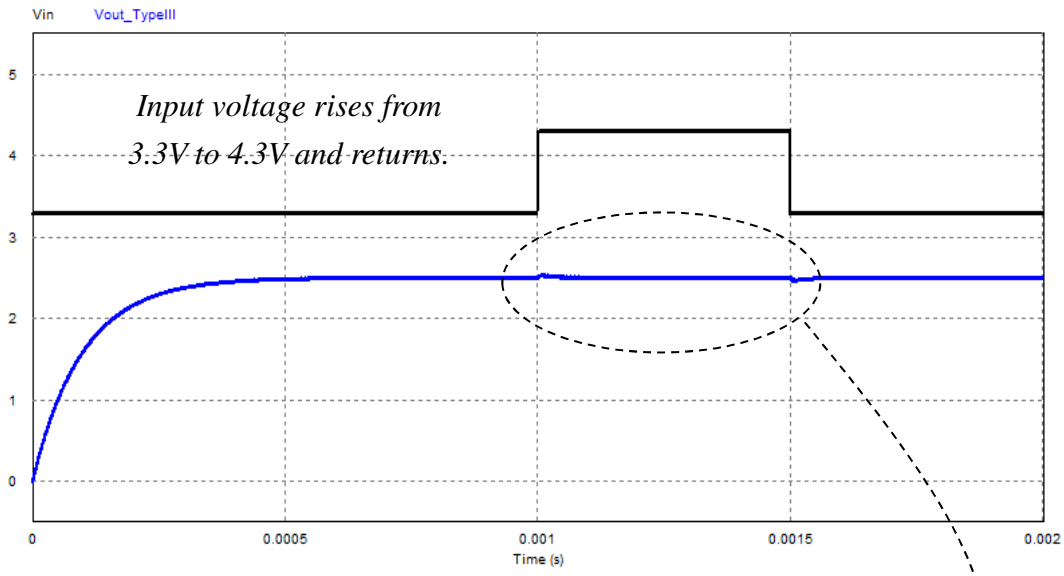


b.

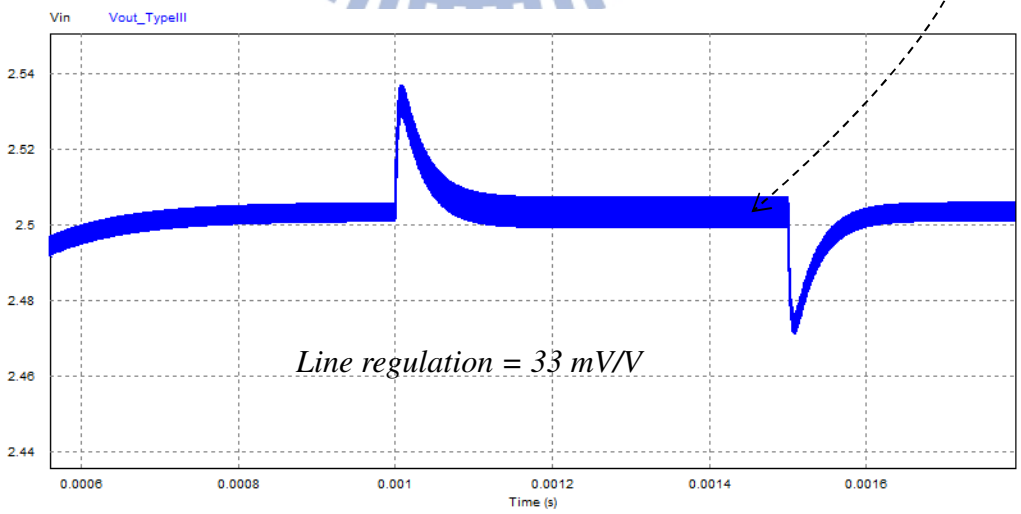
Figure 28 Load regulation of buck converter with PID OCC

2.3.3 Line Regulation

Line regulation is expressed as ratio of change in the output voltage relative to the change in the input line voltage. The line regulation of buck with Type III is 33mV/V at the condition that input voltage changes from 3.3V to 4.3V within 1 μsec as shown in Figure 29 (a) and (b) that is the enlarged view.



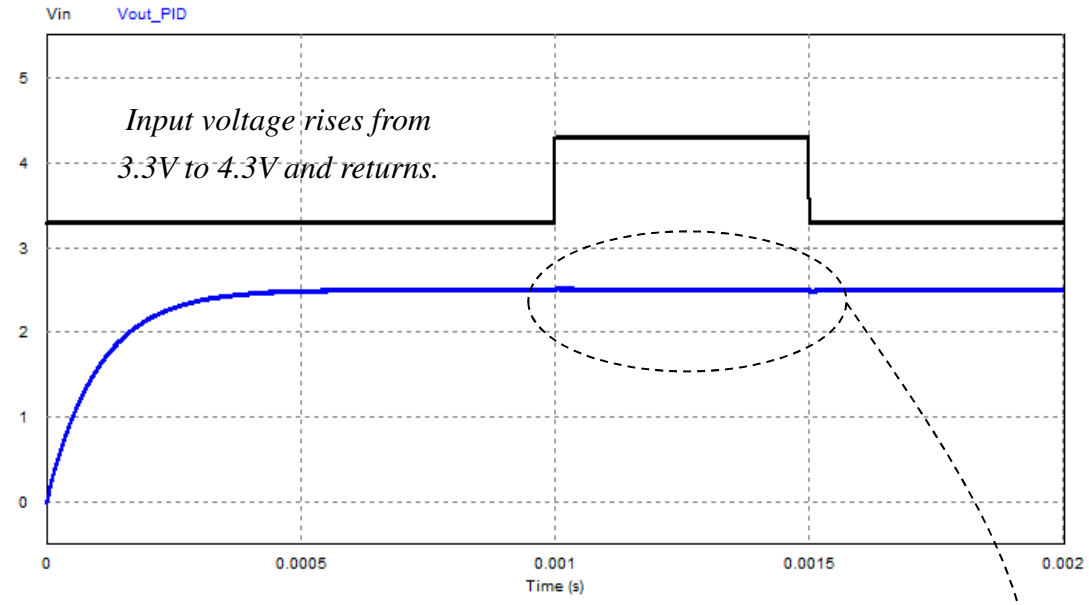
(a) Line regulation of buck with Type III compensator



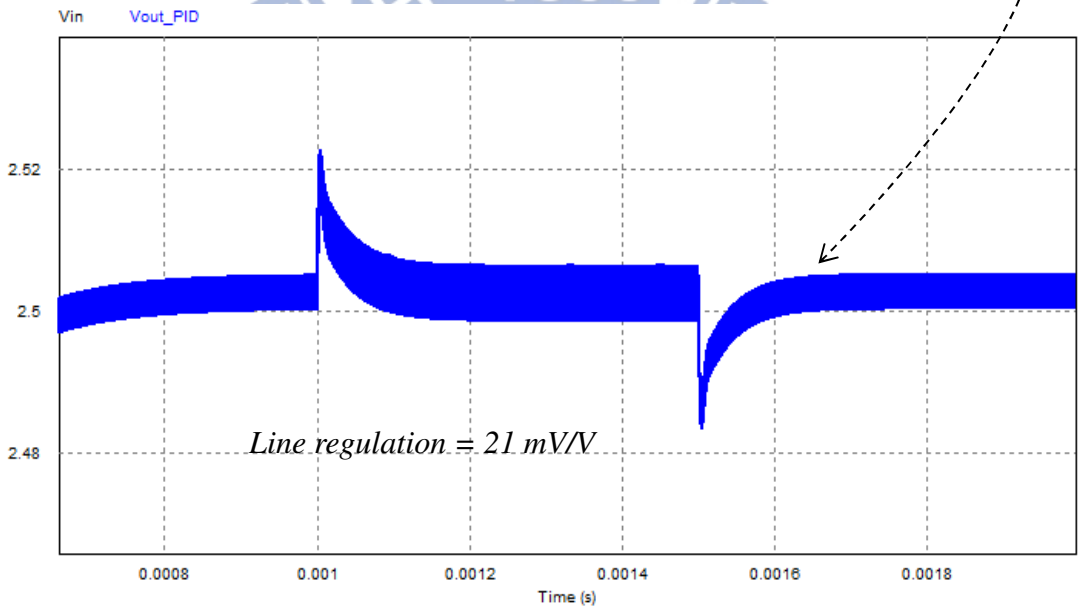
(b)

Figure 29 Line regulation of buck converter with off-chip Type III compensator

Figure 30 (a) and (b) shows the regulation of buck with PID compensator is 21mV/V as input voltage changed from 3.3V to 4.3V. Compared with that of Type III, it is 10mV better, but for load regulation, buck with PID is 15mV worse than that of Type III.



(a) Line regulation of buck with PID OCC



(b)

Figure 30 Line regulation of buck converter with PID OCC

2.4 Type III and PID OCC Comparison

. As listed in Table 6, it summarizes the comparison between DC-DC buck with voltage mode control compensated by off-chip Type III and on-chip PID and the performance of transient and frequency response for them are quite comparable.

Table 6 Comparison of Type III and PID OCC

Compensation		**Type III**	**PID**
Power Stage	Supply Voltage	3.3V	
	Output Voltage	2.5V	
	Switching Frequency	1MHz	
	Control Scheme	Voltage Mode	
LC Filter	Inductor-DCR	2.2μH-18mΩx2	
	Capacitor-ESR	22μF-16mΩx2	
Compensator	Technique	Off-Chip	On-Chip
	Components	OPA1	OTA1
		R1 7kΩ	OTA2
		C1 1pF	OTA3
		R2 70kΩ	OTA4
		C2 400pF	Rz 50MΩ
		R3 100Ω	Cz 40pF
		C3 600pF	Rl 200kΩ
			Cl 20pF
	Zero1	$\frac{1}{R2C2}$	$\frac{G_{m1}}{C_Z}\frac{G_{m2}}{G_{m3}}$
	Zero2	$\frac{1}{(R1+R3)C3}$	$\frac{G_{m3}}{G_{m4}}\frac{ClRl}{LC_O}$
	Crossover Frequency	200kHz	
	Phase Margin	60°	
	Line Transient	Comparable	
	Load Transient	Comparable	

Chapter 3

OCC for Current Mode Buck Converter

Chapter 3 presents the concepts of current mode synchronous buck converter with on-chip compensations. The simplified diagram of the system is as shown in Figure 31. As far as the compensators are concerned in this chapter, first as it is discussed in the Chapter 1 that PI compensation is sufficient to stabilize the current mode buck, PI compensation will be reviewed in short. Second, following Miller compensation and capacitor multiplier, they pave the way for the application of current mode Miller (CMM) OCC in section 3.2. Then, the current mode counterpart is thus named time mode Miller (TMM) OCC that will be discussed in section 3.3.

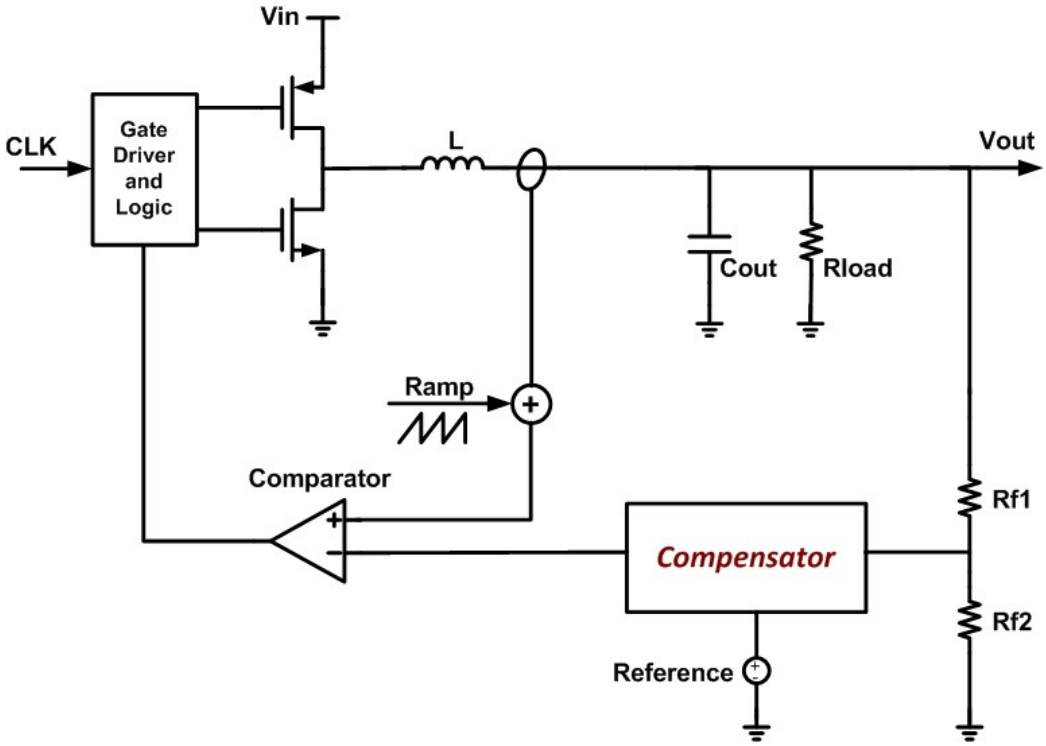


Figure 31 Simplified diagram of synchronous buck with current mode control

3.1 PI off Chip Compensation

Figure 32 illustrates PI compensator realized by OPA that is actually taken away one capacitor and one resistor from PID compensator as mentioned in chapter two. Thus, it only has one pair of zero and pole. In the PI compensator, the ripple of the output voltage (Vo) is filtered by the integrator during the full period comparison process, in which the error between the average value of Vfb and Vref is integrated in a large C2. From circuit point of view, PI compensator by OPA could be correspondingly implemented by OTA. [2][9]

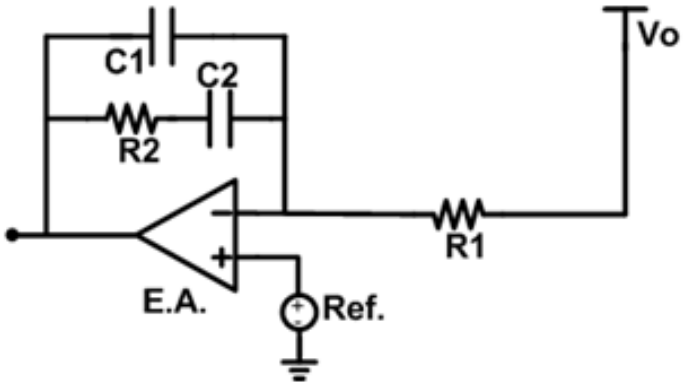


Figure 32 PI compensation implemented by OPA

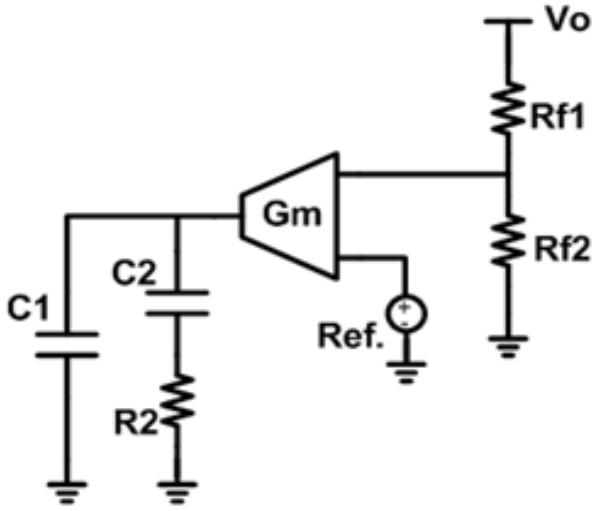


Figure 33 PI compensation implemented by OTA

The transfer function and the formula of pole and zero positions for PI compensator are shown in the following equations 2-1 to 2-3. From Figure 34, it shows the Bode plots and the phase boost that is 90°for PI compensation.

$$GAIN_{TYPEII} = \mathrm{K}\frac{s + \frac{1}{R2C2}}{s + \frac{C1 + C2}{R2C1C2}} \qquad (2-1)$$

$$Zero1 = \frac{1}{R2 * C2} \qquad (2-2)$$

$$Pole1 = \frac{1}{R2(\frac{C1C2}{C1 + C2})} \qquad (2-3)$$

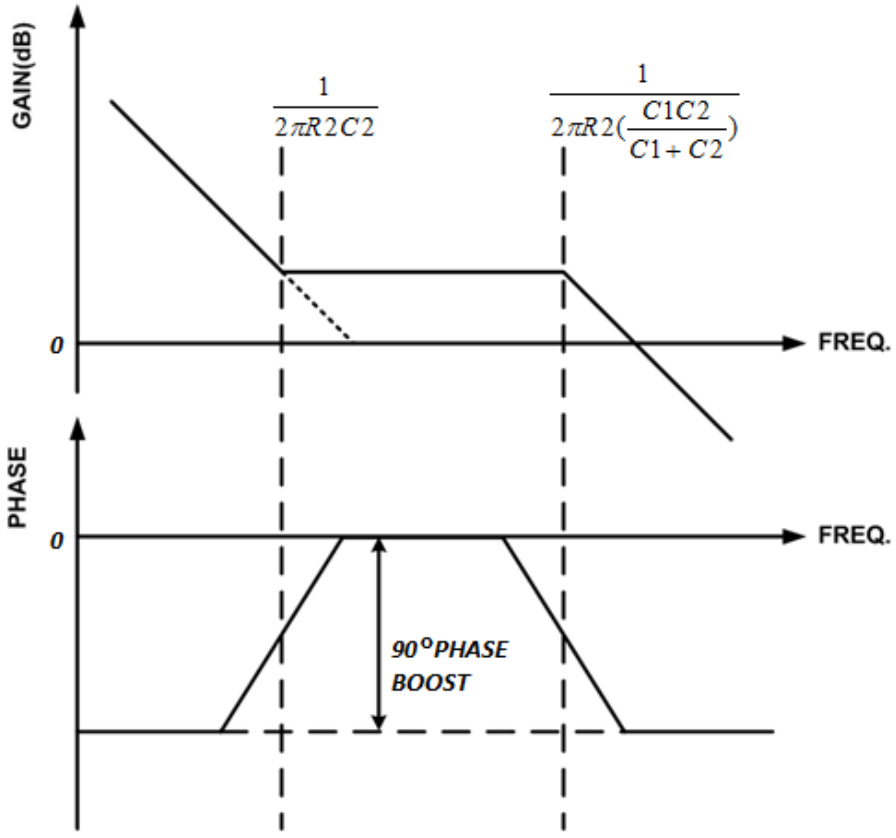


Figure 34 PI compensation Bode plots

It would help get the picture of a buck converter with PI compensator from Figure 35 and the overall Bode plots of PI compensated system as illustrated in Figure 36.

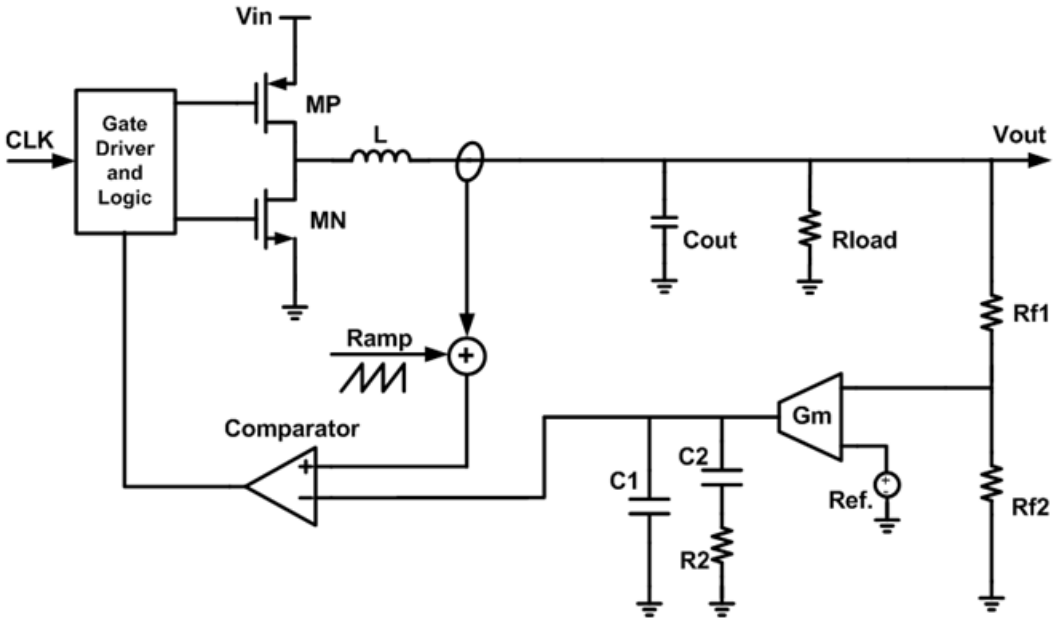


Figure 35 Synchronous current mode Buck with PI compensator

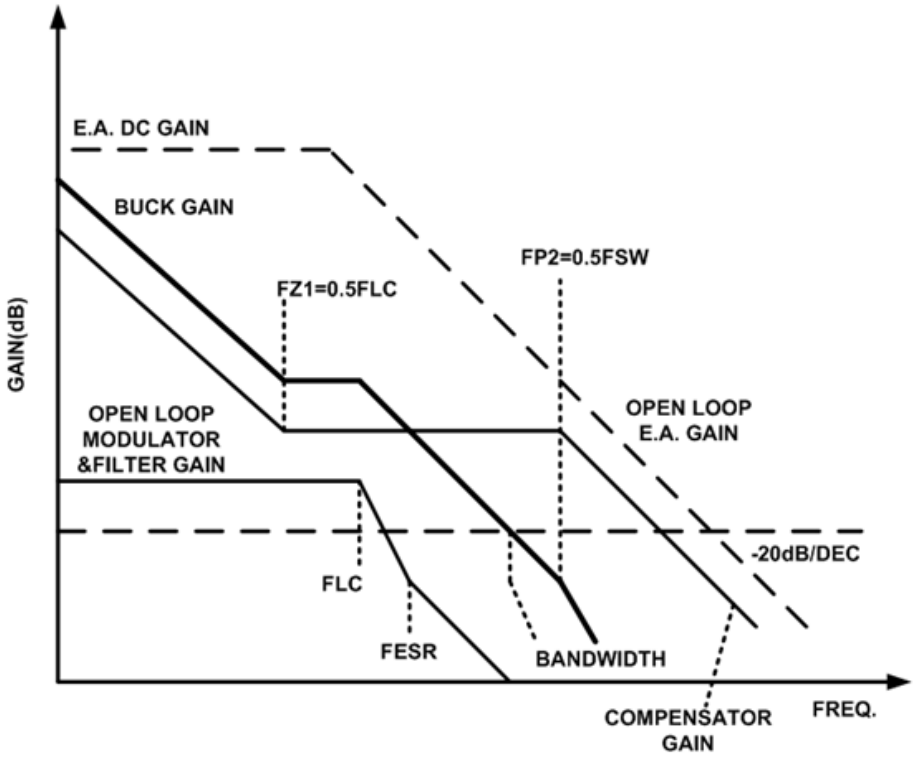


Figure 36 PI compensated system Bode plots

3.2 CMM On-Chip Compensation Technique

In this section, the technique named current mode Miller (CMM) OCC is described for its application of on-chip integration compared with that of off chip compensation in section 3.1. The background of Miller compensation and capacitor multiplier are also introduced in the followings for better appreciation of CMM OCC.[23]

3.2.1 Miller Compensation

As illustrated in Figure 37 a two-stage amplifier circuit is applied the common technique to use Miller capacitor for compensating amplifier feedback circuits. The poles of a two-stage amplifier are split, one toward low frequencies and the other toward high frequencies. The pole at the output of the first stage becomes dominant. Transconductors Gm1 and Gm2 are assumed to be ideal, and R1 and R2 resistors model the effective impedance to ground at their corresponding nodes, CL and Cc are the load capacitor and the compensating capacitor, respectively. The dominant low-frequency pole is located at node n1 and is defined by [12]

$$P_{n1} \approx \frac{1}{2\pi R1 A_2 C_C} \quad where \;\; A_2 = G_{m2} R2$$

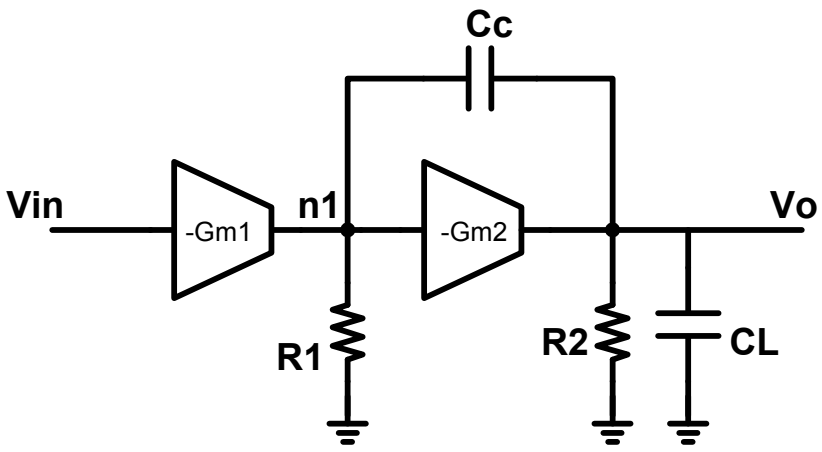


Figure 37 Miller compensated two stages amplifier

3.2.2 Capacitor Multiplier

As illustrated in Figure 38 the voltage mode capacitor multiplier that takes advantage of Miller effect discussed in section 3.2.1. The equivalent capacitance to ground at node is derived from the displacement current flowing through capacitor. The current is

$$I_c = \Delta V_c s C_c = (V_{n1} - V_o) s C_c = V_{n1}(1 + A_2) s C_c$$

$$where\ V_c\ is\ the\ voltage\ across\ the\ capacitor$$

$$(I_c = \frac{V_c}{Z_c}, Z_c\ is\ the\ impedance\ of\ the\ capacitor)$$

The equivalent capacitance to ground Ceq is

$$C_{eq} = \frac{I_c}{sV_{n1}} = (1 + A_2) C_c$$

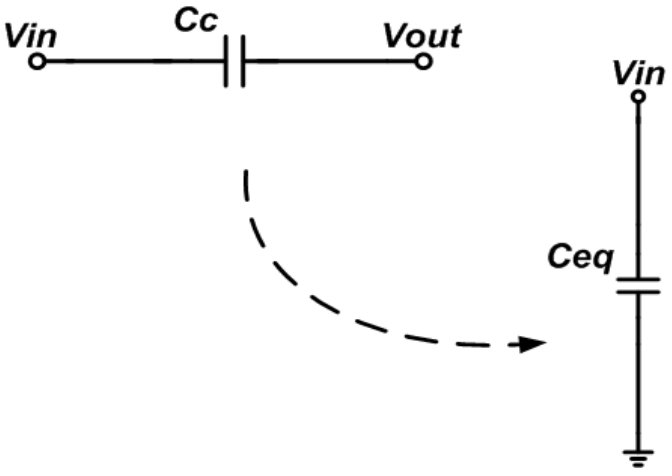


Figure 38 Voltage mode capacitor multiplier

$$V_O = -A_2 * V_{n1}$$
$$C_{eq} = (1 + A_2) * C_C$$

In Figure 39, on the other hand, shows the concept of the current-mode capacitor multiplier. The essence of the idea is to sense the current through the capacitor, multiply it by a factor greater than one (k > 1) and put it back to the same node by means of a current-controlled current source. The amplification could be realized by current mirrors. The equivalent capacitance seen at node n1 is [11][12]

$$C_{eq} = \frac{I_{ceq}}{sV_{n1}} = \frac{I_C + kI_C}{sV_{n1}} = \frac{I_C(1+k)}{sV_{n1}} = (1+\mathrm{k})C_C$$

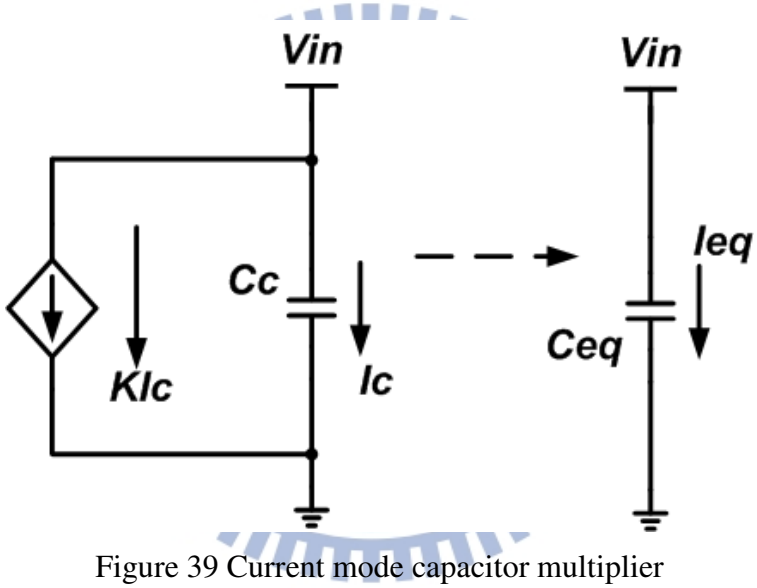


Figure 39 Current mode capacitor multiplier

$$i_C = \mathrm{C}\frac{dv_C}{dt}$$

$$(\mathrm{k}+1) * i_C = (k+1) * C\frac{dv_C}{dt}$$

$$C_{eq} = (\mathrm{k}+1) * C_C$$

3.2.3 CMM OCC Architecture

When the operation condition of a MOSFET is $V_{DS} << 2(V_{GS}-V_{TH})$, one would have

$$I_D \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS}$$

The linear relationship can be also represented by a linear resistor equal to

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$

If two MOSFETs operating in linear region have the same VGS and VDS, the equivalent impedances are inversely proportional to their aspect ratios. The principle can be the implementation of current mode Miller capacitor multiplier discussed in section 3.2.2. As shown in Figure 40, it is to integrate current mode Miller capacitor multiplier into PI compensation for the application in DC-DC buck converter, and therefore is named current mode Miller (CMM) on-chip compensation (OCC). [15][16][17][18]

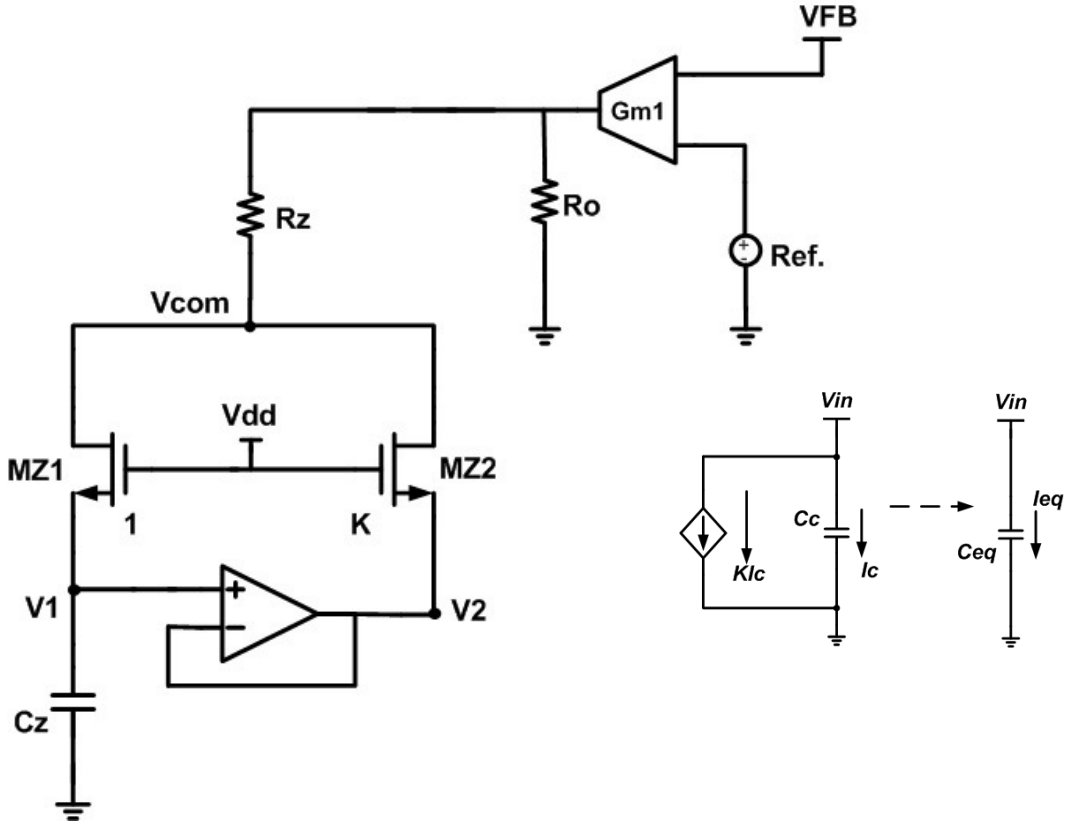


Figure 40 CMM OCC schematics

The equivalent impedances of MOS transistors in triode region are modeled as *R* and *KR* as shown in Figure 40. If high frequency components are neglected, the transfer function of current mode Miller compensation is

$$\mathrm{A(s)} \approx -g_{m1}R_O\frac{1+sKC_zR_z}{1+sKC_z(R_z+R_O)} \qquad (3-1)$$

Then, if R_O is much larger than R_Z, the zero and pole generated by CMM OCC can be written as,

$$\text{Zero} \approx -\frac{1}{KC_zR_z}$$

$$\text{Pole} \approx -\frac{1}{KC_zR_O}$$

As shown in Figure 41 synchronous current mode DC-DC buck converter with TMM compensation, we could be easier to assign the parameters of compensator using the worksheet as Table 7 that will be introduced in circuit implementation in next chapter.

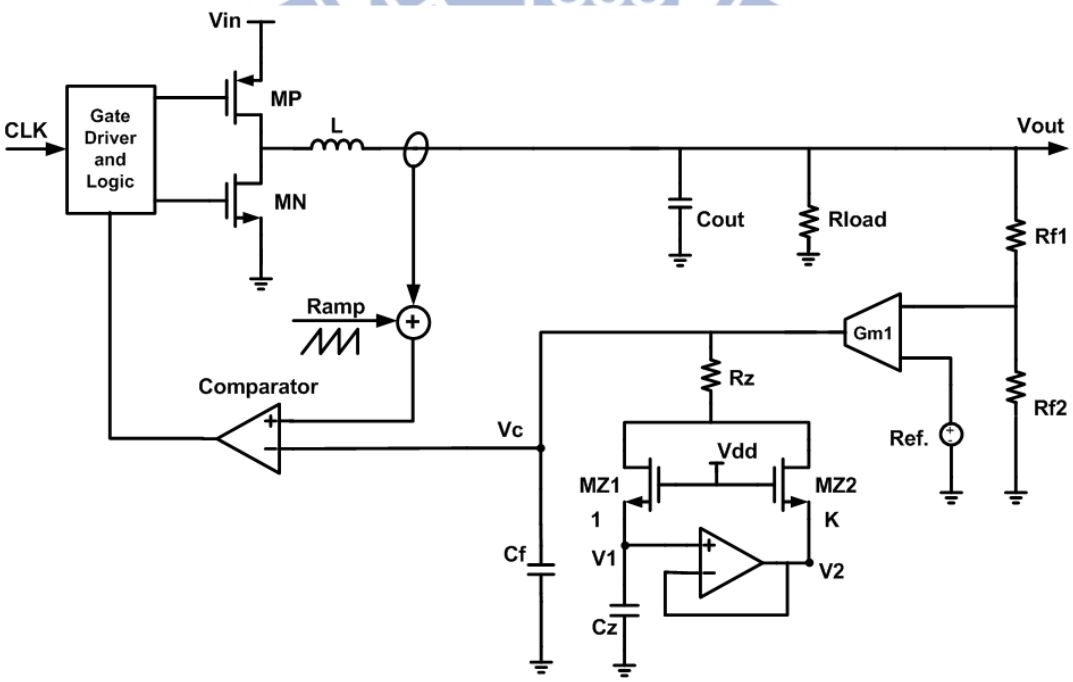


Figure 41 Synchronous current mode buck with CMM OCC

3.3 TMM On-Chip Compensation Technique

This section presents the on-chip compensation technique of current mode synchronous DC-DC buck converter named TMM OCC, which decreases the charging or discharging time of the capacitor in order to obtain the capacitance amplification that resembles to the Miller effect. In the following passages the concept of TMM OCC will be addressed. [21]

3.3.1 TMM OCC Concept

Figure 42 consists of a TMM path, a continuous zero and a noise filter. Gm1, Cc and switch form TMM path generating integral information. Gm2 and Rz form the continuous zero path. It features a pre-determined short time (TS) defined in one switching period. As the switch is turned on during TS, control voltage is changed within TS. For the rest of a period, switch is OFF and holding buffer keeps the output of Gm1 to Vc. If TS is short enough, Vc changes slowly. Thus, a capacitance amplifying similar to Miller effect is obtained.

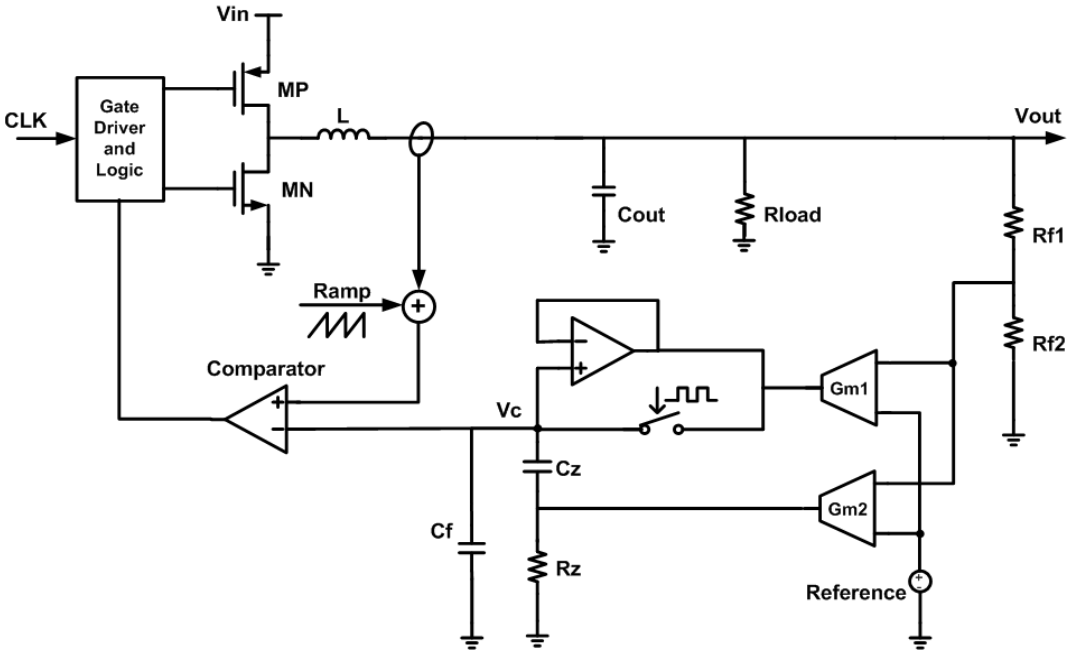


Figure 42 DC-DC buck converter with TMM compensation

3.3.2 Qualitative Analysis of TMM OCC

TMM OCC in Figure 43 shows the operation of TMM OCC integration that is very similar to that of PI compensator except for the switch added. Compared with conventional integration in PI compensation as the illustration in Figure 44 and Figure 45, for conventional integration, Vc2 changes slowly and continuously during the switching period. On the other hand, TMM OCC integration path, Vc1 changes discontinuously during only TS and holds in the rest of the switching period. The point here is that the total change of both vc1 and vc2 is exactly the same. The relation between the capacitances Cc1 and Cc2 is

$$C_{C1} \cdot \Delta v = Gm \cdot v_e \cdot TS$$

$$C_{C2} \cdot \Delta v = Gm \cdot v_e \cdot TP_e$$

$$\rightarrow C_{C2} = \frac{TP_e}{TS} \cdot C_{C1}$$

From this operation, the equivalent Miller capacitor of TMM OCC is as

$$C_{eq} = \frac{TP_e}{TS} C_c$$

Where TP_e is one switching period

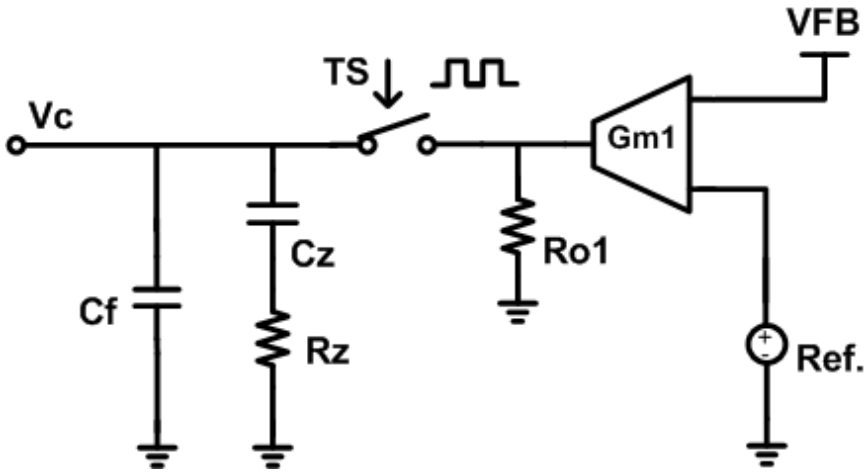


Figure 43 TMM OCC only with Cz and Rz

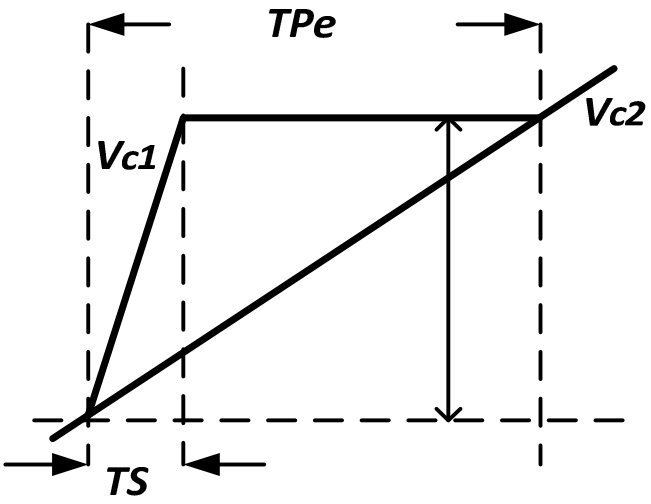
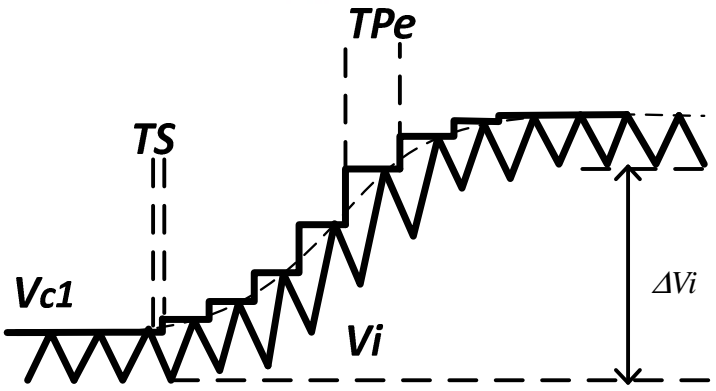


Figure 44 Interpretation of TMM OCC within a period

(a) PI compensation



(b) TMM OCC

Figure 45 Comparison of PI compensation with TMM OCC

Miller gain is the ratio of TPe and TS. To have a larger gain, a shorter TS or longer TPe is necessary, but it is limited to make TS significantly short. TPe also cannot be changed because it is determined by the switching frequency. However, as shown in Figure 46 TS can be generated per 2^N switching periods by using an N-bit counter. In Figure 47, the total change (Δvi) controlled by (Δvc) is equivalent to that of the conventional compensator. By this operation, the miller gain of TMM OCC is multiplied by 2^N. The equivalent capacitance is

$$C_{eq} = \frac{2^N \cdot TP_e}{TS} C_c$$

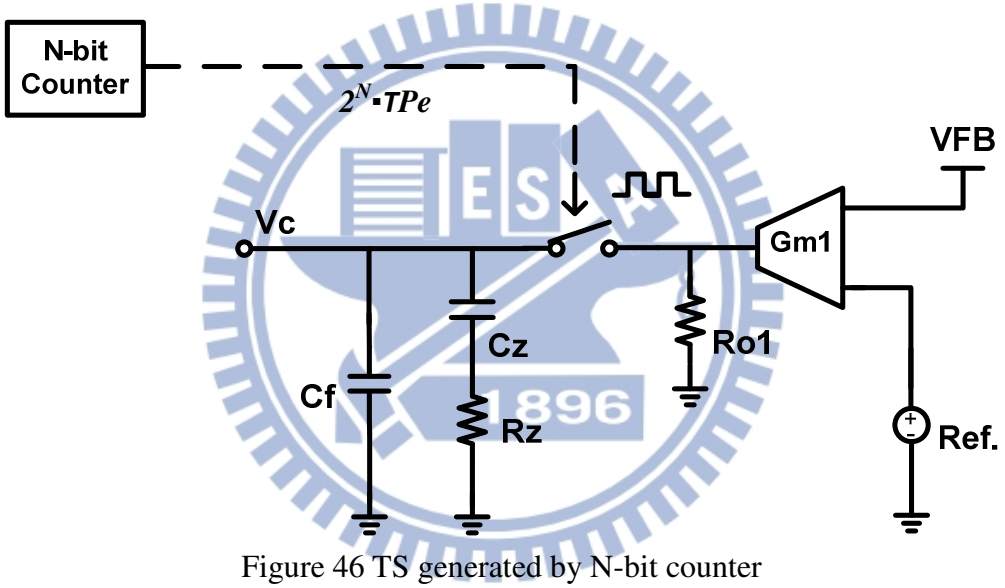


Figure 46 TS generated by N-bit counter

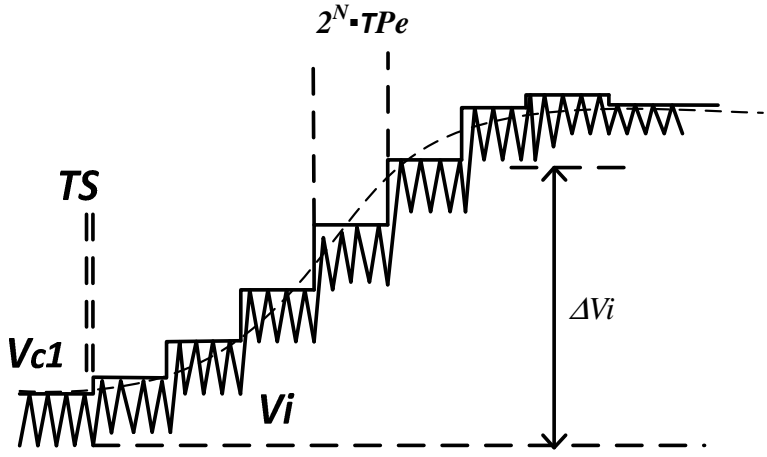


Figure 47 TMM OCC operation per 2^N switching period

In PI compensator, the zero is simply obtained by connecting Rz with Cc in series. However, in the TMMC the zero is not obtained even if Rz is connected with Cc in series as in Figure 48 with Bode plot that is without any zero. It is due to a simple resistor is not suitable for the TMMC since the resistor cannot reflect the phase lead information in a very short period. Therefore, an additional continuous path is connected to Rz in order to pass the proportional signal of the Vfb to Vc. This proportional signal of the Vfb is divided by the ratio of Cc and Cc + Cf and added to the Vc signal to generate the zero as shown in Figure 49 with Bode plot that is the same as that of PI compensator.

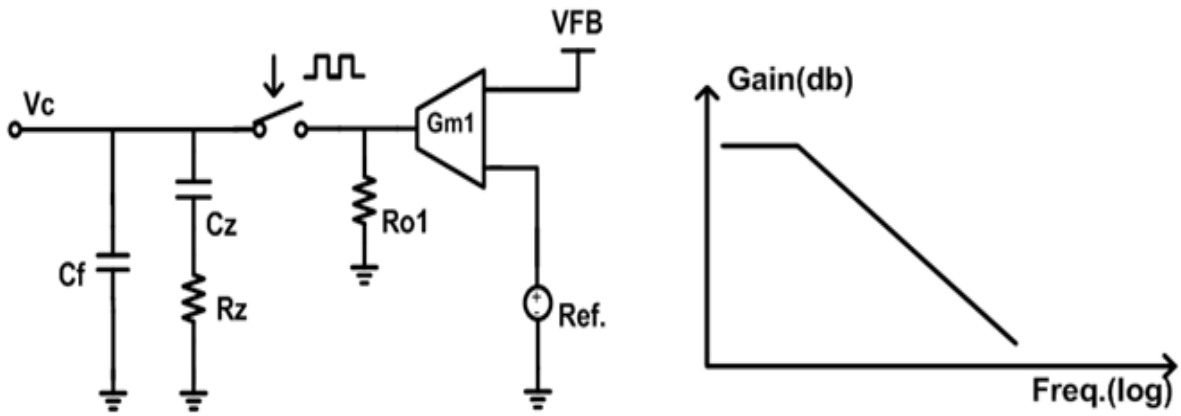


Figure 48 TMM OCC using small Cz and Rz

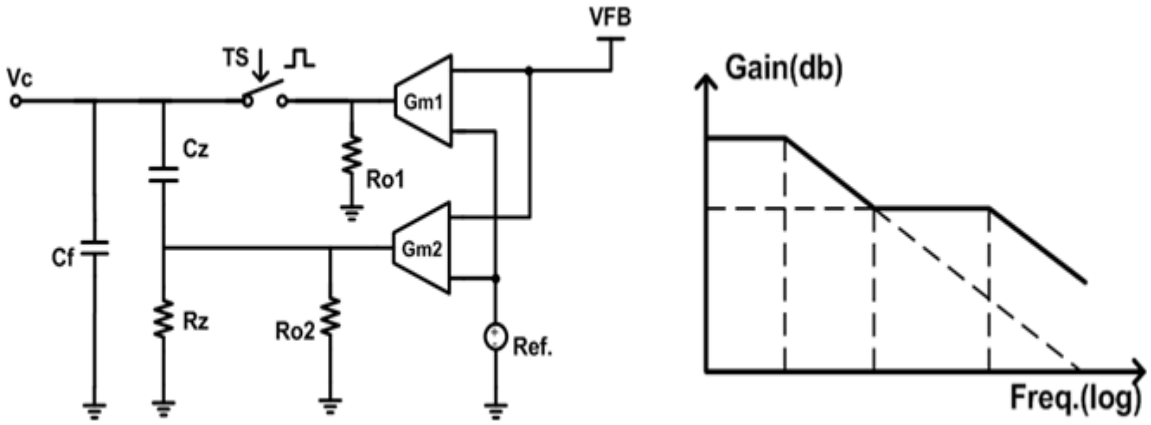


Figure 49 TMM OCC using small Cz with continuous zero

3.3.3 Quantitative Analysis of TMM OCC

As mentioned by TMMC concept, the Vc signal generated from the sum of the TMMC signal and the continuous zero signal is interpreted by the superposition method. So does for transfer function of TMMC as shown in Figure 50. The transfer function of the TMM compensator is the sum of the transfer functions of the TMMC path and continuous zero path which are derived in this section, respectively.

The error voltage (Ve) which is the difference between Vfb and Vref, is converted to current by Gm1 and the switching TS. The current flows into or from the equivalent output impedance of compensator to generate Vc. The transfer function of the TMMC path is

$$\frac{V_{C1}(s)}{V_e(s)} \approx \frac{g_{m1}R_{o1}}{1 + s\frac{2^N TPe}{TS}(C_C + C_f)R_{o1}}$$

The Ve is also converted to current by Gm2. The current is divided by the ratio of impedance of Rz and the series connection of Cc and Cf. This divided current flows into or from Cf to generate Vc. The transfer function of the continuous zero path is

$$\frac{V_{C2}(s)}{V_e(s)} \approx g_{m2}\frac{R_Z}{R_Z + \frac{1}{sC_C} + \frac{1}{sC_f}} \cdot \frac{1}{sC_f}$$

By superposing the transfer function of TMM path and the one of continuous zero path , the total transfer function of the TMM OCC is

$$\frac{V_C(s)}{V_e(s)} = \frac{V_{C1}(s)}{V_e(s)} + \frac{V_{C2}(s)}{V_e(s)}$$

$$\frac{V_C(s)}{V_e(s)} \approx g_{m1}R_{o1}\frac{\left[1+\frac{s}{\omega_Z}\right]}{\left[1+\frac{s}{\omega_{p1}}\right]\left[1+\frac{s}{\omega_{p2}}\right]}$$

$Where$

$$\omega_Z = \frac{1}{\frac{g_{m2}}{g_{m1}}\frac{2^N TPe}{TS}C_Z R_Z}$$

$$\omega_{p1} = \frac{1}{\frac{2^N TPe}{TS}(C_Z + C_f)R_{O1}}$$

$$\omega_{p2} = \frac{1}{\frac{C_Z C_f}{C_Z + C_f}R_Z} \qquad ( )$$

As shown above, ω_{p1} and ω_z are placed at the low frequency range because of the miller effect of TMM OCC; however, ω_{p2} not affected by the miller effect of TMM OCCC is located at a high frequency. This pole-zero locations are corresponding to those of the conventional PI compensator that needs large capacitance whose value equals to (2^N·TPe /TS)*Cz.

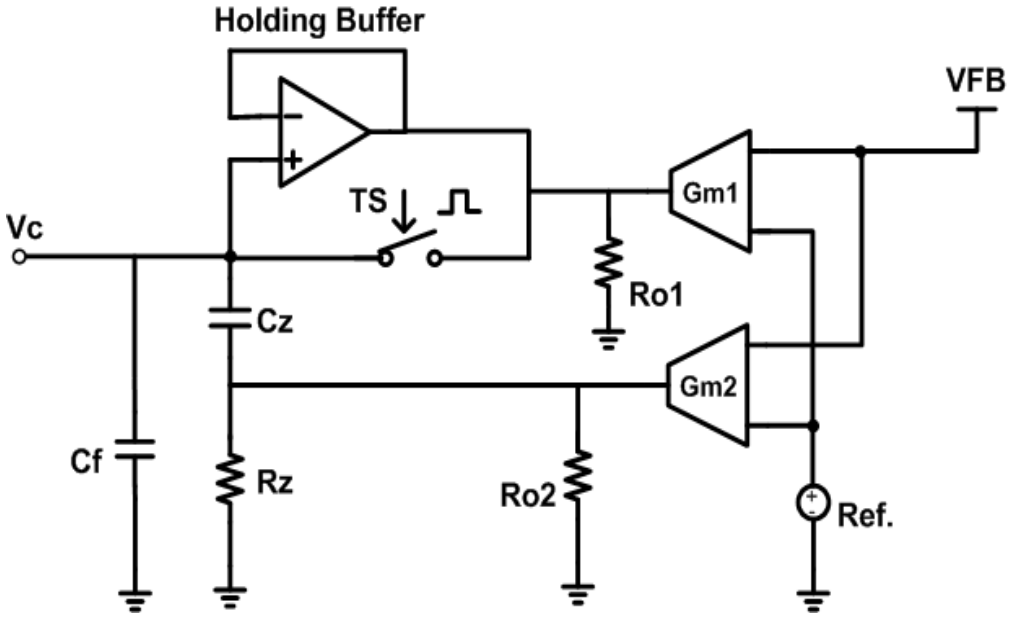


Figure 50 TMM compensator schematics

Chapter 4

Circuit Implementation and Simulation Results

In this chapter, the details of the key sub circuits for CMM OCC and TMM OCC in chapter 3 are presented. The circuit analyses and HSPICE simulations for these sub blocks are also discussed in this chapter. In the beginning the technology information will be provided.

4.1 Technology Description

The device models such as CMOS, MiM Cap, HR, BJT etc. in this integrated circuit simulation are based on VIS 0.25um CMOS Mixed-Signal 1P5M (single poly, 5 metal layers), silicide, Al technology. The node actually is a TSMC-like process that is compatible with industry standard. [25][26]

Key features of frond-end of line are including shallow trench isolation (STI) for active isolation to reduce device pitch, retrograde twin well for a low well sheet resistance, enhancement of latch-up behavior, and for a better control of parasitic field transistor, and self-aligned Ti-silicided drain, source and gate that significantly reduces gate and S/D serial resistance. For high value resistors offered in this technology are 1kΩ per square and 1.5kΩ per square.

For back-end key features, they include Tungsten contact and via for connecting metal layers, chemical mechanical polishing (CMP) to enhance planarization of STI, contact, via, and inter-metal dielectric. The metal insulator metal (MiM) capacitor provided in this process is with 1.15fF per square unit capacitance.

4.2 Circuit Implementation

The section is to present the circuit implementations of CMM OCC and TMM OCC including the major building blocks such as OTA, voltage follower, 3-input OTA, short pulse generator etc.

4.2.1 CMM OCC

The schematic of CMM OCC is as shown in Figure 51. By means of control for the transistors working at linear regions, the current ratio of I1 flowing through left side in CMM OCC and I2 through right side is K. As described in section 3.2.3, the equivalent capacitance Ceq is equal to (1+k)*Cz.

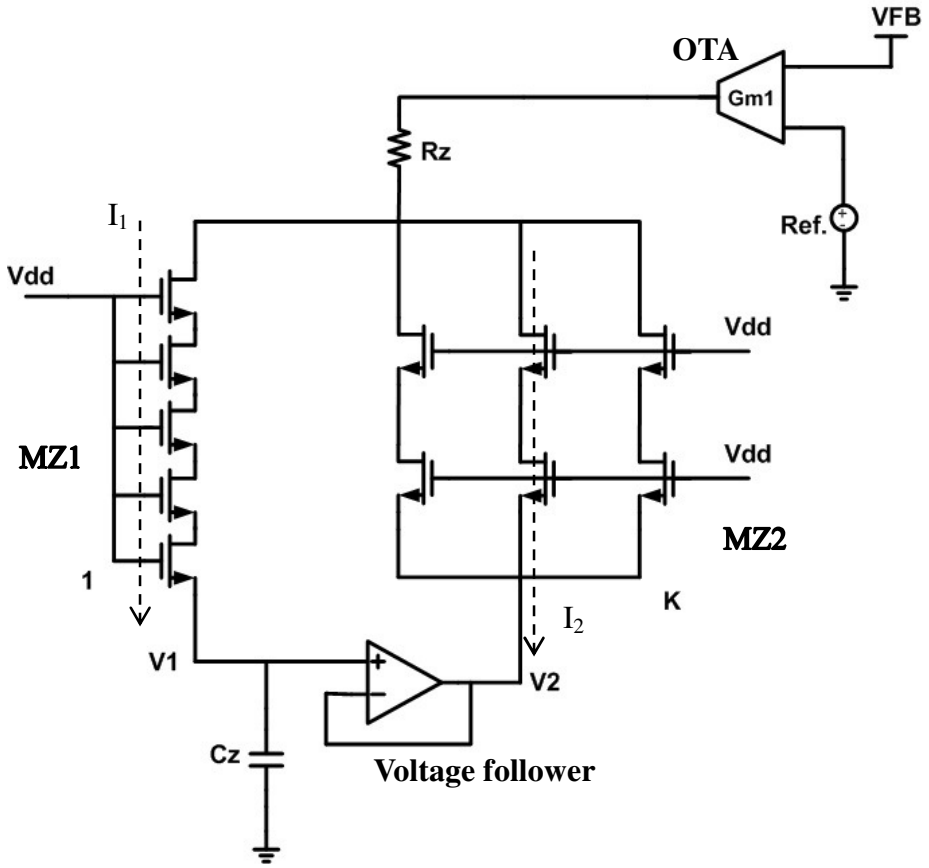
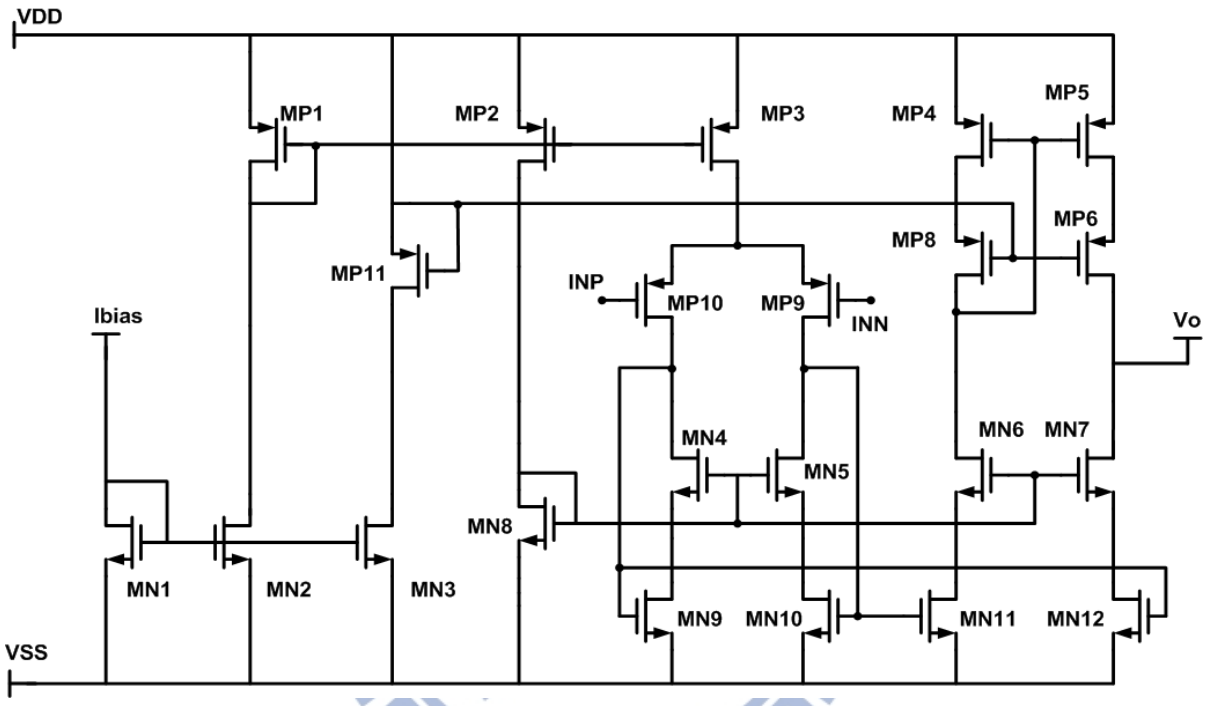


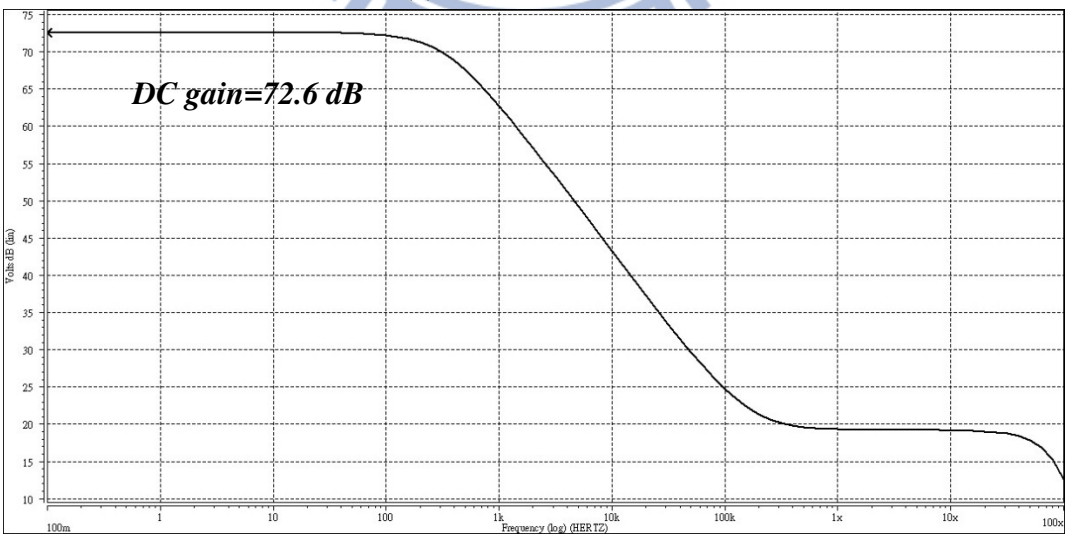
Figure 51 CMM compensator schematics

4.2.2 OTA Amplifier

The error amplifier used in Figure 51 is constructed by an OTA. The frequency response of OTA is as shown in Figure 52. The DC gain of OTA is designed to be 72.6 dB and bandwidth is over hundreds of MHz.[6]



(a) OTA Schematics



(b) OTA DC gain

Figure 52 OTA schematics and DC gain

4.2.3 Voltage Follower

The gate terminals of transistors MZ1 and MZ2 as shown in Figure 51 are connected to voltage source Vdd and the voltage level of output node of OTA is designed smaller to ensure that the transistors of MZ1 and MZ2 work in linear region. When capacitor Cz is discharged, the source voltage of MZ1 is higher than its drain voltage. When capacitor Cz is charged, the source voltage of MZ1 is lower than its drain voltage. To count with these two circumstances, it is necessary to use a voltage follower to sink and source current to transistor MZ2 according to the drain-source voltage of MZ1. The circuit of voltage follower is as shown in Figure 53 that is a two-stage amplifier and C1, C2 and Rcomp are to compensate the frequency response of the amplifier.

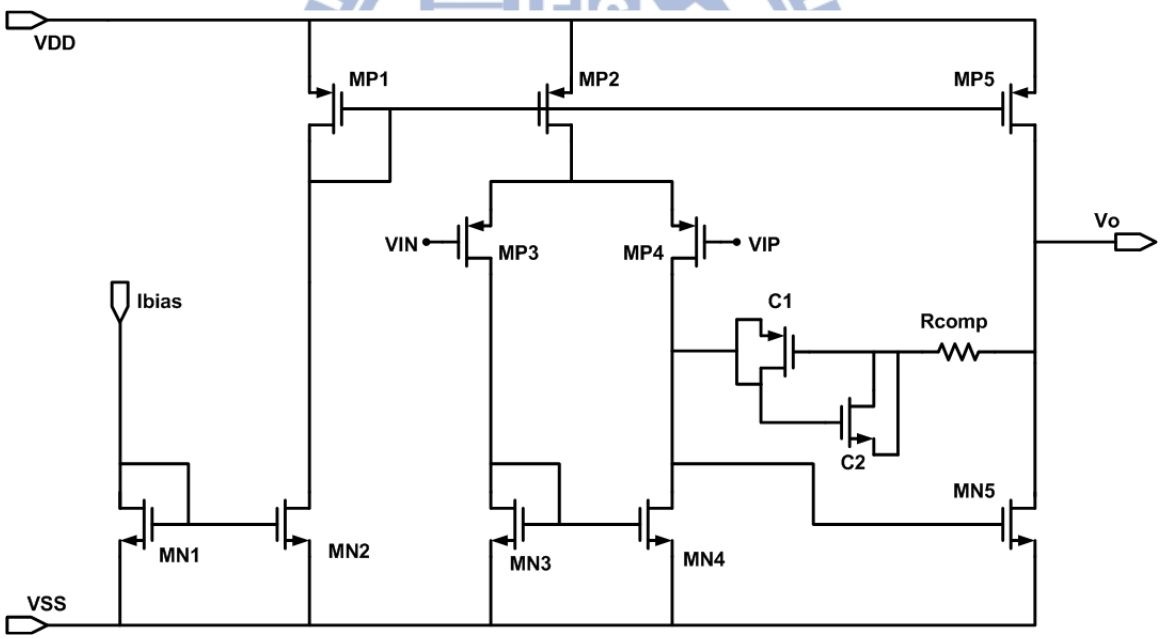


Figure 53 Schematics of voltage follower

4.2.4 TMM OCC

The schematic of TMM OCC shown in Figure 54 consists of a TMM path, a continuous zero and a noise filter. The G_{m1}, Cz and transmission gate (TG) generating the integral information also obtain the large equivalent compensation capacitance through the sampling and hold procedure of TS. The G_{m2} and Rz form the continuous zero path generating the proportional gain information as discussed in section 3.3.2. to have the zero similar to that in PI compensator frequency response.

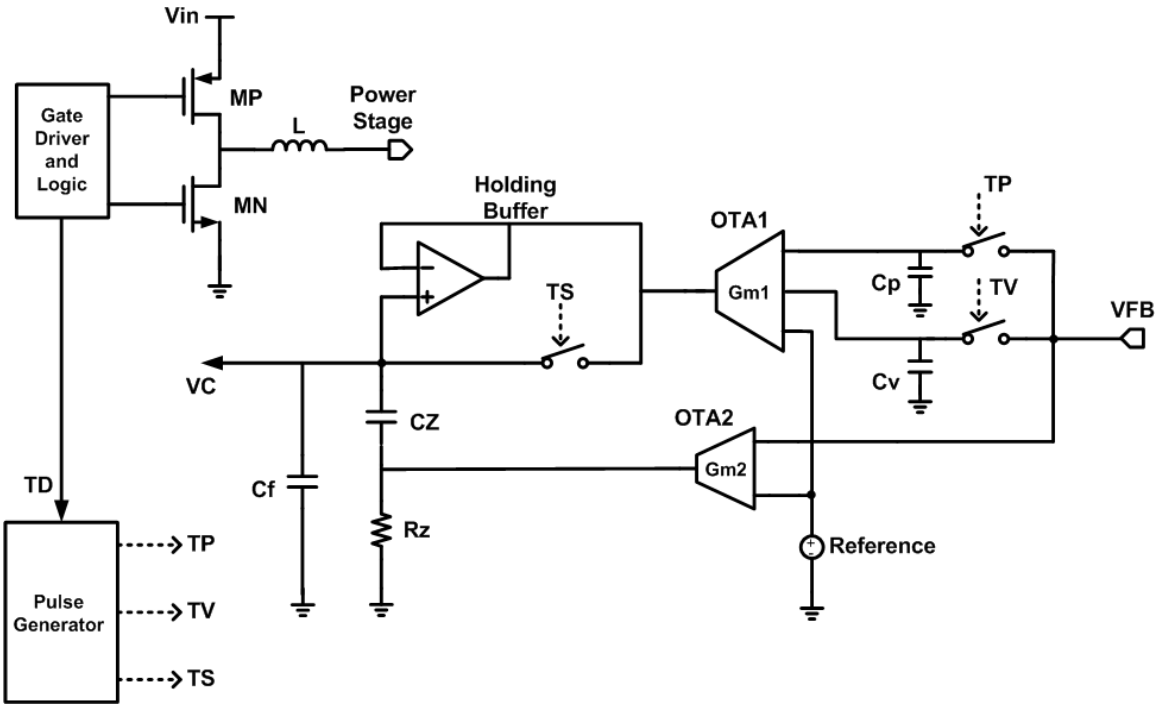


Figure 54 Schematics of TMM OCC

For TMM OCC the comparison time is limited to TS, but the error amplifier has to locate the center value of feedback voltage during this short period to integrate the difference between reference voltage and feedback voltage. Because of the ripple voltage it is not easy to know the moment if feedback voltage is at the center value.

4.2.5 Three-Input OTA

To resolve the issue mentioned in the end of section 4.2.4, the 3-input OTA (Gm1) and the two track-and-holds as illustrated in Figure 54 are used. The two track-and-holds are realized by two transmission gates as shown in Figure 55.

Peak holding capacitor (Cp) captures the peak of V_{FB} (Vp) during a peak capture pulse (TP) generated at the moment when the low side power transistor is turned on, while the valley holding capacitor (Cv) captures the valley of V_{FB} (Vv) during a valley capture pulse (TV) generated at the moment when the high side power transistor (MP) is turned on.

The effective average value of Vp and Vv, which is the center of V_{FB}, is then obtained through 3-input OTA (Gm1). By means of this process, the error between reference voltage and the center of feedback voltage is properly integrated into Cz.

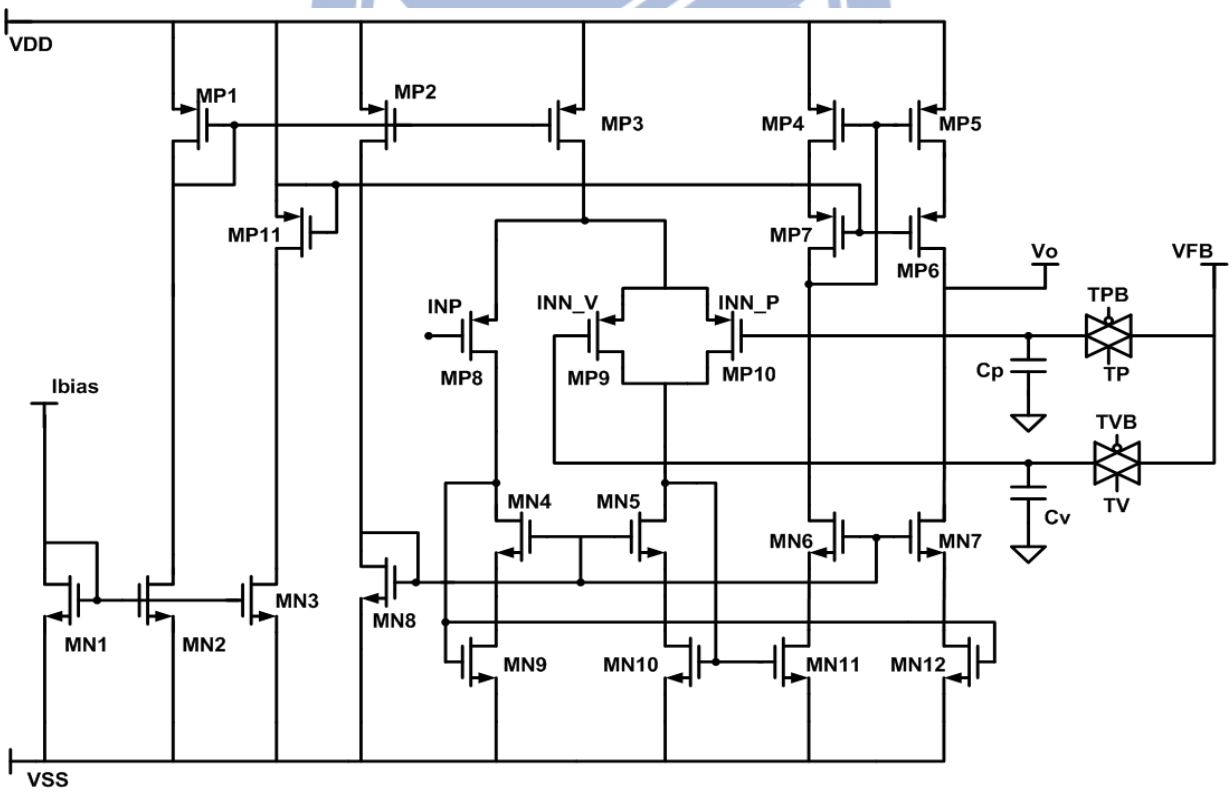


Figure 55 Schematics of 3-input OTA amplifier

4.2.6 Holding Buffer

In the procedure described in section 4.2.5, it is important that the output node of 3-input OTA needs to be kept by Vc even when the transmission gate St is in the open state in order to guarantee the proper operation of Gm1 during TS. In addition, the leakage current of St should be minimized to prevent the mal-function of the compensator resulting from the significantly small Cz. The holding buffer as shown in Figure 54 can solve the problem by maintaining the output node voltage of Gm1 to Vc. The schematic of holding buffer is as shown in Figure 56 that is similar to voltage follower used in CMM compensator.

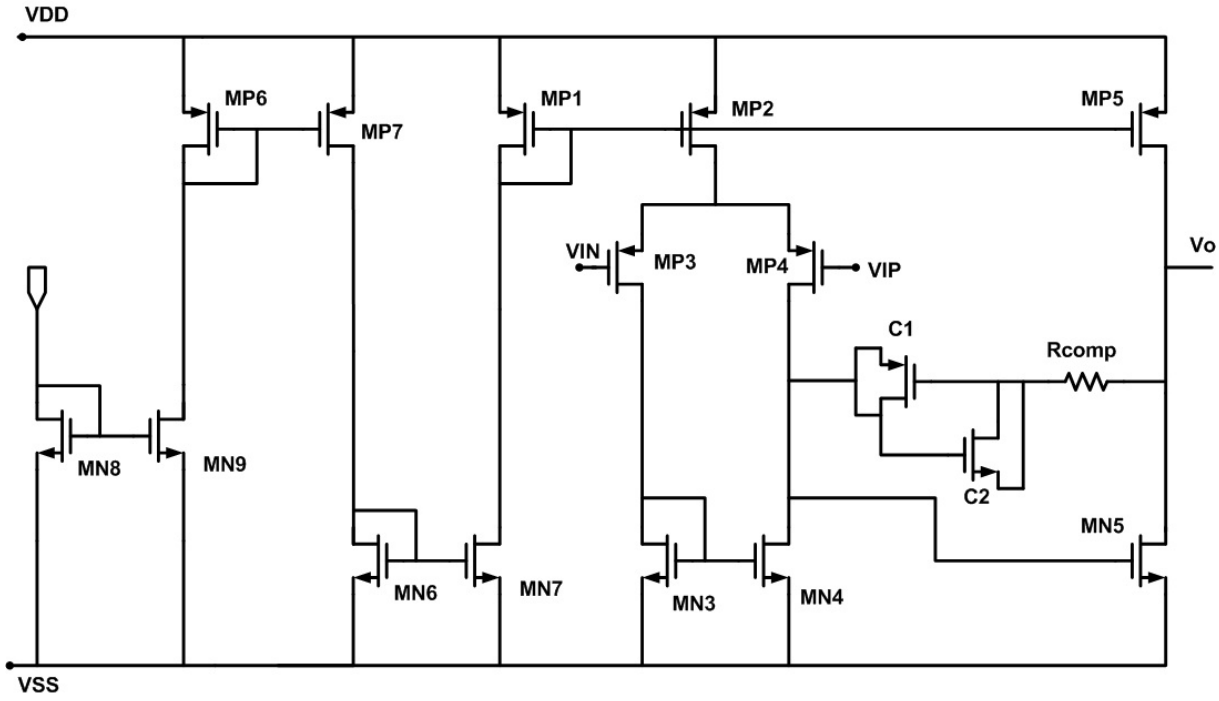


Figure 56 Holding buffer of TMM OCC

4.2.7 Pulse Generator

The pulse generator shown in Figure 57 is to provide the pulses TS with sample and hold for Cz amplification, and two pulses TV and TP for two track-and-holds signals. In pulse generator, there are actually three short pulse generators as shown in Figure 58. In order to compensate the variation of Cz and Cf in TMM OCC, the short pulse is generated by using RC delay.

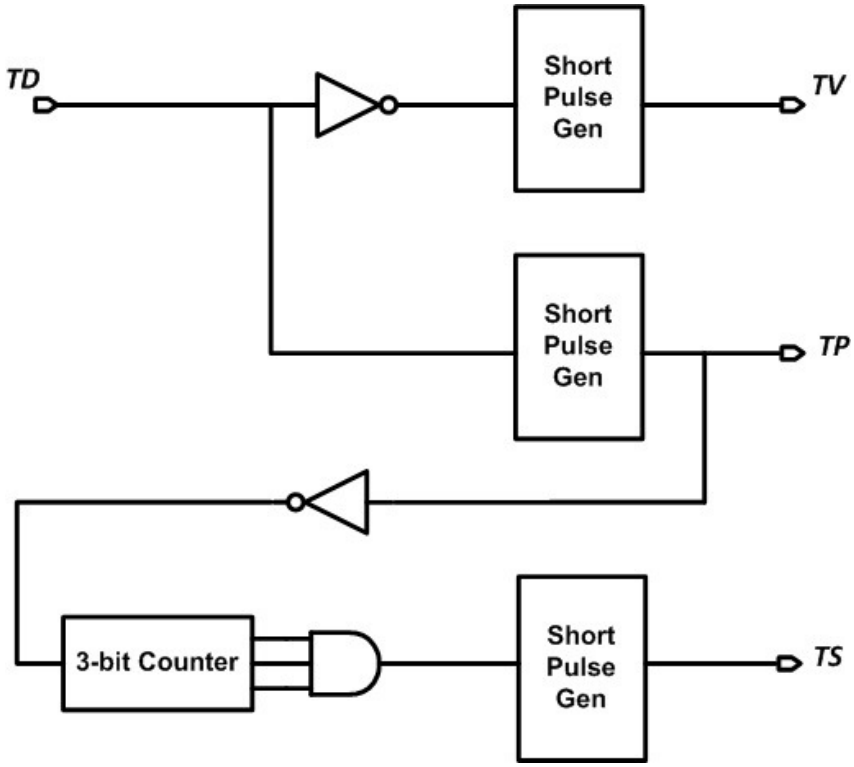


Figure 57 Schematics of pulse generator

The width of the generated short pulse is given by

$$\mathrm{TS} = R_s C_s ln \frac{V_{in}}{V_{in} - V_{th,inv}}$$

$$Where\ V_{in}\ is\ the\ input\ supply\ voltage\ and$$
$$V_{th,inv}\ is\ the\ threshold\ voltage\ of\ inverter$$

For accurate compensation, Rs value is chosen to be much larger than on-resistance of transistors connected to Rs in series. The value of Cs is also chosen much larger than the parasitic capacitances parallel connected to Cs. For proper selection of Rs and Cs, the on-resistances and the parasitic capacitances could be ignored when determining TS. That is reason why TS cannot be significantly short.

The solution to relax the limitation, TS can be generated with a proper duration per multiple switching periods, rather than one switching period, to increase TP effectively. As shown in Figure 57, TS has been generated per 2^3 switching periods by using a 3-bit counter.

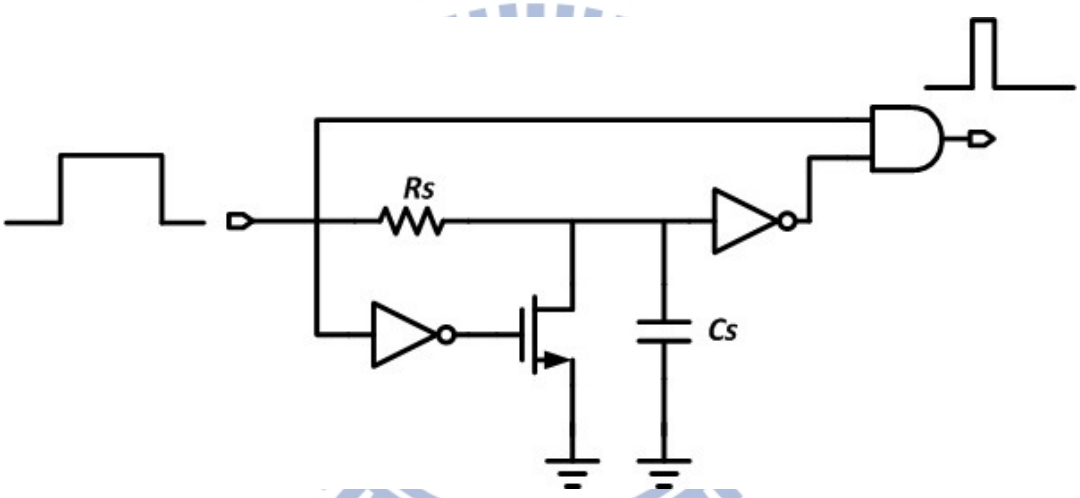


Figure 58 Short pulse generator

4.2.8 Compensation Worksheets

As shown in Table 7and Table 8, the worksheets of CMM compensation and TMM compensation are efficient to calculate the pole and zero. As parameters tuning in running the simulations, they also provide the helpful reference.

Table 7 CMM OCC worksheet

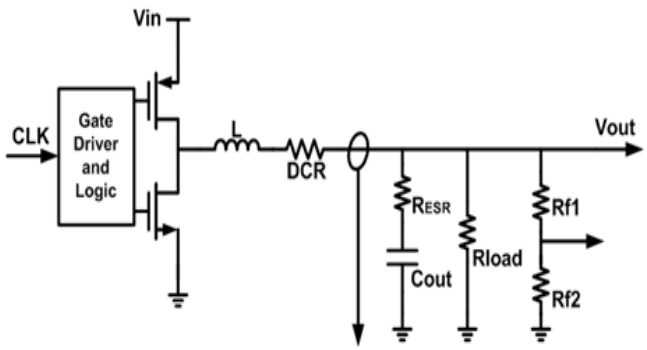
Converter Parameters

Input Voltage: VIN 5V
Output Voltage: VOUT 3V
Output current: 300mA ~ 800mA
Switching Frequency: F_{SW} 1MHz
Total Output Cap.: C_{OUT} 20µF
Total ESR: R_{ESR} 30mΩ
Inductor: L 2.2µH
Inductor DCR: DCR 0.1Ω
Control scheme: current mode
Compensation : On-chip CMM
Reference Voltage: V_{REF} 0.8V
Error Amp DC Gain 72.6dB

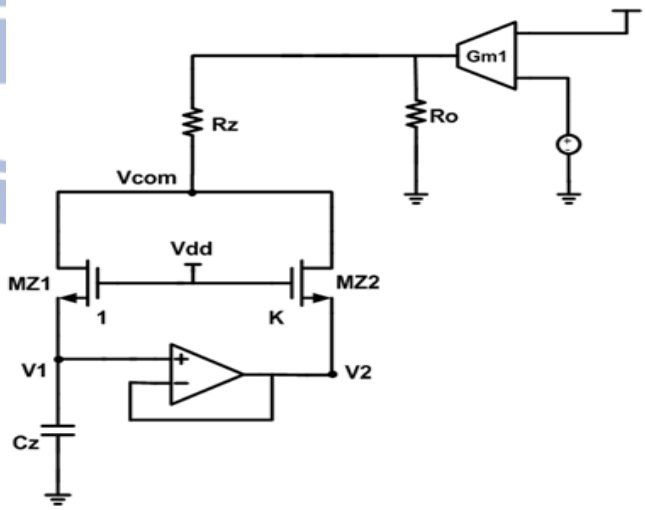
R_O= 9.5 MΩ
R_Z= 70 kΩ
C_Z= 10 pF
K = 15
r ($\frac{L}{W} = \frac{10\mu}{0.6\mu}$)
$MZ1 = 10r$
$MZ1 = \frac{2}{3}r$
Zero= 15.2 kHz
Pole= 112 Hz

(r: the resistance as transistor at linear region with length 10µm, width 0.6µm)

Synchronous current mode buck converter



CMM compensator



Pole and zero location

$$\text{Zero} \approx \frac{1}{KC_zR_z}$$

$$\text{Pole} \approx \frac{1}{KC_zR_O}$$

Table 8 TMM OCC worksheet

Converter Parameters

Input Voltage: VIN 5V

Output Voltage: VOUT 3V

Output current: 300mA ~ 800mA

Switching Frequency: F_{SW} 1MHz

Total Output Cap: C_{OUT} 20uF

Total ESR: R_{ESR} 30mΩ

Inductor: L 2.2uH

Inductor DCR: DCR 0.1Ω

Control scheme: current mode

Compensation : On-chip TMM

Reference Voltage: V_{REF} 0.8V

R_O= 9.5 MΩ

R_Z= 70 kΩ

C_Z= 1 pF

C_f = 0.1pF

C_P= 1fF

C_V= 1fF

$2^N = 8$

$\frac{TPe}{TS} \sim 20$

$\frac{g_{m2}}{g_{m1}} \sim 1$

Zero= 14.2 kHz

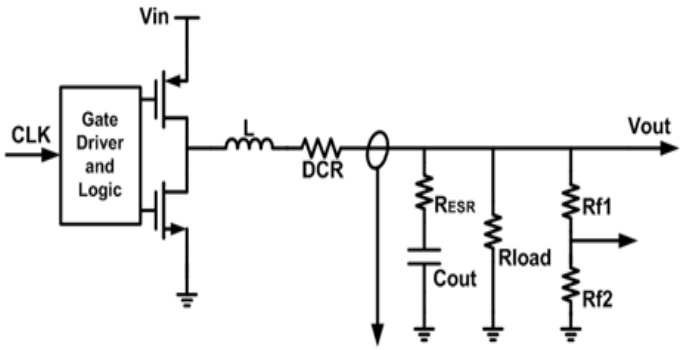
Pole1= 1.9 kHz

Pole2 > 25 MHz

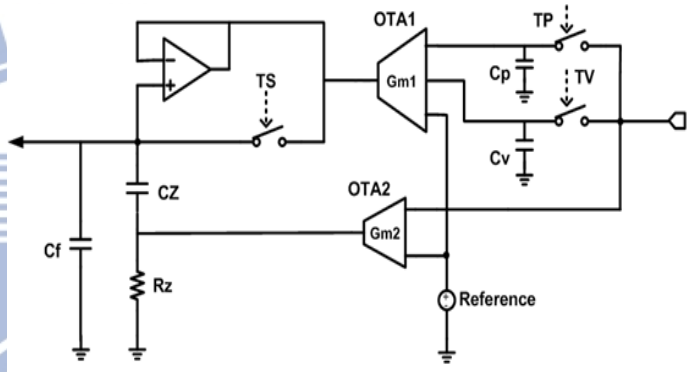
(N = 3, 3-bit counter)

TPe = 1/Fsw

Synchronous current mode buck converter



TMM compensator



Pole and zero location

$$\omega_Z = \frac{1}{\frac{g_{m2}}{g_{m1}}\frac{2^N TPe}{TS} C_Z R_Z}$$

$$\omega_{p1} = \frac{1}{\frac{2^N TPe}{TS}(C_Z + C_f)R_O}$$

$$\omega_{p2} = \frac{1}{\frac{C_Z C_f}{C_Z + C_f} R_Z}$$

4.3 Simulation Results

The section is to present the circuit implementations of CMM OCC and TMM OCC mainly including the major building blocks such as OTA, voltage follower, 3-input OTA, short pulse generator etc.

4.3.1 Frequency Response

Table 9 Schematics and parameters of PI off chip, CMM OCC, and TMM OCC

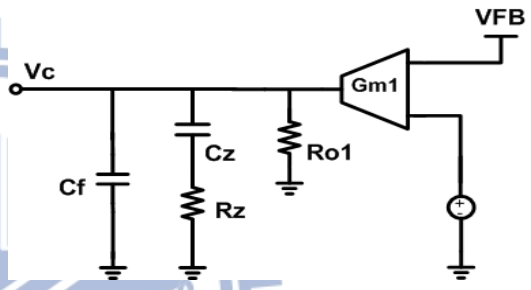
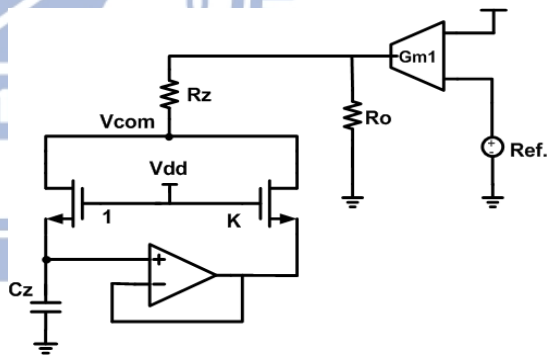
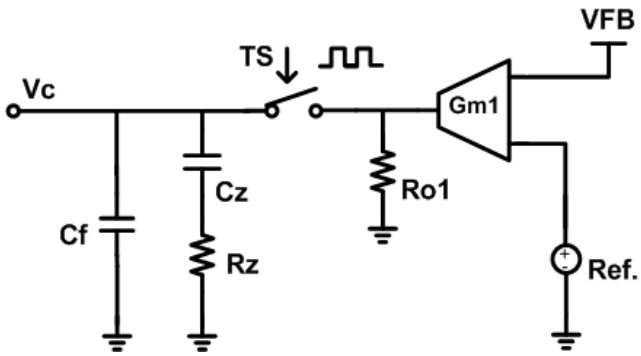
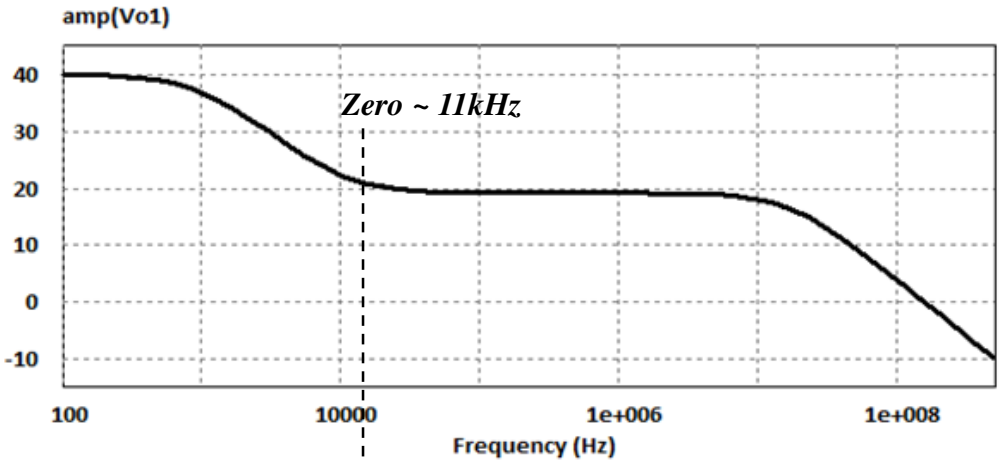
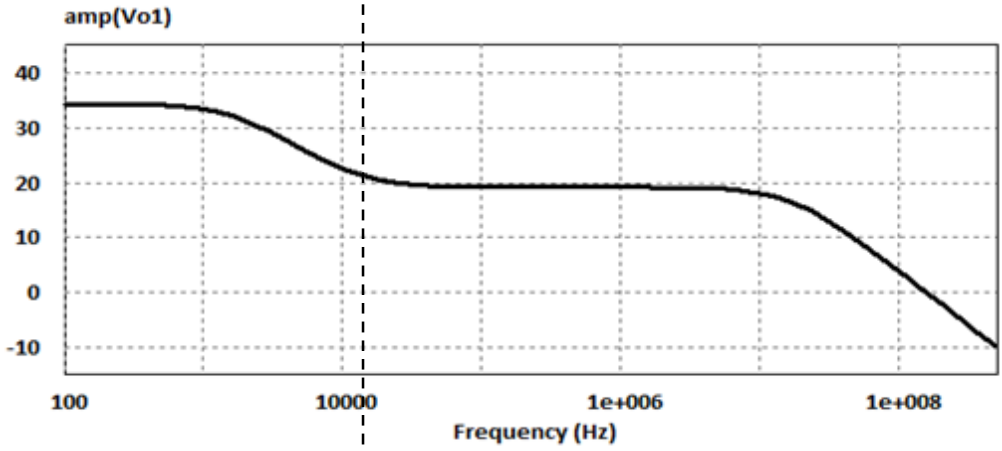
Parameters	Compensator
PI Compensation $\text{Zero} \approx \frac{1}{C_Z R_Z}$ $C_Z = 150p$ $R_Z = 100k\Omega$	
CMM OCC $\text{Zero} \approx \frac{1}{kC_Z R_Z}$ $C_Z = 10p,$ k = 15 $R_Z = 100k\Omega$	
TMM OCC $\text{Zero} \approx \frac{1}{\frac{g_{m2}}{g_{m1}}\frac{2^N TPe}{TS} C_Z R_Z}$ $C_Z = 1p,$ $\frac{g_{m2}}{g_{m1}}\frac{2^N TPe}{TS} = 150$ $R_Z = 100k\Omega$	

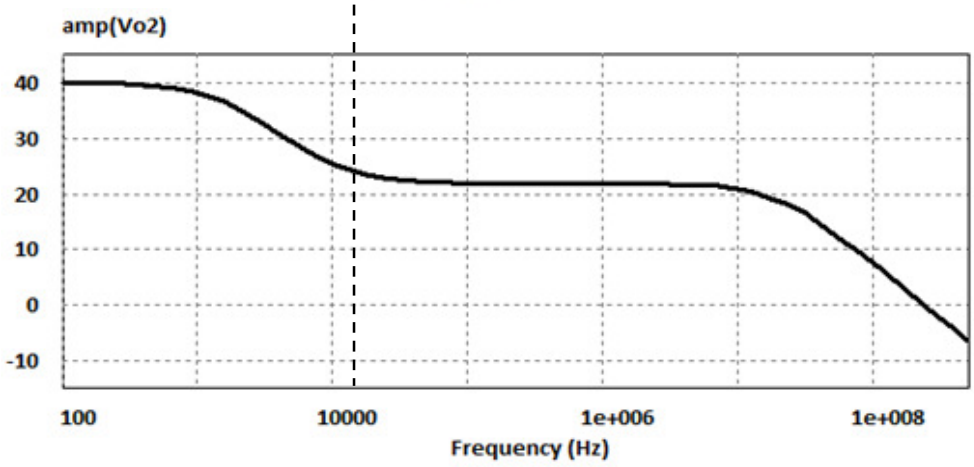
Table 9 lists the schematics and the formulas to calculate the parameters of PI, CMM OCC and TMM OCC. Bode plots of them as shown in Figure 59.



a. PI compensation Bode plot



b. CMM OCC Bode plot

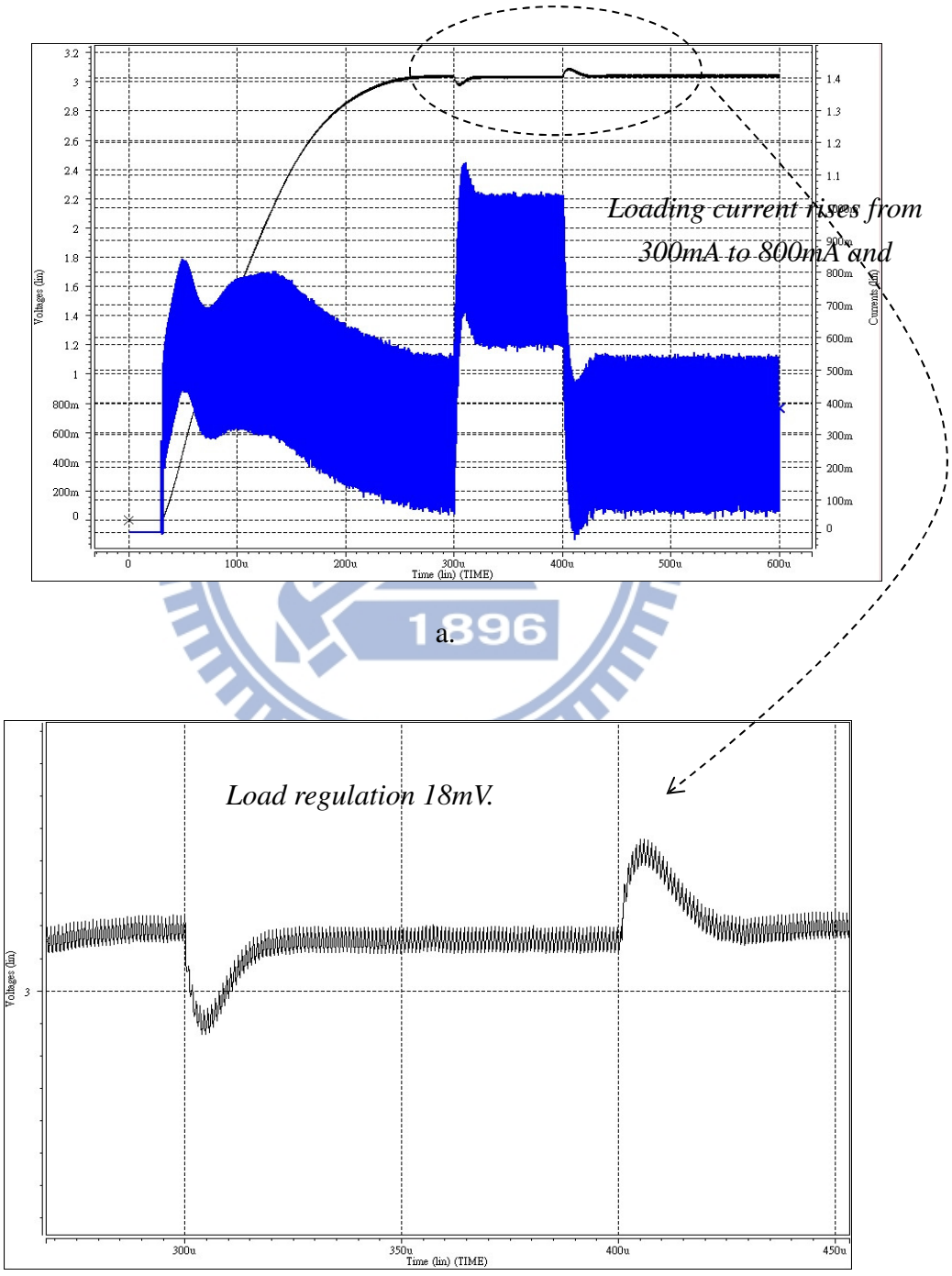


c. TMM OCC Bode plot

Figure 59 Bode plots of a. PI compensation, b. CMM OCC, and c. TMM OCC

4.3.2 Load Regulation

Figure 60 shows the load regulation performance of CMM OCC as loading current changed from 300mA to 800mA within 1μsec. As shown in (b) is the enlarged view of (a) the load regulation is 18 mV/A.

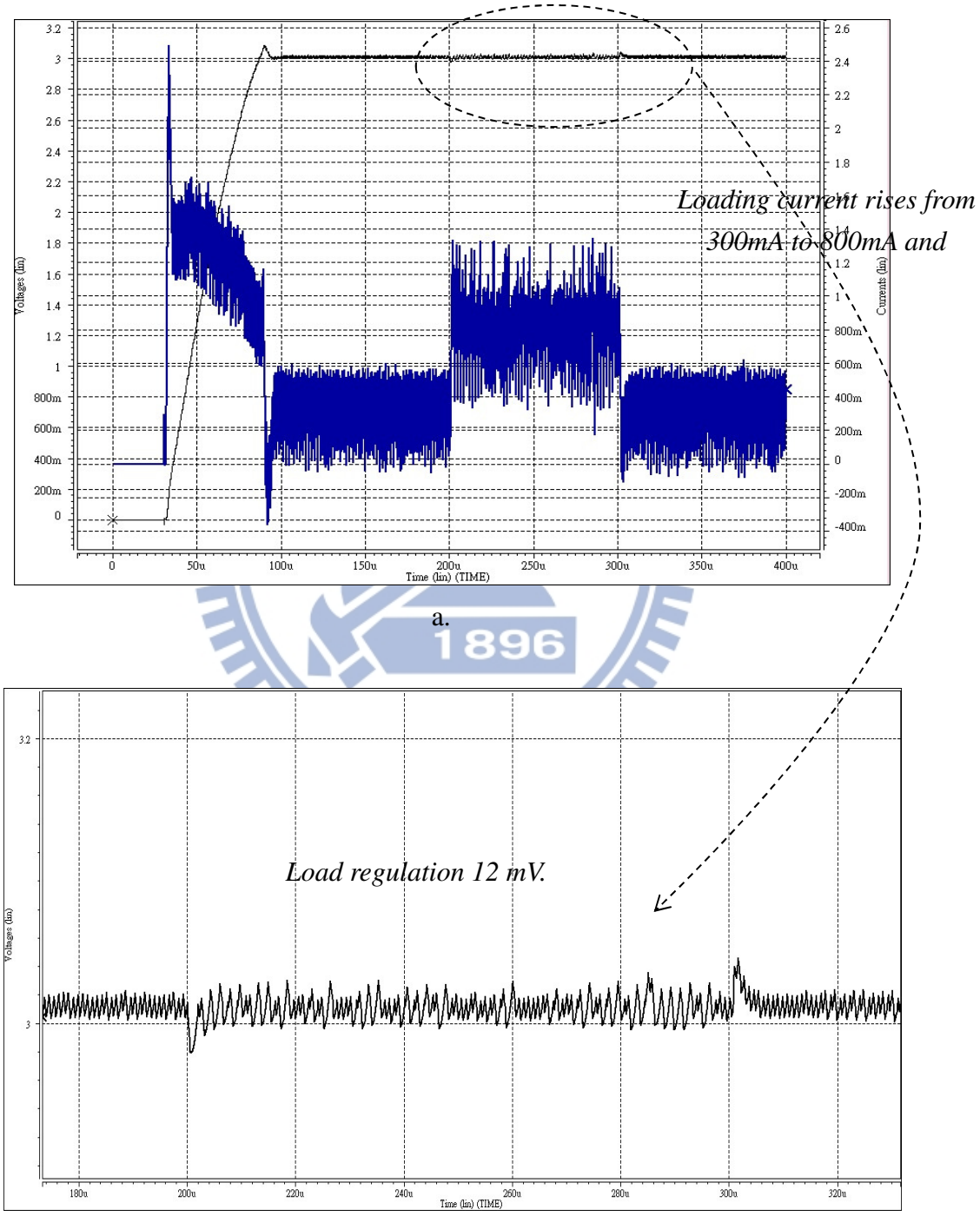


a.

b.

Figure 60 Load regulation of buck converter with on-chip CMM OCC

Figure 61 shows the load regulation performance of buck converter with TMM OCC as loading current changed from 300mA to 800mA within 1μsec. As shown in (b) is the enlarged view of (a) the load regulation is 12 mV/A.



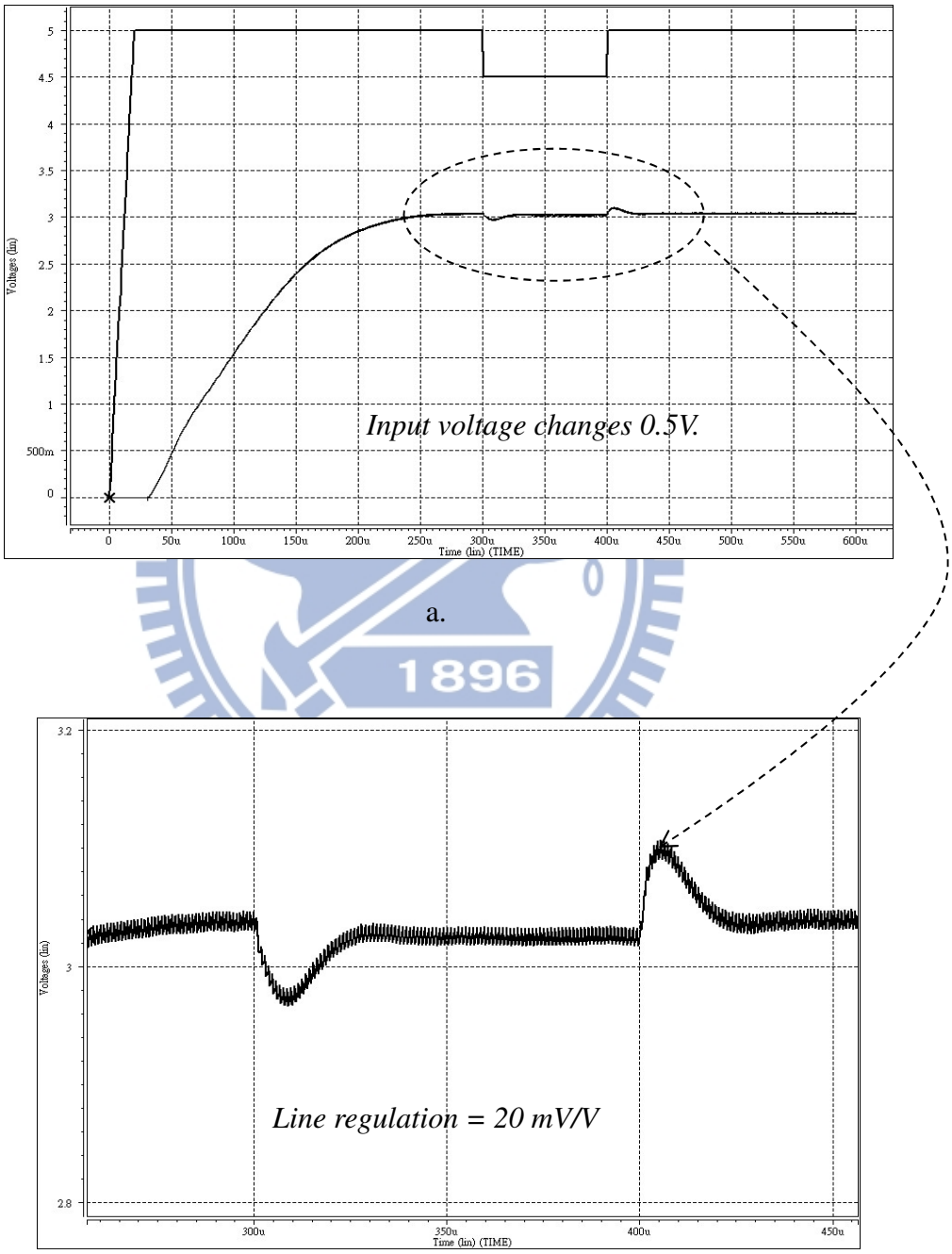
a.

b.

Figure 61 Load regulation of buck converter with TMM OCC

4.3.3 Line Regulation

Figure 62 shows the line regulation performance of buck converter with CMM OCC As shown in (b) is the enlarged view of (a) the line regulation is 20 mV/A.

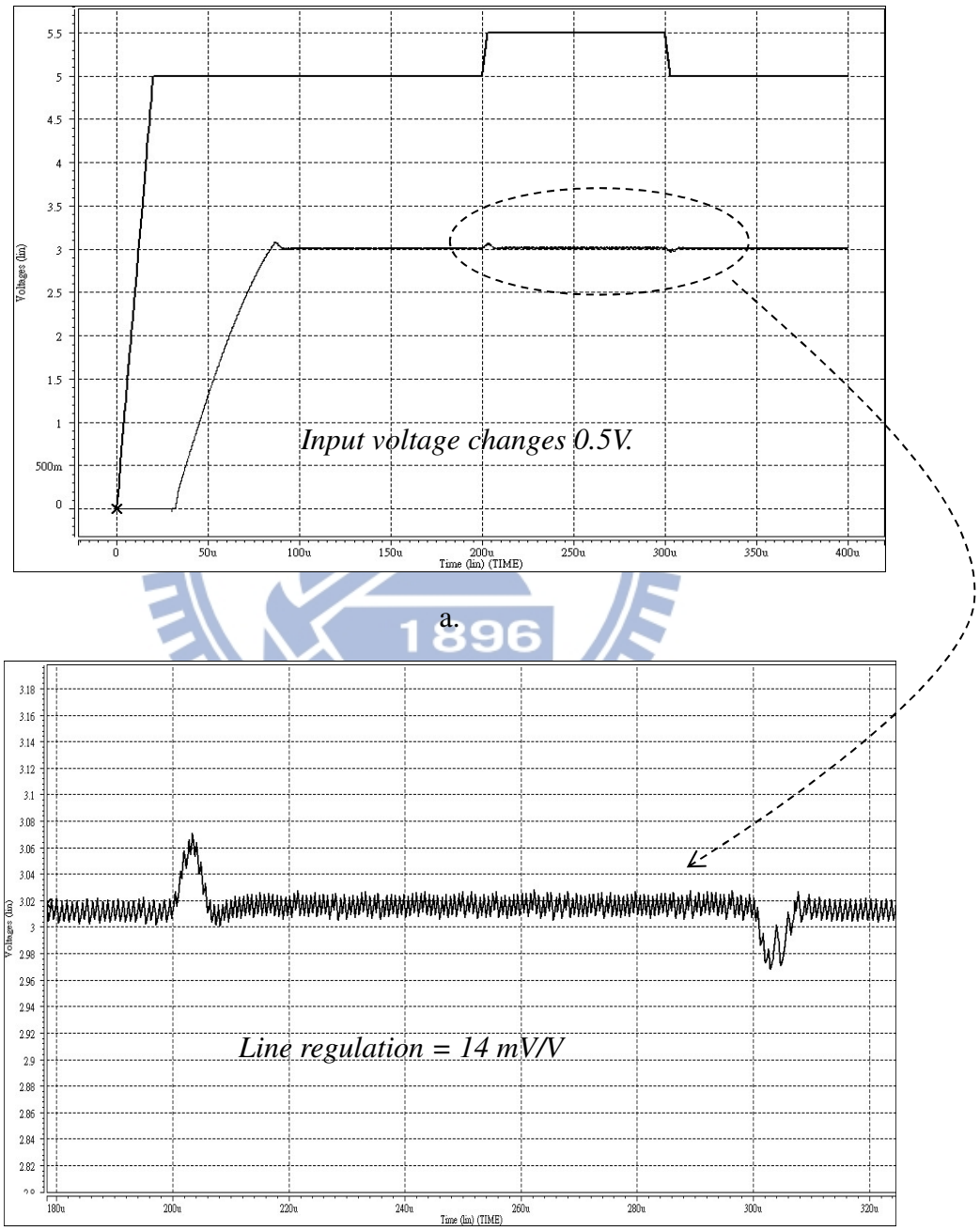


a.

b.

Figure 62 Line regulation of buck converter with CMM OCC

Figure 63 shows the line regulation performance of buck converter with TMM OCC. As shown in (b) is the enlarged view of (a) the line regulation is 24 mV/A. Compared the load and line regulation of CMM OCC with those of TMM OCC, they are only with a couple of mV difference from simulation results.



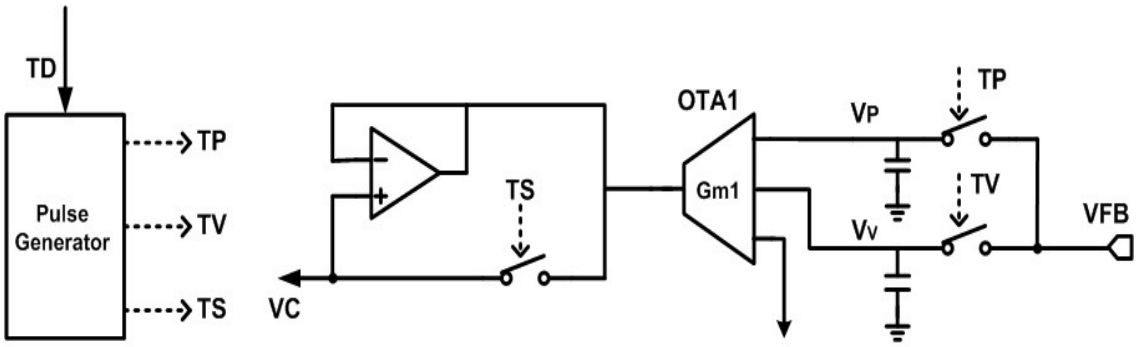
a.

b.

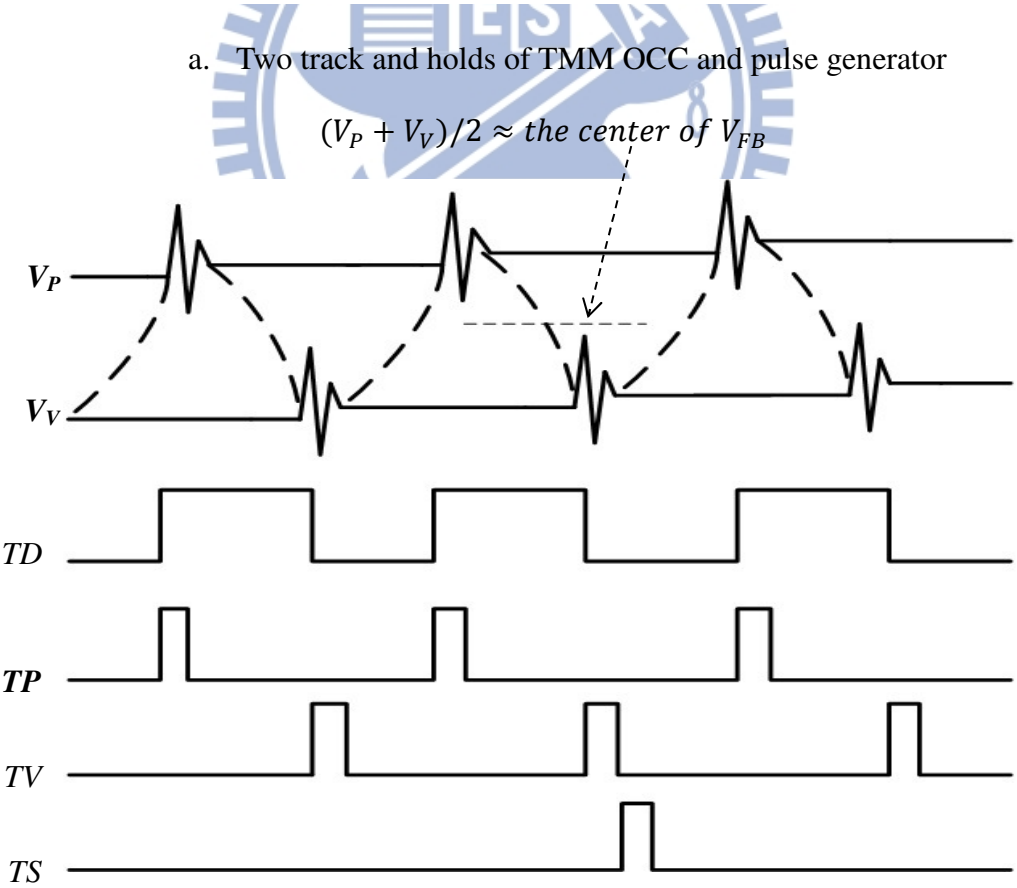
Figure 63 Line regulation of buck converter with TMM OCC

4.3.4 Track and Hold

As discussed in section 4.2.5 to solve the problem of locating the center value of feedback voltage, the operation wave forms of two track and holds, and the pulse generator are as shown in Figure 64 for the ideal timing diagrams to streamline the comparison with the simulation results in the following pages.



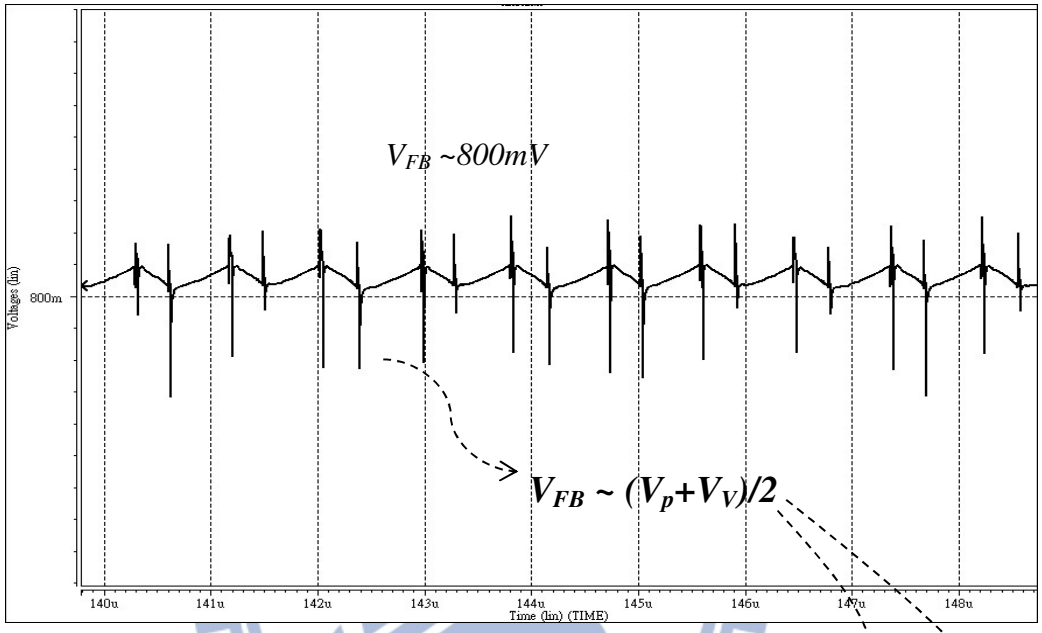
a. Two track and holds of TMM OCC and pulse generator



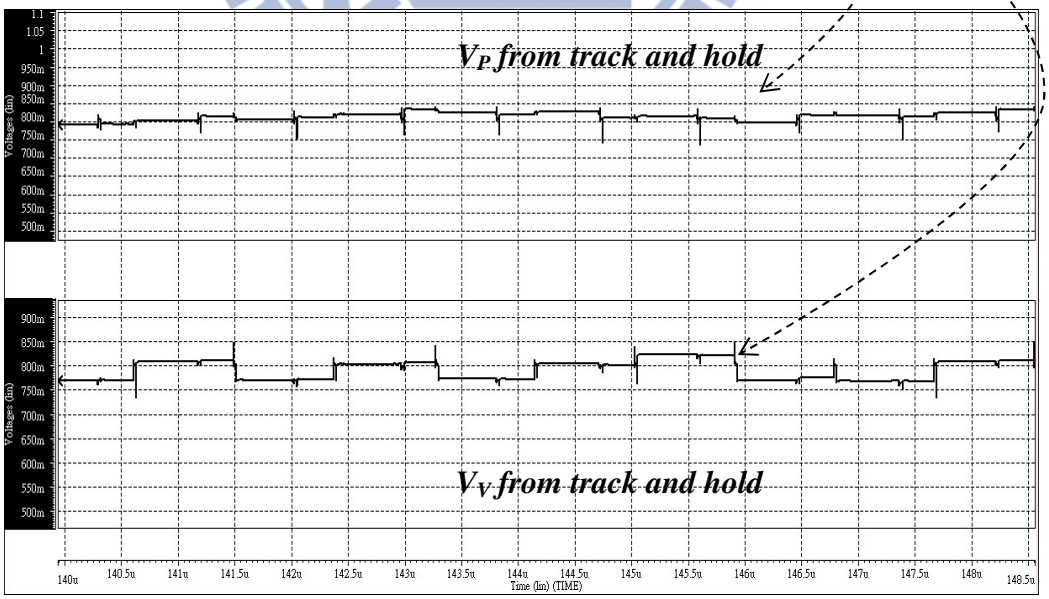
b. The wave forms from pulse generator

Figure 64 TMM OCC and operation wave forms of 3-input OTA

As shown in Figure 64 for the their ideal wave forms, the average of V_P and V_V is the center of the feedback voltage V_{FB}, and compared with Figure 65 for the wave forms from simulation of V_{FB}, V_P and V_V, they are working properly except for the spikes from the switching noise.



a. Feedback voltage wave form

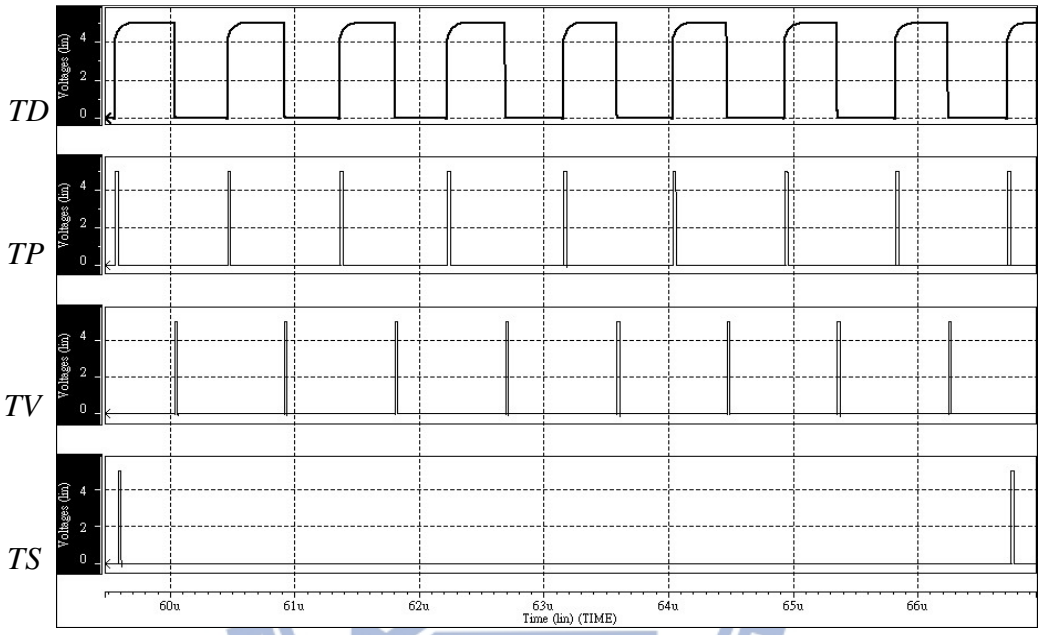


b. V_P and V_V wave forms

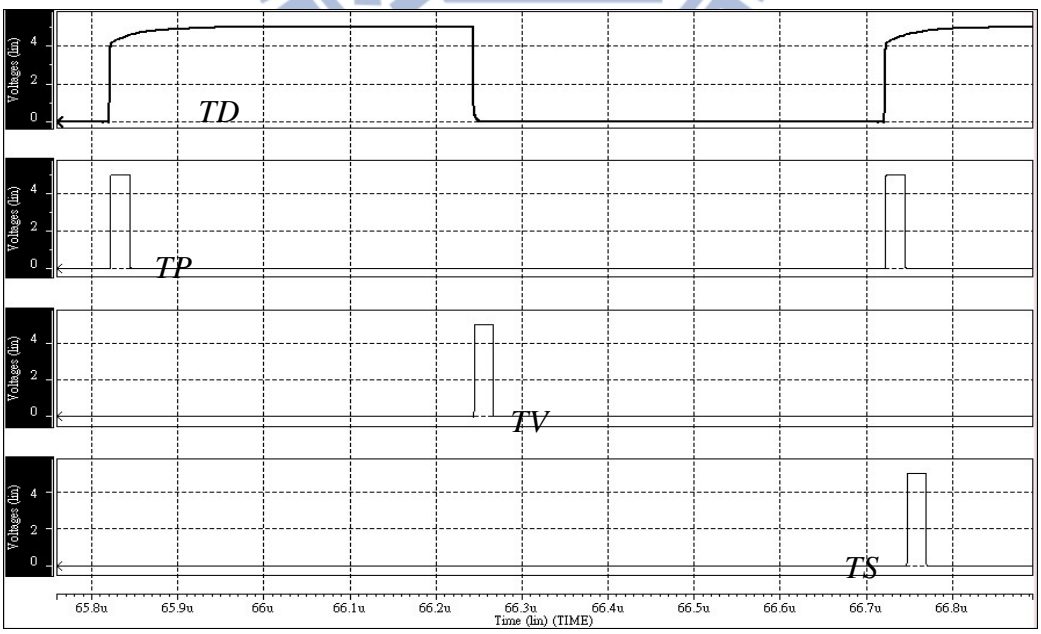
Figure 65 Two track and holds wave forms

4.3.5 Pulse Generator

The comparison of the wave forms TD, TP, TV, and TS in Figure 64 to the ones in Figure 66 from simulation results shows that the timing of these wave forms are in good shape to turn on and turn on appropriately.



a. The simulation wave forms from pulse generator



b. Enlarged view of wave forms

Figure 66 Pulse generator wave forms

4.4 CMM OCC and TMM OCC Comparison

In Table 10 it shows the comparisons between CMM OCC and TMM OOC techniques.

Table 10 Comparison of CMM OCC and TMM OCC

Compensation		CMM OCC	TMM OCC
Power stage	Supply voltage	5V	
	Output voltage	3V	
	Output current	300mA~800mA	
	Switching frequency	1MHz	
	Control scheme	Control mode control	
LC filter	Inductor-DCR	2.2μH-10mΩ	
	Capacitor-ESR	20μF-30mΩ	
Compensator	Technique	On-chip	On-chip
	Circuitry	OTA1	3-input OTA1
		Voltage follower	OTA2
		Dependence current source	Holding buffer
			Track and hold
			Sample and hold
			3-bit counter
		Cz 10pF	Cz 1pF
		Rz 70kΩ	Rz 70kΩ
	Load transient	comparable	comparable
	Line transient	comparable	comparable
	Output ripple	Low	High
	Sensitive to process variation	Less sensitive	More sensitive

Chapter5

Conclusions and Future Work

5.1 Conclusion

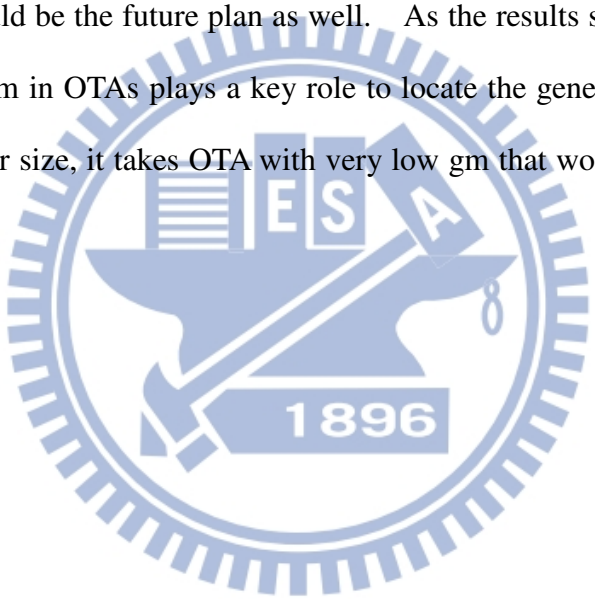
Considering DC-DC buck converter with voltage mode control, both off-chip Type III compensator and PID OCC are implemented. According to table 6 for the comparisons of two techniques, it is hardly possible for Type III compensator to be put into the chip because of compensation capacitors over hundreds of picofarad; however, it is more likely to integrate PID OCC for the capacitors needed are much smaller than those used in Type III. For PID OCC, the systematic procedure of parameters tuning for OTAs, capacitors and resistors, and the locations of the generated zeros is also validated. The compensation results of PID OCC are the same as that by Type III capable of stabilize the converter with crossover frequency at 200 kHz and phase margin 60°.

Concerning DC-DC buck converter with current mode control, although PI compensator provides the competent performance for system stability, the large compensation capacitor is still the major obstacle to the on-chip integration of compensator. CMM OCC and its counterpart techniques by time mode take the advantage of amplifying capacitance and succeed in downsizing the value of capacitor to make on-chip compensation for current mode buck converter feasible and compatible. The circuit level simulations of the major building blocks of two techniques are verified and analyzed accordingly. As the comparison shown in Table 10, it looks that the 1pF capacitor in TMM OCC is smaller than that in CMM OCC. On the other hand, it is also the potential risk for over all circuit reliability because it is so small that the demands for precision and stability of wafer process will be very challenging.

5.2 Future Work

As the concern mentioned in the section 5.1, in addition to complete simulations of each device corner based on SPICE model of the target process node as mentioned in section 4.1, the best way to make sure of it is to have the real silicon data. The splits for device corners such as design of experimental (DOE) could be therefore planned particularly for MiM capacitor which is the major device used in this thesis on compensation capacitor design.

With respect to the technique for voltage mode buck converter with PID OCC in chapter 2, the implementation is in the system level for their behavior verifications. A further study in the circuit level would be the future plan as well. As the results shown in section 2.4, the parameter tuning for gm in OTAs plays a key role to locate the generated zero position. To further reduce capacitor size, it takes OTA with very low gm that would be a critical issue on OTA circuit design.



Reference

[1] Vatche Vorperian, Fast analytical techniques for electrical and electronic circuits, Cambridge Books Online © Cambridge University Press, 2013

[2] "Technical Brief of Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators" Intersil, Dec. 2003

[3] Robert W. Erickson and Dragan Maksimovic, Fundamentals of Power Electronics, 2nd ed., Norwell, MA: Kluwer Academic Publishers, 2001.

[4] Christophe Basso, Switch-Mode Power Supplies Spice Simulations and Practical Designs, McGraw-Hill Inc., 2008

[5] Abraham Pressman, Switching Power Supply Design, McGraw-Hill Inc., 3rd ed., 2009

[6] Behzad Razavi, "Design of Analog CMOS Integrated Circuits". *McGRAW-HILL*, 2001

[7] Ned Mohan, Tore M. Undeland, William P. Robbins, "Power Electronics Converters, Applications, and Design". *JOHN WILEY & SONS*, 3rd edition, 2003

[8] Sanjaya Maniktala, Switching Power Supplies A to Z, Elsevier Science, 2006

[9] "Application Note AN-1043 Stabilize the Buck Converter with Transconductance Amplifier" International Rectifier, Jul. 2002

[10] Ray Ridley, "CURRENT MODE VOLTAGE MODE?" Switching Power Magazine October 2000

[11] Makharia A., Rincon-Mora, G.A. "Integrating Power Inductors onto the IC-SOC Implementation of Inductor Multipliers for DC-DC Converters". *IECON '03. The 29th Annual Conference of the IEEE*, Vol. 1, pp.556-561, 2-6 NOV, 2003.

[12] Rincon-Mora, G.A. "Active capacitor multiplier in Miller-compensated circuits". *Solid-State Circuits, IEEE Journal*, Vol. 35, pp.26-32, Jan. 2000.

[13] Cheung Fai Lee and Philip K. T. Mok, "A Monolithic Current-Mode CMOS DC–DC Converter With On-Chip Current-Sensing Technique," *IEEE Journal of Solid-State*

Circuits,vol. 39, no. 1 Jan. 2004

[14] Patrick Y. Wu, Sam Y. S. Tsui, and Philip K. T. Mok, Area- and Power-Efficient Monolithic Buck Converters With Pseudo-Type III Compensation, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 8, AUGUST 2010.

[15] Ke-Horng Chen, Chia-Jung Chang, and Te-Hsien Liu, "Bidirectional Current-Mode Capacitor Multipliers for On-Chip Compensation" IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 23, NO. 1, JANUARY 2008

[16] Chia-Jung Chang and Ke-Horng Chen, "Bidirectional Current-Mode Capacitor Multiplier in DC-DC Converter Compensation" Proceedings of the 9th International Database Engineering & Application Symposium (IDEAS'05)

[17] Ke-Horng Chen, Hong-Wei Huang, and Sy-Yen Kuo "Fast-Transient DC–DC Converter With On-Chip Compensated Error Amplifier" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 54, NO. 12, DECEMBER 2007

[18] Hong-Wei Huang, Hsin-Hsin Ho, Chieh-Ching Chien, Ke-Horng Chen, Gin-Kou Mat, and Sy-Yen Kuo, "Fast Transient DC-DC Converter with On-Chip Compensated Error Amplifier" Solid-State Circuits Conference, 2006. ESSCIRC 2006. Proceedings of the 32nd European.

[19] Yu-Huei Lee,Shao-Chang Huang,Shih-Wei Wang,and Ke-Horng Chen, "Fast Transient (FT) Technique With Adaptive Phase Margin (APM) for Current Mode DC-DC Buck Converters" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 10, OCTOBER 2012

[20] Hyun-Hee Park, Young-Jin Woo and Gyu-Hyeong Cho "A Fully Integrated Wide-band PID Controller with Capacitor-Less Compensation for Step-Down DC-DC Converter" Circuits and Systems (ISCAS), 2011 IEEE International Symposium

[21] Sung-Wan Hong, Tae-Hwang Kong, Sang-Hui Park, Changbyung Park, Seungchul Jung, Sungwoo Lee, and Gyu-Hyeong Cho "High Area-Efficient DC-DC Converter With High Reliability Using Time-Mode Miller Compensation (TMMC)" IEEE JOURNAL OF

SOLID-STATE CIRCUITS, VOL. 48, NO. 10, OCTOBER 2013.

[22] Dr. Ke-Horng Chen, “DC to DC Converter Integrated Circuit Design Class Hand-Out” NCTU EE 2011 Spring

[23] Dr. Ke-Horng Chen, “Advanced Power Management Integrated Circuit Design Class Hand-Out” NCTU EE October 2012

[24] S. FRANCO, “Design with operational amplifiers and analog integrated circuits,” Mcgraw-Hill International Editions, Second Edition, 1998

[25] Design Manual of VIS 0.25um CMOS Mixed-Signal 1P5M (single poly, 5 metal layers), silicide, Al technology.

[26] SPICE Model of VIS 0.25um CMOS Mixed-Signal 1P5M (single poly, 5 metal layers), silicide, Al technology.