國 立 交 通 大 學

電子物理學系

博 士 論 文

非對稱金氧半場效電晶體及無接面多晶矽薄膜電晶體的研究

A Study on Asymmetrical MOSFETs and Junctionless Polycrystalline Silicon Thin-Film Transistors

研 究 生：蔡子儀

指導教授：趙 天 生 博士

林 鴻 志 博士

黃 調 元 博士

中華民國一零三年一月

非對稱金氧半場效電晶體及無接面多晶矽薄膜電晶體的研究

A Study on Asymmetrical MOSFETs and Junctionless Polycrystalline Silicon Thin-Film Transistors

指導教授：趙天生 博士
林鴻志 博士
黃調元 博士

Advisors：Dr. Tien-Sheng Chao
Dr. Horng-Chih Lin
Dr. Tiao-Yuan Huang

研 究 生：蔡子儀

Student：Tzu-I Tsai

國 立 交 通 大 學

電子物理學系

博士論文

A Dissertation

Submitted to Department of Electrophysics
College of Science
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electrophysics
December 2013
Hsinchu, Taiwan, Republic of China

中華民國一零三年一月

非對稱金氧半場效電晶體及無接面多晶矽薄膜電晶體的研究

研究生：蔡子儀　　　　　　　　　　　　　　指導教授：趙天生 博士
林鴻志 博士
黃調元 博士

國立交通大學

電子物理學系

摘　　要

在本論文中，我們利用傳統 I-line 步進機發展一新穎雙重微影技術，可將閘極長度微縮至 80 奈米；而後改良此雙重微影製程可進一步縮小其線寬以製作出次 60 奈米線寬圖形，並將之用於 45 奈米 n 型通道金氧半場效電晶體的製作。此技術與一般大學實驗室常用的方法，例如電子束直寫系統與光阻灰化技術進行比較，包括臨界尺寸(CD)均勻性、產率、線邊緣粗糙度(LER)、最小線寬等特性，作定量上的比較。憑藉所提出的 I-line 雙重微影技術，我們也研製出對稱與非對稱源汲極元件，並討論其電性特性與相關的可靠度議題。

我們發現，雖然對稱暈邊(halo)結構相較於對照組能有效降低 10^4 倍次臨界漏電及改善短通道效應，但同時造成嚴重的逆短通道效應與犧牲 25%電流驅動力。為了改善這項缺失，我們提出非對稱暈邊結構製程以解決上述的矛盾。相較於對稱暈邊結構，非對稱暈邊結構貢獻了 7.8% 的轉導增益以及 15%電流驅動力增益另外在可靠度議題方面，我們發現暈邊摻雜會增加在閘極邊緣下汲極的側向電場強度，進而使熱載子退化效應變得更嚴重。藉由非對稱暈邊結構，我們可以減緩熱載子退化效應，其臨界電壓偏移為 0.21 伏特，對稱式結構則為 0.32 伏特的臨界電壓偏移。此外，我們也藉由探討熱載子測試前後的閃爍雜訊特性來評估暈邊摻雜對元件的影響，發現汲極端暈邊摻雜也會造成元件雜訊劣化。

另一方面，我們研製出各式不需佈植製程的無接面元件，包含多閘極組態奈

米線場效電晶體、三維多層堆疊奈米線場效電晶體、多閘極組態奈米線 SONOS 記憶體元件、以及平面式薄膜電晶體以探討其操作機制。藉由導入臨場磷摻雜多晶矽薄膜作為上述無接面元件的通道及源汲極材料以實現無佈植技術的製程方式。由無接面奈米線場效電晶體的電性結果發現，足夠小的奈米線通道截面對於關閉 n 型重摻雜通道與得到優異電流開關比值(在閘極電壓為 2 伏特下有 5.2×10^6 倍)是非常重要的。此外，由於較低的源汲極串聯阻值與通道阻值，無接面元件具有較高的電流驅動表現約為反轉式元件的 1.75 倍。

接下來，相較於反轉式元件而言，無接面奈米線 SONOS 記憶體元件展現較快的寫入速度與不錯的資料保存能力，而相當的抹除速度與毫不遜色的記憶窗口也被記錄。另一方面，摻雜濃度與閘極組態對於無接面記憶體元件的效應也一併探討。由電性與記憶體特性結果發現對於高性能 SONOS 應用方面而言，無接面多晶矽奈米線記憶體元件的摻雜濃度必須謹慎的調整。簡而言之，就低成本與極高密度非揮發記憶體應用而言，所提出的無接面奈米線 SONOS 技術是相當有潛力的。

最後，我們研製 n 型平面式超薄型無接面多晶矽薄膜電晶體以探討對射頻與低頻雜訊之影響。在汲極電壓 2 伏特偏壓下無接面元件展現出優異的截止頻率(3.36 GHz)與最大共振頻率(7.37 GHz)以實現低電壓操作的應用。在低頻雜訊方面，相較於對照組的反轉式元件，無接面元件改善了低頻雜訊以及達到較高的信號雜訊比。此外，我們也建立了無接面元件的小訊號模型並且對照實驗與模擬結果以驗證其準確性，由對照的結果發現所建立的小訊號模型是成功運作的。

A Study on Asymmetrical MOSFETs and Junctionless Polycrystalline Silicon Thin-Film Transistors

Student：Tzu-I Tsai

Advisors：Dr. Tien-Sheng Chao
Dr. Horng-Chih Lin
Dr. Tiao-Yuan Huang

Department of Electrophysics
National Chiao-Tung University

Abstract

In this dissertation, we have developed a novel double-patterning (DP) technique for generation of gate patterns with gate length down to 80 nm using only a conventional I-line stepper. With a modification in the process steps, this DP technique can further shrink the patterns down below sub-60 nm and have been employed to fabricate 45nm nMOSFETs. This technique is also compared with alternative methods, such as electron-beam direct writing and photoresist-ashing scheme which are often adopted in the university-based laboratories, from the perspectives of the uniformity of critical dimension (CD), throughput, line edge roughness (LER), and minimum line width. Moreover, with the aid of the proposed I-line DP technique, several symmetrical or asymmetrical S/D devices were fabricated and characterized.

We found that, although the symmetrical halo-doping structure helps reduce the subthreshold leakage by four orders of magnitude over the control and improve the short-channel effects (SCEs), severe reverse-short-channel effect (RSCE) and degenerate current drivability (25% output current degradation as compared with the control) are compromised at the same time. To address this issue, the implementation of asymmetrical halo structure was proposed to relieve such a dilemma. In contrast with symmetrical halo structure, the Asymmetric Halo split shows a 7.8% higher transconductance and a 15% larger driving current. For reliability issue, we found that the drain-side halo doping is the primary culprit of hot-carrier (HC) degradation due to the increased peak lateral electric field. The aggravation of HC degradation is alleviated with the Asymmetric Halo split, while the Symmetric Halo split exhibits threshold

voltage shift of 0.32 V and the Asymmetric Halo split performs that of 0.21 V after 5000-second of hot-electron stressing. Furthermore, we have evaluated the impact of halo on device performance by investigating the flicker noise (1/f) characteristics before and after the hot-carrier stress, indicating that drain-side halo doping. deteriorates low-frequency noise as well.

Concurrently, we have fabricated and characterized junctionless (JL) polycrystalline silicon-based thin-film transistors (TFTs) of various configuration, including multiple-gated nanowire (NW) field-effect transistors (FETs), 3-D multilayer-stacked NWFETs, multiple-gated NW silicon–oxide–nitride–oxide–silicon (SONOS) memory cells, and planar TFTs with an implant-free technique. The results indicate that a sufficiently small cross section of the channel, less than 20 nm × 20 nm, is essential to switch off the device and obtain a superior on-to-off current ratio of 5.2×10^6 at $V_G = 2$ V. Moreover, JL devices exhibit boosted on-state behavior (a 1.75 times output current value over the inversion-mode counterpart), as ascribed to lower S/D series resistances and channel resistances.

The fabricated NW SONOS memory devices with JL scheme depict faster programming speed and better data retention behavior, while a comparable erase window and similar erasing efficiency to the inversion-mode (IM) counterparts are also observed. On the other hand, the effects of doping concentration and gate configuration implemented with JL scheme have also been investigated. From the results of the electrical characterizations and memory properties, the doping concentration of the JL poly-Si NW device should be carefully optimized for high-performance SONOS applications.

We've also fabricated and characterized n-type planar ultrathin JL poly-Si TFTs with emphasis on RF and low-frequency noise (LFN) performance. The 0.2-μm JL device shows remarkable f_t and f_{max} of 3.36 and 7.37 GHz, respectively, at a V_D of 2 V. In addition, the JL devices improve the LFN and achieves higher signal-to-noise ratio as compared with those of the IM devices. Finally, we have derived a small-signal model for the fabricated JL devices and verified its accuracy by comparing the *S*-parameters.

Acknowledgement

首先要感謝指導教授趙天生博士、林鴻志博士與黃調元博士。三位老師在專業領域上的知識，對於研究的熱誠，嚴慎的做事態度與強烈追求新知的精神是學生由衷景仰與遵循的楷模。無論是日常生活或是專業研究領域，老師們常給予學生種種的指導、教誨與關心，老師們的所有建議學生都謹記在心，於此誠摯感謝老師們的一切付出。

本論文的完成也要感謝口試委員—胡振國教授、李明逵教授、鄭晃忠教授、賴朝松教授、蘇彬教授授—所給予的寶貴建議與指導。

接下來我要感謝先進元件技術實驗室的所有成員在生活與實驗上所提供的各種協助。感謝李耀仁博士、盧文泰博士、呂嘉裕博士、李明賢博士、盧景森博士、徐行徽博士、陳威臣博士、林哲民博士、張凱翔學長、黃健銘學長等等早期辛苦為實驗室奠定的基礎，由量測系統的建立到許多便利的量測技術以及實驗室制度等，正所謂前人植樹後人乘涼，學弟在此由衷感謝前輩們的付出。感謝蘇俊榮博士在奈米線元件上深厚的功力與經驗得以順利完成本論文無接面奈米線元件相關的討論。感謝曾經一起努力熬夜爆肝做實驗與趕國科會計畫的博班夥伴們—政頤(阿毛)、嘉豪(maca)、克慧(Kerker)、博璿(阿莫)、嘉文(Albert)、榮哲、明鴻、金儀與你們共事是我的榮幸，還有碩士班的學弟妹們—冠樟、忠祐、政雄、漢仲、陳玲、小強、SRJ、Gay 綸、敏峰、家維、博翔、段凱、禹伶、孝雄、廷耀、靜玲、信宏,族繁不及備載，謝謝你們在研究實驗上的協助與生活的交流，為研究生涯增添不少樂趣。

另外還要感謝國家奈米元件實驗室與交大奈米中心所有的工作人員，提供如此便利與完善的環境，雖然設備有時會故障但優秀的工程師能快速的回復狀況，使得實驗最終能夠順利的進行。感謝國家奈米元件實驗室的林家毅工程師在 FIB 上的鼎力相助、薛富國工程師在蝕刻上的協助、鄭旭君工程師在微影上的協助、陳柏源工程師在高頻量測上的協助、陳坤明博士在 RF 相關研究的討論，以及製程服務組的幫忙—耘木走、明娟、家如、李姊、琇芝、婉貞、庭瑋、台鳳、子綾、宋爺、蔣姊，即使我離開了，精神永遠與你們同在，最後一年的低潮期中感謝你們與實驗室學弟妹的開導與鼓勵讓我完成了這本論文。

最後特別要感謝我的父母親 蔡文全先生與邱昭綾女士，對我從小到大無怨無悔的付出與照顧，該是您老享清福的時候，兒子終於能夠回饋您們的養育之恩。感謝兩位姐姐如涵、依珊，在我求學過程中的關懷與照顧。

謹以此論文獻給我最敬愛的家人、朋友以及敬重的師長們。

蔡　子　儀

誌於風城交大

2014 年 1 月

Contents

Abstract (Chinese)……………………………………………………………….. i

Abstract (English)……………………………………………………………... iii

Acknowledgement (Chinese)……………………………………………………. v

Contents ……………………………………………………………………….. vii

Table Captions ……………………………………………………………………… x

Figure Captions ……………………………………………………………….. xi

Chapter 1 Introduction…………………………………………………………. 1

1.1 General Background……………………………………………………… 1

1.1-1 Double Patterning Technique ……………………………………….. 1

1.1-2 Junctionless Technique……………………..……………………….. 2

1.1-3 Asymmetric S/D Devices...……………………..……………………... 2

1.1-4 Flicker Noise Characteristics………...……………………………….. 4

1.1-5 Radio Frequency Techniques………………..………………………… 6

1.2 Motivation…………………………………………………………………... 7

1.3 Thesis Organization ………………………………………………………… 8

References ………………………………………………………………………… 11

Chapter 2 A Simple Method for Sub-100 nm Pattern Generation with I-line Double Patterning Technique…………………………..……………. 25

2.1 Introduction ………………………………………………………………… 25

2.2 Development of Double Patterning with I-line Stepper…….…………………… 26

2.3 Devices Fabrication ...…...…….…..…………………… 27

2.4 Results and Discussion ……………………………………………………... 28

2.4-1 End Point Detection Issue …………………..…………………………. 28

2.4-2 Feasibility of Double Patterning Technique .....…………………………. 29

2.4-3 Device Characteristics ……………...…………………………………. 31

2.5 Summary ……………………………………………………………………… 33

References ……………………………………………………………………… 34

Chapter 3 A Comparison of Nano-scale Patterning Techniques…..…………………. 54
3.1 Introduction …………………………………………………………………. 54
3.2 Lithographic Experiments ..…………………………………………………. 56
3.2-1 Brief Illustrations of Lithographic Experiments ……………………….. 56
3.2-2 Experiments of Electron Beam Systems ………………………………. 56
3.2-3 Experiments of I-Line Stepper with PR Ashing Method ………………… 56
3.2-4 Experiments of I-Line Stepper with Double Patterning Method ………… 57
3.2-5 Experiments of I-Line Stepper with Modified Double Patterning Method. 58
3.3 Devices Fabrication …………………………………………………………. 59
3.4 Results and Discussion ……………………………………………………... 60
3.4-1 Performance Comparison of Lithographic Techniques ..………………… 60
3.4-2 Devices Characteristics ………………..………………………………. 61
3.5 Summary ……………………………………………………………………. 64
References …………………………………………………………………….. 65

Chapter 4 Fabrication of Sub-100 nm Devices with Asymmetrical Source/Drain Using I-line Double Patterning Technique………………………………….. 82
4.1 Introduction …………………………………………………………………. 82
4.2 Devices Fabrication …………………………………………………………. 84
4.3 Measurement Setup …………………………………………………………. 86
4.3-1 Electrical Measurement Setup ……………………………..…..……… 86
4.3-2 Hot-Carrier Stress Measurement Setup ……………….............……… 86
4.3-3 Charge Pumping Measurement Setup………………...................……… 87
4.3-4 Flicker Noise Measurement Setup…………………………..…...……... 88
4.4 Results and Discussion ……………………………………………………... 88
4.4-1 Electrical Characteristics of TFETs…………………….……………… 88
4.4-2 Electrical Characteristics of nMOSFETs…………………...………….. 91
4.4-3 Hot-Carrier Stress (HCS) of Asymmetrical Halo nMOSFETs…………... 93
4.4-4 Lateral Distribution of Interface Trap Density of Asymmetrical Halo nMOSFETs……………………………………………………………………….. 95
4.4-5 Flicker Noise Characteristics on Asymmetrical Halo nMOSFETs……….. 96
4.5 Summary ……………………………………………………………………. 100
References …………………………………………………………………….. 102

Chapter 5 Fabrication and Characterization of Junctionless Devices Using an Implant-free Technique……..…………………….............................. 135
5.1 Introduction …………………………………………………………………… 135
5.2 Device Fabrication and Experiment…………………………………………… 137
5.2-1 Junctionless NWFETs ………………..…………………………………... 137
5.2-2 Junctionless SONOS Nonvolatile memory Devices……………………..... 139
5.2-3 Three-Dimensional Multilayer-Stacked Junctionless NWFETs…….….…... 140
5.2-4 Planar Junctionless TFTs……………..…………………………………... 141
5.3 Measurement Setup………………………………………….……………………... 142
5.3-1 Electrical Measurement Setup………………………………………….. 142
5.3-2 S-Parameter Measurement Setup………………………………………. 142
5.3-3 De-embedding Process……………………………….…………………... 143
5.4 Results and Discussion …………………………………………………………... 144
5.4-1 Electrical Characteristics of Junctionless NWFETs... …………………… 144
5.4-2 NVM Characteristics of JL NW SONOS Devices ……………………… 147
5.4-3 Electrical Characteristics of 3-D Multilayer-Stacked JL NWFETs……… 151
5.4-4 RF Characteristics and Small-Signal Modeling of Planar JL TFTs……… 152
5.5 Summary …………………………………………………………………… 155
References ……………………………………………………………………… 157

Chapter 6 Conclusions and Suggested Future Works……………………………… 195
6.1 Conclusions …………………………………………………………………… 195
6.2 Suggestions for Future Work ………………………………………………….. 196
References ……………………………………………………………………… 198

Vita (Chinese)……………………………………………………………………….. 199
Publication list………………………………………………………………………. 200

Table Captions

Chapter 2

Table 2-1 Overall implantation conditions used in the n-MOSFET fabrication. 36

Table 2-2 Overall implantation conditions used in the p-MOSFET fabrication. 36

Table 2-3 Specifications of Canon FPA-3000i5+ Stepper. 36

Chapter 3

Table 3-1 Overall implantation conditions used in the device fabrication. 67

Table 3-2 Comparisons of electron beam tools and I-line processes........................67

Chapter 4

Table 4-1 Overall implantation conditions used in the device fabrication of TFETs. 106

Table 4-2 Overall implantation conditions used in the device fabrication of nMOSFETs..106

Chapter 5

Table 5-1 Hall measurement results of poly-Si films. 162

Table 5-2 Splits of JL NW SONOS devices with various gate configuration and channel doping. 162

Table 5-3 Performance comparison of the fabricated JL and IM poly-Si TFTs with W/L=8 μm/0.4 μm..162

Table 5-4 Summary of the small-signal parameters of fabricated JL and IM poly-Si TFTs with W/L=8 μm/0.4 μm..163

Figure Captions

Chapter 1

Fig. 1-1 Schematic diagram of a TFET……..………………………………..…………………………17

Chapter 2

Fig. 2-1 Transistor cost and scaling trend of channel length versus years for technology node [1]. …………………..……………………………………………….37

Fig. 2-2 Process flow of poly-Si gate formation with double patterning technique. ……………………………….…………………………...37

Fig. 2-3 Mask layouts of the first (G1) and second (G2) gate patterns for defining the gate pattern on the active region. Gate length (L_{ovp}) of the final gate is determined by the overlap region of the two gate patterns. …………………………………...…………………………….38

Fig. 2-4 Major process steps for fabricating n-MOSFETs with the DP method. (a) Formation of gate oxide and poly-Si on Si wafer with LOCOS isolation. (b) Generation of first PR pattern (G1), followed by the first poly-Si etching. (c) Generation of second PR pattern (G2) after removing the first PR. (d) Completion of the poly-Si gate after second poly-Si etching and subsequent PR removal. (e) Formation of S/D structure. ………………………………..38

Fig. 2-5 Typical optical emissive signal recorded during the main etching stage of the second gate etching with the original mask design. No end point was detected. …………………………………………………………………...39

Fig. 2-6 Cross-sectional SEM view of a MOSFET showing an etch-induced recess at the right side of the gate. Top illustration is used to help visualize the structure. The recess was formed during the G2 etching stage due to the failure of EPD. ………………………………………………………………….…39

Fig. 2-7 (a) Optical emissive signal recorded during the main etching stage of the first gate etching step with the modified mask design. …………….……………………40

(b) Optical emissive signal recorded during the main etching stage of the

second gate etching step with the modified mask design. Successful EPD is achieved in the two etch steps……………………………………………..40

Fig. 2-8 (a) In-line SEM views of gate patterns on active region etched with original mask designs. The etch-induced damage region can be distinguished vividly. ……………………………………………………………………41

(b) In-line SEM views of gate patterns on active region etched with modified mask designs. The etch recess phenomenon can be resolved with the modified mask design……………………………………………………………..41

Fig. 2-9 Throughput of two lithography tools. ………..………………………………………………………42

Fig. 2-10 Mask layout for defining the gate pattern and observed area on the active region marked with a red dashed line. ……………………………………42

Fig. 2-11 (a) In-line SEM image of a patterned poly-Si line with nominal line width of 500 nm. The measured line width in this case is 498 nm. ……………………………..…………………………………………..43

(b) In-line SEM image of a patterned poly-Si line with nominal line width of 400 nm. The measured line width in this case is 390 nm……………………43

(c) In-line SEM image of a patterned poly-Si line with nominal line width of 300 nm. The measured line width in this case is 294 nm……………………44

(d) In-line SEM image of a patterned poly-Si line with nominal line width of 200 nm. The measured line width in this case is 214 nm……………………44

Fig. 2-12 In-line SEM images of patterned poly-Si lines located at eight different dies of a wafer with nominal line width of 100 nm. ……………………………………………………………….……..45

Fig. 2-13 In-line SEM images of patterned poly-Si lines located at eight different dies of a wafer with nominal line width of 80 nm. …………………………………………………………….………..45

Fig. 2-14 In-line SEM images of patterned poly-Si lines randomly located on a wafer with nominally shortest line width of 50 nm. …………………………………………………………………...46

Fig. 2-15 Measured poly-Si gate length (L_{poly}) as a function of nominal gate length

(L_{ovp}). ……………………………………………………………..……….46

Fig. 2-16 Cumulative plots of poly-Si gates patterned with DP method with nominal length of 80, 300, and 400 nm, and with conventional single patterning (SP) with nominal length of 350 nm. Each curve represents the results measured from 35 test structures. ……………………………………………………47

Fig. 2-17 Cross-sectional SEM image of a fabricated device with nominal gate length of 120 nm. Practical length was measured to be 115 nm. …………………………..……………………………………………..47

Fig. 2-18 (a) Transfer characteristics of NMOS control split biased at V_D = 0.05V with various channel length ranging from 0.12 to 10 μm. All devices have the same width of 10 μm. ………………………………………………..…….48

(b) Transfer characteristics of NMOS control split biased at V_D = 1.5V with various channel length ranging from 0.12 to 10 μm. All devices have the same width of 10 μm.…………………………………..……………….…..48

Fig. 2-19 (a) Transfer characteristics of NMOS and N-HALO splits with W/L=10 μm/120 nm. ………………………………………………..……………49

(b) Transfer characteristics of PMOS and P-HALO splits with W/L=10 μm/120 nm………………………………………………..……………..…49

Fig. 2-20 (a) Output characteristics of NMOS and N-HALO splits with W/L=10 μm/120 nm. ……………………………………………………….……..................50

(b) Output characteristics of PMOS and P-HALO splits with W/L=10 μm/120 nm……………………………………………..……..……..................50

Fig. 2-21 (a) Threshold voltage as a function of gate length for NMOS and N-HALO splits. ……………………………………………………………………51

(b) Threshold voltage as a function of gate length for PMOS and P-HALO splits ……………………………………………………………….……51

Fig. 2-22 (a) Drain induced barrier lowering (DIBL) as a function of gate length for NMOS and N-HALO splits. ………………………………………………52

(b) Drain induced barrier lowering (DIBL) as a function of gate length for PMOS and P-HALO splits…………………………………..…………52

Fig. 2-23 (a) On-current at V_{GS} = 1.5V and V_D = 1.5V as a function of gate length for

NMOS and N-HALO splits. …………………………………………………………………....53
(b) On-current at V_{GS} = -1.5V and V_D = -1.5V as a function of gate length for PMOS and P-HALO splits……………………………………………...……....53

Chapter 3

Fig. 3-1 Lithography roadmap for DRAM, MPU and Flash [1]. …………………………………………………………………...68

Fig. 3-2 (a) Mask layouts for defining the gate pattern and observed area on the active region. A single mask is used in the single-patterning process. ……………………………………………………………..……..69
(b) Mask layouts for defining the gate pattern and observed area on the active region. Gates 1 and 2 represent the two masks used in the DP process.……..90

Fig. 3-3 In-line SEM images patterned by the shaped-beam tool. ……………………………………………………………..………70

Fig. 3-4 In-line SEM images patterned by the Gaussian-beam tool. ……………………………………………………………………..…70

Fig. 3-5 In-line SEM images patterned by the PR ashing method after over-ashing process. ……………………………………………………………..……..71

Fig. 3-6 In-line SEM images patterned by the PR ashing method. ………….............71

Fig. 3-7 In-line SEM images patterned by the DP method. ……………………………………………………………...……….72

Fig. 3-8 Major process steps for fabricating n-MOSFETs with the Modified I-DP method. (a) Deposition of TEOS oxide hard mask and *in situ* phosphorus-doped poly-Si layers onto the HfO_2 gate dielectric (active region) with LOCOS isolation. (b) Generation of first PR pattern (G1), followed by the anisotropic etching of hard mask layer. (c) Lateral etching of the hard mask layer, followed by the PR removal and the first anisotropic etching of poly-Si layer. (d) Generation of second PR pattern (G2). (e) Completion of the poly-Si gate pattern after second hard mask and poly-Si etching, and subsequent PR removal. (f) Formation of S/D junctions. ……………………………...…..72

Fig. 3-9 In-line SEM images patterned by the Modified I-DP method. ……..73

Fig. 3-10 In-line SEM images of dense line patterns generated by the Modified I-DP method compared with single patterning method (I-SP). ……..73

Fig. 3-11 Cross-sectional TEM image of a fabricated nMOSFET……..74

Fig. 3-12 Throughput of two lithographic systems. …....74

Fig. 3-13 Process time versus device throughput of two lithographic systems. ……75

Fig. 3-14 CD distribution of two lithographic systems. ……75

Fig. 3-15 (a) Transfer characteristics of two gate dielectric splits measured at V_D = 0.05V with gate length of 10 μm and gate width of 10 μm. ……..76

(b) Output characteristics of two gate dielectric splits with gate length of 10 μm and gate width of 10 μm measured at V_{GS}-V_{th} = 0 ~ 2 V, step= 0.4 V, and V_D = 0 ~ 2 V……..76

Fig. 3-16 Transconductance curves of two gate dielectric splits measured at V_D = 0.05V with gate length of 10 μm and gate width of 10 μm. ……....77

Fig. 3-17 Transfer characteristics of two gate dielectric splits measured at V_D = 0.05 and 2 V with gate length of 45 nm and gate width of 10 μm. ……...77

Fig. 3-18 (a) Transfer characteristics of Symmetric and Asymmetric Halo splits measured at V_D = 0.05 and 2 V with gate length of 45 nm and gate width of 10 μm. ……...78

(b) Output characteristics of Symmetric and Asymmetric Halo splits with gate length of 45 nm and gate width of 10 μm measured at V_{GS}-V_{th} = 0 ~ 2 V, step= 0.4V, and V_D=0~2 V……...78

Fig. 3-19 (a) Transfer characteristics of Symmetric Halo split with HfO_2 dielectric

measured at V_D = 0.05 V with W/L = 50 μm/50 μm. ………………………..79

(b) Transfer characteristics of Symmetric Halo split with HfO_2 dielectric measured at V_D = 0.05 V with W/L = 20 μm/20 μm……………….………..79

(c) Transfer characteristics of Symmetric Halo split with HfO_2 dielectric measured at V_D = 0.05 V with W/L = 10 μm/10 μm……………….………..80

Fig. 3-20 Capacitance-Voltage (C-V) characteristics of HfO_2 dielectric split randomly sampled at eleven different dies of a six-inch wafer with gate length of 5 μm and gate width of 10 μm. The measurement frequency is 100 kHz. ……………………………………………….............................80

Fig. 3-21 Threshold voltage as a function of gate length for Symmetric and Asymmetric Halo splits……………………………………………................................81

Fig. 3-22 Current drivability (I_{on}) as a function of gate length for Symmetric and Asymmetric Halo splits measured at V_{GS}-V_{th} = 2 V and V_D = 2 V. 81

Chapter 4

Fig. 4-1 Schematic diagram of a TFET. …………………………………………………………..………...107

Fig. 4-2 Energy band diagrams of a TFET operated in the on/off-states…………….107

Fig. 4-3 Major process steps for fabricating TFETs with the DP method. (a) Formation of gate oxide and poly-Si on Si wafer with LOCOS isolation. (b) Generation of first PR pattern (G1), (c) First poly-Si etching and drain-junction implant. (d) Generation of second PR pattern (G2), (e) Second poly-Si etching and source-junction implant. (f) Completion of poly-Si gate after second PR removal……………………………………………………………...108

Fig. 4-4 Major process steps for fabricating nMOSFETs with the DP method. (a) Deposition of TEOS oxide hard mask and *in situ* phosphorus-doped poly-Si layers onto N_2O gate dielectric (active region) with LOCOS isolation. (b) Generation of first PR pattern (G1), (c) First oxide/poly-Si etching. (d) Generation of second PR pattern (G2), (e) Second poly-Si etching. (f) Completion of poly-Si gate after second PR removal, and formation of spacer, halo and S/D junctions……………………………………………………108

Fig. 4-5 Cross-sectional SEM image of a fabricated nMOSFET with nominal gate length of 80 nm……………………………………………………...…109

Fig. 4-6 Cross-sectional views of TFETs and the four splits of nMOSFETs……...…109

Fig. 4-7 Schematic illustrations for the charge pumping measurements with (a) fixed peak sweep, (b) fixed base sweep, and (c) fixed amplitude sweep……..….110

Fig. 4-8 Basic setup for charge pumping measurements……………………….…....110

Fig. 4-9 Measurement setup for single-junction charge pumping measurement…......111

Fig. 4-10 Schematic setup for flicker noise measurements………………….……..111

Fig. 4-11 Transfer curves of TFETs for different source dose splits with W/ L = 10 μm/0.2 μm…………………………………………..……..……...112

Fig. 4-12 Absolute value of source current versus source voltage curves with various channel length (0.2/0.5/1μm) and W of 10 μm. The gate is floating during measurements…………………………………………….……..…….112

Fig. 4-13 Absolute value of source current versus source voltage curves with various channel length (50/60/80/100nm) and W of 10 μm. The gate is floating during measurements………………………………………..…………..…….113

Fig. 4-14 Length dependence of transfer characteristics for nMOSFETs with various channel length and W = 10 μm biased at V_D =1.2 V and V_S =0 V. …..…….113

Fig. 4-15 Length dependence of transfer characteristics for TFETs with various channel length and W = 10 μm biased at V_D =0.5 V and V_S = -0.5 V……………….114

Fig. 4-16 Transfer characteristics of a TFET with constant V_{DS} (1.25V) but different S/D biases. W/L = 10 μm/0.2 μm……………………………………………..114

Fig. 4-17 The simulated doping concentration of boron in the source junction for the fabricated TFETs…………………………..…………………..115

Fig. 4-18 Transfer characteristics of all splits measured at V_D=0.05 and 1.2 V with W/L = 10 μm/80 nm…………………………..…………...……………..115

Fig. 4-19 Transconductance characteristics of all splits measured at V_D=0.05 V with W/L = 10 μm/80 nm……………………..…………...……………..116

Fig. 4-20 Output characteristics of all splits measured at V_G -V_{th} = 0~2 V and step = 0.4

V with W/L = 10 μm/80 nm. ……………….………..……..……………..116

Fig. 4-21 Threshold voltage roll-off characteristics of all splits measured at V_D = 0.05 V with W/L = 10 μm/80 nm……………..………..……..……………..……..117

Fig. 4-22 DIBL as a function of channel length for all splits measured at V_D = 0.05 V with W = 10 μm………..………..……..……………..…………………117

Fig. 4-23 Substreshold swing as a function of channel length for all splits measured at V_D = 0.05 V with W = 10 μm……..……..……………..………………..…118

Fig. 4-24 On-current as a function of channel length for all splits measured at V_G - V_{th} = 1 V and V_D = 1.2 V with W = 10 μm. ……..……………..………………..118

Fig. 4-25 Off-current as a function of channel length for all splits measured at V_G = 0 V and V_D = 1.2 V with W = 10 μm…...……………………..………………..119

Fig. 4-26 Transfer characteristics of 15 Control nMOSFETs, with W/L = 10 μm/80 nm measured at V_D = 1.5 V…...……………………...………………………....119

Fig. 4-27 Transfer characteristics of 15 Sym-Halo nMOSFETs, with W/L = 10 μm/80 nm measured at V_D = 1.5 V……………………..………….…………….....120

Fig. 4-28 Transfer characteristics of 15 Asy-Halo nMOSFETs, with W/L = 10 μm/80 nm measured at V_D = 1.5 V...……………………...………………………........120

Fig. 4-29 Transfer characteristics of 15 Asy-Halo-R nMOSFETs, with W/L = 10 μm/80 nm measured at V_D = 1.5 V. …………………..……….……………………...121

Fig. 4-30 Substrate current (I_{sub}) versus gate voltage for all splits of devices measured at V_D of 3 V with W/L = 10 μm /100 nm. ………...………….…………………121

Fig. 4-31 Impact ionization rate (I_{sub}/I_D) for all splits of devices measured at V_D of 3 V with W/L = 10 μm /100 nm……...………….…………………………….....122

Fig. 4-32 Subthreshold characteristics and transconductance of Control device before and after 5000-second of hot-electron stressing measured at V_D of 0.05 V with W/L = 10 μm /100 nm……...………….…………………………………….....122

Fig. 4-33 Subthreshold characteristics and transconductance of Sym-Halo device before and after 5000-second of hot-electron stressing measured at V_D of 0.05 V with W/L = 10 μm /100 nm...………….……………………………………….....123

Fig. 4-34 Subthreshold characteristics and transconductance of Asy-Halo device before

and after 5000-second of hot-electron stressing measured at V_D of 0.05 V with W/L = 10 μm /100 nm……….…………………………………...…....123

Fig. 4-35 Subthreshold characteristics and transconductance of Asy-Halo-R device before and after 5000-second of hot-electron stressing measured at V_D of 0.05 V with W/L = 10 μm /100 nm…….……………………………………...124

Fig. 4-36 Threshold voltage shift as a function of stress time for all splits of devices measured at V_D of 0.05 V with W/L = 10 μm /100 nm. The hot-electron stressing was performed at V_D = 3 V and V_G at maximum substrate current..124

Fig. 4-37 Transconductance degradation as a function of stress time for all splits of devices measured at V_D of 0.05 V with W/L = 10 μm /100 nm. The hot-electron stressing was performed at V_D = 3 V and V_G at maximum substrate current...125

Fig. 4-38 The increase in interface state density as a function of stress time for all splits of devices measured at V_D of 0.05 V with W/L = 10 μm /100 nm. The hot-electron stressing was performed at V_D = 3 V and V_G at maximum substrate current...125

Fig. 4-39 The increase in charge pumping current after 5000-second of hot carrier stress for all splits of devices with W/L = 10 μm /100 nm. The hot-electron stressing was performed at V_D = 3 V and V_G at maximum substrate current...............126

Fig. 4-40 Non-uniform distribution of local threshold voltage and flat-band voltage across the device caused by variation of lateral doping concentration. (x=0 is at the drain junction and direct to source junction) 126

Fig. 4-41 Derivation of the relationship between local threshold voltage and lateral distance x from the single-junction charge pumping data of the control device…………………………………………………………………..127

Fig. 4-42 Extracted lateral profile of local threshold voltage near the graded drain junction in the control sample……………………………………………....127

Fig. 4-43 Charge pumping current before and after 5000-second of hot-electron stressing (V_G@$Isub_{max}$ and V_D = 3 V) with W/L = 10 μm /100 nm………………….....128

Fig. 4-44 Lateral profile of generated interface states for the four splits of devices after

5000-second of hot-electron stressing (V_G@$Isub_{max}$ and V_D = 3 V) with W/L = 10 μm /100 nm……………..128

Fig. 4-45 Drain current noise spectrum density (S_{id}) of a virgin Control device measured at gate overdrive of 0.1 V (V_G –V_{th} = 0.1 V) and V_D = 0.05 V with W/L = 10 μm/100 nm…………...129

Fig. 4-46 Drain current noise spectrum density for all splits of virgin devices measured at a gate overdrive of 0.1 V (V_G –V_{th} = 0.1 V) and V_D = 0.05 V with W/L = 10 μm/100 nm………..129

Fig. 4-47 Normalized noise power spectrum density (S_{id}/I_D^2) and $(gm/I_D)^2$ as a function of drain current for Control device with W/L = 10 μm/0.2 μm at 100 Hz. ...130

Fig. 4-48 Normalized noise power spectrum density (S_{id}/I_D^2) and $(gm/I_D)^2$ as a function of drain current for Sym-Halo device with W/L = 10 μm/0.2 μm at 100 Hz. ………………………………………………………………………….130

Fig. 4-49 Normalized noise power spectrum density (S_{id}/I_D^2) versus gate overdrive (V_G–V_{th}) for all splits of devices with W/L = 10 μm/10 μm at 100 Hz…….131

Fig. 4-50 Normalized noise power spectrum density (S_{id}/I_D^2) versus gate overdrive (V_G–V_{th}) for all splits of devices with W/L = 10 μm/0.1 μm at 100 Hz. …..131

Fig. 4-51 Drain current noise spectrum density for all splits of stressed devices measured at gate overdrive of 0.1 V (V_G –V_{th} = 0.1 V) and V_D = 0.05 V with W/L = 10 μm/100 nm………………………………………………………………..132

Fig. 4-52 Normalized noise power spectrum density (S_{id}/I_D^2) versus gate overdrive (V_G–V_{th}) before and after 5000-second of hot-electron stressing for Control device with W/L = 10 μm/0.1 μm at 100 Hz. ………………………………132

Fig. 4-53 Normalized noise power spectrum density (S_{id}/I_D^2) versus gate overdrive (V_G–V_{th}) before and after 5000-second of hot-electron stressing for Sym-Halo device with W/L = 10 μm/0.1 μm at 100 Hz. ………………………………133

Fig. 4-54 Normalized noise power spectrum density (S_{id}/I_D^2) versus gate overdrive (V_G–V_{th}) before and after 5000-second of hot-electron stressing for Asy-Halo device with W/L = 10 μm/0.1 μm at 100 Hz………………………………..133

Fig. 4-55 Normalized noise power spectrum density (S_{id}/I_D^2) versus gate overdrive

($V_G–V_{th}$) before and after 5000-second of hot-electron stressing for Asy-Halo-R device with W/L = 10 μm/0.1 μm at 100 Hz……………..…..134

Fig. 4-56 The increase in normalized noise power spectrum density ($\Delta S_{id}/I_D^2$) versus gate overdrive ($V_G–V_{th}$) after 5000-second of hot-electron stressing for all splits of devices with W/L = 10 μm/0.1 μm at 100 Hz. …………..………..134

Chapter 5

Fig. 5-1 Key fabrication process flow of the proposed GAA JL NWFET. (a) Deposition and patterning of a sandwich stack of nitride/TEOS oxide/nitride layers on Si substrate capped with 200-nm-thick wet oxide, followed by selective lateral etching of TEOS oxide layer using DHF to form sub-100-nm cavity underneath both sides of the top nitride. (b) Deposition of an *in situ* phosphorus-doped poly-Si layer. (c) Simultaneous definition of NW doped channels and S/D regions. (d) Etching of the nitride and oxide, followed by the ALD deposition of the high-κ/metal gate stack structure (10-nm Al_2O_3 and 10-nm TiN). (e) Sputter deposition of another 140 nm TiN film to make a final gate electrode of 150 nm. (f) Schematic top-view layout of the device.. ……………………………………………………………..……….164

Fig. 5-2 Tilted scanning electron microscopic (SEM) images before and after cavity formation. ………………………………………………………....……….165

Fig. 5-3 Tilted SEM images of different-sized NW devices before the gate stack formation. (a) A tiny NW device showing NWs exposed on both sides of the temporary dielectric step, (b) a mid-sized NW device, and (c) a large-sized NW device……………………………………………..………..…….165

Fig. 5-4 Cross-sectional HRTEM image of a fabricated GAA JL NWFET with the TEOS oxide/TiN gate stack. A NW size is around of 12 nm in thickness (T) and 23 nm in width (W). The inset is the corresponding diffraction pattern of the NW, revealing the monocrystalline structure of the grain with [110] orientation. ……………………………………………..……..……….165

Fig. 5-5 TEM and tilted SEM images of fabricated JL devices. (a) Cross-sectional TEM image of a JL device with tiny NW covered with Al_2O_3/TiN GAA stack. 52°

tilted SEM images of a mid-sized JL device with a NW cross section of 75 × 30 nm and a large-sized JL device with a NW cross section of 152 × 74 nm. ……………………………………………………………………….166

Fig. 5-6 Key fabrication process flow of the proposed GAA JL NW SONOS memory device. (a) Deposition and patterning of a sandwich stack of nitride/TEOS oxide/nitride layers on Si substrate capped with 200-nm-thick wet oxide. (b) Selective lateral etching of TEOS oxide using DHF to form a sub-100-nm cavity underneath both sides of the top nitride. (c) Deposition of an *in situ* phosphorus-doped poly-Si layer. (d) Simultaneous definition of the NW doped channels and S/D regions, followed by etching off the nitride and oxide surrounding the NW channels. (e) LPCVD deposition of gate dielectric stack of blocking oxide/trapping nitride/tunneling oxide (ONO) with thicknesses of 12/7/3 nm. (f) Deposition and patterning of an *in situ* phosphorous doped n^+-poly-Si layer as the gate electrode. ……………………..…………….167

Fig. 5-7 Schematic illustrations of gate structures (GAA/Ω-gate) implemented in our JL-SONOS memory cells. ………………….……………………………...168

Fig. 5-8 (a) Top-view SEM and cross-sectional TEM images of the NW channel with (b) GAA and (c) Ω-gate structures. ……………………………………………………..………...168

Fig. 5-9 Illustration of the key steps for building 3-D multilayer stacked JL poly-Si NW device. (a) Formation of sub-100 nm cavities. (b) Formation of channel and S/D. ……………………………………………………..……………….169

Fig. 5-10 Tilted SEM images of anisotropically-etched dummy patterns. …..……….169

Fig. 5-11 Overhead-view SEM images of the nano-cavities with (a) 30- and (b) 40-second lateral-etching time. ……………………..……………………170

Fig. 5-12 Cross-sectional TEM images of fabricated 3-D stacked JL NW memory device. ……………………..……………………………..…………………170

Fig. 5-13 Key fabrication process flow of the proposed planar JL poly-Si TFT. (a) Growth of 1000-nm-thick oxide by wet oxidation on a six-in silicon substrate as the buried oxide. (b) Deposition of a 9-nm-thick *in situ* phosphorous doped n^+-poly-Si layer as the channel layer. (c) Successive depositions of a 13-nm

TEOS oxide as the gate dielectric and a 200-nm *in situ* n^+-poly-Si as the gate electrode, followed by the gate pattern definition. (d) Formation of sidewall spacers (20-nm TEOS oxide layer and 20-nm nitride layer). (e) Depositions of a 5-nm-thick nickel layer and a 15-nm-thick titanium nitride layer. (f) Annealing process for forming NiSi on the gate, and S/D regions. ………..171

Fig. 5-14 Top-view SEM and cross-sectional TEM images of the fabricated planar JL poly-Si TFT. ………….…………………………..……………………..172

Fig. 5-15 *S*-parameter measurement system. …………………..……………………..172

Fig. 5-16 Equivalent circuit diagram used for the two-step correction including parasitic effect. ………..…………………………..………………………………173

Fig. 5-17 (a)The open test fixture and (b) the diagram of equivalent circuit. ……..….173

Fig. 5-18 (a)The short test fixture and (b) the diagram of equivalent circuit. …..…….174

Fig. 5-19 Transfer characteristics of JL and IM NWFETs with an NW channel dimension of W/T = 23 nm/12 nm and a channel length (L) of 1 μm measured at V_D = 0.5 and 2 V. ……………………..……………………………………174

Fig. 5-20 Comparison of transconductance versus gate voltage for the JL and IM devices at V_D = 0.5 V. ……………………..…………………..………………………175

Fig. 5-21 Measured total resistance $R_{total} \equiv V_D/I_D = R_{SD} + R_{ch}$ versus channel length for JL and IM NWFETs measured at $V_G - V_{th}$ of 4 V and V_D of 0.15 V. …..175

Fig. 5-22 Transfer characteristics of the JL and IM NW devices. Mid-sized (75 × 30 nm) and large-sized (152 × 74 nm) JL NW devices are also plotted for comparison. All devices characterized here are with channel length of 0.4 μm. ………………………………………………………………………176

Fig. 5-23 Output characteristics of JL and IM splits measured at V_G - V_{th} = 0 ~ 2 V and step = 1 V with L = 0.4 μm. ……………………..…………………………176

Fig. 5-24 Transconductance (Gm) and increments of Gm as a function of gate length for JL and IM splits measured at V_D = 0.5 V. ……..……………………...…….177

Fig. 5-25 Threshold voltage (V_{th}) as a function of gate length for JL and IM splits measured at V_D = 0.5 V. …………………..…………………………….…..177

Fig. 5-26 On-state current (I_{on}) and increments of I_{on} as a function of gate length for JL

and IM splits extracted at V_G - V_{th} = 2 V and V_D = 0.5 V. ………………....178

Fig. 5-27 Tilted SEM and cross-sectional TEM images of a fabricated GAA JL NWFET with L=5 μm showing collapse of NWs in the central channel region with an omega-shaped gate structure. The inset shows a NW device with L=1 μm depicting normal suspension of NWs between the S/D regions. ………....178

Fig. 5-28 Programming properties of the JL and IM NW SONOS devices at gate biases of 9, 11, and 13 V. ……………..……………………………………..……..179

Fig. 5-29 Transfer characteristics of JL SONOS split in the programmed states biased at V_G = 13 V for various duration times. ……………………………….……..179

Fig. 5-30 Multilevel programming behavior of the JL NW device. Transfer characteristics of JL SONOS device with gate biases of 9, 11, and 13 V for 100 ns. Inset shows the definition of V_{th} range for each state. …………..……..180

Fig. 5-31 Erasing properties of the JL and IM NW SONOS devices at gate biases of -9, -11, and -13 V. Before erasing, the cells were programmed to V_{th} shift of +3 V and +2.5 V for the JL and IM structures, respectively. …………..………..180

Fig. 5-32 Retention behaviors for the JL and IM NW SONOS devices at room temperature. ……..……………………………………………………………...181

Fig. 5-33 Endurance behaviors for the JL and IM NW SONOS devices at room temperature. …...………………………………………………………………...181

Fig. 5-34 Transfer characteristics of GAA-L, Ω-L, GAA-H and Ω-H JL NW SONOS devices measured at V_D = 0.5 and 2 V. …………………………………..182

Fig. 5-35 Programming behaviors for GAA-L, Ω-L, GAA-H and Ω-H JL NW SONOS devices. The programming gate bias is 11 V. ………………………………182

Fig. 5-36 Erasing behaviors for GAA-L, Ω-L, GAA-H and Ω-H JL NW SONOS devices. The Erasing gate bias is -11 V. ……………………………………………..183

Fig. 5-37 Retention behaviors for the GAA-L and GAA-H JL NW SONOS devices at room temperature. ……………………………………………………….183

Fig. 5-38 Retention behaviors for the Ω-L and GAA-L JL NW SONOS devices at room temperature………………………………………………………………184

Fig. 5-39 Transfer characteristics and the affiliated cross-sectional SEM image of a

non-working 3-D JL device. ………………………………………………….……….184

Fig. 5-40 Cross-sectional SEM image of a non-working 3-D JL device. ……………..185

Fig. 5-41 Transfer and output characteristics of both 1-level and 3-level JL splits with L = 1 μm, (a) measured at V_D = 0.1 and 2 V, (b) V_G - V_{th} = 0 ~ 4 V with step = 2 V. …………………………………………………………………….…...185

Fig. 5-42 Cumulative distribution of V_{th} for both 1-level and 3-level JL splits with L = 1 μm measured at V_D = 0.1 V. ……………………………………………......186

Fig. 5-43 Cumulative distribution of SS for both 1-level and 3-level JL splits with L = 1 μm measured at V_D = 0.1 V. ……………………………………………......186

Fig. 5-44 Cumulative distribution of I_{on} for both 1-level and 3-level JL splits with L = 1 μm extracted by maximum drain current at V_D = 2 V. …………………......187

Fig. 5-45 Cumulative distribution of I_{off} for both 1-level and 3-level JL splits with L = 1 μm extracted by minimum drain current at V_D = 2 V. ……………….........187

Fig. 5-46 Transfer characteristics of both JL and IM planar poly-Si TFTs with W/L = 8/0.4 μm measured at V_D = 0.1 and 2 V. ………………………….……….......188

Fig. 5-47 Output characteristics of both JL and IM planar poly-Si TFTs with W/L = 8/0.4 μm measured at V_G - V_{th} = 0 ~ 3 V with step = 1 V. ……………….........188

Fig. 5-48 Drain-current noise power spectral density (S_{id}) versus frequency for both JL and IM planar poly-Si TFTs with W/L = 8/0.4 μm measured at V_{GS} - V_{th} =0.5 V and V_D = 0.1 V. …………………………………...……………......189

Fig. 5-49 (Symbols) S_{id}/I_d^2 and (dashed lines) $(g_m/I_d)^2$ versus drain current for both JL and IM planar poly-Si TFTs with W/L = 8/0.4 μm measured at V_D = 0.1 V. ………………………………………………………………….………..189

Fig. 5-50 H_{21} and U of JL device measured at V_D of 2 V and (V_{GS} − V_{th}) of 4 V with W/L = 8/0.4 μm. …………………………………………………….………..190

Fig. 5-51 H_{21} and U of IM device measured at V_D of 2 V and (V_{GS} − V_{th}) of 4 V with W/L = 8/0.4 μm. …………………………………………………….………..190

Fig. 5-52 f_t and f_{max} of the JL and IM devices measured at V_D of 2 V and (V_{GS} − V_{th}) of 0.5–3.5 V with respect to the drain current. …………………….………..191

Fig. 5-53 The cross section of the fabricated TFT with corresponding small-signal

equivalent circuit. ……………………………………..……….……..……..191

Fig. 5-54 The extraction results of extrinsic resistances. ………..…….….……….……..192

Fig. 5-55 The extraction results of $Im(Y_{11})+Im(Y_{12})$, $-Im(Y_{12})$, and $Im(Y_{12})+Im(Y_{22})$ as a function of the angular frequency. …………………..……..…….………..192

Fig. 5-56 The extraction results of g_m and r_o as a function of the angular frequency. ..193

Fig. 5-57 The extraction results of τ as a function of the angular frequency. ………...193

Fig. 5-58 The modeling results of the fabricated TFT (a) S_{11} and S_{22} and (b) S_{12} and S_{21} (lines for measurements, symbols for models). …..………….…………………194

Chapter 1

Introduction

1.1 General Background

1.1-1 Double Patterning Technique

The well-known Moore's Law describes that the number of transistors on an integrated circuit (IC) chip will double every 18 months [1-2]. Since the advent of IC manufacturing, this law has been in force for decades. In order to keep up with the Moore's Law, shrinkage in device dimensions is indispensable, which also promotes device density, operation speed, and chip functionality. In other words, for better performance and cheaper manufacturing cost, the continuous scaling of the devices is evitable. To keep pace with the law, it requires innovation to overcome several fundamental physical barriers lying ahead, and first of all is to extend the photolithography limit. According to the Rayleigh's criterion, the resolution, R, of a photolithography technique can be expressed as follows [3]:

$$R = {k_1 \lambda}/{NA} \quad (1\text{-}1),$$

where *k1* is a system constant, λ is the wavelength of incident light, and *NA* is the numerical aperture of the lithography system. Based on such criterion, we could adjust the three factors of the criterion so as to boost the resolution of a lithography system [4-6]. Recently, it was reported that the double exposure (DE) technique [7], and double patterning (DP) technique [8-10] were being considered as the promising candidates to extend lithography processing beyond the 45 nm node at *k1* factors below 0.30. DP is a process that splits one patterning step into two to relax the imaging fidelity requirements for small technology nodes. The most common form of DP typically decomposes a target layout pattern into two separate photomasks employing two exposure steps and subsequent etching steps. Consequently, the dimensions of the final target patterns can easily break the resolution limit with single exposure. Usually I-line stepper is not capable of sub-100 nm pattern generation owing to its long exposure wavelength of 365 nm. In this work, we develop a DP technique with conventional I-line stepper to generate sub-100 nm photoresist (PR) patterns with the goal to fabricate nano-scale

MOSFETs. Although this technique consists of two times the lithographic and subsequent etching steps, we show that the DP method could reliably generate line patterns with dimension down below 100 nm.

1.1-2 Junctionless Technique

For the sake of keeping pace with the Moore's Law, continuously downscaling the dimension of the semiconductor devices is indispensable to maintain device functionality and make manufacturing cost cheaper. However, the traditional planar bulk MOSFET structure used in the past decades inherently consists of two PN junctions, the source/drain-to-channel junctions, and the extremely high doping concentration gradient of S/D region causes the fluctuation of diffusing impurities especially within a range of few nanometers for the nano-scale devices [11]. To precisely control the doping prolife of S/D region, it needs an excessively tight and efficient thermal process for the dopant activation, which imposes more challenges on the device fabrication with the continuous shrinkage of device dimension.

To address the aforementioned challenge of controlling the doping profile, a novel device named "junctionless (JL) field-effect transistor" has been revived recently [12-14], while the same idea has been revealed in an old patent filed by Lilienfeld in 1926 [15]. In a JL transistor, the same doping polarity and concentration are used throughout the entire device from the source, channel to drain. Furthermore, the operation of a JL transistor is different from that of an accumulation-mode device, and is inherently a gated resistor in the on-state. In particular, a JL transistor is turned off through full depletion of carriers in the channel by the gate in the off-state. Besides, the much higher doping concentration in the channel, larger than 10^{19} cm^{-3}, is the unique feature of JL transistor, and is different from an accumulation-mode transistor. Due to the inherently homogeneous doping concentration across S/D and channel in the JL transistor, no conventional p-n junctions are present in it. Therefore, the JL technique can relieve the constraints related to the formation of the ultra-shallow or ultra-abrupt junction encountered in the conventional inversion-mode (IM) transistor, thus the fabrication process can be greatly simplified and the manufacturing cost can be cheaper as well.

1.1-3 Asymmetric S/D Devices

With the dimensional scaling of the MOSFETs, it accompanies a lot of challenges including the increasingly rising off-state leakage current and the short channel effects (SCE), such as the threshold voltage (V_{th}) roll-off, the drain induced barrier lowering (DIBL), and bulk punch-through. As for the IC industry, which has traditionally been driven by the Moore's Law, it has brought about catastrophic power consumption, and thus the emergent demand for lower power supply is without any description. But it also requires a coexisting reduction in the threshold voltage to sustain the device performance leveraging the Moore's Law. Nevertheless, a concomitant increase in off-state leakage is inevitable due to the restriction of non-scalable subthreshold swing (SS). For the sake of leakage current reduction, low power consumption and good SCE immunity, optimization of the source and drain junctions separately would be an effective scheme.

The asymmetric MOSFET with asymmetric lightly-doped drain (LDD) architecture [16-17] was fabricated by using additional implantation mask, followed by formation of selective oxide deposition. However, the latent misalignment would obstruct the device scaling. Fortunately, the self-aligned asymmetric structure [18] was proposed to settle the aforementioned issue. But, unfortunately, the inevitable use of phosphoric acid would likely be another issue resulted from the gate oxide damage caused by isotropic etching of phosphoric acid. The implantation scheme is an approach to achieve an asymmetric architecture as well. As described in [19], the implementation of tilt-angle implantation facilitated the fabrication of asymmetric architecture. Nonetheless, the shielding of denser gate electrodes would increase more challenges in the adoption of tilt-angle implantation with downscaling. On the other hand, the halo doping scheme employed in standard CMOS process certainly can be adopted to accomplish the asymmetric structure in terms of boosting the device performance as reported in [20-22]. The adoption of source-junction-only halo doping scheme can not only reduce the capacitance of n^+p junction at the drain junction but also the electrical field of drain side. Therefore the issue of leakage current can effectively be relieved, and further the power consumption can be reduced.

With the ever-increasing concerns about the forthcoming exhaust of petroleum in the near future and the unavoidable power consumption by the IC appliances, the green technology is highly demanded for reducing the supply voltage of CMOS logic devices. The most fundamental limitation that controls the turn-on efficiency of a transistor stems from its inherent properties related to thermodynamic carrier distribution. The

basic drift-diffusion theory gives the physical limitation on the subthreshold swing (SS) at 60 mV/dec at room temperature [23]. The concept of tunneling field-effect transistor (TFET) was proposed by Sanjay Banerjee *et al*. in 1987 [24] and called "surface tunneling transistor" as well in those days [24-26]. The TFET is inherently a gated p-i-n diode and certainly can be categorized as an asymmetric S/D device as depicted in Fig. 1.1, using band-to-band tunneling (BTBT) as carrier transport mechanism. As a result, TFETs do not undergo the same physical limitation as MOSFETs, and are a promising candidate for achieving sub-60 mV/dec of SS.

1.1-4 Flicker Noise Characteristics

In an electronic circuit, currents and voltages are randomly perturbed from their given values because of inextricable interference of noise. Considering the random nature of noise, it can't be excluded thoroughly and further restricts the accuracy of measured results eventually [27-28]. Hence, in view of both science and engineering, noise is a basic problem, essential to comprehend and consider for the sake of alleviating its effects and increasing the precision of desired signals. There are many kinds of noise sources such as thermal noise, shot noise, generation-recombination (g-r) noise, random-telegraph-signal (RTS) noise, and flicker (1/f) noise [29-35]. Because the transistor dimensions have been continuously downscaled, CMOS technology has been developed for the RF and analog applications which were governed by bipolar transistors in the past [36-40]. For low-noise RF/analog applications, low 1/f noise in MOSFETs is an important requirement. Therefore, accurate MOSFET noise models are highly correlated with circuit designers as well as semiconductor manufacturers that are required to pay attention to reducing the 1/f noise in transistors.

The flicker noise in MOSFETs has been extensively studied for more than two decades [41-47]. The flicker noise, called 1/f noise as well, is the common name for the fluctuations with its power spectral density proportional to $1/f^{\gamma}$, with γ close to 1, usually in the range of 0.7 to 1.3. In the past, there were two major theories to explain the physical origins of flicker noise in MOSFETs. One is the number fluctuation theory based on McWhorter's charge trapping model [43]. The other is the bulk mobility fluctuation theory based on Hooge's empirical relation [48].

In the carrier number fluctuation theory, the random trapping and detrapping processes of charges occurred in the oxide traps near the interface between Si channel

and SiO_2 are the culprit of flicker noise [41-42], [49-50] which was originally presented by McWhorter in 1957 [43]. The charge fluctuation influences fluctuation of the surface potential, and further the channel carrier density is modulated. The conventional number fluctuation theory predicts that the 1/f noise power in the linear region is given by

$$S_{Id}(f) = \frac{I_d^2}{fWLN^2}\frac{N_t(E_{fn})_{eff}}{\gamma} \tag{1-2},$$

where $N_t(E_{fn})_{eff}$ is the effective oxide trap density at the quasi Feimi level; I_d is the drain current; f is frequency; N is the number of channel carrier per unit area; γ is the attenuation coefficient of electron wave function in the oxide and the value is typically taken to be 10^8 cm^{-1} for the Si-SiO_2 system [51]; W and L are channel width and length, respectively.

On the other hand, the mobility fluctuation theory considers 1/f noise as a result of fluctuation in bulk mobility, and moreover, the spectral density in a homogeneous material based on Hooge's empirical relation can be given by

$$S_{Id}(f) = \frac{I_d^2 \alpha_H}{fWLN} \tag{1-3},$$

where S_{Id} is the spectral density of the noise in the current; I_d is the drain current; f is the frequency; N is the number of channel carriers per unit area; α_H is the Hooge's parameter with a value of around 2×10^{-3} [46]; W and L are channel width and length, respectively.

Later a unified flicker noise model which was proposed by K. K. Hung [52] incorporated both the carrier number fluctuation theory and the mobility fluctuation mechanism to explain the origin of low-frequency noise in a correlated manner. The total drain current noise power can be expressed as

$$S_{Id}(f) = \frac{1}{L^2}\int_0^L S_{\Delta Id}(x,f)\Delta x dx = \frac{kTI_d^2}{\gamma fWL^2}\int_0^L N_t(E_{fn})\left[\frac{1}{N(x)} \pm \alpha\mu\right]^2 dx \tag{1-4},$$

where $N_t(E_{fn})$ is the oxide trap density at Fermi level E_{fn}; $N(x)$ is the number of channel carriers per unit area; α is the Columbic scattering parameter; γ is the attenuation coefficient and typically equals to 10^8 cm^{-1} [51]; The sign of the mobility term can be determined by fitting the expression with the measured data. For the majority of samples, the sign has to be chosen as positive. This equation is the basic expression of the unified flicker noise model. Furthermore, we can yield the input referred noise power by virtue of dividing S_{Id} by the square of the transconductance, and the formula

can be given by

$$S_{Vg}(f)=\frac{S_{Id}(f)}{{g_m}^2}=\frac{kTq^2}{\gamma fWLC_{ox}^2}(1+\alpha\mu N)^2 N_t(E_{fn}) \qquad (1\text{-}5).$$

1.1-5 Radio Frequency Techniques

In the past, wireless communication industry was regarded as an important part of the defense industry due to the importance of instantaneous transmission, and its mysterious muffler was gradually taken off until Cold War came to the end. People were looking forward to breaking the space constraint by virtue of wireless communication, and therefore the private enterprise found their motivation in the development of wireless communication industry nonstop. Based on the continuous development of the integrated circuit technology and the desperate demand for the people's livelihood application, it makes possible to bring out the cheap wireless communication products. However, human beings really manifest their hungers for larger capacity of data transmission after both the convenience and timeliness of the wireless transmission are met. In the case of no longer extra bandwidth being squeezed out through both the network protocol and the developments of systematic architecture, it is the fundamental solution to obtain a large number of bandwidth by increasing the communication frequency. While using the wireless communication technology for facilitating some innovative applications such as distant and timely medical care [53], immediate disaster warning, logistics management to create better living is another important target worthy of development. Therefore, how to attain low power operation and energy-saving goals is the common objective of relative research topic. Nonetheless, the core value of wireless communication development is the high-frequency technology regardless of oncoming developments of both wireless communication technology and application.

There are various high-frequency devices including heterojunction bipolar transistor (HBT) such as AlGaAs/GaAs HBT, InGaP/GaAs HBT and InP HBT of III-V compound semiconductors [54], or silicon based devices such as SiGe HBT and CMOS [55]. For the past decades, transistors have been widely used and continuously developed because the raw material of silicon is easily obtained and the correlated fabrication process is well mature. Moreover, IC manufacturing vendors have made great efforts to scale down the device’s gate length for achieving higher operation frequency of the circuits and further encroaching in the field of high-frequency

applications in recent years. There are various RF transmission chips constructed by transistors including voltage-controlled oscillator (VCO) [56], low-noise amplifier (LNA) [57], filter, mixer, and phase-locked loop (PLL) [58]. On the other hand, the RF performance of thin-film transistors (TFTs) is expected to improve significantly by properly shrinking the dimensions of devices, and further it is demonstrated that the polycrystalline silicon TFT technology is feasible for low-cost RF IC applications such as RF identification (RFID) and RF modules integrated on display panel [59-60].

1.2 Motivation

To keep pace with the Moore's Law, it requires innovation to accomplish shrinkage in device dimensions, and first of all extending the photolithography limit is indispensable. 32 nm technology node mass production of nano-scale ICs employs the immersion lithography tools with the excimer laser to generate the nano-scale patterns [61]. However, the extremely high-cost equipment employed for high-volume manufacturing is not affordable in the university-based laboratories. Therefore, a large part of researches focused on the device size of nano-scale regime accomplished in the university-based laboratories barely count on some substitute methods, such as electron beam direct writing [62], ion beam lithography system [63], nanoimprint lithography [64], *etc*. In this dissertation, a simple method which combines both I-line lithographic process and double patterning (DP) technique, as stated in Sec.1.1-2, is proposed and developed to generate sub-100 nm photoresist (PR) patterns with the goal to fabricate nano-scale MOSFETs. In addition, the proposed lithographic technique was implemented to fabricate symmetric or asymmetric devices as stated in Sec. 1.1-4. The additional merit associated with the proposed DP process is increasing the flexibility in device design in terms of accomplishment of independent S/D engineering to promote the device performance.

On the other hand, polycrystalline silicon (poly-Si) thin-film transistor (TFT) technology has been very attractive for the flexible electronics, the emerging 3-D IC and system-on-panel (SoP) electronics integration owing to its low thermal budget and very mature fabrication processes [65-66]. In recent years, the nanowire (NW) TFTs with the implementation of NWs as the channels have been demonstrated with excellent device performance thanks to their inherently tiny volume and the following reduction of defects [67-68]. Furthermore, the NW TFT combined with multiple-gated (MG)

structure [69] benefits not only current drive, but also subthreshold slope, as well as better immunity to the short-channel effects thanks to better gate controllability for effectively controlling the electrostatic potential in its tiny NW channel. To cope with the issue of formation of extremely abrupt junctions, as mentioned in Sec. 1.1-3, NWTFT technology previously developed by our group with the MG configuration was adopted to implement the JL scheme by using one *in situ* doped poly-Si layer to serve as source, channel and drain junctions [70]. In this dissertation, we exploit the feasibility of JL technology through the fabrication and characterization of both MG NWTFT and planar ultrathin-channel TFT schemes, and furthermore adopt these JL devices in the applications of logic circuits, nonvolatile memory devices and even high-frequency techniques.

Owing to well developed and very mature fabrication processes of TFTs, the performance of TFTs has been greatly boosted to serve as not only the mainstream technology, the switches of pixels in the AMLCDs [71] at the start, but also the basic building blocks of ICs on the periphery of displays, SoP especially. In addition, with the thriving in portable electronics, wireless transmission among electronics equipment doubtlessly prevails throughout our daily life as mentioned in Sec. 1.1-6. However, owing to the relatively low mobility of poly-Si as compared with the bulk Si counterparts, as well as the quite giant device size in state-of-the-art manufacturing (*e.g.*, channel length > 3 μm), few works are reported on studying the high-frequency characteristics of poly-Si TFTs. Therefore, in this dissertation, we undertook the studies to investigate the high-frequency characteristics of short-channel poly-Si TFTs (*e.g.*, channel length < 3 μm), including the fabrication and characterization of both IM and JL planar poly-Si TFTs to demonstrate the feasibility of low-cost RF IC applications, as well as the related small-signal modeling and parameter extraction of fabricated devices.

1.3 Thesis Organization

Total seven chapters are contained in this dissertation.

In Chapter 1, the related backgrounds and motivations of this dissertation are described.

In Chapter 2, we have developed a simple method adopting double-patterning (DP) technique to extend the I-line stepper limit to define nano-scale structures. Through in-line and cross-sectional scanning electron microscopy analyses of the generated

patterns, we confirmed the feasibility of the DP technique for the fabrication of nano-scale devices. Resolution capability of this technique has been confirmed to be at least 100 nm, which is much superior to the resolution limit of conventional I-line lithography. Moreover, an unexpected obstacle, the etching issue of second gate pattern, occurred in the DP process is addressed as well.

In Chapter 3, we have developed a modified DP technique with an I-line stepper and also compared several lithographic techniques implemented as promising candidates for the purpose of patterning nano-scale structures in the university-based laboratories. By virtue of in-line and cross-sectional scanning electron microscopy analyses of the generated patterns, we confirmed the feasibility of the ameliorative DP technique for generating sub-30 nm line patterns, and furthermore some features of these lithographic techniques were discussed in terms of throughput, line edge roughness (LER), critical dimension uniformity (CDU), minimum line width, *etc*.

In Chapter 4, we have fabricated asymmetric devices, including asymmetric halo nMOSFETs and tunneling field-effect transistors (TFETs) after demonstrating the feasibility of DP technique in Chapter 2. In addition, several device performances of symmetric and asymmetric devices are discussed in terms of both dc characteristics and reliability tests such as hot-carrier stress and flicker noise characteristics.

In Chapter 5, we have investigated the feasibility of gate-all-around (GAA) polycrystalline silicon (poly-Si) nanowire transistors with junctionless (JL) configuration by utilizing only one heavily doped poly-Si layer to serve as source, channel, and drain regions. *In situ* n^+-doped poly-Si material features high and uniform-doping concentration, facilitating the fabrication process and reducing the process cost. Moreover, we have also investigated the impacts of other gate stacks such as TiN gate/Al_2O_3 dielectric and n^+ poly-Si gate/oxide-nitride-oxide (ONO) dielectric, and further the performances of fabricated devices are discussed through basic electrical analyses and memory reliability characteristics compared with undoped-channel counterpart, demonstrating that the JL scheme is a promising candidate for the emerging SoP and 3D-IC or high density memory applications. On the other hand, we have demonstrated the feasibility of poly-Si technology for RF applications by virtue of both fabricating the *in situ* doped-channel TFTs adopted with salicide process, and furthermore characterizing the fabricated devices, including basic electrical analyses, small-signal modeling and the related parameter extraction. The results suggest the poly-Si TFT technology is applicable to low-cost RF IC and RF modules integrated on

display panel.

In Chapter 6, we conclude with summaries of the experimental results. Suggested items for future works are also given.

References

[1] P. K. Bondyopadhyay, “Moore's law governs the silicon revolution,” *Proc. IEEE*, vol. 86, no. 1, pp. 78-81, Jan. 1998.

[2] C. A. Mack, “Fifty years of Moore’s law,” *IEEE Trans. on Semiconductor Manufacturing*, vol. 24, no. 2, pp. 202-207, May 2011.

[3] James D. Plummer, Michael D. Deal, and Peter B. Griffin, “Silicon VLSI technology: Fundamentals, Practice and Modeling,” Prentice Hall Inc., New Jersey, 2000, pp. 209-213.

[4] M. Switkes and M. Rothschild, “Immersion lithography at 157 nm,” *J. Vac. Sci. Technol. B*, vol. 19, no. 6, pp. 2353-2356, 2001.

[5] M. D. Levenson, N. S. Viswanathan, and R. A. Simpson, “Improving resolution in photolithography with a phase-shifting mask,” *IEEE Trans. on Electron Devices*, vol. ED-29, no. 12, pp. 1828-1836, Dec. 1982.

[6] M. Drapeau, V. Wiaux, E. Hendrickx, S. Verhaegen, and T. Machida, “Double patterning design split implementation and validation for the 32nm node,” *Proc. SPIE*, vol. 6521, pp. 652109-01-652109-15, Mar. 2007.

[7] S. Hsu, J. Park, D. Van Den Broeke, and J. F. Chen, “Double exposure technique for 45nm node and beyond,” *Proc. SPIE*, vol. 5992, pp. 59921Q-1-59921Q-16, Nov. 2005.

[8] P. Rigolli, C. Turco, U. Iessi, G. Capetti, P. Canestrari, and A. Fradilli, “Double patterning overlay budget for 45 nm technology node single and double mask approach,” *J. Vac. Sci. Technol. B*, vol. 25, no. 6, pp. 2461-2465, 2007.

[9] L. S. Melvin III, B. S. Ward, H. Song, S. U. Rhie, K. D. Lucas, V. Wiaux, S. Verhaegen, and M. Maenhoudt, “Exploration of etch step interactions in the dual patterning process for process modeling,” *J. Vac. Sci. Technol. B*, vol. 26, no. 6, pp. 2434-2440, 2008.

[10] M. Maenhoudt, J. Versluijs, H. Struyf, J. Van Olmen, and M. Van Hove, “Double patterning scheme for sub-0.25 k1 single damascene structures at NA=0.75, λ=193nm,” *Proc. SPIE*, vol. 5754, pp. 1508-1518, May 2005.

[11] S. Thompson, P. Packan, T. Ghani, M. Stettler, M. Alavi, I. Post, S. Tyagi, S. Ahmed, S. Yang, and M. Bohr, “Source/drain extension scaling for 0.1 μm and below channel length MOSFETs,” in *VLSI Symp. Tech. Dig.*, 1998, pp. 132-133.

[12] C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge,

"Junctionless multigate field-effect transistor," *Appl. Phys. Lett.*, vol. 94, no. 5, p. 053511, 2009.

[13] C. W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J. P. Colinge, "Performance estimation of junctionless multigate transistors," *Solid-State Electronics*, vol. 54, no. 2, pp. 97-103, 2010.

[14] J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 225-229, 2010.

[15] J. E. Lilienfeld, U.S. Patent 1,745,175 (filed in 1926, issued in 1930), U.S. Patent. 1,877,140 (filed in 1928 issued in 1932), and U.S. Patent 1,900,018 (filed in 1928, issued in 1933).

[16] J. F. Chen, J. Tao, P. Fang, C. Hu, "Performance and reliability comparison between asymmetric and symmetric LDD devices and logic gates," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 367-371, 1999.

[17] T. Horiuchi, T. Homma, Y. Murao, and K. Okumura, "A high performance asymmetric LDD MOSFET using selective oxide deposition technique," in *VLSI Symp. Tech. Dig*., 1992, pp. 88-89.

[18] C. S. Choi, K. W. Kim, and W. Y. Choi, "A new self-aligned asymmetric structure (SAAS) for 0.1 μm MOSFET technology," in *Proc. IEEE Electron Devices Meeting*, 2000, pp.60-63.

[19] T. Ghani, K. Mistry, P. Packan, M. Armstrong, and S. Thompson, "Asymmetric source/drain extension transistor structure for high performance sub-50nm gate length CMOS devices," in *VLSI Symp. Tech. Dig*., 2001, pp. 17-18.

[20] W. Yeh and J. Chou, "Optimum halo structure for sub-0.1 μm CMOSFETs," *IEEE Trans. on Electron Devices*, vol. 48, no. 10, pp. 2357-2362, Oct. 2001.

[21] A. Bansal, and K. Roy, "Asymmetric halo CMOSFET to reduce static power dissipation with improved performance," *IEEE Trans. on Electron Devices*, vol. 52, no. 3, pp. 397-405, Mar. 2005.

[22] S. Odanaka and A. Hiroki, "Potential design and transport property of 0.1-μm MOSFET with asymmetric channel profile," *IEEE Trans. on Electron Devices*, vol. 44, no. 4, pp. 595-600, Apr. 1997.

[23] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. New York: Wiley, 2007.

[24] S. Banerjee, W. Richardson, J. Coleman and A. Chatterjee, “A new three-terminal tunnel device,” *IEEE Electron Device Lett.*, vol. EDL-8, no. 8, pp. 347-349, Aug. 1987.

[25] T. Baba, “Proposal for surface tunnel transistors,” *Jpn. J. Appl. Phys.*, vol. 31, no. 4, pp. L455-L457, Apr. 1992.

[26] William M. Reddick and Gehan A. J. Amaratunga, “Surface tunnel transistor,” *Appl. Phys. Lett.,* vol. 67, no. 4, pp. 494-496, July 1995.

[27] A. Van Der Ziel, *Noise in Solid State Devices and Circuits*, New York: John Wiley & Sons, 1986.

[28] C. D. Motchenbacher and J. A. Connelly, *Low-noise Electronic System Design*, New York: John Wiley & Sons, 1993.

[29] J. B. Johnson, “Thermal agitation of electricity in conductors,” *Phys. Rev.*, vol. 32, pp. 97-109, 1928.

[30] H. Nyquist, “Thermal agitation of electric charge in conductors,” *Phys. Rev.*, vol. 32, pp. 110-113, 1928.

[31] F. N. Hooge, “1/f noise sources,” *IEEE Trans. on Electron Devices*, vol. 41, no. 11, pp. 1926-1935, Nov. 1994.

[32] G. Bosman and R. J. J. Zijlstra, “Generation-recombination noise in p-type silicon,” *Solid-State Electronics*, vol. 25, no. 4, pp. 273-280, Apr. 1982.

[33] N. V. Amarasinghe, Z. Celik-Butler, and A. Keshavarz, “Extraction of oxide trap properties using temperature dependence of random telegraph signals in submicron metal-oxide-semiconductor field-effect transistors,” *J. Appl. Phys.,* vol. 89, no. 10, pp. 5526-5532, May 2001.

[34] G. Ghibaudo and T. Boutchacha, “Electrical noise and RTS fluctuations in advanced CMOS devices,” *Microelectron. Reliab.*, vol. 42, pp. 573-582, 2002.

[35] P. Dutta and P. M. Horn, “Low-frequency fluctuations in solids: 1/f noise,” *Rev. Mod. Phys.*, vol. 53, no. 3, pp. 497-516, 1981.

[36] P. H. Woerlee, M. J. Knitel, R. van Langevelde, D. B. M. Klaassen, L. F. Tiemeijer, A. J. Scholten, and A. T. A. Zegers-van Duijnhoven, “RF-CMOS performance trends,” *IEEE Trans. on Electron Devices*, vol. 48, no. 8, pp. 1776-1782, Aug. 2001.

[37] A. A. Abidi, “RF CMOS comes of age,” in *Proc. Symp. VLSI Circuits*, 2003, pp. 113-116.

[38] J. J. Liou and F. Schwierz, “RF MOSFET: recent advances, current status and

future trends," *Solid-State Electronics*, vol. 47, no. 11, pp. 1881-1895, Nov. 2003.

[39] A. Mercha, W. Jeamsaksiri, J. Ramos, D. Linten, S. Jenei, P. Wambacq and S. Decoutere, "Impact of scaling on analog/RF performance," in *Proc. IEEE Int. Conf. Solid-State and Integrated Circuits Technology*, 2005, pp. 147-152.

[40] K. Lee, I. Nam, I. Kwon, J. Gil, K. Han, S. Park and B.-I. Seo, "The impact of semiconductor technology scaling on CMOS RF and digital circuits for wireless application," *IEEE Trans. on Electron Devices*, vol. 52, no. 7, pp. 1415-1422, July 2005.

[41] S. T. Hsu, "Surface state related 1/f noise in MOS transistors," *Solid-State Electronics*, vol. 13, no. 11, pp. 1451-1459, 1970.

[42] H. S. Fu and C. T. Sah, "Theory and experiments on surface 1/f noise," *IEEE Trans. on Electron Devices*, vol. ED-19, no. 2, pp. 273-285, 1972.

[43] A. L. McWhorter, *1/f noise and germanium surface properties*, in *Semiconductor Surface Physics*. Philadelphia: University of Pennsylvania Press, 1957, p.207.

[44] H. Mikoshiba, M. Sakamoto and S. Thompson, "Characterization of 1/f noise in MOS transistors," in *IEDM Tech. Dig.*, 1982, p. 662.

[45] H. Mikoshiba, "1/f noise in n-channel silicon-gate MOS transistors," *IEEE Trans. on Electron Devices*, vol. ED-29, no. 6, pp. 965-970, 1982.

[46] F. N. Hooge, "1/f noise," *Physica*, vol. 83B, pp. 14-23, 1976.

[47] K. K. Hung, P. K. Ko, C. Hu and Y. C. Cheng, "Flicker noise characteristics of advanced MOS technologies," in *IEDM Tech. Dig.*, 1988, p. 34.

[48] F. N. Hooge, "1/f noise is no surface effect," *Phys. Lett. A*, vol. 29a, pp. 139-140, 1969.

[49] S. T. Hsu, "Low frequency noise in MOS transistors," *Solid-State Electronics*, vol. 13, no. 11, pp. 1451-1459, 1970.

[50] S. T. Hsu, "Surface state related 1/f noise in MOS transistors," *Solid-State Electronics*, vol. 13, no. 11, pp. 1451-1459, 1970.

[51] S. Christensson I. Lundstrom and C. Svensson, "Low frequency noise in MOS transistors-I Theory," *Solid-State Electronics*, vol. 11, no. 9, pp. 797-812, 1968.

[52] K. K. Hung, P. K. Ko, C. Hu and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. on Electron Devices*, vol. 37, no. 3, pp. 654-665, 1990.

[53] E. Jovanov, A. Milenkovic, C. Otto and P. C de Groen, "A wireless body area network of intelligent motion sensors for computer assisted physical

rehabilitation," *J. NeuroEngineering and Rehabilitation*, vol. 2, no. 6, pp. 1-10, 2005.

[54] O. Esame, Y. Gurbuz, I. Tekin and A. Bozkurt, "Performance comparison of state-of-the-art heterojunction bipolar devices (HBT) based on AlGaAs/GaAs, Si/SiGe and InGaAs/InP," *Microelectronics Journal*, vol. 35, no. 11, pp. 901-908, 2004.

[55] J. D. Cressler, "SiGe HBT technology: a new contender for Si-based RF and microwave circuit applications," *IEEE Trans. Microwave Theory & Tech.*, vol. 46, no. 5, pp. 572-589, 1998.

[56] J. Craninckx and M. S. J. Steyaert, "A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 736-744, 1997.

[57] T. K. Nguyen, C. H. Kim, G. J. Ihm, M. S. Yang and S. G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microwave Theory & Tech.*, vol. 52, no. 5, pp. 1433-1442, 2004.

[58] I. A. Young, J. K. Greason and K. L. Wong, "A PLL clock generator with 5 to 110 MHz of lock range for microprocessors," *IEEE J. Solid-State Circuits*, vol. 27, no. 11, pp. 1599-1607, 1992.

[59] J. L. Botrel, O. Savry, O. Rozeau, F. Templier and J. Jomaah, "Polysilicon high frequency devices for large area electronics: characterization, simulation and modeling," *Thin Solid Films*, vol. 515, no. 19, pp. 7422-7427, 2007.

[60] Y.-J. E. Chen, Y.-J. Lee and Y.-H. Yu, "Investigation of polysilicon thin-film transistor technology for RF application," *IEEE Trans. Microwave Theory & Tech.*, vol. 58, no. 12, pp. 3444-3451, 2010.

[61] P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S-H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. St. Amour, K. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luo and S. Natarajan, "High performance 32 nm logic technology featuring 2nd generation high-*k* + metal gate transistors," in *IEDM Tech. Dig.*, 2009, p. 659.

[62] K. H. Chen, C. Y. Chien, P. W. Li and O. Adams, "Precise Ge quantum dot placement for quantum tunneling devices," *IEEE Trans. Nanotechnology*, vol. 21, no. 5, p. 055302, 2010.

[63] R. F. Pease and S. Y. Chou, “Lithography and other patterning techniques for future electronics,” *Proceedings of the IEEE*, vol. 96, no. 2, pp. 248-270, 2008.

[64] M. Shibata, A. Horiba, Y. Nagaoka, H. Kawata, M. Yasuda and Y. Hirai, “Process-simulation system for UV-nanoimprint lithography,” *J. Vac. Sci. Technol. B*, vol. 28, pp. C6M108-C6M113, 2010.

[65] H. Wang, M. Chan, S. Jagar, Y. Wang and P. K. Ko, “Submicron super TFTs for 3-D VLSI applications,” *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 439-441, Sep. 2000.

[66] E. K. Lai, H. T. Lue, Y. H. Hsiao, J. Y. Hsieh, C. P. Lu, S. Y. Wang, L. W. Yang, T. Yang, K. C. Chen, J. Gong, K. Y. Hsieh, R. Liu and C. Y. Lu, “A multilayer stackable thin-film transistor (TFT) NAND-type Flash memory,” in *IEDM Tech. Dig.*, 2006, p. 41.

[67] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles and J. L. Goldma, “High-performance thin-film transistors using semiconductor nanowires and nanoribbons,” *Nature*, vol. 425, no. 6955, pp. 274-278, Sep. 2003.

[68] H. C. Lin and C. J. Su, “High-performance poly-Si nanowire NMOS transistors,” *IEEE Trans. Nanotechnol.*, vol. 6, no. 2, pp. 206-212, Mar. 2007.

[69] M. Im, J. W. Han, H. Lee, L. E. Yu, S. Kim, C. H. Kim, S. C. Jeon, K. H. Kim, G. S. Lee, J. S. Oh, Y. C. Park, H. M. Lee and Y. K. Choi, “Multiple-gate CMOS thin-film transistor with polysilicon nanowire,” *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 102-105, Jan. 2008.

[70] C. J. Su, T. I. Tsai, Y. L. Liou, Z. M. Lin, H. C. Lin and T. S. Chao, “Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels,” *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 521-523, Apr. 2011.

[71] S. Zhang, C. Zhu, J. K. O. Sin, J. N. Li and P. K. T. Mok, “Ultra-thin elevated channel poly-Si TFT technology for fully-integrated AMLCD system on glass,” *IEEE Trans. on Electron Devices*, vol. 47, no. 3, pp. 569-575, Mar. 2000.

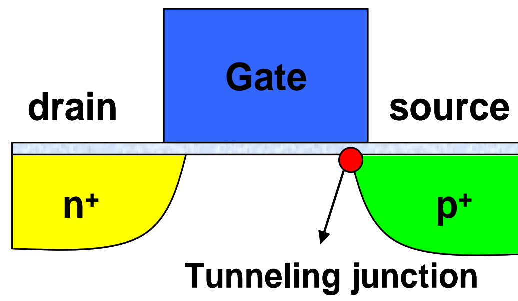


Fig. 1-1 Schematic diagram of a TFET.

Chapter 2

A Simple Method for Sub-100 nm Pattern Generation with I-line Double Patterning Technique

2.1 Introduction

Since the advent of integrated circuit (IC), lithography has been playing a critical role in semiconductor manufacturing for the sake of achieving shrinkage in device dimensions and keeping up with the Moore's Law. Figure 2-1 illustrates the historical trends of transistor cost and feature size for CMOS during the past three decades [1]. In fact, the successful evolution of IC technology very closely counts upon the advancement of lithography instruments and associated processes. 32 nm technology node mass production of nano-scale ICs employs the immersion lithography tools with the ArF-193nm excimer laser to generate the nano-scale patterns [2]. Nevertheless, the extremely high cost on the skyrocketing lithography tool and related process is not usually affordable in the laboratories of universities. On the other hand, electron-beam (e-beam) lithography [3] is therefore far more popular in the universities for generating sub-100 nm patterns, although the throughput is dramatically limited as compared with photolithography methods, and thus its proliferation in mass manufacturing is prohibited.

I-line steppers have been employed for a long time for both manufacturing and research purposes, and the associated lithographic process is very mature and reliable. However, for conventional I-line process, the line width of generated photoresist (PR) pattern is typically 0.3 μm or wider. Although nano-scale dimensions can be achieved by combining with the PR ashing scheme [4-5], a highly stable asher is necessary to ensure good reproducibility and uniformity of critical dimension (CD) of the printed patterns. Besides, rounding of the top PR can be another concern for subsequent etching step [5]. Recently, it was reported that the double exposure (DE) technique [6], and double-patterning (DP) technique [7-12] were being considered as promising candidates to extend lithography processing beyond the 45 nm node at *k1* factors below 0.30. Furthermore, DP technique has been considered as a viable approach for sub-32-nm

nodes by integrating with the immersion ArF-193-nm process [13].

In this chapter, we propose a simple method which combines both I-line lithographic process and DP technique to address the aforementioned issues. As compared with the e-beam direct writing method, I-line process surpasses in throughput but is much worse in resolution capability which can be ascribed to the optical diffraction phenomenon. On the other hand, DP technique which typically requires twice lithographic and/or etch steps has been proposed to increase the density of devices [7-8] and has also been demonstrated with the capability of breaking the resolution limit of an optical system [9-10]. Even with the I-line process, generated structures with nano-scale dimensions can be expected if the DP technique is incorporated. Hence, we exploit such feasibility by successfully fabricating and characterizing both nano-scale n-channel metal-oxide-semiconductor field-effect transistors (n-MOSFETs) and p-MOSFETs. Besides, an issue encountered in polycrystalline silicon (poly-Si) gate electrode etch step of the proposed method is presented and discussed as well.

2.2 Development of Double Patterning with I-line Stepper

To implement the above-mentioned DP technique, it is necessary to ensure the feasibility of DP scheme. For all lithographic steps carried out in this work, we used an I-line stepper (Canon FPA-3000i5+) to generate PR patterns. Fundamental process steps of the proposed scheme for forming the test patterns are shown in Fig. 2-2. The poly-Si film was deposited on a six-inch Si substrate capped with a thermal oxide layer (100 nm) as shown in Fig. 2-2 (a), followed by the first lithographic step [Fig. 2-2 (b)]. Afterwards, the regions of exposed poly-Si layer were etched with a reactive plasma step, as shown in Fig. 2-2 (c). In Fig. 2-2 (d), the second lithographic step was employed to generate PR patterns which covered portions of the poly-Si layer remained on the surface of the substrate, followed by a reactive plasma etching step to complete the final poly-Si structure [Fig. 2-2 (e)]. With suitable design and process control, the dimension of final poly-Si line patterns [Fig. 2-2 (f)] could be scaled well below 100 nm. This procedure employed two masks denoted as G1 and G2 to define the gate electrode, as shown in Fig. 2-3. As can be seen in Fig. 2-3, the most critical portion in the design is the overlapped region of the two gate patterns in the active area which determines the channel length (L_{ovp}) of the fabricated device. In-line and cross-sectional scanning electron microscopy (SEM) techniques were used to characterize and verify the

resultant PR and etched poly-Si structures formed by DP technique.

2.3 Devices Fabrication

The above DP process has also been implemented in practical n-MOSFET and p-MOSFET fabrication for forming 120 nm gate patterns, and the fabricated n-MOSFETs were performed on 6-inch p-type (100) bare Si wafers (n-type bare Si wafers for p-MOSFETs). Figure 2-4 illustrates the major process steps in the fabrication of MOSFETs with the DP technique. First, local oxidation of Si (LOCOS) scheme was used for device isolation. P-type well for n-MOSFETs (n-type well for p-MOSFETs) was formed by the implantation of BF_2^+ with energy of 70 keV and dose of 1×10^{13} cm^{-2} (P_{31}^+ with energy of 120 keV and dose of 7.5×10^{12} cm^{-2}), followed by a drive-in anneal step at 1100 ^oC. Channel stop implantation was performed by implanting BF_2^+ (120 keV, 4×10^{13} cm^{-2}) for n-MOSFETs and As^+ (120 keV, 3×10^{12} cm^{-2}) for p-MOSFETs. Anti-punchthrough (APT) and threshold voltage (V_{th}) adjustment implantations of n-MOSFETs were performed individually by implanting B^+ (70 keV, 2×10^{12} cm^{-2}) and BF_2^+ (90 keV, 1×10^{13} cm^{-2}), and those for p-MOSFETs were P_{31}^+ (120 keV, 7.5×10^{12} cm^{-2}) and As^+ (120 keV, 3×10^{12} cm^{-2}), respectively. Thermal gate oxide of about 3 nm was grown in an N_2O ambient of a vertical furnace, followed by the deposition of a 150 nm-thick *in situ* phosphorous-doped poly-Si layer (undoped poly-Si layers for p-MOSFETs) to serve as the gate electrode, as shown in Fig. 2-4 (a). Gate implant was implemented only for p-channel devices by implanting BF_2^+ (15 keV, 5×10^{15} cm^{-2}), followed by gate dopant activation at 900 °C for 30 seconds. Afterwards, DP technique was executed to pattern the poly-Si gate. The two lithographic processes of DP scheme using G1 and G2 masks were aligned with the preexisting zero-layer alignment mark formed on the wafer. Mask G1 was first applied to generate PR patterns covering portions of the poly-Si, as shown in Fig. 2-4(b), followed by a reactive ion etch (RIE) step done by a Lam-TCP9400 to remove the uncovered poly- Si. The second lithographic step with mask G2 was then employed to generate PR patterns which covered portions of the poly-Si layer remaining on the surface of the substrate [Fig. 2-4 (c)], followed by an RIE step to complete the final poly-Si structure. After the gate patterning [Fig. 2-4 (d)], the source/drain (S/D) extensions were formed by implanting As^+ (10 keV, $1\times10^{15}$$cm^{-2}$) for n-MOSFETs and BF_2^+ (10 keV, 5×10^{14} cm^{-2}) for p-MOSFETs. In addition, the n-MOSFET halo implantations were executed by

implanting BF_2^+ (50 keV, 2.5×10^{12} cm^{-2}, tilt angle =45°) denoted as N-HALO, while p-MOSFET halo implantations were executed by implanting As^+ (50 keV, 2.5×10^{12} cm^{-2}, tilt angle =45°) denoted as P-HALO. Some wafers skipping the halo implantations, denoted individually as NMOS and PMOS, serve as the controls. After forming a 100 nm-thick TEOS sidewall spacer, deep S/D junctions were formed by implanting As^+ (20 keV, $5\times10^{15}cm^{-2}$), and then rapid thermal anneal (RTA) was then individually carried out in a nitrogen ambient at 1000 ^oC for 10 seconds (n-MOSFETs) and spike-1000 ^oC (p-MOSFETs) to activate dopants in the gate and S/D junctions, as depicted in Fig. 2-4 (e). Finally, 680 nm-thick TiN/AlSiCu/TiN/Ti metallization was carried out in a PVD system to form the metal pads, and then the processing steps were completed with a forming gas anneal at 400 °C for 30 minutes. The overall implantation conditions used in the device fabrication were marshaled as shown in Tables 2-1 and 2-2 for n-MOSFETs and p-MOSFETs, respectively. Electrical characteristics were performed using an Agilent 4156 system.

2.4 Results and Discussion

2.4-1 End Point Detection Issue

During device fabrication with DP technique, a major issue related to the ineffectiveness of end point detection (EPD) in the second poly-Si etch step was found. Figure 2-5 shows the evolution of optical emission signal intensity during the second poly-Si etch step on a test wafer. Normally the end point should be detected at around 20 seconds after the turning on of plasma, but this did not happen instead the signal remained stable. Moreover, the signal intensity appeared to be much weaker than that recorded during the first poly-Si etch step. Since the signal intensity is related to the etch by-products [14], which is believed to be related to the layout design of mask G1. In the original version of G1 mask, over 90% of the blanket poly-Si area is not covered by the PR and is etched off in the first poly-Si etch step, and consequently the end point (defined as the moment when the intensity drops to 90% of the peak intensity) can be easily detected in the main etch stage of the first etch step. However, with the scanty poly-Si left during the second etch, only a very weak optical signal is detectable, causing the failure of EPD.

Besides, owing to the ultrathin gate oxide, EPD failure may cause the breakthrough

of the gate oxide, Si recess in the substrate, and further result in device failure. Figure 2-6 illustrates the cross-sectional scanning electron microscopy (SEM) image of a MOSFET showing a recess in the Si substrate at the right side of the gate, an indication of the damage induced in the second etching process. When this happens, the devices exhibit very leaky characteristics and are no longer suitable for practical application. The aforementioned issue could be resolved by modifying the layout design of the mask G1. This was implemented by inserting some dummy patterns to the layout of the mask G1 to increase the remaining area of the poly-Si film after the first etching step. These dummy patterns removed in the second etching step could contribute more etch by-products and increase the optical signal for effective EPD. The feasibility of the modified mask design is evidenced by the EPD results recorded during the first and second poly-Si gate etching steps, as shown in Figs. 2-7(a) and 2-7(b), respectively. In the two etching steps, EPD could both be successfully carried out. To further highlight the effectiveness of the new layout design, the in-line SEM pictures of the poly-Si line after the second etch step with original and modified layout are shown in Figs. 2-8(a) and 2-8(b), respectively. An obvious etch-induced damage region, corresponding to the Si recess region shown in Fig. 2-6, is observed at the right side of the gate in Fig. 2-8(a). In Fig. 2-8(b), with the modified layout, such damage could be completely eliminated.

2.4-2 Feasibility of Double Patterning Technique

The e-beam lithography suffers from a very low throughput, as stated in Sec. 2.1. Figure 2-9 illustrates the throughput comparison between processes with e-beam tool (LEICA WEPRINT 200) and I-line stepper (Canon FPA-3000i5+). The patterning method with e-beam tool is denoted as Shaped beam. Conventional single exposure with I-line stepper and DP scheme with I-line stepper are denoted as I line-SP and I line-DP, respectively. We could find that, though the throughput is cut by half for I-line process when DP scheme is employed, it is still about 100 times the throughput of the e-beam process, implying that I line-DP possesses both high throughput and nano-scale pattern generation capability.

Before confirming the feasibility of DP technique in this section, both test structure and observed area of line pattern are illustrated in Fig. 2-10, and the observed zone is marked with a red dashed line over the active region of the device. Figure 2-11 shows the after-etching-inspection (AEI) images, with the designed value larger than 100 nm,

recorded by in-line SEM. Here, L_{ovp} is the nominal designed length of mask layout and L_{poly} is the practical physical length through lithography and etching processes. Figure 2-11 (a) shows in-line SEM image of a patterned poly-Si line with nominal line width of 500 nm and the measured line width is 498 nm. In-line SEM image of a patterned poly-Si line with nominal line width of 400 nm is illustrated in Fig. 2-11 (b) and the measured line width is 390 nm. Figure 2-11 (c) depicts in-line SEM image of a patterned poly-Si line with nominal line width of 300 nm and the measured line width is 294 nm. In-line SEM image of a patterned poly-Si line with nominal line width of 200 nm is exhibited in Fig. 2-11 (d) and the measured line width is 214 nm. In contrast with Fig. 2-11, Figs. 2-12, 2-13 and 2-14 show the in-line SEM images of AEI with L_{ovp} less than 100 nm. In-line SEM images of patterned poly-Si lines located at eight different dies of a wafer with nominal line width of 100 nm are shown in Fig. 2-12, and the measured line widths are distributed from 81 nm to 126 nm. Figure 2-13 illustrates in-line SEM images of patterned poly-Si lines located at eight different dies of a wafer with nominal line width of 80 nm, and the measured line widths are distributed from 60 nm to 103 nm. Next, the minimum L_{ovp} of mask layout is 50 nm, and in-line SEM images of patterned poly-Si lines randomly located on a wafer are depicted in Fig. 2-14. Obviously discontinuous line patterns can be discovered in the active regions of devices even if L_{poly} of these disabled patterned poly-Si lines can achieve 25 nm. The aforementioned L_{poly} values displayed in Figs 2-12, 2-13 and 2-14 are quite reasonable as far as the overlay accuracy of the I-line stepper is concerned. As shown in Table 2-3 provided by the vendor, the overlay accuracy is 45 nm at most. This implies that the gate length designed below 80 nm is out of control and difficult to reproduce, which is consistent with Fig. 2-14. Anyway, the present DP method is useful for generation of line patterns down to 80 nm with reliable control of critical dimensions, as shown in Fig. 2-13.

The controllability of critical dimension (CD) is checked by a collection of the linewidth of patterned poly-Si gates measured by in-line SEM, as depicted in Fig. 2-15. As can be seen in this figure, the dimensions of the printed polygates are close to those of the mask patterns. Figure 2-16 shows the cumulative plots of the measured poly-Si gates with nominal lengths of 80, 300, and 400 nm, patterned with the present DP technique. Also shown in the figure are the results of poly-Si gates with nominal length of 350 nm patterned with conventional I-line technique. In the figure each curve represents measured data obtained from 35 test samples distributed across the test wafer.

The results clearly demonstrate the capability of this approach of not only shrinking the gate length beyond the resolution limit of single patterning technique (>300 nm) but also achieving a better dimension control as compared with conventional I-line process. Even with a much smaller gate dimension, the distribution in the measured gate width of the DP-patterned lines is obviously tighter than that of the conventional I-line method. Since the feature sizes of G1 and G2 patterns are much larger than the resolution limit of the I-line stepper, the CD variation is strongly dependent on the alignment accuracy of the exposure tool. According to the specifications of the employed stepper as shown in Table 2-3, the overlay accuracy (3σ) is about 45 nm. This value is close to the deviation of the measured data (51 nm) with the DP technique shown in Figs. 2-15 and 2-16. In other words, the overlay accuracy of the exposure tool sets the limit for the CD control of the present approach. This may result in a noticeable variation in device characteristics as its dimensions are small. Fortunately, such concern can be relieved with a modification in process steps to tailor the device structure. An example is the implementation of asymmetrical S/D, which is characterized and discussed in Chapter 4. Finally, the profile of an etched poly-Si gate pattern of a fabricated device recorded by cross-sectional SEM is shown in Fig. 2-17. The image obviously indicates that a gate length of about 115 nm with the designed L_{ovp} of 120 nm is achieved, further confirming the feasibility of the proposed I-line DP lithographic technique.

2.4-3 Devices Characteristics for n-MOSFETs and p-MOSFETs

Figures 2-18 (a) and (b) show the transfer characteristics of NMOS control devices with various channel length under different drain biases. When the dimensions of devices scale down from 10 μm to 0.12 μm, severe bulk punchthrough current occurs and causes the degradation of subthreshold characteristics in control samples, resulting in subthreshold leakage current of two orders larger than long-channel devices at V_{GS} = 0 V. The above-mentioned bulk punchthrough current induced degradation of subthreshold characteristics can be comprehended with the charging sharing model [15-16], sharing the charges in the channel depletion region with S/D junctions. For a long-channel device, there is little impact of S/D depletion on the channel potential due to its remote channel from source to drain area. In contrast with long-channel case, the short-channel counterpart, comparable to its depletion-width in the channel region, suffers from significant effect of charges sharing with S/D junctions, causing the V_{th}

lowering. Furthermore, such phenomenon becomes severer as a high drain bias applied to the short-channel device, and causes further penetration of drain-side depletion region into the channel, resulting in lowering of the surface potential barrier of the channel. Therefore, when device size is scaling down, the gate controllability becomes weaker as shown in Fig. 2-18 (b).

Figures 2-19 (a) and (b) illustrate the comparison of subthreshold characteristics with channel length (L) of 10 μm and channel length (W) of 0.12 μm for n-MOSFETs and p-MOSFETs, respectively. The implementation of halo implant efficiently relieves the aforementioned degradation of subthreshold characteristics in terms of reducing off-state leakage current (drain current at gate voltage of 0 V and V_D = +/-1.5 V) of two orders lower than control samples, improving subthreshold swing and increasing V_{th} as clearly shown in those figures. Halo implant was adopted to increase the local substrate doping concentration and consequently relax the penetration of drain-side depletion region into the channel. Especially, the lowering in surface potential barrier height under a high drain bias is improved as well. However, you can not sell the cow and drink the milk. The recovery of gate controllability over the short-channel effect by using halo scheme is at the expense of device performance such as transconductance and current drivability degradation. Figures 2-20 (a) and (b) show the output characteristics of both n- and p-MOSFETs with W/L = 10 μm/0.12 μm and V_{GS}-V_{th} = 0 ~ 2 V. A drain current degradation of about 13% is found as the halo implant is executed. Such degeneracy is ascribed to the RSCE induced V_{th} increment and accordingly ruined the current drivability.

Threshold voltage as a function of channel length for both n- and p-MOSFETs with W = 10 μm are shown in Figs. 2-21 (a) and (b). The threshold voltage is defined as the gate voltage at drain current of (W/L) · 10nA biased with a small drain voltage (V_D = +/-0.05 V). As can be seen in the plots, both N-HALO and P-HALO splits exhibit obviously the reverse-short-channel-effect (RSCE) because halo increases doping distribution near the S/D edges of the channel, and therefore results in a locally higher threshold voltage. Figures 2-22 (a) and (b) depict drain induced barrier lowering (DIBL) as a function of channel length for both n- and p-MOSFETs with W = 10 μm. It is apparently identified that halo scheme indeed relieves the lowering in surface potential barrier height under a high drain bias in terms of reducing DIBL of N-HALO and P-HALO splits as compared with the control counterparts. Nonetheless, one of the side effects of halo is the degenerate current drivability as illustrated in Fig. 2-23. On-current

(I_{on}) as a function of channel length for both n- and p-MOSFETs with W = 10 μm is shown in Figs. 2-23 (a) and (b), respectively. From the plots, the I_{on} of the halo devices is about 13% smaller than that of control devices, once more indicating the degradation of driving current with the adoption of halo.

2.5 Summary

In this chapter, we have developed a simple method which combines both I-line lithographic process and DP technique to accomplish nano-scale pattern generation, and confirmed such feasibility by successfully fabricating and characterizing both 120 nm n-/p-MOSFETs. In comparison with the conventional single-patterning method, the DP technique displays better CD control and acceptable throughput, as have been demonstrated in our study. Besides, through both in-line and cross-sectional SEM analyses, we further manifested the present I-line DP technique is a promising candidate for the purpose of patterning sub-100 nm structures in the university-based laboratories. Finally, the impact of halo on device performance is discussed, including short-channel effect, current drivability and V_{th} roll-off. We have found that the halo implantation would improve the SCEs and reduce the subthreshold leakage. However, at the same time the halo implantation increases V_{th} in short-channel devices and causes the severe RSCE, resulting in the degradation of driving current. In short, it is very important to optimize the halo implant for nano-scale device manufacturing.

References

[1] S. E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C.-H. Jan, C. Kenyon, J. Klaus, K. Kuhn, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, B. Obradovic, R. Nagisetty, P. Nguyen, S. Sivakumar, R. Shaheed, L. Shifren, B. Tufts, S. Tyagi, M. Bohr, and Y. El-Mansy, "A 90-nm logic technology featuring strained silicon," *IEEE Trans. on Electron Devices*, vol. 51, no. 11, pp. 1790-1797, 2004.

[2] P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S-H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. St. Amour, K. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luo and S. Natarajan, "High performance 32nm logic technology featuring 2nd generation high-*k* + metal gate transistors," in *IEDM Tech. Dig.*, 2009, p. 659.

[3] M. Drapeau, V. Wiaux, E. Hendrickx, S. Verhaegen, and T. Machida, "Double patterning design split implementation and validation for the 32nm node," *Proc. SPIE*, vol. 6521, pp. 652109-01-652109-15, Mar. 2007.

[4] S. Hsu, J. Park, D. Van Den Broeke, and J. F. Chen, "Double exposure technique for 45nm node and beyond," *Proc. SPIE*, vol. 5992, pp. 59921Q-1-59921Q-16, Nov. 2005.

[5] J. Chung, M. Jeng, J. E. Moon, A. T. Wu, T. Y. Chan, P. K. Ko, and C. Hu, "Deep-submicrometer MOS device fabrication using a photoresist-ashing technique," *IEEE Electron Device Lett.*, vol. 9, no. 4, pp. 186-188, 1988.

[6] K. Asano, Y.-K. Choi, T.-J. King, and C. Hu, "Patterning sub-30-nm MOSFET gate with i-line lithography," *IEEE Trans. on Electron Devices*, vol. 48, no. 5, pp. 1004-1006, 2001.

[7] J. R. Sheats and B. W. Smith, "Microlithography: Science and Technology," Marcel Dekker Inc., New York, 1998, p. 102.

[8] K. M. Monahan, "Enabling double patterning at the 32nm node," in *Proc. IEEE International Symposium on Semiconductor Manufacturing*, 2006, pp. 126-129.

[9] P. Rigolli, C. Turco, U. Iessi, G. Capetti, P. Canestrari, and A. Fradilli, "Double patterning overlay budget for 45 nm technology node single and double mask approach," *J. Vac. Sci. Technol. B*, vol. 25, no. 6, pp. 2461-2465, 2007.

[10] K. Ronse, P. Jansen, R. Gronheid, E. Hendrickx, M. Maenhoudt, V. Wiaux, A.-M.

Goethals, R. Jonckheere, and G. Vandenberghe, “Lithography options for the 32 nm half pitch node,” *IEEE Trans. Circuits Syst., I: Regul. Pap.*, vol. 56, no. 8, pp. 1883-1890, 2009.

[11] L. S. Melvin III, B. S. Ward, H. Song, S. U. Rhie, K. D. Lucas, V. Wiaux, S. Verhaegen, and M. Maenhoudt, “Exploration of etch step interactions in the dual patterning process for process modeling,” *J. Vac. Sci. Technol. B*, vol. 26, no. 6, pp. 2434-2440, 2008.

[12] M. Maenhoudt, J. Versluijs, H. Struyf, J. Van Olmen, and M. Van Hove, “Double patterning scheme for sub-0.25 *k1* single damascene structures at NA=0.75, λ=193nm,” *Proc. SPIE*, vol. 5754, pp. 1508-1518, May 2005.

[13] V. S. Basker *et al.*, “A 0.063 μm^2 FinFET SRAM cell demonstration with conventional lithography using a novel integration scheme with aggressively scaled fin and gate pitch,” in *VLSI Symp. Tech. Dig.*, 2010, pp. 19-20.

[14] C. Y. Chang and S. Sze, “ULSI Technology,” McGraw-Hill Inc., New York, 1996, p.362.

[15] Y. Taur and T. H. Ning, “Fundamentals of modern VLSI devices,” Cambridge Univ. Press, New York, 1998, p.142.

[16] L. D. Yau, “A simple theory to predict the threshold voltage of short-channel IGFET’s,” *Solid-State Electronics*, vol. 17, no. 10, pp. 1059-1063, 1974.

Table 2-1 Overall implantation conditions used in the n-MOSFET fabrication.

Conditions	Ion	Energy / Dose / Tilt angle / Twist angle
P-well	BF_2^+	70 keV / 1×10^{13} cm^{-2} / 7° / 22°
Channel Stop	BF_2^+	120 keV / 4×10^{13} cm^{-2} / 7° / 22°
V_{th}	BF_2^+	40 keV / 1×10^{13} cm^{-2} / 7° / 22°
APT	B^+	35 keV / 5×10^{12} cm^{-2} / 7° / 22°
Halo	BF_2^+	50 keV / 2.5×10^{12} cm^{-2} / 45° / 27°
S/D extension	As^+	10 keV / 1×10^{15} cm^{-2} / 0° / 0°
Deep S/D	As^+	20 keV / 5×10^{13} cm^{-2} / 0° / 0°

Table 2-2 Overall implantation conditions used in the p-MOSFET fabrication.

Conditions	Ion	Energy / Dose / Tilt angle / Twist angle
N-well	P_{31}^+	120 keV / 7.5×10^{12} cm^{-2} / 7° / 22°
Channel Stop	As^+	120 keV / 3×10^{12} cm^{-2} / 7° / 22°
V_{th}	As^+	80 keV / 1×10^{13} cm^{-2} / 7° / 22°
APT	P_{31}^+	120 keV / 4×10^{12} cm^{-2} / 7° / 22°
Halo	As^+	50 keV / 2.5×10^{12} cm^{-2} / 45° / 27°
S/D extension	BF_2^+	10 keV / 5×10^{14} cm^{-2} / 0° / 0°
Deep S/D	BF_2^+	15 keV / 5×10^{13} cm^{-2} / 0° / 0°

Table 2-3 Specifications of Canon FPA-3000i5+ Stepper.

Resolution	0.35 micron (dense lines)
NA	0.63 – 0.45 (automatically variable)
Reticle Size	5-inch
Reduction Ratio	5:1
Field Size	20 mm x 20 mm
Overlay Accuracy	Mean + 3 sigma ≦ 45 nm
Throughput	100 wph (200 mm)

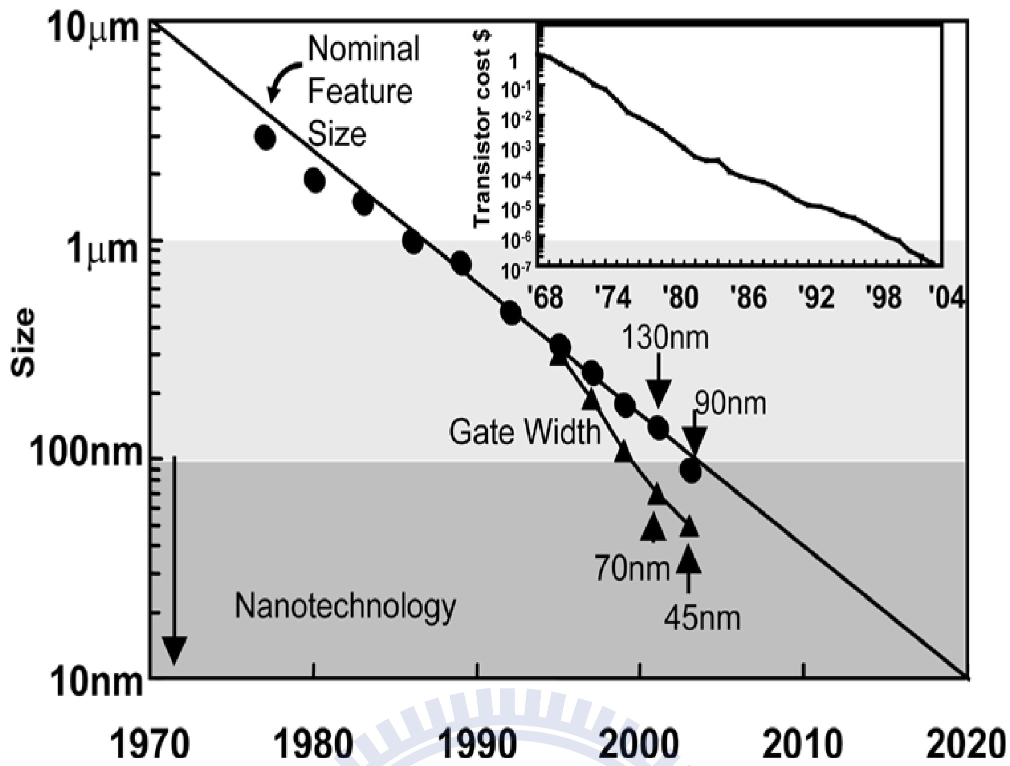


Fig. 2-1 Transistor cost and scaling trend of channel length versus years for technology node [1].

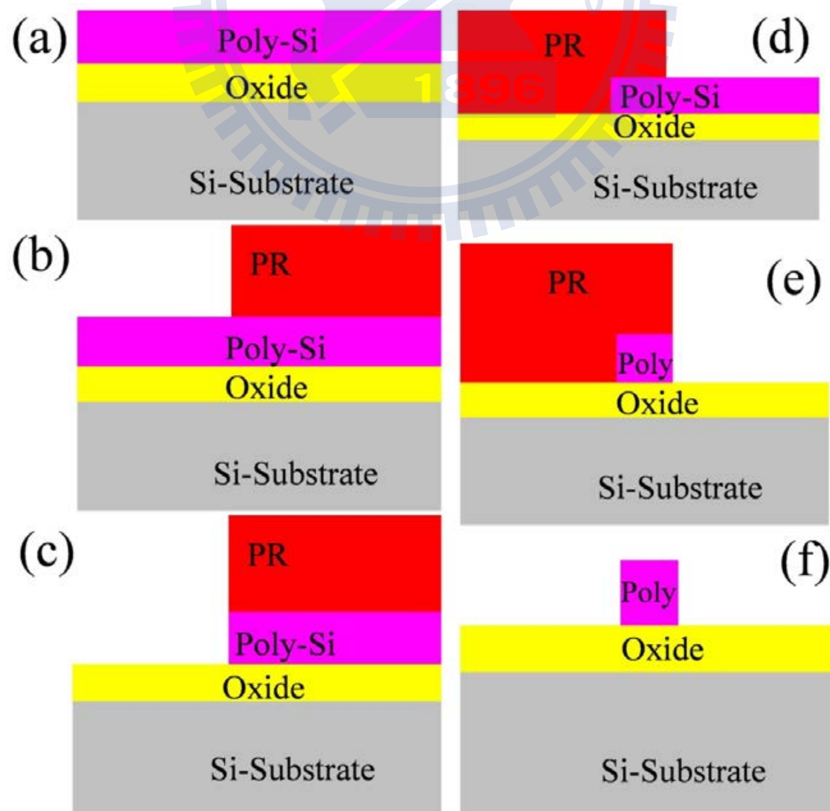


Fig. 2-2 Process flow of poly-Si gate formation with double patterning technique.

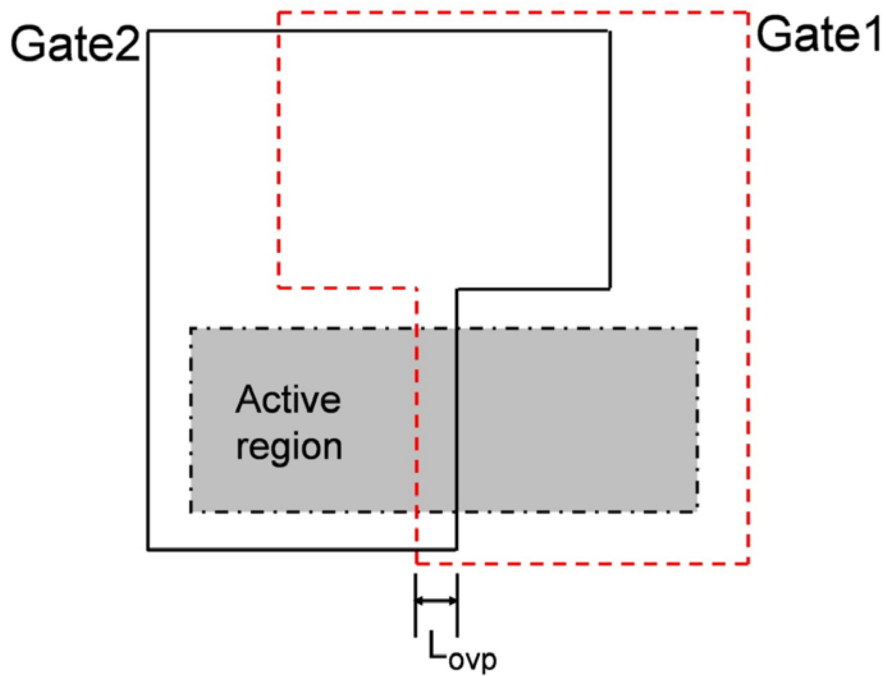


Fig. 2-3 Mask layouts of the first (G1) and second (G2) gate patterns for defining the gate pattern on the active region. Gate length (L_{ovp}) of the final gate is determined by the overlap region of the two gate patterns.

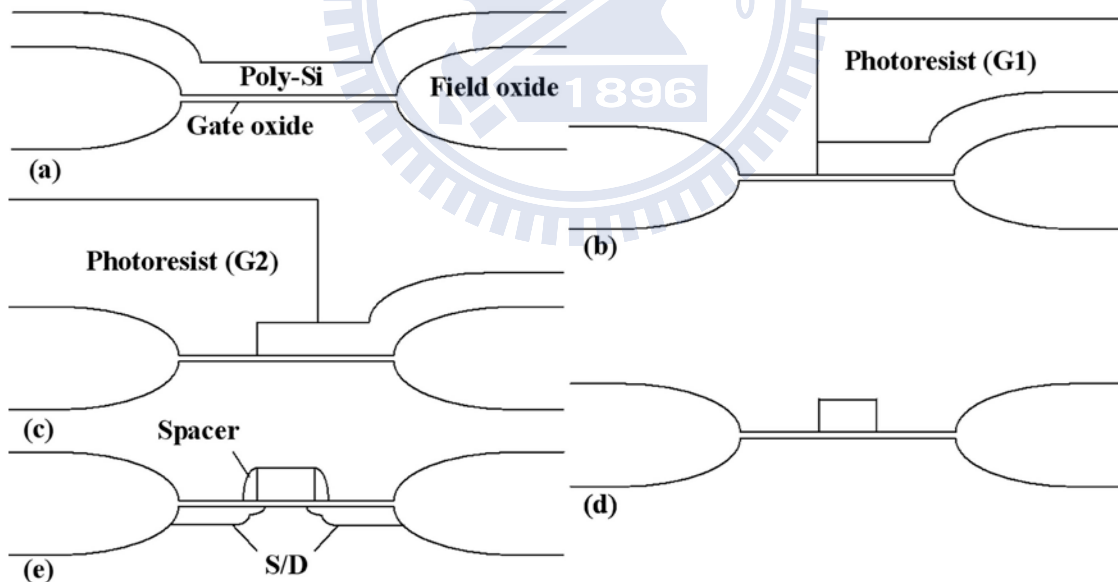


Fig. 2-4 Major process steps for fabricating n-MOSFETs with the DP method. (a) Formation of gate oxide and poly-Si on Si wafer with LOCOS isolation. (b) Generation of first PR pattern (G1), followed by the first poly-Si etching. (c) Generation of second PR pattern (G2) after removing the first PR. (d) Completion of the poly-Si gate after second poly-Si etching and subsequent PR removal. (e) Formation of S/D structure.

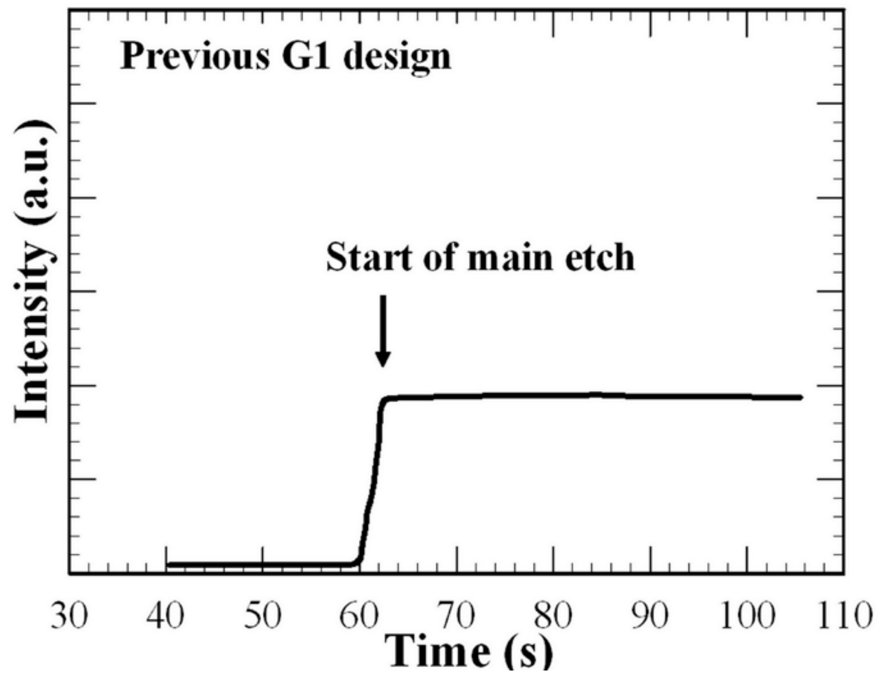


Fig. 2-5 Typical optical emissive signal recorded during the main etching stage of the second gate etching with the original mask design. No end point was detected.

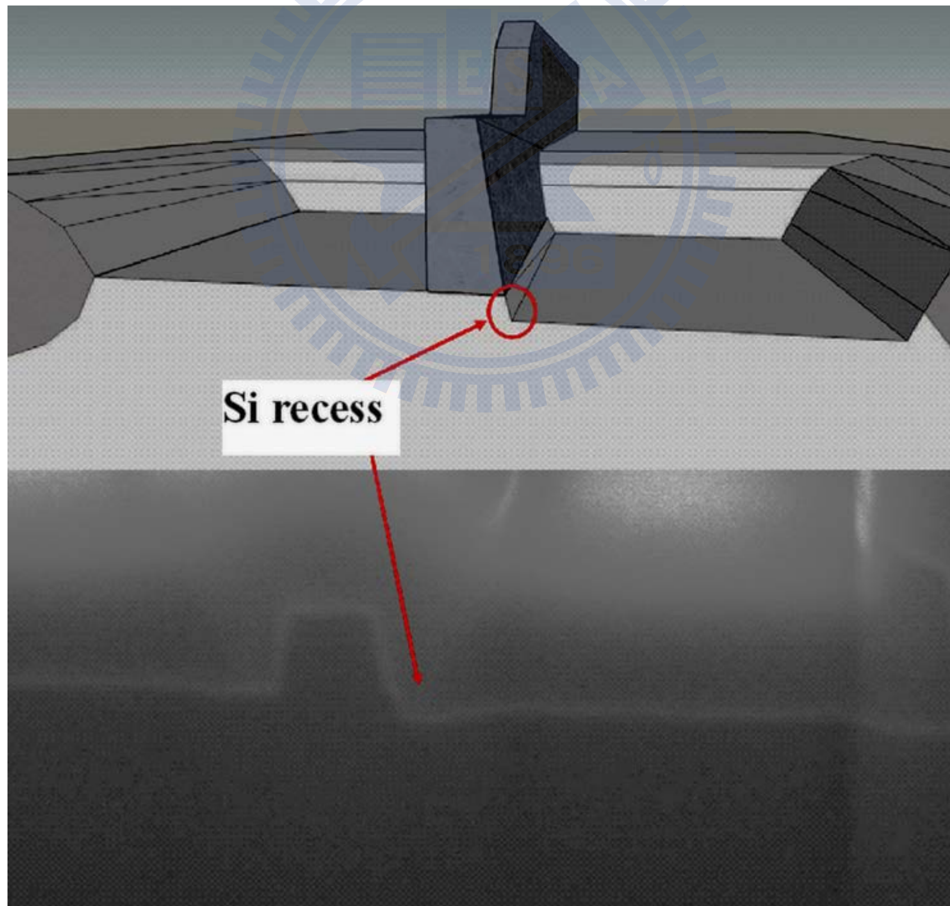


Fig. 2-6 Cross-sectional SEM view of a MOSFET showing an etch-induced recess at the right side of the gate. Top illustration is used to help visualize the structure. The recess was formed during the G2 etching stage due to the failure of EPD.

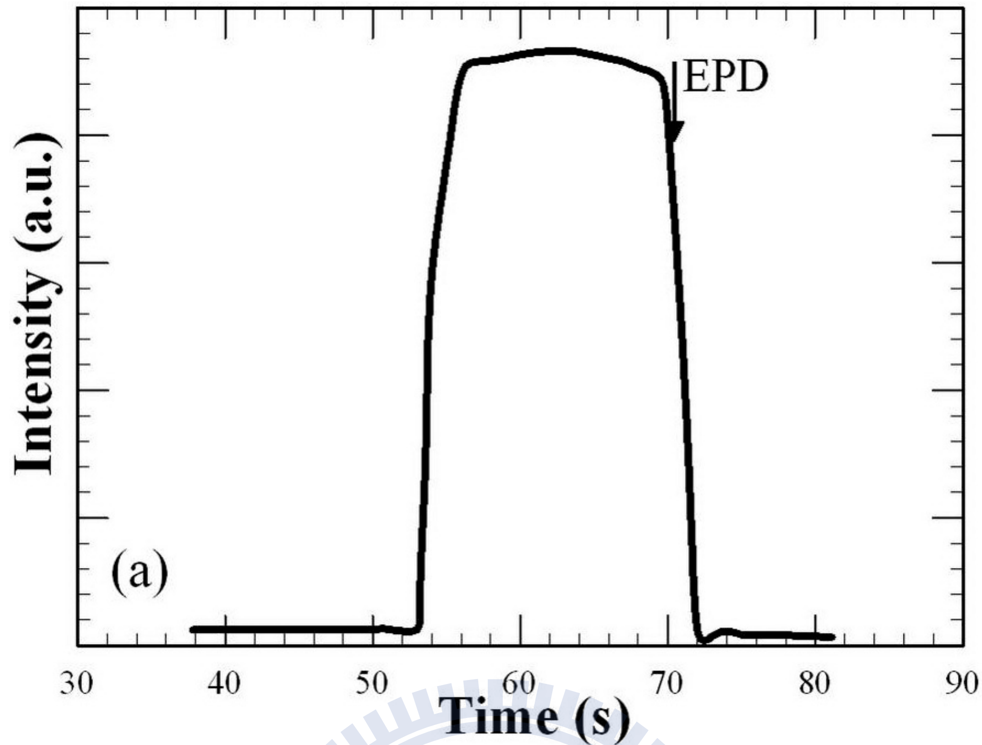


Fig. 2-7 (a) Optical emissive signal recorded during the main etching stage of the first gate etching step with the modified mask design.

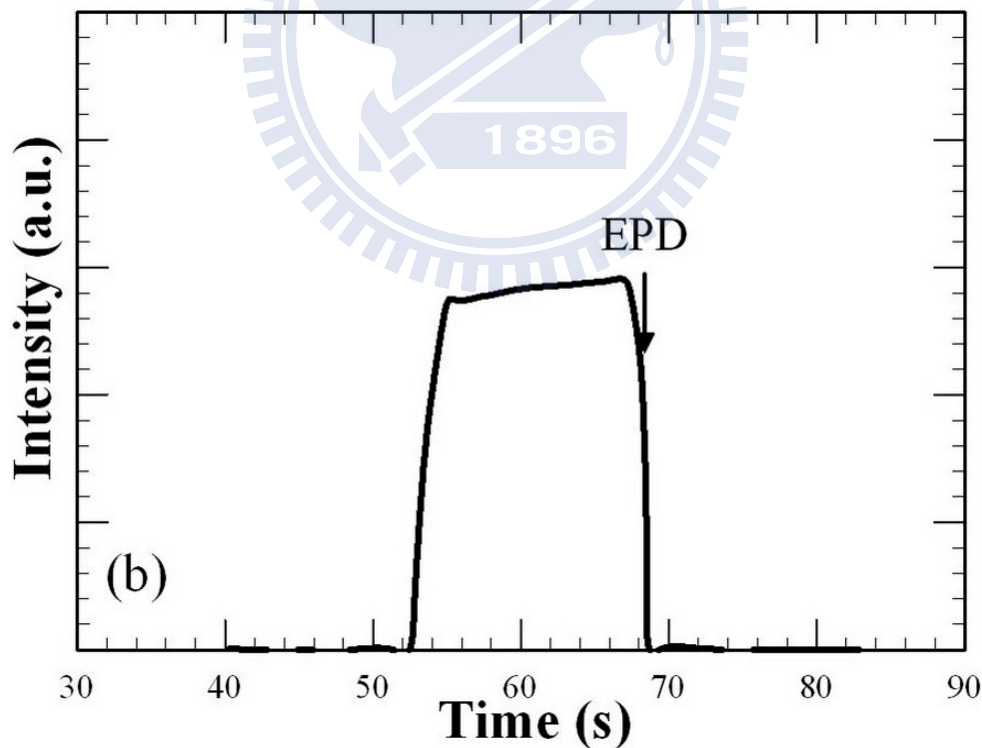


Fig. 2-7 (b) Optical emissive signal recorded during the main etching stage of the second gate etching step with the modified mask design. Successful EPD is achieved in the two etch steps.

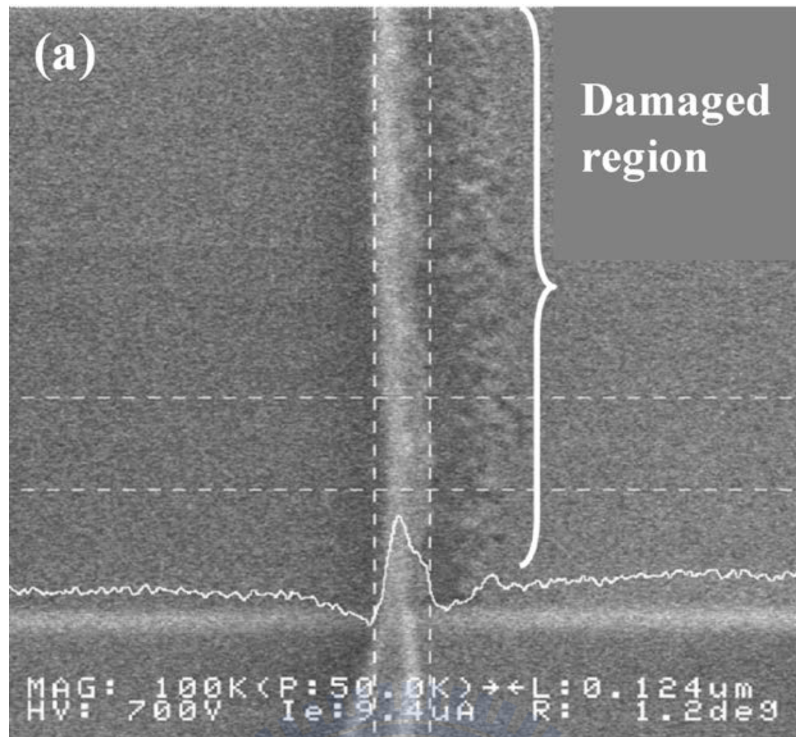


Fig. 2-8 (a) In-line SEM views of gate patterns on active region etched with original mask designs. The etch-induced damage region can be distinguished vividly.

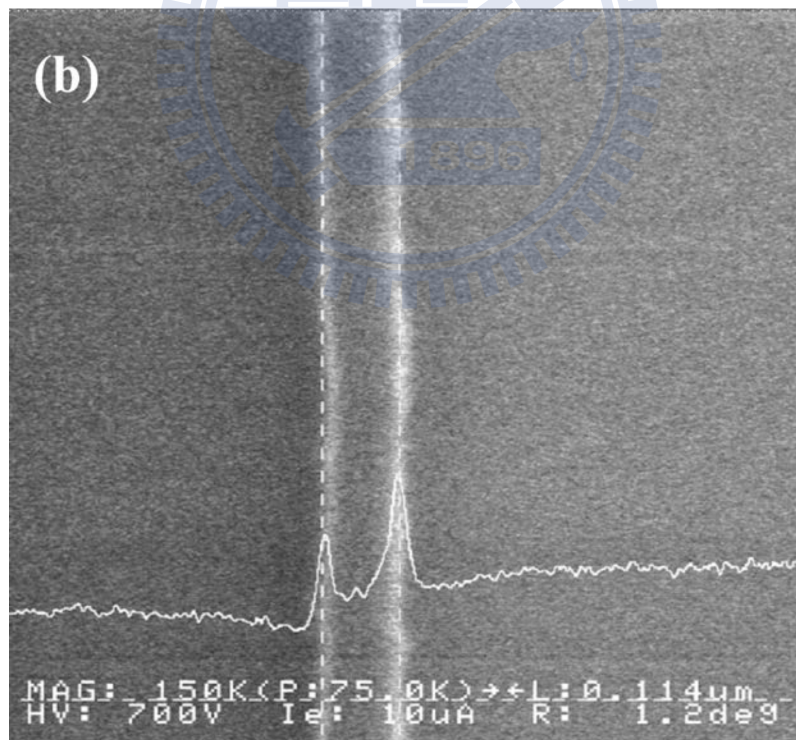


Fig. 2-8 (b) In-line SEM views of gate patterns on active region etched with modified mask designs. The etch recess phenomenon can be resolved with the modified mask design.

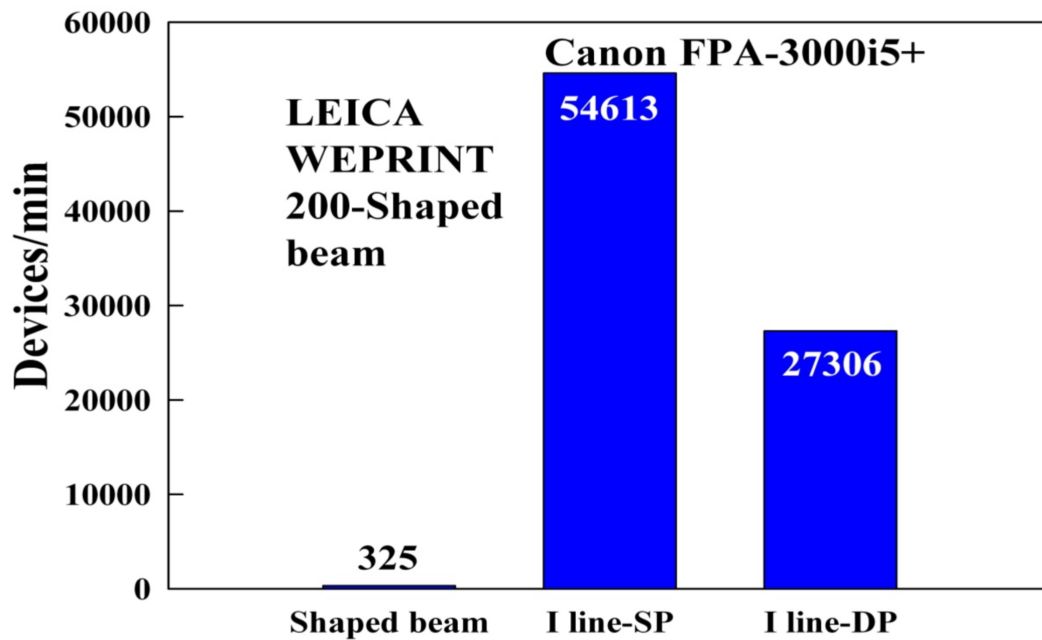


Fig. 2-9 Throughput of two lithography tools.

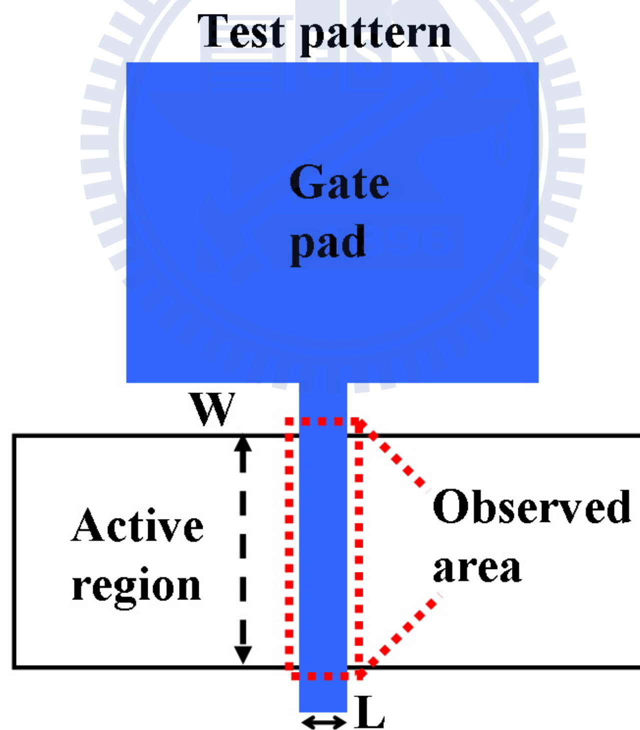


Fig. 2-10 Mask layout for defining the gate pattern and observed area on the active region marked with a red dashed line.

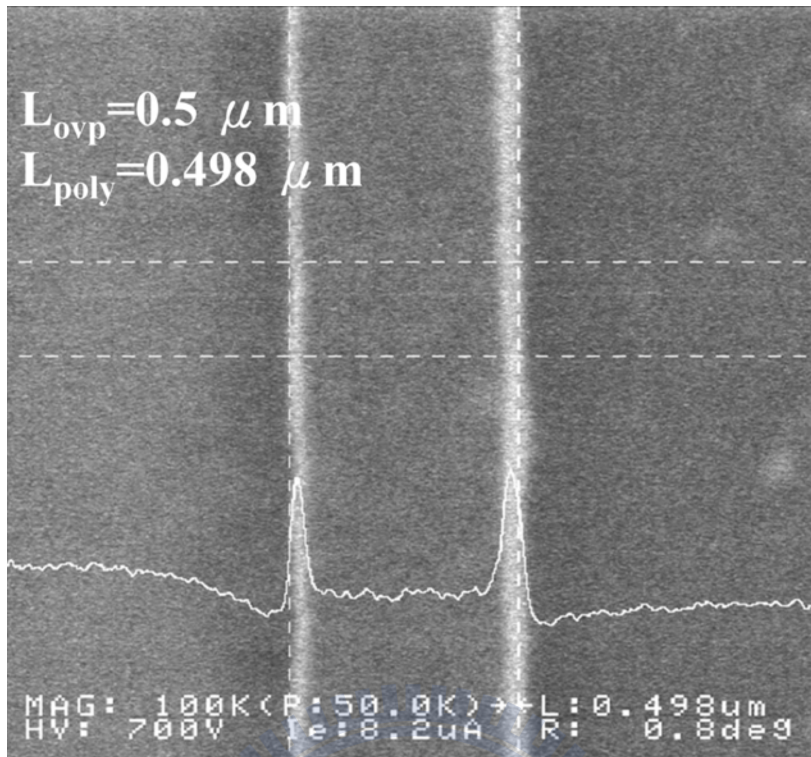


Fig. 2-11 (a) In-line SEM image of a patterned poly-Si line with nominal line width of 500 nm. The measured line width in this case is 498 nm.

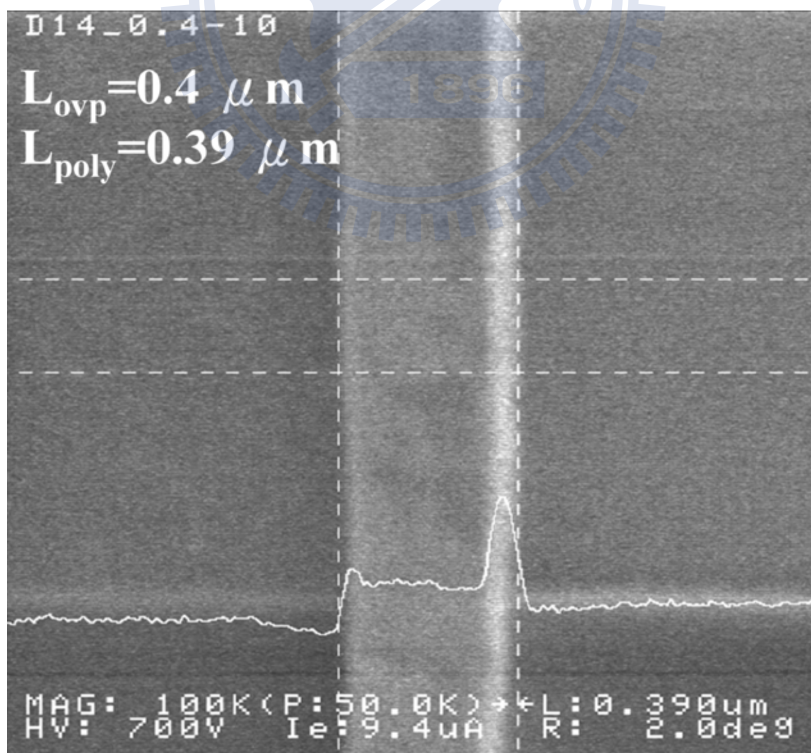


Fig. 2-11 (b) In-line SEM image of a patterned poly-Si line with nominal line width of 400 nm. The measured line width in this case is 390 nm.

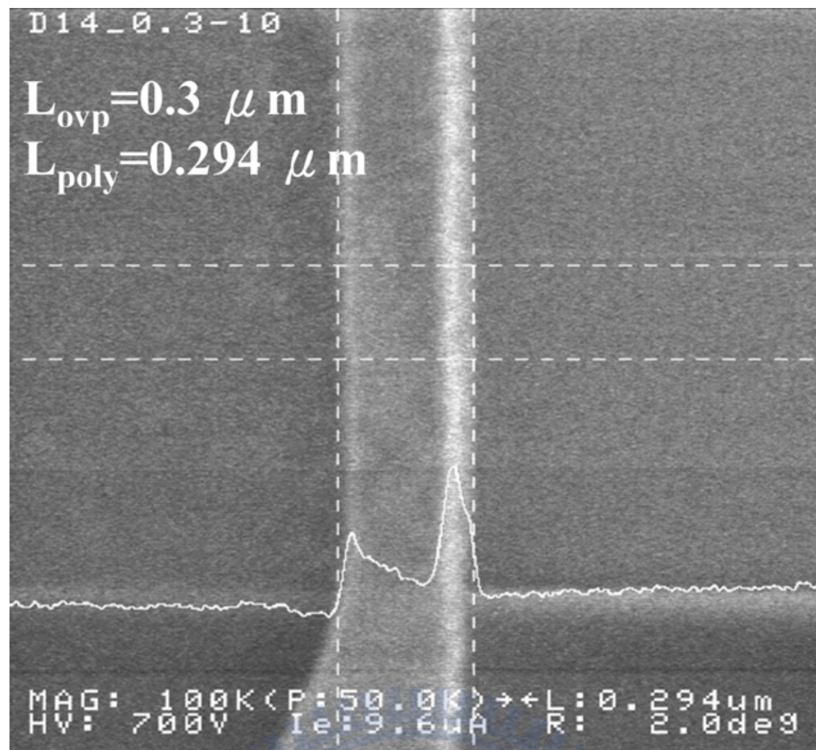


Fig. 2-11 (c) In-line SEM image of a patterned poly-Si line with nominal line width of 300 nm. The measured line width in this case is 294 nm.

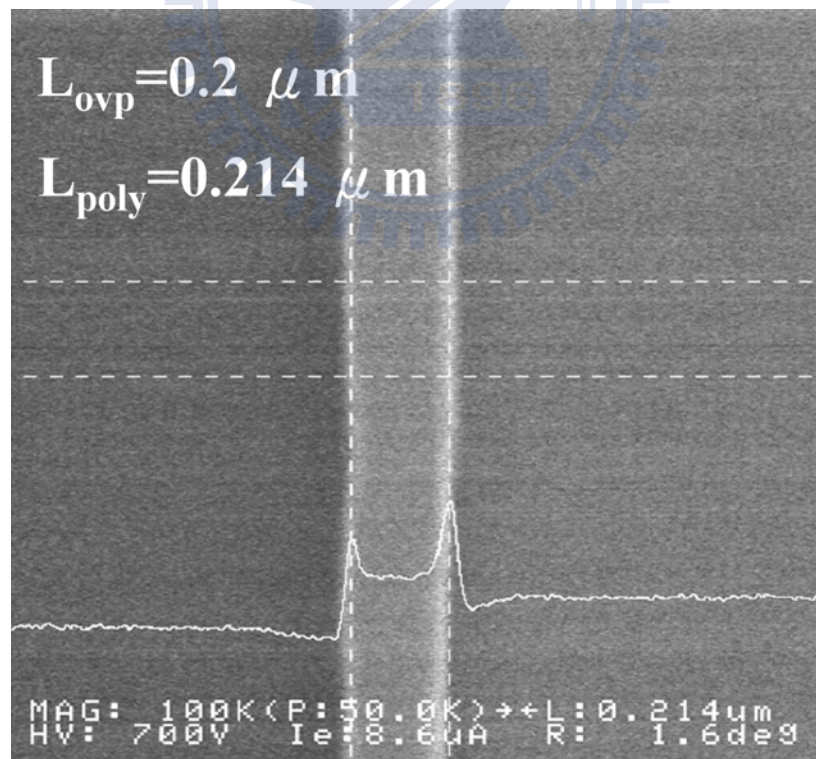


Fig. 2-11 (d) In-line SEM image of a patterned poly-Si line with nominal line width of 200 nm. The measured line width in this case is 214 nm.

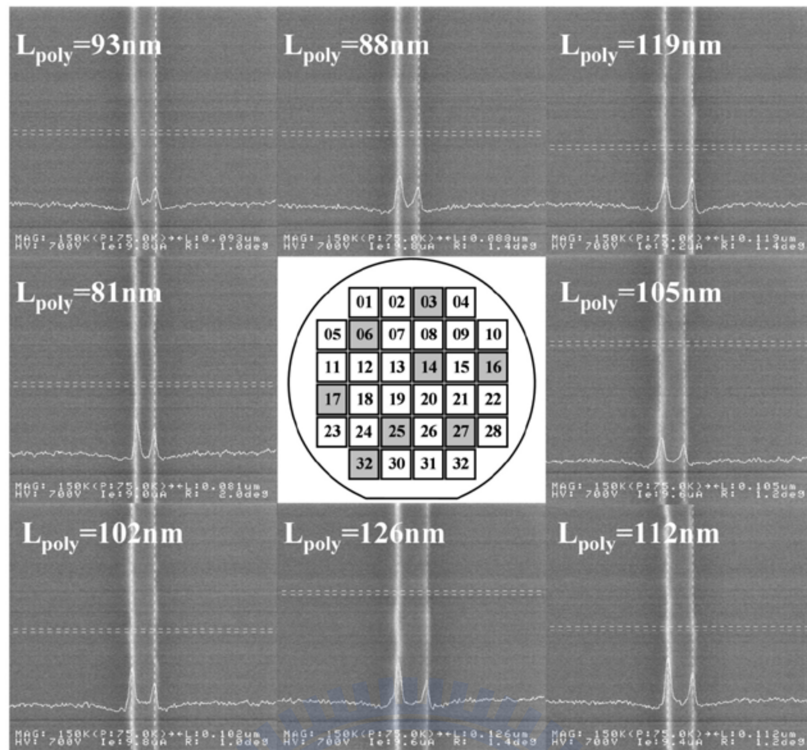


Fig. 2-12 In-line SEM images of patterned poly-Si lines located at eight different dies of a wafer with nominal line width of 100 nm.

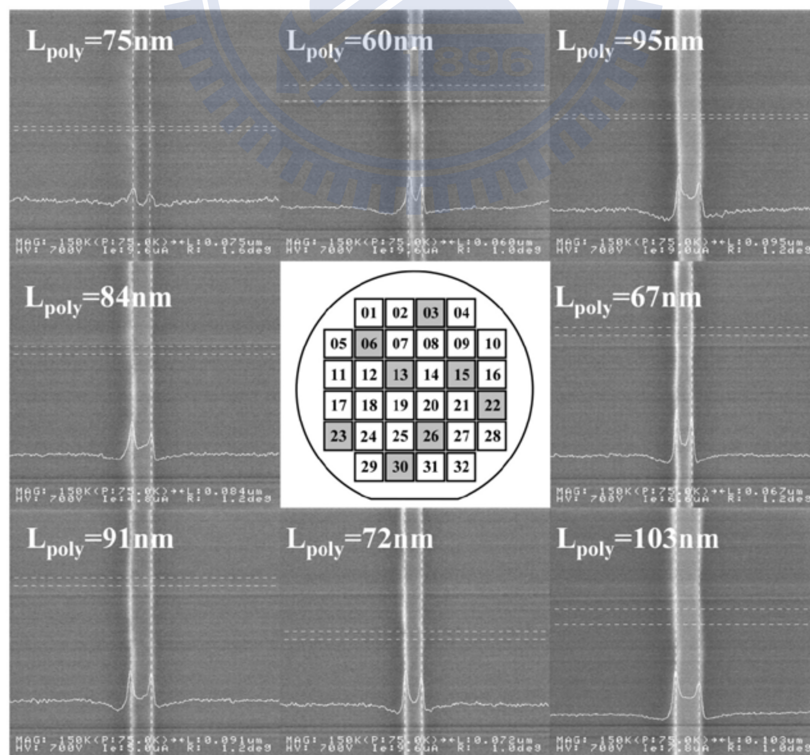


Fig. 2-13 In-line SEM images of patterned poly-Si lines located at eight different dies of a wafer with nominal line width of 80 nm.

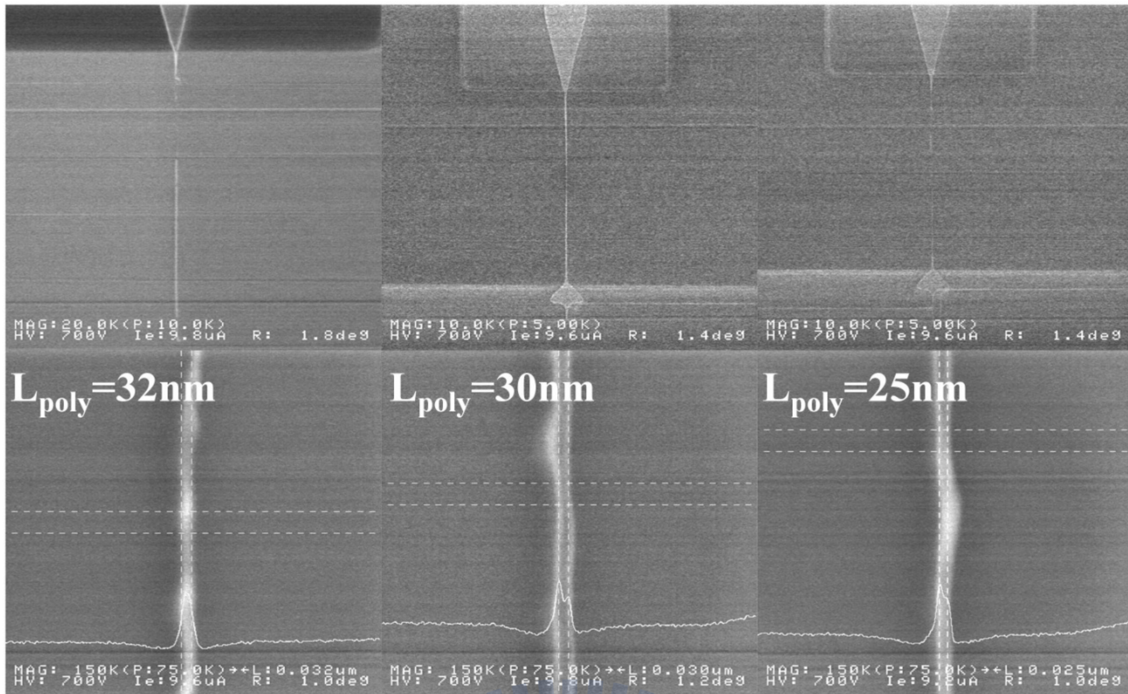


Fig. 2-14 In-line SEM images of patterned poly-Si lines randomly located on a wafer with nominally shortest line width of 50 nm.

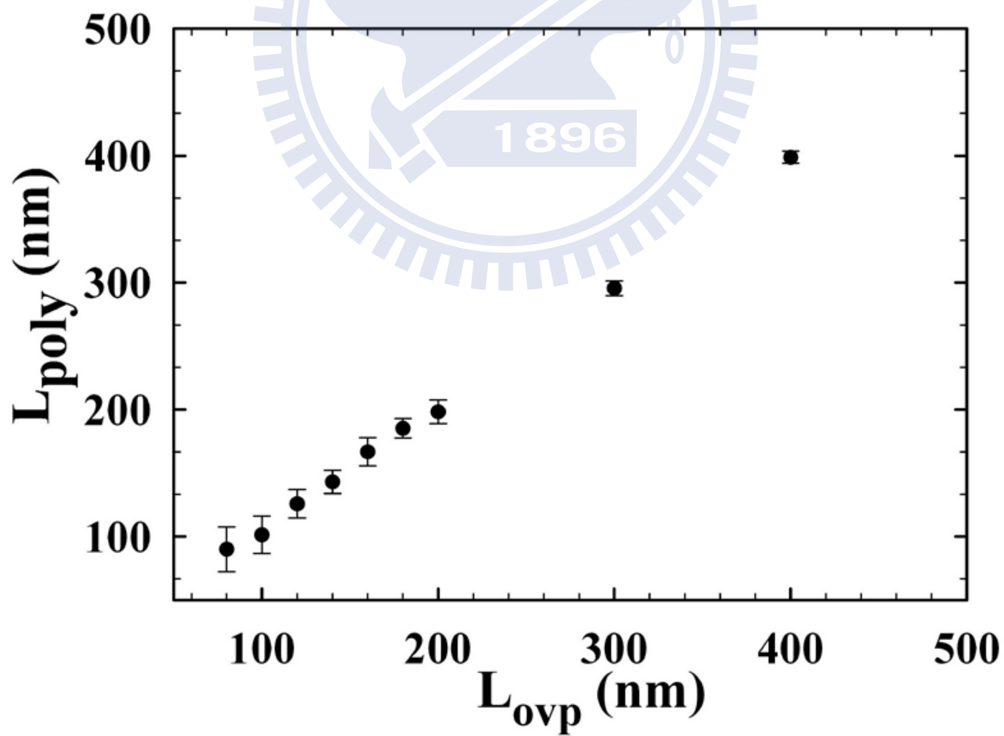


Fig. 2-15 Measured poly-Si gate length (L_{poly}) as a function of nominal gate length (L_{ovp}).

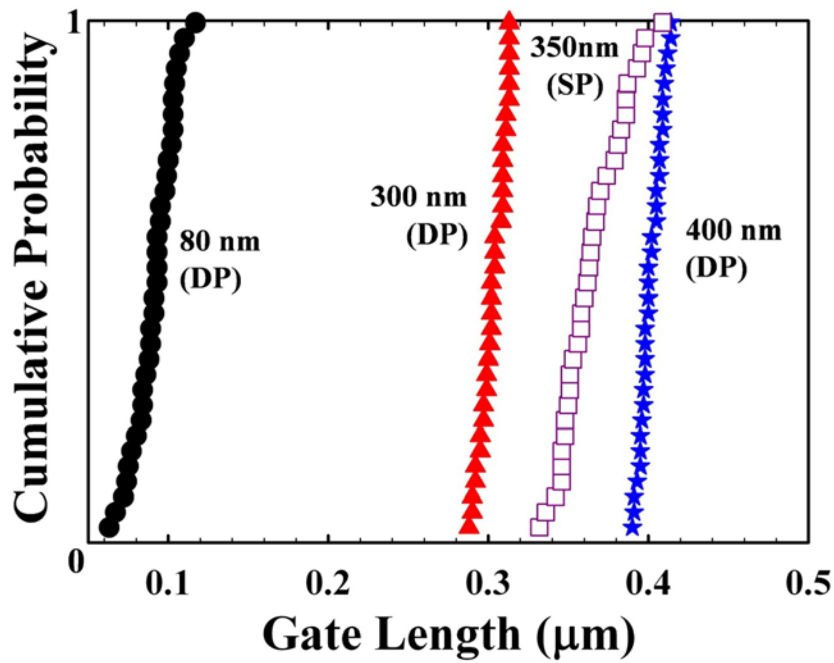


Fig. 2-16 Cumulative plots of poly-Si gates patterned with DP method with nominal length of 80, 300, and 400 nm, and with conventional single patterning (SP) with nominal length of 350 nm. Each curve represents the results measured from 35 test structures.

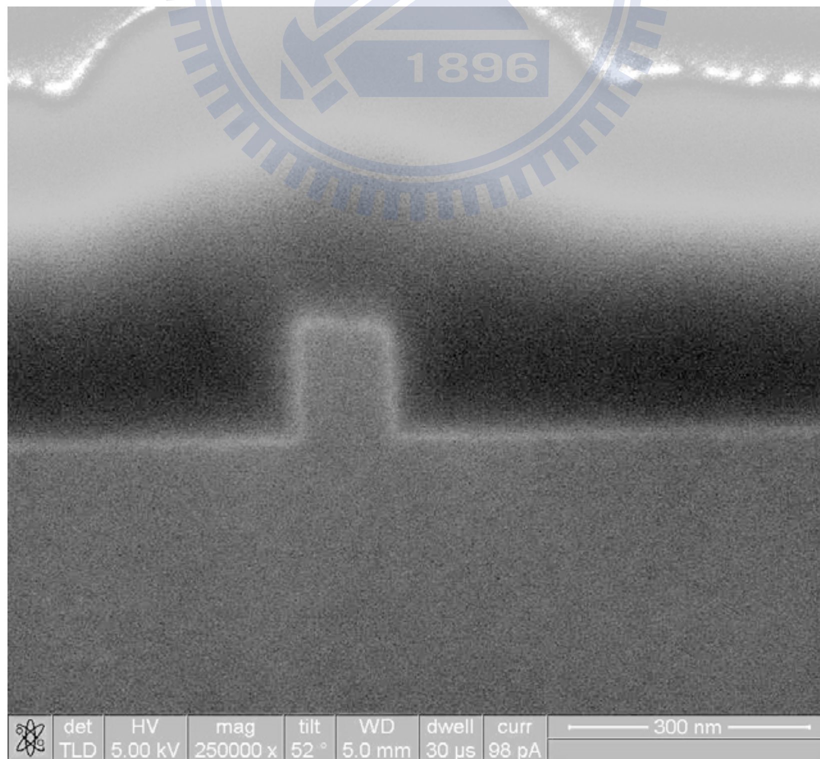


Fig. 2-17 Cross-sectional SEM image of a fabricated device with nominal gate length of 120 nm. Practical length was measured to be 115 nm.

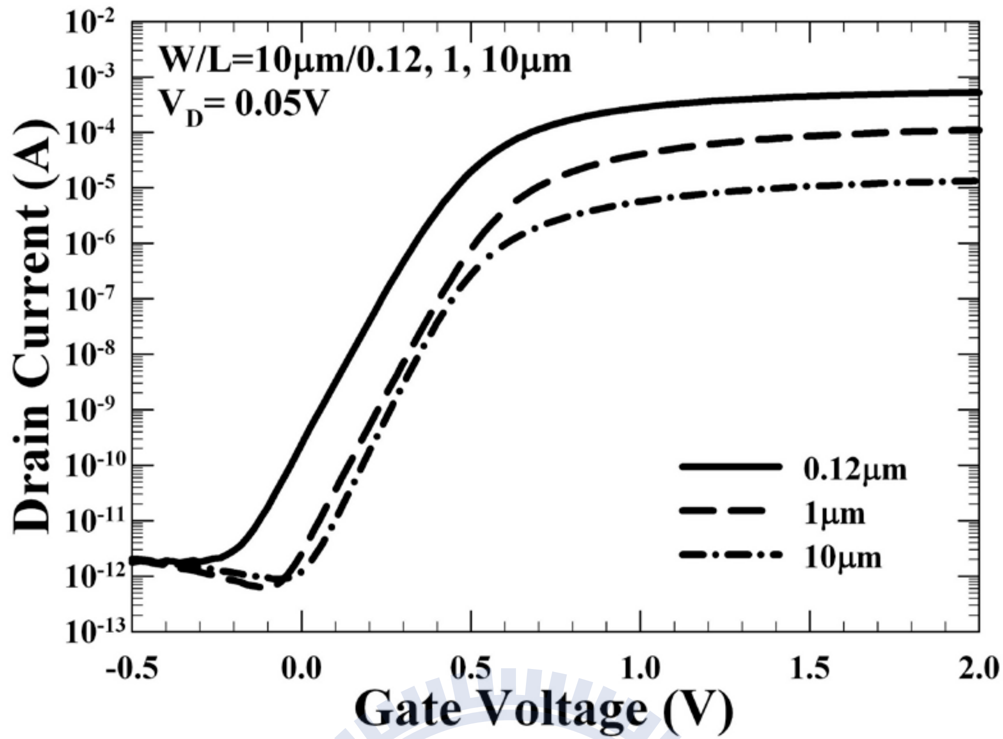


Fig. 2-18 (a) Transfer characteristics of NMOS control split biased at V_D = 0.05V with various channel length ranging from 0.12 to 10 μm. All devices have the same width of 10 μm.

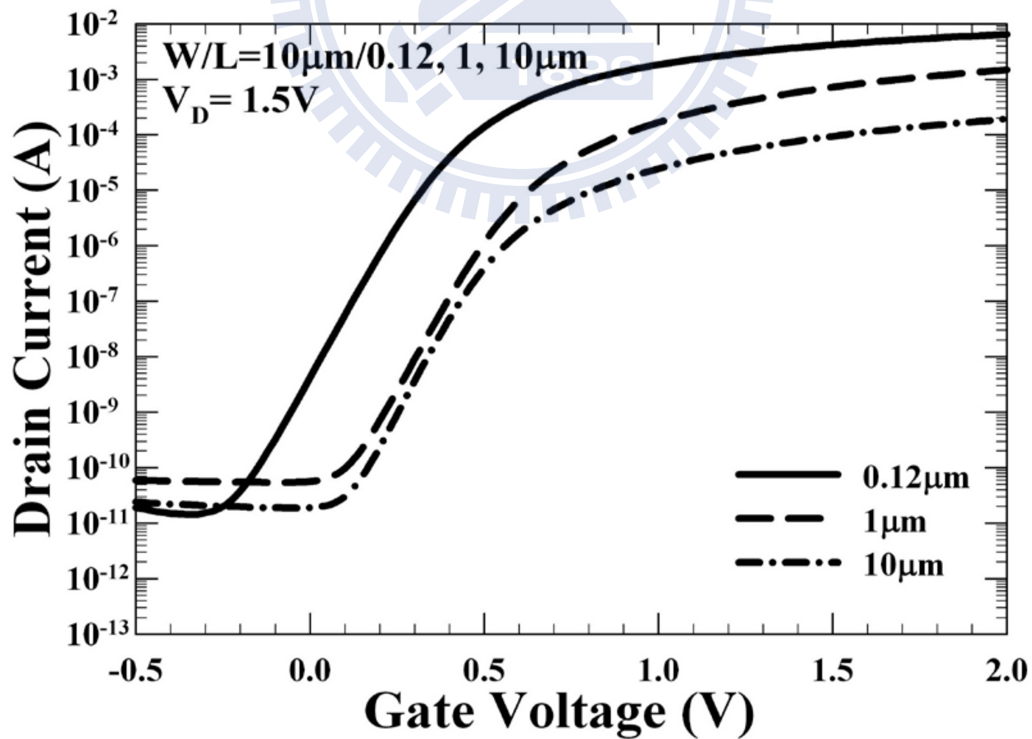


Fig. 2-18 (b) Transfer characteristics of NMOS control split biased at V_D = 1.5V with various channel length ranging from 0.12 to 10 μm. All devices have the same width of 10 μm.

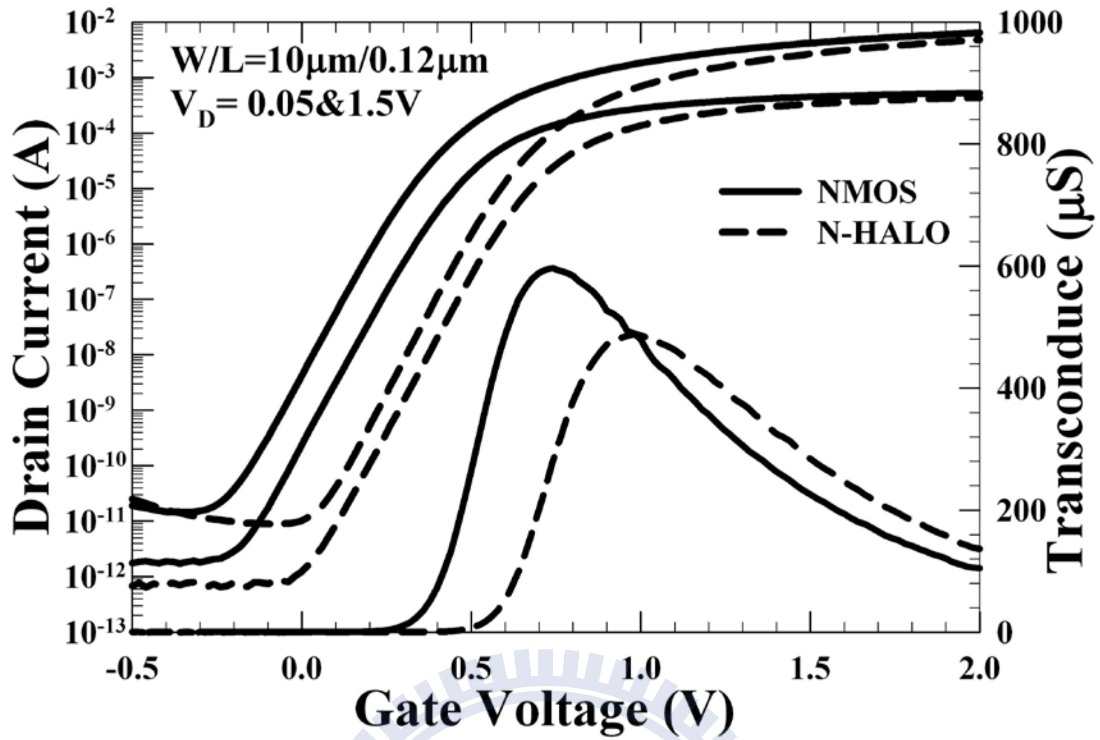


Fig. 2-19 (a) Transfer characteristics of NMOS and N-HALO splits with W/L=10 μm/120 nm.

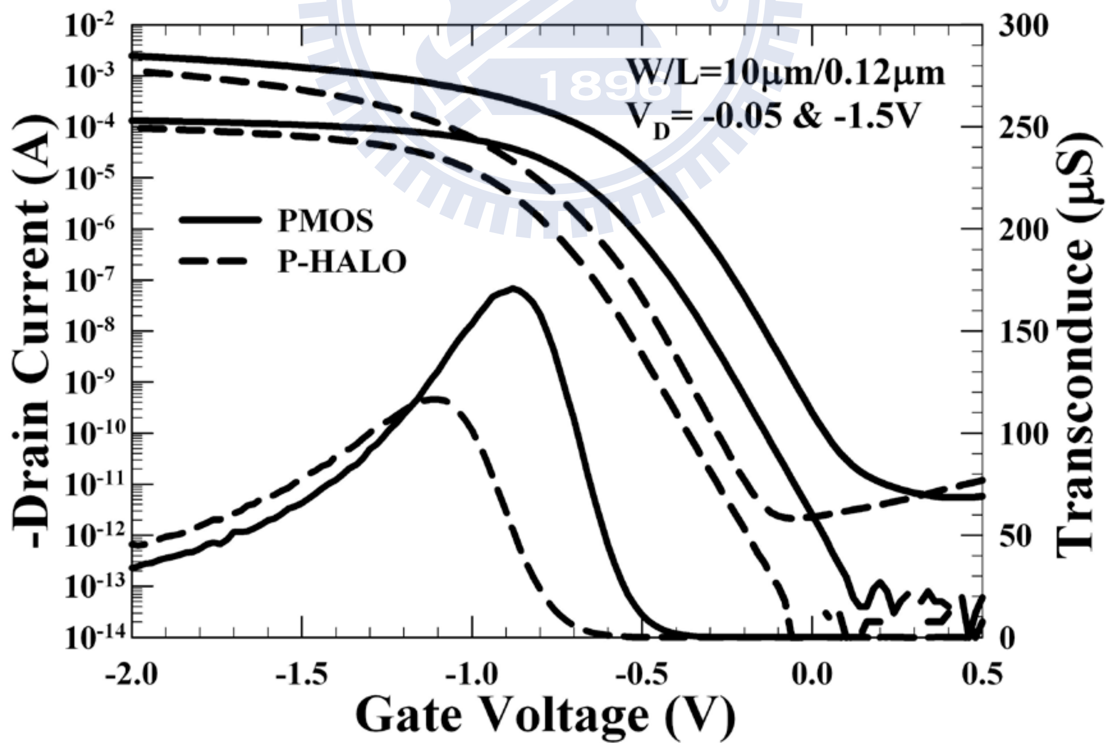


Fig. 2-19 (b) Transfer characteristics of PMOS and P-HALO splits with W/L=10 μm/120 nm.

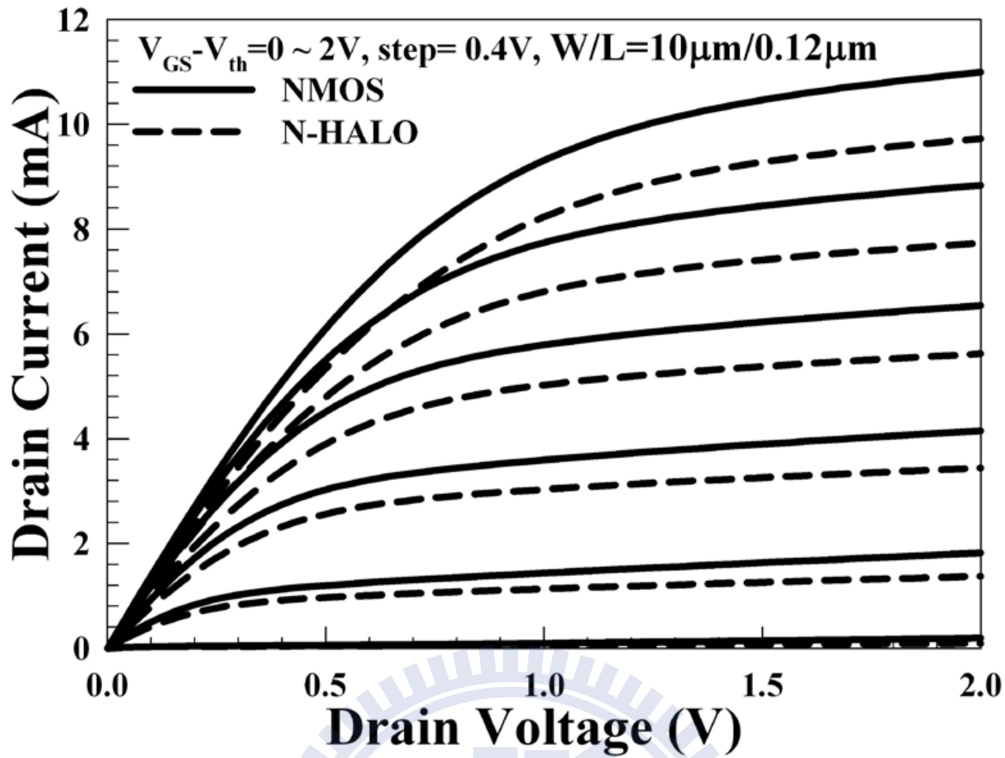


Fig. 2-20 (a) Output characteristics of NMOS and N-HALO splits with W/L=10 μm/120 nm.

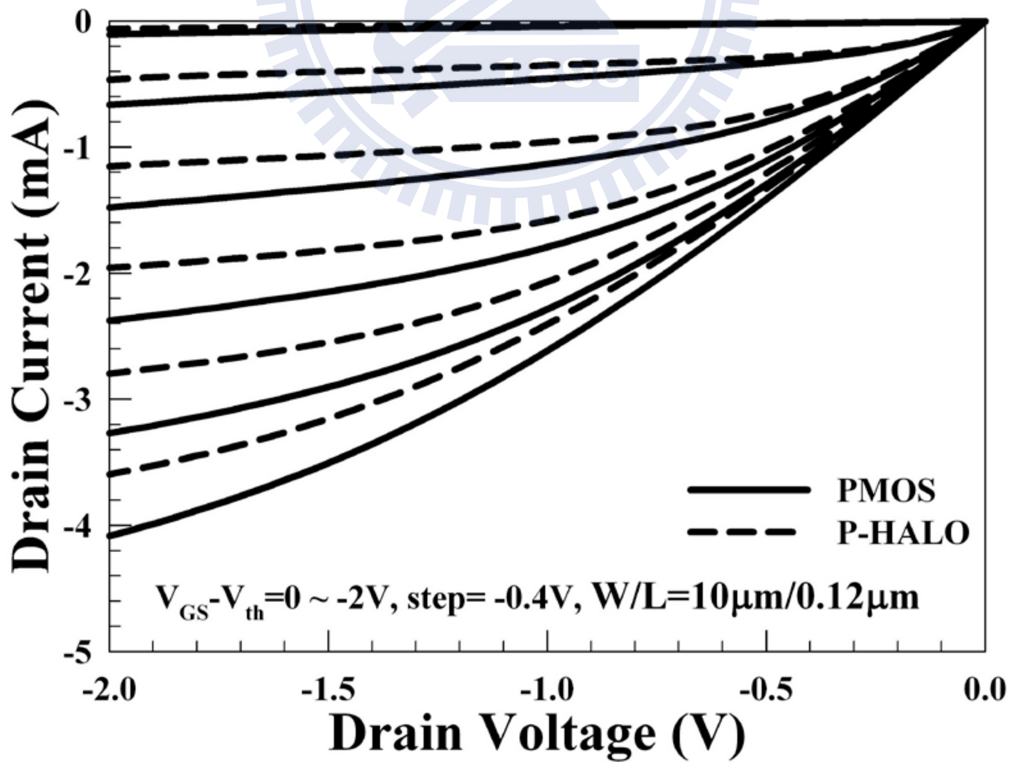


Fig. 2-20 (b) Output characteristics of PMOS and P-HALO splits with W/L=10 μm/120 nm.

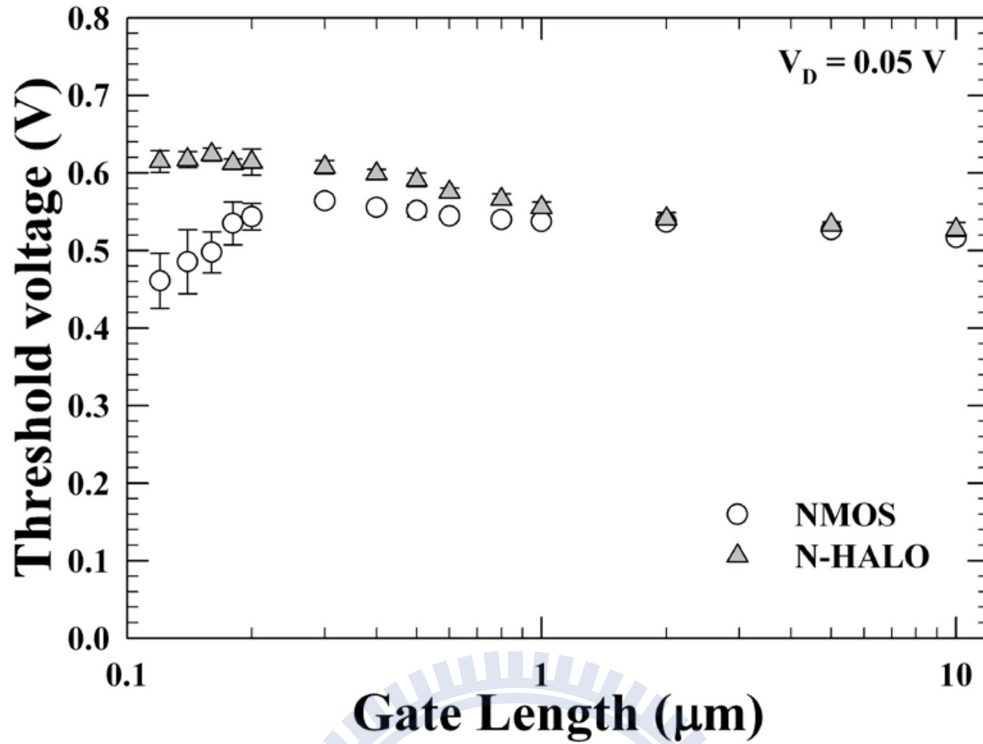


Fig. 2-21 (a) Threshold voltage as a function of gate length for NMOS and N-HALO splits.

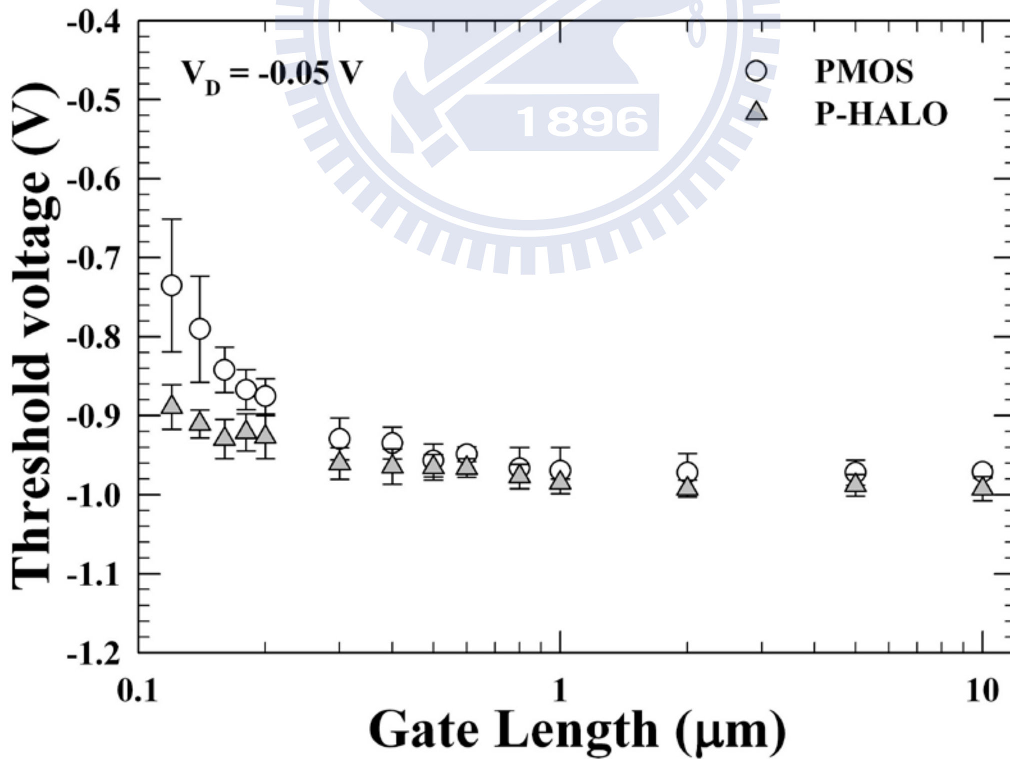


Fig. 2-21 (b) Threshold voltage as a function of gate length for PMOS and P-HALO splits.

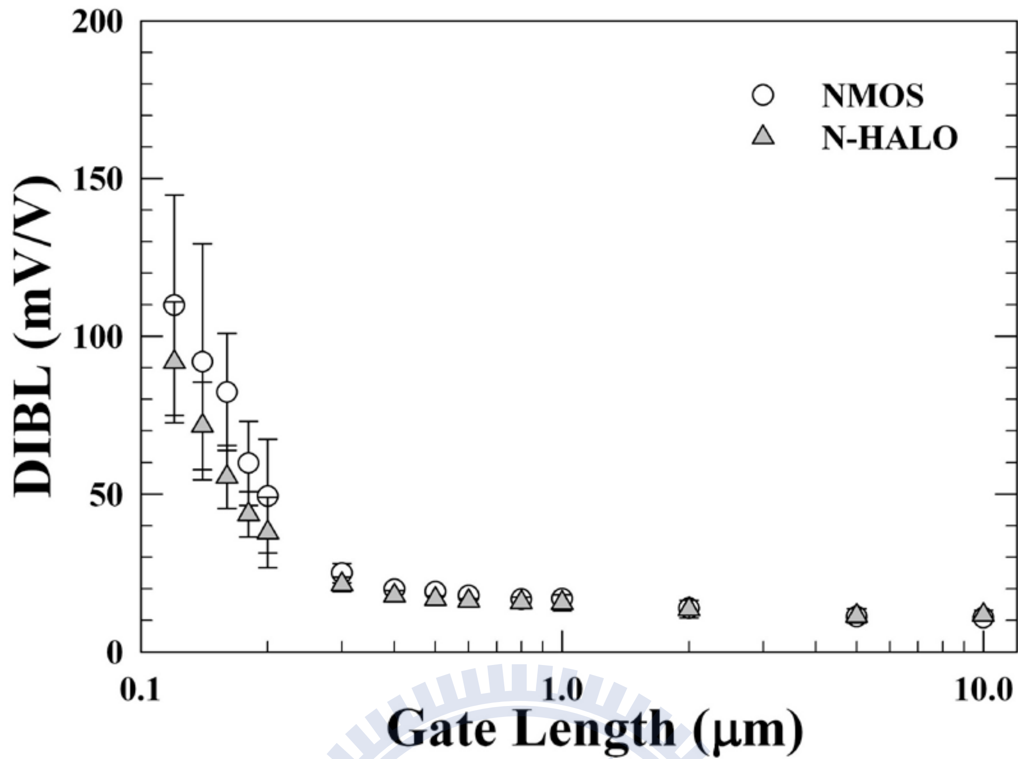


Fig. 2-22 (a) Drain induced barrier lowering (DIBL) as a function of gate length for NMOS and N-HALO splits.

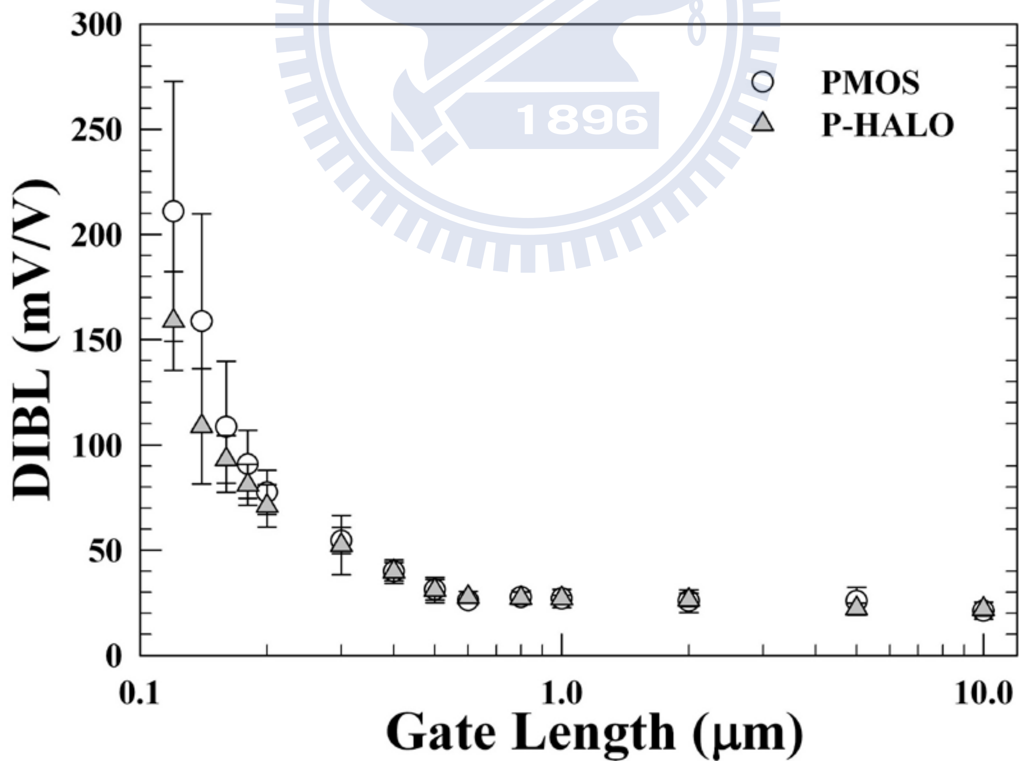


Fig. 2-22 (b) Drain induced barrier lowering (DIBL) as a function of gate length for PMOS and P-HALO splits.

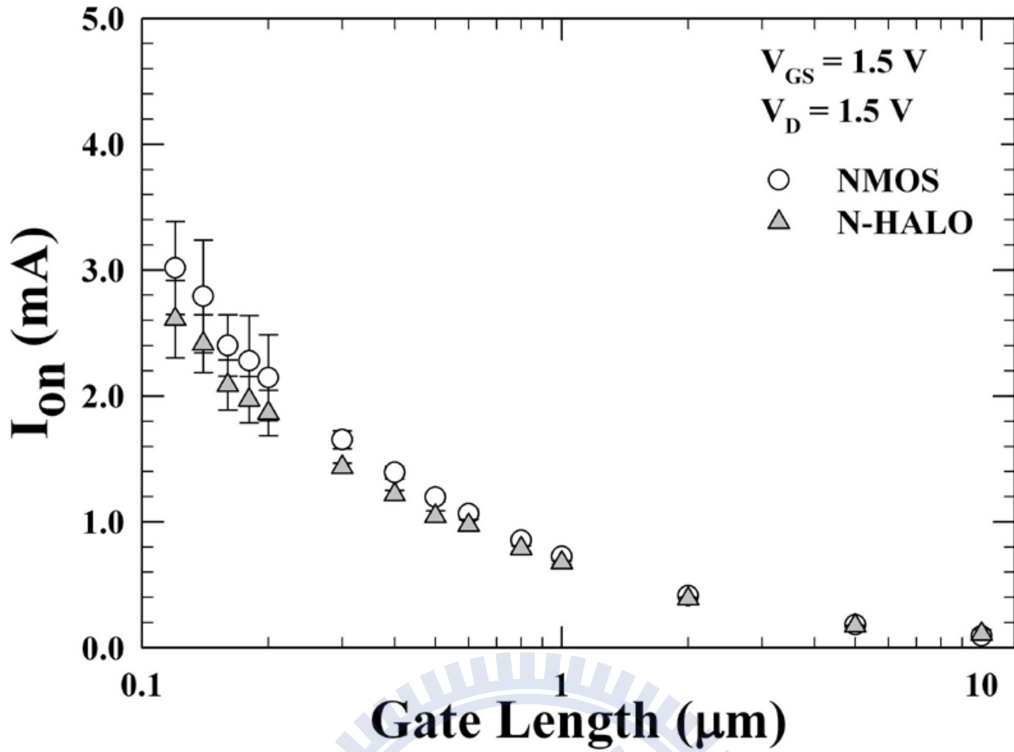


Fig. 2-23 (a) On-current at V_{GS} = 1.5V and V_D = 1.5V as a function of gate length for NMOS and N-HALO splits.

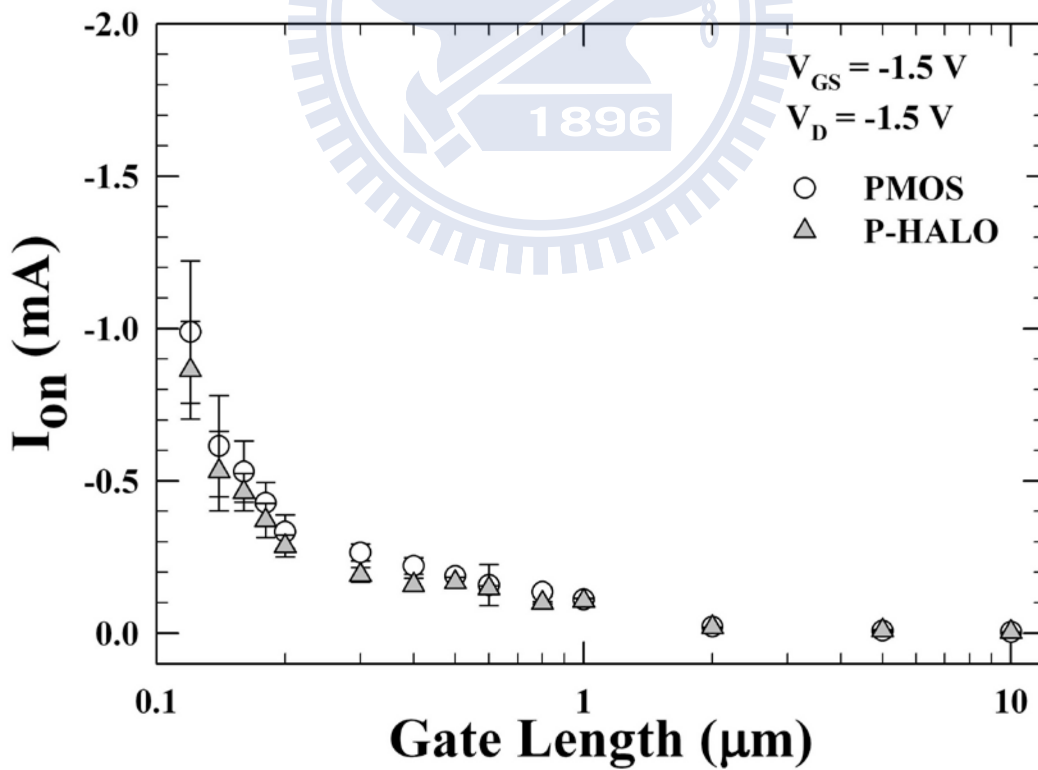


Fig. 2-23 (b) On-current at V_{GS} = -1.5V and V_D = -1.5V as a function of gate length for PMOS and P-HALO splits.

Chapter 3

A Comparison of Nano-scale Patterning Techniques

3.1 Introduction

Lithography has been playing a pivotal role in semiconductor manufacturing to keep the Moore's Law in force since the inception of integrated circuits (IC). Actually the advancements of both lithography tools and associated processes have paved the way for the successful evolution of IC technology. Figure 3-1 displays the lithography roadmap for the potential solutions of dynamic random access memory (DRAM), micro processor unit (MPU) and Flash, respectively, predicted by the International Technology Roadmap for Semiconductors (ITRS) in 2012 [1], indicating that the continuous scaling of the devices is evitable for better performance and cheaper manufacturing cost. In recent years, 32 nm technology node employs the 193 nm immersion lithography tools for mass production [2]-[3]. However, the aforementioned advanced lithography modules accomplish a finer resolution at the expense of incredibly high tool and process costs which are usually not affordable in the university-based laboratories. As a result, a large part of academic studies focusing on exploring the properties and physics of nano-scale strcutures in the university-based laboratories need to count on an alternative method, such as electron-beam direct writing [4], ion-beam lithography [5], photoresist (PR) ashing [6-7], nanoimprint lithography (NIL) [8-11], or utilizing the bottom-up methods like metal-catalytic growth [12], solid-liquid-solid growth [13], oxide-assisted growth [14], etc.

Certainly specific issues are present to each of the aforementioned approaches. The electron-beam and ion-beam lithography methods suffer from extremely low throughput as compared with the stepper-based photolithography, prohibiting them from being implemented in practical manufacturing [4-5]. The process development of NIL has been over one decade, but most of NIL processes are still slow and not proper to serve the purse of mass production. Some challenges, such as homogeneous heat transfer, recovery due to material time constant, and reduction of defects due to limited air dissolution or mechanical abrasion, are confronted as using thermal NIL [10-11]. For applying UV-NIL, fast curing speed, wetting, and nonreactive resists for enhancing the

lifetime of stamps are some of the major requests [9]. On the other hand, although the bottom-up approach like metal-catalytic growth provides more flexibility experimentally, it lacks good control over the dimensions, positioning, and alignment of nano-size structure. Plus, metal contamination [12] which would affect the device characteristics is also a concern.

From the viewpoints of both high-volume manufacturing and research, I-line steppers with mercury lamp as the exposure light source have been widely adopted for decades, and the correlated fabrication process is quite stable and well developed. Nevertheless, the fatality of I-line lithographic process is the resolution around 300 nm owing to its long exposure wavelength of 365 nm, and it is not likely to directly accomplish sub-100 nm line patterns. Even if the PR ashing method is capable of pushing the resolution of conventional I-line process down to the nano-scale regime, a highly stable asher is very pivotal for the purposes of good reproducibility and uniformity of critical dimension (CD) of the printed patterns. In addition, the profile of ashed PR pattern would be distorted or even collapsed due to high aspect ratio after over-ashing process for finer line pattern, and such poor PR pattern would ruin the subsequent etching step. As far as process cost and throughput are concerned, the conventional I-line lithographic process combined with double-patterning technique (DP) [15] is developed as an alternative approach for researches of sub-100 nm nano-scale devices carried out in the university-based laboratories. Besides, DP technique and related processes combined with spacer patterning technique such as self-aligned double patterning (SADP) [16] and sidewall spacer quadruple patterning [17] are proposed as the potential solutions for lithography roadmap, as previously illustrated in Fig. 3-1. Consequently, we have focused on and compared two kinds of lithographic systems often applied in universities for research purpose, including electron beam tool and I-line stepper in this chapter. The merits and shortcomings of some techniques using two lithographic systems are discussed in terms of CD uniformity, line edge roughness (LER), throughput, and minimum line width. We have also developed an ameliorative DP technique with conventional I-line stepper to generate sub-60 nm photoresist (PR) patterns with the goal to fabricate asymmetric devices of nano-scale regime in this work. Finally, 45 nm gate length HfO_2 dielectrics nMOSFETs with or without asymmetric channel doping were fabricated by the proposed I-line lithographic process and characterized as well.

3.2 Lithographic Experiments

3.2-1 Brief Illustrations of Lithographic Experiments

Before the execution of relative lithographic experiments discussed in this chapter, both test structure and observed area of line pattern are illustrated in Fig. 3-2 (a) for good comprehension of this section. Apparently, Fig. 3-2 (a) is applied for single-patterning schemes such as e-beam direct writing tools and PR ashing method. On the other hand, double-patterning processes such as conventional and modified double-patterning techniques are illustrated in Fig. 3-2 (b). The observed zone is marked with a red dashed line over the active region of device for all lithographic experiments discussed as follows.

3.2-2 Experiments of Electron Beam Systems

Two types of electron beam direct writing tools, namely, LEICA WEPRINT 200 and ELIONIX ELS-7500EX are employed in this study. The former belongs to the shaped beam type and the latter is classified as Gaussian beam system. The exposure doses are around 7.2 $\mu C/cm^2$ at 40 keV with the shaped beam system, and 10 $\mu C/cm^2$ at 50 keV with the Gaussian beam system, respectively. In-line scanning electron microscope (SEM) technique was used to characterize the resultant photoresist (PR) patterns. Figure 3-3 depicts the in-line SEM images of isolated PR line patterns sampled randomly on a six-inch wafer exposed by the shaped beam system, while the images exposed by the Gaussian beam system are shown in Fig. 3-4. Due to the extremely long exposure process of the Gaussian beam system, the sampling area is limited to around 2 cm $\times$ 2 cm for one chip and totally we have accomplished three chip areas. As can be seen in Fig. 3-3, the line widths of resultant PR patterns distribute from 78 to 120 nm located at eight different dies of a wafer, while the Gaussian beam system exhibits the distribution from 69 to 111 nm in an area of 2 cm $\times$ 6 cm as shown in Fig. 3-4, indicating the Gaussian beam system is capable of generating finer line patterns.

3.2-3 Experiments of I-Line Stepper with PR Ashing Method

For all photolithographic steps carried out in this work, we used an I-line stepper (Canon FPA-3000i5+) to generate the PR patterns. First, the line width of PR pattern around 300 nm was implemented with modulating the exposure doses and focuses of

I-line stepper. To accomplish the finer line width of nano-scale regime, we adopted the PR ashing technique with oxygen plasma in a low process temperature environment to reduce the PR trimming rate and increase the process uniformity. The PR patterns were trimmed by oxygen plasma at RF power of 700 W for top electrode and 20 W for bottom electrode with oxygen flow rate of 35 sccm and chlorine flow rate of 20 sccm, and the process temperature and pressure were set to 65 ^{o}C and 80 mtorr, respectively. The over-ashing PR patterns causing the LER degradation and/or the broken lines are shown in Fig. 3-5. Apparent broken lines, severe LER of PR patterns, and further the collapsed PR patterns suggest that the narrowest line patterns below 70 nm are not suitable to be generated directly by PR ashing method. Fig. 3-6 exhibits the in-line SEM images of isolated PR line patterns randomly sampled at eight different dies of a six-inch wafer generated by PR ashing method in a proper manner. The fluctuation of line width is about 56 nm, larger than 42 nm of the electron beam system, and the observed shortest line width is 84 nm, far thicker than the electron beam tool, and further the resultant PR patterns of less than 80 nm display terrible shapes, implying that PR ashing scheme gives self-imposed limitations on the implementation of finer line pattern generation.

3.2-4 Experiments of I-Line Stepper with Double Patterning Method

Another way to generate sub-100 nm line patterns through the conventional I-line process was done with the double patterning (DP) [15] technique. Figure 3-2 (b) shows the illustration of the two masks, denoted as G1 and G2, used for the DP method to define the gate electrode. The detailed process of DP technique basically is the same as that previously described in chapter 2. In brief, the process follows a lithography-etching-lithography-etching sequence which involves two separate masks, and the overlap regions of the two masks define the final etched structures on the wafer surface. In-line SEM images of randomly sampled line patterns at eight different dies of a six-inch wafer generated by DP method are depicted in Fig. 3-7. The overlay accuracy of the employed I-line stepper is about 45 nm which is one of the dominant factors for the CD deviation. As can be seen in the plots, the line widths of resultant PR patterns distribute from 81 to 126 nm, and the variation of 45 nm, mainly ascribed to the overlay accuracy of equipment, is better than PR ashing one.

3.2-5 Experiments of I-Line Stepper with Modified Double Patterning Method

The modified DP method (denoted as Modified I-DP) is similar to the aforementioned DP method (denoted as I-DP). The unique feature of Modified I-DP distinct from previous DP method is the implementation of oxide hard mask trimming employed during the first gate pattern definition. Figure 3-8 illustrates the major process steps in the fabrication of nMOSFETs with symmetric channel doping by virtue of the modified I-DP technique. After the lithographic process of first gate pattern with mask G1, the anisotropic etching of the tetraethyl orthosilicate (TEOS) oxide hard mask layer was implemented by a reactive ion etch (RIE) step done by a Lam-TCP9400, as illustrated in Fig. 3-8 (b). Prior to the implementation of second gate patterning, the oxide hard mask layer trimming was executed as illustrated in Fig. 3-8 (c), followed by the removal of PR (G1) and a RIE of polycrystalline silicon (poly-Si) layer below. The second lithographic step with mask G2 was then employed to generate PR patterns which covered portion of both TEOS oxide hard mask layer and poly-Si layer remaining on the surface of the substrate [Fig. 3-8 (d)], followed by a RIE step to complete the final gate structure. By carefully controlling the lateral etching of the TEOS oxide hard mask layer in dilute HF solution as shown in Fig. 3-8 (c), the dimension of final line patterns [Fig. 3-8 (e)] could be further downscaled shorter than the conventional DP method. Furthermore, the Modified I-DP method would achieve sub-60 nm line patterns without the risk of collapsed PR patterns and the CD non-uniformity issue encountered in PR ashing technique. In-line SEM images of randomly sampled line patterns at eight different dies of a six-inch wafer generated by the modified DP method are depicted in Fig. 3-9. The line widths of resultant PR patterns distribute from 42 to 93 nm, confirming the resolution capability of the modified DP method in terms of sub-50 nm line pattern generation at the expense of 51 nm variation. In addition, the variation of 51 nm, mainly ascribed to the inherent overlay accuracy of equipment plus the uniformity of TEOS oxide hard mask trimming process, is a little worse than conventional DP method (45 nm), albeit still better than PR ashing scheme (63 nm). In-line SEM images of dense line patterns generated by the modified DP method compared with conventional I-line single patterning process are illustrated in Fig. 3-10. Here the conventional single patterning and the modified double patterning are denoted as I-SP and Modified I-DP, respectively. We find Modified I-DP can achieve almost half pitch of I-SP and generate line widths of about 32 nm.

3.3 Devices Fabrication

After confirming the feasibility of the present Modified I-DP technique, we have also implemented this technique on the practical fabrication of nano-scale n-channel metal-oxide-semiconductor field-effect transistors (nMOSFETs) with or without asymmetric channel doping architecture. Figure 3-8 illustrates the major process steps in the device fabrication. Local oxidation of Si (LOCOS) scheme was first used for device isolation. P-type well was then formed by BF_2^+ implantation with energy of 70 keV and dose of 1×10^{13} cm^{-2}, followed by a drive-in anneal step at 1100 ^oC. Next, channel stop implantation was performed by implanting BF_2^+ (120 keV, 4×10^{13} cm^{-2}), followed by wet oxidation to form 450 nm-thick field oxide. Anti-punchthrough (APT) and threshold voltage (V_{th}) adjustment implantations were performed individually by implanting B^+ (70 keV, 2×10^{12} cm^{-2}) and BF_2^+ (90 keV, 1×10^{13} cm^{-2}), respectively. Afterwards, 7 nm-thick HfO_2 was deposited as the gate dielectric by an ALD system with 1 nm-thick interfacial oxide layer fabricated by the rapid thermal oxidation at 500 ^oC for 10 seconds. Gate electrode with thickness of about 100 nm-thick *in situ* phosphorus-doped poly-Si was deposited, followed by the deposition of 50 nm low pressure chemical vapor deposition (LPCVD) TEOS oxide layer as hard mask as shown in Fig. 3-8 (a). After gate definition with the modified DP method as previously described [Figs. 3-8 (b), (c), (d) and (e)], halo implantations were executed by implanting BF_2^+ (50 keV, 5×10^{12} cm^{-2}, tilt = 45°) embedded symmetrically in both source and drain (S/D) junctions for the symmetric S/D doping split (denoted as Symmetric Halo). In contrast, the asymmetric S/D doping split (denoted as Asymmetric Halo) could be implemented by embedding halo doping only in the source side prior to the second lithographic step with mask G2. Shallow S/D extensions were formed by implanting As^+ (5 keV, 1×10^{15} cm^{-2}). After forming a 100 nm-thick TEOS sidewall spacer, deep S/D junctions were formed by implanting As^+ (20 keV, 2×10^{15} cm^{-2}) and P_{31}^+ (10 keV, 5×10^{15} cm^{-2}) in sequence, and then rapid thermal anneal (RTA) was carried out in a nitrogen ambient at 1000 ^oC for 10 seconds to activate dopants in the gate and S/D junctions, as depicted in Fig. 3-8 (f). Finally, 680 nm-thick TiN/AlSiCu/TiN/Ti metallization was carried out in a PVD system to form the metal pads, and then the processing steps were completed with a forming gas anneal at 400 °C for 30 minutes. The overall implantation conditions used in the device fabrication were arranged as shown in Table 3-1. Figure 3-11 depicts the cross-sectional transmission

electron microscopic (TEM) image of a fabricated HfO_2 dielectric nMOSFET, and gate length is about 45 nm. Finally, electrical characteristics were performed using an Agilent 4156 system.

3.4 Results and Discussion

3.4-1 Performance Comparison of Lithographic Techniques

The lithographic throughput comparison among aforementioned processes with electron beam tools or I-line stepper is illustrated in Fig. 3-12, and further the correlative process time versus device throughput is shown in Fig. 3-13. For good comprehension of this section, we name all lithographic techniques as follows: "Shaped beam" represents shaped beam system of electron beam tool, "Gaussian beam" stands for another electron beam tool employed with discrete Gaussian distribution as electron beam dose, "I-line SP" represents the conventional single-patterning scheme with I-line stepper, "PR-ashing" represents the conventional I-line process with PR ashing technique, "I-line DP" represents the double-patterning technique with I-line stepper, and "Modified I-DP" represents the modified double-patterning technique with I-line stepper. From both Figs. 3-12 and 3-13, apparently we find out that although the throughput is cut in half for I-line process when conventional DP scheme and Modified I-DP method are employed, it is still approximately 100 and 50000 times higher than the throughput of the shaped beam process and the Gaussian beam process, respectively. In addition, the throughput of PR ashing scheme is similar to that of the DP method due to 0.7 nm/s PR etching rate of oxygen plasma trimming. Figure 3-14 illustrates the CD distributions of I-DP, Modified I-DP, PR ashing method, Shaped beam and Gaussian beam splits. Among these CD distributions, both electron beam tools share the best uniformity of CD at the expense of very low throughput. The CD distribution of PR ashing is obviously wider than the others, hence a highly stable asher for good reproducibility and uniformity of CD of the printed pattern is essential. Moreover, the oxide hard mask trimming of the modified I-DP process is capable of pushing the CD down to sub-60 nm without compromising its deviation as compared with conventional DP method. In summary, the uniformity of CD, throughput, LER and minimum line width of the aforementioned lithographic processes are quantitatively compared and organized in Table 3-2. From this table, the DP technique and the modified DP

technique have above-average performance, and the minimum line width of isolated line pattern can be further downscaled to 45 nm by virtue of the proposed modified DP scheme without sacrificing other performances.

3.4-2 Devices Characteristics

After the discussion about performance comparison of lithographic techniques, we have not only comprehended some lithographic features but confirmed the feasibility of the proposed Modified I-DP scheme as well. The following are the fundamental electrical characteristics of the fabricated devices we will pay attention to. Here we define the junction fabricated with single halo implantation in the Asymmetric Halo split as the source side. First of all, the transfer characteristics of nMOSFETs measured at V_D = 0.05V with gate length (L) of 10 μm and gate width (W) of 10 μm are illustrated in Fig. 3-15 (a), where both devices have the same architecture with symmetric channel doping. The difference of fabricated devices is in the applied materials of gate dielectrics, *i.e.*, one split is thermal N_2O oxide with thickness of about 2.5 nm denoted as N_2O dielectric, and another split is 7 nm-thick HfO_2 with 1 nm-thick interfacial oxide layer denoted as HfO_2 dielectric. The output characteristics of nMOSFETs with gate length of 10 μm and gate width of 10 μm measured at V_{GS}-V_{th} = 0 ~ 2 V, step= 0.4 V, and V_D = 0 ~ 2 V are illustrated in Fig. 3-15 (b). As can be seen in Figs. 3-15 (a) and (b), the HfO_2 dielectric split displays about 130 mV/dec subthreshold swing, worse than the 80 mV/dec for the N_2O dielectric split, and the HfO_2 dielectric split exhibits poor current drivability apparently. Two shortcomings can be ascribed to the extremely awful interface between gate dielectric and channel, and further it ruins not only device switching property, but other performance such as transconductance as shown in Fig. 3-16. The HfO_2 dielectric split shows a normalized transconductance of 1.34×10^{-7} μS/μm, 10 times lower than the N_2O dielectric split, and is consistent with the aforementioned difference of output characteristics as depicted in Fig. 3-15 (b). Therefore a good interface property is critical to device performance. Figure 3-17 shows transfer characteristics of two gate dielectrics splits measured at V_D = 0.05 and 2 V with gate width of 10 μm and the same symmetric channel doping architecture, both with 45 nm gate length. Even though the halo implantation was implemented in the N_2O dielectric split, severe punchthrough current resulted from poor gate controllability over channel region and serious penetration of depletion region from drain to source side,

leads to delinquency of device operation. In contrast with the N_2O dielectric split, the HfO_2 dielectric split exhibits better immunity to short-channel effect in terms of successful suppression of both surface and bulk punchthrough currents. Thanks to the implementation of HfO_2 dielectric, stronger gate controllability is achieved with the aid of thinner capacitance equivalent thickness (CET) of HfO_2 dielectric and is credited for the successful operation of such short-channel device.

Figures 3-18 (a) and (b) illustrate the transfer and output characteristics of nMOSFETs with symmetric and asymmetric S/D doping configuration, respectively, The device dimension is gate length of 45 nm and gate width of 10 μm. The Symmetric Halo split exhibits better suppression of short channel effects (SCEs) including less drain induced barrier lowering (DIBL) and lower off-state leakage current, even biased under a high drain voltage of 2 V. This is ascribed to the fact that the symmetrical halo implant increases the local substrate doping concentration and reduces the depletion width at channel edges, and therefore the lowering in surface potential barrier height with a higher drain voltage is relieved. However, the downside is the worse current drivability as compared with the Asymmetric Halo split. Thanks to inherently asymmetric S/D doping, the Asymmetric Halo split suffers from less side effect of halo doping as compared with bilateral halo doping architecture, and therefore contributes to a 20% enhancement of driving current as illustrated in Fig. 3-18 (b). In addition, the 20% increment of driving current may not be totally contributed by unilateral halo doping architecture while the variation of CET or gate capacitance could be another possible contributor discussed as follows. Prior to the discussion of gate capacitance of HfO_2 dielectric, we have to choose the suitable device dimension for capacitance measurement. Figures 3-19 (a), (b) and (c) exhibit the transfer characteristics including gate current components of three kinds of device sizes (W/L = 50 μm/50 μm, 20 μm/20 μm, and 10 μm/10 μm) measured at V_D = 0.05 V. Gate current comparable to or even larger than drain current can be distinguished from Figs. 3-19 (a) and (b), and such unbelievable gate leakage current is attributed to the crystallization of HfO_2 film after dopant activation annealing process, even if the interfacial oxide layer was artificially introduced to the device fabrication. The crystallization temperature of HfO_2 is relatively low (*i.e.*, around 300~400 ^oC) and its thermal stability is not good as well [18], and therefore 1000 ^oC RTA process certainly is sufficient to result in a crystallized HfO_2 dielectric. Besides, gate leakage current issue is relieved with downscaling the device size as illustrated in Fig. 3-19 (c). From this plot, the gate current apparently decreases

with gate length of 10 μm and gate width of 10 μm, implying that larger channel area has higher possibility of the generation of crystallized leakage paths in HfO_2 dielectrics. In addition, the artificial interfacial oxide is not robust as expected, and it leads to gate leakage current as well. In short, we selected devices with W/L = 10 μm/10 μm for the capacitance measurement owing to the gate leakage current issue mentioned above. The capacitance-voltage characteristics of the HfO_2 dielectric split randomly sampled at eleven different dies of a six-inch wafer with gate length of 5 μm and gate width of 10 μm are shown in Fig. 3-20. The measurement frequency is 100 kHz. Here we measured the two test samples with gate lengths of 5 μm and 10 μm for the same gate width of 10 μm, and subtracted the capacitance of 5 μm-sample from that of 10 μm-sample in order to eliminate the parasitic capacitance. As can be seen, the normalized capacitances distribute from 2.83 to 3.03 $\mu F/cm^2$, and the variation of 8 % would be likely ascribed to the uniformity of rapid-thermal-oxidation (RTO) process suspected for the interfacial oxide growth. For the ALD HfO_2 dielectric, we believe the fluctuation of capacitance is derived mainly from the variation of interfacial oxide thickness induced by rapid thermal process, and the delicate interfacial oxide possibly came from RTO process as well.

Figure 3-21 shows the threshold voltage of the fabricated devices as a function of the gate length with W = 10 μm. The threshold voltage is defined as the gate voltage at drain current of (W/L) · 10nA biased with a small drain voltage (V_D) of 0.05 V. As described in Fig. 3-18, halo implantation effectively improves the SCEs in MOSFETs, however, it has some drawbacks including the drain-substrate coupling, the degradation of driving current and enhanced reverse-short-channel-effect (RSCE). The Symmetric Halo split depicts severer RSCE than the Asymmetric Halo split because bilateral halo increases doping distribution near the S/D edges of the channel, and therefore results in a locally higher threshold voltage. In addition, as the gate length downscales to below 100 nm, the threshold voltage of Symmetric Halo device is slight larger than Asymmetric Halo device. Owing to the sufficiently short channel comparable to the width of channel depletion region, the portion of the sharing of the charges in the channel depletion region with the S/D junctions becomes much significant and thus results in threshold voltage rolling. Hence the inherently unilateral halo doping of Asymmetric Halo device exhibits more threshold voltage rolling as compared with the Symmetric Halo counterpart. The current drivability (I_{on}) as a function of the gate length with W = 10 μm biased at gate over-drive voltage (V_{GS}-V_{th}) of 2 V and drain voltage

(V_D) of 2 V is shown in Fig. 3-22. The Asymmetric Halo device exhibits higher driving current than Symmetric Halo device, indicating the benefit of adopting asymmetric structure. Even with the larger subthreshold leakage current, the Asymmetric device can be implemented with some application such as radio-frequency (RF) IC, with its relatively higher driving current.

3.5 Summary

In this chapter, we have extended the lithography limit of DP technique developed previously in chapter 2. We have also confirmed the feasibility of both forming sub-60 nm line patterns and fabricating 45nm-nMOSFETs with symmetric or asymmetric S/D doping using the proposed modified I-line double patterning technique through the in-line SEM and TEM characterizations, which is far beyond the resolution capability of conventional single patterning I-line lithographic process. In addition, several lithographic processes developed by two lithographic systems including electron beam tool and I-line stepper are quantitatively compared from the perspectives of the uniformity of CD, throughput, LER and minimum line width. Our results indicate that the proposed modified DP technique in this work not only shows remarkable performance on generating fine line patterns, but also is promising for the research works carried out at the university-based laboratories in terms of more flexible applications, decent throughput (as compared with electron beam tool) and much lower cost (as compared with state-of-the-art immersion DUV lithography). Besides, the fabricated devices with the proposed method are conducive to the optimization solution to the S/D engineering as far as the device performance is concerned. The asymmetric S/D doping device shows higher current drivability, which could be suitable for RF IC application.

References

[1] *ITRS Roadmap*. [Online]. Available: http://www.itrs.net/

[2] P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S-H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. St. Amour, K. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luo and S. Natarajan, "High performance 32nm logic technology featuring 2nd generation high-*k* + metal gate transistors," in *IEDM Tech. Dig.*, 2009, p. 659.

[3] K. Ronse, P. Jansen, R. Gronheid, E. Hendrickx, M. Maenhoudt, M. Goethals, and G. Vandenberghe, "Lithography options for the 32nm half pitch node and beyond," *IEEE Custom Integrated Circuits Conference (CICC)*, vol. 15, no. 1, pp. 371-378, 2008.

[4] K. H. Chen, C. Y. Chien, and P. W. Li, and O. Adams, "Precise Ge quantum dot placement for quantum tunneling devices," *IEEE Trans. Nanotechnology*, vol. 21, no. 5, p. 055302, 2010.

[5] R. F. Pease, and S. Y. Chou, "Lithography and other patterning techniques for future electronics," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 248-270, Feb. 2008.

[6] J. Chung, M. Jeng, J. E. Moon, A. T. Wu, T. Y. Chan, P. K. Ko, and C. Hu, "Deep-submicrometer MOS device fabrication using a photoresist-ashing technique," *IEEE Electron Device Letters*, vol. 9, no. 4, pp. 186-188, 1988.

[7] K. Asano, Y.-K. Choi, T.-J. King, and C. Hu, "Patterning sub-30-nm MOSFET gate with i-line lithography," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 1004-1006, 2001.

[8] M. Shibata, A. Horiba, Y. Nagaoka, H. Kawata, M. Yasuda, and Y. Hirai, "Process-simulation system for UV-nanoimprint lithography," *J. Vac. Sci. Technol. B*, vol. 28, pp. C6M108-C6M113, 2010.

[9] H. Schift, "Nanoimprint lithography: An old story in modern times? A review," *J. Vac. Sci. Technol. B*, vol. 26, pp. 458-480, 2008.

[10] C. M. Sotomayor Torres, "Nanostructure science and technology," Kluwer Academic, New York, 2003.

[11] H. Schulz, M. Wissen, N. Bogdanski, H.-C. Scheer, K. Mattes, and Ch. Friedrich, "Impact of molecular weight of polymers and shear rate effects for nanoimprint

lithography," *Microelectronic Engineering*, vol. 83, pp. 259-280, 2006.

[12] V. Robbins, D. Taylor, C. Wanqing, A. Fischer-Colbrie, P. Chungdee, S. Ahmed, and D Stumbo, "VLS growth of Si nanowires with *in-situ* doping for MOS transistors," in *Proc. of IEEE Nanotechnology Conference*, 2009, pp. 326-329.

[13] H. F. Yan, Y. J. Xing, b, Q. L. Hang, D. P. Yu, Y. P. Wang, J. Xu, Z. H. Xi and S. Q. Feng, "Growth of amorphous silicon nanowires via a solid–liquid–solid mechanism," *Chemical Physics Letters*, vol. 323, pp. 224-228, 2000.

[14] N. Wang, Y. F. Zhang, Y. H. Tang, C. S. Lee, and S. T. Lee, "SiO2-enhanced synthesis of si nanowires by laser ablation," *Appl. Phys. Lett.*, vol. 73, pp. 3902-3904, 1998.

[15] H. C. Lin, T. I. Tsai, T. S. Chao, M. F. Jian, and T. Y. Huang, "Fabrication of sub-100-nm metal-oxide-semiconductor field-effect transistors with asymmetrical source/drain using I-line double patterning technique," *J. Vac. Sci. Technol. B*, vol. 29, pp. 021007-1-021007-7, 2011.

[16] C. Bencher, Y. Chen, H. Dai, W. Montgomery and L. Huli, "22nm half-pitch patterning by CVD spacer self alignment double patterning (SADP)," *Proc. SPIE*, vol. 6924, pp. 69244E-1- 69244E-7, 2008.

[17] P. Xu, Y. Chen, Y. Chen, L. Miao, S. Sun, S.-W. Kim, A. Berger, D. Mao, C. Bencher, R. Hung and C. Ngai, "Sidewall spacer quadruple patterning for 15nm half-pitch," *Proc. SPIE*, vol. 7973, pp. 79731Q-1- 79731Q-12, 2011.

[18] W. Zhu and T. P. Ma, "HfO_2 and HfAlO for CMOS：thermal stability and current transport," in *IEDM Tech. Dig.*, 2001, p. 463.

Table 3-1 Overall implantation conditions used in the device fabrication.

Conditions	Ion	Energy / Dose / Tilt angle / Twist angle
P-well	BF_2^+	70 keV / 1×10^{13} cm^{-2} / 7° / 22°
Channel Stop	BF_2^+	120 keV / 4×10^{13} cm^{-2} / 7° / 22°
V_{th}	BF_2^+	40 keV / 1×10^{13} cm^{-2} / 7° / 22°
APT	B^+	35 keV / 5×10^{12} cm^{-2} / 7° / 22°
Halo	BF_2^+	50 keV / 2.5×10^{12} cm^{-2} / 45° / 27°
S/D extension	As^+	5 keV / 1×10^{15} cm^{-2} / 0° / 0°
Deep S/D	As^+	20 keV / 2×10^{15} cm^{-2} / 0° / 0°
	P_{31}^+	10 keV / 5×10^{15} cm^{-2} / 0° / 0°

Table 3-2 Comparisons of electron beam tools and I-line processes.

	Throughput (#/min)	CD Uniformity (3σ)	LER	Min. Line Width
I-DP	27306	45.4nm	<20nm	83nm
PR ashing	28659	73.6nm	<40nnm	84nm
Modified I-DP	24909	52.8nm	<20nm	45nm
Shaped beam	310	32.2nm	<5nm	78nm
Gaussian beam	0.55	37.5nm	<5nm	69nm

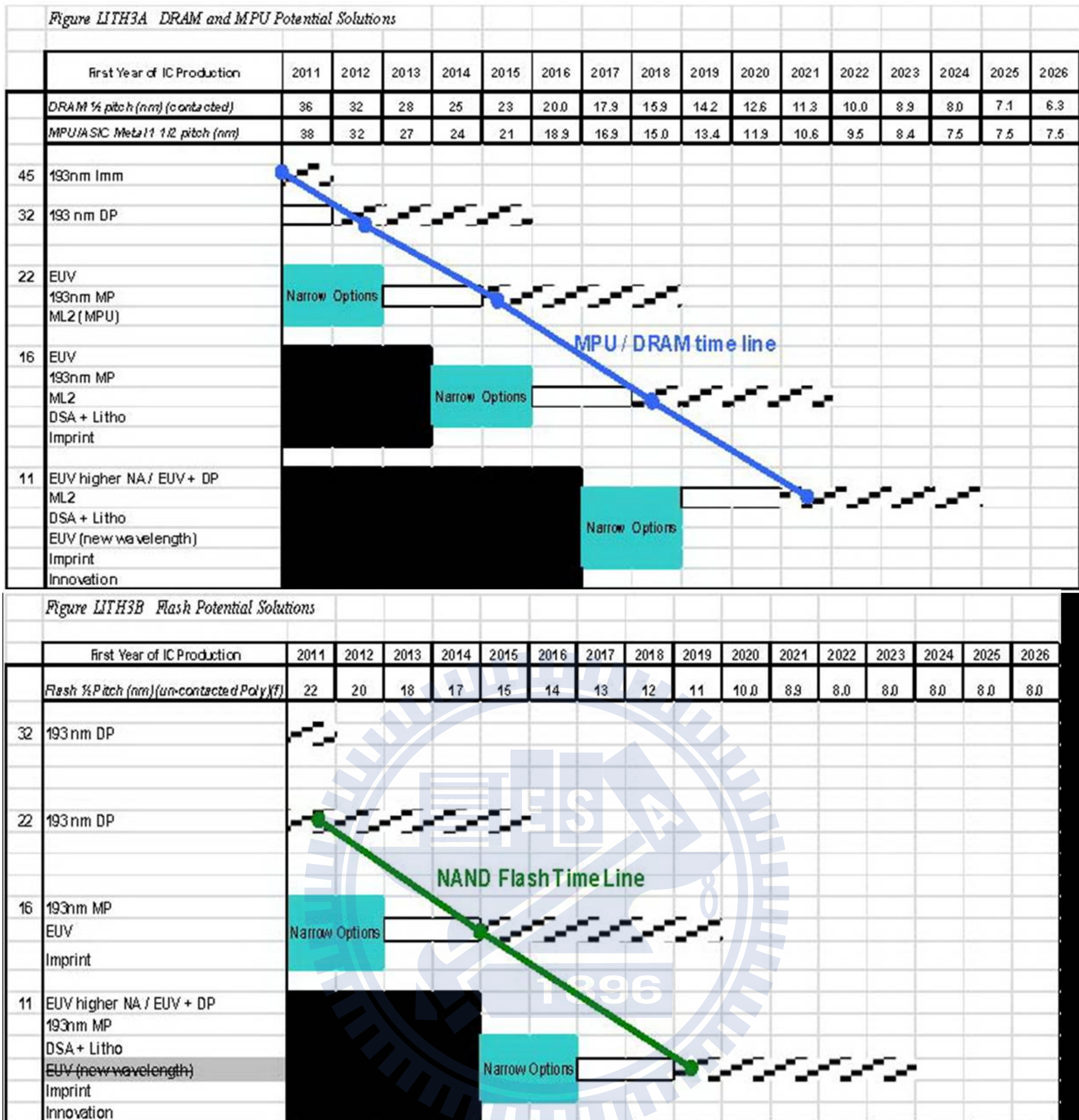


Fig. 3-1 Lithography roadmap for DRAM, MPU and Flash [1].

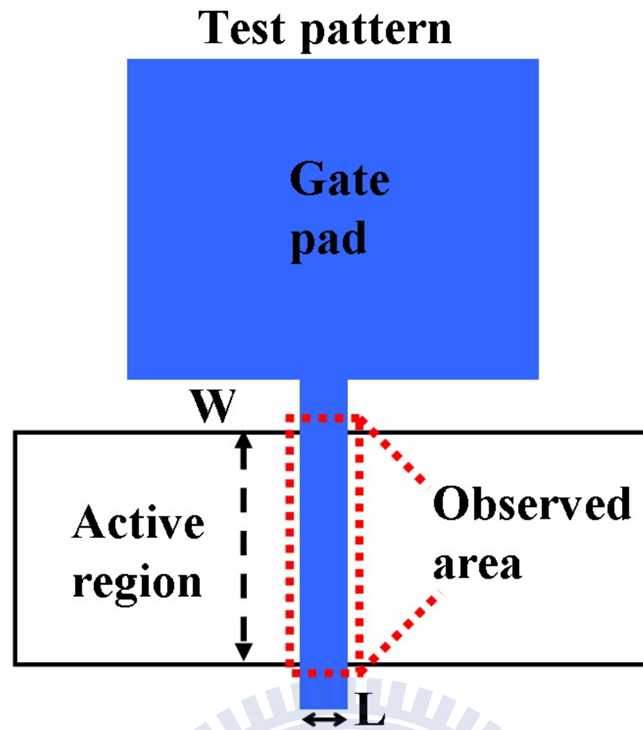


Fig. 3-2 (a) Mask layouts for defining the gate pattern and observed area on the active region. A single mask is used in the single-patterning process.

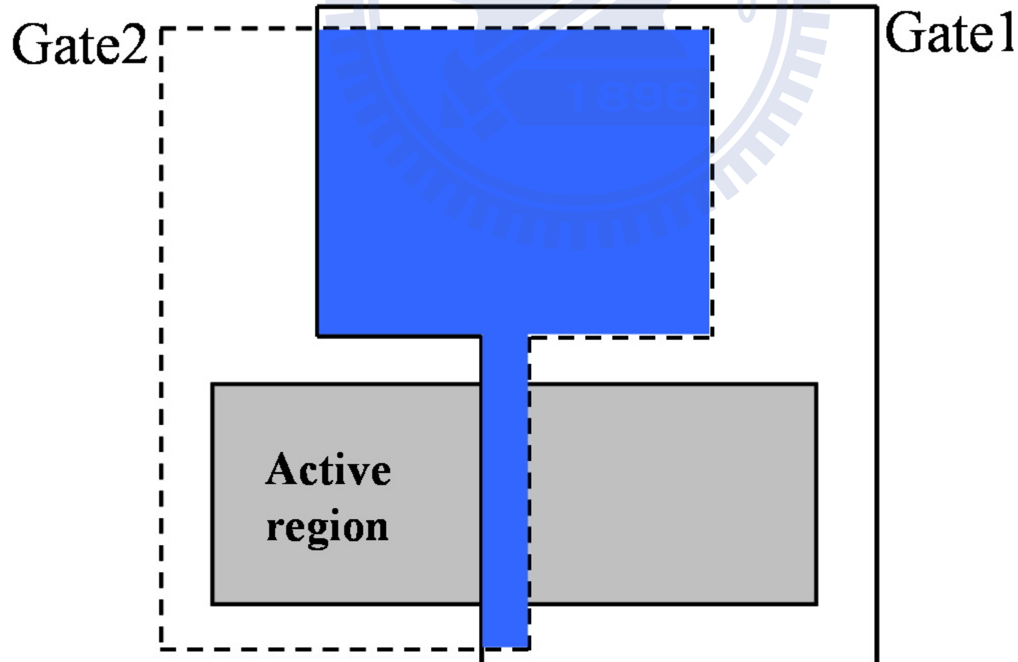


Fig. 3-2 (b) Mask layouts for defining the gate pattern and observed area on the active region. Gates 1 and 2 represent the two masks used in the DP process.

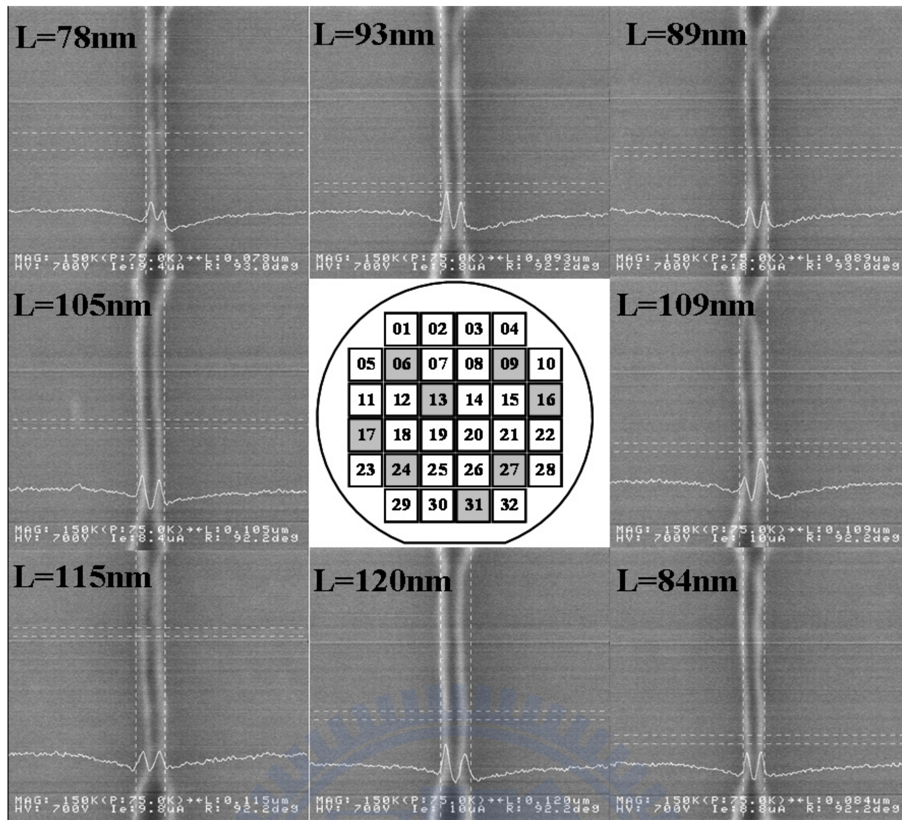


Fig. 3-3 In-line SEM images patterned by the shaped-beam tool.

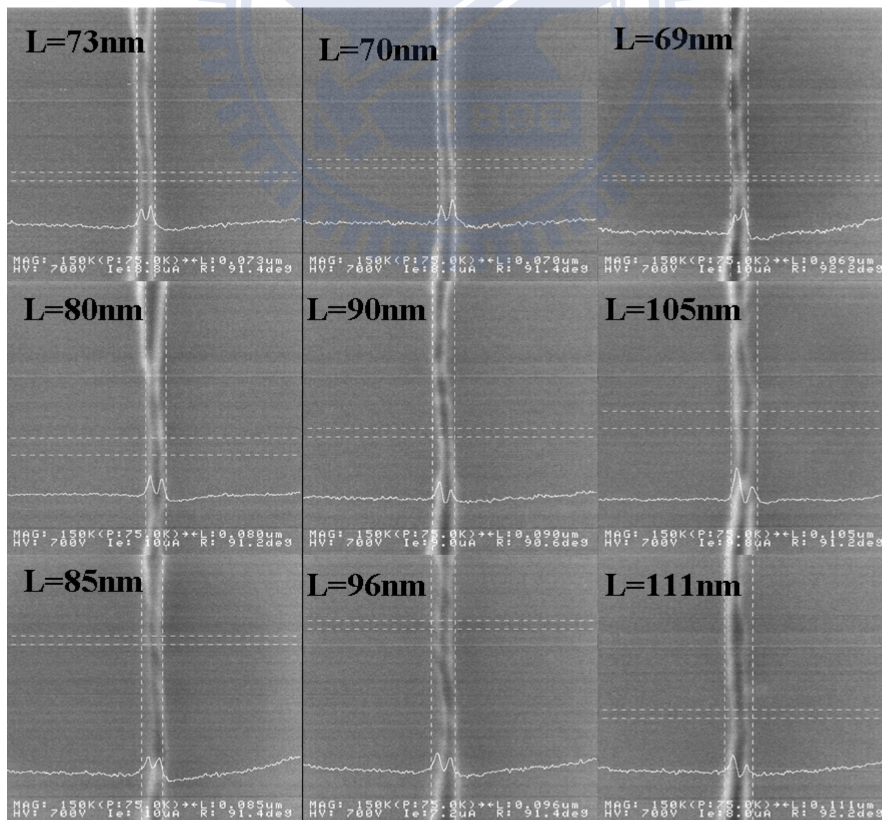


Fig. 3-4 In-line SEM images patterned by the Gaussian-beam tool.

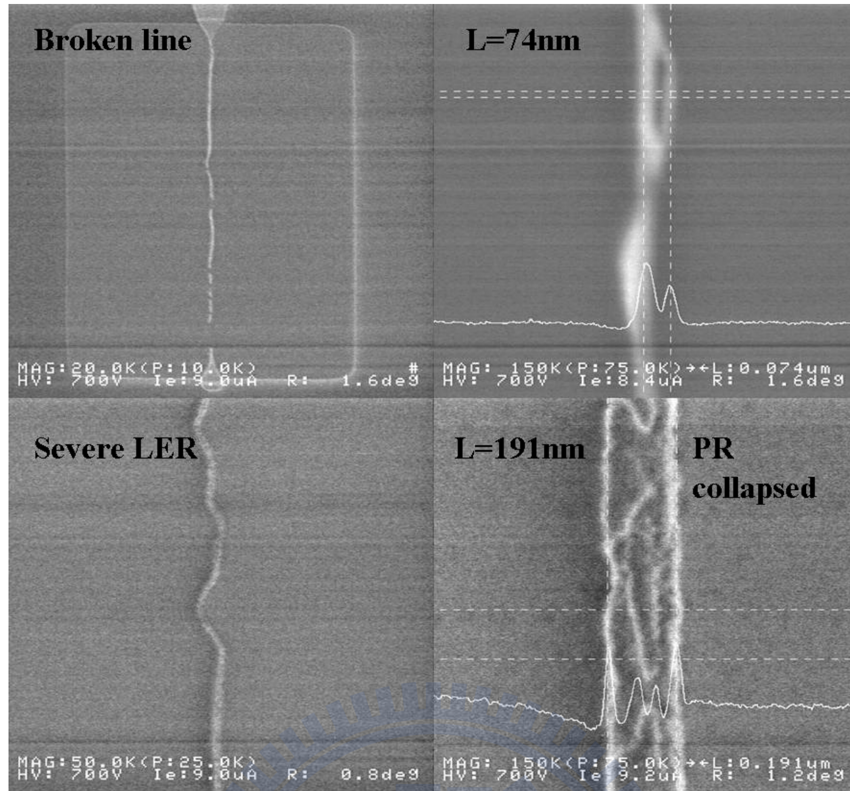


Fig. 3-5 In-line SEM images patterned by the PR ashing method after over-ashing process.

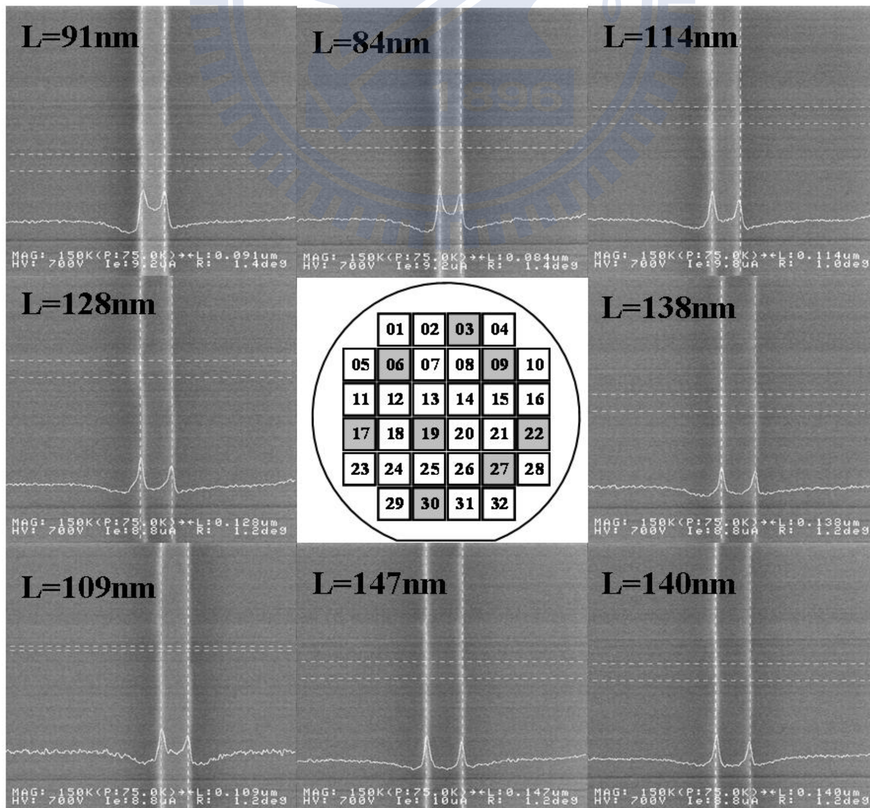


Fig. 3-6 In-line SEM images patterned by the PR ashing method.

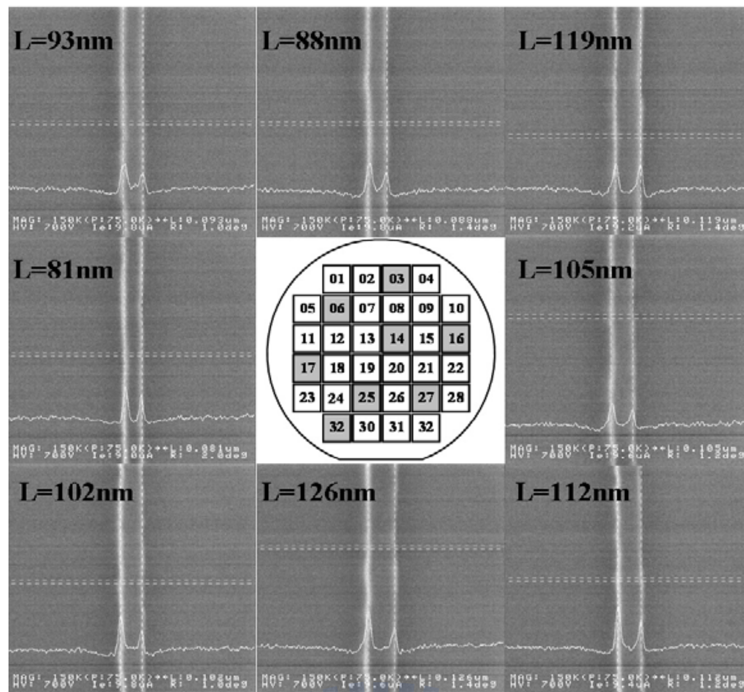


Fig. 3-7 In-line SEM images patterned by the DP method.

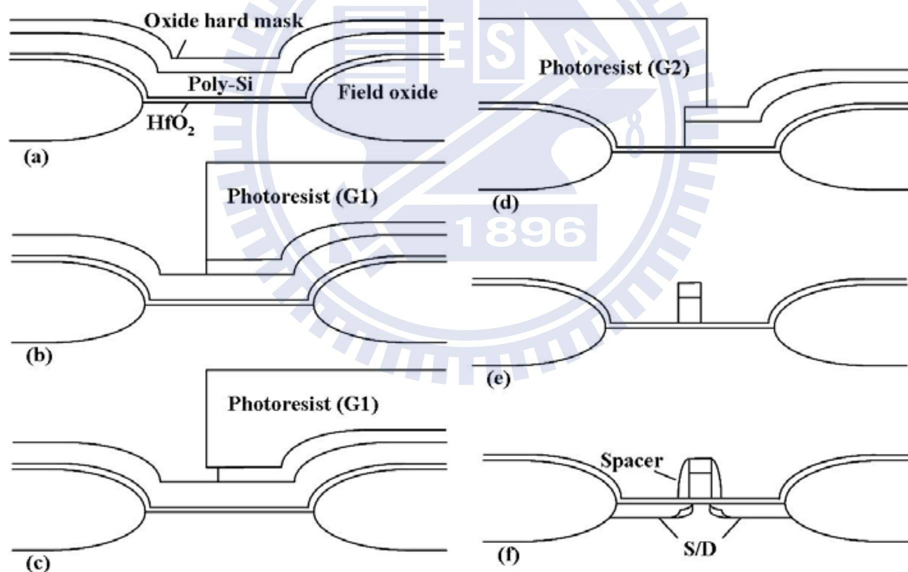
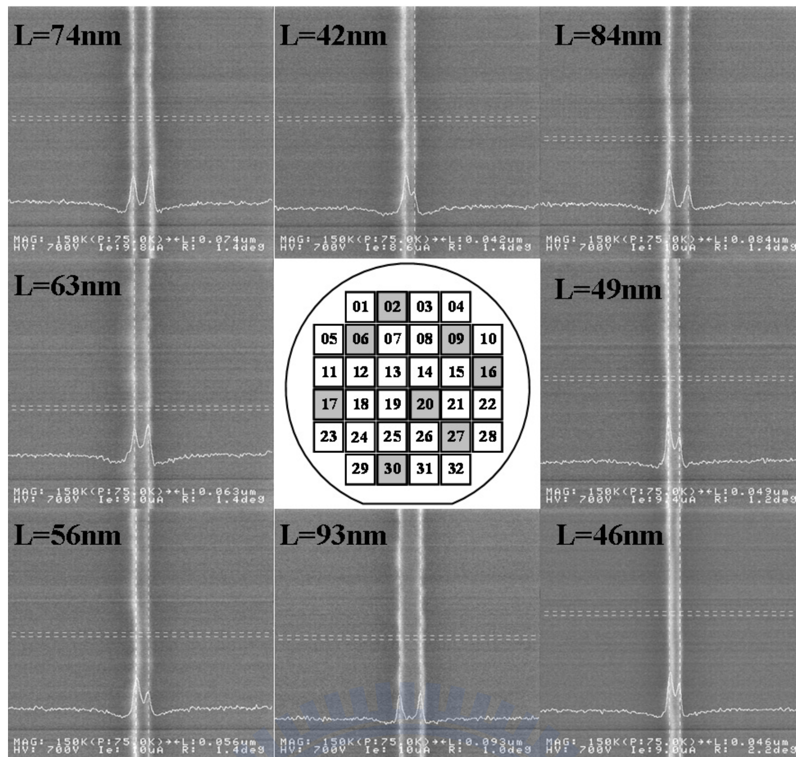


Fig. 3-8 Major process steps for fabricating n-MOSFETs with the Modified I-DP method. (a) Deposition of TEOS oxide hard mask and *in situ* phosphorus-doped poly-Si layers onto the HfO_2 gate dielectric (active region) with LOCOS isolation. (b) Generation of first PR pattern (G1), followed by the anisotropic etching of hard mask layer. (c) Lateral etching of the hard mask layer, followed by the PR removal and the first anisotropic etching of poly-Si layer. (d) Generation of second PR pattern (G2). (e) Completion of the poly-Si gate pattern after second hard mask and poly-Si etching. (f) Formation of S/D junctions.



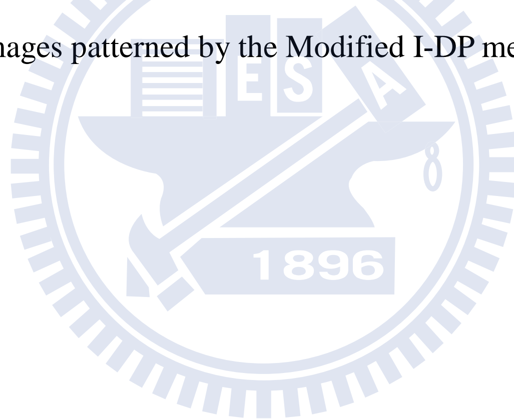


Fig. 3-9 In-line SEM images patterned by the Modified I-DP method.

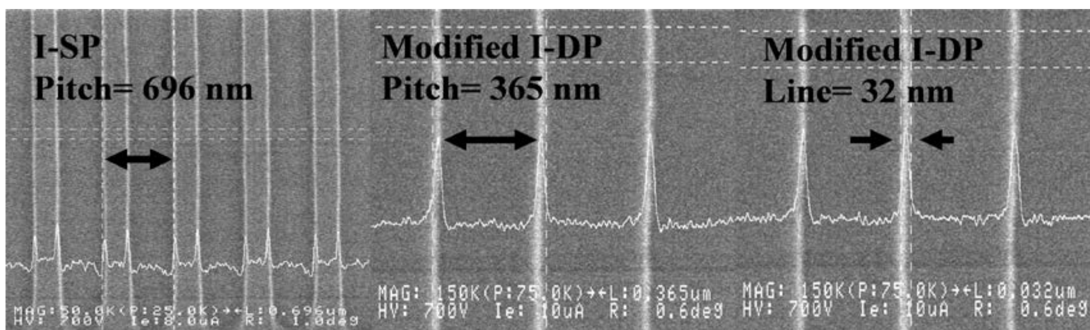


Fig. 3-10 In-line SEM images of dense line patterns generated by the Modified I-DP method compared with single patterning method (I-SP).

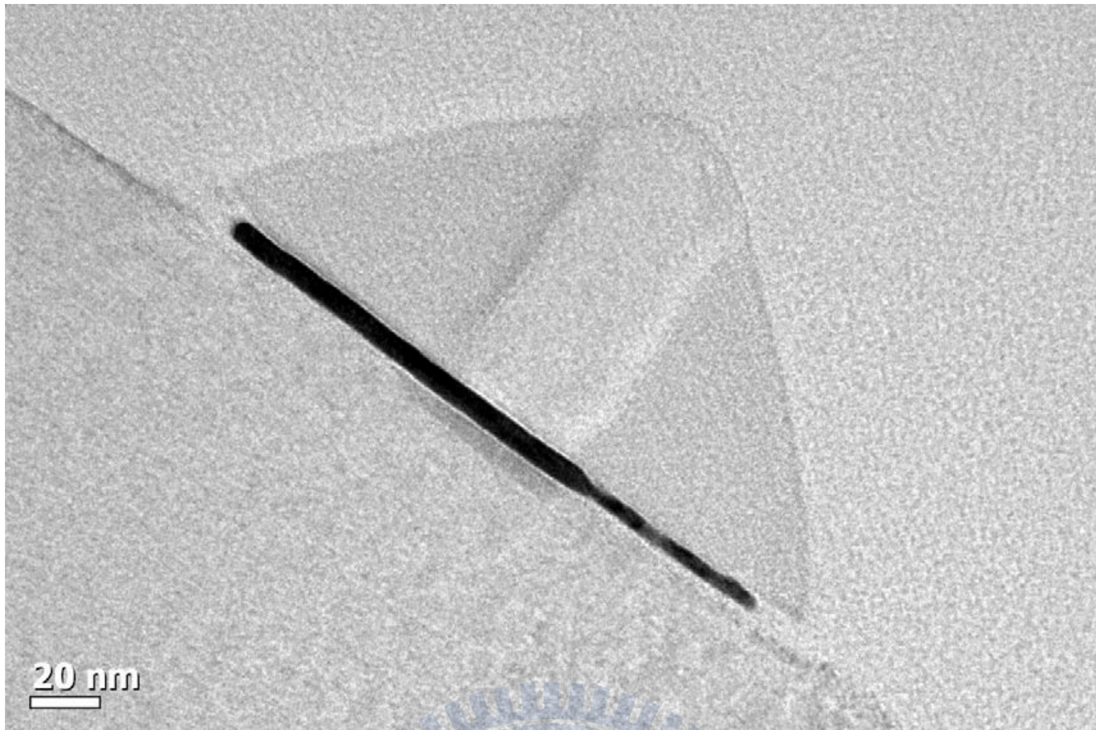


Fig. 3-11 Cross-sectional TEM image of a fabricated nMOSFET.

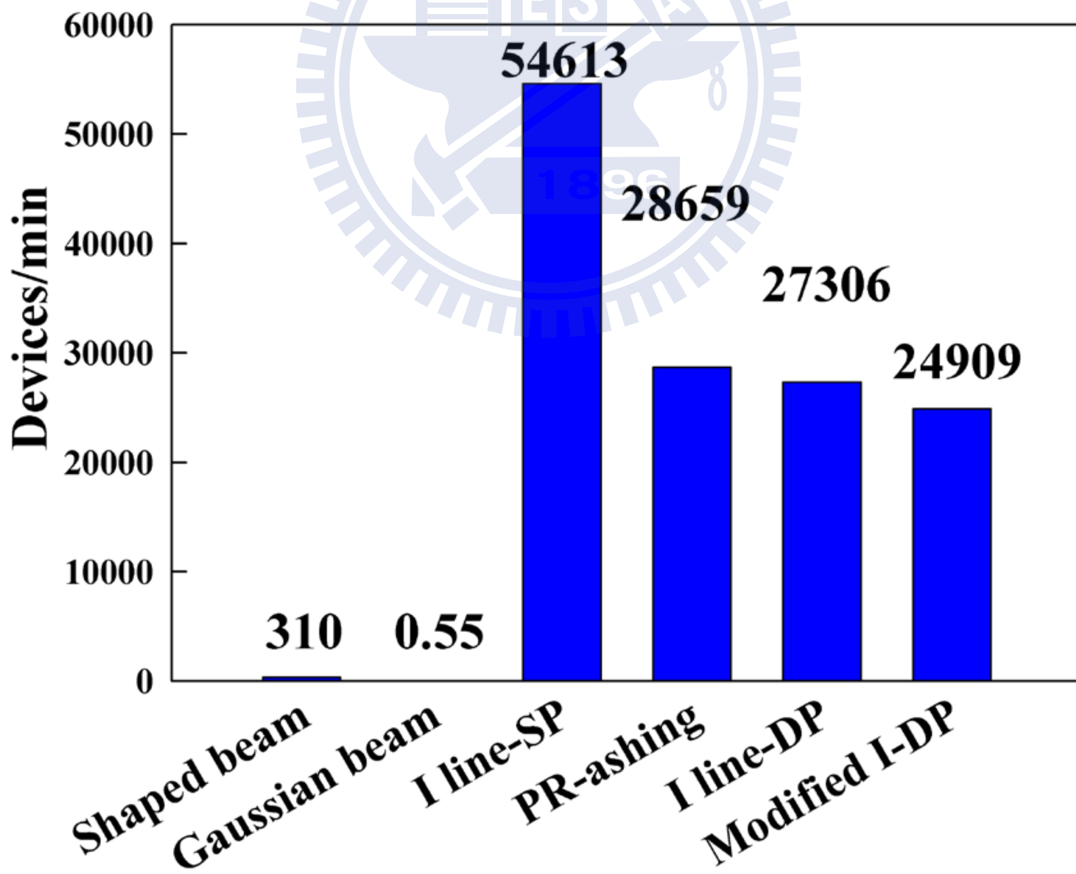


Fig. 3-12 Throughput of two lithographic systems.

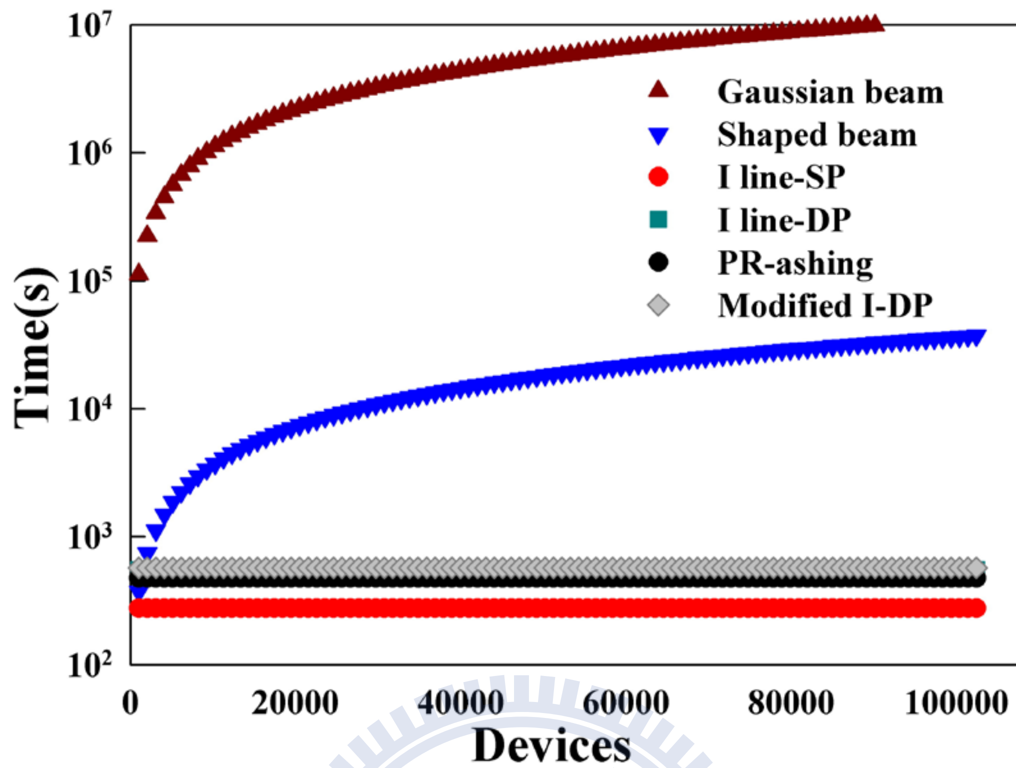


Fig. 3-13 Process time versus device throughput of two lithographic systems.

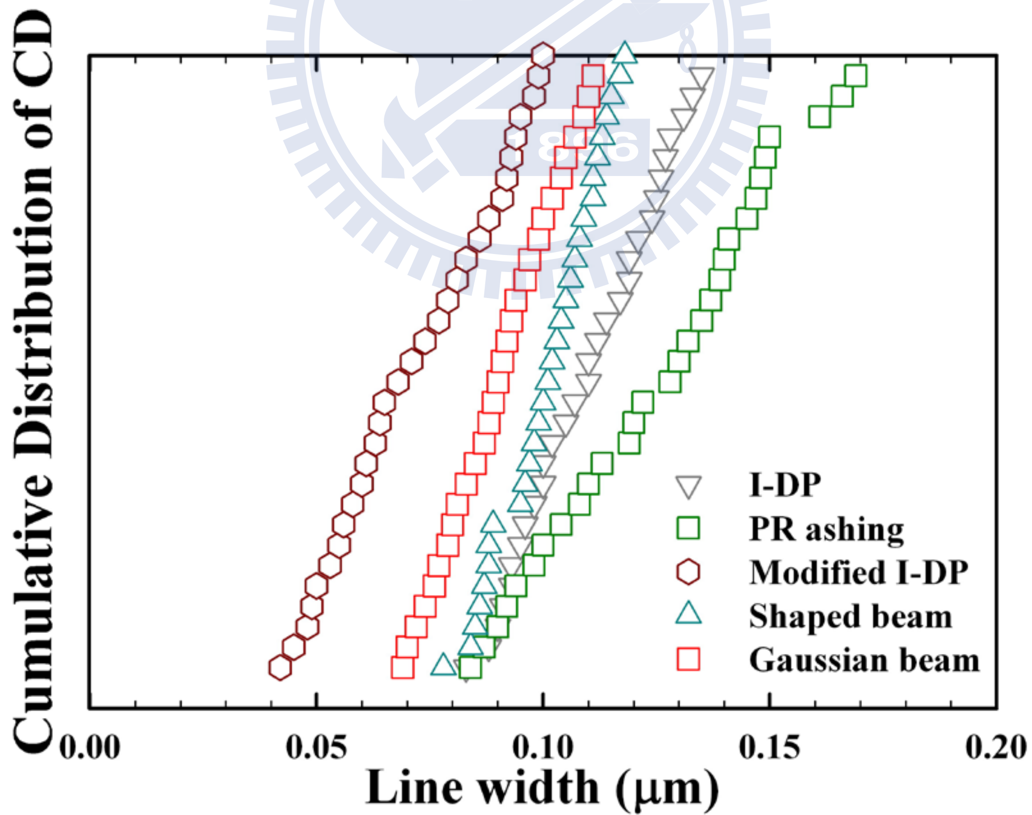


Fig. 3-14 CD distribution of two lithographic systems.

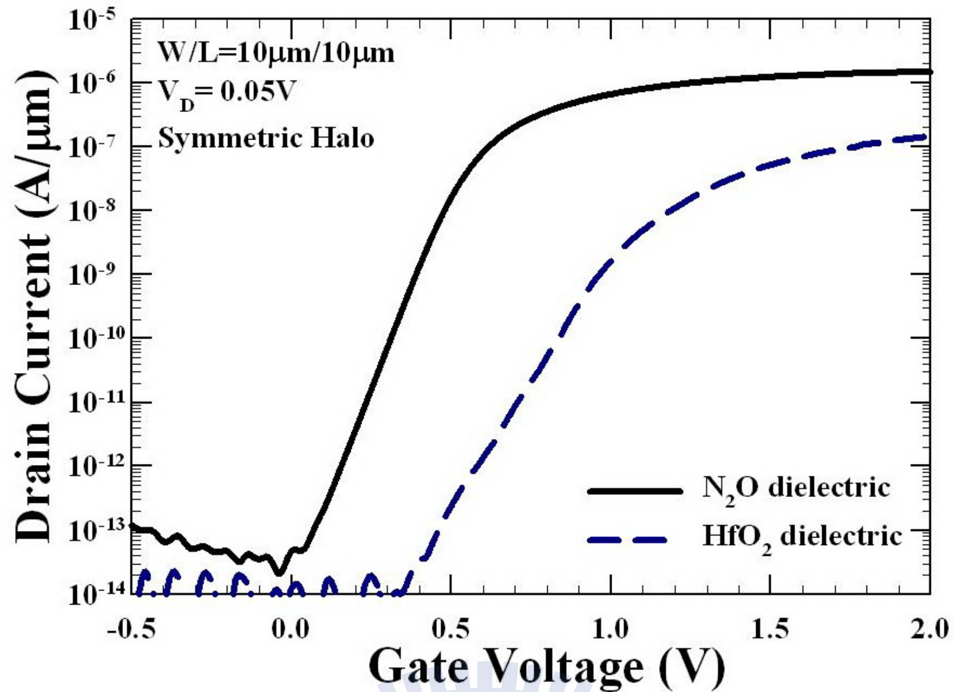


Fig. 3-15 (a) Transfer characteristics of two gate dielectric splits measured at V_D = 0.05V with gate length of 10 μm and gate width of 10 μm.

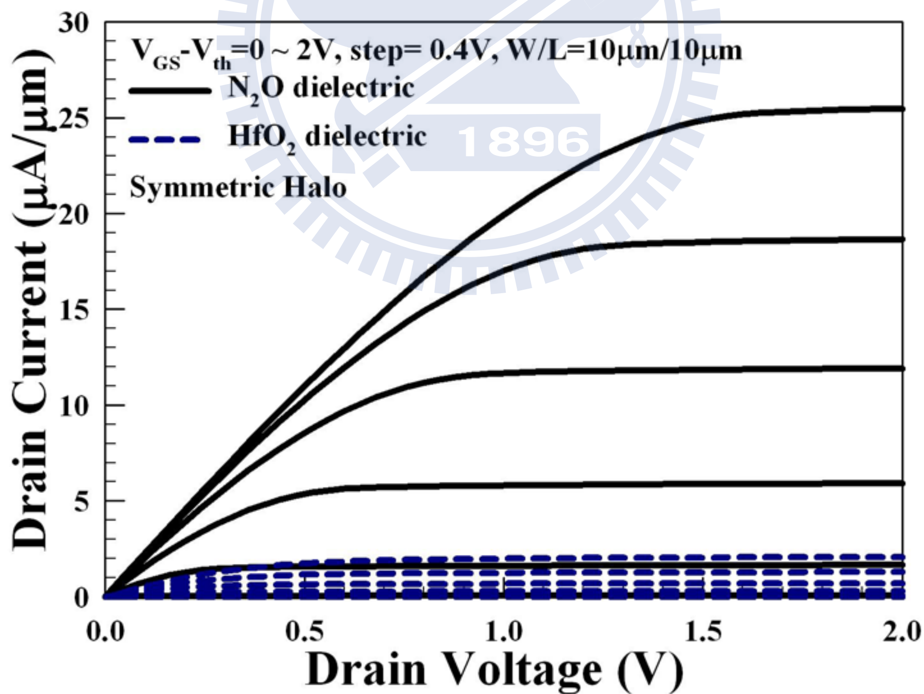


Fig. 3-15 (b) Output characteristics of two gate dielectric splits with gate length of 10 μm and gate width of 10 μm measured at V_{GS}-V_{th} = 0 ~ 2 V, step= 0.4 V, and V_D = 0 ~ 2 V.

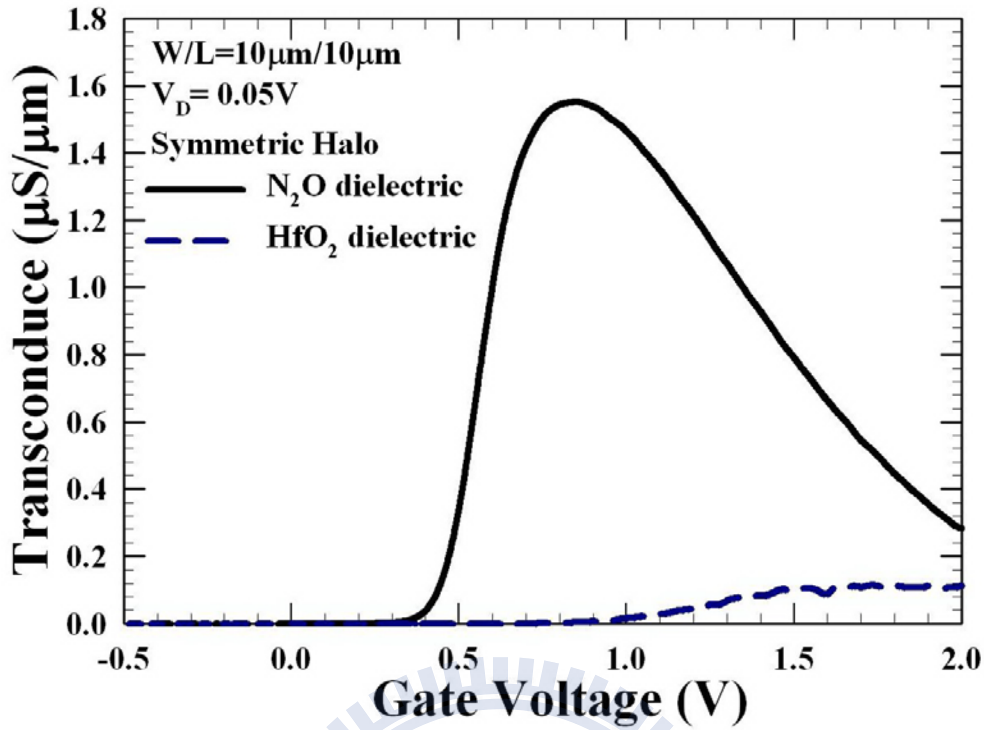


Fig. 3-16 Transconductance curves of two gate dielectric splits measured at $V_D = 0.05V$ with gate length of 10 µm and gate width of 10 µm.

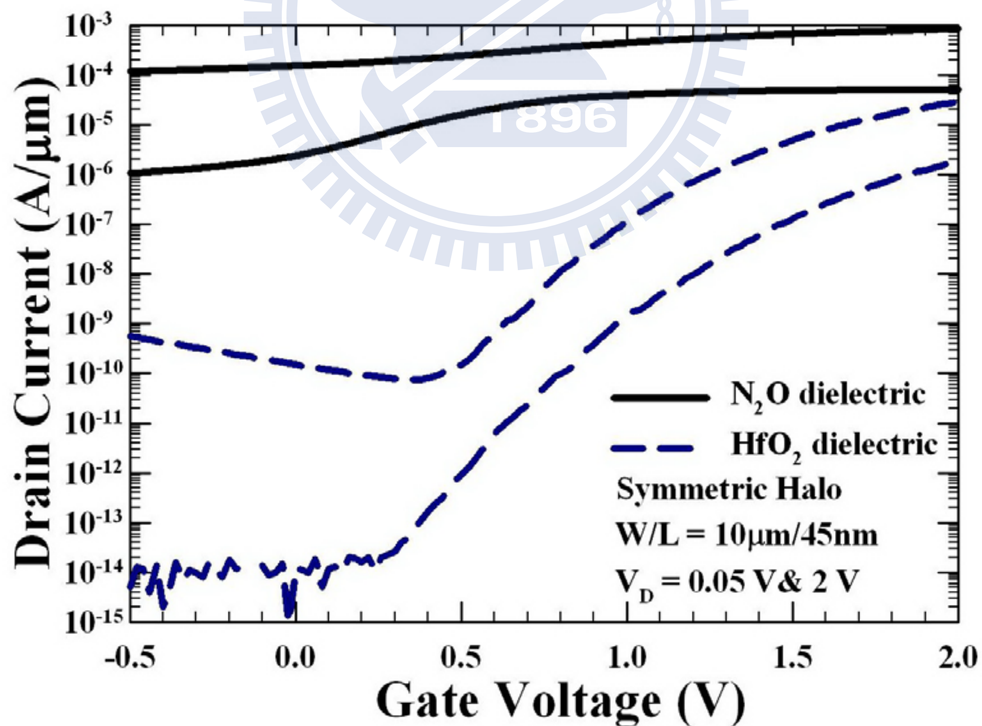


Fig. 3-17 Transfer characteristics of two gate dielectric splits measured at $V_D = 0.05$ and 2 V with gate length of 45 nm and gate width of 10 µm.

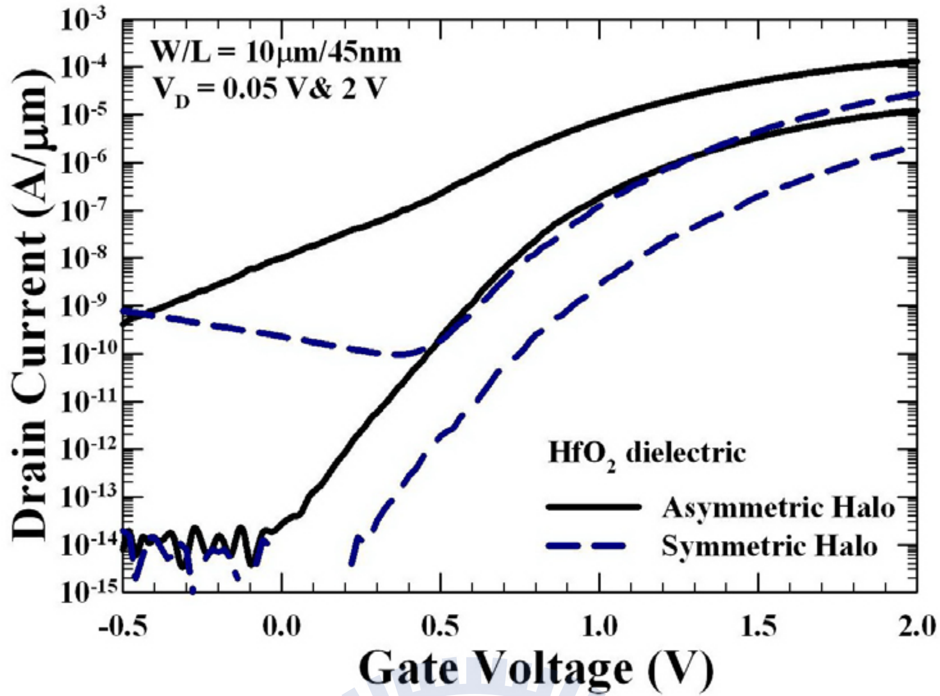


Fig. 3-18 (a) Transfer characteristics of Symmetric and Asymmetric Halo splits measured at V_D = 0.05 and 2 V with gate length of 45 nm and gate width of 10 μm.

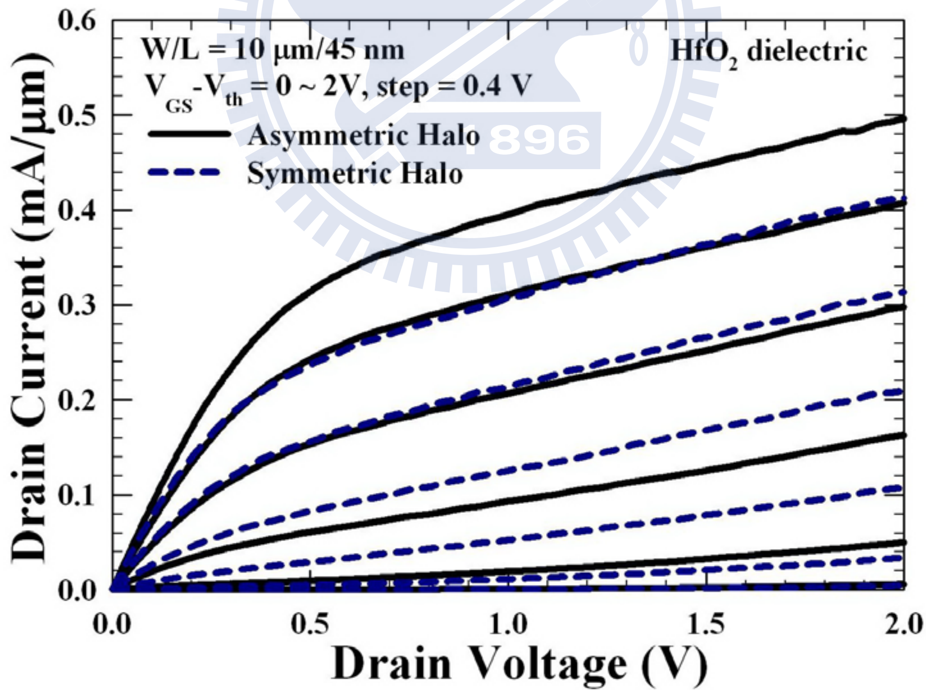


Fig. 3-18 (b) Output characteristics of Symmetric and Asymmetric Halo splits with gate length of 45 nm and gate width of 10 μm measured at V_{GS}-V_{th} = 0 ~ 2 V, step= 0.4 V, and V_D = 0 ~ 2 V.

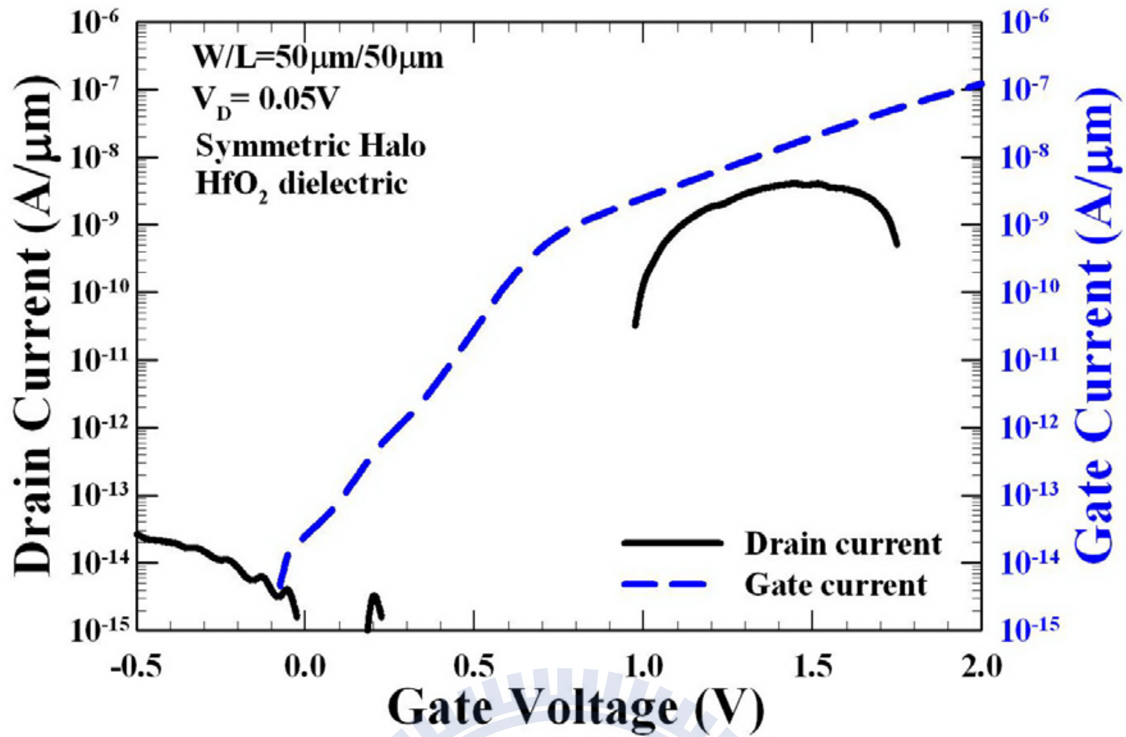


Fig. 3-19 (a) Transfer characteristics of Symmetric Halo split with HfO_2 dielectric measured at V_D = 0.05 V with W/L = 50 μm/50 μm.

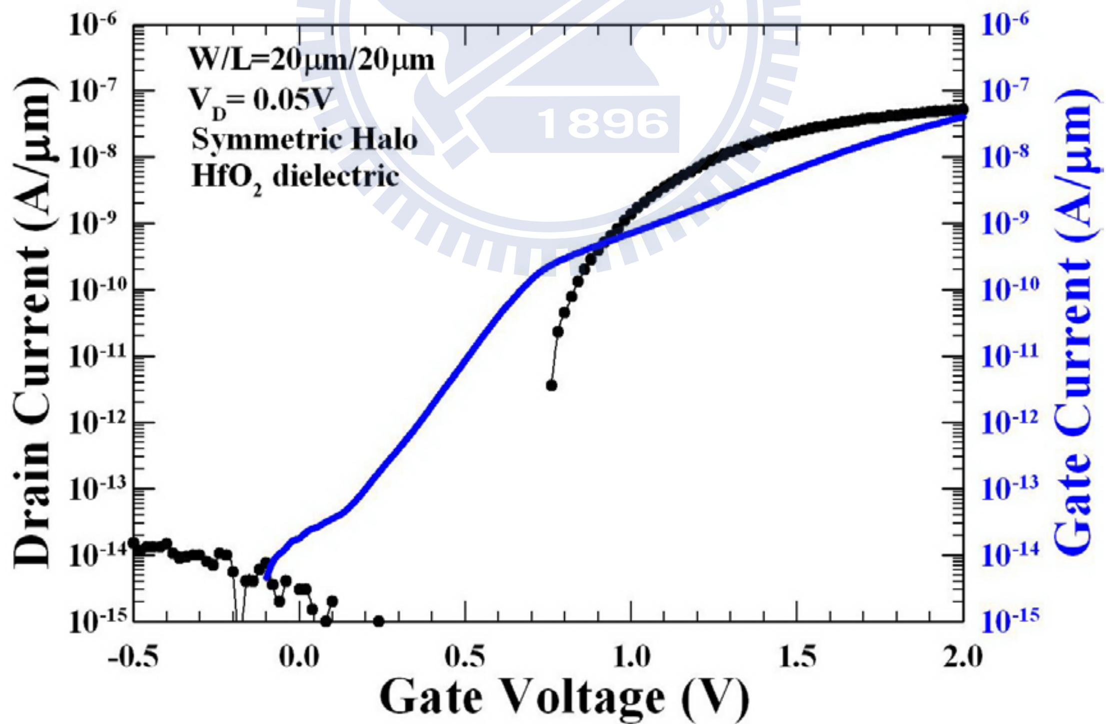


Fig. 3-19 (b) Transfer characteristics of Symmetric Halo split with HfO_2 dielectric measured at V_D = 0.05 V with W/L = 20 μm/20 μm.

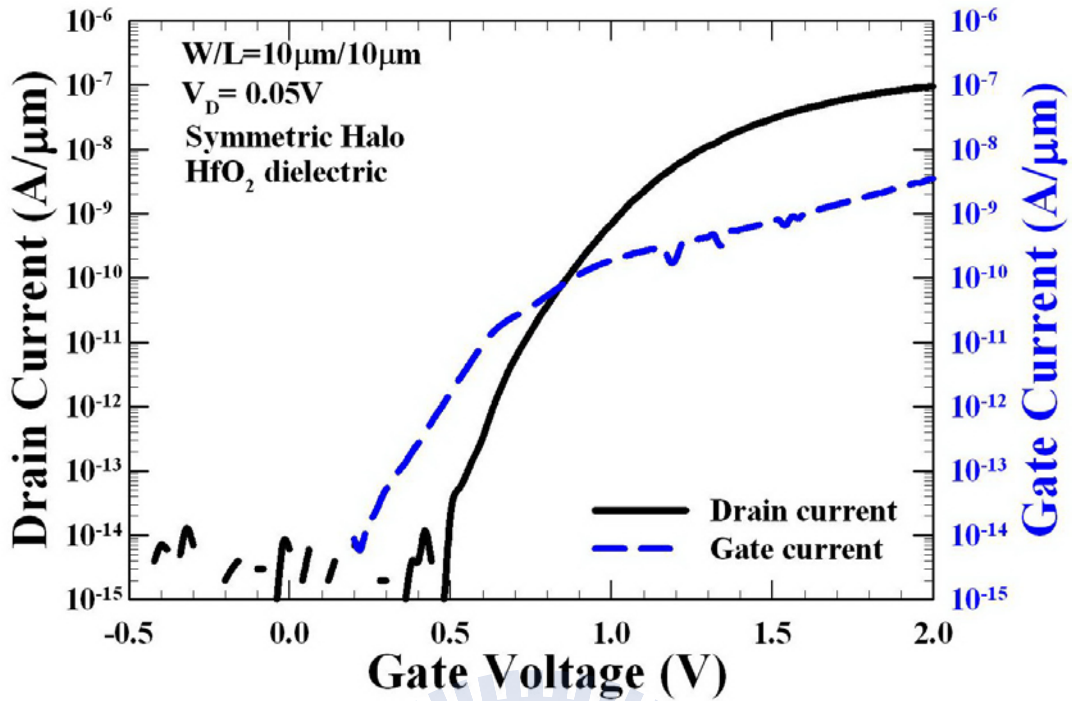


Fig. 3-19 (c) Transfer characteristics of Symmetric Halo split with HfO_2 dielectric measured at V_D = 0.05 V with W/L = 10 μm/10 μm.

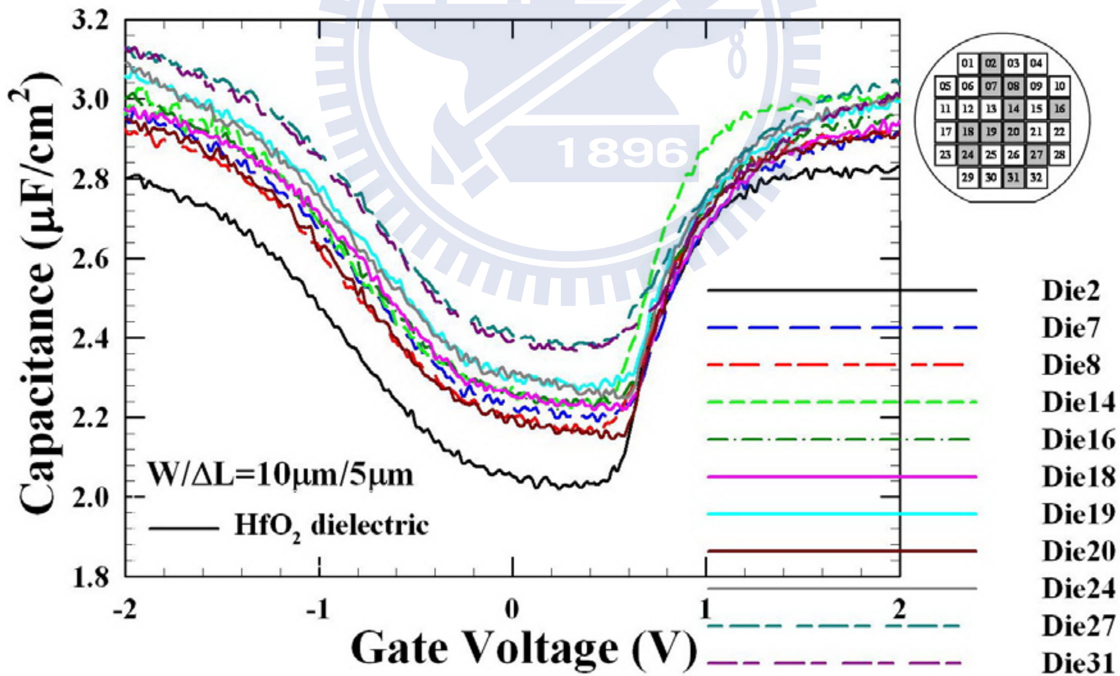


Fig. 3-20 Capacitance-Voltage (C-V) characteristics of HfO_2 dielectric split randomly sampled at eleven different dies of a six-inch wafer with gate length of 5 μm and gate width of 10 μm. The measurement frequency is 100 kHz.

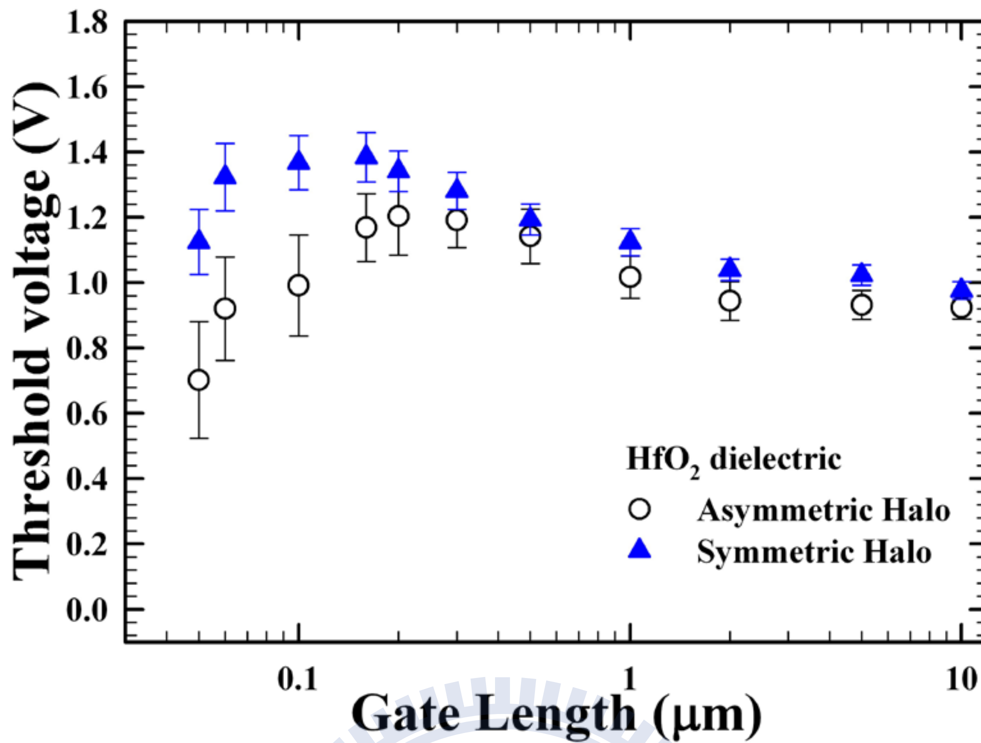


Fig. 3-21 Threshold voltage as a function of gate length for Symmetric and Asymmetric Halo splits.

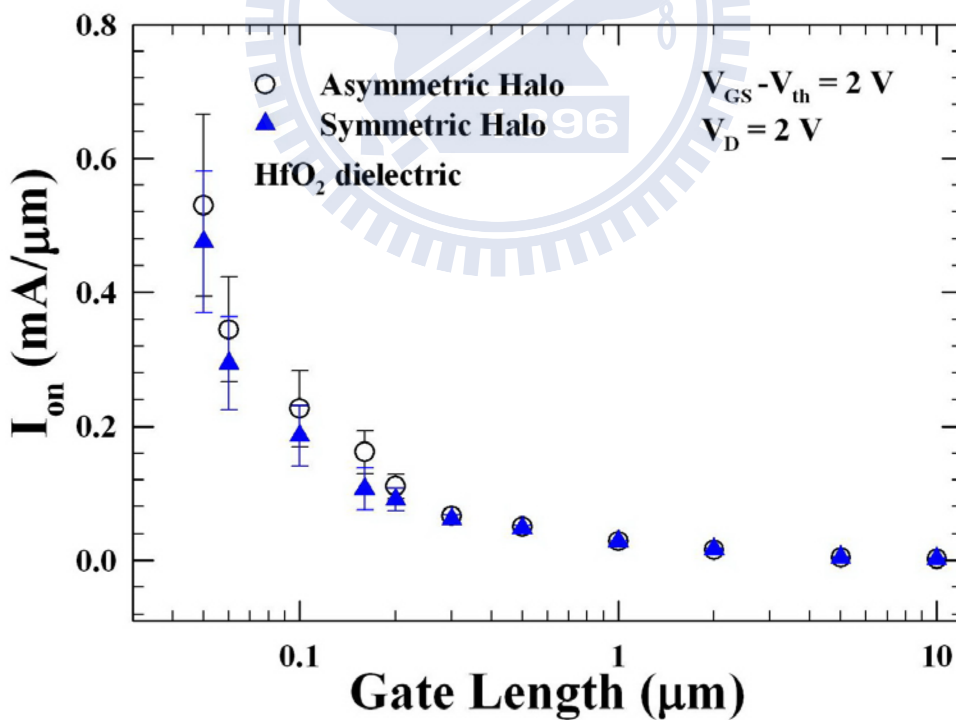


Fig. 3-22 Current drivability (I_{on}) as a function of gate length for Symmetric and Asymmetric Halo splits measured at V_{GS}-V_{th} = 2 V and V_D = 2 V.

Chapter 4

Fabrication of Sub-100 nm Devices with Asymmetrical Source/Drain Using I-line Double Patterning Technique

4.1 Introduction

As the dimension of transistor is scaled down, the suppression of short channel effects (SCEs) becomes one of the most important issues, especially when the channel length is comparable to the depletion width of the source/drain junctions. For this case, the carrier transport would be greatly influenced by the drain bias, and furthermore bring about surface punch-through, threshold voltage (V_{th}) roll-off, bulk punch-through, and consequently the gate would lose its controllability over channel carrier conduction. On the other hand, the most fundamental limitation that controls the turn-on efficiency of a transistor stems from its inherent properties related to thermodynamic carrier distribution. The basic drift-diffusion theory gives the physical limitation on the subthreshold swing (SS) at 60 mV/dec at room temperature [1]. For conventional metal-oxide-semiconductor field-effect transistors (MOSFETs), the subthreshold swing and maximum depletion width of the channel (W_{dm}), are individually expressed as follows:

$$SS \approx \ln 10 \frac{kT}{q}(1+\frac{C_d + C_{it}}{C_{OX}}) \text{ ....(4-1),}$$

$$W_{dm} = \sqrt{\frac{2\varepsilon_s(2\varphi_b - V_{bs})}{qN_a}} \text{ ....(4-2),}$$

$$C_d = \varepsilon_s / W_{dep} \text{ ....(4-3),}$$

where T is absolute temperature, k is the Boltzmann's constant, q is the electronic charge, C_{ox} is the oxide capacitance, C_{it} is the capacitance of the interface states, C_d is the depletion capacitance, W_{dep} is the depletion width, φ_b is the Fermi potential with respect to the midgap, V_{bs} is the substrate bias, ε_s is the silicon permittivity, and N_a is the substrate doping concentration. From these formulas, we clearly figure out an increase in N_a could reduce W_{dm} and simultaneously increase C_d, therefore it is a trade-off

between SCE immunity and *SS* performance. For settling the foregoing dilemma, it demands to build up a new device scheme with different transport and operation mechanisms.

The concept of tunneling field-effect transistor (TFET) was proposed by Sanjay Banerjee *et al*. in 1987 [2] and called "surface tunneling transistor" as well in those days [2-4]. The TFET is a gated p-i-n diode as depicted in Fig. 4-1, using band-to-band tunneling (BTBT) as carrier transport mechanism. As a TFET is operated in the off-state, the tunneling barrier between source and channel is very wide so as to prevent the occurrence of tunneling. Therefore, only an extremely low current generated by the reversed-biased leakage current of the p-i-n diode exists in the off-state. On the contrary, for a TFET in the on-state, the applied gate voltage is larger than V_{th}, and thus the valence band of source side will be higher than the conduction band of channel region. This leads to a sufficiently narrow barrier width for the occurrence of tunneling. The band diagrams of a TFET operated in the on/off-states are illustrated in Fig. 4-2. The conduction mechanism of TFET depends on the tunneling barrier width instead of the formation of channel inversion as in conventional MOSFET. As a result, TFETs are not constrained by the same physical limitation as MOSFETs, and represent a promising candidate for sub-60 mV/dec of *SS*.

On the other hand, one of the issues induced by the SCEs in conventional MOSFETs is an increase in off-state leakage owing to the restriction of non-scalable *SS*. Since the suppression of the penetration of drain-side depletion region into channel is effective to cope with the leakage current, channel doping prolife engineering appears to be one of the promising solutions. Some options have been proposed such as source-to-drain nonuniformity doped channel MOSFET [5], tilt-implanted punchthrough stopper scheme [6], super-steep-retrograde channel profile [7], elevated S/D structure [8], and asymmetric S/D extension structure [9-11] to reduce the leakage currents and increase the SCE immunity. Moreover the implementation of halo implant fulfills modulation of channel doping profile by means of locally forming the p-type doping regions underneath the n-type S/D extensions with higher concentration than substrate. The halo doping can suppress the penetration of drain-side electric field into channel, hence the punchthrough issue can be relieved as well. In addition, the SCE immunity can be accomplished by improving the drain-induced barrier lowering (DIBL) with the aid of halo doping. Nevertheless, the use of overdosed halo doping would lead to unwanted band-to-band tunneling (BTBT) occurring between drain extension and

halo region. Besides, the increase of local substrate doping concentration with halo scheme would probably result in the increment of V_{th} or reverse-short-channel effect (RSCE), degrading the current drivability. In short, the implementation of halo is a trade-off between the SCE immunity and device performance, and thus the optimization of halo doping is important. As far as the process cost is concerned, symmetrical doping structures, including halo dopings, are adopted in standard CMOS fabrication. However, the halo doping can be implemented to accomplish the asymmetrical structure in terms of boosting the device performance as pointed out previously [12-14]. For instance, the source-junction-only halo doping scheme can reduce the capacitance of n^+p junction at the drain junction, and further good SCE immunity and reliability would be expected by means of modulating asymmetrical S/D and halo doping profiles carefully. On the other hand, halo doping would ruin Early voltage (V_A), which increased slowly with channel length, resulted in a large drain-induced V_{th} shift (DITS) and low output resistance to long channel devices, therefore making certain halo processes unsuitable for analog applications [15-16]. Accordingly, the effect of halo implant parameters on the tradeoff between digital and analog performance is essential.

Both TFETs and asymmetrical-halo-doping MOSFETs inherently are asymmetrical architectures, and thus the corresponding fabrication is quite suitable with the DP technique introduced in the previous chapters. Since the feasibility of double-patterning (DP) technique has been confirmed in the previous chapters, and therefore we will discuss two kinds of asymmetrical source/drain (S/D) devices in terms of device fabrication, electrical characterization and correlative reliability issues in this chapter.

4.2 Device Fabrication

After confirming the feasibility of the proposed DP technique in the previous chapters, we have also implemented this technique on the practical fabrication of both TFETs and nano-scale n-channel MOSFETs (nMOSFETs) with or without asymmetric halo doping architecture. Figure 4-3 illustrates the major process steps in the device fabrication of TFETs. Single-crystal TFETs were fabricated on 6-inch (100) p-type wafers with resistivity of 15~25 Ω-cm. Local oxidation of Si (LOCOS) scheme was first used for device isolation. Channel stop implantation was performed by implanting BF_2^+ (120 keV, 4×10^{13} cm^{-2}), followed by wet oxidation to form 550 nm-thick field oxide.

Anti-punchthrough (APT) and threshold voltage adjustment implantation are skipped for realizing the intrinsic channel of gated p-i-n diode. After RCA clean, thermal gate oxide of about 2.5 nm was grown in an N_2O ambient using a vertical furnace, followed by the deposition of a 100 nm-thick *in situ* phosphorous-doped poly-Si layer to serve as the gate electrode, as shown in Fig. 4-3 (a). Mask G1 was first applied to generate photoresist (PR) patterns covering portions of the poly-Si, as shown in Fig. 4-3 (b), followed by a reactive ion etch (RIE) step done by a Lam-TCP9400 to remove the uncovered poly- Si. N-type drain formation was performed with As^+ implantation at 10 keV and 5×10^{14} cm^{-2}, as shown in Fig. 4-3 (c). The second lithographic step with mask G2 was then employed to generate PR patterns which covered portions of the poly-Si layer remaining on the surface of the substrate [Fig. 4-3 (d)], followed by an RIE step to complete the final poly-Si structure. P-type source was formed by implanting BF_2^+ with split conditions as shown in Table 4-1 [Fig. 4-3 (e)]. Spike-1000 ^{o}C rapid thermal anneal (RTA) process was then carried out in a nitrogen ambient to activate dopants in the gate and S/D junctions, as depicted in Fig. 4-3 (f). Afterwards, standard back-end process was carried out. All wafers were deposited with a 500 nm-thick tetraethoxysilane (TEOS) oxide passivation layer by plasma enhanced chemical vapor deposition (PECVD) system. Contact holes were then etched, followed by 600 nm-thick Al-Si-Cu metallization to form the metal pads. All processing steps were completed with a forming gas anneal at 400 °C for 30 minutes.

Next, we introduce another process flow of asymmetrical halo nMOSFETs. Since the process is similar to device fabrication described in Chapter 2, we only describe some key process parameters in this section. Figure 4-4 illustrates the major process steps in the device fabrication. Thermal gate oxide of about 2.5 nm was grown in an N_2O ambient using a vertical furnace, followed by the deposition of a 100 nm-thick *in situ* phosphorous-doped poly-Si layer to serve as the gate electrode. A 50 nm-thick TEOS oxide layer was deposited upon the poly-Si layer to serve as hard mask, as shown in Fig. 4-4 (a). Asymmetrical halo structure was implemented by implanting BF_2^+ (50 keV, 5×10^{12} cm^{-2}, tilt angle =45°) (denoted as "Asy-Halo") during the first gate pattern definition, while the symmetrical counterpart was accomplished by BF_2^+ implant after gate pattern definition (denoted as "Sym-Halo"). Some wafers skipping the halo implantations, denoted as "Control", serve as the control samples. Shallow S/D extensions were formed by implanting As^+ (10 keV, 1×10^{15} cm^{-2}). After forming a 100

nm-thick TEOS sidewall spacer by PECVD system, deep S/D junctions were formed by implanting As^+ (20 keV, 2×10^{15} cm^{-2}) and P_{31}^+ (10 keV, 5×10^{15} cm^{-2}) in sequence, and then rapid thermal anneal (RTA) was carried out in a nitrogen ambient at 1000 ^oC for 5 seconds to activate dopants in the gate and S/D junctions, as depicted in Fig. 4-4 (f). Figure 4-5 is a SEM picture showing the cross-sectional image of the fabricated nMOSFET with nominal gate length of 80 nm. The overall implantation conditions used in the device fabrication were marshaled as shown in Tables 4-1 and 4-2 for TFETs and n-MOSFETs, respectively. Cross-sectional views of TFETs and the four splits of nMOSFETs are shown in Fig. 4-6.

4.3 Measurement Setup

4.3-1 Electrical Measurement Setup

Electrical measurements of all devices were performed by an HP4156A precision semiconductor parameter analyzer, an HP4284 LCR meter, an Agilent-E5250A switch, an Agilent-8110A pulse generator, and a temperature-regulated hot chuck. The hot chuck was used to maintain the measurement temperature at 25 ^oC. The measurement systems were applied to record the current-voltage (I-V) characteristics and test the hot-carrier reliability.

4.3-2 Hot-Carrier Stress Measurement Setup

In this study, we have executed the hot-carrier stress (HCS) to explore the impact of asymmetrical halo structure on device performance. The test samples with the channel width (W) of 10 μm and channel length (L) of 0.1 μm are chosen for the sake of small fluctuation in device characteristics as compared with L of 0.08 μm. In addition, devices for HCS were stressed with the drain voltage set at a highly positive voltage, and the gate terminal was biased at the voltage where maximum absolute value of substrate current (I_{sub}) occurred to accelerate the degradation. To find the condition, we first measured the I_{sub}-V_G characteristics with drain terminal biased at moderate positive drain voltage. To monitor the hot-electron induced degradation, both the I_D-V_G characteristics at V_{DS} = 50 mV (linear region) and charge pumping current were measured before and after the stress. The degradations in terms of threshold voltage shift (ΔV_{th}), generation of interface trap density (ΔN_{it}), transconductance degradation (ΔGm) and so on, were examined and recorded in the accelerated stress test.

4.3-3 Charge Pumping Measurement Setup

The charge pumping method, first proposed by Brugler and Jespers in 1969, is a powerful tool for interface trap measurements on small-geometry MOSFETs instead of large-diameter MOS capacitors [17]. In addition, this measurement allows the exclusion of gate leakage contribution to the calculated interface state densities existing within thin gate oxides and at lower frequencies [18-19], so we don't need to pay attention to the leakage issue for precisely analyzing the interface state densities or the bulk traps in the gate dielectrics from the charge pumping measurement results. For better comprehension of the damage mechanism induced by HCS, it is important to profile the distributions of both generated interface states and trapped charges by the charge pumping method. The basic measurement is composed of applying a small fixed reverse bias to the S/D, connecting the substrate to ground, and performing a series of base voltage pulses with fixed amplitude, rise time, fall time, frequency, and duty cycle to the gate of the device from a low accumulation level to a high inversion level. The maximum charge pumping current will occur when the base level is lower than the flat-band voltage and the top level of the pulse is higher than the threshold voltage, revealing that once the device is pulsed from inversion toward accumulation, the net charges will be transferred from the S/D to the substrate through the fast interface traps and result in the charge pumping current. An MOSFET with a gate area of A_G (=W×L) gives the charge pumping current (I_{cp}) as [20]:

$$I_{cp} = q \cdot f \cdot A_G \cdot N_{it} \quad \text{(4-4)},$$

while the interface trap density (N_{it}) could be calculated from this equation. On the contrary, the fast interface traps are continuously filled with electrons in the inversion level or holes in the accumulation level for nMOSFETs, while the base level of the pulse is higher than the threshold voltage or the top level is lower than the flat band voltage. It is impossible to generate the recombination current, and therefore no I_{cp} can be collected.

There are three conventional types of voltage pulse train individually applying to the gate electrode, which are named as follows: (a) fixed peak sweep, (b) fixed base sweep, and (c) fixed amplitude sweep, as illustrated in Fig. 4-7. In this thesis, "fixed amplitude sweep" is used to calculate interface trap density, and "fixed base sweep" mode is used to analyze the lateral distribution of interface trap, respectively. The basic setup of charge pumping measurement is shown in Fig. 4-8. Both source and drain are

biased at 50 mV while the substrate electrodes are connected to ground. Square-wave waveforms with 1 MHz provided by HP8110A are applied to the gate, and the base voltage is varied to transfer the surface condition from inversion to accumulation, while keeping the pulse amplitude at 1.5 V. In addition, the lateral distribution of generated interface states after the hot-carrier stress is extracted and discussed in this chapter. This scheme is developed by C. Chen *et al*. [21], and the measurement setup is shown in Fig. 4-9. The measurement procedures are described below:

(1) Measure the I_{cp}-V_h curve (V_h is the high level of the pulsed voltage train applied to the gate as depicted in Fig. 4-9) on a virgin MOSFET from the drain junction (with the source junction floating), thereby establishing the V_h versus $V_{th}(x)$ relationship near the junction of interest [22].

(2) Record the I_{cp}-V_h characteristics after HCS.

(3) Get the hot-carrier-induced interface state distribution, $N_{it}(x)$, from the difference of the I_{cp}-V_h curves before and after HCS.

4.3-4 Flicker Noise Measurement Setup

Figure 4-10 illustrates the experimental setup for measuring low frequency flicker noise. The transistor is coupled to the pre-amplifier and noise analyzer. The output of the pre-amplifier is connected to the dynamic signal analyzer (DSA), executing both sampling and computing the Fast Fourier Transform of the input signal, and then calculates the density spectrum at the frequency of interest. A personal computer (PC) is used to control the correlative setups of measurement parameters, including the range of frequency and the voltage for four terminals (*i.e.*, gate, drain, source, and bulk). Besides, an I-V meter is applied to measure the electrical characteristics and check if the test samples have failed during measurement. In this chapter, the frequency range of noise measurement is set from 10 Hz to 1 kHz.

4.4 Results and Discussion

4.4-1 Electrical Characteristics of TFETs

For all the measurements on the TFETs, we define the n^+ region as drain and the p^+ region as source. Dependence on different source dose splits of TFETs with W of 10 μm and L of 0.2 μm is shown in Fig. 4-11 biased at drain voltage (V_D) of 0.5 V and source voltage (V_S) of -0.5 V, respectively. In this plot, none of them shows the emblematic

character of a TFET, *i.e.*, a steep *SS* of sub-60 mV/dec, and the average *SS* of fabricated TFETs is beyond 300 mV/dec, indicating that even if the highest dose ($1x10^{15}$ cm^{-2}) is adopted to increase the penetration probability of carriers, it still fails. This failure in steep SS would be ascribed to some potential culprits discussed as follows. Based on the work developed by Z. Qin *et al*. [23], *SS* can be reduced by increasing two components expressed as below:

$$SS = \ln 10[\frac{1}{V_{eff}} \times \frac{dV_{eff}}{dV_{GS}} + \frac{\xi + b}{\xi^2} \times \frac{d\xi}{dV_{GS}}]^{-1} \quad \text{..................(4-5)}$$

,

while the tunnel-junction bias (V_{eff}) governed by the gate-to-source voltage (V_{GS}) is described as the first component in this equation, revealing that the implementation of both high-κ dielectric and ultra-thin body would be helpful. The second component describes that increasing the derivative of the junction electric field (ξ) on the V_{GS} is effective to steepen *SS*. However, both the tunnel-junction bias (V_{eff}) and ξ are coupled and cannot be engineered independently. Therefore, steepening *SS* is simpler to accomplish by the adoptions of high-κ dielectric and ultra-thin body. According to Eq. 4-5, both thick gate oxide of 2.5 nm and bulk silicon substrate of the fabricated TFET are the main culprits of flattening *SS*.

To demonstrate the functionality of p-i-n diode (source-channel-drain) in our fabricated TFET, we set the gate floating and applied voltage at the source side (p^+ region) to comprehend the dependence of channel length on the channel conductance, as illustrated in Figs 4-12 and 4-13. Figure 4-12 shows the absolute value of source current versus source voltage curves with various channel length and W of 10 μm, indicating that all curves follow their good p-i-n diode behaviors. On the contrary, for those TFETs with the nominal channel length shorter than 100 nm, all the characteristics act like failed p-n diodes with incredible leakage currents as shown in Fig. 4-13, implying that the intrinsic portion of channel seems to disappear. Such phenomenon probably resulted from the thermal budget of dopant activation process, and hence the reliable channel length of fabricated TFETs is 200 nm as depicted in Fig. 4-12. The dependence of channel length on drain current is inherently different between TFETs and MOSFETs. For the drain current behavior of TFET, Eq. 4-6 built by Krishna Kumar Bhuwalka *et al*. [24] identifies the drain current of a TFET is independent of channel length.

$$I_{DS} = \frac{(e^2 m_o^{1/2})}{(18\pi\hbar^2)} D^2 W_g^{-1/2} V_{GS}^2 e^{-[(\pi m_o^{1/2})/(2e\hbar)W_g^{3/2} / (V_{GS}D)]} \quad \text{..............(4-6)},$$

where e is the electronic charge, m_o is the carrier effective mass, $\hbar$ is the Planck's constant, W_g is the bandgap, D is a function of V_{DS}, oxide thickness, doping concentrations and channel length (E_{max}=DV_{GS}, the maximum electric field across the tunnel junction). Figures 4-14 and 4-15 show the aforementioned channel-length dependence of nMOSFETs and TFETs, respectively. As can be seen in Fig. 4-14, drain current shows strong dependence on the channel length. On the contrary, the transfer characteristics of TFETs show indistinct I_{DS} dependence on the channel length as illustrated in Fig. 4-15. Next, the impact of drain-to-source voltage (V_{DS}) on the drain current is discussed with W/L = 10 μm/0.2 μm as shown in Fig. 4-16. In this plot, we set V_{DS} at 1.25 V and modulate the drain voltage from -0.25 V to 0.75 V with step of 0.25 V. From these different biased transfer curves, we find that they are not only parallel to one another but spaced out 0.25 V apart. The shifted transfer curves correspond with the same V_D step of 0.25 V, agreeing with the work proposed by P.-F. Wang *et al.* [25]. In addition, the steepest *SS* among these biasing conditions occurring at V_D of 0.25 V and V_S of -1 V is 231 mV/dec, while the minimum value of average *SS* occurring at V_D of 0.75 V and V_S of -0.5 V is 367 mV/dec in the range of drain current between 10^{-11} A and 10^{-9} A. According to Eq. 4-7 [24], *SS* can be expressed as:

$$SS = \frac{V_{GS}^2}{2V_{GS} + \left((\pi m_o^{1/2}) / (2e\hbar) \cdot W_g^{3/2} \right) / D} \quad \text{.....................(4-7)},$$

so we can see that *SS* is directly proportional to V_{GS} (strong dependence) and inversely proportional to W_g (weak dependence). Furthermore, the tunnel barrier width can be lowered with increasing V_{GS} to improve the tunneling probability and drop *SS* [24]. Therefore precise control of S/D doping profile is extremely important for significant occurrence of BTBT, the doping concentration must be higher than 10^{19} cm^{-3}. Without abrupt S/D junction, the tunneling width would become long and worsen the *SS*. The doping concentration of boron in the source junction plotted by means of computer simulations for the fabricated TFETs is illustrated in Fig. 4-17. From this doping distribution plot, we clearly demonstrate our critical tunneling junction is not abrupt enough to BTBT, resulting in smooth *SS* beyond 300 mV/dec in average.

4.4-2 Electrical Characteristics of nMOSFETs

Figure 4-18 shows the transfer characteristics of all splits measured at V_D=0.05 and 1.2 V with W/L = 10 μm/80 nm. Here we define the junction with halo as source in the Asy-Halo split for the forward mode operation, and thus the source of Asy-Halo split is biased with V_D for the reverse mode operation denoted as Asy-Halo-R. As can be seen in the plot, the bulk punchthrough current becomes noticeable and leads to the horrible degradation of subthreshold characteristics in the Control split. Because the channel length is downscaling to some extent, even comparable to the depletion width of channel region, the sharing of the charges in the channel depletion region with the S/D junctions becomes noteworthy, and further, brings about the V_{th} lowering. As the gate length becomes shorter, the gate controllability becomes more impotent. On the contrary, the implementation of halo implantation in Sym-Halo split is helpful in keeping the subthreshold characteristics steep, and reducing the off-state leakage current (I_D at V_G = 0 V) by four orders of magnitude over the control, ascribed to both the improved subthreshold swing and the increased V_{th}. With the aid of halo implant, not only the depletion width of channel region can be reduced by increasing the substrate doping concentration locally, but also the lowering in surface potential barrier height with a high V_D can be relieved. As far as the suppression of off-state leakage current is concerned, the Sym-Halo split is more efficient than the Asy-Halo split due to its inherently bilateral halo dopings, and therefore less penetration of drain-side electric field. Furthermore, the location of halo doping plays an important role in increasing the SCE immunity for the asymmetrical structures. As can be seen in the plot, the Asy-Halo-R split shows an improved DIBL as compared with the Asy-Halo counterpart, implying that the drain-side halo is more helpful than the source-side halo in suppressing the penetration of drain-side electric field into the channel region. Therefore, the halo doping is effective to restrain the SCEs even if unilateral structure is adopted. The transconductance characteristics of all splits measured at V_D=0.05 V with W/L = 10 μm/80 nm are plotted in Fig. 4-19. The output characteristics of all splits measured at V_G-V_{th} = 0~2 V in step of 0.4 V with W/L = 10 μm/80 nm are compared and shown in Fig. 4-20. Both transconductance and output characteristics of the Sym-Halo device are the worst among all splits and lower than the Control split by 19% (transconductance) and 25% (output current), respectively. This indicates that halo dopings would significantly degrade the device performance, which could be ascribed to the RSCE and

the degenerate carrier mobility induced by extra substrate doping in the channel. In fact, since the Asymmetric Halo split suffers from less degradation as compared with bilateral halo doping architecture (Sym-Halo), it shows a 7.8% higher transconductance and a 15% larger driving current. Even if the unilateral doping structure is adopted in the Asy-Halo-R split, there are 4.6% reduction of transconductance and 10% reduction of driving current as compared with the Asy-Halo counterpart. The differences of transconductance and driving current between the Asy-Halo and Asy-Halo-R splits result from the fact that the width of depletion region at drain junction is slightly thicker than that at source junction biased at a small V_D, thus V_{th} of the Asy-Halo-R split is slightly higher than that of the Asy-Halo split, leading to the performance degradation. Threshold voltage roll-off characteristics of all splits measured at V_D = 0.05 V are shown in Fig. 4-21. The threshold voltage is defined as the gate voltage at drain current of (W/L) × 10 nA. The Sym-Halo split shows obvious RSCE among all splits because halo doping would increase the substrate doping concentration near the edge of the channel, and therefore causing the regional V_{th} rising. Besides, the V_{th} of Asy-Halo split is less than that of the Asy-Halo-R split with downscaling channel length due to their different depletion widths. In the case of Asy-Halo-R split, drain bias is applied at the drain junction with halo doping, and thus the width of depletion region at drain is thinner than that of the Asy-Halo counterpart. As a result, V_{th} of the Asy-Halo-R split is slightly higher than that of the Asy-Halo split. Figure 4-22 illustrates the drain-induced-barrier-lowering (DIBL) as a function of channel length for all splits to evaluate the short channel effect. We use the interpolation method to calculate DIBL effect. It is clearly seen that the devices with halo schemes depict better DIBL distribution, especially the bilateral halo structure. On the other hand, subthrehold swing (SS) is another criterion to evaluate the short channel effect. The *SS* as a function of channel length for all splits measured at V_D = 0.05 V is plotted in Fig. 4-23. It can be seen that the Control split shows the worst *SS* degradation with decreasing channel. In addition, both Sym-Halo and Asy-Halo-R devices exhibit excellent robustness to SCE, implying that the drain-side halo undoubtedly increases the SCE immunity by effectively suppressing the penetration of drain-side electric field and reducing the drain-side depletion width. The Asy-Halo-R device has less penetration of electric field and smaller depletion width of the drain junction, and therefore, gives rise to the enhanced SCE immunity, including less V_{th} roll-off, better DIBL and steeper *SS*, as compared with the Control and Asy-Halo devices. However, you cannot sell the cow

and sup the milk. Halo implant also brings some side effects such as the drain-substrate coupling, the degradation of driving current and the enhanced RSCE. Figure 4-24 exhibits the on-state current (I_{on}) as a function of channel length for all splits to evaluate the penalty of halo implant. I_{on} is measured at V_G -V_{th} = 1 V and V_D = 1.2 V. The Sym-Halo device exhibits the worst I_{on} degradation among all splits, which is ascribed to the degenerate carrier mobility induced by extra substrate doping in the channel, while Asy-Halo and Asy-Halo-R splits show better current drivability due to their inherently unilateral halo structures. On the contrary, the Sym-Halo device shows the lowest off-state current (I_{off}) as depicted in Fig. 4-25. The reduction of I_{off} with halo scheme is ascribed to the V_{th} increment induced by RSCE. Figures 4-26 and 4-27 exhibit the transfer characteristics of 15 Control and 15 Sym-Halo nMOSFETs, respectively, with W/L = 10 μm/80 nm measured at V_D = 1.5 V to leverage the degraded current drivability induced by the halo implant. As can be seen in these plots, the halo implant is beneficial to tightening the variation of device characteristics. Clearly the bilateral halo structure (Sym-Halo) can help reduce the device variation. Similar measurements were also performed on the unilateral-halo devices. The transfer characteristics of 15 Asy-Halo and 15 Asy-Halo-R nMOSFETs are shown in Figs. 4-28 and 4-29, respectively, with W/L = 10 μm/80 nm measured at V_D = 1.5 V. The results clearly show that the Asy-Halo-R devices exhibit a tighter distribution of the current-voltage curves, confirming the ability of drain-side halo in preventing the penetration of electric field from the nearby junction into the channel.

4.4-3 Hot-Carrier Stress (HCS) of Asymmetrical Halo nMOSFETs

Next, we shift our attention to the hot-carrier characterization to discuss the impacts of bilateral or unilateral halo structures on the device reliability. The degradation induced by HCS in MOSFETs closely depends on the drain-side impact ionization under a high electric field horizontally [26-27]. The produced hot carriers are injected into the gate dielectric by hot-carrier injection, and thus lead to the interface states causing V_{th} shift, *SS* increment and performance degradation as time goes by [28]. In our case, these HCS-induced electrons and holes are collected by the drain and substrate terminals, respectively. Therefore, the substrate current (I_{sub}) can be used to monitor hot-carrier effect, and the impact ionization rate (I_{sub}/I_D) has been adopted to evaluate the amount of electron-hole pairs generated by impact ionization. Figure 4-30

shows the substrate current (I_{sub}) versus gate voltage for all splits of devices measured at V_D of 3 V with W/L = 10 μm /100 nm. As can be seen in the plot, the devices with halo schemes exhibit larger I_{sub} than the Control device, especially the Sym-Halo split. Figure 4-31 depicts the impact ionization rate (I_{sub}/I_D) for all splits of devices measured at V_D of 3 V with W/L = 10 μm /100 nm, and the adoption of halo architecture causes higher impact ionization rate (I_{sub}/I_D), while high I_{sub}/I_D is closely connected with the device with halo doping at drain side. In other words, the halo doping apparently has direct impact on the impact ionization process and the associated byproducts, hot electrons. In addition, both the largest I_{sub} and I_{sub}/I_D of Sym-Halo split can be ascribed to the highest peak electric field under the gate edge of drain junction, consistent with the simulation results presented by T. N. Buti *et al.* [29-30] On the other hand, the Control and Asym-Halo devices exhibit lower I_{sub} and I_{sub}/I_D than those devices with drain-side halo structure, owing to the absence of lateral electric field induced by the drain-side halo doping [30]. As a result, drain-side halo doping would aggravate the hot-carrier degradation due to its higher lateral electric field, and the correlative tests will be discussed as follows.

To confirm the aforementioned halo-induced hot-carrier degradation, the transfer characteristics of stressed samples are measured before and after the 5000-second HCS as shown in Figs. 4-32 ~ 4-35. The I_D-V_G characteristics were measured at V_D = 0.05 V with W/L = 10 μm/100 nm. The devices were stressed at V_D = 3 V and V_G at the maximum substrate current ($Isub_{max}$). As can be seen in these plots, the Sym-Halo device exhibit the worst hot-carrier degradation among all splits, including V_{th} shift, transconductance (Gm) reduction and SS increase. The aggravation is alleviated in the device with source-side halo doping (Asy-Halo), though the resultant degradation is still worse than the Control split. In order to observe the evolution of degradation, some characteristics as a function of stress time are measured and compared, including the V_{th} shift (ΔV_{th}), the degraded peak transconductance (ΔGm), and the increased interface state density (ΔN_{it}) as shown in Figs. 4-36 ~ 4-38. First of all, we define the degradation as the stressed value subtracting from the virgin value, such as $\Delta V_{th} = V_{th}(t) - V_{th}(0)$. According to these resultant degradation indexes, the devices with drain-side halo doping (Sym-Halo and Asy-Halo-R) indeed show worsened hot-carrier degradation in terms of larger shift in these parameters, further demonstrating the aggravated hot-carrier degradation induced by drain-side halo doping as mentioned above. The primary culprit for the aggravated degradation is believed to be the lateral electric field

under the gate edge of drain junction boosted by the drain-side halo implant [30]. Although both the Sym-Halo and the Asy-Halo-R splits possess the same drain-side-halo architecture, the Sym-Halo device exhibits the severest aggravation in hot-carrier degradation among all splits of devices. According to Buti's simulation results [30], the peak of lateral electric field at the drain-side halo region for the Sym-Halo split is much higher than that of the Asy-Halo-R split, and the different peak electric fields should be responsible for the aggravated degradation in the Sym-Halo split. Figure 4-39 shows the difference of charge pumping current (ΔI_{cp}) before and after a 5000-second HCS among all splits. After hot-carrier stress, we can see that more interface states are generated for both drain-halo splits, while the source-halo (Asy-Halo) split suffers from less aggravated degradation, though the resultant ΔI_{cp} is still worse than the Control split. The trend of interface state generation is consistent with those of above-mentioned threshold voltage shift and increased interface state density.

4.4-4 Lateral Distribution of Interface Trap Density of Asymmetrical Halo nMOSFETs

The measurement procedures of this method have been described in Section 4.3-3, and we will use it to extract the lateral distribution of interface trap states. It should be noted that the local threshold voltage (V_{th}) and flat-band voltage (V_{fb}), across the channel of MOSFET, are not uniform due to the lateral doping variation, as shown in Fig. 4-40. In order to detect the interface states, the voltage pulses applied during measurements must undergo alternating accumulation and inversion cycles. Therefore, there should be no Icp as the high-level voltage (V_h) is lower than the minimum V_{th} under the gate. Only after V_h starts to exceed the local V_{th} in the channel will I_{cp} begin to grow. Before V_h reaches the maximum local V_{th} in the channel, only interface states residing near the drain side (*i.e.*, the shadow region in Fig. 4-40) will contribute to I_{cp}, while the supplied electrons cannot yet flow to the drain side from the source.

Here we demonstrate the procedure by taking the Control split as an example. If we assume that the interface state density is spatially uniform along the channel, which can be expressed as:

$$I_{cp,\max} = q \cdot f \cdot W \cdot L \cdot N_{it} \quad \text{......(4-8)},$$

where f is the gate pulse frequency, W is the channel width, and L is the channel length.

In Fig. 4-41, the corresponding I_{cp} (V_h) comes from the interface state distributed in the region between the gate edge and the position where its local V_{th} is equals to V_h, *i.e.*,

$$I_{cp}(V_h) = q \cdot f \cdot W \cdot x \cdot N_{it} \quad \text{(4-9)},$$

where x represents the distance from the gate edge to the position where V_{th} (x) = V_h. Comparing Eqs. (4-8) and (4-9), we can derive x as:

$$x = \frac{L \cdot I_{cp}(V_h)}{I_{cp,\max}} \quad \text{(4-10)}.$$

The local V_{th} versus distance x for the control sample is shown in Fig. 4-42. The local V_{th} decreases as x is smaller than 0.06 μm. We can therefore presume that the drain junction is near x = 0.06 μm. The charge pumping currents before and after the 5000-second HCS (V_G@$Isub_{max}$ and V_D = 3 V) are depicted in Fig. 4-43. The incremental in the charge pumping current (ΔI_{cp}), at a given V_h is proportional to the amount of generated interface traps from the gate edge to the point x. ΔI_{cp} can be written as:

$$\Delta I_{cp} = q \cdot f \cdot W \cdot \int_0^x N_{it}(x)dx \quad \text{(4-11)}.$$

Therefore, the N_{it}(x) generated by the hot-carrier stress can be expressed as follows:

$$N_{it}(x) = \frac{d(\Delta I_{cp})}{dx} \cdot \frac{1}{q \cdot f \cdot W} = \frac{d(\Delta I_{cp})}{dV_h} \cdot \frac{dV_h}{dx} \cdot \frac{1}{q \cdot f \cdot W} \quad \text{(4-12)},$$

where the dependence of dV_h/dx on x can be derived from V_h versus x (Fig. 4-41). As a result, the lateral distribution, N_{it}(x), could be obtained from the procedure mentioned above. The derived profiles of the interface states for all splits of devices could be extracted by repeating the same procedure with Eq. (4-12), and the results are shown in Fig. 4-44. From this figure we can directly profile the position-dependent damage region and calculate the amount of interface states generated by the HCS. We can see that the major damage region is confined near the drain edge in all splits. This is reasonable since the hot-carrier effect is known to be an edge-effect stress inherently. It is obviously seen that more interface states are generated in those drain-halo devices, and particularly the Sym-Halo split contributes to the most N_{it} near the drain region, consistent with those trends mentioned above in Section 4.4-3.

4.4-5 Flicker Noise Characteristics on Asymmetrical Halo nMOSFETs

According to previous discussions in Sections 4.4-2 ~ 4.4-4, we realized that halo

doping is capable of reducing off-state leakage current and increasing the SCE immunity at the cost of lower current drivability. In addition, halo would worsen the hot-carrier degradation primarily induced by the drain halo as mentioned above. Next, we shift our attention to evaluate the impact of halo on device performance by investigating the flicker noise (1/f) characteristics before and after the hot-carrier stress. Before we set about the correlative study on 1/f noise, more comprehending on the mechanism that dominates the 1/f noise is our primary task. In the past, there were two major theories to explain the physical origins of flicker noise in MOSFETs. One is the number fluctuation theory based on McWhorter's charge trapping model [31]. The other is the bulk mobility fluctuation theory based on Hooge's empirical relation [32]. In the carrier number fluctuation theory, the random trapping and detrapping processes of charges occurred in the oxide traps near the interface between Si channel and SiO_2 are the culprit of flicker noise [31, 33-34], which was originally presented by McWhorter in 1957 [31]. These fluctuations can also cause fluctuations in the channel mobility because these traps act as Coulomb scattering sites when they capture a carrier, known as the mobility number fluctuation theory [32, 35]. As a result, these traps or interface states are believed to be the major culprits for flicker noise.

Later a unified flicker noise model which was proposed by K. K. Hung [36] incorporated both the carrier number fluctuation theory and the mobility fluctuation mechanism to explain the origin of low-frequency noise in a correlated manner. The total drain current noise power can be expressed as

$$S_{id}(f) = \frac{1}{L^2}\int_0^L S_{\Delta id}(x,f)\Delta x dx = \frac{kTI_d^2}{\gamma f W L^2}\int_0^L N_t(E_{fn})\left[\frac{1}{N(x)} \pm \alpha\mu\right]^2 dx \quad \text{..........(4-13)}$$

,

where $N_t(E_{fn})$ is the oxide trap density at Fermi level E_{fn}; $N(x)$ is the number of channel carriers per unit area; α is the Columbic scattering parameter; γ is the attenuation coefficient and typically is equal to 10^8 cm^{-1} [37]. The drain current noise spectrum density (S_{id}) of a virgin Control device measured at a gate overdrive of 0.1 V ($V_G - V_{th}$ = 0.1 V) and V_D = 0.05 V with W/L = 10 μm/100 nm is shown in Fig. 4-45. The distinguishing feature of flicker noise can be clearly identified with the frequency index γ close to one as the sloped line inserted in the $1/f^{\gamma}$ spectrum figure, indicating that the measured low-frequency noise in our device belongs to flicker (1/f) noise. Figure 4-46 illustrates the drain current noise spectrum density for all splits of virgin devices

measured at a gate overdrive of 0.1 V and V_D = 0.05 V with W/L = 10 μm/100 nm. As can be seen in the plot, the Sym-Halo split exhibits larger S_{id} than others, similar with the previously discussed trends, implying that halo doping would possibly worsen low-frequency noise for the moment. Both the normalized noise power spectrum density (S_{id}/I_D^2) and transconductance to current ratio squared $(gm/I_D)^2$ as a function of drain current for two splits of devices (Control and Sym-Halo) with W/L = 10 μm/0.2 μm at 100 Hz are shown in Figs. 4-47 and 4-48, respectively. Based on the efforts made by Ghibaudo and Bouchacha [38], the noise characteristics would be suitably explained by the carrier number fluctuation theory if the S_{id}/I_D^2 is proportional to the $(gm/I_D)^2$. On the contrary, the noise characteristics would be dominated by the Hooge's mobility fluctuation theory if the S_{id}/I_D^2 is proportional to the reciprocal of the drain current from the weak to strong inversion. As can be seen in the figures, the S_{id}/I_D^2 is proportional to the $(gm/I_D)^2$, and thus the number fluctuation model dominates the noise characteristics in our case. Furthermore, both Control and Sym-Halo splits have similar S_{id}/I_D^2 dependence on the $(gm/I_D)^2$, implying that halo doping would not alter the mechanism of noise characteristics in our devices.

In our low-frequency noise measurement discussed as follows, each noise measurement datum point contains an average of 5 to 10 devices for the sake of reducing the characteristic deviation coming from the miniature device size [39] and further verifying the trend of device characteristics. The noise is measured in linear region (V_D = 0.05 V) to minimize the influence of drain bias on the inversion charges, and the noise data are sampled at 100 Hz. In addition, the devices were stressed at V_D = 3 V and V_G at the maximum substrate current ($Isub_{max}$). To investigate the noise behavior of asymmetrical halo nMOSFET post the hot-carrier degradation, the low-frequency noise characteristics of test samples are measured before and after the 5000-second HCS. The S_{id}/I_D^2 as a function of gate overdrive for all splits of devices measured at V_D = 0.05 V and sampled at 100 Hz with W/L = 10 μm/10 μm is shown in Fig. 4-49, and the differences among all samples are small, implying that the halo doping causes negligible impact on the noise characteristics and the halo-implant-induced non-uniform threshold voltage distribution is insignificant in these long-channel devices. On the contrary, the noise characteristics of all splits are quite different for the short-channel devices (L = 0.1 μm) as shown in Fig. 4-50. As can be seen in the plot, the halo-implant-induced noise degradation is much obvious in the short-channel devices due to noticeably non-uniform threshold voltage distribution

along the channel induced by the halo implant. Based on the efforts made by J. W. Wu *et al.*[40], the noise behavior can be simplified as follows, assuming the distribution of oxide trap density is uniform along the channel.

$$\frac{S_{id}(f)}{I_D^2} = \frac{kTq^2}{\alpha f W L_{eff}^2 C_{ox}^2} \cdot N_t(E_{fn}) \cdot \left[\frac{L_1}{(V_G - V_{th1})^2} + \frac{L_2}{(V_G - V_{th2})^2} + \frac{L_3}{(V_G - V_{th3})^2} \right] \quad (4\text{-}14),$$

where L_1, L_2, L_3, are the effective channel lengths of three regions along the channel with different threshold voltages, and V_{th1}, V_{th2}, V_{th3} are the threshold voltages corresponding to the regions with various lengths of L_1, L_2, L_3, respectively. For the region with L_2 located at the channel center, its threshold voltage, V_{th2} is smaller than V_{th1} and V_{th3} with the halo dopings. As a result, the Sym-Halo device with larger V_{th1} and V_{th3} in the halo regions would induce a larger noise fluctuation than the Control device for the short-channel case (L = 0.1 μm) according to Eq. 4-14. The asymmetrical halo devices, including Asy-Halo and Asy-Halo-R splits, show better noise immunity than the Sym-Halo counterpart, which is ascribed to their inherently unilateral structures, as shown in Fig. 4-50. On the other hand, the middle factor in Eq. 4-14 will dominate in the long-channel device, and hence, there is no obvious difference in noise characteristics among all splits of devices as illustrated in Fig. 4-49, inferring that the noise component associated with the halo region is negligible for long-channel case.

Figure 4-51 shows the drain current noise spectrum density for all splits of hot-carrier stressed devices measured at a gate overdrive of 0.1 V and V_D = 0.05 V with W/L = 10 μm/100 nm. As can be seen in the plot, all splits of devices exhibit increased S_{id} curves post the HCS, inferring that the extra oxide traps generated by HCS would worsen the noise characteristics. Besides, both Sym-Halo and Asy-Halo-R splits exhibit larger S_{id} than others, similar with the previously discussed trend in Section 4.4-3, implying that drain-halo doping would aggravate the HC degradation, and further deteriorate low-frequency noise. Figures 4-52 ~ 4-55 illustrate the S_{id}/I_D^2 as a function of gate overdrive before and after the 5000-second HCS for all splits of devices measured at V_D = 0.05 V and sampled at 100 Hz with W/L = 10 μm/100 nm. The increase in normalized noise power spectrum density ($\Delta S_{id}/I_D^2$) as a function of gate overdrive for all splits of devices is shown in Fig. 4-56. As can be seen in the plot, the Sym-Halo device indeed depicts the largest shift, and the Asy-Halo split, suffering from less drain-halo-induced degradation than the Asy-Halo-R counterpart, shows better noise immunity post the HCS, though the resultant $\Delta S_{id}/I_D^2$ of Asy-Halo is still worse

than the Control split. In a word, halo doping causes much severe noise degradation due to non-uniform threshold voltage distribution especially with the downscaling channel length. Drain-side halo doping aggravates the HC degradation and deteriorates low-frequency noise further.

4.5 Summary

In this chapter, we have fabricated and characterized both asymmetrical devices, including TFETs and asymmetrical halo nMOSFETs with the delivered double-patterning technique in order to investigate the operation mechanism of TFET and the nMOSFET design for reliability and performance.

For the fabricated TFETs, an on-to-off current ratio of about 4~5 orders in magnitude was achieved, and the minimum SS was about 230~260 mV/dec, which is ascribed to the failure of forming abrupt junction profile and the reduction of BTBT. The spike RTA employed in this work seems not appropriate for the requirement of abrupt junction profile. Besides, the adoptions of both bulk silicon substrate and 2.5 nm-thick gate oxide are main culprits of flattening SS. Therefore, the uses of high-κ dielectric, ultra-thin channel, innovative architecture, heterojunction materials, and so on will be indispensable for the implementation of TFET and boosting of the performance.

For the fabricated nMOSFETs, we have discovered the symmetrical halo-doping structure helps reduce the subthreshold leakage in terms of off-state-current suppression by four orders in magnitude, and improves the SCEs. But, the halo doping also increases V_{th} with the shrinking channel length and induces severe RSCE, resulting in the degraded current drivability. The implementation of asymmetrical halo structure relieves the aforementioned dilemma. The drain-side halo structure (Asy-Halo-R) exhibits better SCE immunity than the Asy-Halo counterpart, which is ascribed to the effective suppression of penetration of electric field from the drain junction. In reliability test, we found that the drain-side halo doping is the primary culprit of hot-carrier degradation due to the increased peak lateral electric field, while the Asy-Halo device suffers from less hot-carrier degradation, boosting the hot-carrier reliability. The measured results of lateral distribution of N_{it} in this work also confirm that the drain-side halo doping aggravates the hot-carrier degradation with more interface state generation for both devices (Sym-Halo and Asy-Halo-R) with drain-side

halo structure. Finally, we have evaluated the impact of halo on device performance by investigating the flicker noise (1/f) characteristics before and after the hot-carrier stress. For the virgin devices, we found that halo implantation does not change the mechanism of noise characteristics. The halo implant-induced non-uniformity of the threshold voltage along the channel is significant for the short-channel device and results in worse noise performance. On the contrary, the long-channel device is free from the aforementioned impact with similar noise behavior for all splits of devices. Through the normalized noise power spectrum density ($\Delta S_{id}/I_D^2$) measurements before and after the HCS, we conclude that drain-side halo doping aggravates the HC degradation and deteriorates low-frequency noise further.

ES A
1896

References

[1] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. New York: Wiley, 2007.

[2] S. Banerjee, W. Richardson, J. Coleman and A. Chatterjee, "A new three-terminal tunnel device," *IEEE Electron Device Lett*., vol. ED-8, no. 8, pp. 347-349, 1987.

[3] Toshio Baba, "Proposal for surface tunnel transistors," *Jpn. J. Appl. Phys*., vol. 31, pp. 455-457, 1992.

[4] William M. Reddick and Gehan A. J. Amaratunga, "Surface tunnel transistor," *Appl. Phys. Lett*., vol. 67, no. 4, pp. 494-496, July 1995.

[5] Y. Okumura, "A novel source-to-drain nonuniformity doped channel (NUDC) MOSFET for high-current drivability and threshold voltage controllability," in *IEDM Tech. Dig*., 1999, pp. 391-394.

[6] T. Hori, "A 0.1-μm CMOS technology with tilt-Implanted punchthrough stopper (TIPS)," in *IEDM Tech. Dig*., 1994, pp. 75-78.

[7] I. De and C. M. Osburn, "Impact of super-steep-retrograde channel doping profiles on the performance of scaled devices," *IEEE Trans. on Electron Devices*, vol. 46, no. 8, pp. 1711-1717, 1999.

[8] H. Tian, K. W. Kim, J. R. Hauser, N. A. Masnari, and M. A. Littlejohn, "Effects of profile doped elevated source/drain structures on deep-submicron MOSFETs," *Solid-State Electronics*, vol. 38, no. 3, pp. 573-579, 1995.

[9] T. Ghani, K. Mistry, P. Packan, M. Armstrong, and S. Thompson, "Asymmetric source/drain extension transistor structure for high performance sub-50nm gate length CMOS devices," in *VLSI Symp. Tech. Dig.*, 2001, pp. 17-18.

[10] T. Murakami, T. Yoshimura, Y. Goto, and S. Kimura, "Gate length scalability of N-MOSFET's down to 30nm: Comparison between LDD and Non-LDD structures," *IEEE Trans. on Electron Devices*, vol. 47, no. 4, pp. 835-840, 2000.

[11] J. F. Chen, J. Tao, P. Fang, and C. Hu, "Performance and reliability comparison between asymmetric and symmetric LDD devices and logic gates," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 367-371, 1999.

[12] W. Yeh and J. Chou, "Optimum halo structure for sub-0.1 μm CMOSFETs," *IEEE Trans. on Electron Devices*, vol. 48, no. 10, pp. 2357-2362, Oct. 2001.

[13] A. Bansal, and K. Roy, "Asymmetric halo CMOSFET to reduce static power dissipation with improved performance," *IEEE Trans. on Electron Devices*, vol. 52,

no. 3, pp. 397-405, Mar. 2005.

[14] S. Odanaka and A. Hiroki, "Potential design and transport property of 0.1-μm MOSFET with asymmetric channel profile," *IEEE Trans. on Electron Devices*, vol. 44, no. 4, pp. 595-600, Apr. 1997.

[15] A. Chatterjee, K. Vasanth, D. T. Grider, M. Nandakumar, G.. Pollack, R. Aggarwal, M. Rodder, and H. Shichijo, "Transistor design issues in integrating analog functions with high performance digital CMOS," in *VLSI Symp. Tech. Dig.*, 1999, pp. 147-148.

[16] K. M. Cao, W. Liu, X. Jin, K. Vasanth, K. Green, J. Krick, T. Vrotsos, and C. Hu, "Modeling of Pocket Implanted MOSFETs for Anomalous Analog Behavior," in *IEDM Tech. Dig.*, 1999, pp. 171-174.

[17] J. S. Brugler and P. G. A. Jespers, "Charge Pumping in MOS Devices," *IEEE Trans. on Electron Devices*, vol. 16, pp. 297-302, 1969.

[18] S. S. Chung, S. J. Chen, C. K. Yang, S. M. Cheng, S. H. Lin, Y. C. Sheng, H. S. Lin, K. T. Hung, D. Y. Wu, T. R. Yew, S. C. Chien, F. T. Liou, and F. Wen, "A novel and direct determination of the interface traps in sub-100nm CMOS devices with direct tunneling regime (12-16Å) gate oxide," in *VLSI Symp. Tech. Dig.*, 2002, pp. 74-75.

[19] P. Masson, J. L. Autran, and J. Brini, "On the tunneling component of charge pumping current in ultrathin gate oxide MOSFET's," *IEEE Electron Device Lett.*, vol. 20, no. 2, pp. 92-94, 1999.

[20] D. K. Schroder, *Semiconductor material and device characterization*, 3rd ed. New York: Wiley, 2009, Ch. 4.

[21] C. Chen and T. P. Ma, "Direct lateral profiling of hot-carrier-induced oxide charge and interface traps in thin gate MOSFET's," *IEEE Trans. on Electron Devices*, vol. 45, no. 2, pp. 512-520, 1998.

[22] M. Tsuchiaki, H. Hara, T. Morimoto, and H. Iwai, "A new charge pumping method for determining the spatial distribution of hot-carrier induced fixed charge in p-MOSFET's," *IEEE Trans. on Electron Devices*, vol. 40, no. 10, pp. 1768-1778, 1993.

[23] Z. Qin, Z. Wei, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *IEEE Electron Device Lett.*, vol. 27, no. 4, pp. 297-300, 2006.

[24] K. K. Bhuwalka, Jörg Schulze and I. Eisele, "A simulation approach to optimize the electrical parameters of a vertical tunnel FET," *IEEE Trans. on Electron Devices*, vol. 52, no. 7, pp. 1541-1547, 2005.

[25] P.-F. Wang, K. Hilsenbeck, Th. Nirschl, M. Oswald, Ch. Stepper, M. Weis, D. Schmitt-Landsiedel, and W. Hansch, “Complementary tunneling transistor for low power application,” *Solid-State Electronics*, vol. 48, no. 12, pp. 2281-2286, 2004.

[26] H. Wong, “A physical based drain avalanche breakdown model for MOSFET’s,” *IEEE Trans. on Electron Devices*, vol. 42, no. 12, pp. 2033-2035, 1997.

[27] A. Das, H. De, V. Misra, S. Venkaresan, and S. Veeraraghavan, “Effects of halo implant on hot carrier reliability of sub-quarter micron MOSFETs,” in *Proc. Int. Reliability Physics Symp.*, 1998, pp. 189-193.

[28] H. S. Momose, S. Nakamura, T. Ohguro, T. Yoshitomi, E. Morifuji, T. Morimoto, Y. Katsumata, and H. Iwai, “A study of hot-carrier degradation in n- and p-MOSFETs with ultra-thin gate oxides in the direct-tunneling regime,” in *IEDM Tech. Dig*., 1997, pp. 453-456.

[29] T. N. Buti, S. Ogura, N. Rovedo, K. Tobimatsu, and C. F. Codella, “Asymmetrical halo source GOLD drain (HS-GOLD) deep sub-half micron n-MOSFET design for reliability and performance,” in *IEDM Tech. Dig*., 1989, pp. 617-620.

[30] T. N. Buti, S. Ogura, N. Rovedo, and K. Tobimatsu, “A new asymmetrical halo source GOLD drain (HS-GOLD) deep sub-half-micrometer n-MOSFET design for reliability and performance,” *IEEE Trans. on Electron Devices*, vol. 38, no. 8, pp. 1757-1764, 1991.

[31] A. L. McWhorter, *1/f noise and germanium surface properties*, in *Semiconductor Surface Physics*. Philadelphia: University of Pennsylvania Press, 1957, p.207.

[32] F. N. Hooge, “1/f noise is no surface effect,” *Phys. Lett. A*, vol. 29a, pp. 139-140, 1969.

[33] A. L. McWhorter, “Semiconductor surface physics,” Ph. D. dissertation, Lincoln Lab., Mass. Inst. Technol., Lexington, MA, 1955.

[34] Y. Nemirovsky, I. Brouk, and C. G. Kakobson, “1/f noise in CMOS transistors for analog applications,” *IEEE Trans. on Electron Devices*, vol. 38, no. 8, pp. 1757-1764, 1991.

[35] T. G. M. Kleinpenning, and L. K. J. Vandamme, “Model for 1/f noise in metal-oxide-semiconductor transistors,” *J. Appl. Phys.*, vol. 52, no. 3, pp. 1594-1596, 1981.

[36] K. K. Hung, P. K. Ko, C. Hu and Y. C. Cheng, “A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors,” *IEEE Trans. on Electron Devices*, vol. 37, no. 3, pp. 654-665, 1990.

[37] S. Christensson I. Lundstrom and C. Svensson, “Low frequency noise in MOS transistors-I Theory,” *Solid-State Electronics*, vol. 11, no. 9, pp. 797-812, 1968.

[38] G. Ghibaudo and T. Bouchacha, “Electrical noise and RTS fluctuations in advanced CMOS devices,” *Microelectronic Reliability*, vol. 42, no. 4, pp. 573-582, 2002.

[39] R. Brederlow, W. Weber, D. S. Landsiedel, and R. Thewes, “Fluctuations of the low-frequency noise of MOS transistors and their modeling in analog and RF-circuits,” in *IEDM Tech. Dig*., 1999, pp. 159-162.

[40] J. W. Wu, C. C. Cheng, K. L. Chiu, J. C. Guo, W. Yi. Lien, C. S. Chang, G. W. Huang, and T. Wang, “Pocket implantation effect on drain current flicker noise in analog nMOSFET devices,” *IEEE Trans. on Electron Devices*, vol. 51, no. 8, pp. 1262-1266, 2004.

Table 4-1 Overall implantation conditions used in the device fabrication of TFETs.

Conditions	Ion	Energy / Dose / Tilt angle / Twist angle
Channel Stop	BF_2^+	120 keV / 4×10^{13} cm^{-2} / 7° / 22°
n-type drain	As^+	10 keV / 5×10^{14} cm^{-2} / 0° / 0°
p-type source	BF_2^+	10 keV / 2×10^{14} cm^{-2} / 0° / 0°
		10 keV / 4×10^{14} cm^{-2} / 0° / 0°
		10 keV / 6×10^{14} cm^{-2} / 0° / 0°
		10 keV / 8×10^{14} cm^{-2} / 0° / 0°
		10 keV / 1×10^{15} cm^{-2} / 0° / 0°

Table 4-2 Overall implantation conditions used in the device fabrication of nMOSFETs.

Conditions	Ion	Energy / Dose / Tilt angle / Twist angle
P-well	BF_2^+	70 keV / 1×10^{13} cm^{-2} / 7° / 22°
Channel Stop	BF_2^+	120 keV / 4×10^{13} cm^{-2} / 7° / 22°
V_{th}	BF_2^+	40 keV / 1×10^{13} cm^{-2} / 7° / 22°
APT	B^+	35 keV / 5×10^{12} cm^{-2} / 7° / 22°
Halo	BF_2^+	50 keV / 5×10^{12} cm^{-2} / 45° / 27°
S/D extension	As^+	10 keV / 1×10^{15} cm^{-2} / 0° / 0°
Deep S/D	As^+	20 keV / 2×10^{15} cm^{-2} / 0° / 0°
	P_{31}^+	10 keV / 5×10^{15} cm^{-2} / 0° / 0°

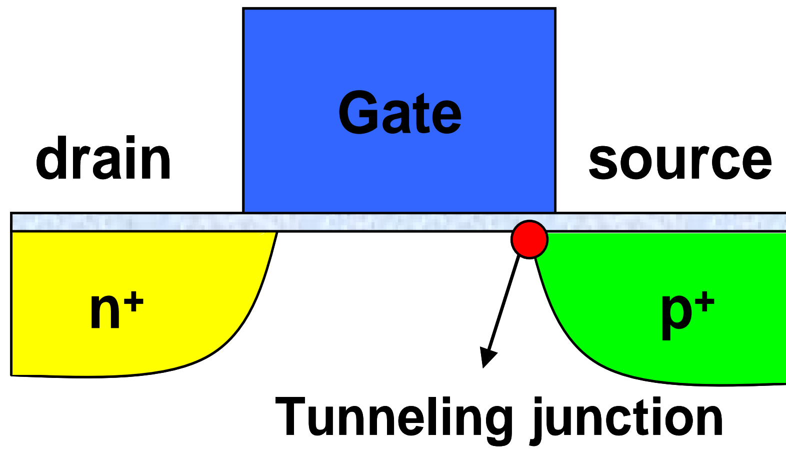


Fig. 4-1 Schematic diagram of a TFET.

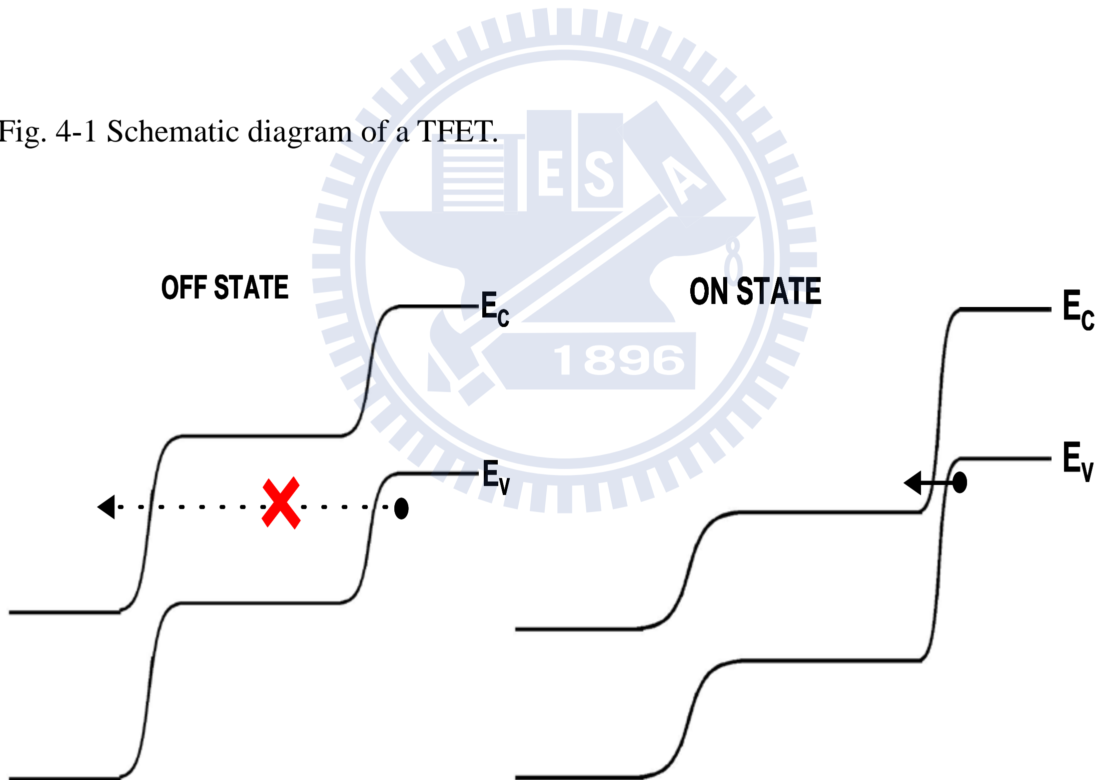


Fig. 4-2 Energy band diagrams of a TFET operated in the on/off-states.

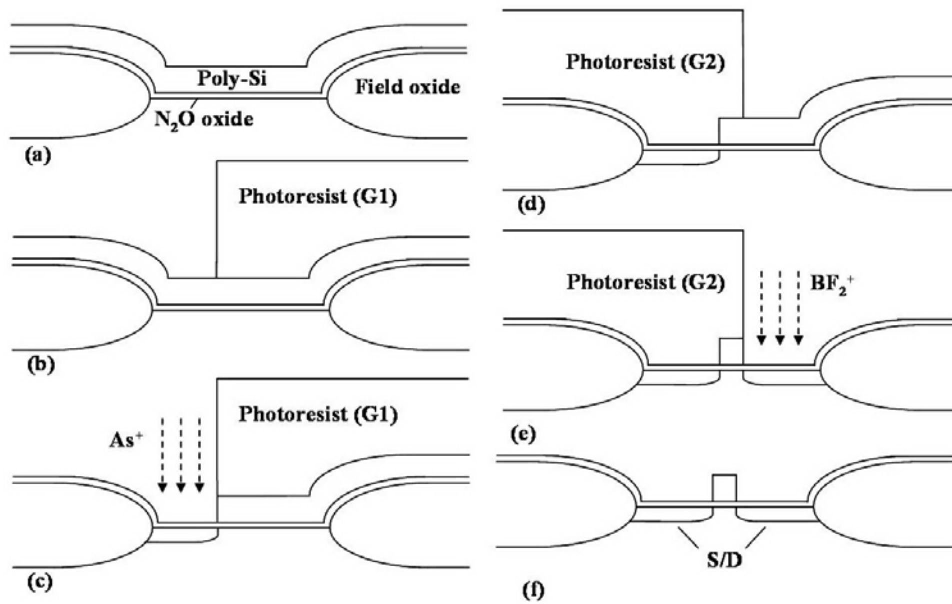


Fig. 4-3 Major process steps for fabricating TFETs with the DP method. (a) Formation of gate oxide and poly-Si on Si wafer with LOCOS isolation. (b) Generation of first PR pattern (G1), (c) First poly-Si etching and drain-junction implant. (d) Generation of second PR pattern (G2), (e) Second poly-Si etching and source-junction implant. (f) Completion of poly-Si gate after second PR removal.

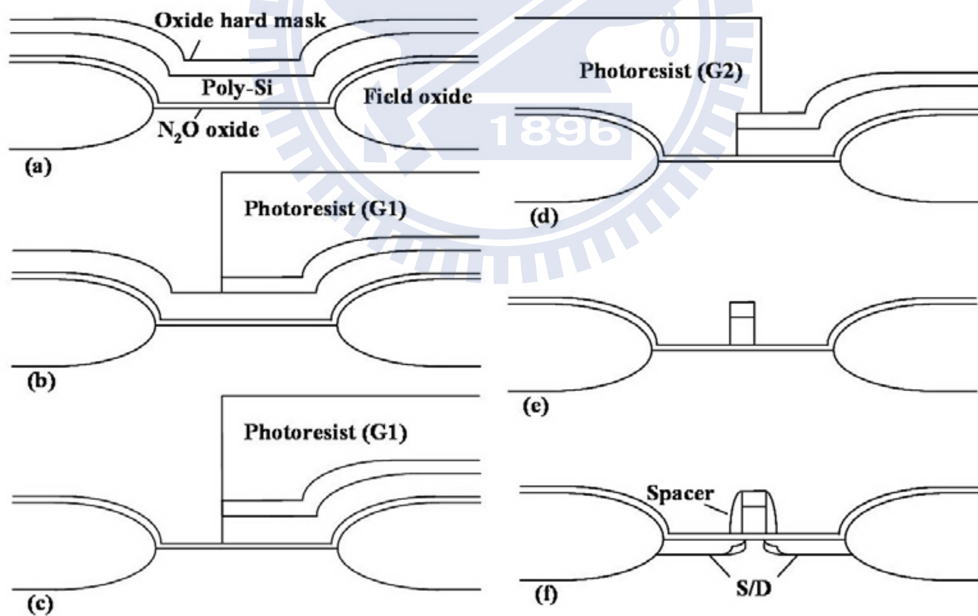


Fig. 4-4 Major process steps for fabricating nMOSFETs with the DP method. (a) Deposition of TEOS oxide hard mask and *in situ* phosphorus-doped poly-Si layers onto N_2O gate dielectric (active region) with LOCOS isolation. (b) Generation of first PR pattern (G1), (c) First oxide/poly-Si etching. (d) Generation of second PR pattern (G2), (e) Second poly-Si etching. (f) Completion of poly-Si gate after second PR removal, and formation of spacer, halo and S/D junctions.

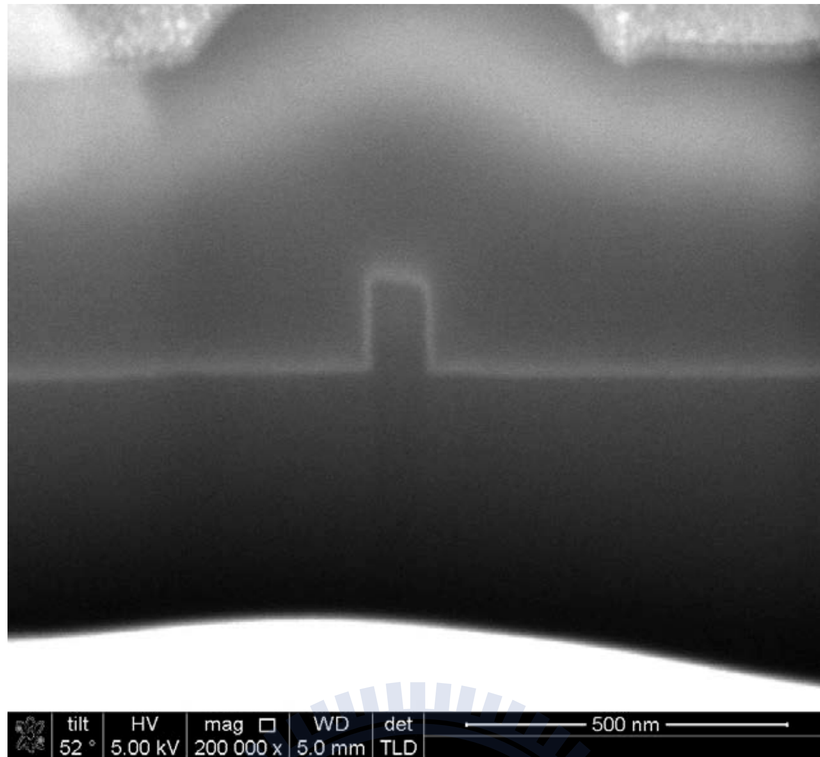
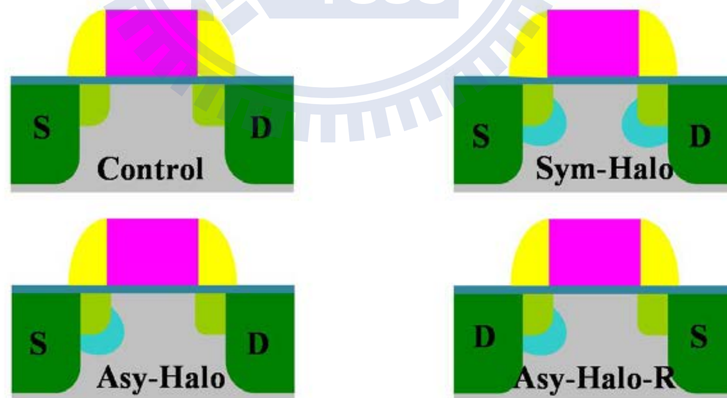


Fig. 4-5 Cross-sectional SEM image of a fabricated nMOSFET with nominal gate length of 80 nm.



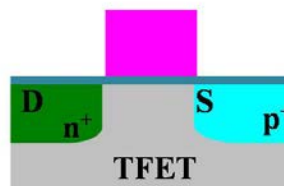


Fig. 4-6 Cross-sectional views of TFETs and the four splits of nMOSFETs.

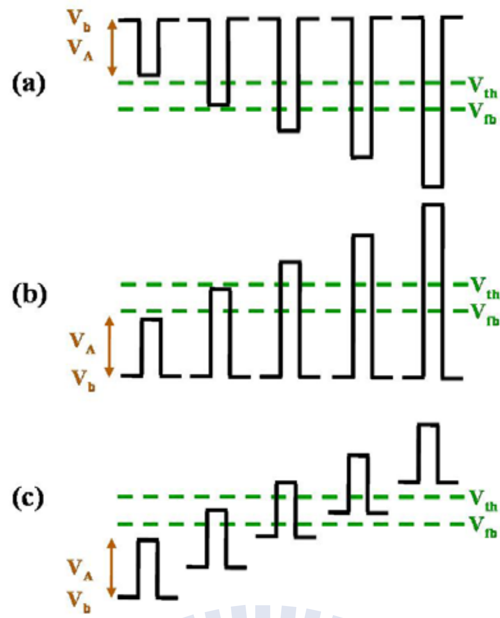


Fig. 4-7 Schematic illustrations for the charge pumping measurements with (a) fixed peak sweep, (b) fixed base sweep, and (c) fixed amplitude sweep.

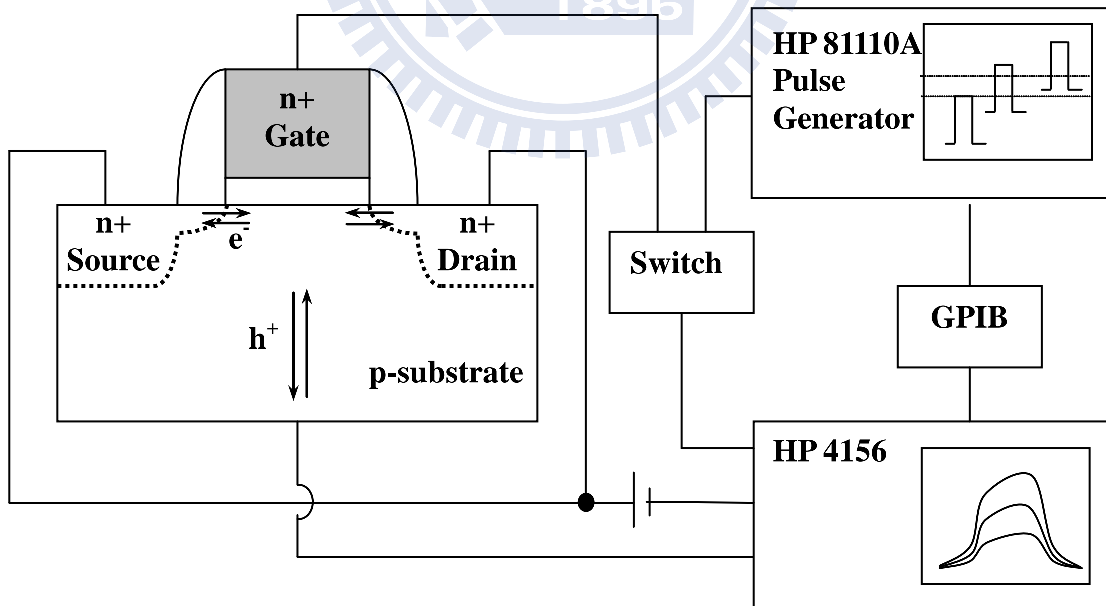


Fig. 4-8 Basic setup for charge pumping measurements.

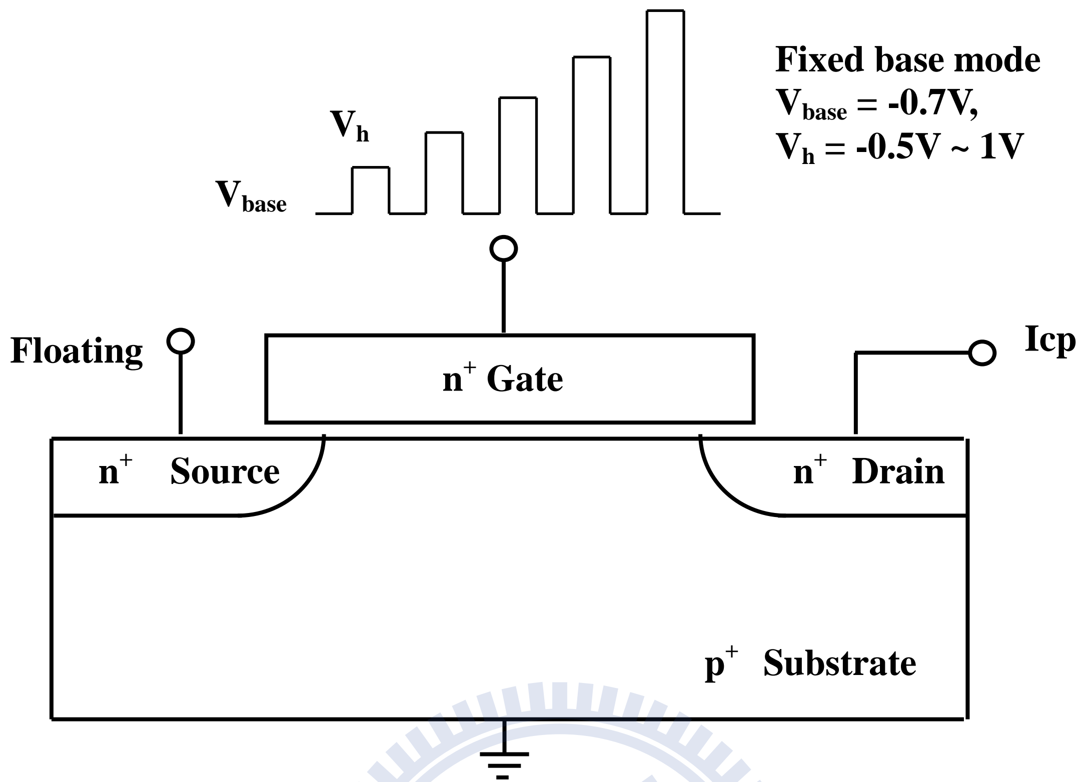


Fig. 4-9 Measurement setup for single-junction charge pumping measurement.

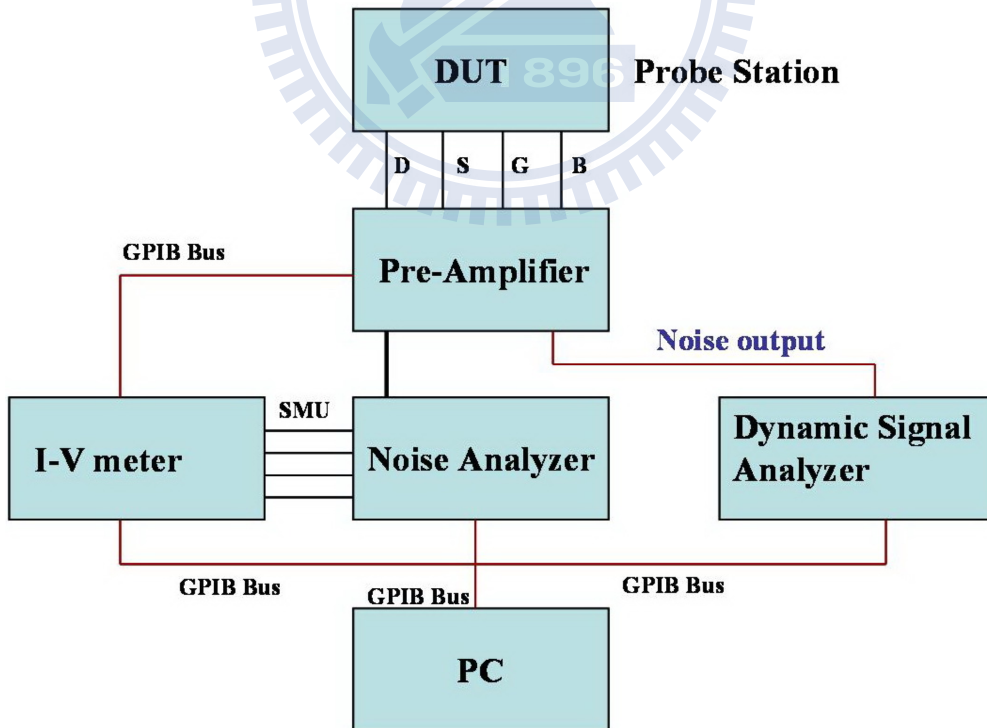


Fig. 4-10 Schematic setup for flicker noise measurements.

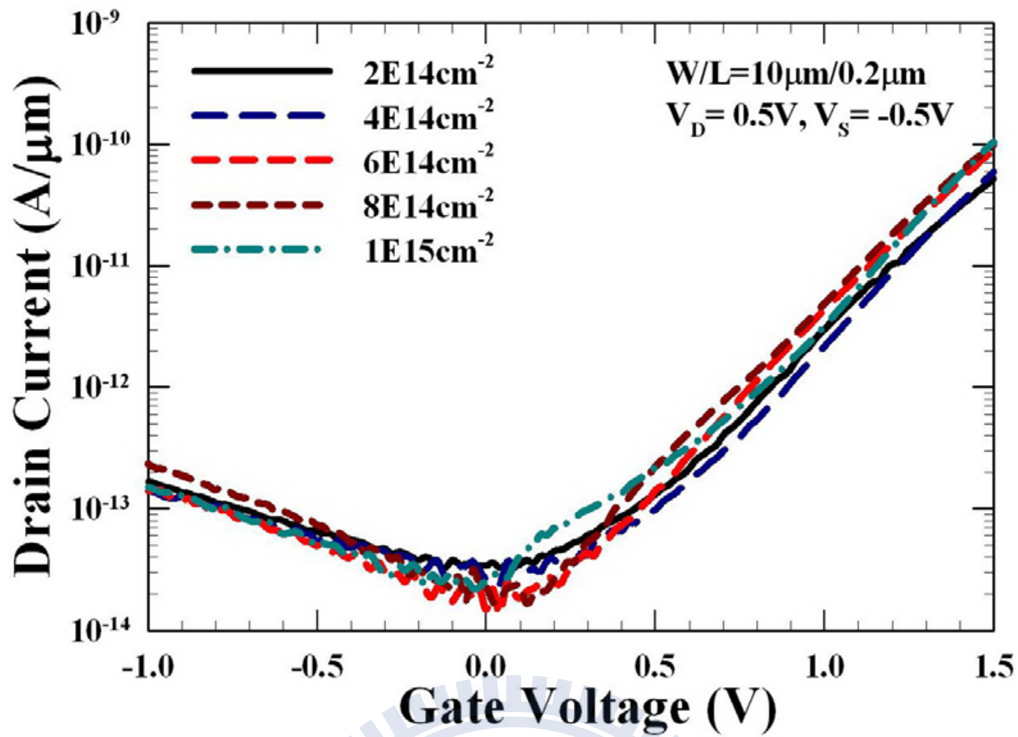


Fig. 4-11 Transfer curves of TFETs for different source dose splits with W/ L = 10 μm/0.2 μm.

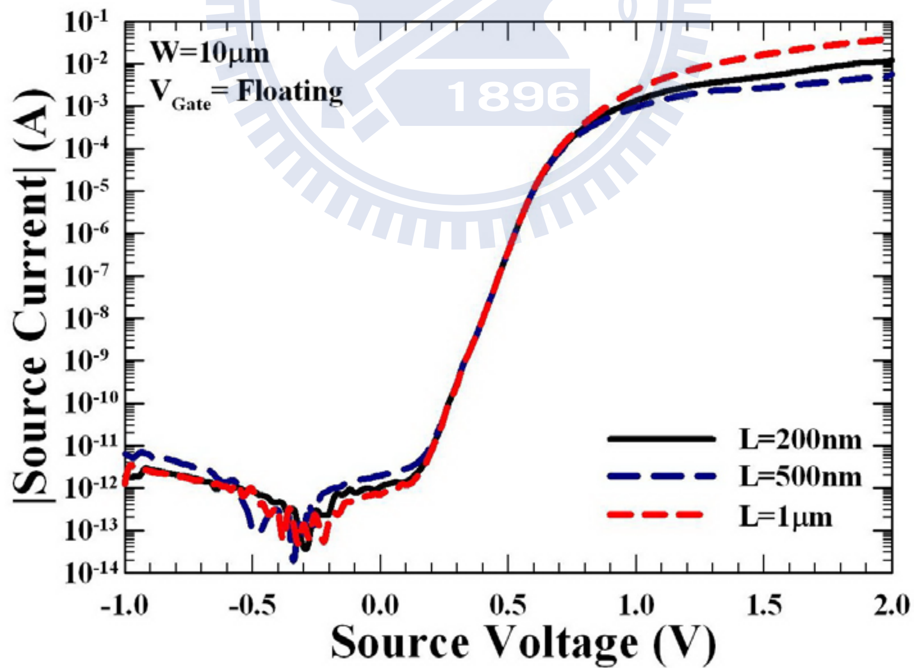


Fig. 4-12 Absolute value of source current versus source voltage curves with various channel length (0.2/0.5/1μm) and W of 10 μm. The gate is floating during measurements.

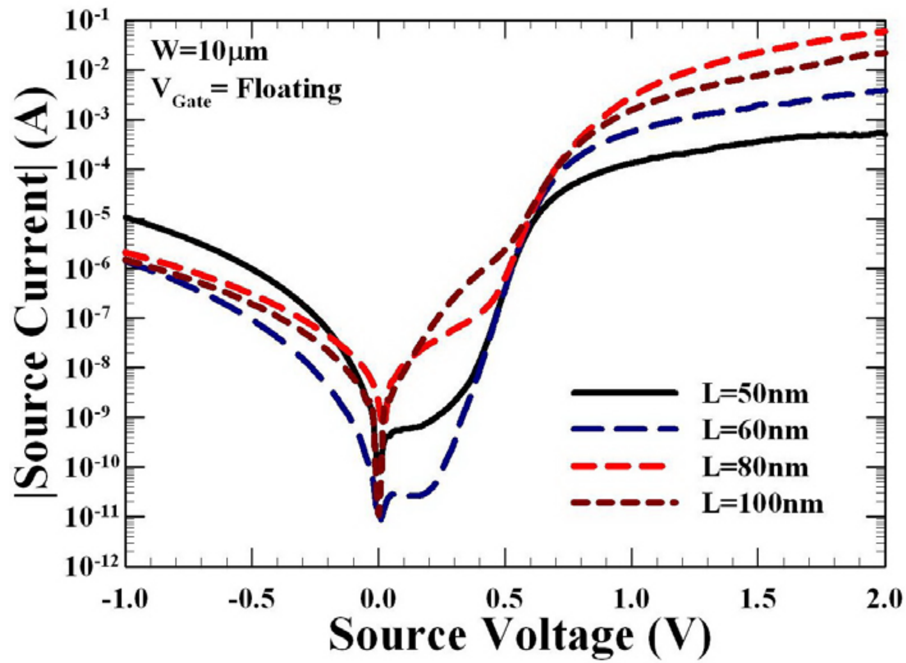


Fig. 4-13 Absolute value of source current versus source voltage curves with various channel length (50/60/80/100nm) and W of 10 μm. The gate is floating during measurements.

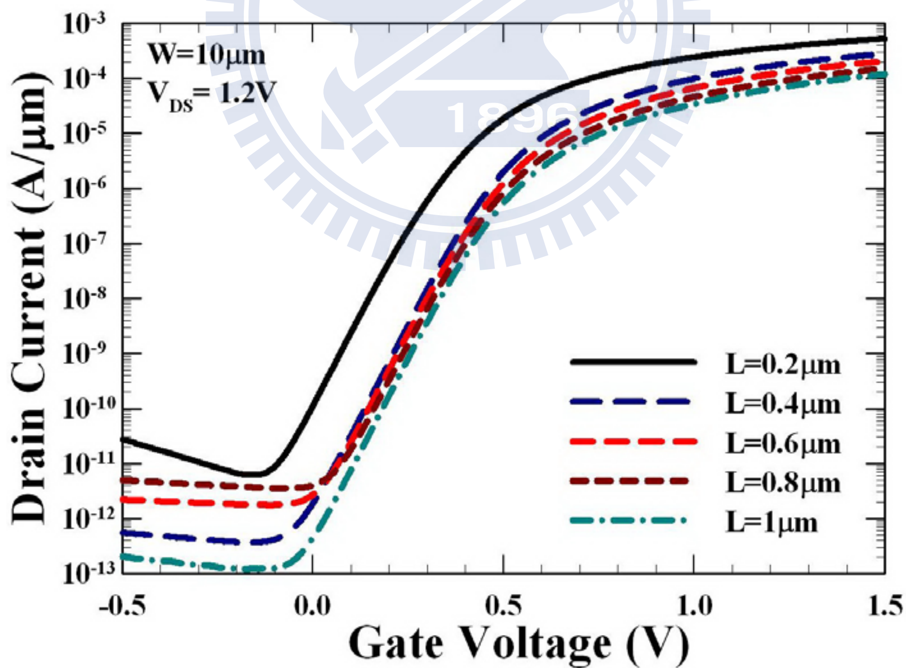


Fig. 4-14 Length dependence of transfer characteristics for nMOSFETs with various channel length and W = 10 μm biased at V_D =1.2 V and V_S =0 V.

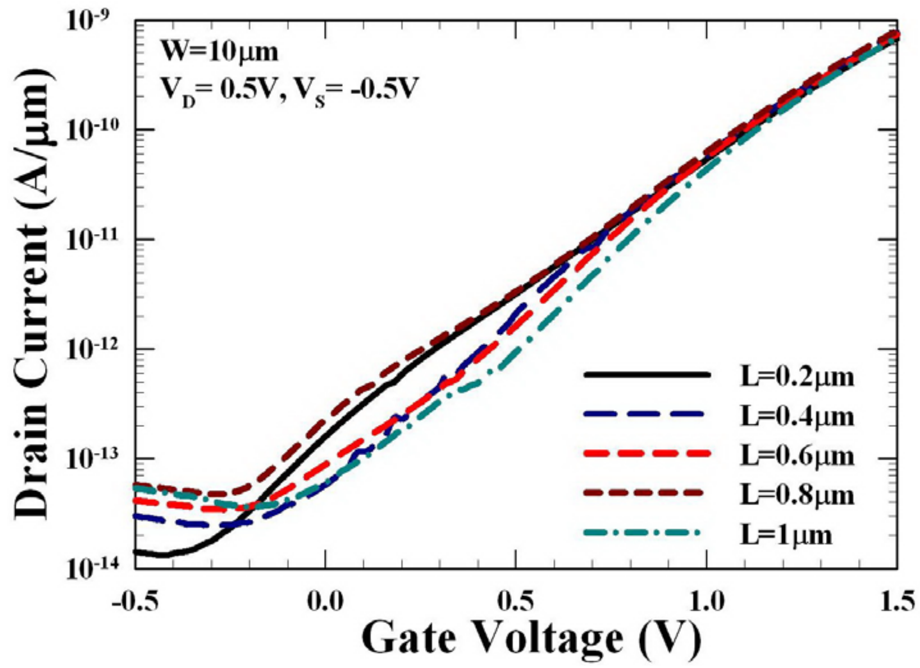


Fig. 4-15 Length dependence of transfer characteristics for TFETs with various channel length and W = 10 μm biased at V_D =0.5 V and V_S = -0.5 V.

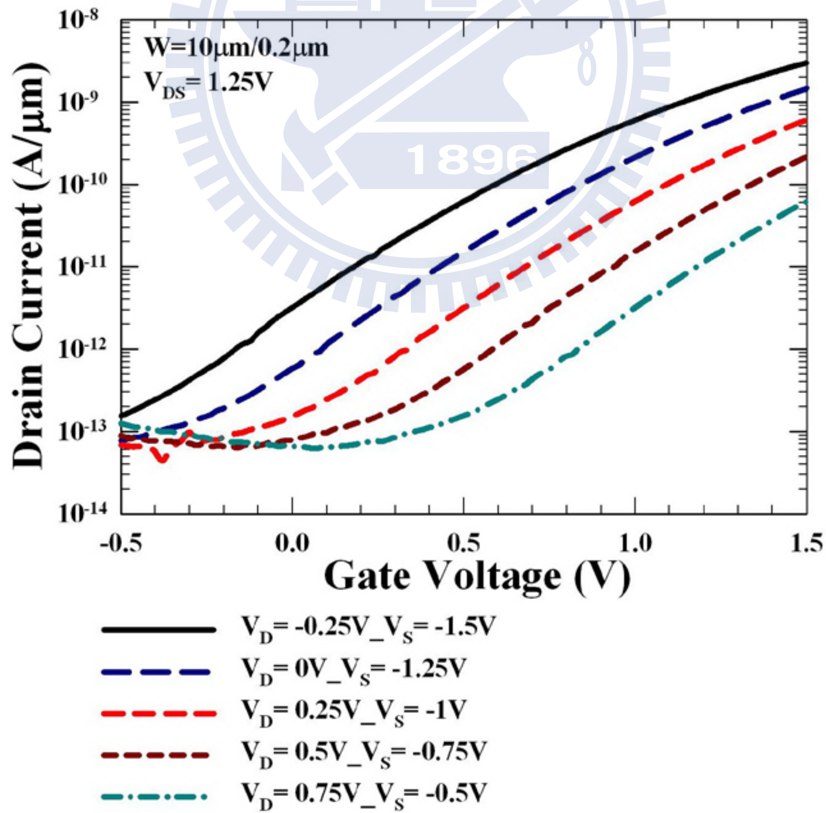


Fig. 4-16 Transfer characteristics of a TFET with constant V_{DS} (1.25V) but different S/D biases. W/L = 10 μm/0.2 μm.

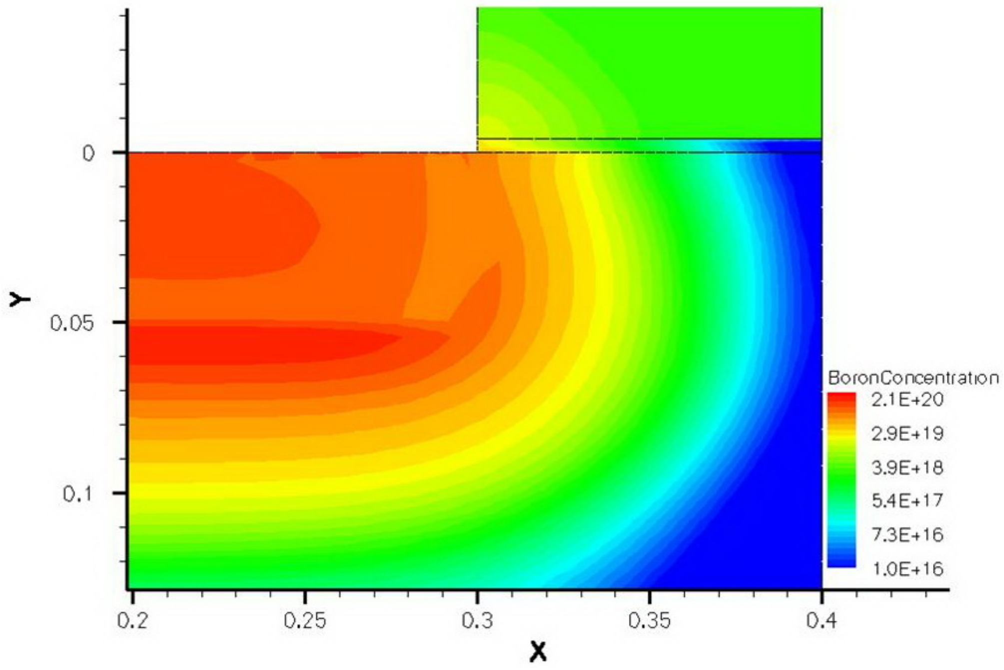


Fig. 4-17 The simulated doping concentration of boron in the source junction for the fabricated TFETs.

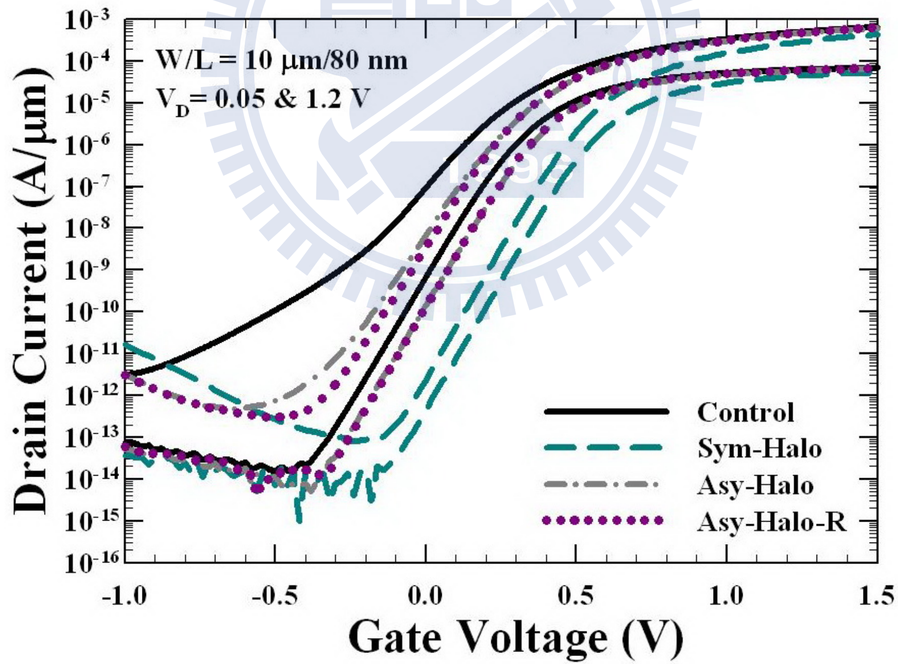


Fig. 4-18 Transfer characteristics of all splits measured at V_D=0.05 and 1.2 V with W/L = 10 μm/80 nm.

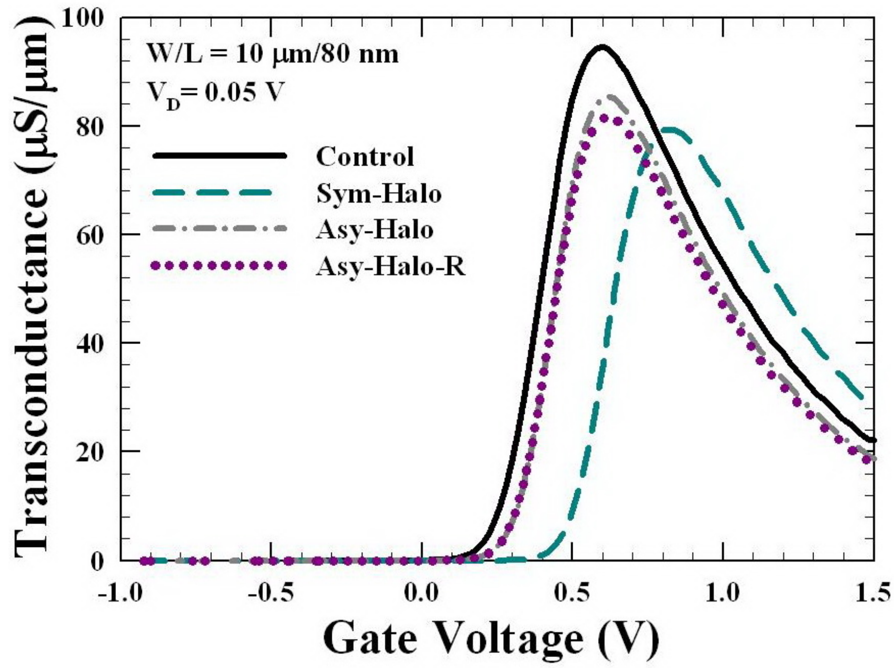


Fig. 4-19 Transconductance characteristics of all splits measured at V_D=0.05 V with W/L = 10 μm/80 nm.

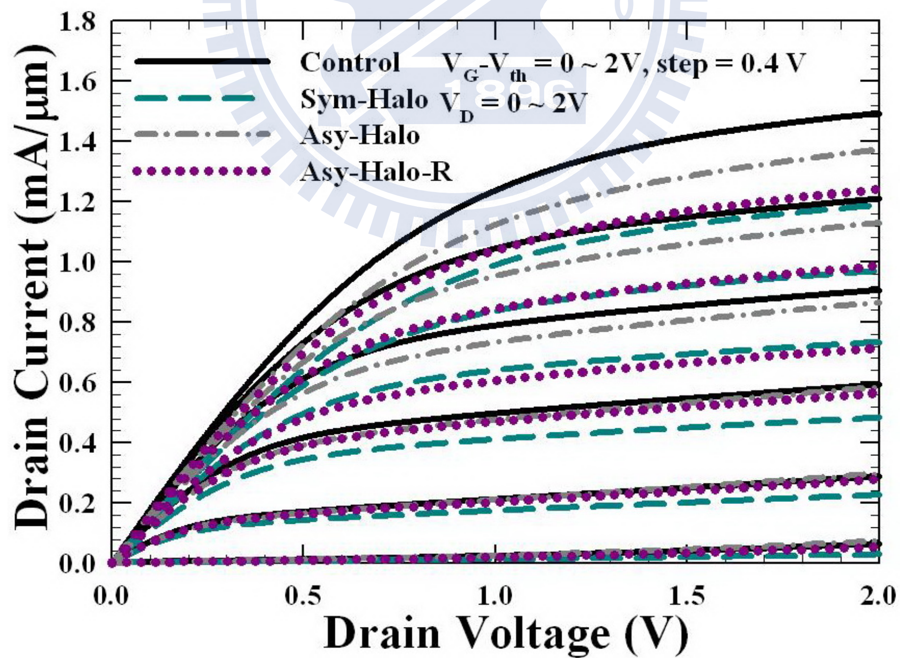


Fig. 4-20 Output characteristics of all splits measured at V_G -V_{th} = 0~2 V and step = 0.4 V with W/L = 10 μm/80 nm.

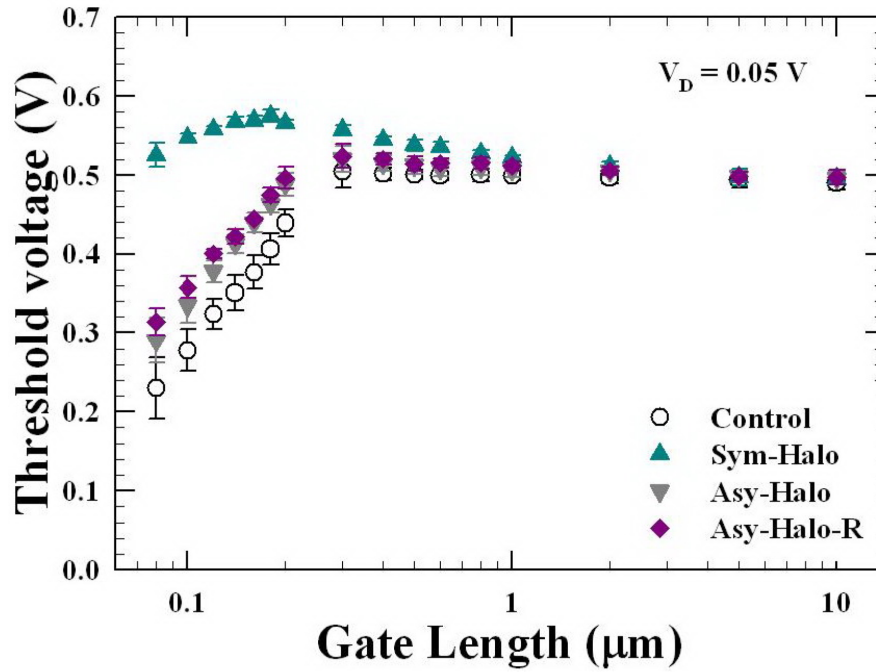


Fig. 4-21 Threshold voltage roll-off characteristics of all splits measured at $V_D = 0.05$ V with W/L = 10 μm/80 nm.

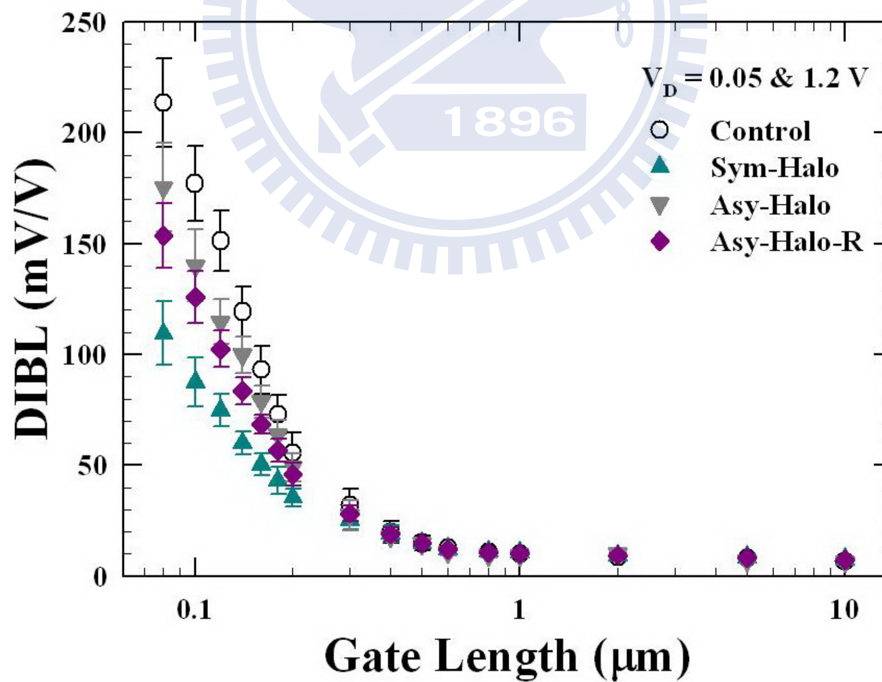


Fig. 4-22 DIBL as a function of channel length for all splits measured at $V_D = 0.05$ V with W = 10 μm.

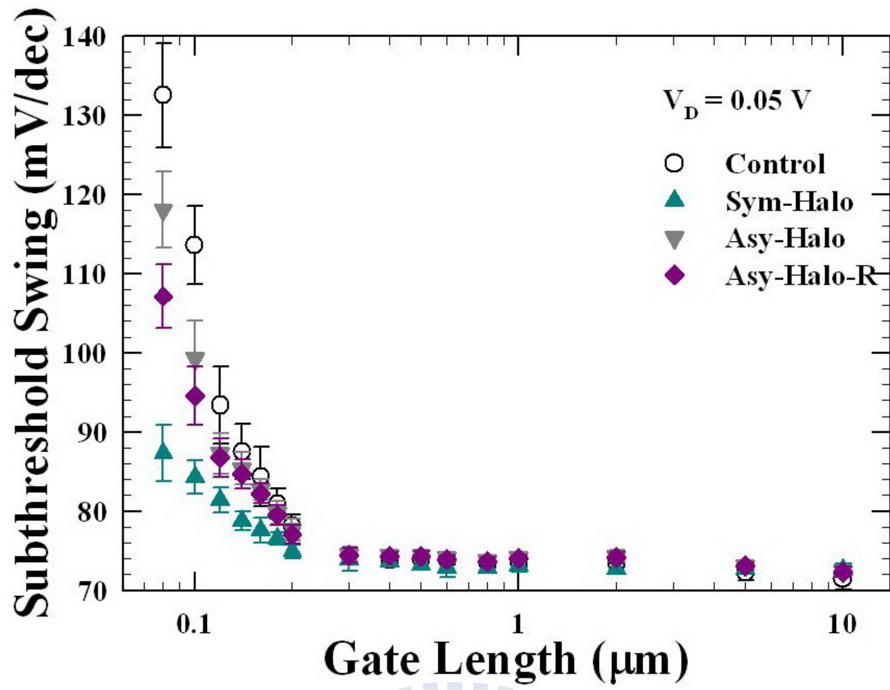


Fig. 4-23 Substreshold swing as a function of channel length for all splits measured at $V_D = 0.05$ V with W = 10 μm.

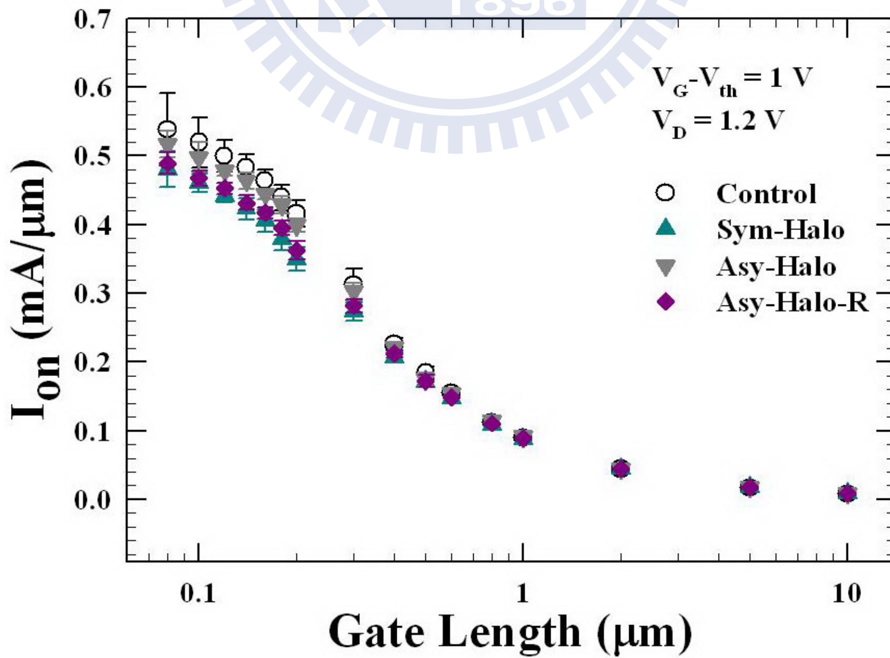


Fig. 4-24 On-current as a function of channel length for all splits measured at $V_G - V_{th} = 1$ V and $V_D = 1.2$ V with W = 10 μm.

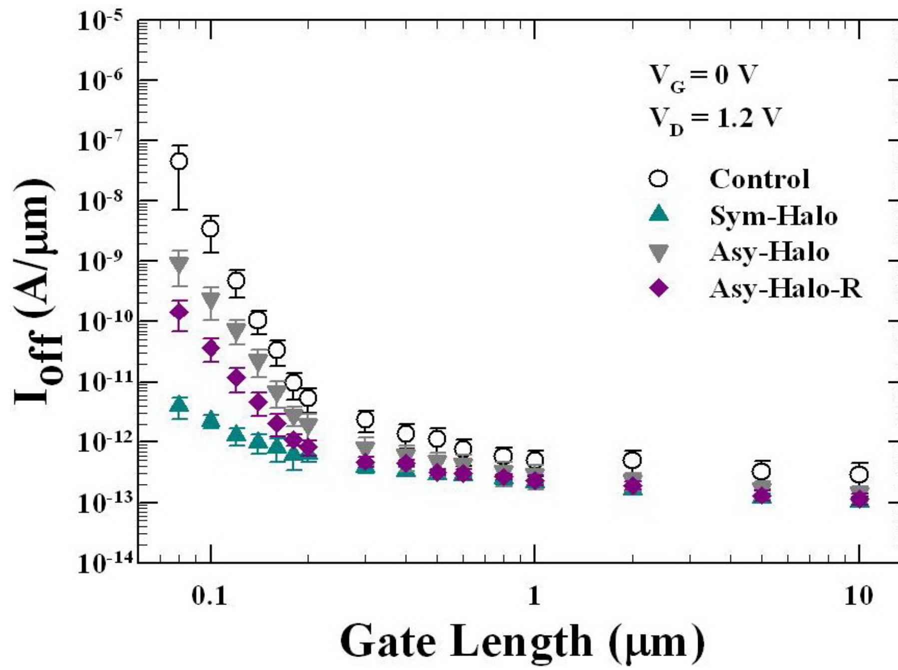


Fig. 4-25 Off-current as a function of channel length for all splits measured at $V_G = 0$ V and $V_D = 1.2$ V with W = 10 μm.

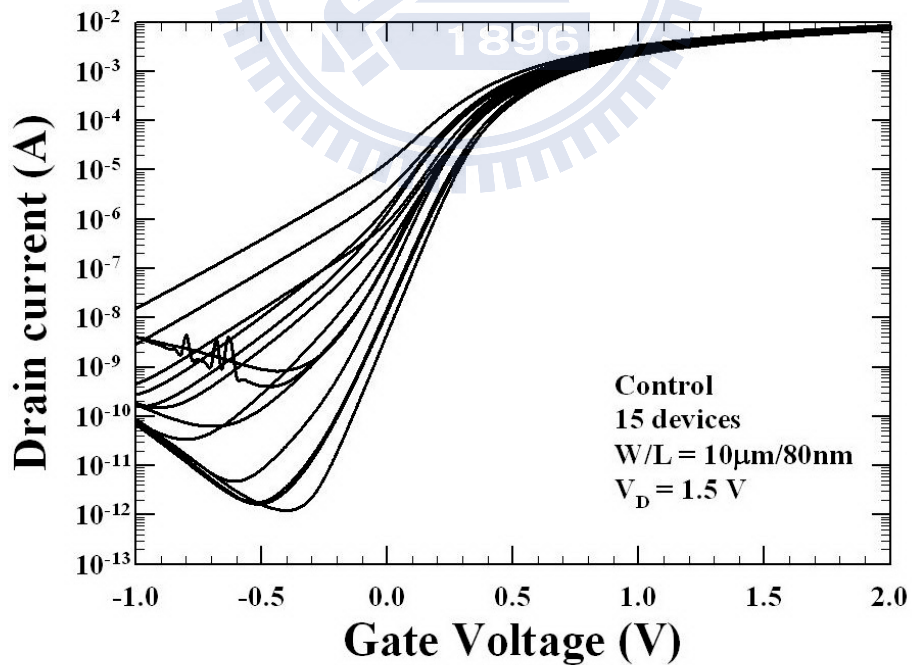


Fig. 4-26 Transfer characteristics of 15 Control nMOSFETs, with W/L = 10 μm/80 nm measured at $V_D = 1.5$ V.

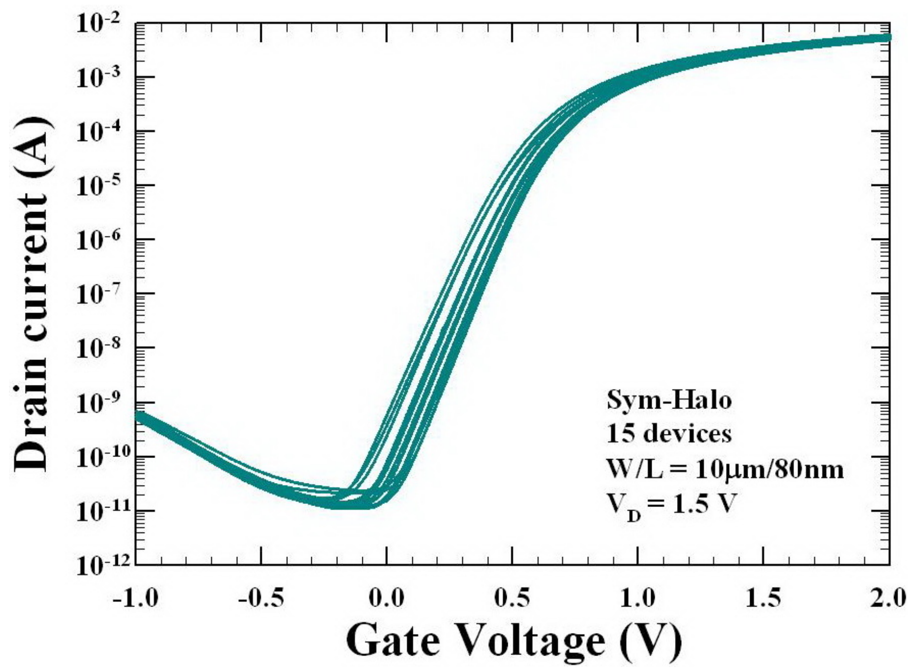


Fig. 4-27 Transfer characteristics of 15 Sym-Halo nMOSFETs, with W/L = 10 μm/80 nm measured at V_D = 1.5 V.

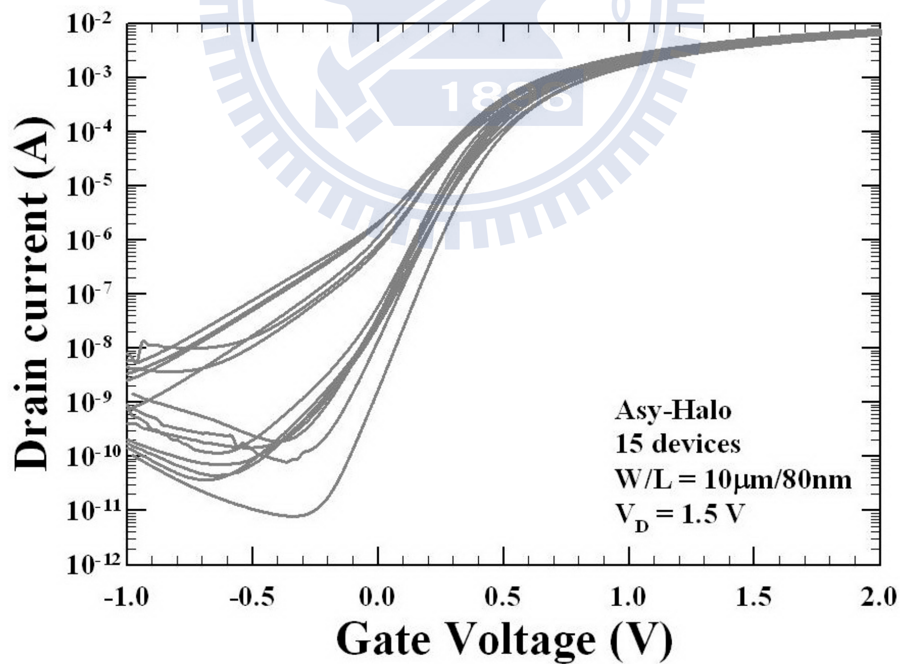


Fig. 4-28 Transfer characteristics of 15 Asy-Halo nMOSFETs, with W/L = 10 μm/80 nm measured at V_D = 1.5 V.

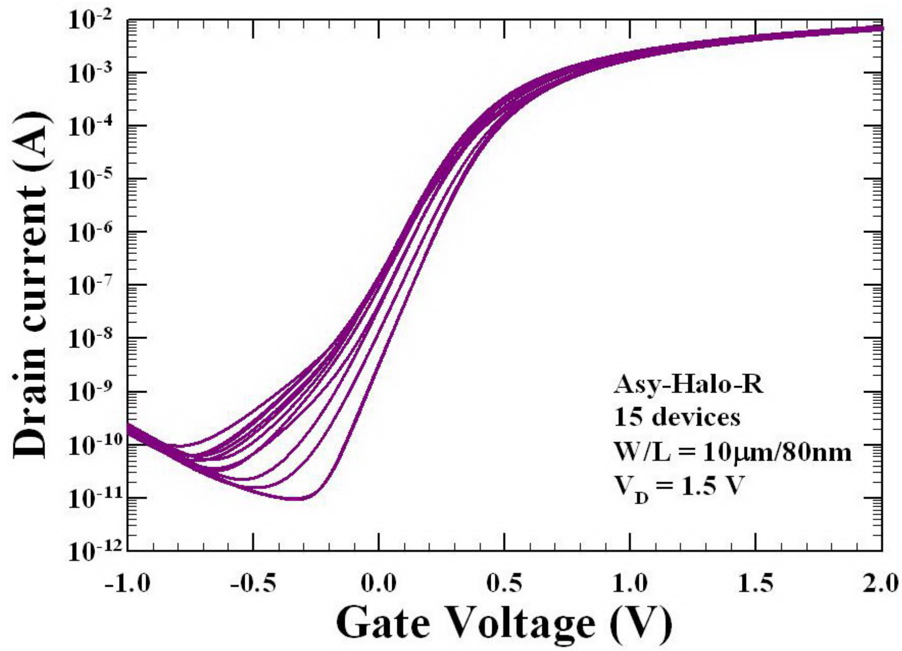


Fig. 4-29 Transfer characteristics of 15 Asy-Halo-R nMOSFETs, with W/L = 10 μm/80 nm measured at V_D = 1.5 V.

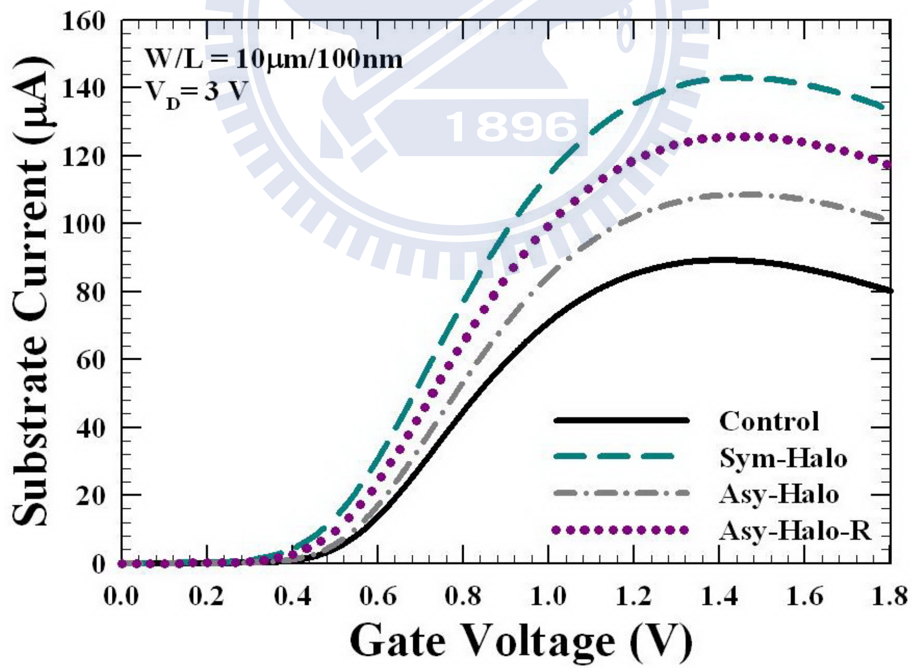


Fig. 4-30 Substrate current (I_{sub}) versus gate voltage for all splits of devices measured at V_D of 3 V with W/L = 10 μm /100 nm.

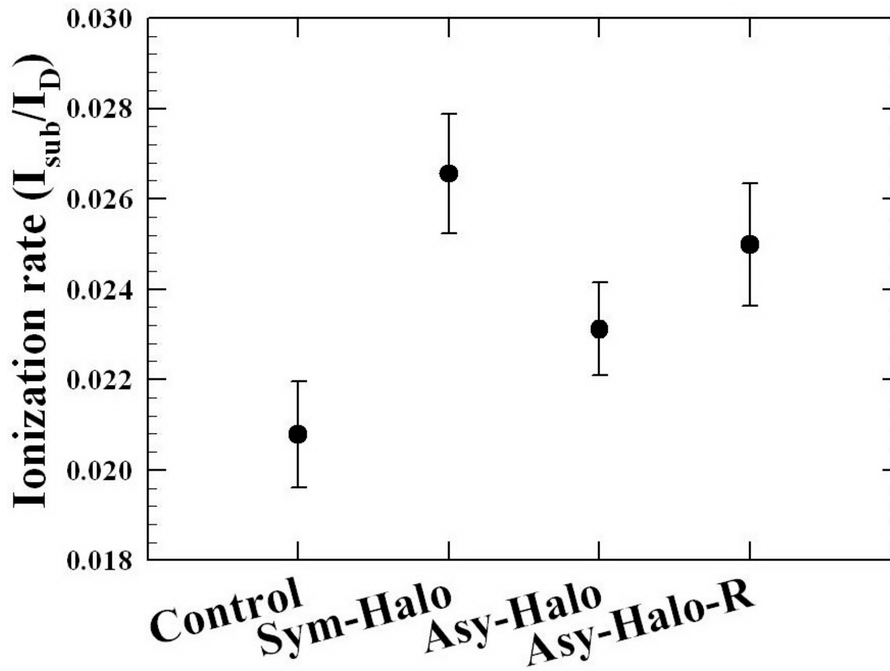


Fig. 4-31 Impact ionization rate (I_{sub}/I_D) for all splits of devices measured at V_D of 3 V with W/L = 10 μm /100 nm.

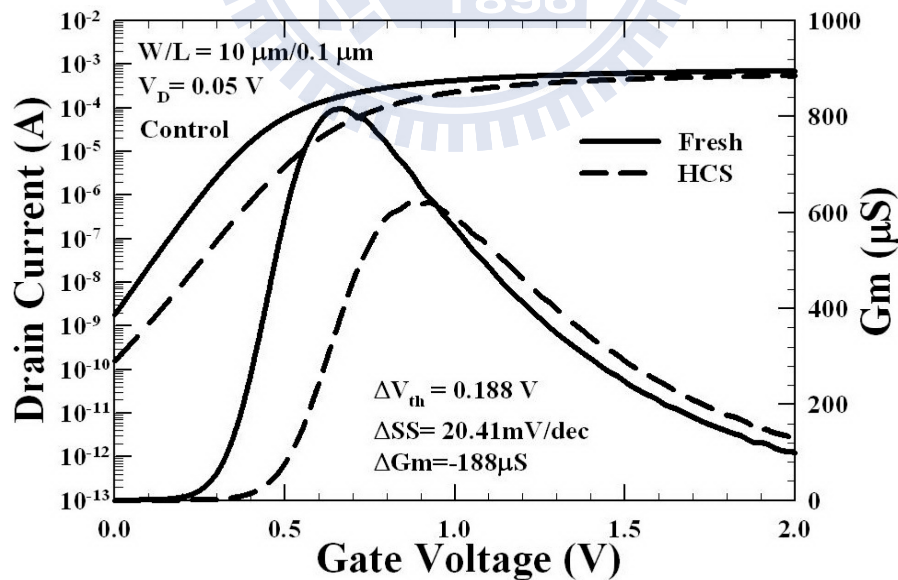


Fig. 4-32 Subthreshold characteristics and transconductance of Control device before and after 5000-second of hot-electron stressing measured at V_D of 0.05 V with W/L = 10 μm /100 nm.

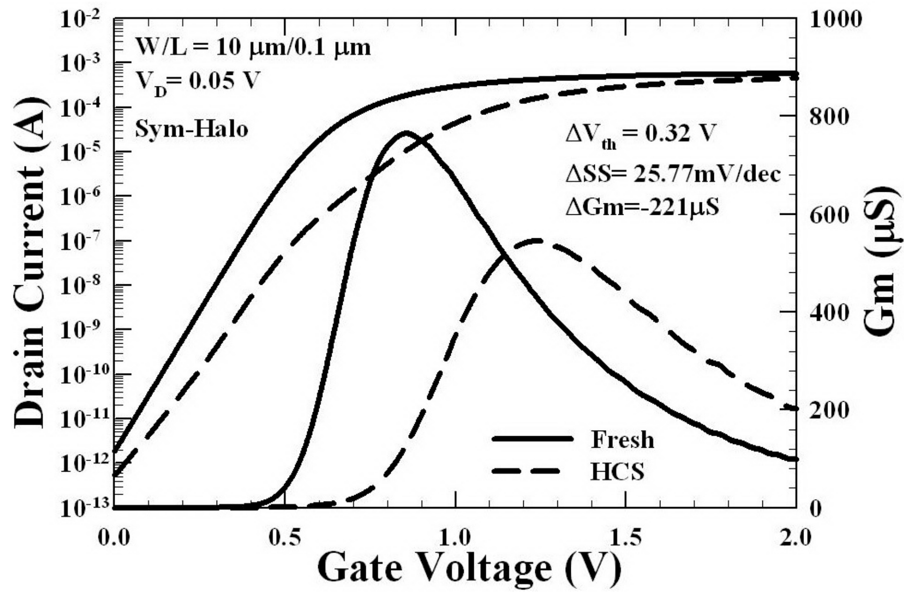


Fig. 4-33 Subthreshold characteristics and transconductance of Sym-Halo device before and after 5000-second of hot-electron stressing measured at V_D of 0.05 V with W/L = 10 μm /100 nm.

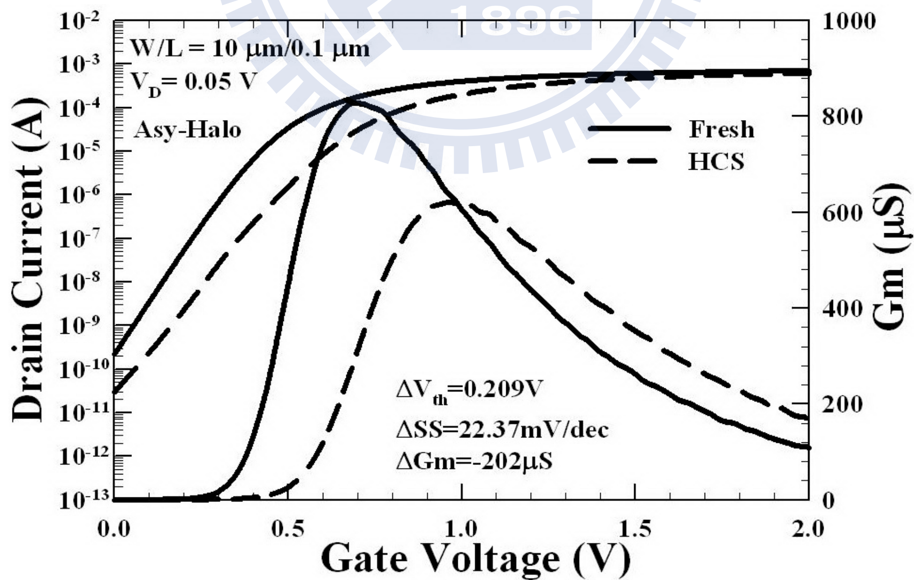


Fig. 4-34 Subthreshold characteristics and transconductance of Asy-Halo device before and after 5000-second of hot-electron stressing measured at V_D of 0.05 V with W/L = 10 μm /100 nm.

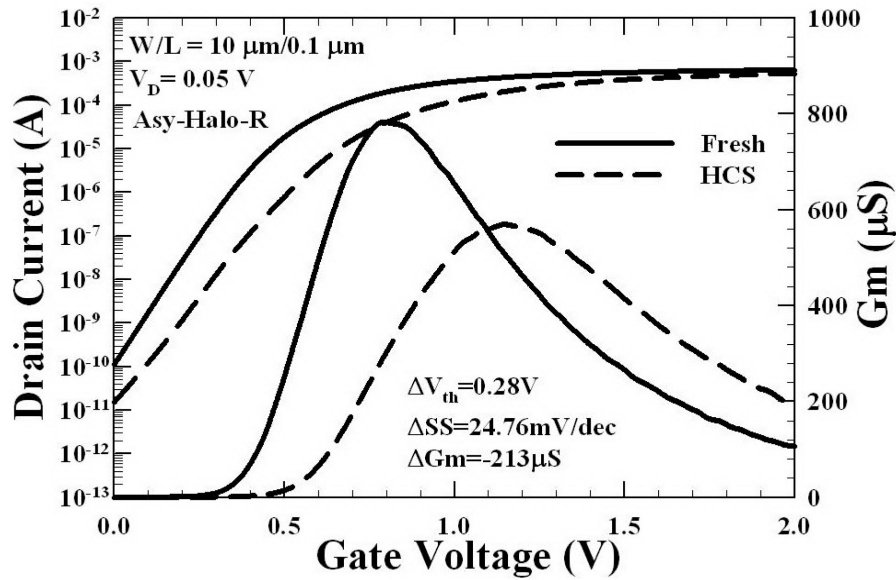


Fig. 4-35 Subthreshold characteristics and transconductance of Asy-Halo-R device before and after 5000-second of hot-electron stressing measured at V_D of 0.05 V with W/L = 10 μm /100 nm.

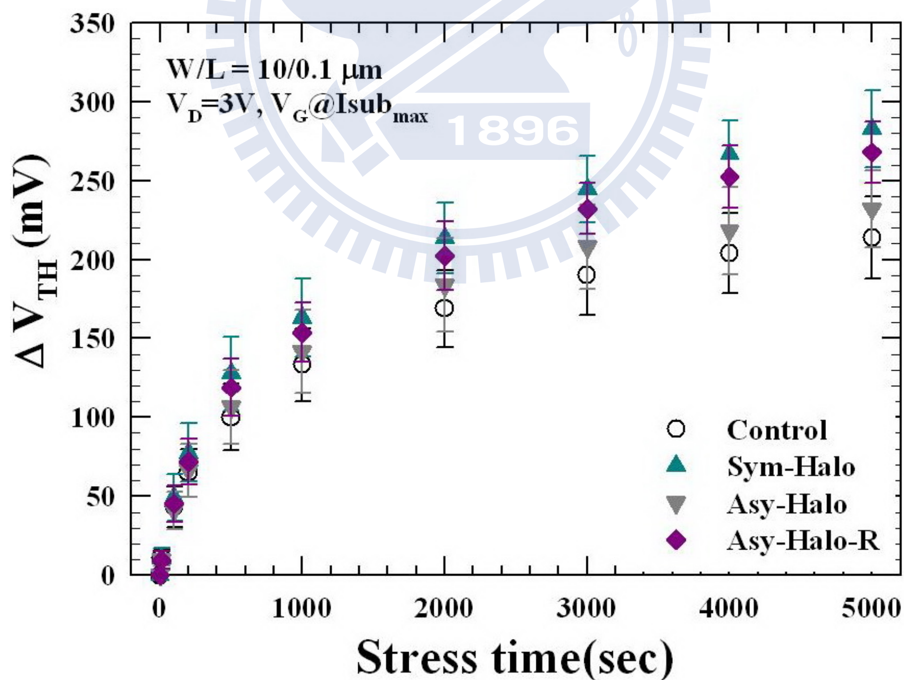


Fig. 4-36 Threshold voltage shift as a function of stress time for all splits of devices measured at V_D of 0.05 V with W/L = 10 μm /100 nm. The hot-electron stressing was performed at V_D = 3 V and V_G at maximum substrate current.

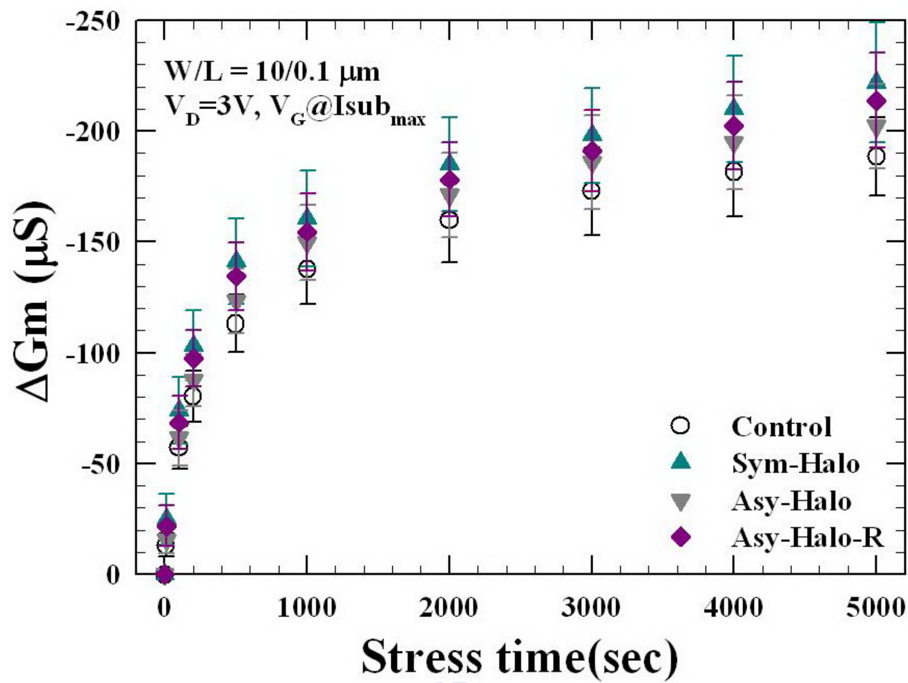


Fig. 4-37 Transconductance degradation as a function of stress time for all splits of devices measured at V_D of 0.05 V with W/L = 10 μm /100 nm. The hot-electron stressing was performed at V_D = 3 V and V_G at maximum substrate current.

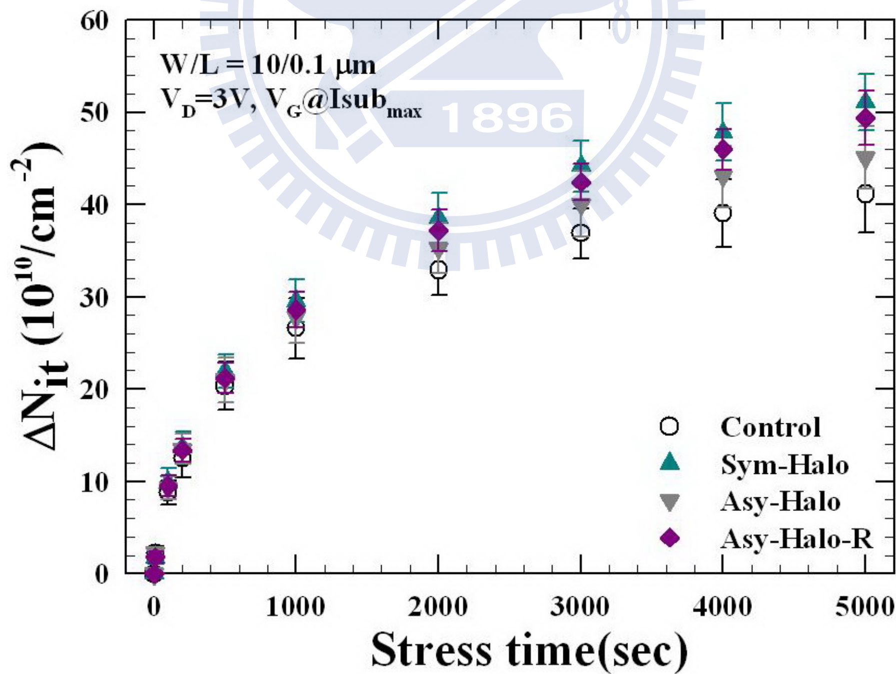


Fig. 4-38 The increase in interface state density as a function of stress time for all splits of devices measured at V_D of 0.05 V with W/L = 10 μm /100 nm. The hot-electron stressing was performed at V_D = 3 V and V_G at maximum substrate current.

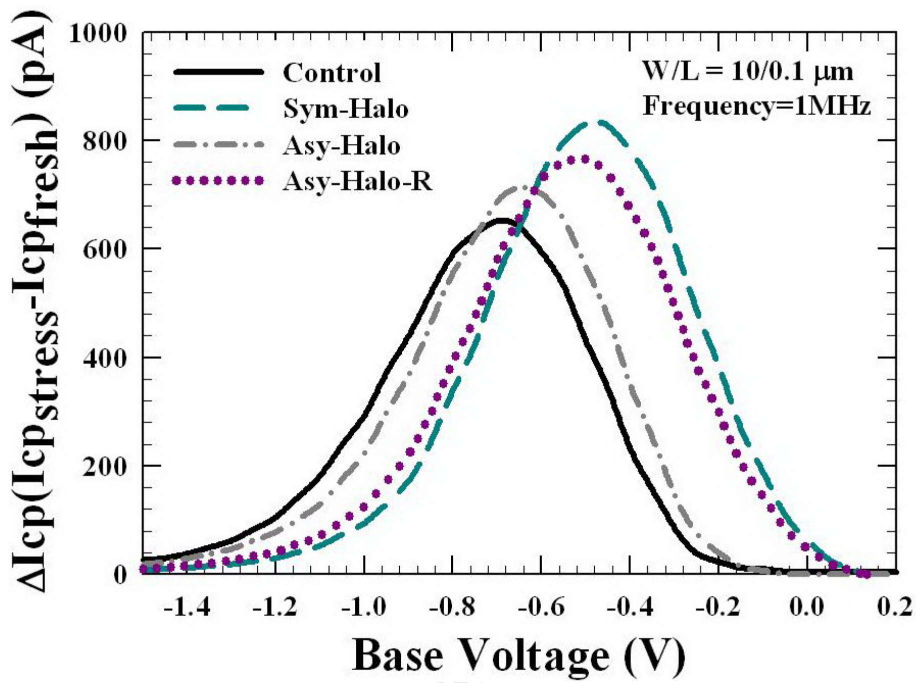


Fig. 4-39 The increase in charge pumping current after 5000-second of hot carrier stress for all splits of devices with W/L = 10 μm /100 nm. The hot-electron stressing was performed at V_D = 3 V and V_G at maximum substrate current.

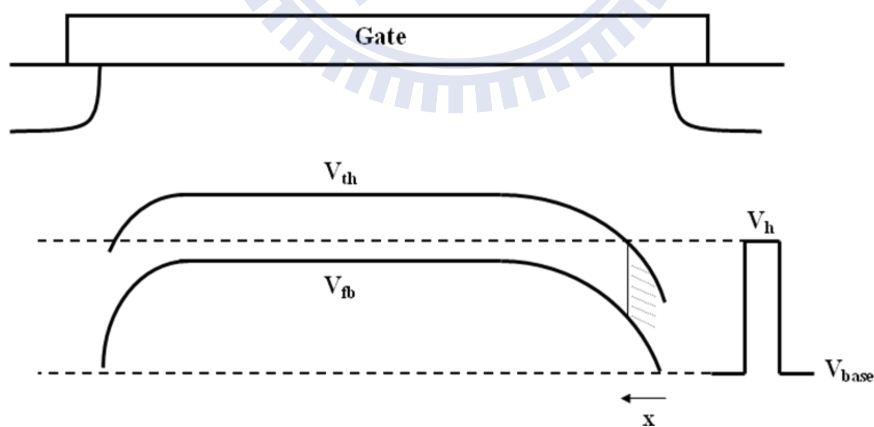


Fig. 4-40 Non-uniform distribution of local threshold voltage and flat-band voltage across the device caused by variation of lateral doping concentration. (x=0 is at the drain junction and direct to source junction)

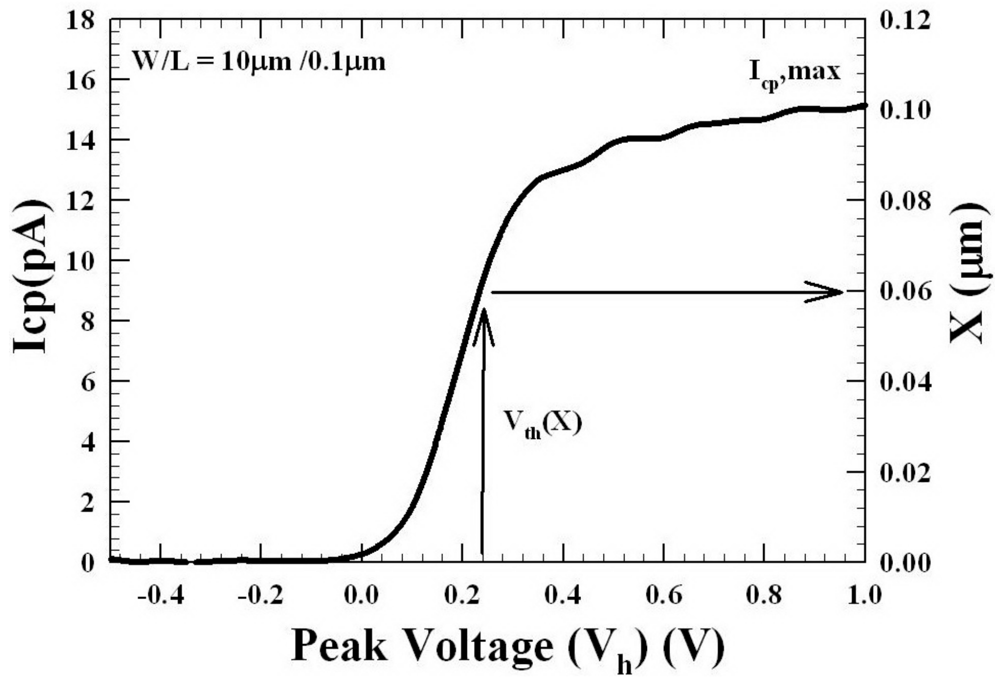


Fig. 4-41 Derivation of the relationship between local threshold voltage and lateral distance x from the single-junction charge pumping data of the control device.

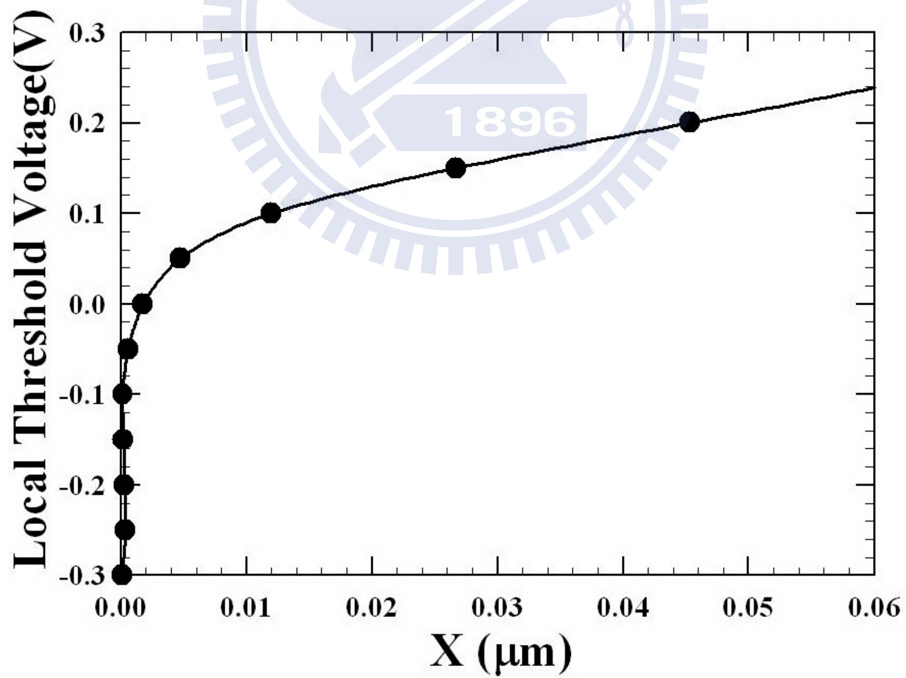


Fig. 4-42 Extracted lateral profile of local threshold voltage near the graded drain junction in the control sample.

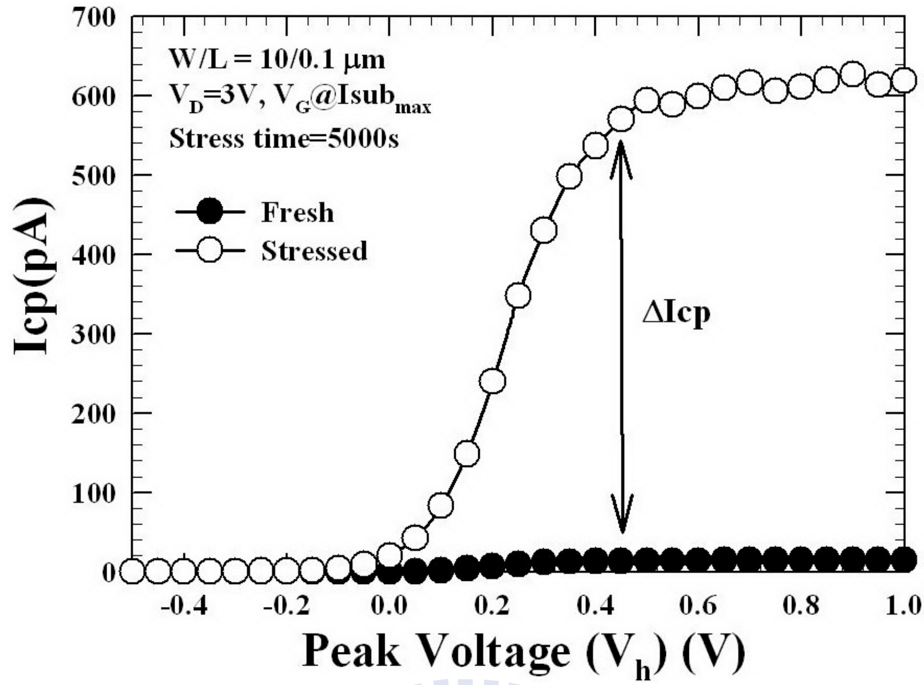


Fig. 4-43 Charge pumping current before and after 5000-second of hot-electron stressing (V_G@$Isub_{max}$ and V_D = 3 V) with W/L = 10 μm /100 nm.

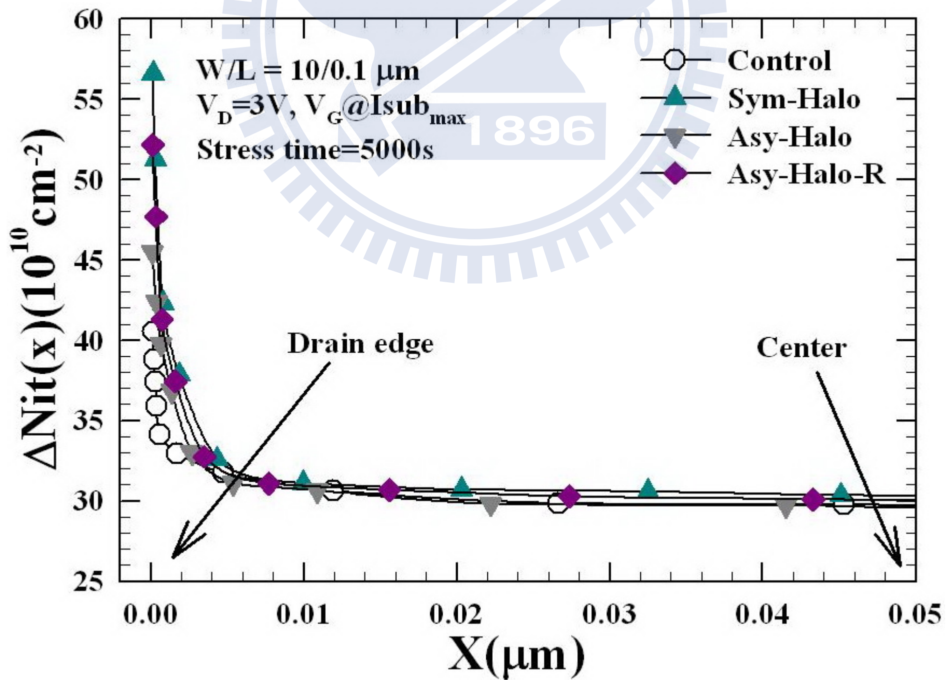


Fig. 4-44 Lateral profile of generated interface states for the four splits of devices after 5000-second of hot-electron stressing (V_G@$Isub_{max}$ and V_D = 3 V) with W/L = 10 μm /100 nm.

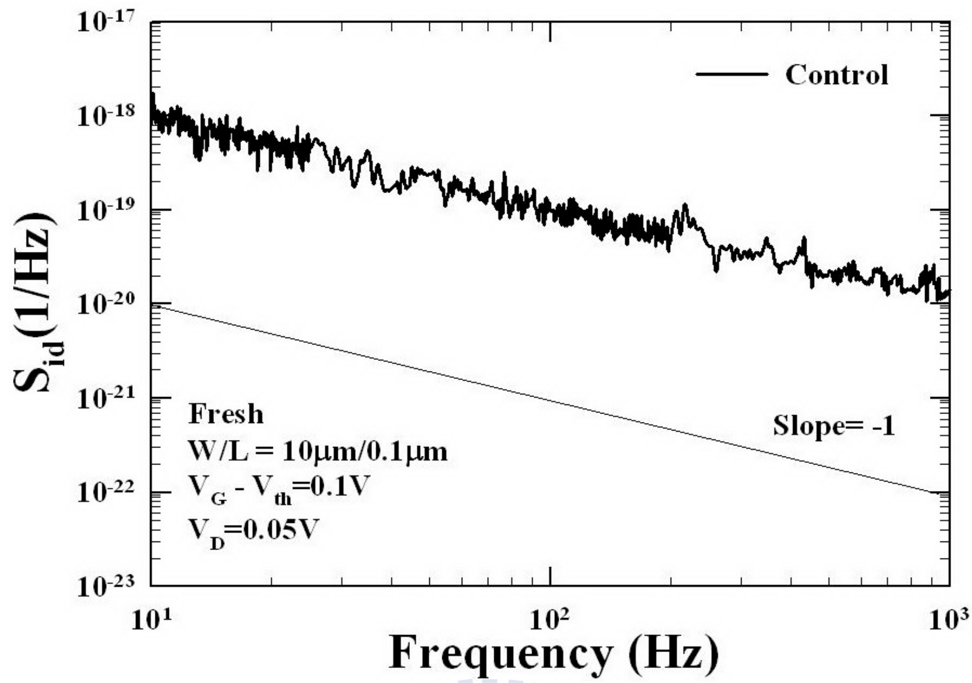


Fig. 4-45 Drain current noise spectrum density (S_{id}) of a virgin Control device measured at gate overdrive of 0.1 V ($V_G - V_{th}$ = 0.1 V) and V_D = 0.05 V with W/L = 10 μm/100 nm.

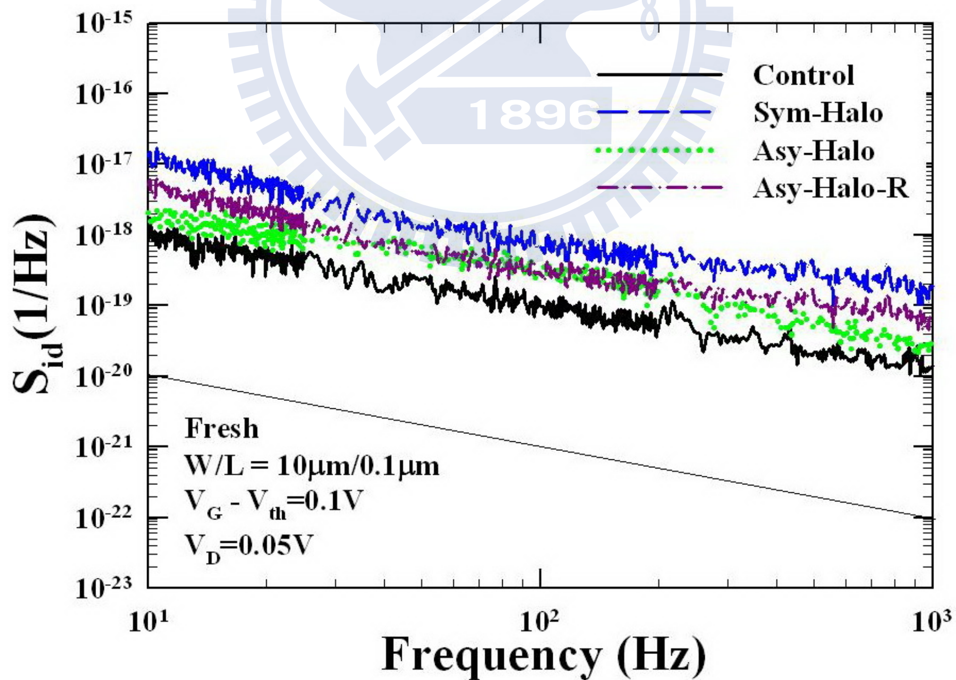


Fig. 4-46 Drain current noise spectrum density for all splits of virgin devices measured at a gate overdrive of 0.1 V ($V_G - V_{th}$ = 0.1 V) and V_D = 0.05 V with W/L = 10 μm/100 nm.

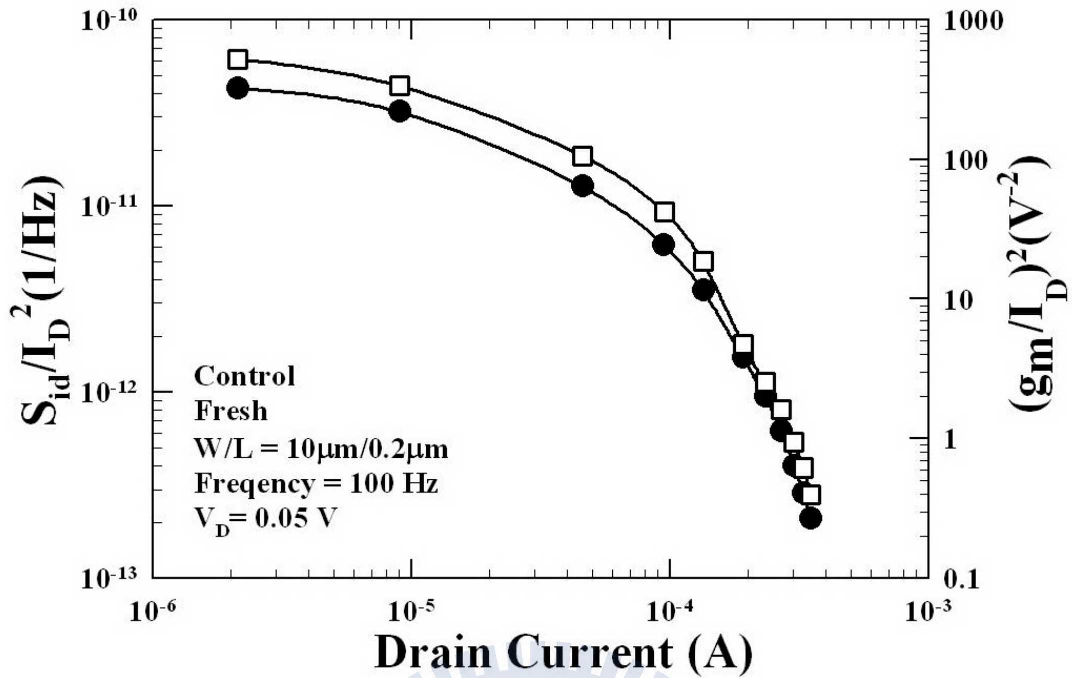


Fig. 4-47 Normalized noise power spectrum density (S_{id}/I_D^2) and $(gm/I_D)^2$ as a function of drain current for Control device with W/L = 10 μm/0.2 μm at 100 Hz.

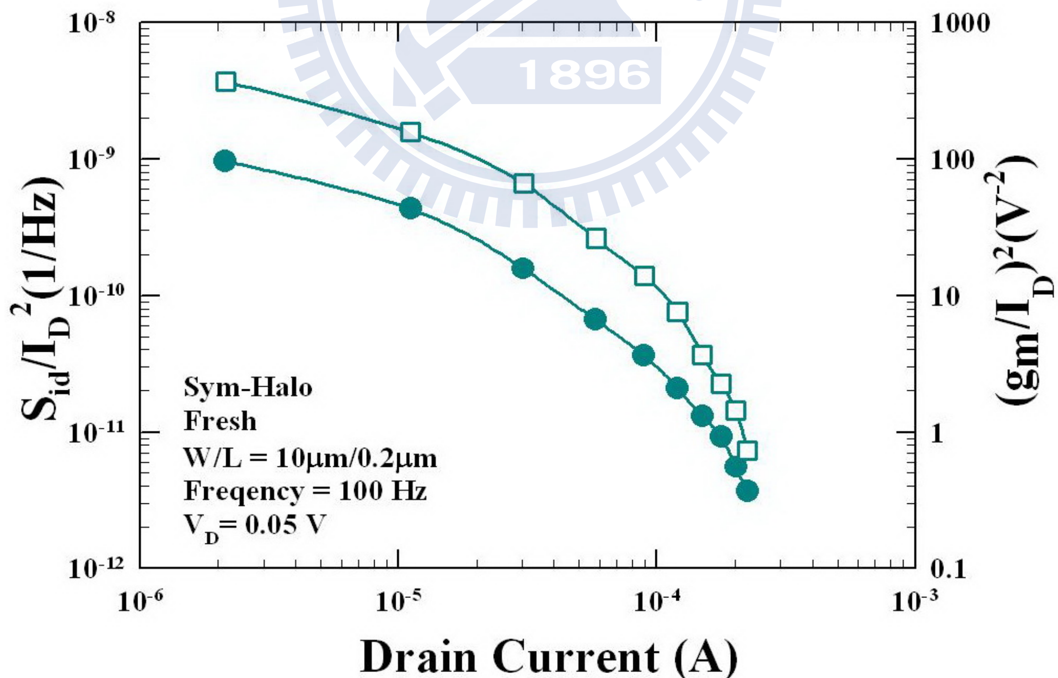


Fig. 4-48 Normalized noise power spectrum density (S_{id}/I_D^2) and $(gm/I_D)^2$ as a function of drain current for Sym-Halo device with W/L = 10 μm/0.2 μm at 100 Hz.

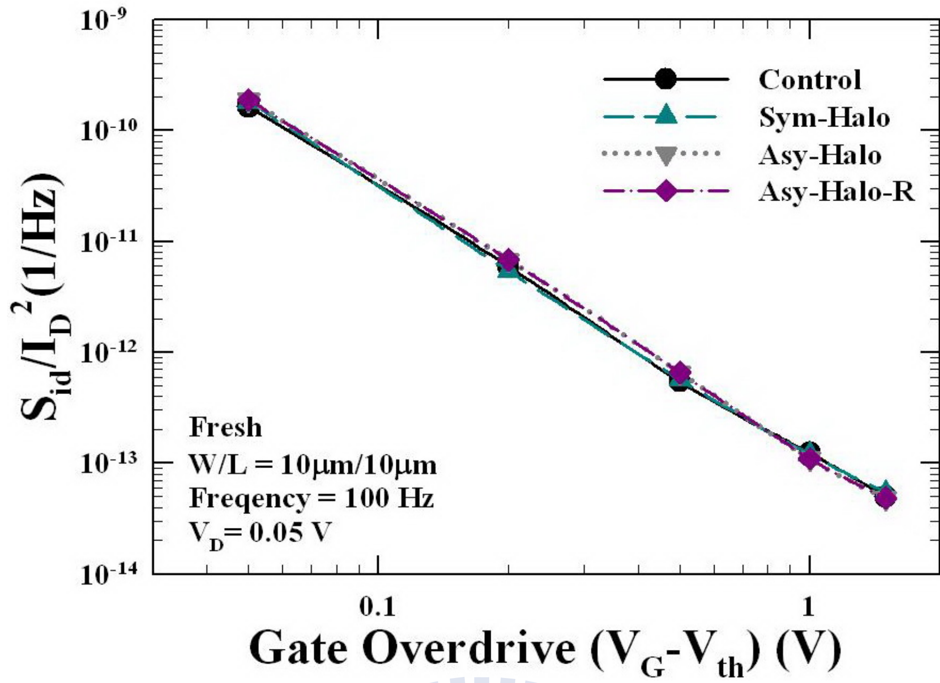


Fig. 4-49 Normalized noise power spectrum density (S_{id}/I_D^2) versus gate overdrive (V_G–V_{th}) for all splits of devices with W/L = 10 μm/10 μm at 100 Hz.

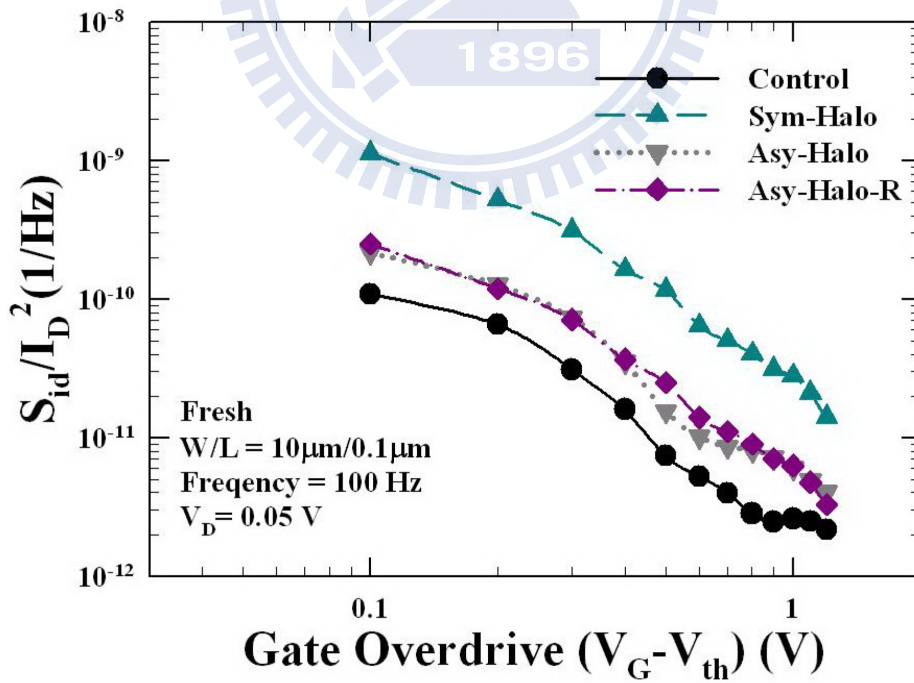


Fig. 4-50 Normalized noise power spectrum density (S_{id}/I_D^2) versus gate overdrive (V_G–V_{th}) for all splits of devices with W/L = 10 μm/0.1 μm at 100 Hz.

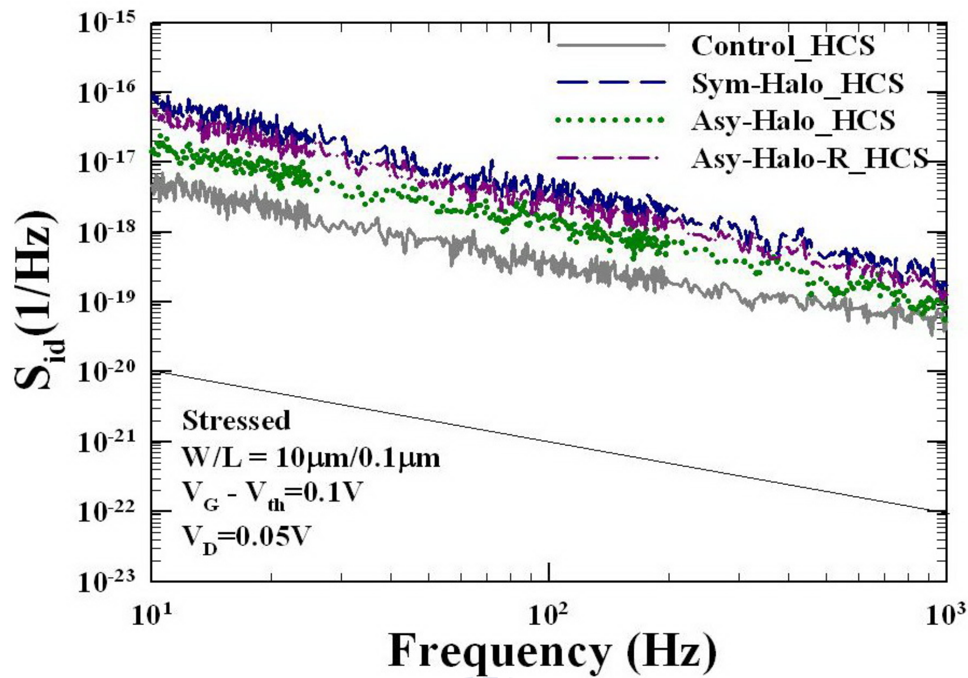


Fig. 4-51 Drain current noise spectrum density for all splits of stressed devices measured at gate overdrive of 0.1 V ($V_G - V_{th}$ = 0.1 V) and V_D = 0.05 V with W/L = 10 μm/100 nm.

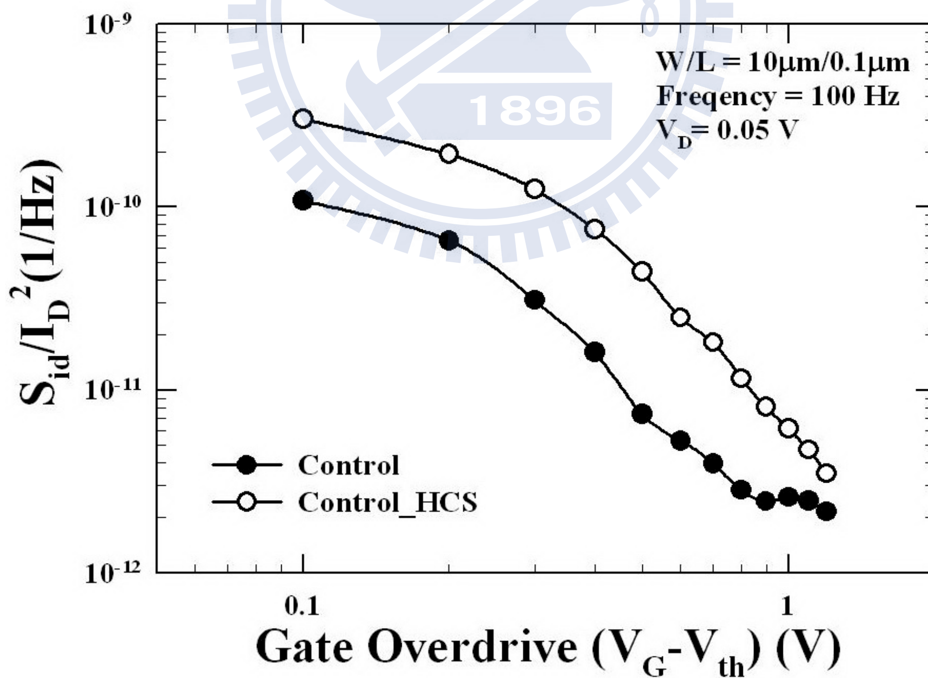


Fig. 4-52 Normalized noise power spectrum density (S_{id}/I_D^2) versus gate overdrive ($V_G - V_{th}$) before and after 5000-second of hot-electron stressing for Control device with W/L = 10 μm/0.1 μm at 100 Hz.

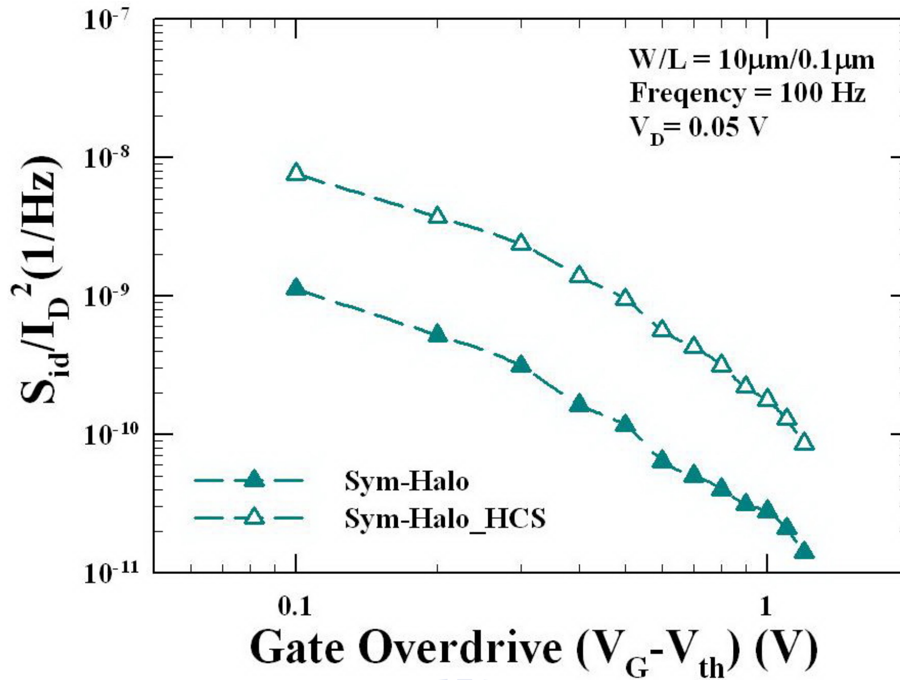


Fig. 4-53 Normalized noise power spectrum density (S_{id}/I_D^2) versus gate overdrive (V_G–V_{th}) before and after 5000-second of hot-electron stressing for Sym-Halo device with W/L = 10 μm/0.1 μm at 100 Hz.

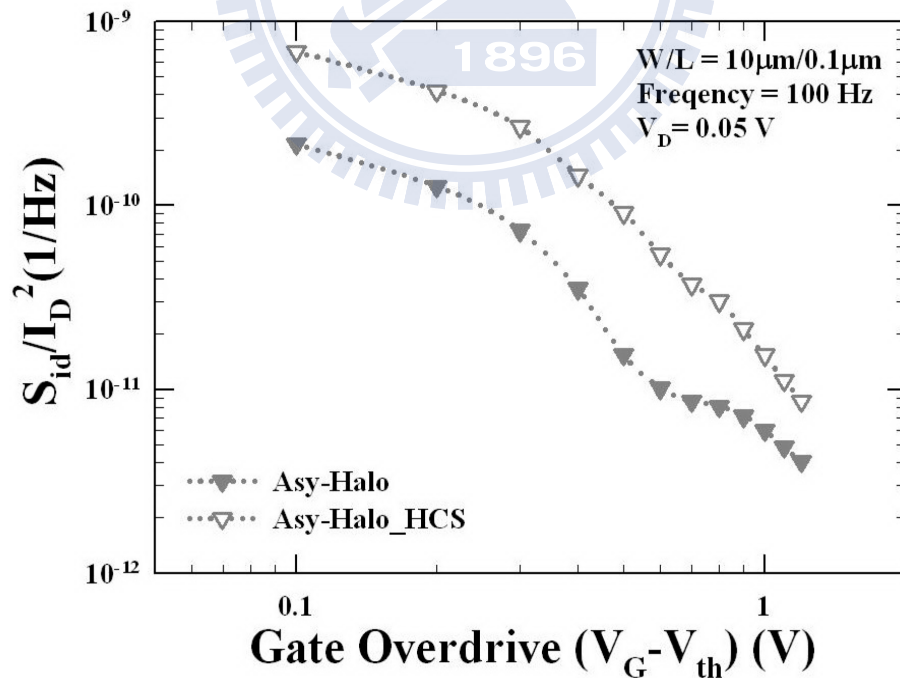


Fig. 4-54 Normalized noise power spectrum density (S_{id}/I_D^2) versus gate overdrive (V_G–V_{th}) before and after 5000-second of hot-electron stressing for Asy-Halo device with W/L = 10 μm/0.1 μm at 100 Hz.

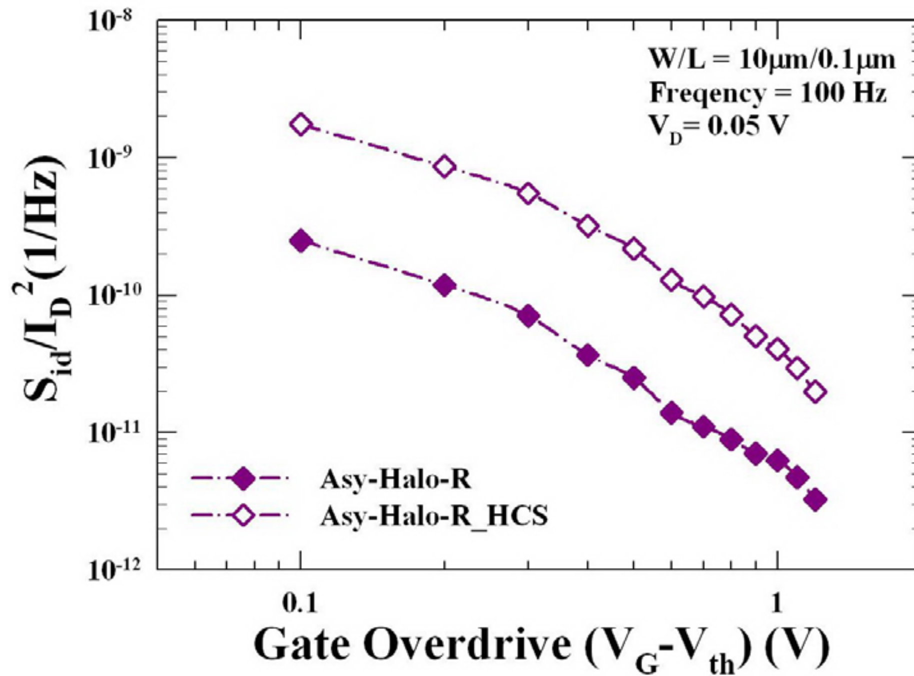


Fig. 4-55 Normalized noise power spectrum density (S_{id}/I_D^2) versus gate overdrive (V_G–V_{th}) before and after 5000-second of hot-electron stressing for Asy-Halo-R device with W/L = 10 μm/0.1 μm at 100 Hz.

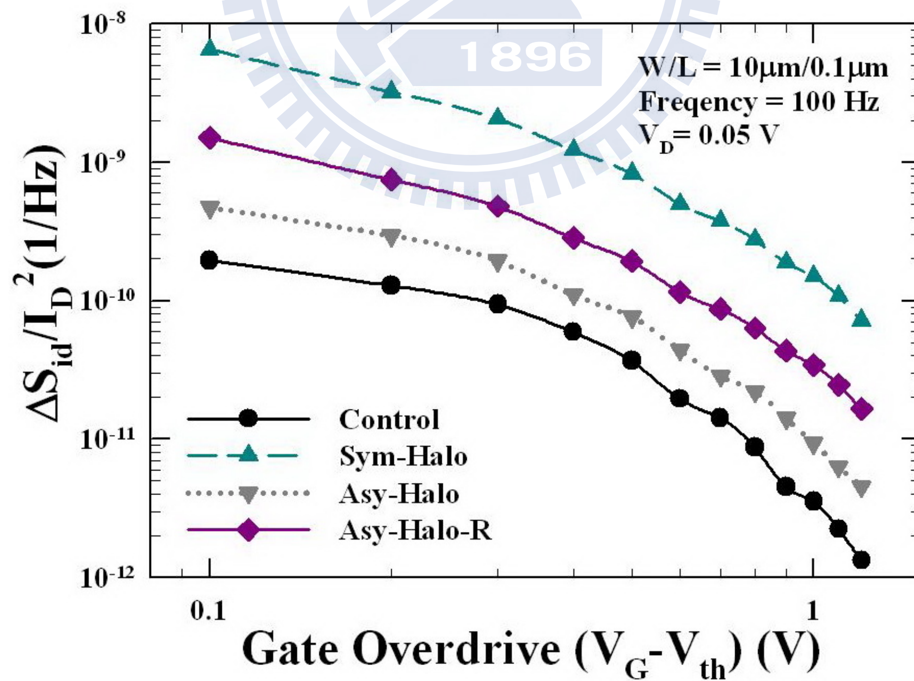


Fig. 4-56 The increase in normalized noise power spectrum density ($\Delta S_{id}/I_D^2$) versus gate overdrive (V_G–V_{th}) after 5000-second of hot-electron stressing for all splits of devices with W/L = 10 μm/0.1 μm at 100 Hz.

Chapter 5

Fabrication and Characterization of Junctionless Polycrystalline Silicon Thin-Film Transistors Using an Implant-free Technique

5.1 Introduction

In order to keep pace with the Moore's Law, aggressively downscaling the dimension of the semiconductor devices is necessary to not only increase the speed and density of transistors on an integrated circuit, but also make manufacturing cost cheaper. However, two p-n junctions, the source/drain (S/D)-to-channel junctions, inherently existed in the conventional planar bulk MOSFET structure with the extremely high doping concentration gradients of S/D regions result in the fluctuation of diffusing impurities for the nano-scale devices [1]. Concurrently, the precise control on junction doping profiles of S/D regions becomes extremely challenging in nanoscale regimes. In line with this, junctionless (JL) devices have been proposed to cope with the doping profile issue [2-4]. In a JL structure, the dopant type and concentration are the same all the way from the source, channel to drain. Since no conventional p-n junctions are formed in it, the JL scheme can relieve the precise formation technique of the ultra-shallow or ultra-abrupt junction, thus simplifying the fabrication process.

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have become very attractive for future 3-D electronics integration due to the low deposition temperature and mature fabrication processes [5-6]. Lately, the adoption of nanowires (NWs) as the channel in TFTs has demonstrated superior performance thanks to their small volume and the accompanying reduction in defects [7-8]. Therefore, numerous researches focusing on NW-based devices especially with multiple-gated (MG) structure have been widely explored [9-12]. The NW device demonstrates enhanced current drivability and steep subthreshold slope (SS), as well as good immunity to short-channel effects because the MG configuration can effectively control the electrostatic potential in the tiny volume and high surface-to-volume ratio NW channel, so that the channel suffers

from less electrical interference from the drain [9, 11]. Thus the MG field-effect transistor (FET) with NW channel is considered as one of the promising device architectures for next-generation nanoscale devices. In this chapter, we present an NWFET with gate-all-around (GAA) configuration using one *in situ* doped poly-Si layer to form source, NW channel, and drain regions without additional implantation procedure to implement the JL technique.

On the other hand, with the proliferation of portable electronic products, the demand of high density nonvolatile memories (NVMs) has increased dramatically. Two types of NVMs have been developed, namely, the floating gate (FG) device and the charge-trapping (CT) device. The former has governed the NVM market for decades, but FG device suffers from fatal data loss through a single defect in the tunnel oxide [13] and more challenges in device downscaling due to the FG coupling issue [14]. Recently, CT devices, such as silicon-oxide-nitride-oxide-silicon (SONOS) [15] and its various branches [16-18], have emerged as one of potential candidates for replacing the FG devices as the next generation NVMs owing to its inherent immunity to gate-coupling issue and more tolerance to the defects in the thin tunnel oxide. Besides, thinner gate stacks in SONOS devices facilitate stronger electrostatic control, and therefore make SONOS devices relieve of device scaling. Furthermore, poly-Si TFT-SONOS memories have attracted much attention for the purposes of the low-cost and low-temperature fabrication processes, inherent compatibility with system-on-panel (SoP) or system-on-chip integration [6], and ultrahigh memory cells density accomplished by 3-D multilayer stack architecture [19, 20]. However, there are still some challenges in poly-Si TFT-based memory devices to be addressed such as slow memory operation speed and poor SS ascribed to the inherent grain boundaries and accompanying defects in poly-Si films. Fortunately, the implementation of NW channel with MG configuration in TFTs has been demonstrated to improve the aforementioned shortcomings, ascribed to superior gate controllability and reduced defects in their tiny volume of NW channels [12]. In this chapter, we demonstrate the feasibility of JL scheme through the implementation of SONOS flash memory device fabricated with MG configuration and NW channels for the sake of simplifying the process complexity and boosting the programming efficiency by virtue of inherently abundant carriers in JL NW channels.

In addition, with the thriving in portable electronics, wireless transmission among electronics equipment doubtlessly prevails throughout our daily life. By properly

downscaling the dimensions of TFTs, the radio-frequency (RF) performances of TFTs are expected to improve significantly and become feasible for RF applications. For example, it could be integrated into a cell phone which is capable of doing transaction by electric wallet or RF identification (RFID) [21]. Furthermore, the operating frequency of LTPS TFT has exceeded to over gigahertz and the feasibility of related RF integrated circuits (ICs) has been investigated as well [22]. In the last section of this chapter, we explore the feasibility of JL scheme utilizing planar poly-Si TFT technique for RF applications, and further, both the small-signal modeling of the fabricated TFTs and the related parameters are characterized as well.

5.2 Device Fabrication and Experiment

5.2-1 Junctionless NWFETs

Figure 5-1 briefly illustrates the key fabrication process flow of the proposed GAA JL NWFET. First, a sandwich stack of nitride/tetraethyl orthosilicate (TEOS) oxide/nitride layers was sequentially deposited and then patterned on a six-inch silicon substrate capped with a 200-nm-thick thermally grown oxide. Next, the formation of sub-100-nm cavities underneath both sides of the top nitride was implemented by selective lateral etching of the TEOS oxide layer using diluted hydrofluoric (HF) solution ($HF:H_2O$ = 1:100) as shown in Fig. 5-1 (a). The tilted scanning electron microscopic (SEM) images before and after cavity formation are illustrated in Fig. 5-2. An indistinct cavity was formed after 20-second etching time. In contrast with 20-second etching time, with 60-second etching time, a distinguished shape of cavity was formed and served as the mold for the formation of NW channels. An *in situ* phosphorus-doped poly-Si layer was then deposited using SiH_4 of 0.49 slm and PH_3 of 15 sccm in the low-pressure chemical vapor deposition (LPCVD) system at 550 ^{o}C and 600 mtorr onto the nano-cavity [Fig. 5-1 (b)]. The doped poly-Si film was then patterned and etched in a transformer-coupled plasma reactor using Cl_2/HBr gases to define NW doped channels (denoted as JL) and S/D regions simultaneously for the purpose of realizing the structure without junctions (*i.e.*, n^+-n^+-n^+), as illustrated in Fig. 5-1 (c). Note that the conventional inversion-mode (IM) counterparts (*i.e.*, n^+-i-n^+) were also processed along with a similar flow but using an undoped poly-Si film as the channel (denoted as IM), while the S/D regions were formed with the same *in situ* phosphorus-doped poly-Si layer as in the JL devices. In addition, the *in situ* doping

process was chosen to yield a uniform resistivity distribution of around 2.7 mΩ·cm on a six-inch wafer and has good reproducibility, and further, has been commonly employed as the material of gate electrode. To fulfill the GAA structure, the sandwich stack comprising nitride/TEOS oxide/nitride layers was sequentially removed by wet-etching process in order to suspend the NW channels, as depicted in Fig. 5-3 with various sizes of NWs. As can be seen in the plots recorded by in-line SEM, different sized NW channels, including tiny, mid-sized and large-sized NWs, were exposed before the gate stack formation. Afterwards, the high-κ/metal gate stack structure was formed by using an atomic-layer deposition (ALD) system to deposit 10-nm-thick Al_2O_3 and 10-nm-thick TiN films conformally onto the NW channel, as shown in Fig. 5-1 (d). Note that the final thickness of the TiN gate electrode is 150 nm by sputtering another 140-nm-thick TiN film. Some wafers skipping the deposition of Al_2O_3, adopted the LPCVD TEOS oxide as gate dielectric layer. After the definition of gate electrode, the deposition of PECVD TEOS passivation layer and AlSiCu metallization procedure, the fabrication of JL and IM NW devices were accomplished, as illustrated in Fig. 5-1 (e). Figure 5-1 (f) shows the schematic top-view layout, indicating the location of NW channels.

Figure 5-4 depicts the cross-sectional high-resolution transmission electron microscopic (HRTEM) image of a fabricated GAA JL NWFET with the TEOS oxide/TiN gate stack, and an NW size of around 12 nm in thickness (T) and 23 nm in width (W). Here we performed the fast Fourier transform technique on the HRTEM image to acquire diffraction pattern revealed in the inset, indicating that the monocrystalline structure of the Si grain with [110] orientation. According to Wada's work [23], poly-Si with higher n-type doping concentration exhibits larger grain size. Therefore, the fabrication of poly-Si NWFETs would benefit by the adoption of an n^+-poly-Si material with the enhanced crystallinity, inferring that it is one merit of JL scheme. The cross-sectional TEM images of fabricated GAA JL NWFETs with the Al_2O_3/TiN gate stack structure and three different sizes of NW channels are shown in Fig. 5-5. As can be seen in these images, the smallest one is around 10 nm in thickness and 15 nm in width, while other larger NWs are 75 nm × 30 nm denoted as mid-sized JL and 152 nm × 74 nm denoted as large-sized JL, respectively. In addition, Hall measurements were performed on a blanket *in situ* doped poly-Si thin film of 300 nm with two kinds of PH_3 flow rates, as recorded in Table 5-1. It should be noted that the

nominal doping concentrations are 6×10^{20} cm^{-3} and 1×10^{20} cm^{-3} for the n^+-poly-Si gate and the NW channels, respectively. However, the practical active carrier concentration in the NW channels of the fabricated devices would be much lower than the result of Hall measurements. According to a report by Fred Lacy [24], the electrical resistivity of a thin film will increase as the dimensions of the film become sufficiently small owing to the reduced mean free path of conduction carriers. On the other hand, the effects of donor deactivation and phosphorous segregation occurring in the NW channel are other culprits of lower carrier concentration [25, 26].

5.2-2 Junctionless SONOS Nonvolatile memory Devices

The process flow of poly-Si NW SONOS memory device with JL scheme is similar to that of the previously described JL GAA NWFET, and is illustrated in Fig. 5-6. Here we describe some key process parameters in this section. A 100-nm-thick *in situ* phosphorous doped poly-Si layer, which was carried out using mixed gases of SiH_4 and PH_3, was adopted as the channel material of the JL structure (*i.e.*, n^+-n^+-n^+), as shown in Fig 5-6 (c). The doping concentration can be varied by simply adjusting the PH_3 flow rate such as 15 sccm for lighter doping and 30 sccm for heavier doping, while keeping the same SiH_4 flow rate of 0.49 slm. To implement the GAA configuration, the top-nitride/bottom-nitride and TEOS oxide layers were removed by hot H_3PO_4 and HF solution, respectively, to expose the NW channels, as depicted in Fig. 5-6 (d). To fulfill the SONOS structure, a gate dielectric stack of blocking oxide/trapping nitride/tunneling oxide (ONO) with thicknesses of 12/7/3 nm was deposited by LPCVD, as illustrated in Fig. 5-6 (e). In comparison, conventional IM memory devices (*i.e.*, n^+-i-n^+) with undoped poly-Si NW channels having the same ONO stack were also fabricated. Afterwards, an *in situ* phosphorous doped n^+-poly-Si layer was deposited using SiH_4 of 0.49 slm and PH_3 of 100 sccm by LPCVD and then patterned to serve as the gate electrode, as shown in Fig. 5-6 (f). On the other hand, the omega-shaped gate (Ω-gate) configuration was fabricated as well by retaining a portion of the bottom-nitride during the removal of the sandwich stack comprising nitride/TEOS oxide/nitride layers. Figure 5-7 illustrates two schematic gate structures (GAA/Ω-gate) implemented in our JL-SONOS memory cells for better comprehension.

Figure 5-8 (a) shows the top-view SEM image of a fabricated JL NW memory device and the channel length is defined as the spacing between the S/D regions. The cross-sectional TEM image of the NW channel with GAA structure is shown in Fig. 5-8

(b) and the dimension of NW is about 11 nm × 6 nm, apparently enclosed by the ONO gate stack and poly-Si gate. According to our original process design of nano-cavity formation, the cross section of the poly-Si NWs is supposed to be rectangular in shape. Nonetheless the observed NW exhibits a nearly elliptic profile. Because our NW channels experienced a series of wafer cleaning and etching steps proceeded in chemical solutions through device fabrication, the NW's corners were rounded, eventually leading to an elliptic shape. In contrast with the GAA configuration, the cross-sectional TEM image of NW channel with Ω-gate structure is shown in Fig. 5-8 (c), indicating that the cross section of the NW is about 12 nm × 6.5 nm. For the purpose of better understanding in discussing device characterization, the splits of fabricated JL SONOS memory cells are listed in Table 5-2. Note that the NW memory devices with channel length of 0.4 μm were used for the analyses of both electrical and memory characteristics.

5.2-3 Three-Dimensional Multilayer-Stacked Junctionless NWFETs

The Illustration of the key steps for building three-dimensional (3-D) multilayer stacked JL poly-Si NW device, similar to that of the previously described JL GAA NWFET, is displayed in Fig. 5-9. Here we describe some key process parameters in this section. The sequential depositions of 3-level nitride (SiN)/TEOS oxide stacked layers were implemented to accomplish 3-D structure, totally comprising one 100-nm-thick bottom-SiN/three 30-nm-thick sandwiched TEOS oxide/two 60-nm-thick sandwiched SiN/one 110-nm-thick top-SiN layers. After lithographic and anisotropic etching steps, a 3-level stacked dummy pattern was formed, followed by the formation of six nano-cavities underneath the sandwiched SiN layers by carefully-controlled lateral-etching of the TEOS oxide layers in a dilute HF solution as shown in Fig. 5-9 (a). Here we performed anisotropic etching process in a transformer-coupled plasma (TCP) reactor using CF_4 of 100 sccm, Ar of 50 sccm, and pressure set to 4.9 mtorr at RF power of 320 W for top electrode and 150 W for bottom electrode, to define 3-level multilayer-stacked dummy pattern. Figure 5-10 depicts the tilted SME images of anisotropic-etching dummy patterns, indicating that TCP reactor facilitates an abrupt etching profile. The overhead-view SEM images of the nano-cavities with 30- and 40-second lateral-etching time are depicted in Fig. 5-11, and both conditions exhibit obvious cavities between these sandwiched SiN layers. Afterwards, deposition of an *in situ* phosphorous-doped n^+-poly-Si layer as NW channels and S/D regions (denoted as

3-level JL) was executed using SiH_4 of 0.49 slm and PH_3 of 15 sccm in a LPCVD system, followed by an anisotropic etching to define NW channels and S/D regions simultaneously, as illustrated in Fig. 5-9 (b). Note that control devices (denoted as 1-level JL) were also processed along with a similar flow, except the formation of 1-level stacked dummy pattern. To prevent the collapse of 3-level NWs, we retained portions of sandwiched SiN layers during the removal of 3-level stacked dummy patterns, instead of implementing GAA structure. Next, sequential depositions of gate dielectric stack comprising blocking oxide/trapping nitride/tunneling oxide (ONO) layers with thicknesses of 11/7/3 nm and 150-nm-thick n^+-doped poly-Si films were executed to serve as gate dielectrics and electrode, respectively. Note that for the purpose of investigating the impacts of both enhanced current density and increased memory density with 3-D flash memories [27], we adopted the ONO gate dielectric stack rather than gate dielectric oxide layer. The cross-sectional TEM image of the fabricated 3-D stacked JL NW memory device is shown in Fig. 5-12, revealing that the 3-level stacked NWs with Ω-gate structure successfully avoid the occurrence of collapsed NWs after partially removing the sandwiched SiN layers of dummy patterns.

5.2-4 Planar Junctionless TFTs

Figure 5-13 briefly illustrates the key fabrication process flow of the proposed ultrathin JL poly-Si TFT. First of all, wet oxidation was performed to form 1000-nm-thick oxide on a six-in silicon substrate as the buried oxide [Fig. 5-13 (a)], followed by the deposition of a 17-nm-thick nitride layer as the etching-stop layer. A 9-nm-thick *in situ* phosphorous doped n^+-poly-Si layer was deposited to serve as the channel layer [Fig. 5-13 (b)]. The poly-Si active region was then defined by lithographic and. subsequent anisotropic etching steps, followed by the successive depositions of a 13-nm TEOS oxide as the gate dielectric and 200-nm *in situ* n^+-poly-Si as the gate electrode. Afterwards, the gate pattern was defined by a lithographic step and subsequently etched by reactive-ion etching, as shown in Fig. 5-13 (c). Sidewall spacers were formed with a 20-nm TEOS oxide layer and a 20-nm nitride layer [Fig. 5-13 (d)]. To reduce the parasitic S/D resistances, a 5-nm-thick nickel layer and a 15-nm-thick titanium nitride layer were first deposited [Fig. 5-13 (e)] and consecutively annealed to form NiSi on the gate, and S/D regions [Fig. 5-13 (f)], followed by a standard back-end process to form the metal connections. In contrast with JL devices, the control samples, denoted as inversion-mode (IM) counterparts, were fabricated with a similar process

flow. The major differences from the JL devices are the adoption of a 9-nm-thick undoped poly-Si channel and the S/D junctions formed with the implant-to-silicide technique [28]. Figure 5-14 displays the top-view SEM and cross-sectional TEM images of a fabricated JL device showing NiSi in the S/D regions. In the picture, an unexpected void above the NiSi region was formed during the preparation of the test sample by focus ion beam.

5.3 Measurement Setup

5.3-1 Electrical Measurement Setup

The experimental setup for the measurement of I-V characteristics consists of an HP4156A precision semiconductor parameter analyzer, an Agilent-81110A pulse generator, an Agilent-E5250A low leakage switch mainframe, and a Visual Engineering Environment (VEE) software. All the equipment is controlled by the interactive characterization software (ICS) program. An exsiccator and a temperature-regulated hot chuck are used to keep the humidity and temperature at the same level (relative humidity of 30% and 25 ^{o}C).

The HP-4156 provides a high current resolution to pico-ampere range for the current measurement. The Agilent-81110A with high timing resolution generates the pulse for transient and P/E characteristics. The Agilent-E5250A switches the signal from the HP-4156 and the Agilent-81110A to the device automatically. The measurement systems are applied to record the current-voltage (I-V) characteristics and test the memory characteristics.

5.3-2 S-Parameter Measurement Setup

To evaluate the high-frequency performances of fabricated JL poly-Si TFTs, S-parameters are measured on chip from 200 MHz to 20 GHz. The measurement system mainly consists of an Agilent N5245A PNA-X network analyzer, a bias-network (HP 11612V K11, HP 11612V K21), and a HP 4142B dc source/monitor, as illustrated in Fig. 5-15. All the equipment is controlled by the Agilent Integrated Circuit Characterization and Analysis Program (IC-CAP) software platform, and the data processing is served by IC-CAP as well. Afterwards, the measured S-parameters are used to acquire additional RF information such as cutoff frequency (f_t), maximum oscillation frequency (f_{max}), Y parameters and Z parameters, *etc*.

5.3-3 De-embedding Process

For the purpose of precisely measuring the high-frequency characteristics from devices, two-step correction procedure must be carried out. First step is to calibrate the whole measurement system. Available calibration techniques, including through-reflect-line (TRL), line-reflect-match (LRM), and short-open-load-through (SOLT), are commonly adopted to boost the accuracy of measurement results [29]. In the second step, the parasitic effects resulted from the bonding pads and interconnect have to be deducted owing to the significant coupling effects between the metals especially at high frequency. This is the so-called "de-embedding" procedure in terms of deducting the parasitic effects.

In our high-frequency characterization, we adopt the SOLT technique to calibrate the measurement system, and implement the aforementioned de-embedding procedure to remove the parasitic effects via open and short test fixtures. The SOLT calibration model consists of open-circuit capacitance, short-circuit inductance, matching load, and length of the through line [30]. Figure 5-16 illustrates the equivalent circuit diagram comprising the parallel parasitic capacitances (Y_{p1}, Y_{p2}, Y_{p3}) and series parasitic impedances (Z_{p1}, Z_{p2}, Z_{p3}) surrounding the transistor. The mask layout of open test fixture and the diagram of the equivalent circuit equipped with parallel parasitic capacitances are shown in Figs. 5-17 (a) and (b), respectively. The mask layout of short test fixture and the diagram of the equivalent circuit equipped with serial parasitic impedances and parallel parasitic capacitances are shown in Figs. 5-18 (a) and (b), respectively. In the first step of de-embedding process, the parallel parasitic capacitances and serial parasitic impedances can be separately calculated by mathematical matrixes described in Eqs. 5-1 and 5-2,

$$Y_{open} = \begin{bmatrix} Y_{p1} + Y_{p3} & -Y_{p3} \\ -Y_{p3} & Y_{p1} + Y_{p3} \end{bmatrix} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(5\text{-}1),$$

$$\left(Y_{short} - Y_{open}\right)^{-1} = \begin{bmatrix} Z_{p1} + Z_{p3} & Z_{p3} \\ Z_{p3} & Z_{p1} + Z_{p3} \end{bmatrix} \ldots\ldots\ldots\ldots\ldots\ldots(5\text{-}2),$$

where Y_{open} is Y-parameter matrix measured from the open test fixture, and Y_{short} is Y-parameter matrix measured from the short test fixture. Next, the actual transistor's Y-parameter matrix without parasitic effects can be calculated using Eq. 5-3:

$$Y_{transistor} = \left[(Y_{DUT} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1} \right]^{-1} \ldots\ldots\ldots\ldots\ldots(5\text{-}3),$$

where $Y_{transistor}$ is Y-parameter matrix measured from the transistor, and Y_{DUT} is Y-parameter matrix measured from the transistor with parasitic effects. By virtue of two-step de-embedding process, the impact of parasitic effects can be deducted and accordingly the accuracy of measured high-frequency characterization is guaranteed [31].

5.4 Results and Discussion

5.4-1 Electrical Characteristics of Junctionless NWFETs

Figure 5-19 shows the transfer characteristics of JL and IM devices with the TEOS oxide/TiN gate stack and its NW cross-sectional dimension as previously described in Fig. 5-4. The JL device with such tiny NW volume exhibits an on current-to-off current ratio (I_{on}/I_{off}) ratio of 5.2×10^6 at $V_G = 2$ V and an excellent subthreshold slope (SS) of 199 mV/dec comparable to that in the IM counterpart (184 mV/dec). Owing to the adoption of the small volume of the NW channels together with GAA configuration, both IM and JL devices exhibit good transfer characteristics as expected [32]. But the on-state current drivability of IM device is obviously worse than that of the JL device. The transconductance (Gm) versus gate voltage of the JL and IM devices with the TEOS oxide/TiN gate stack at $V_D = 0.5$ V is shown in Fig. 5-20. The Gm peak value of JL device is approximately five times larger than that of the IM one ascribed to the abundance of the carriers flowing through the body of the channel in the JL device. Therefore, the I_{on} is inherently enhanced with the JL scheme. Figure 5-21 illustrates total resistance (R_{total}) versus channel length measured at $V_G - V_{th}$ of 4 V and V_D of 0.15 V for both JL and IM devices with the TEOS oxide/TiN gate stack. The R_{total} can be calculated using the output characteristics data with various channel lengths and can be described as:

$$R_{total} \equiv {V_D}/{I_D} = R_{SD} + R_{ch} \quad \text{..........(5-4)}$$

,

where R_{SD} is the S/D series resistance and R_{ch} is the channel resistance, respectively. The R_{SD} could be estimated by extrapolating the curves to L = 0 since R_{ch} decreases to zero at L = 0, and accordingly R_{SD} could be extracted at low V_D and high V_G [33, 34]. The extracted R_{SD} are 0.49 and 9.65 kΩ for the JL and IM devices, respectively. The larger R_{SD} found in the IM device reveals that the JL technique can eliminate the S/D

junction-effect by its inherently homogeneous doping configuration from S/D to channel. On the other hand, the slope of the curves in the plot reveals the information of R_{ch} per unit channel length, indicating that the IM device exhibits a larger R_{ch} of 403.62 kΩ/μm, as compared with 108.66 kΩ/μm in JL one. Since the carrier transport in JL device is bulk conduction and accordingly the cross section for carrier flow is much larger than that in the IM counterpart. Consequently, both R_{ch} and R_{SD} are lower in the JL device, leading to the boosted current drivability as expected.

Figure 5-22 exhibits the transfer characteristics of JL and IM devices with the Al_2O_3/TiN gate stack and the correlative NW cross-sectional dimension as previously described in Fig. 5-5, while another two JL devices with larger channel cross sections are compared as well to evaluate the volume effect on the device switching-behavior. Note that we denote JL and IM devices as doped channel (JL) and undoped channel (IM), respectively. Larger NW channels (Mid-sized JL and Large-sized JL) perform more aggravated switching properties in terms of poor I_{on}/I_{off} behaviors. The conduction mechanism is through the current of majority carriers flowing in the bulk of the doped NW channel, and the bulk conduction path would be progressively depleted by decreasing the gate voltage to switch off the JL device, implying that the cross section of NW channel in the JL scheme has great impact on the device switching-behavior. Therefore, both Mid-sized JL and Large-sized JL splits can not be effectively turned off by gate, even with the GAA configuration and Al_2O_3/TiN gate stack biased at a high gate voltage of -10 V, as illustrated in the plot. On the other hand, the JL split with tiny NW channels exhibits superior switching ability with SS of 210 mV/dec and I_{on}/I_{off} ratio of 7×10^6, similar to the previously mentioned JL device in Fig. 5-19, where I_{on} is defined as the drain current at $V_G - V_{th} = 2$ V and I_{off} is the minimal drain current. In addition, the output characteristics of JL and IM splits measured at $V_G - V_{th} = 0\sim2$ V and step = 1 V with L = 0.4 μm are shown in Fig. 5-23, indicating a 1.75 times output current value over the IM counterpart is achieved through the JL scheme. Figure 5-24 shows the transconductance (Gm) as a function of gate length. Apparently, the JL split depicts larger Gm than the IM one, ascribed to the abundance of the carriers flowing through the body of channel in the JL device. Besides, the Gm in JL split obviously increases with decreasing gate length compared with the IM device, implying the impact of parasitic S/D resistance is diminished in the JL devices. One plausible reason for such findings is the elimination of S/D junctions in the JL scheme as previously demonstrated in Fig. 5-21. The threshold voltage (V_{th}) as a function of channel length

for both JL and IM splits is shown in Fig. 5-25. As can be seen in the plot, both JL splits (JL with Al_2O_3 and JL with SiO_2) exhibit lower V_{th} values owing to the inherent accumulation-mode operation. In addition, positive V_{th} values can be observed in the JL devices with Al_2O_3 as compared with the SiO_2 counterparts, due to the effect of negative fixed charges contained in the Al_2O_3 gate dielectrics. Furthermore, no obvious V_{th} roll-off phenomenon is observed with Al_2O_3 splits, confirming that the adoptions of both GAA configuration and Al_2O_3 gate dielectric are beneficial for device performance. Figure 5-26 shows I_{on} as a function of gate length for JL and IM devices with Al_2O_3/TiN gate stack, extracted at V_G - V_{th} = 2 V and V_D = 0.5 V. Obviously the JL devices show better current drive as compared with IM counterparts, particularly for the long-channel devices. Because JL devices inherently possess much larger cross section for carrier transport, this brings about the reduction in the channel resistance for the JL devices, as previously demonstrated in Fig. 5-21. However, the enhancement for short-channel devices is not remarkable as long-channel counterparts. Both increments of I_{on} and Gm in terms of JL-to-IM ratios, denoted as I_{on}(JL)/I_{on}(IM) and Gm(JL)/Gm(IM), are exhibited in Figs. 5-24 and 5-26, respectively. There are two plausible reasons described as follows. The series resistances in the S/D regions (R_{SD}) for the JL devices are not low enough and thus contribute to this trend when the channel length decreases, even if R_{SD} has been previously verified with reduced values for JL devices. Therefore, the S/D regions could be engineered with the high doping concentration or silicide process to further reduce R_{SD} and boost I_{on}. For second plausible reason, the shape of long-channel NW is possibly like a drawbridge rather than straight from source to drain ideally, as shown in Fig. 5-27. For the long-channel NWs, the central region of NW channel located away from the supporting S/D ends would topple down and further touch the substrate surface. In contrast with long channel, the short-channel NWs maintain straight suspension between the S/D regions as depicted in the inset. Consequently, the actual gate configuration in the central part of a long channel would become omega-shaped gate structure (Ω-gate) rather than ideal GAA structure. Owing to such Ω-gate configuration in the central region of a long channel, the transport carriers induced in the surfaces of IM devices would be decreased as compared with bulk-conduction JL devices. Accordingly, both Gm and I_{on} enhancement for the JL split become pronounced as channel length increases, implying that the JL device is insensitive to gate configuration in the on state.

5.4-2 NVM Characteristics of JL NW SONOS Devices

In this section, the Fowler-Nordheim (FN) tunneling mechanism was employed for the program/erase (P/E) operations of the fabricated SONOS memory devices with channel length of 0.4 μm. Note that n^+-doped poly-Si employed as NW channel in the JL SONOS is fabricated with the PH_3 flow rate of 15 sccm. In the programming process (PGM), large positive biases ranging from 9 to 13 V were applied to the gate while keeping the S/D grounded. The programming behaviors of both JL and IM devices are shown in Fig. 5-28. Apparently, the JL SONOS split performs faster programming characteristics compared with IM counterpart. Such superior programming speed can be ascribed to its inherently higher carrier concentration in the heavily doped NW channel, and hence, results in the enhancement of tunneling probability of carrier injection into the nitride trapping layer. Accordingly, a larger window of V_{th} shift is achieved by virtue of an abundance of electrons tunneling through the tunnel oxide and being trapped in the nitride trapping layer. Figure 5-29 shows the transfer characteristics of JL SONOS split in the programmed states biased at $V_G = 13$ V for various duration times, indicating that a wide program window up to 4.8 V can be achieved without obvious degradation in the SS. In contrast with the JL SONOS, the maximal program window of IM counterpart is around 3.2 V, when biased at $V_G = 13$ V for 1 ms, inferring that the JL SONOS is capable of performing the low-voltage program operation and multilevel programming with distinguishable V_{th} values. Such multilevel programming property of JL SONOS is illustrated in Fig. 5-30. As can be seen in the plot, total four states with V_{th} difference of 1 V among them are obtained by applying erasing bias of -9 V and programming biases of 9, 11, and 13 V for 100 ns. These results demonstrate the JL SONOS is effective to promote the programming behaviors in terms of higher speed, lower operation voltage and larger program window, thanks to its inherent abundance of carriers.

Before we explore the erase property of JL scheme, two SONOS devices initially were programmed to memory windows (V_{th} shift) of 3 and 2.5 V for the JL and IM splits, respectively. For the erasing process (ERS), negative biases were applied to the gate while keeping the S/D grounded. Figure 5-31 exhibits the erase properties of the JL and IM SONOS splits. In a typical charge trapping SONOS device, the erase mechanism can be ascribed to the de-trapping of trapped electrons back to the channel or the injection of holes into the nitride layer, depending on the band alignment

conditions. Therefore, the JL SONOS exhibits slower erasing speed, which is ascribed to the dearth of hole concentration in the n^+-doped poly-Si channel. In contrast with the program property, the difference in erasing speed between the JL and IM splits is not so pronounced. We attribute such interesting finding to some plausible reasons described as follows. According to the work contributed by M. Lenzlinger and E. H. Snow [35], the electron injection from Si substrate to nitride under Fowler-Nordheim (FN) tunneling can be described as:

$$J = \alpha E_{ox}^2 \exp\left(-\frac{E_c}{E_{ox}}\right) \quad \text{.......................................(5-5),}$$

with

$$\alpha = \frac{m_0}{m_{ox}} \frac{q^3}{16\pi^2 \hbar} \frac{1}{q\Phi_1} \quad \text{...(5-6),}$$

and

$$E_c = 4\sqrt{2m_{ox}} \frac{(q\Phi_1)^{3/2}}{3\hbar q} \quad \text{...(5-7),}$$

when

$$E_{ox} \geq \frac{\Phi_1}{t_{ox}} \quad \text{...(5-8),}$$

in which Φ_1 is the tunneling oxide barrier height for electron, t_{ox} is the thickness of the oxide, q is the electron charge, $\hbar$ is the reduced Planck's constant, m_0 is the mass of free electron and m_{ox} is the effective mass of an electron in the oxide. Therefore, both the carrier effective mass and barrier height at SiO_2/Si interface would affect the magnitude of FN tunneling current as indicated in Eqs. 5-5, 5-6, and 5-7. On the other hand, the holes have larger effective mass and higher potential barrier than the electrons transiting in the programming operation. Consequently, the reduced hole concentration in the n^+-doped poly-Si channel results in inefficient erasing operation, compared with relatively faster programming process as revealed in Fig. 5-28. In addition, the segregation of phosphorus impurities occurring at the surface of n^+-doped Si NW structures leads to lower effective density of the carriers at the SiO_2/Si NW interface than that in the bulk of Si NW [36]. Therefore, a certain number of holes practically would be induced at the surface of the phosphorus-doped Si NW channel under a large negative gate bias during the erasing operation. The smaller difference in the erasing speed between JL and IM splits may result from the mix of phosphorus-segregation

effect and reduced hole concentration as mentioned above. Moreover, the JL SONOS split performs a comparable V_{th} shift of 2.5 V to the IM counterpart at -13 V for 0.2 ms, inferring that the erasing speed of the JL device can be aggressively boosted using a large negative gate bias. In addition, the IM SONOS split exhibits a saturation phenomenon after 10^{-4} s, and the corresponsive V_{th} values slightly rise up with a gate bias of -13 V, ascribed to the electron back-injection from the gate to the charge-trap layer at a high electric field. Such issue would suppress the extension of memory window, and could be relieved by adopting gate materials with higher work function, including TaN, TiN, or p^+-doped poly-Si [37]. Figures 5-32 and 5-33 show the data retention and endurance characteristics of both JL and IM SONOS splits at room temperature with programming operation at 11 V for 50 μs and erasing operation at -10 V for 1 ms. Both splits show a charge loss of less than 10 % during the retention time of 10^4 s, and data retention of around 75% for two splits is observed by extrapolating the retention characteristics at the end of 10 years as compared with the original memory window. In addition, the memory window of the JL device remains almost unchanged after 1 k operation cycles as revealed in the plot. As a result, both splits show almost identical retention behavior and endurance property, implying that the n^+-doped channel has little impact on the data retention and endurance characteristics as compared with the IM counterpart.

Next, we investigate the effects of doping concentration and gate configuration on JL NW-SONOS devices, while the denotements are listed in Table 5-2 for clarity of discussion. Figure 5-34 depicts the typical transfer characteristics for the four splits of JL SONOS devices. Apparently, both GAA-H and Ω-H devices show larger on-state currents and more negative V_{th} as compared with the lighter-doped counterparts, attributing to the higher carrier concentration in the channels. Besides, the heavier doping concentration in the channel and S/D regions is beneficial to reducing the series resistances, and accordingly boosting the current drivability. On the other hand, the GAA-L and Ω-L splits exhibit nearly identical V_{th} and SS properties as compared with the heavier-doped devices, where remarkable disparities in V_{th} and SS between the GAA-H and Ω-H splits can be observed, implying that the lighter-doped devices is relieved from the influence of the gate configuration. Moreover, the Ω-H device show more negative V_{th} and poor SS as compared with the GAA-H split, attributing to the comparatively reduced gate controllability. Figure 5-35 exhibits the programming properties of the four splits with V_G of 11 V and keeping the S/D grounded. As can be

seen in the plot, the programming speed of both lighter-doped splits is apparently faster than the heavier-doped counterparts, contrary to the previous work revealed in Fig. 5-28. According to the discussion of program behaviors between JL and IM splits as depicted in Fig. 5-28, we conclude that the enhanced tunneling probability of carrier injection into the nitride trapping layer is attributed to higher carrier concentration in the heavily doped NW channel, and accordingly results in larger programming window and faster speed. The heavier-doped splits are expected to perform superior programming speed intuitionally rather than much slower performance. In accordance with the simulation results by Yan [38], the JL device with lighter-doped channel may induce an accumulation layer at the surface in the on-state, while the heavier-doped JL device replaces such accumulation layer formed in the surface of channel by the bulk-conduction. In our case, faster programming speed of both lighter-doped splits would be ascribed to such accumulation layer at the channel surface, and therefore, leads to larger tunneling probability and higher programming behavior in the beginning of the programming process. But the programming windows of heavier-doped splits progressively expand during the programming process. In particular, the difference of V_{th} shift between the GAA-L and GAA-H splits is about 1.5 V at the PGM time of 10^{-6} s, and it becomes 0.5 V at the PGM time of 1 s. Before erasing, four splits of devices initially were programmed to memory windows of 3 V. The erasing behaviors of the four splits are shown in Fig. 5-36 with V_G = -11 V and keeping the S/D grounded. Both heavier-doped splits show slower erasing properties, consistent with the previous discussion in Fig. 5-31, attributing to the relative dearth of hole concentration in the n^+-doped poly-Si channel. Moreover, the Ω-H split exhibits much lower erasing efficiency as compared with the GAA-H one, implying the GAA architecture is better at erase operation thanks to its better gate controllability. On the other hand, the lighter-doping devices reveal a comparable ERS speed despite the gate configuration. Figures 5-37 and 5-38 show the data retention characteristics for various splits at room temperature with programming operation at 11 V for 50 μs and erasing operation at -10 V for 1 ms. As can be seen in the Fig. 5-37, both splits show almost identical retention behavior property after 10 years, implying that the channel doping concentration does not influence the data-storage ability. Besides, the Ω-gate configuration exhibits a comparable memory window to the GAA one after 10 years as revealed in Fig. 5-38. The retention behaviors show that the memory window can be larger than 1.3 V at least after 10 years at room temperature, regardless of channel doping concentration and gate

configuration.

5.4-3 Electrical Characteristics of 3-D Multilayer-Stacked JL NWFETs

In this section, all splits having channel length of 1 μm are characterized. Transfer characteristics and the affiliated cross-sectional SEM image of a disabled JL device are shown in Figs. 5-39 and 5-40, respectively. From the SEM picture, apparently, the residues of n^+-doped poly-Si layers left at bilateral sidewalls of multilayer-stacked dummy patterns after the anisotropic etching process for defining NW channels and S/D regions were the main culprit for the fatally leaky behavior as revealed in Fig. 5-39. In contrast with the failed device, the cross-sectional TEM image of working 3-level JL device is depicted in Fig. 5-12. The dimensions of the embedded NWs are not uniform, owing to the non-optimized etching processes in forming the stack and nano cavities. Figures 5-41 (a) and (b) illustrate the transfer and output characteristics of both 1-level and 3-level JL splits with L = 1 μm, measured at V_D = 0.1 and 2 V [Fig. 5-41(a)], V_G - V_{th} = 0 ~ 4 V with step = 2 V [Fig. 5-41(b)], respectively. The feasibility of 3-D stacked JL-NWFET is verified with remarkable current drive enhancement which is at least 10 times higher than that of the 1-level JL. In addition, more negative V_{th}, severer off-state leakage current, and larger drain-induced grain barrier lowering (DIGBL) can be found, attributing to non-uniform volume of stacked NW channels. Consequently, the fluctuation of the fabricated 3-level JL device is worthy to investigate. The cumulative distribution of the V_{th} of the two sets of devices is shown in Fig. 5-42, in which the random sampling devices are around 25 to 30. The results indicate that the 3-level JL split has larger variation in V_{th} as ascribed to irregular NW dimensions mentioned above. Larger size of NW in JL device represents comparatively more carriers need to be depleted for switching off the channel, contributing to a more negative V_{th} distribution. On the other hand, the cumulative distributions of the subthreshold swing (SS), on-current (I_{on}) and off-current (I_{off}) shown in Figs. 5-43, 5-44, and 5-45, respectively, exhibit similar trends as the V_{th} distribution shows, confirming the more severe fluctuation of 3-level split. Further refining the process conditions of etching steps is required to alleviate this issue. Furthermore, it is notable that I_{off} distribution exhibits worse fluctuation in Fig. 5-45. This is because the bulk conduction of JL device is extremely sensitive to the conduction area and the 3-level JL split has a larger variation in geometries of NWs, the origin of the above observation.

5.4-4 RF Characteristics and Small-Signal Modeling of Planar JL TFTs

All splits having 8-μm gate width and 0.4-μm gate length were characterized. Before investigating the RF performance, we start with the typical transfer and output characteristics of the fabricated devices as shown in Figs. 5-46 and 5-47, respectively. In Fig. 5-46, the JL device measured at V_D = 0.1 and 2 V achieves a remarkable on-current-to-off-current ratio of larger than 8×10^7, owing to the use of the ultrathin channel. Because of the heavily doped channel, the V_{th} of the JL device is −0.19 V. V_{th} is defined as the gate voltage (V_G) at a drain current (I_d) equal to $10^{-8} \times W/L$, where W and L are the gate width and length, respectively. The device can be adjusted to be normally off if the gate material is replaced with a higher work function such as p^+-poly-Si, TiN, or TaN relative to the poly-Si channel [37]. Such gate materials are also conducive to obtaining a suitable V_{th} value for heavily-doped n^+-channel devices by depletion of carriers owing to the work function difference between the channel and gate material [39]. Shown in Fig. 5-47 are the output characteristics of the devices measured at various gate overdrive conditions ($V_{GS} - V_{th}$ = 0 ~ 3 V and step = 1 V). When ($V_{GS} - V_{th}$) is equal to 3 V, the JL device shows a drive current about 7.4 times higher than that of the IM counterpart. This is mainly attributed to the reduction in the channel resistance with the JL schemes.

Low-frequency noise (LFN) behavior is an important index for evaluating the device's signal-to-noise performance. Figure 5-48 shows the frequency dependence of the measured drain-current noise power spectral density (S_{id}) operated under ($V_{GS} - V_{th}$) of 0.5 V between 10 Hz and 10 kHz for all splits at V_D = 0.1 V. For the JL device, the S_{id} characteristic is four orders of magnitude lower than that of the IM counterpart. This can be ascribed to the distinct conduction mechanism of the JL device [40]. In addition, the larger grain size of the *in situ* phosphorus-doped poly-Si channel can also meliorate the LFN [41]. To identify the noise source, the normalized noise power spectrum density (S_{id}/I_d^2) and the transconductance-to-drain-current ratio squared [$(g_m/I_d)^2$] versus the drain current for the devices are shown in Fig. 5-49. From the results, it is inferred that the noise in the JL device is mainly dominated by Hooge mobility fluctuation [42] since S_{id}/I_d^2 is proportional to $1/I_d$ and the Hooge parameter is about 1.4×10^{-4}. As has been pointed out previously [43], the Hooge parameter decreases with increasing doping level. This is because an increase in doping level tends to reduce the band bending at the grain boundaries and therefore increases the

current drive (higher carrier concentration and higher effective mobility). It thus improves the LFN for the heavily-doped JL device as compared with the undoped channel of the IM counterpart. On the contrary, the noise in the IM device is mainly dominated by carrier number fluctuation [44], because S_{id}/I_d^2 is proportional to $(g_m/I_d)^2$ [the dashed lines in Fig. 5-49]. In short, the inherent bulk conduction feature of the JL devices improves the LFN and achieves higher signal-to-noise ratio as compared with that of the IM device.

To examine the high-frequency performances of JL devices, *S*-parameters are measured on planar JL poly-Si TFTs rather than NW-based FETs, due to the much larger transconductances in the former. After de-embedding the parasitic pad effects from the measured S-parameters, the ac current gain (H_{21}) and unilateral power gain (U) of JL and IM devices, revealed in Figs 5-50 and 5-51, are calculated to extract cutoff frequency (f_t) and maximum oscillation frequency (f_{max}), respectively. The f_t and f_{max} of all splits with respect to the drain current at V_D = 2 V are shown in Fig. 5-52. The peak f_t and f_{max} are around 0.51 and 1.47 GHz, respectively, for the IM device. In contrast, the JL device exhibits an f_t of 3.4 GHz and an f_{max} of 7.4 GHz, which are almost 6.6 and 5 times higher than those of the IM counterpart, respectively, owing, in large part, to the larger transconductance (G_m) of the JL device, as shown in Fig. 5-46. The dc and ac characteristics of all splits are compared in Table 5-4, implying that the JL poly-Si TFT technology has a potential for RF applications.

The small-signal equivalent circuit of the fabricated TFTs is shown in Fig. 5-53. We used the cold model [45-48] to extract the S/D external parasitic resistances (R_d, R_s) and gate resistance (R_g). Based on the equivalent circuit, the parasitic resistances of the cold model can be measured by the real parts of *Z*-parameters, which can be derived as follows:

$$\mathrm{Re}(Z_{11}-Z_{12}) = R_g + \frac{A_g}{\omega^2 + B} \qquad \text{(5-9)},$$

$$\mathrm{Re}(Z_{12}) = \mathrm{Re}(Z_{21}) = R_S + \frac{A_S}{\omega^2 + B} \qquad \text{(5-10)},$$

$$\mathrm{Re}(Z_{22}-Z_{12}) = R_d + \frac{A_d}{\omega^2 + B} \qquad \text{(5-11)},$$

where A_g, A_s, A_d, and B are constant values at fixed bias. When the frequency approaches infinity, the parasitic resistance components can be extracted. The results of extrinsic resistances of JL device are shown in Fig. 5-54. After the extraction of extrinsic parameters, this can be carried out using the following procedure [46]. First,

the measured S-parameters of the device are transferred to Z-parameters by subtracting R_g, R_d and R_s which are in series. Then the Z-parameters are further transferred to the Y-parameters and the matrix of the intrinsic admittance can be determined. The ac intrinsic equivalent circuit [45, 46, 49] of the TFT is shown in Fig. 5-53 marked by the dashed line, and the following equations can be derived by the Y-parameters

$$Y_{11} = j\omega(C_{gs} + C_{gd}) \quad \text{(5-12)},$$

$$Y_{12} = -j\omega C_{gd} \quad \text{(5-13)},$$

$$Y_{21} = g_m - j\omega(C_{gd} + g_m\tau) \quad \text{(5-14)},$$

$$Y_{22} = \frac{1}{r_o} + j\omega(C_{ds} + C_{gd}) \quad \text{(5-15)},$$

where the resistance (r_o) and the transconductance (g_m) can be extracted directly from the real parts of the Y-parameters. The mean delay time (τ) can be calculated from the imaginary part of the Y-parameters divided by the multiplication of frequency and g_m. The corresponding parasitic parameters of small-signal equivalent circuit can be derived as

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \quad \text{(5-16)},$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})}{\omega} \quad \text{(5-17)},$$

$$C_{ds} = \frac{\mathrm{Im}(Y_{12}) + \mathrm{Im}(Y_{22})}{\omega} \quad \text{(5-18)},$$

$$r_o = \frac{1}{\mathrm{Re}(Y_{22})} \quad \text{(5-19)},$$

$$g_m = \mathrm{Re}(Y_{21}) \quad \text{(5-20)},$$

$$\tau = \frac{\mathrm{Im}(Y_{12}) - \mathrm{Im}(Y_{21})}{g_m \times \omega} \quad \text{(5-21)},$$

The imaginary parts of the measured Y-parameters as a function of the angular frequency (ω) for the JL device are shown in Fig. 5-55, while the values of C_{gs}, C_{ds}, and C_{gd} can be extracted from the slopes of the curves according to Eqs. (5-16) − (5-18). The g_m and r_o with respect to ω are depicted in Fig. 5-56. In addition, Fig. 5-57 illustrates the dependence of the imaginary parts of the Y-parameters divided by g_m ($[\mathrm{Im}(Y_{12})-\mathrm{Im}(Y_{21})]/g_m$), with respect to ω, and the slope of the curve represents τ according to Eq. (5-21). The above procedure is also applied to IM device. Table 5-4 summarizes the small-signal parameters of fabricated JL and IM poly-Si TFTs with

W/L=8 μm/0.4 μm. In addition, we also apply the extracted parameters mentioned above in the small-signal model to simulate and further compare the outcome with the measured *S*-parameters from 1 to 8 GHz at V_D = 2 V and V_G = 4 V. The modeling results of the *S*-parameters verified with the measured values are exhibited in Fig. 5-58, and we find that the simulation results (symbols) correspond well with the measured data (lines), confirming that the small-signal model is accurate.

5.5 Summary

In this chapter, we have fabricated and characterized various JL devices, including multiple-gated NWFETs, multiple-gated NW SONOS memory cells, 3-D multilayer-stacked NWFETs, and planar TFTs with an implant-free technique in order to investigate the operation mechanism of proposed JL scheme and further demonstrate its feasibility for future 3-D electronics and system-on-panel (SoP) applications.

For the JL NWFETs, we have demonstrated the feasibility of GAA poly-Si NWFETs with JL scheme by employing only one *in situ* doped poly-Si layer to act as the active regions without additional intentional doping procedure. From the results of the electrical characterizations, a sufficiently small cross section of the NW channels is essential to obtain a superior on-to-off current ratio and a low subthreshold slope for a heavily-doped channel device. Excellent Vth roll-off properties and boosted on-state performance are found in the JL devices especially as the channel length increases, attributing to lower S/D series resistances and channel resistances. In addition, the adoption of Al_2O_3 as the gate dielectric shifts the V_{th} to a positive value and thus is conducive to acquiring desirable V_{th}. Consequently, the proposed JL NWFETs featuring simplified fabrication processes stand as highly promising transistors for future practical manufacturing and applications.

For memory cells, we have successfully demonstrated the feasibilty of JL NW SONOS memory devices by employing only one *in situ*-doped n^+-poly-Si layer. The fabricated JL devices display enhanced programming properties and desirable data retention behavior. But no improvement in the erasing efficiency is observed, the JL device exhibits comparable erase window to the IM counterpart. On the other hand, the effects of doping concentration and gate configuration on the JL NW SONOS memory cells have been investigated. For the more-heavily-doped JL NW devices, the electrostatic behaviors and memory characteristics are strongly affected by the gate

configuration. They also show degraded program/erase characteristics compared with the lighter-doped counterparts. Small disparity in data retention behaviors is observed as far as channel doping concentration and gate configuration are concerned. Therefore, the doping concentration of the JL poly-Si NW device should be carefully optimized for high-performance SONOS applications. Consequently, the proposed JL NW SONOS cells appear to be very promising for low-cost and ultrahigh-density NVMs for future 3-D electronics and SoP applications.

From the SEM, TEM and electrical characterizations, we have confirmed the feasibility of 3-D stacked JL transistors with heavily-doped poly-Si NW channels. Although the fabricated devices depict notable fluctuations, especially off-current distribution is the worst one ascribed to the extremely sensitive bulk conduction of JL scheme to geometry of NW, we believe the issue will be alleviated with the aids of applying advanced equipment and optimizing process parameters.

N-type planar ultrathin JL poly-Si TFTs have been fabricated and characterized with emphasis on RF and LFN performances. For the RF characteristics, the JL device with a gate length of 0.4 μm can achieve an f_t of 3.37 GHz and an f_{max} of 7.37 GHz at a V_D of 2 V, compared with 0.51 and 1.47 GHz, respectively, for the IM counterpart. As far as LFN is concerned, the inherent bulk conduction feature of the JL devices improves the LFN and achieves higher signal-to-noise ratio as compared with that of the IM devices. These results demonstrate that the JL poly-Si TFT technique is promising for RF modules implemented in SoP applications. Finally, we have also derived a small-signal model of the fabricated JL device and verified the accuracy by comparing the *S*-parameters. The result of comparison clearly infers that the small-signal model works well.

References

[1] S. Thompson, P. Packan, T. Ghani, M. Stettler, M. Alavi, I. Post, S. Tyagi, S. Ahmed, S. Yang, and M. Bohr, "Source/drain extension scaling for 0.1 μm and below channel length MOSFETs," in *VLSI Symp. Tech. Dig.*, 1998, pp. 132-133.

[2] J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 225-229, 2010.

[3] C. J. Su, T. I. Tsai, Y. L. Liou, Z. M. Lin, H. C. Lin, and T. S. Chao, "Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels," *IEEE Electron Device Lett.*, vol. 23, no. 4, pp. 521-523, 2011.

[4] C. J. Su, T. I. Tsai, H. C. Lin, T. Y. Huang, and T. S. Chao, "Low-temperature poly-Si nanowire junctionless devices with gate-all-around TiN/Al_2O_3 stack structure using an implant-free technique," *Nanoscale Research Lett.*, vol. 7, no. 339, pp. 1-6, 2012.

[5] H. Wang, M. Chan, S. Jagar, Y. Wang, and P. K. Ko, "Submicron super TFTs for 3-D VLSI applications," *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 439-441, 2000.

[6] E. K. Lai, H. T. Lue, Y. H. Hsiao, J. Y. Hsieh, C. P. Lu, S. Y. Wang, L. W. Yang, T. Yang, K. C. Chen, J. Gong, K. Y. Hsieh, R. Liu, and C. Y. Lu, "A multilayer stackable thin-film transistor (TFT) NAND-type Flash memory," in *IEDM Tech. Dig.*, 2006, pp. 41-44.

[7] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles, and J. L. Goldma, "High-performance thin-film transistors using semiconductor nanowires and nanoribbons," *Nature*, vol. 425, no. 6955, pp. 274-278, 2003.

[8] H. C. Lin and C. J. Su, "High-performance poly-Si nanowire NMOS transistors," *IEEE Trans. Nanotechnol*, vol. 6, no. 2, pp. 206-212, 2007.

[9] S. D. Suk, M. Li, Y. Y. Yeoh, K. H. Yeo, J. K. Ha, H. Lim, H. W. Park, D. W. Kim, T. Y. Chung, K. S. Oh, and W. S. Lee, "Characteristics of sub 5nm tri-gate nanowire MOSFETs with single and poly Si channels in SOI structure," in *VLSI Symp. Tech. Dig.*, 2009, pp. 142-143.

[10] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "High-performance fully depleted silicon nanowire (diameter ≤ 5 nm) gate-all-around CMOS devices,"

IEEE Electron Device Lett., vol. 27, no. 5, pp. 383-386, 2006.

[11] M. Im, J. W. Han, H. Lee, L. E. Yu, S. Kim, C. H. Kim, S. C. Jeon, K. H. Kim, G. S. Lee, J. S. Oh, Y. C. Park, H. M. Lee, and Y. K. Choi, "Multiple-gate CMOS thin-film transistor with polysilicon nanowire," *IEEE Electron Device Lett*., vol. 29, no. 1, pp. 102-105, 2008.

[12] H. H. Hsu, H. C. Lin, C. W. Luo, C. J. Su, and T. Y. Huang, "Impacts of multiple-gated configuration on the characteristics of poly-Si nanowire SONOS devices," *IEEE Trans. on Electron Devices*, vol. 58, no. 3, pp. 641-649, 2011.

[13] Y. Kamigaki, S. I. Minami, T. Hagiwara, K. Furusawa, T. Furuno, K. Uchida, M. Terasawa, and K. Yamazaki, "Asymmetric halo CMOSFET to reduce static power dissipation with improved performance," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 1714-1722, Dec. 1989.

[14] J. D. Lee, S. H. Hur, and J. D. Choi, "Effects of floating-gate interference on NAND flash memory cell operation," *IEEE Electron Device Lett*., vol. 23, no. 5, pp. 264-266, May 2002.

[15] M. H. White, D. A. Adams, and J. Bu, "On the go with SONOS," *IEEE Circuits Devices Mag*., vol. 16, no. 4, pp. 22-31, 2000.

[16] L. Khomenkova, B. S. Sahu, A. Slaoui and F. Gourbilleau, "Hf-based high-κ materials for Si nanocrystal floating gate memories," *Nanoscale Research Lett*., vol. 6, no. 172, pp. 1-8, 2011.

[17] B. S. Sahu, F. Delachat, A. Slaoui, M. Carrada, G. Ferblantier, and D. Muller, "Effect of annealing treatments on photoluminescence and charge storage mechanism in silicon-rich SiN_x:H films," *Nanoscale Research Lett*., vol. 6, no. 178, pp. 1-10, 2011.

[18] K. H. Lee, H. C. Lin, and T. Y. Huang, "A novel charge-trapping-type memory with gate-all-around poly-Si nanowire and HfAlO trapping layer," *IEEE Electron Device Lett*., vol. 34, no. 3, pp. 393-395, Mar. 2013.

[19] A. J. Walker, S. Nallamothu, E. H. Chen, M. Mahajani, S. B. Hemer, M. Clark, J. M. Cleeves, S. V. Dunton, V. L. Eckert, J. Gu, S. Hu, J. Knall, M. Konevecki, C. Petti, S. Radigan, U. Raghuram, J. Vienna, and M. A. Vyvoda, "3D TFT-SONOS memory cell for ultra-high density file storage applications," in *VLSI Symp. Tech. Dig*., 2003, pp. 29-30.

[20] H. T. Lue, T. H. Hsu, Y. H. Hsiao, S. P. Hong, M. T. Wu, F. H. Hsu, N. Z. Lien, S. Y. Wang, J. Y. Hsieh, L. W. Yang, T. Yang, K. C. Chen, K. Y. Hsieh, and C. Y. Lu, "A

highly scalable 8-layer 3D vertical-gate (VG) TFT NAND Flash using junction-free buried channel BE-SONOS device," in *VLSI Symp. Tech. Dig.*, 2010, pp. 131-132.

[21] Y. H. Yu, Y. J. Lee, Y. H. Li, C. H. Kuo, C. H. Li, Y. J. Hsieh, C. T. Liu, and Y. J. E. Chen, "An LTPS TFT demodulator for RFID tags embeddable on panel displays," *IEEE Trans. on Microwave Theory and Techniques*, vol. 57, no. 5, pp. 1356-1361, 2009.

[22] Y. J. E. Chen, Y. J. Lee, and Y. H. Yu, "Investigation of polysilicon thin-film transistor technology for RF applications," *IEEE Trans. on Microwave Theory and Techniques*, vol. 58, no. 12, pp. 3444-3451, 2010.

[23] Y. Wada and S. Nishimatsu, "Grain growth mechanism of heavily phosphorus-implanted polycrystalline silicon," *J. Electrochem. Soc.*, vol. 125, no. 9, pp. 1499-1504, 1978.

[24] F. Lacy, "Developing a theoretical relationship between electrical resistivity, temperature, and film thickness for conductors," *Nanoscale Research Lett.*, vol. 6, no. 636, pp. 1-14, 2011.

[25] M. T. Björk, H. Schmid, J. Knoch, H. Riel, and W. Riess, "Donor deactivation in silicon nanostructures," *Nature Nanotechnol.*, vol. 4, pp. 103-107, 2009.

[26] M. V. Fernández-Serra, Ch. Adessi, and X. Blase, "Surface segregation and backscattering in doped silicon nanowires," *Phys. Rev. Lett.*, vol. 96, no. 16, pp. 166805-1–166805-4, 2006.

[27] A. Hubert, E. Nowak, K. Tachi, V. M. Alvaro, C. Vizioz, C. Arvet, J. P. Colonna, J. M. Hartmann, V. Loup, L. Baud, S. Pauliac, V. Delaye, C. Carabasse, G. Molas, G. Ghibaudo, B. D. Salvo, O. Faynot, and T. Ernst, "A stacked SONOS technology, up to 4 levels and 6nm crystalline nanowires, with gate-all-around or independent gates (Φ-Flash), suitable for full 3D integration," in *IEDM Tech. Dig.*, 2009, pp. 637-640.

[28] C. P. Lin, Y. H. Xiao, and B. Y. Tsui, "High-performance poly-Si TFTs fabricated by implant-to-silicide technique," *IEEE Electron Device Lett.*, vol. 26, no. 3, pp. 185-187, Apr. 2005.

[29] A. Davidson, E. Strid, and K. Jones, "Achieving greater on-wafer S-parameter accuracy with the LRM calibration technique," in *34th ARFTG Conference Dig.-Winter*, 1989, pp. 61-66.

[30] M. Nishimoto, M. Hamai, J. Laskar, and R. Lai, "On-wafer calibration techniques and applications at V-band," *IEEE Microwave and Guided Wave Lett.*, vol. 4, no. 11, pp. 370-372, 1994.

[31] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, “An improved de-embedding technique for on-wafer high-frequency characterization,” in *IEEE Bipolar Circuits and Technology Meeting*, 1991, pp. 188-191.

[32] H. H. Hsu, T. W. Liu, L. Chan, C. D. Lin, T. Y. Huang, and H. C. Lin, “Fabrication and characterization of multiple-gated poly-Si nanowire thin-film transistors and impacts of multiple-gate structures on device fluctuations,” *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3063-3069, Nov. 2008.

[33] K. Terada and H. Muta, “A new method to determine effective MOSFET channel length,” *Jpn. J. Appl. Phys.*, vol. 18, no. 5, pp. 953-959, May 1979.

[34] J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho, “A new method to determine MOSFET channel length,” *IEEE Electron Device Lett.*, vol. 1, no. 9, pp. 170-173, Sep. 1980.

[35] M. Lenzlinger and E. H. Snow, “Fowler-Nordheim tunneling into thermally grown SiO_2,” *J. Appl. Phys.*, vol. 40, no. 1, pp. 278-283, Jan. 1969.

[36] M. Lenzlinger and E. H. Snow, “Surface segregation and backscattering in doped silicon nanowires,” *Phys. Rev. Lett.*, vol. 96, no. 16, pp. 166805-1–166805-4, Apr. 2006.

[37] C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song , K. C. Park, and K. Kim, “A novel SONOS structure of SiO_2/SiN/$A1_2O_3$ with TaN metal gate for multi-giga bit flash memories,” in *IEDM Tech. Dig.*, 2003, pp. 613-616.

[38] R. Yan, A. Kranti, I. Ferain, C. W. Lee, R. Yu, N. Dehdashti, P. Razavi and J. P. Colinge, “Investigation of high-performance sub-50 nm junctionless nanowire transistors,” *Microelectronic Reliability*, vol. 51, no. 7, pp. 1166-1171, 2011.

[39] C. W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J. P. Colinge, “Performance estimation of junctionless multigate transistors,” *Solid-State Electronics*, vol. 54, no. 2, pp. 97-103, 2010.

[40] C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge, “Junctionless multigate field-effect transistor,” *Appl. Phys. Lett.*, vol. 94, no. 5, pp. 053511-1–053511-2, 2009.

[41] Y. Wada and S. Nishimatsu, “Grain growth mechanism of heavily phosphorus-implanted polycrystalline silicon,” *J. Electrochem. Soc.*, vol. 125, no. 9, pp. 1499-1504, Sep. 1978.

[42] L. K. Vandamme and F. N. Hooge, “What do we certainly know about 1/f noise in MOSTs?” *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3070-3085, Nov. 2008.

[43] H. C. de Graaff and M. T. M. Huybers, “1/f noise in polycrystalline silicon resistor,” *J. Appl. Phys.*, vol. 54, no. 5, pp. 2504-2507, May 1983.

[44] A. L. McWhorter, *Semiconductor Surface Physics*. Philadelphia, PA: Univ. Oklahoma Press, 1957.

[45] D. Lovelace, J. Costa, and N. Camilleri, “Extracting small-signal model parameters of silicon MOSFET transistors,” in *IEEE MTT-S International Microwave Symposium Dig.*, 1994, pp. 865-868.

[46] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, “A new method for determining the FET small-signal equivalent circuit,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 7, pp. 1151-1159, 1988.

[47] S. C. Wang, P. Su, K. M. Chen, C. T. Lin, V. Liang, and G. W. Huang, “On the RF extrinsic resistance extraction for partially-depleted SOI MOSFETs,” *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 5, pp. 364-366, 2007.

[48] S. Lee, H. K. Yu, C. S. Kim, J. G. Koo, and K. S. Nam, “A novel approach to extracting small-signal model parameters of silicon MOSFET's,” *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 3, pp. 75-77, 1997.

[49] S. H. M. Jen, C. C. Enz, D. R. Pehlke, M. Schroter, and B. J. Sheu, “Accurate modeling and parameter extraction for MOS transistors valid up to 10 GHz,” *IEEE Trans. Electron Devices*, vol. 46, no. 11, pp. 2217-2227, 1999.

Table 5-1 Hall measurement results of poly-Si films.

PH_3 (sccm)	Resistivity (Ω-cm)	Hall mobility (cm^2/V-s)	Concentration (cm^{-3})
10	0.00267	24.4	9.586×10^{19}
100	0.000472	19.4	6.797×10^{20}

Table 5-2 Splits of JL NW SONOS devices with various gate configuration and channel doping.

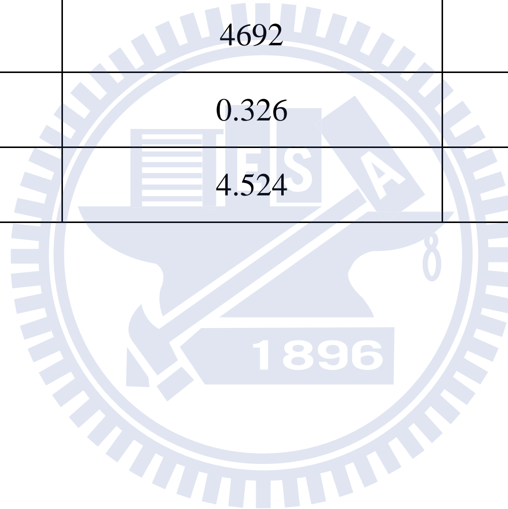
	Gate-all-around	Ω-gate
Heavier doping (PH_3 = 30sccm)	GAA-H	Ω-H
Lighter doping (PH_3 = 15sccm)	GAA-L	Ω-L

Table 5-3 Performance comparison of the fabricated JL and IM poly-Si TFTs with W/L=8 μm/0.4 μm.

	JL(W/L=8 μm/0.4 μm)	IM(W/L=8 μm/0.4 μm)
S.S. (mV/dec)	309	305
DIBL (mV/V)	161	143
V_{th} (V)	-0.19	1.6
G_{msat} (μS/μm)	23.89	3.01
I_{on}/I_{off}	8 × 107	1 × 107
f_t (GHz)	3.36	0.51
f_{max} (GHz)	7.37	1.47
S_{id} (A^2/Hz)@10Hz	5×10^{-21}	3×10^{-18}

Table 5-4 Summary of the small-signal parameters of fabricated JL and IM poly-Si TFTs with W/L=8 μm/0.4 μm.

	JL(W/L=8 μm/0.4 μm)	IM(W/L=8 μm/0.4 μm)
R_g(Ω)	333	349
R_d(Ω)	343	400
R_s(Ω)	50	60
C_{gs}(fF)	9.675	10.5
C_{gd}(fF)	4.672	7.165
C_{ds}(fF)	2.645	1.531
r_o(Ω)	4692	41429
g_m(mS)	0.326	0.049
τ(psec)	4.524	34.332



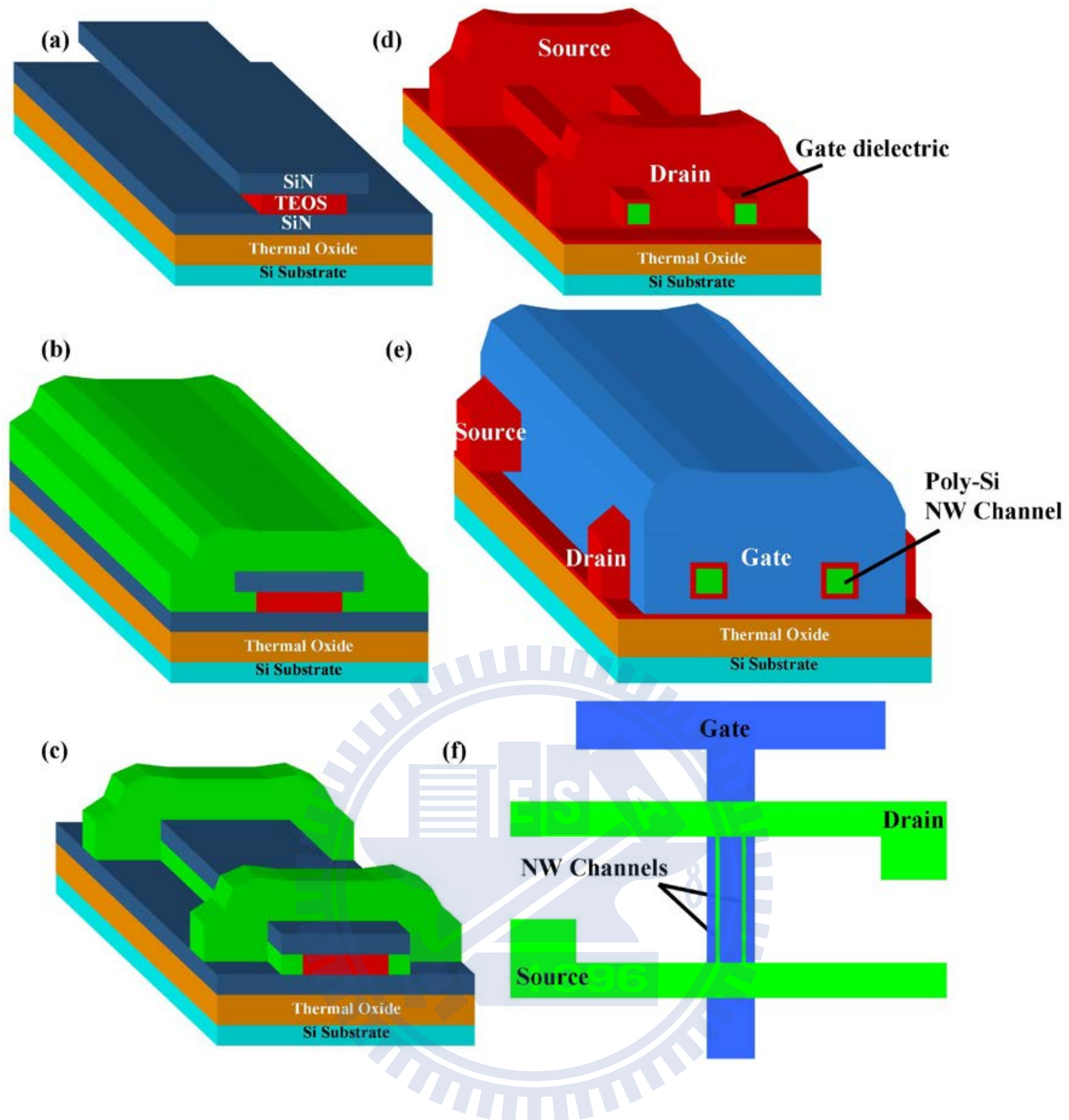


Fig. 5-1 Key fabrication process flow of the proposed GAA JL NWFET. (a) Deposition and patterning of a sandwich stack of nitride/TEOS oxide/nitride layers on Si substrate capped with 200-nm-thick wet oxide, followed by selective lateral etching of TEOS oxide layer using DHF to form sub-100-nm cavity underneath both sides of the top nitride. (b) Deposition of an *in situ* phosphorus-doped poly-Si layer. (c) Simultaneous definition of NW doped channels and S/D regions. (d) Etching of the nitride and oxide, followed by the ALD deposition of the high-κ/metal gate stack structure (10-nm Al_2O_3 and 10-nm TiN). (e) Sputter deposition of another 140 nm TiN film to make a final gate electrode of 150 nm. (f) Schematic top-view layout of the device.

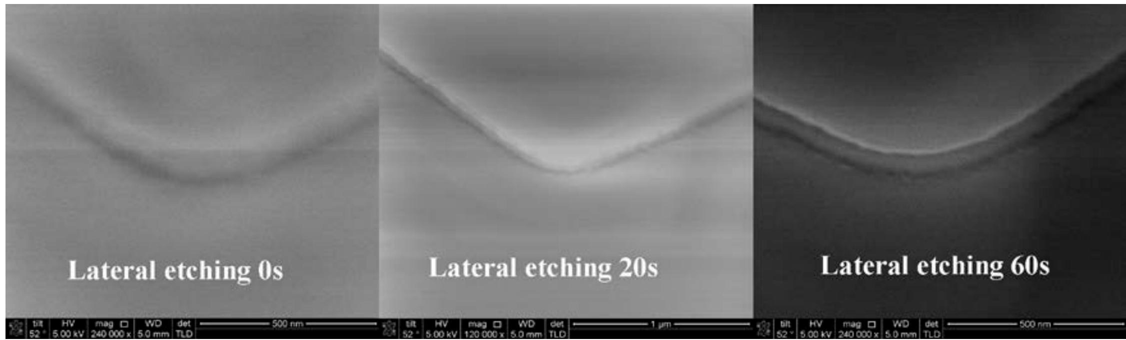


Fig. 5-2 Tilted scanning electron microscopic (SEM) images before and after cavity formation.

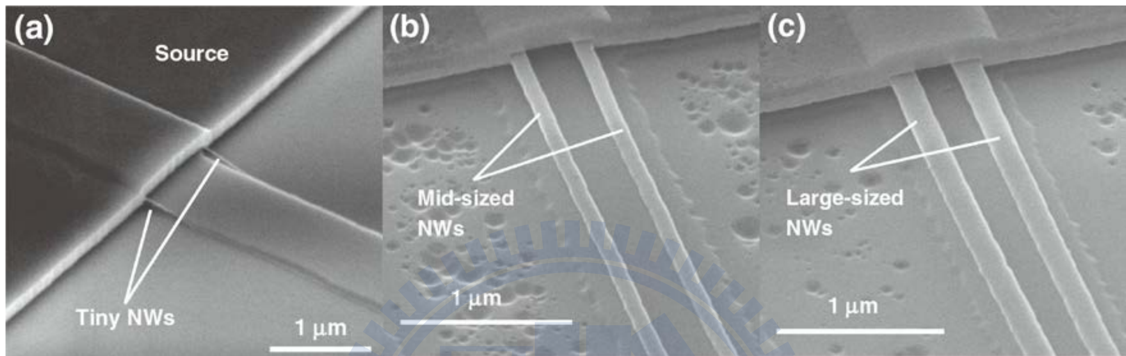


Fig. 5-3 Tilted SEM images of different-sized NW devices before the gate stack formation. (a) A tiny NW device showing NWs exposed on both sides of the temporary dielectric step, (b) a mid-sized NW device, and (c) a large-sized NW device.

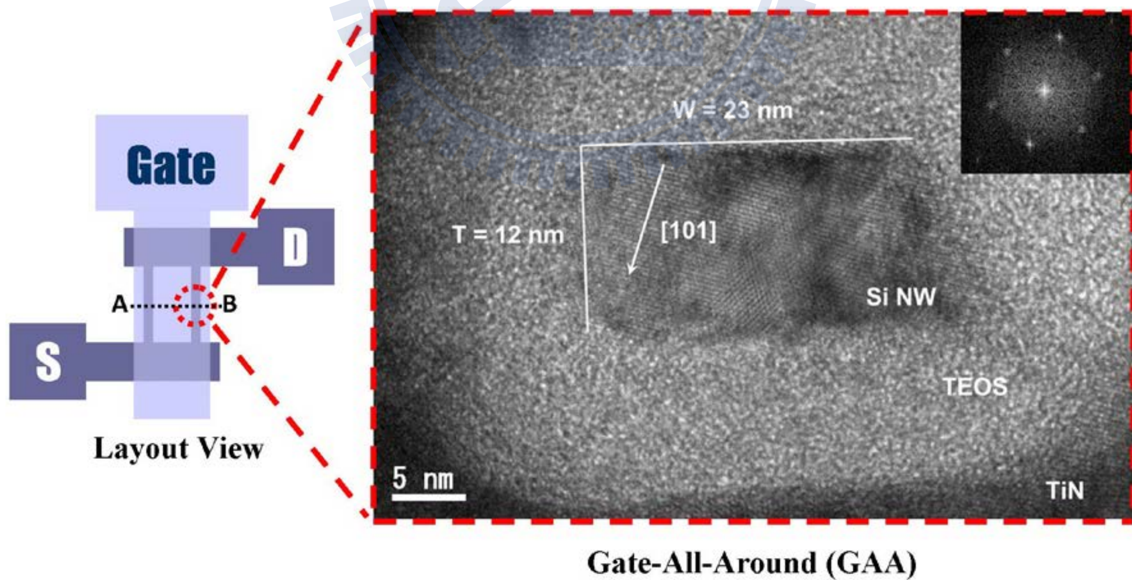


Fig. 5-4 Cross-sectional HRTEM image of a fabricated GAA JL NWFET with the TEOS oxide/TiN gate stack. A NW size is around of 12 nm in thickness (T) and 23 nm in width (W). The inset is the corresponding diffraction pattern of the NW, revealing the monocrystalline structure of the grain with [110] orientation.

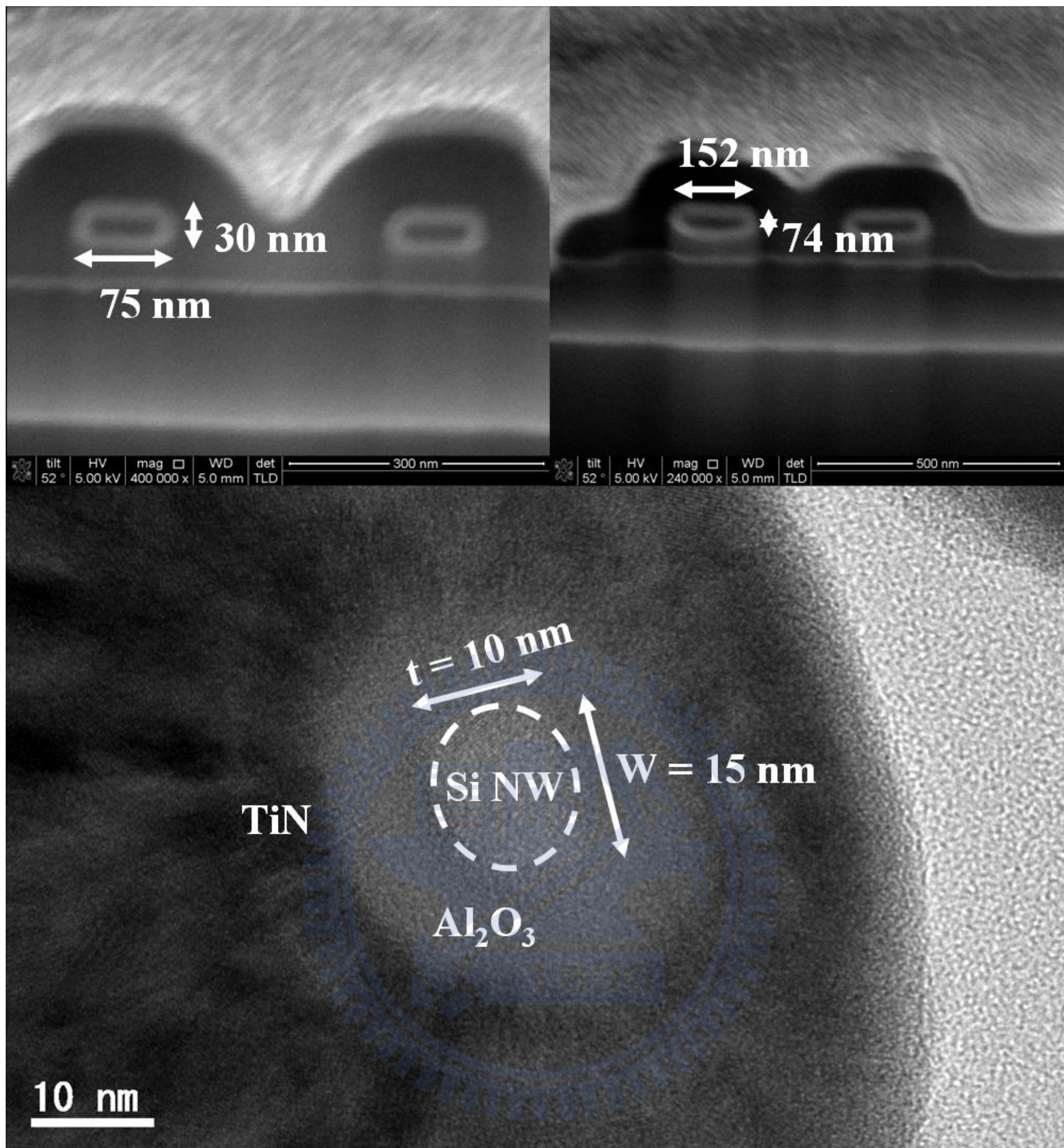


Fig. 5-5 TEM and tilted SEM images of fabricated JL devices. (a) Cross-sectional TEM image of a JL device with tiny NW covered with Al_2O_3/TiN GAA stack. 52° tilted SEM images of a mid-sized JL device with a NW cross section of 75 × 30 nm and a large-sized JL device with a NW cross section of 152 × 74 nm.

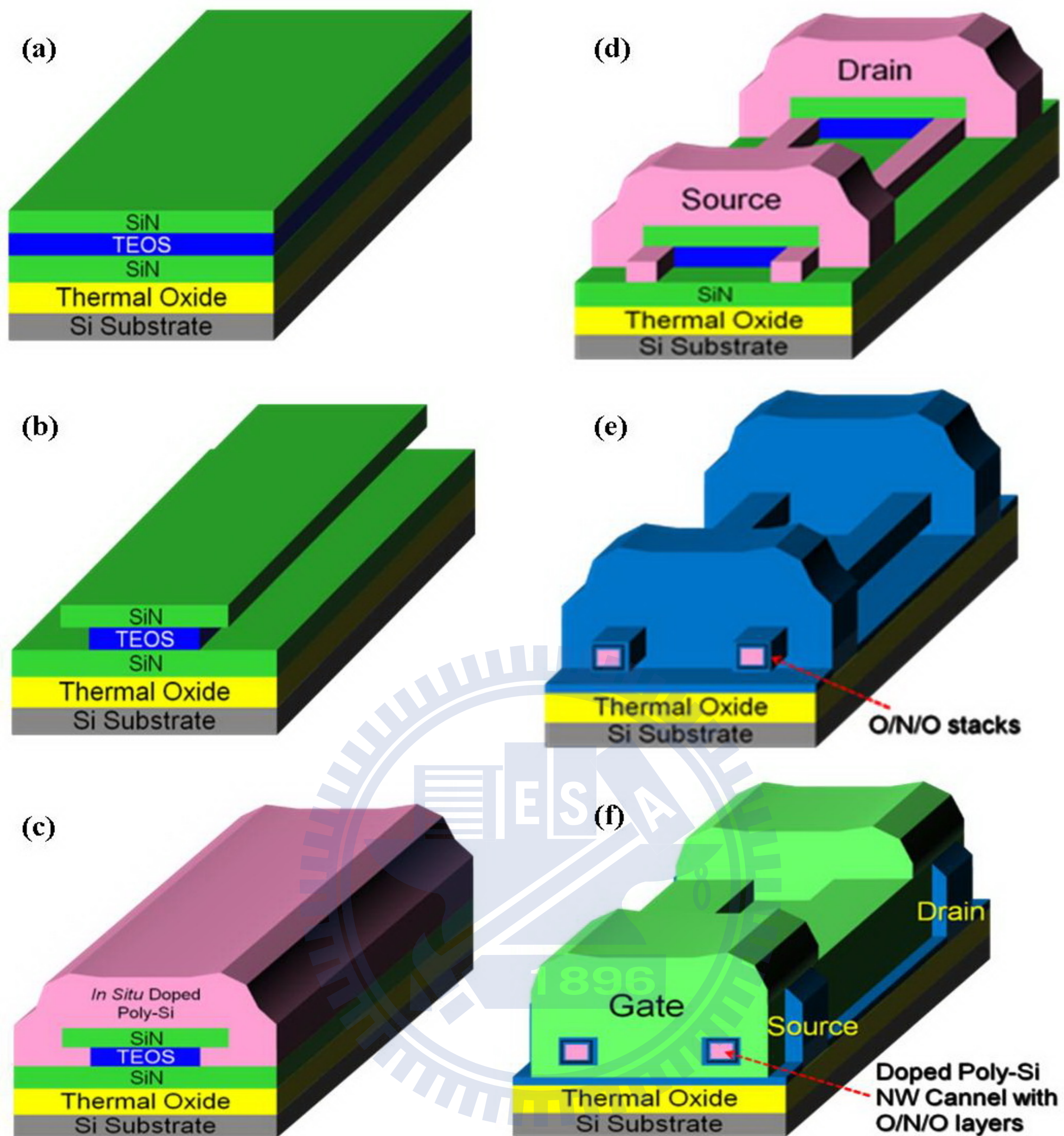


Fig. 5-6 Key fabrication process flow of the proposed GAA JL NW SONOS memory device. (a) Deposition and patterning of a sandwich stack of nitride/TEOS oxide/nitride layers on Si substrate capped with 200-nm-thick wet oxide. (b) Selective lateral etching of TEOS oxide using DHF to form a sub-100-nm cavity underneath both sides of the top nitride. (c) Deposition of an *in situ* phosphorus-doped poly-Si layer. (d) Simultaneous definition of the NW doped channels and S/D regions, followed by etching off the nitride and oxide surrounding the NW channels. (e) LPCVD deposition of gate dielectric stack of blocking oxide/trapping nitride/tunneling oxide (ONO) with thicknesses of 12/7/3 nm. (f) Deposition and patterning of an *in situ* phosphorous doped n^+-poly-Si layer as the gate electrode.

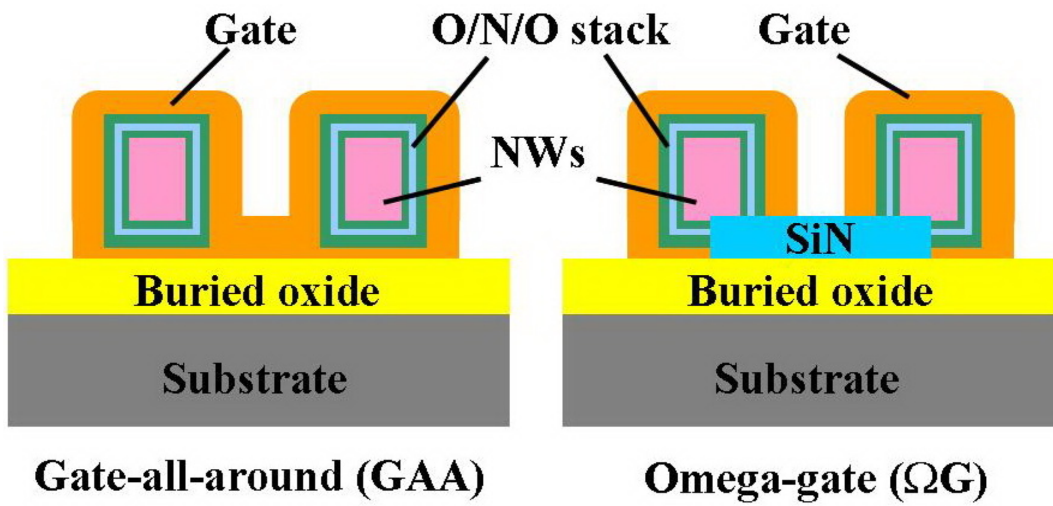


Fig. 5-7 Schematic illustrations of gate structures (GAA/Ω-gate) implemented in our JL-SONOS memory cells.

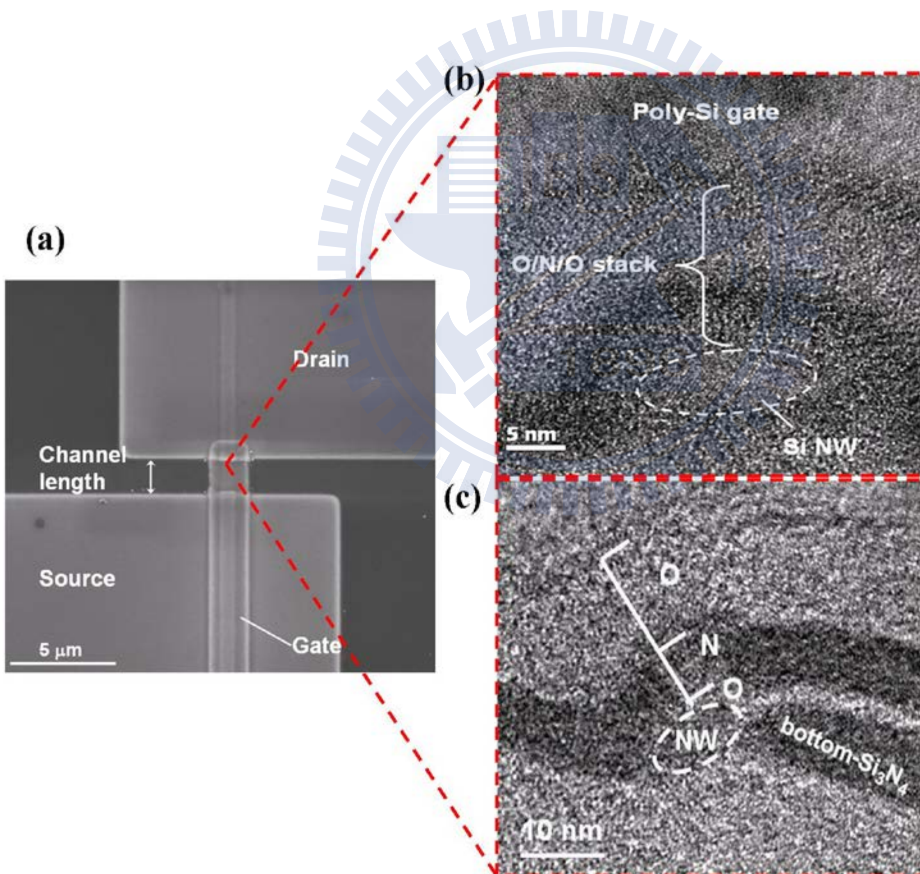


Fig. 5-8 (a) Top-view SEM and cross-sectional TEM images of the NW channel with (b) GAA and (c) Ω-gate structures.

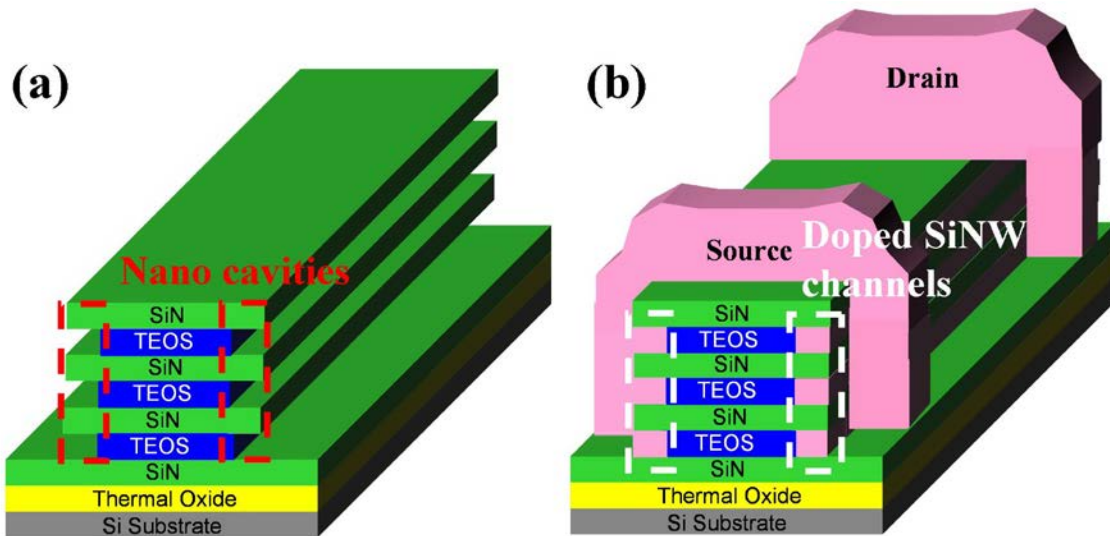


Fig. 5-9 Illustration of the key steps for building 3-D multilayer stacked JL poly-Si NW device. (a) Formation of sub-100 nm cavities. (b) Formation of channel and S/D.

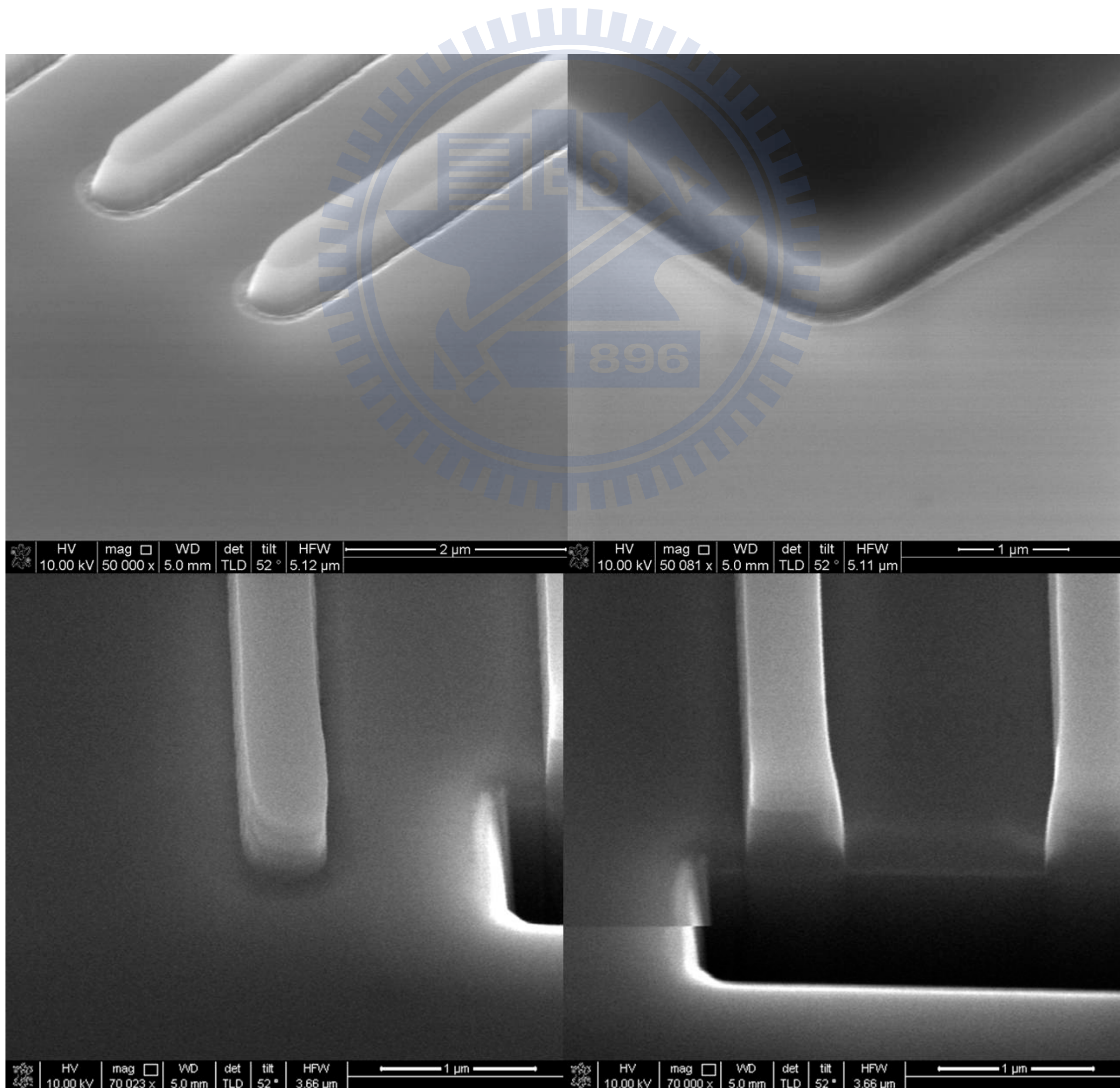


Fig. 5-10 Tilted SEM images of anisotropically-etched dummy patterns.

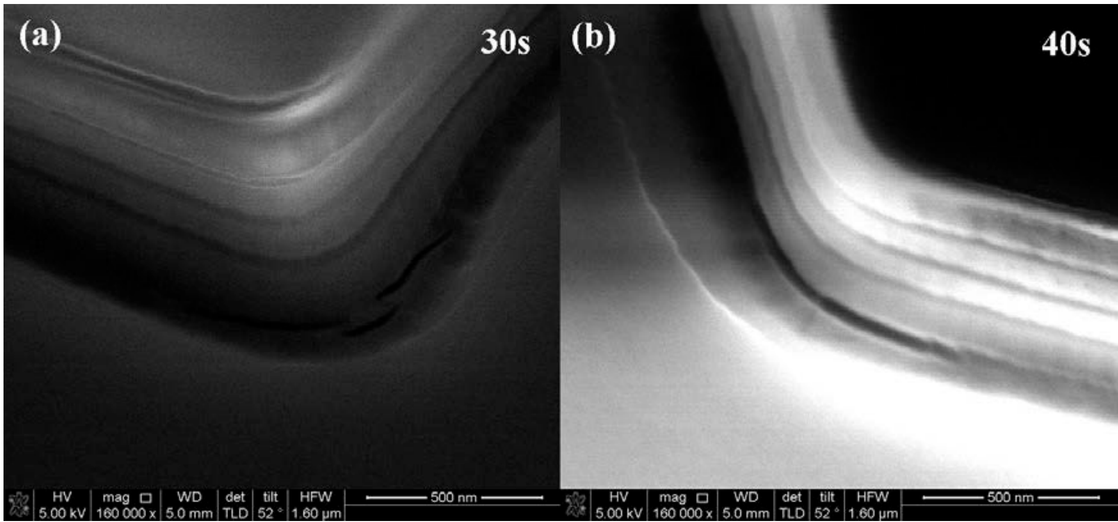


Fig. 5-11 Overhead-view SEM images of the nano-cavities with (a) 30- and (b) 40-second lateral-etching time.

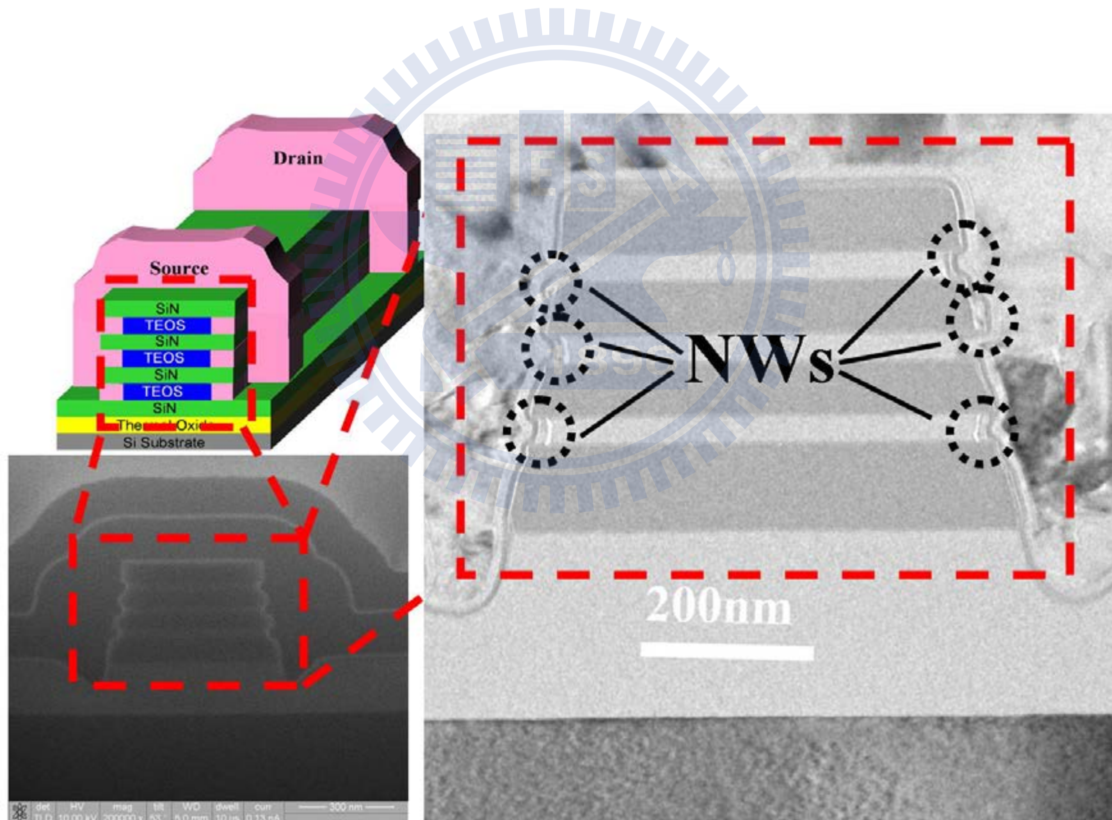


Fig. 5-12 Cross-sectional TEM images of fabricated 3-D stacked JL NW memory device.

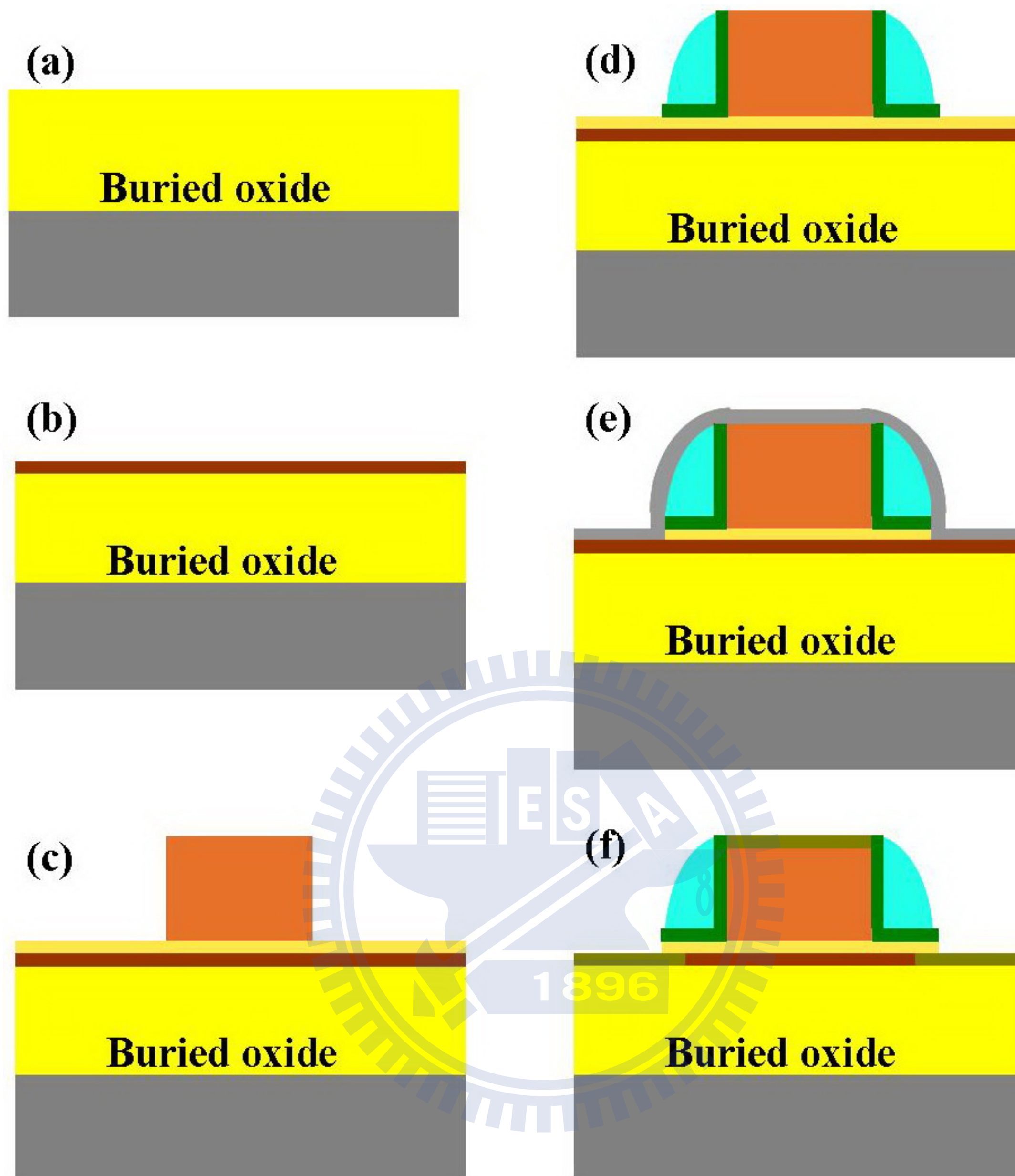


Fig. 5-13 Key fabrication process flow of the proposed planar JL poly-Si TFT. (a) Growth of 1000-nm-thick oxide by wet oxidation on a six-in silicon substrate as the buried oxide. (b) Deposition of a 9-nm-thick *in situ* phosphorous doped n^+-poly-Si layer as the channel layer. (c) Successive depositions of a 13-nm TEOS oxide as the gate dielectric and a 200-nm *in situ* n^+-poly-Si as the gate electrode, followed by the gate pattern definition. (d) Formation of sidewall spacers (20-nm TEOS oxide layer and 20-nm nitride layer). (e) Depositions of a 5-nm-thick nickel layer and a 15-nm-thick titanium nitride layer. (f) Annealing process for forming NiSi on the gate, and S/D regions.

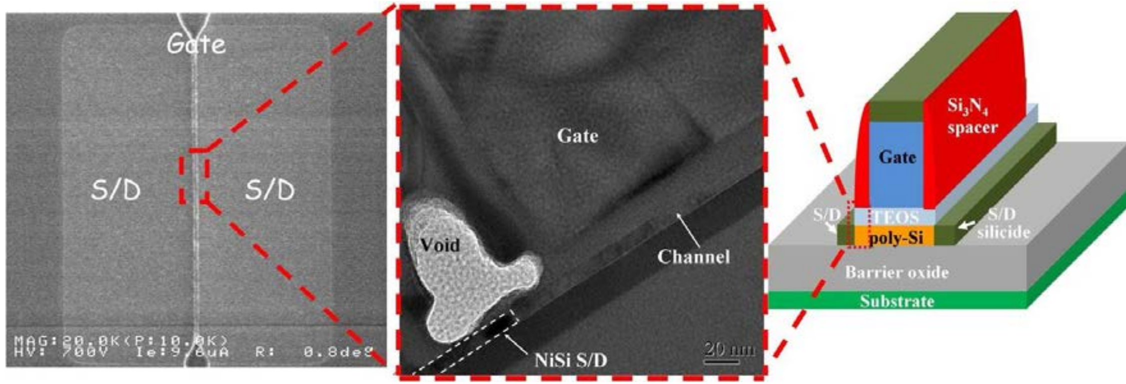


Fig. 5-14 Top-view SEM and cross-sectional TEM images of the fabricated planar JL poly-Si TFT.

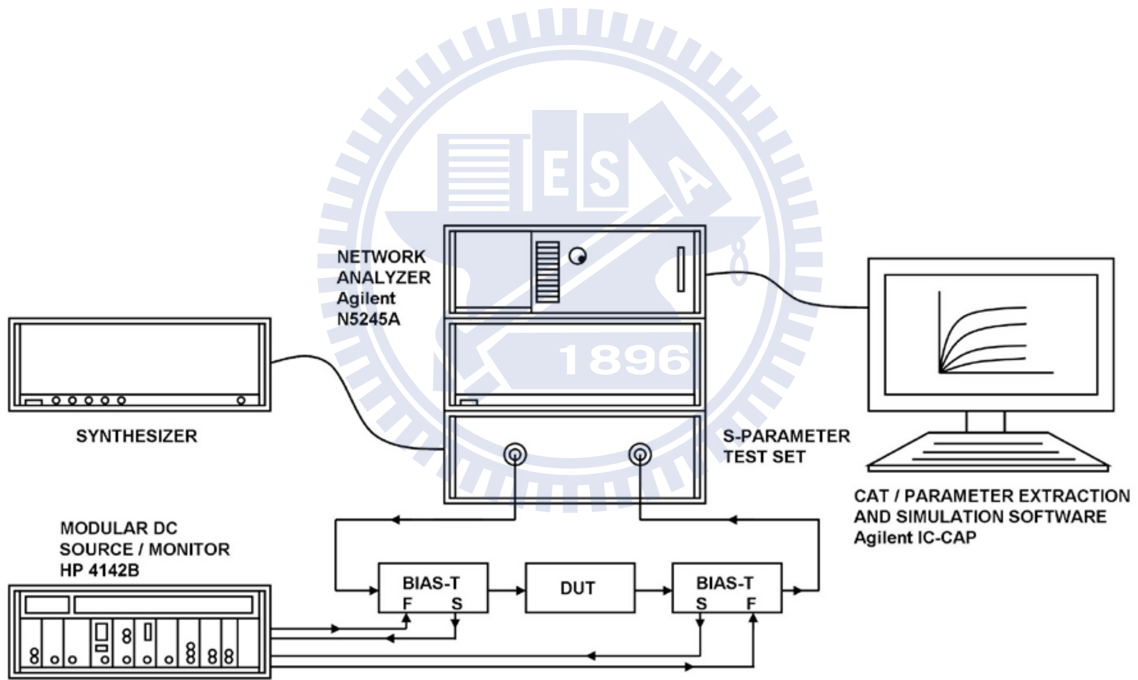


Fig. 5-15 *S*-parameter measurement system.

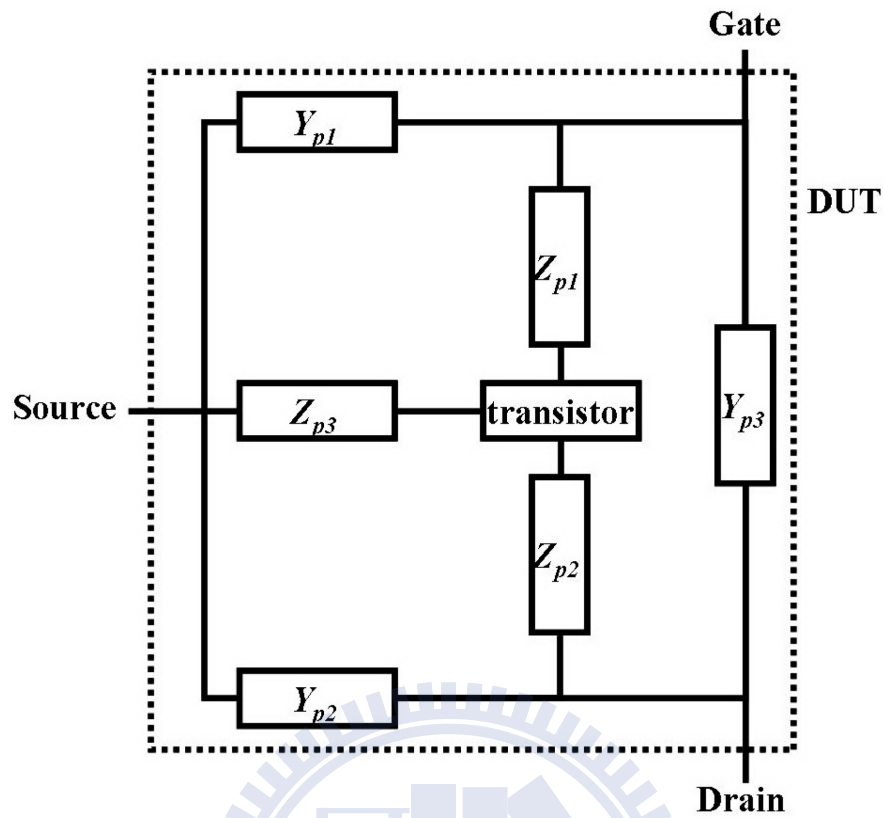


Fig. 5-16 Equivalent circuit diagram used for the two-step correction including parasitic effect.

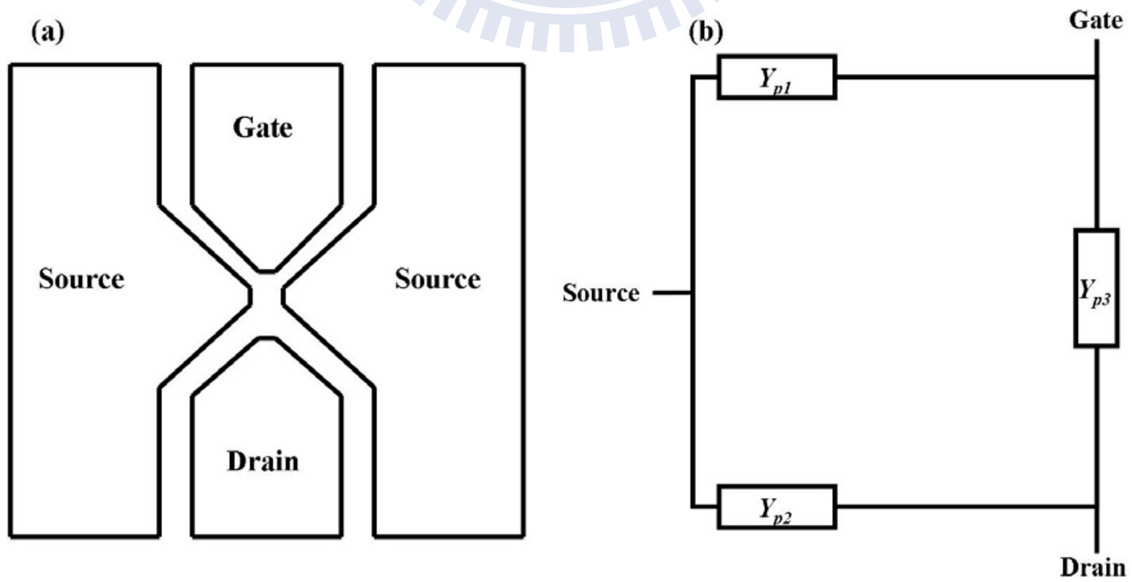


Fig. 5-17 (a)The open test fixture and (b) the diagram of equivalent circuit.

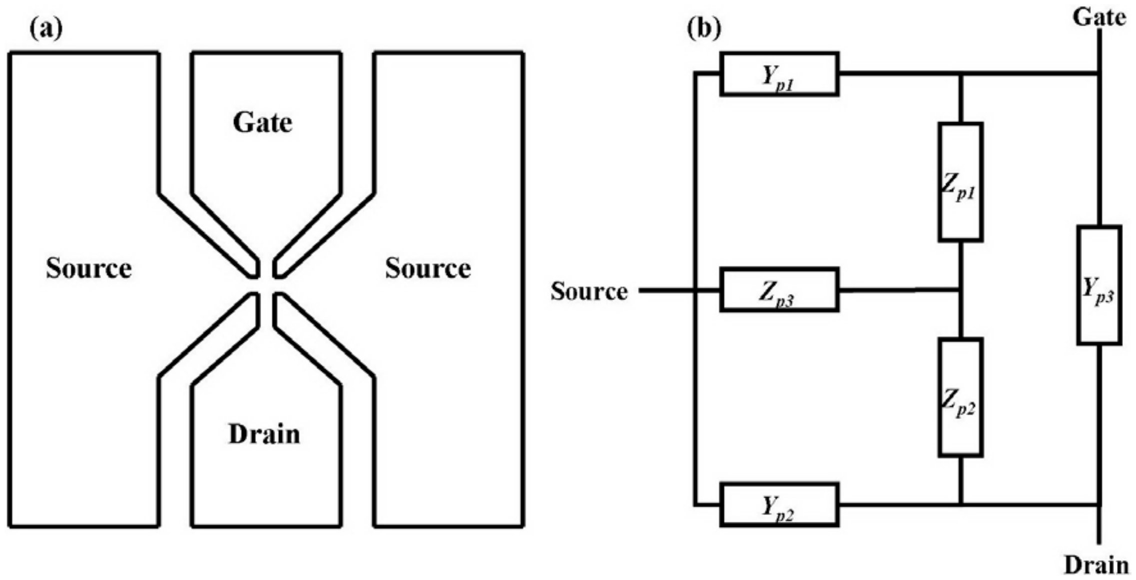


Fig. 5-18 (a)The short test fixture and (b) the diagram of equivalent circuit.

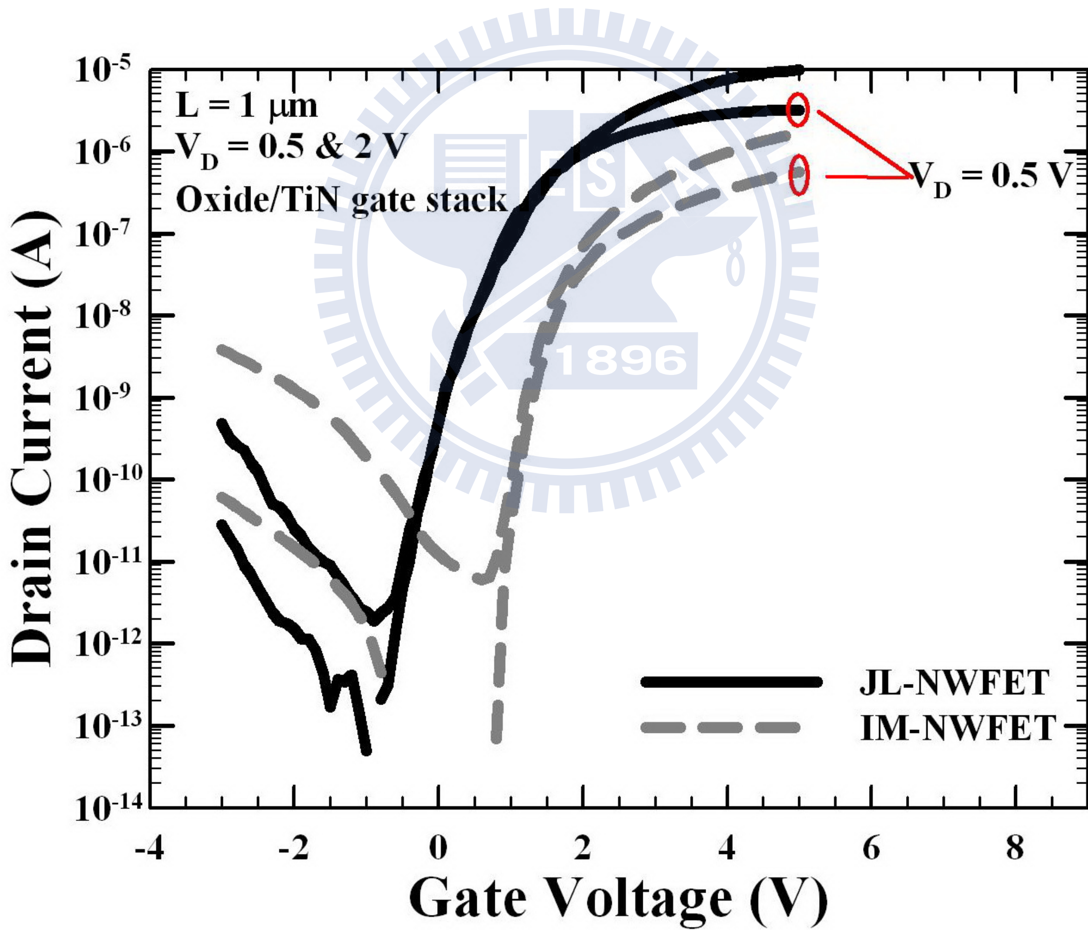


Fig. 5-19 Transfer characteristics of JL and IM NWFETs with an NW channel dimension of W/T = 23 nm/12 nm and a channel length (L) of 1 μm measured at V_D = 0.5 and 2 V.

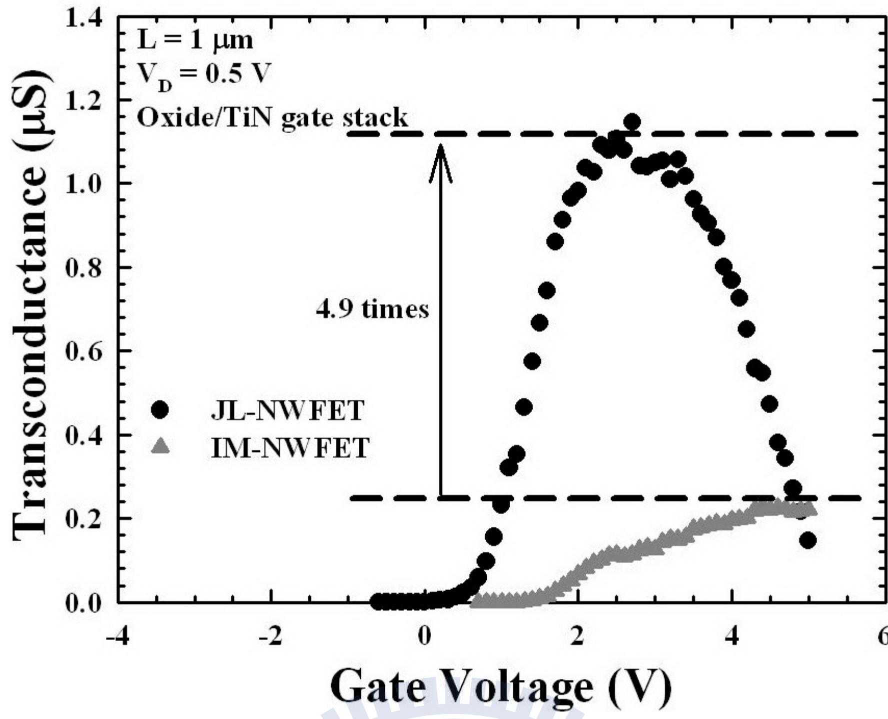


Fig. 5-20 Comparison of transconductance versus gate voltage for the JL and IM devices at $V_D = 0.5$ V.

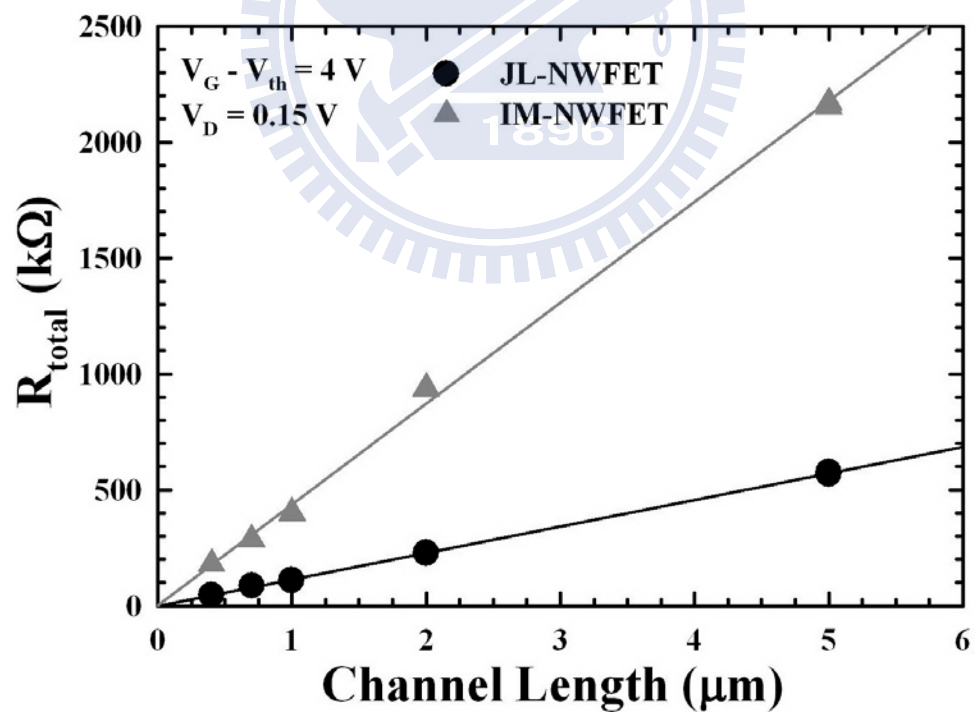


Fig. 5-21 Measured total resistance $R_{total} \equiv V_D/I_D = R_{SD} + R_{ch}$ versus channel length for JL and IM NWFETs measured at $V_G - V_{th}$ of 4 V and V_D of 0.15 V.

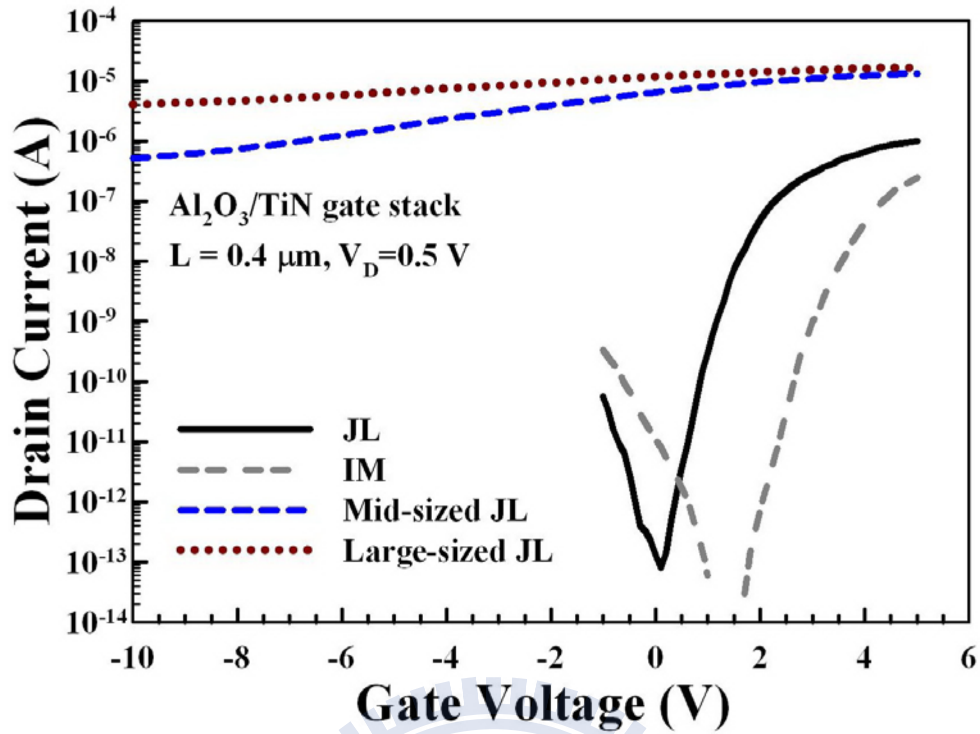


Fig. 5-22 Transfer characteristics of the JL and IM NW devices. Mid-sized (75 × 30 nm) and large-sized (152 × 74 nm) JL NW devices are also plotted for comparison. All devices characterized here are with channel length of 0.4 μm.

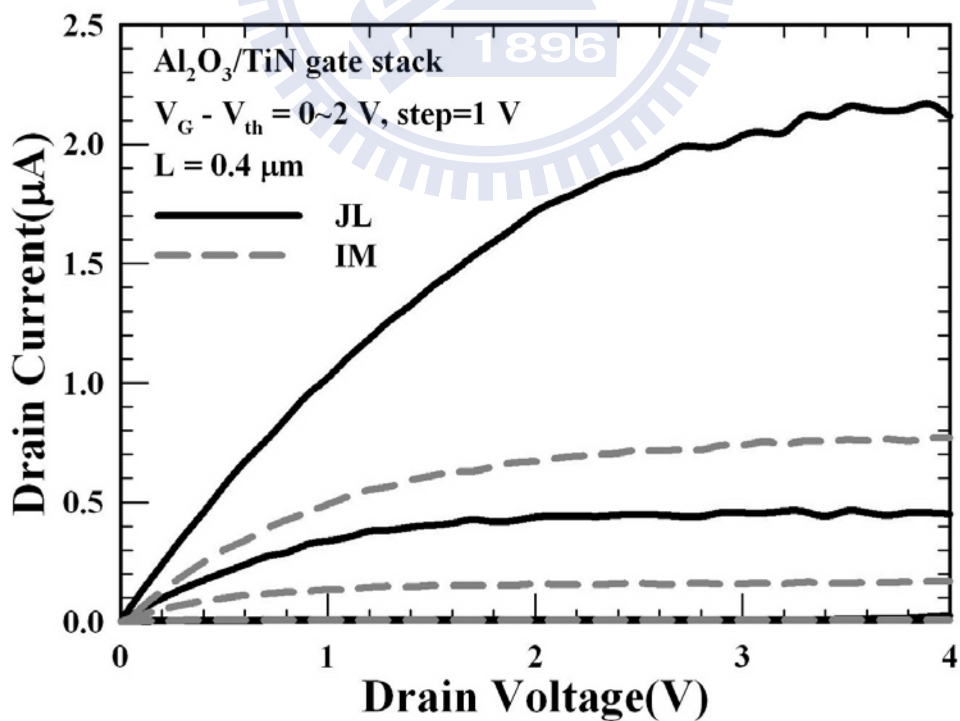


Fig. 5-23 Output characteristics of JL and IM splits measured at V_G - V_{th} = 0 ~ 2 V and step = 1 V with L = 0.4 μm.

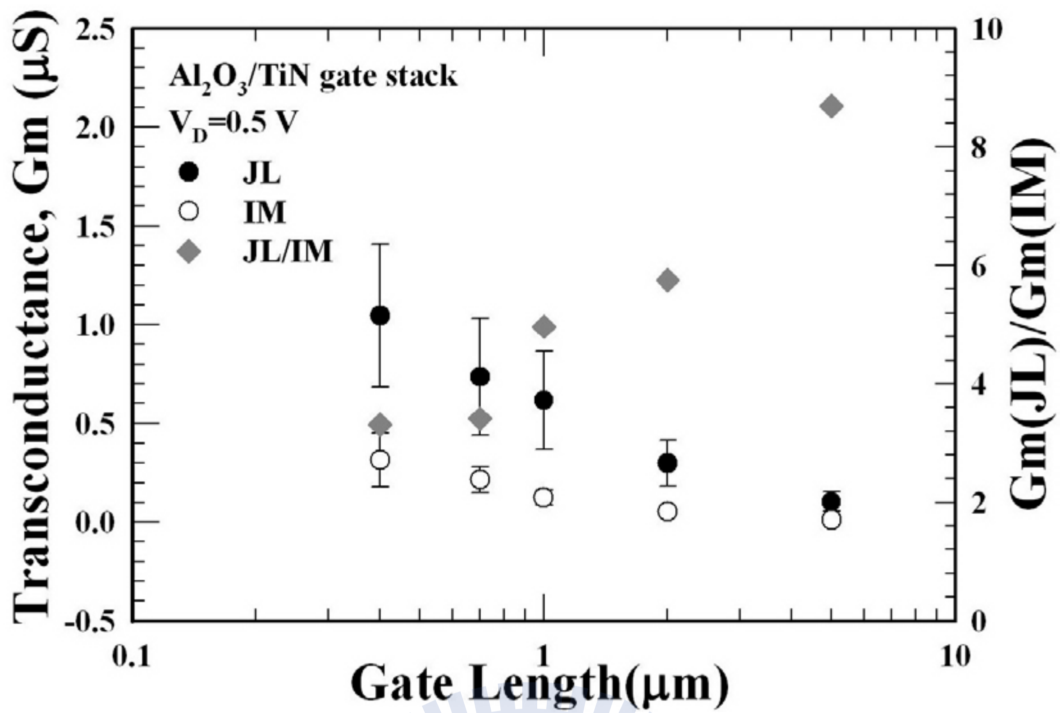


Fig. 5-24 Transconductance (Gm) and increments of Gm as a function of gate length for JL and IM splits measured at $V_D = 0.5$ V.

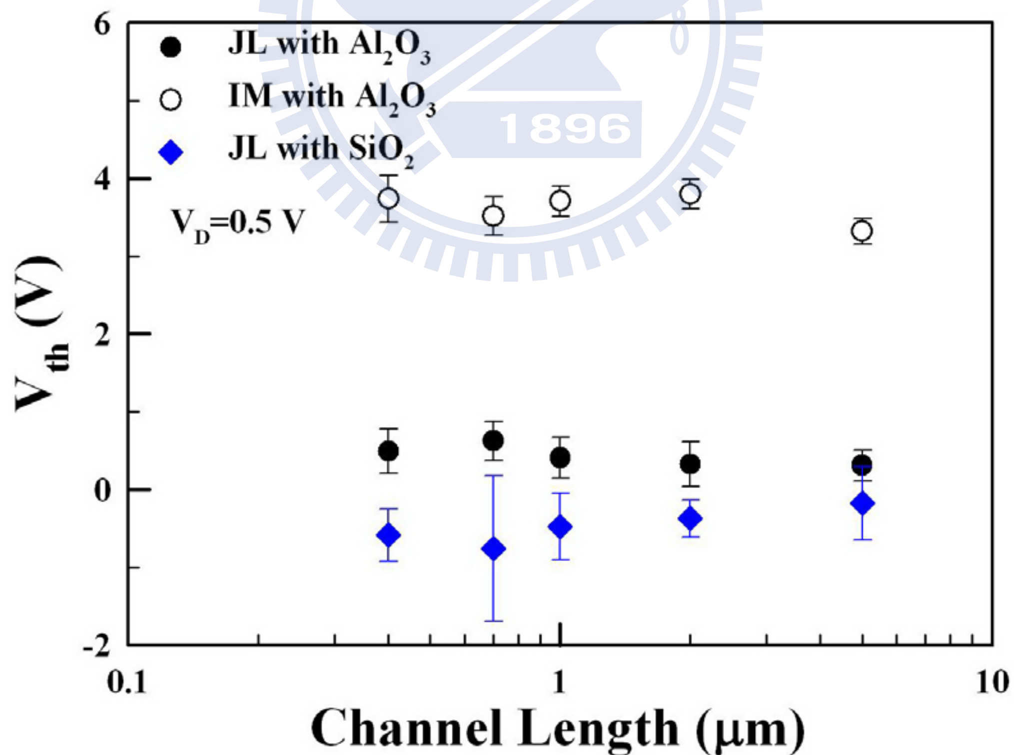


Fig. 5-25 Threshold voltage (V_{th}) as a function of gate length for JL and IM splits measured at $V_D = 0.5$ V.

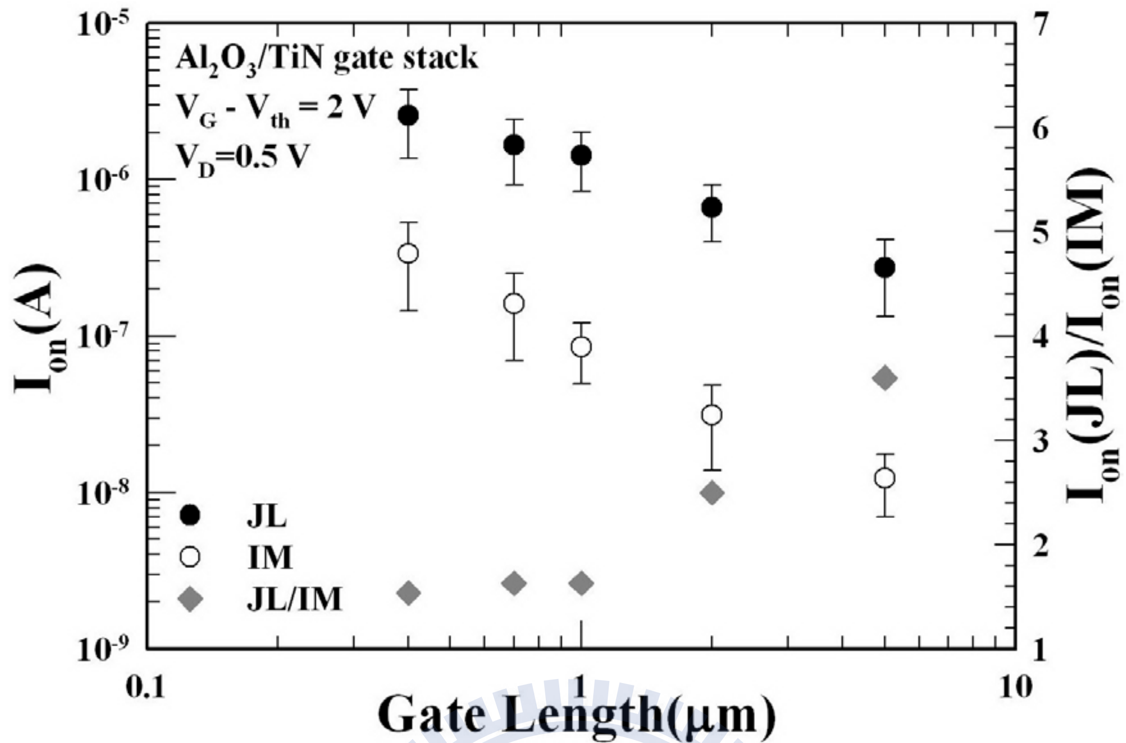


Fig. 5-26 On-state current (I_{on}) and increments of I_{on} as a function of gate length for JL and IM splits extracted at V_G - V_{th} = 2 V and V_D = 0.5 V.

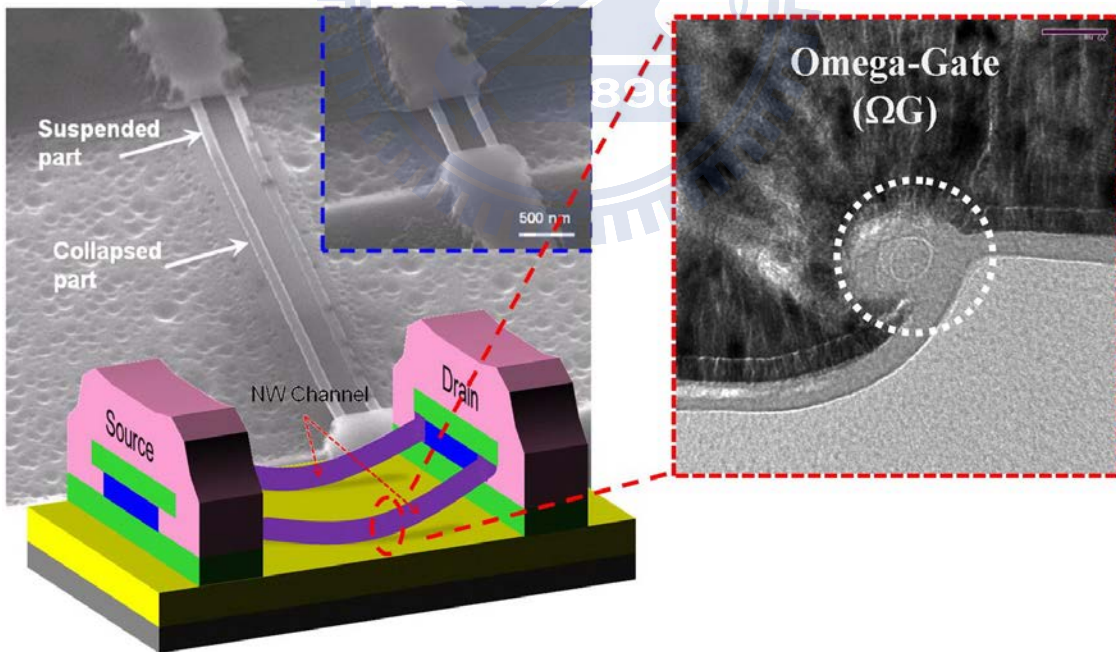


Fig. 5-27 Tilted SEM and cross-sectional TEM images of a fabricated GAA JL NWFET with L=5 μm showing collapse of NWs in the central channel region with an omega-shaped gate structure. The inset shows a NW device with L=1 μm depicting normal suspension of NWs between the S/D regions.

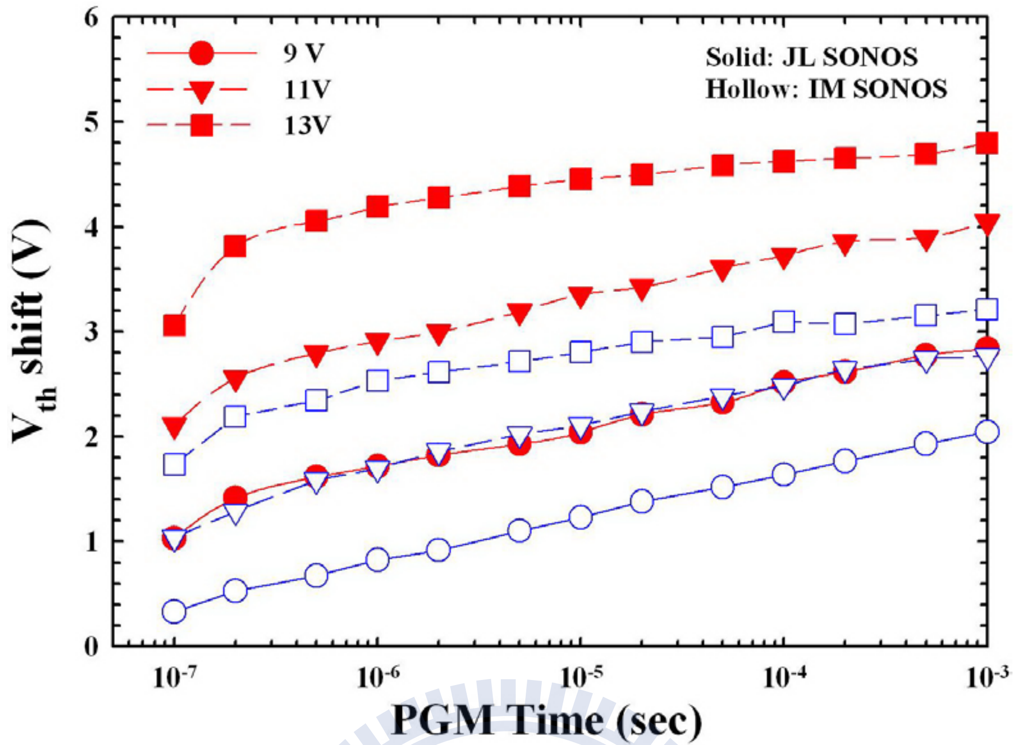


Fig. 5-28 Programming properties of the JL and IM NW SONOS devices at gate biases of 9, 11, and 13 V.

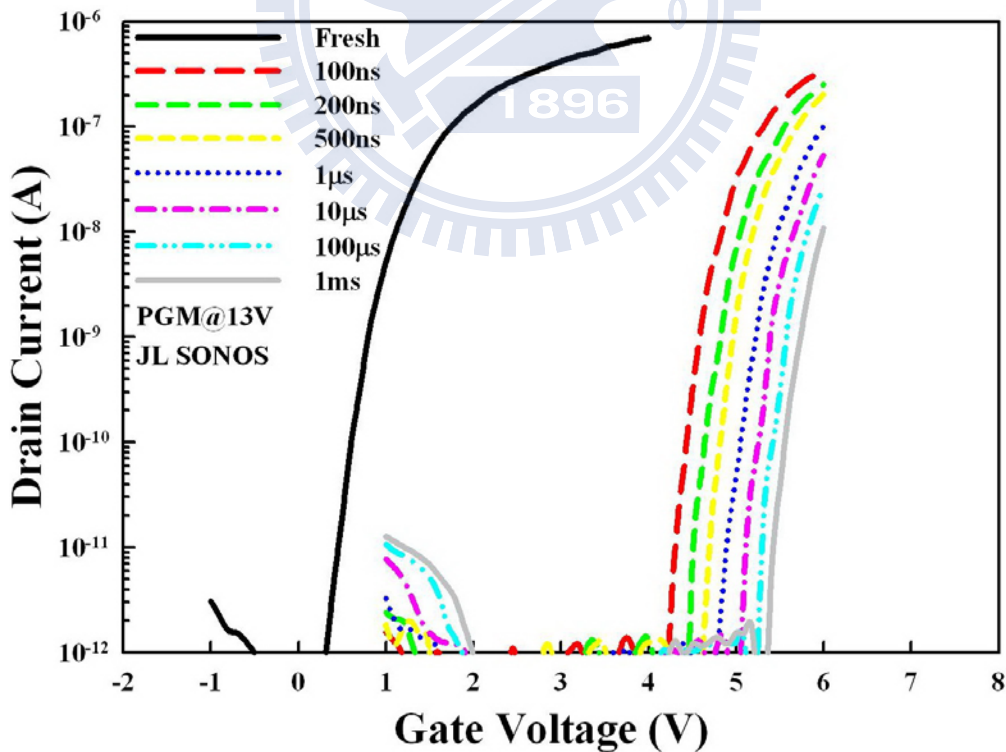


Fig. 5-29 Transfer characteristics of JL SONOS split in the programmed states biased at V_G = 13 V for various duration times.

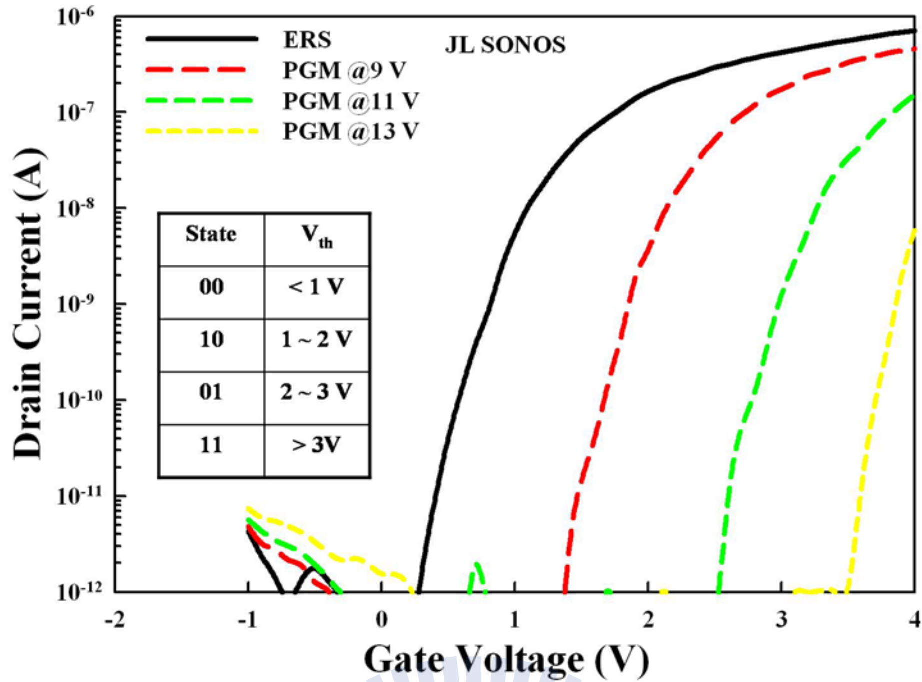


Fig. 5-30 Multilevel programming behavior of the JL NW device. Transfer characteristics of JL SONOS device with gate biases of 9, 11, and 13 V for 100 ns. Inset shows the definition of V_{th} range for each state.

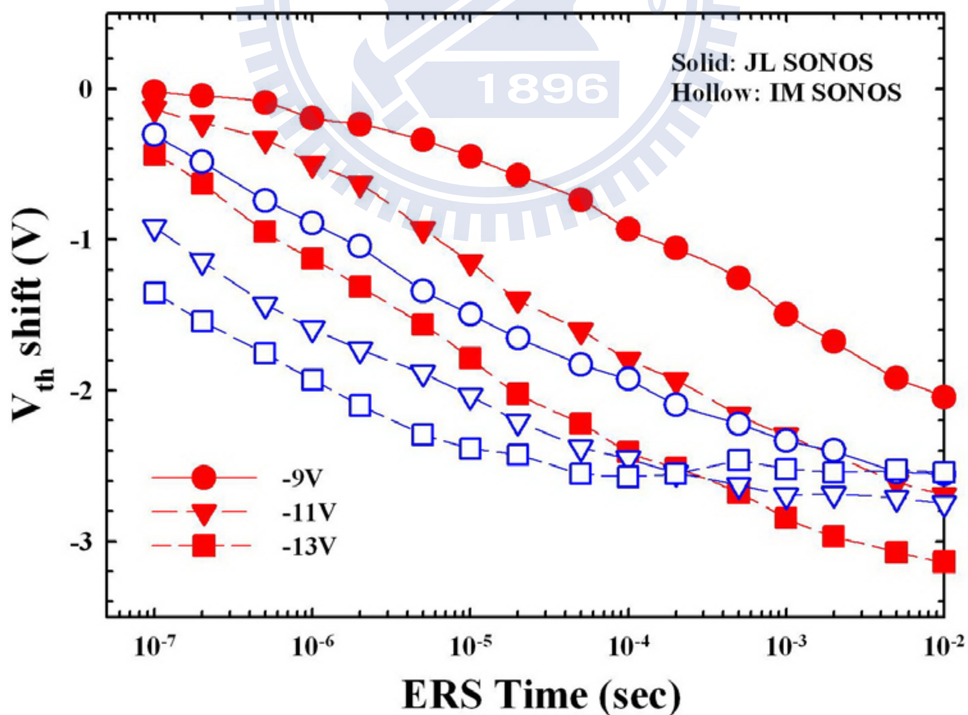


Fig. 5-31 Erasing properties of the JL and IM NW SONOS devices at gate biases of -9, -11, and -13 V. Before erasing, the cells were programmed to V_{th} shift of +3 V and +2.5 V for the JL and IM structures, respectively.

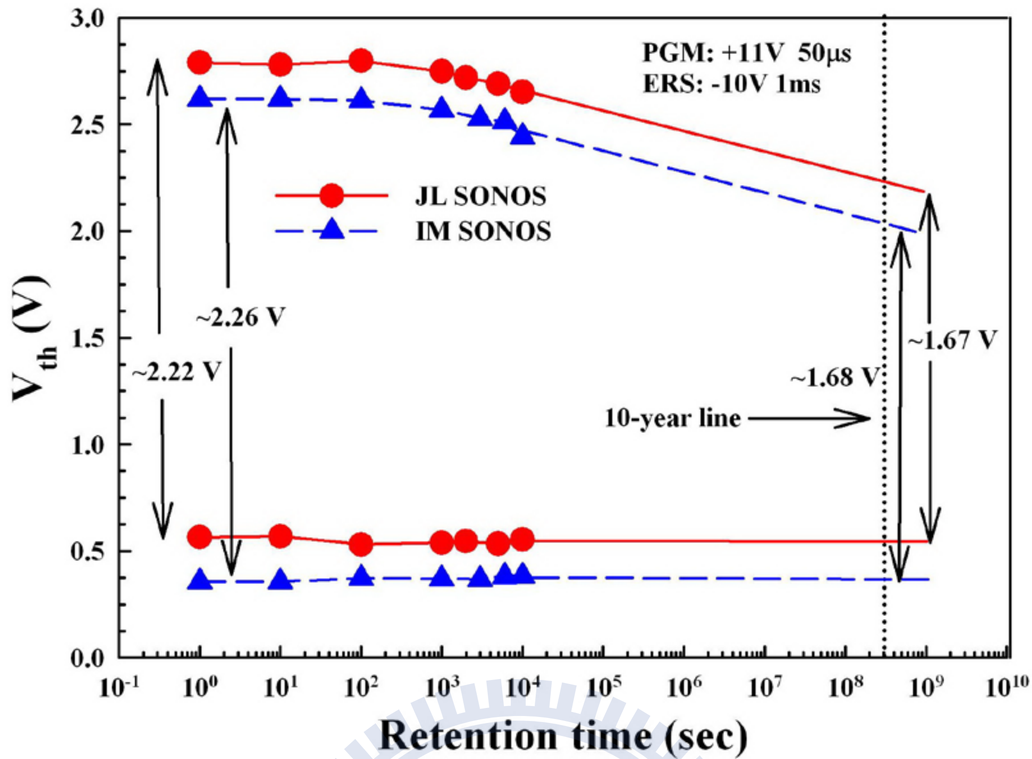


Fig. 5-32 Retention behaviors for the JL and IM NW SONOS devices at room temperature.

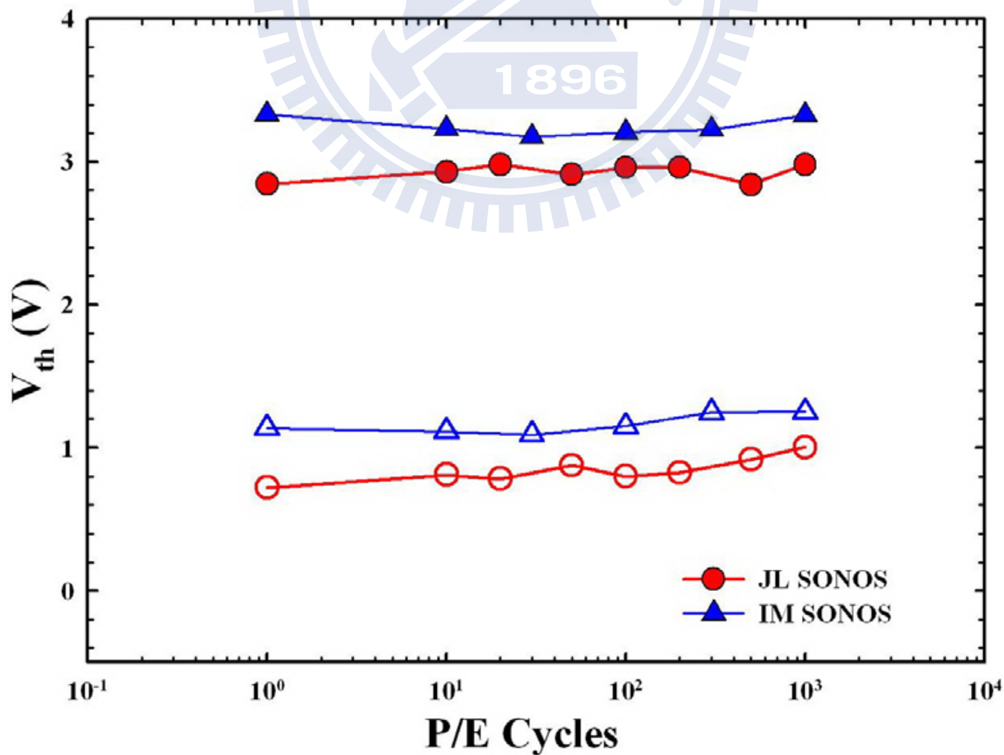


Fig. 5-33 Endurance behaviors for the JL and IM NW SONOS devices at room temperature.

1896

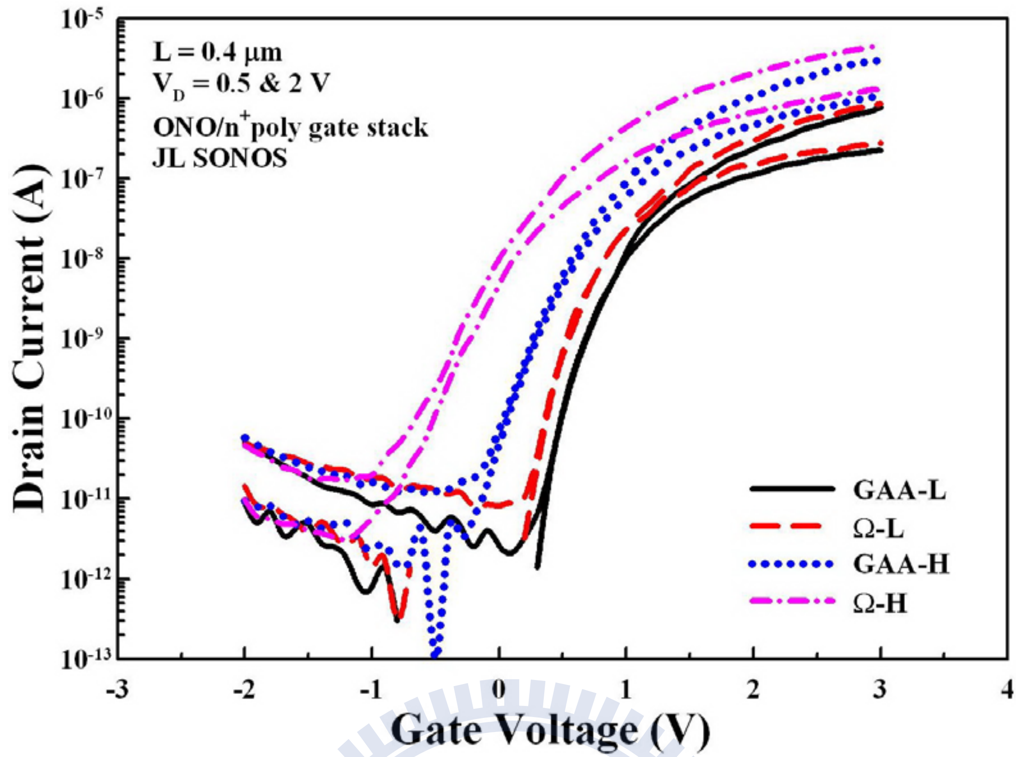


Fig. 5-34 Transfer characteristics of GAA-L, Ω-L, GAA-H and Ω-H JL NW SONOS devices measured at V_D = 0.5 and 2 V.

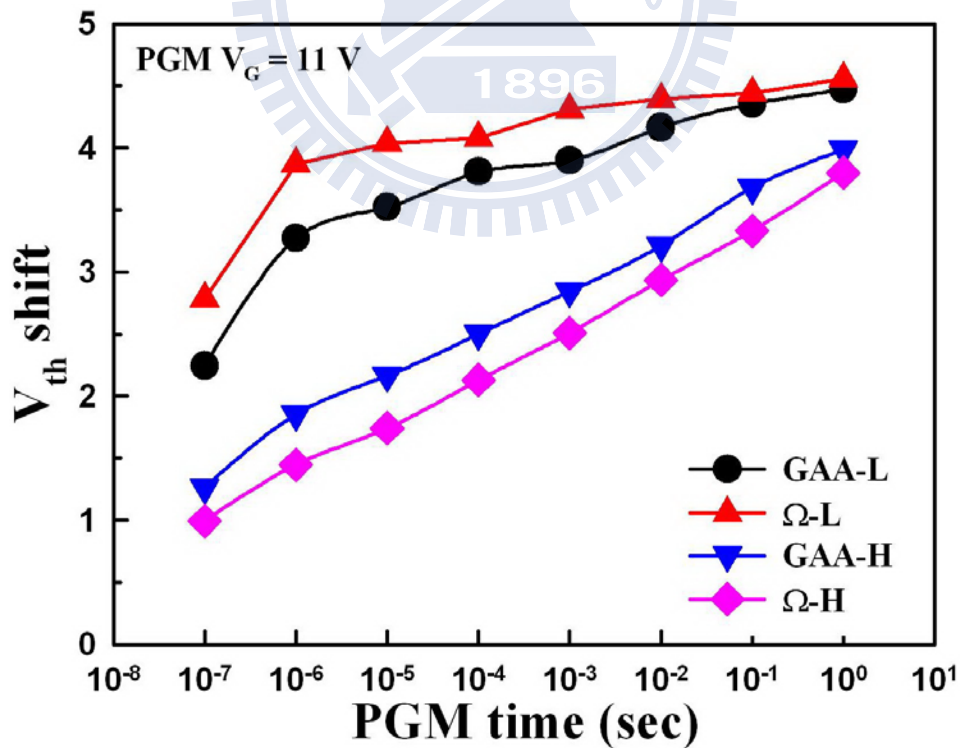


Fig. 5-35 Programming behaviors for GAA-L, Ω-L, GAA-H and Ω-H JL NW SONOS devices. The programming gate bias is 11 V.

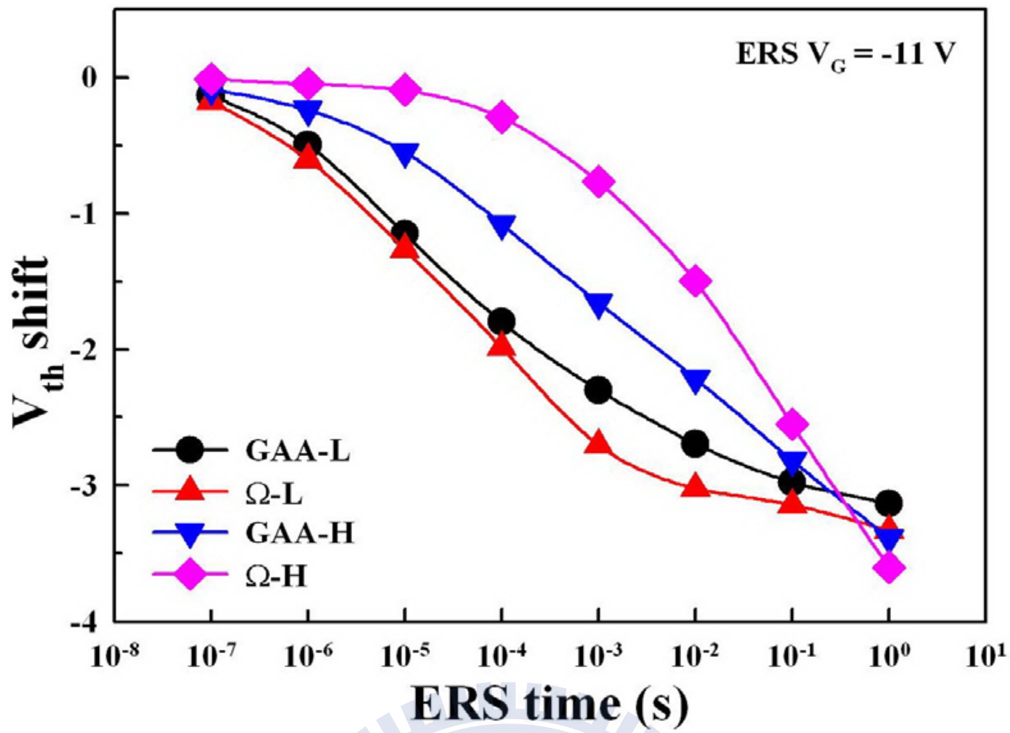


Fig. 5-36 Erasing behaviors for GAA-L, Ω-L, GAA-H and Ω-H JL NW SONOS devices. The Erasing gate bias is -11 V.

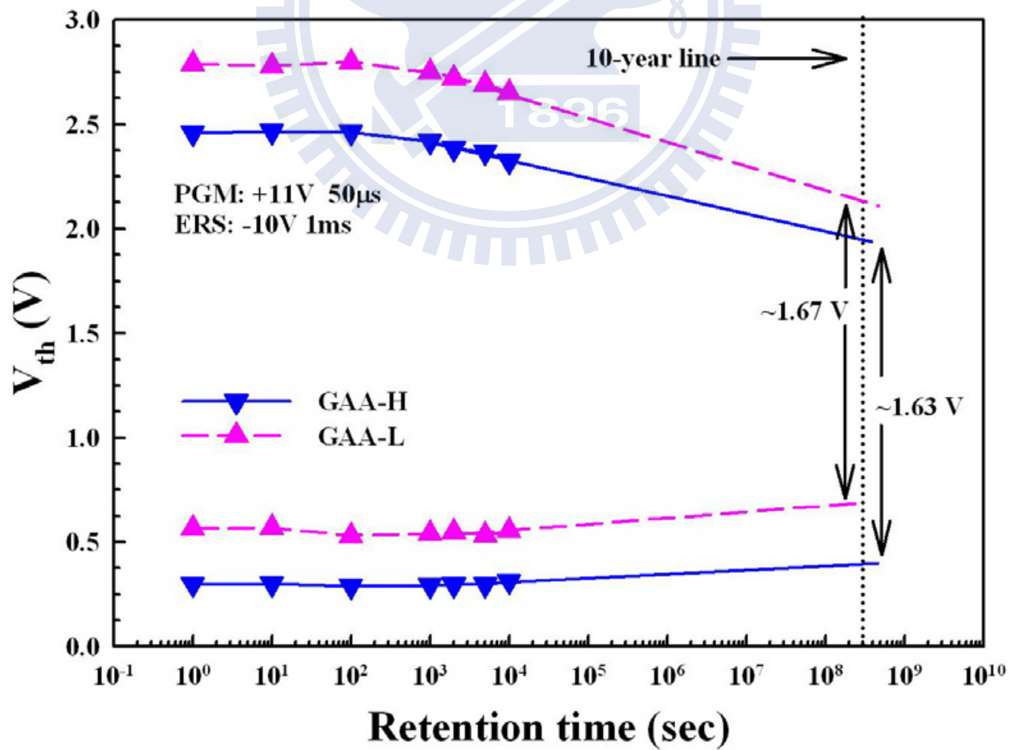


Fig. 5-37 Retention behaviors for the GAA-L and GAA-H JL NW SONOS devices at room temperature.

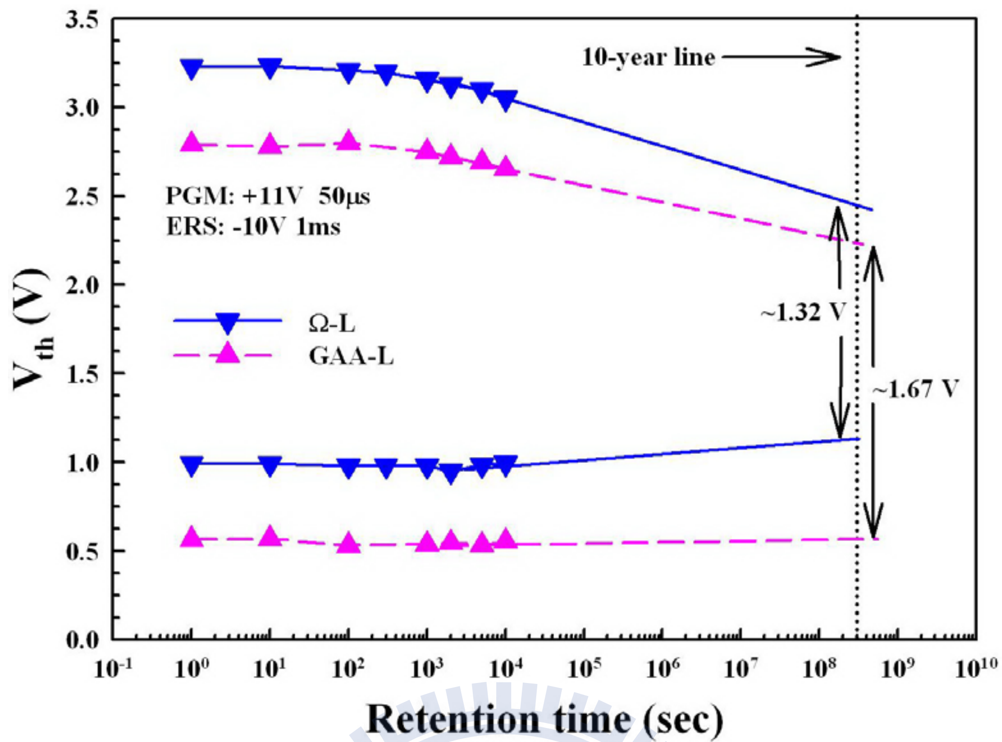


Fig. 5-38 Retention behaviors for the Ω-L and GAA-L JL NW SONOS devices at room temperature.

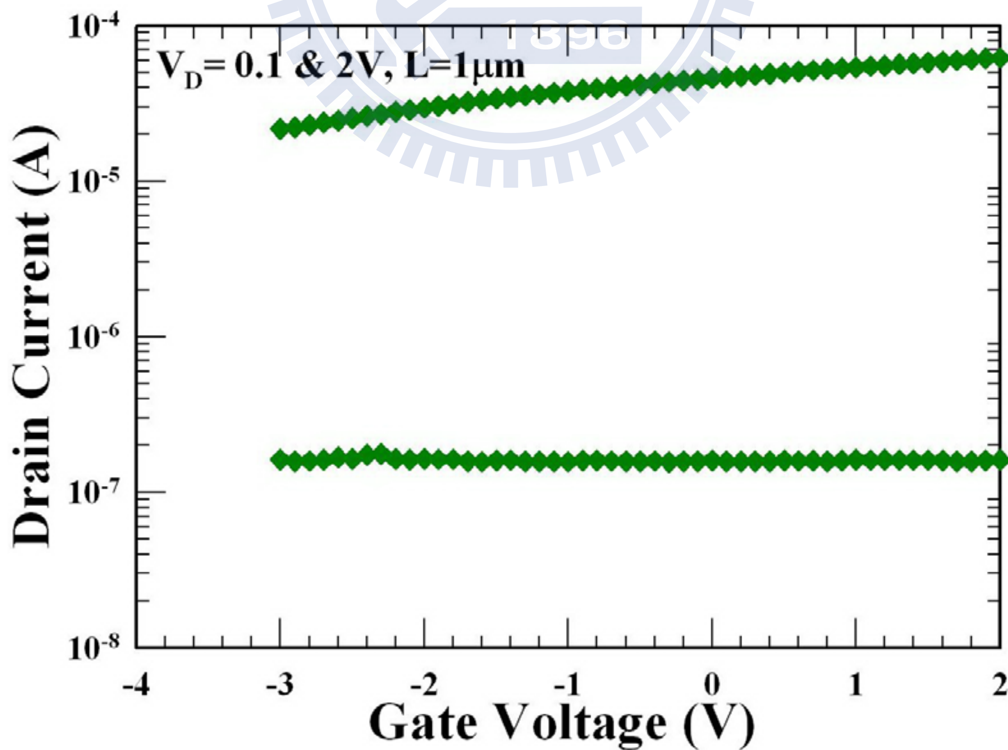


Fig. 5-39 Transfer characteristics and the affiliated cross-sectional SEM image of a non-working 3-D JL device.

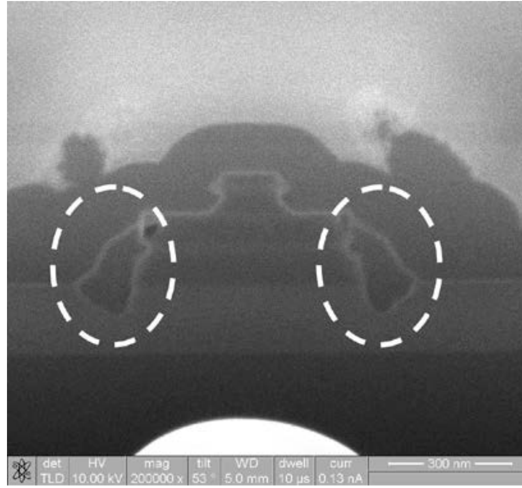


Fig. 5-40 Cross-sectional SEM image of a non-working 3-D JL device.

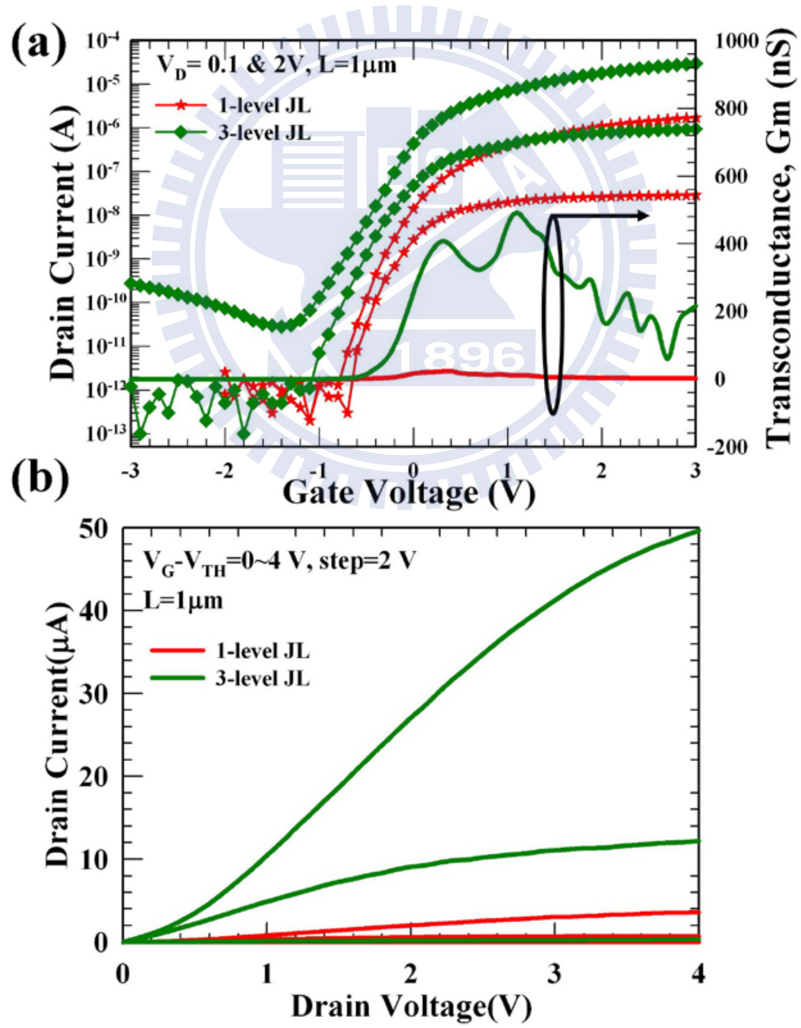


Fig. 5-41 Transfer and output characteristics of both 1-level and 3-level JL splits with L = 1 μm, (a) measured at V_D = 0.1 and 2 V, (b) V_G - V_{th} = 0 ~ 4 V with step = 2 V.

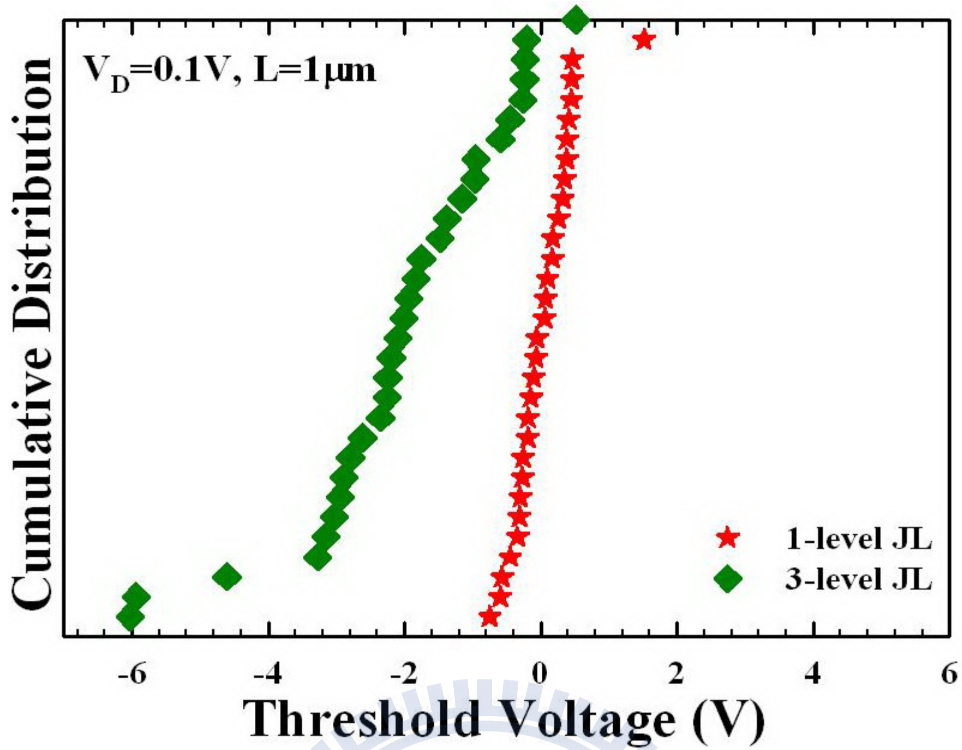


Fig. 5-42 Cumulative distribution of V_{th} for both 1-level and 3-level JL splits with L = 1 μm measured at V_D = 0.1 V.

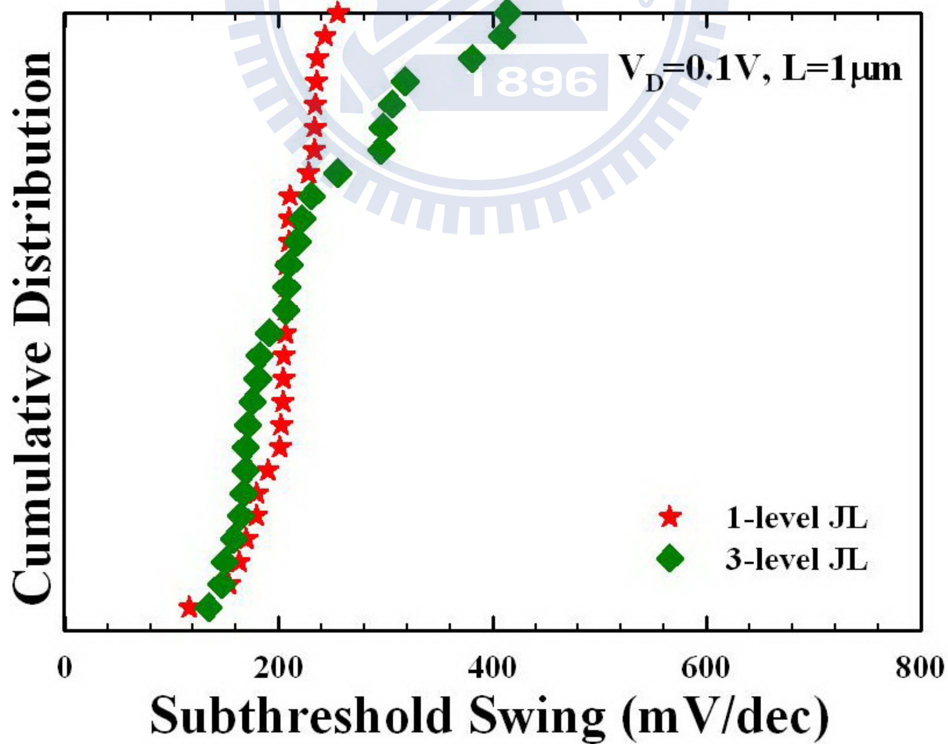


Fig. 5-43 Cumulative distribution of SS for both 1-level and 3-level JL splits with L = 1 μm measured at V_D = 0.1 V.

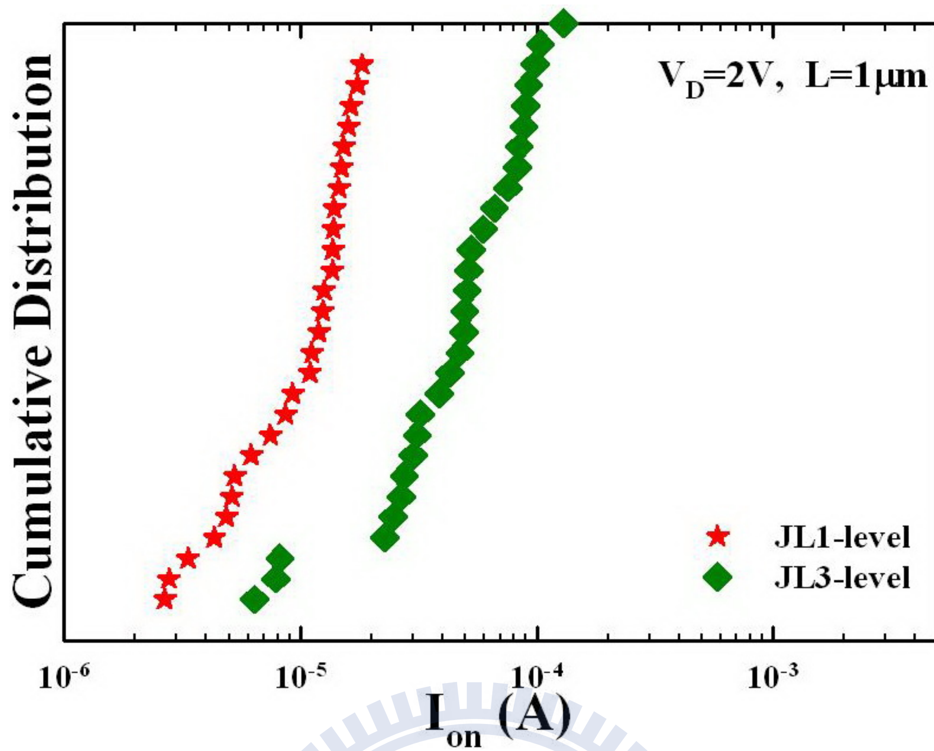


Fig. 5-44 Cumulative distribution of I_{on} for both 1-level and 3-level JL splits with L = 1 μm extracted by maximum drain current at V_D = 2 V.

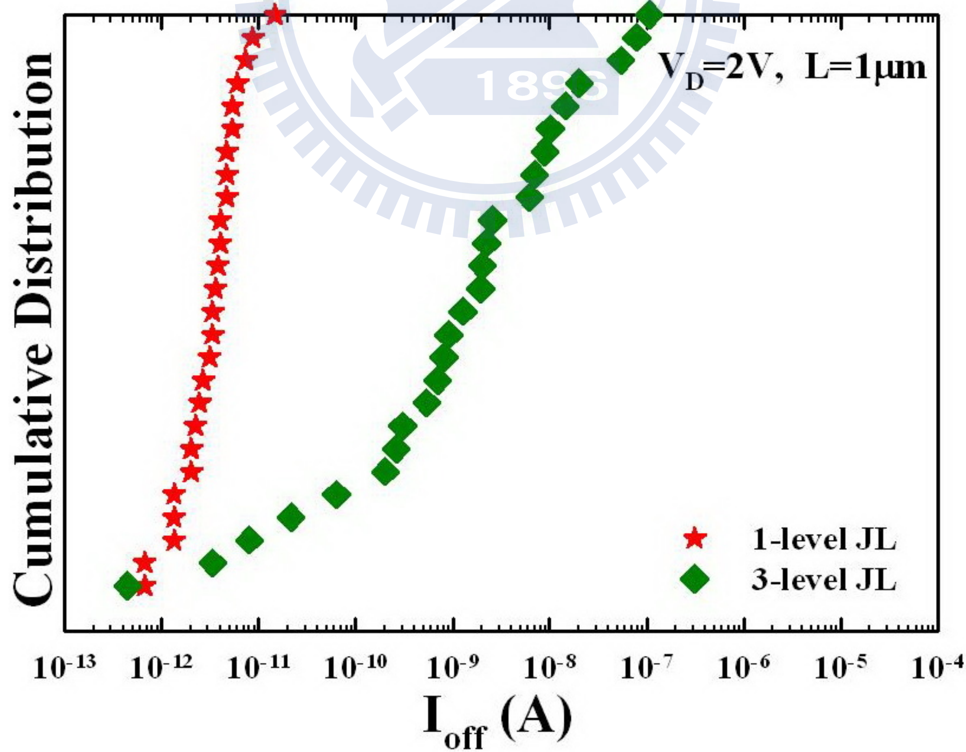


Fig. 5-45 Cumulative distribution of I_{off} for both 1-level and 3-level JL splits with L = 1 μm extracted by minimum drain current at V_D = 2 V.

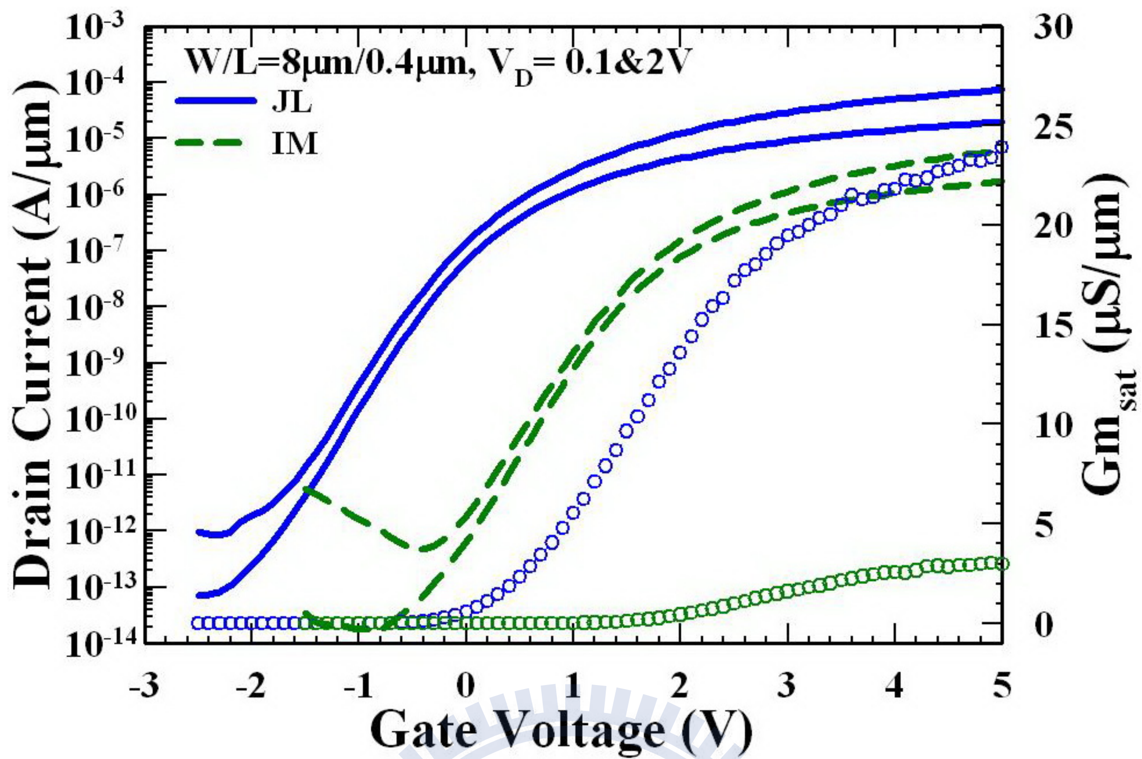


Fig. 5-46 Transfer characteristics of both JL and IM planar poly-Si TFTs with W/L = 8/0.4 μm measured at V_D = 0.1 and 2 V.

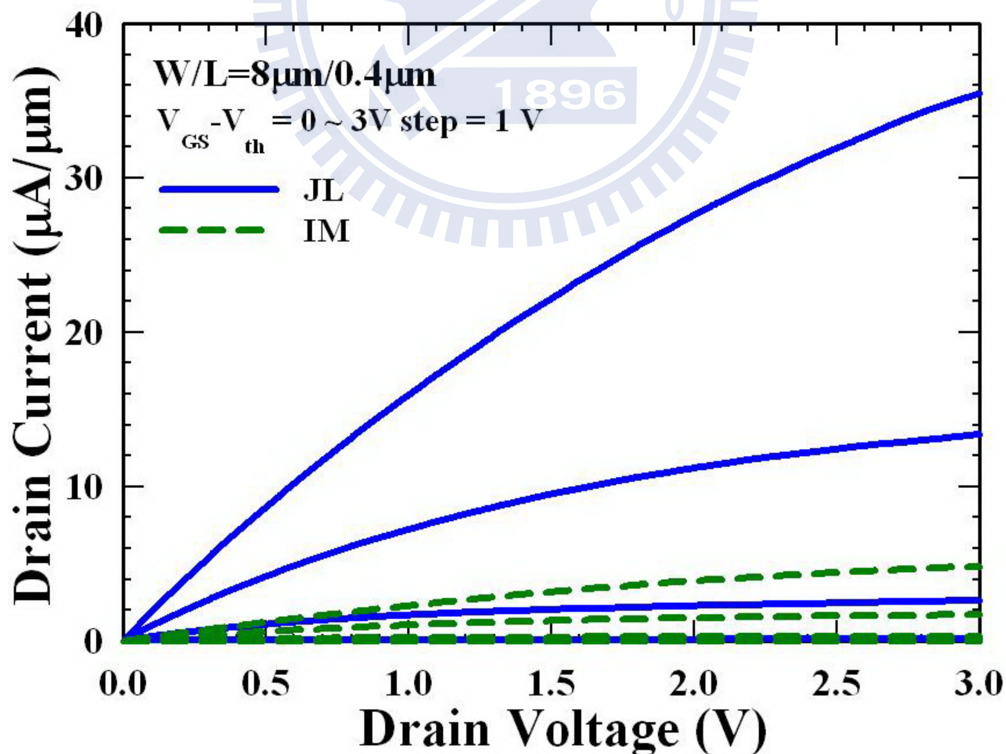


Fig. 5-47 Output characteristics of both JL and IM planar poly-Si TFTs with W/L = 8/0.4 μm measured at V_G - V_{th} = 0 ~ 3 V with step = 1 V.

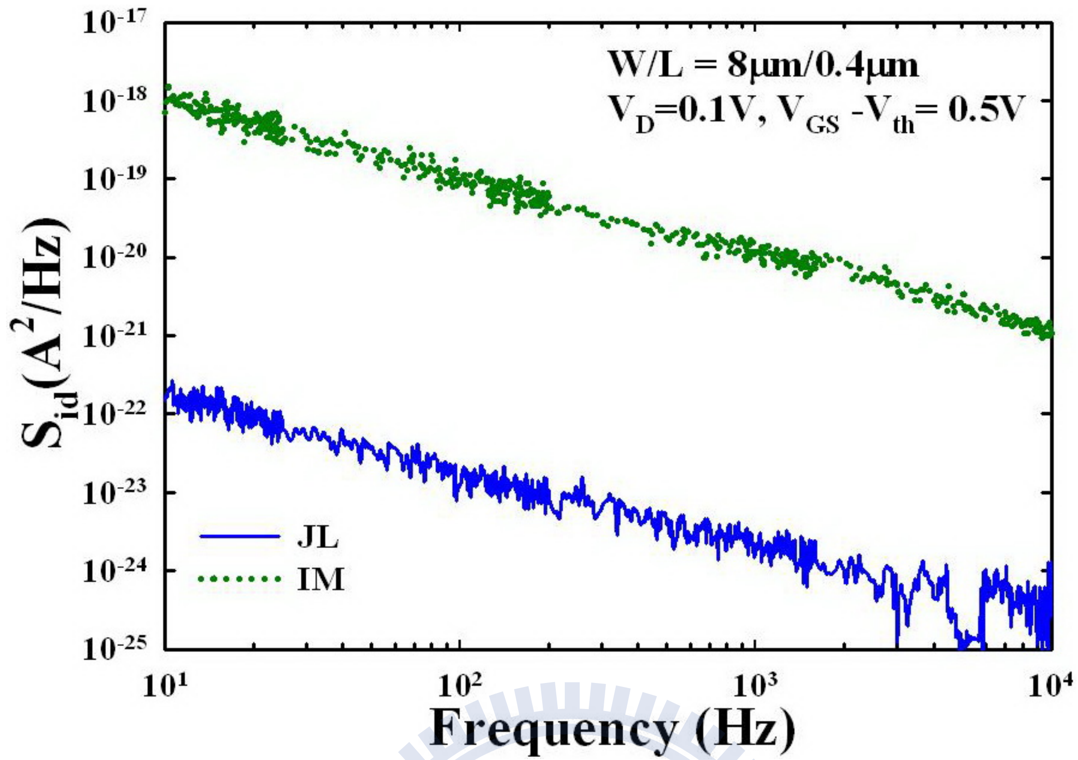


Fig. 5-48 Drain-current noise power spectral density (S_{id}) versus frequency for both JL and IM planar poly-Si TFTs with W/L = 8/0.4 μm measured at V_{GS} - V_{th} =0.5 V and V_D = 0.1 V.

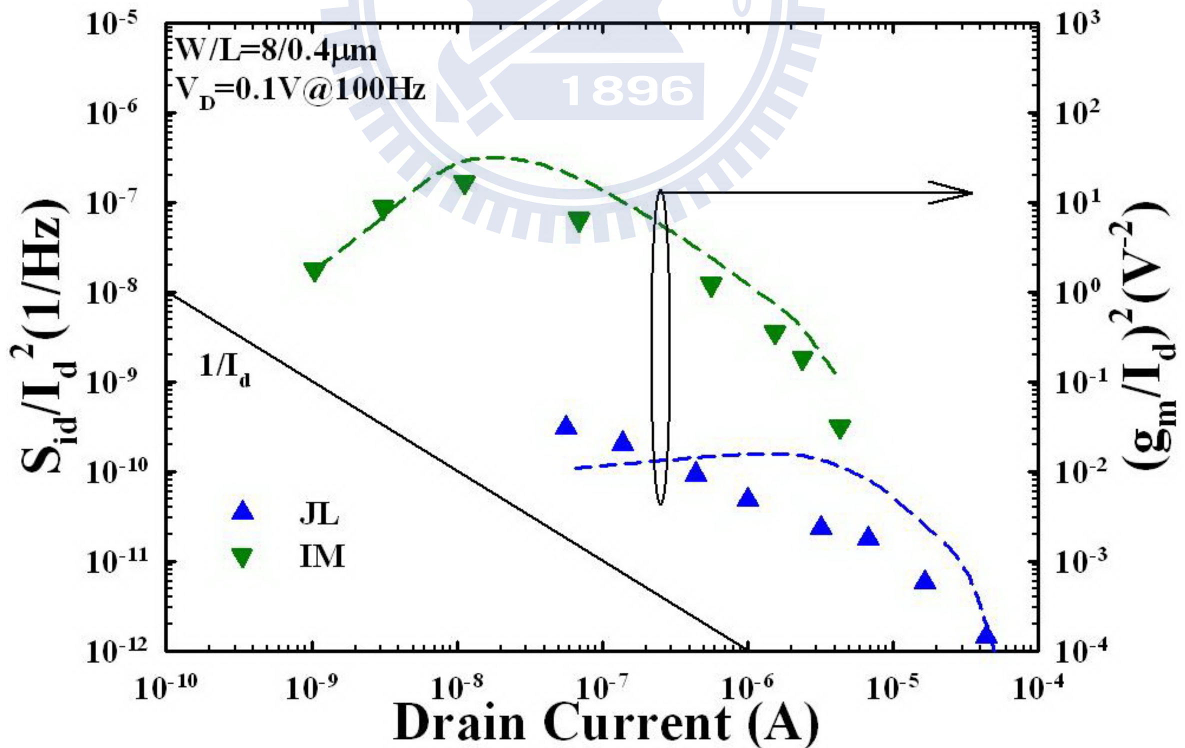


Fig. 5-49 (Symbols) S_{id}/I_d^2 and (dashed lines) $(g_m/I_d)^2$ versus drain current for both JL and IM planar poly-Si TFTs with W/L = 8/0.4 μm measured at V_D = 0.1 V.

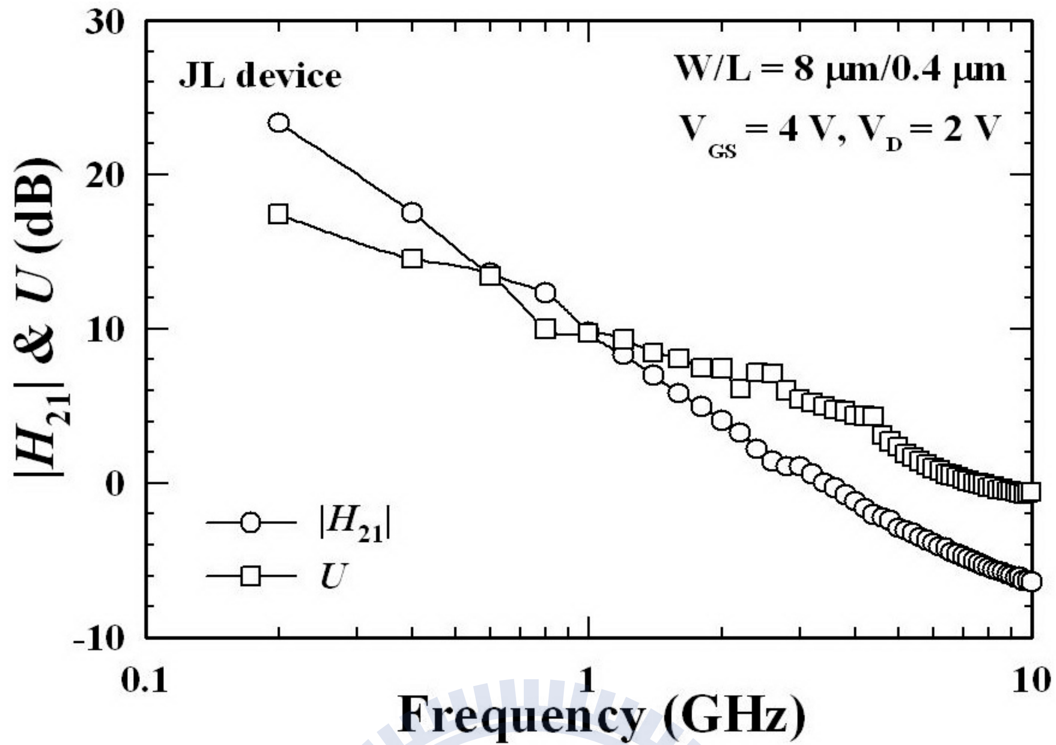


Fig. 5-50 H_{21} and U of JL device measured at V_D of 2 V and ($V_{GS} - V_{th}$) of 4 V with W/L = 8/0.4 μm.

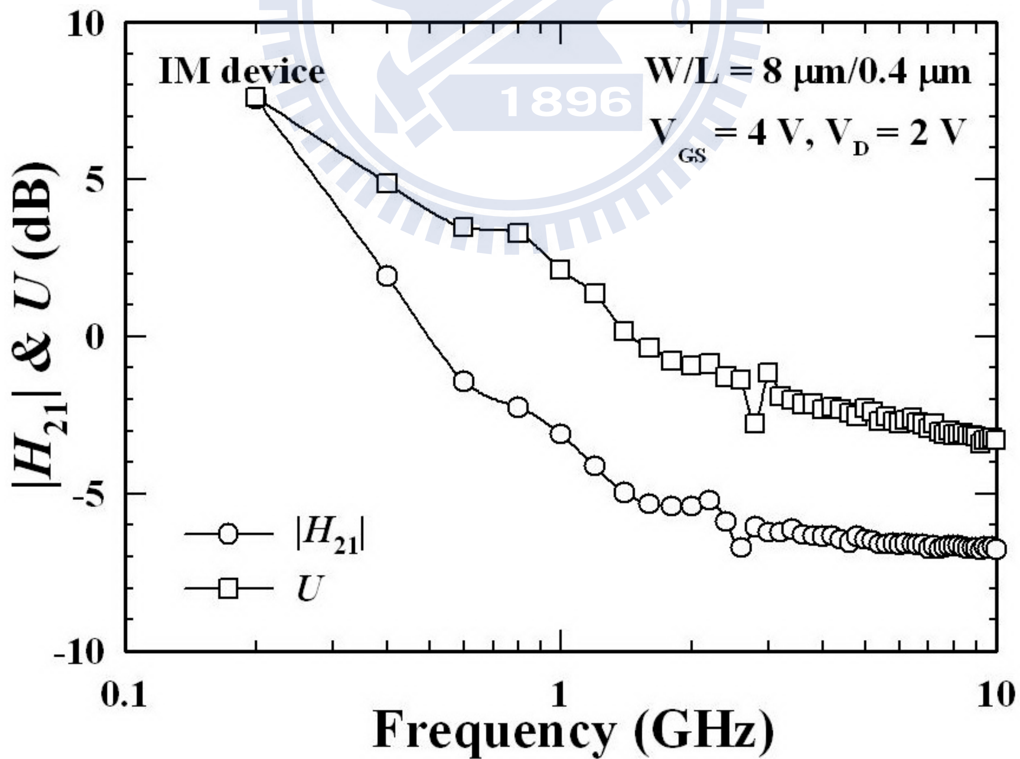


Fig. 5-51 H_{21} and U of IM device measured at V_D of 2 V and ($V_{GS} - V_{th}$) of 4 V with W/L = 8/0.4 μm.

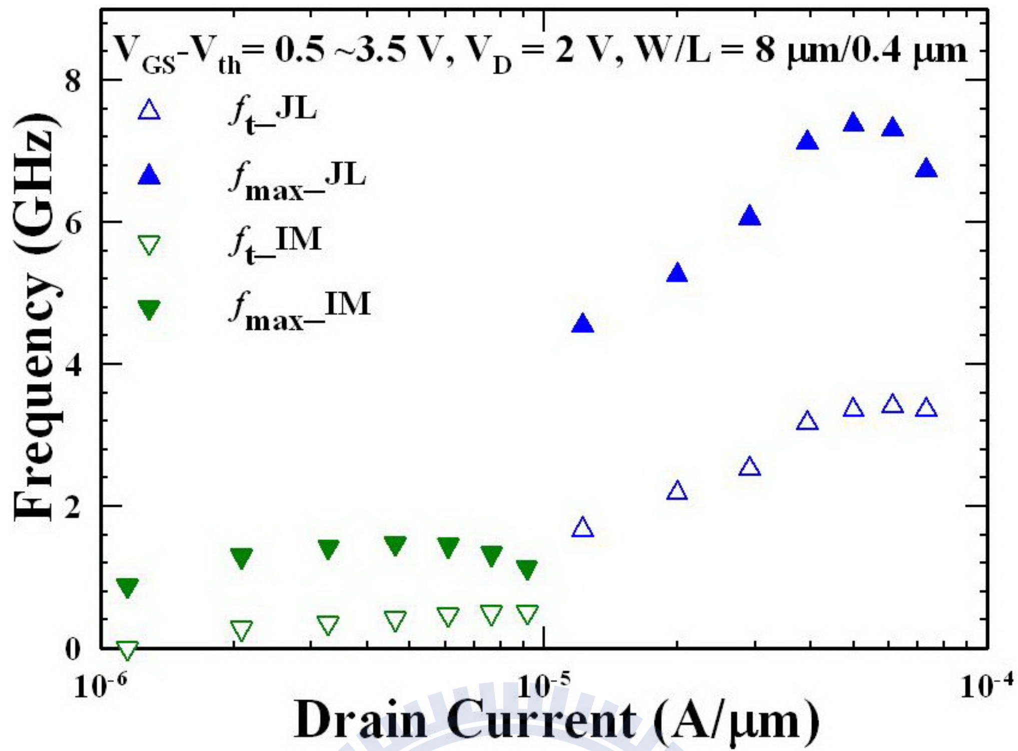


Fig. 5-52 f_t and f_{max} of the JL and IM devices measured at V_D of 2 V and ($V_{GS} - V_{th}$) of 0.5–3.5 V with respect to the drain current.

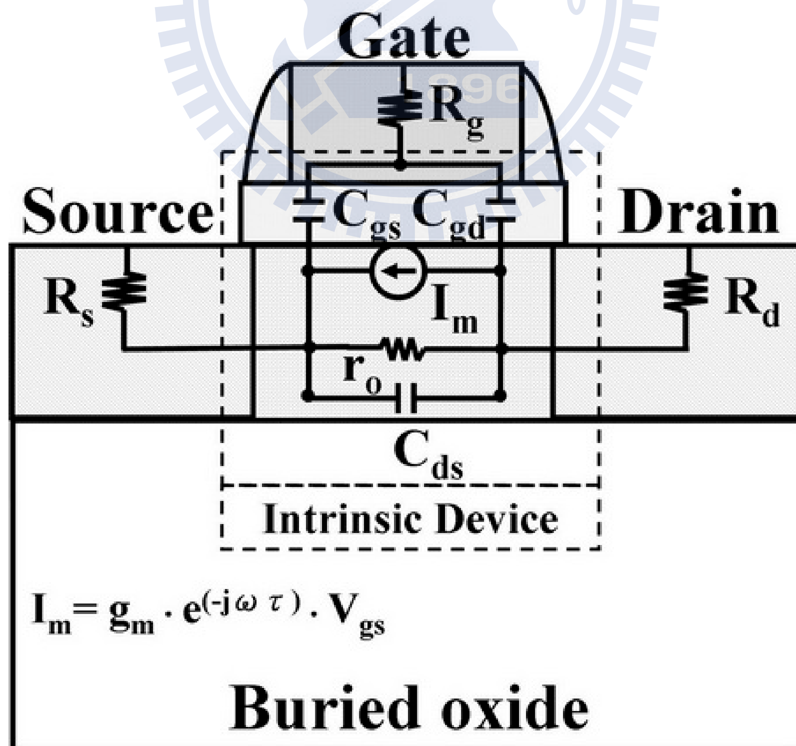


Fig. 5-53 The cross section of the fabricated TFT with corresponding small-signal equivalent circuit.

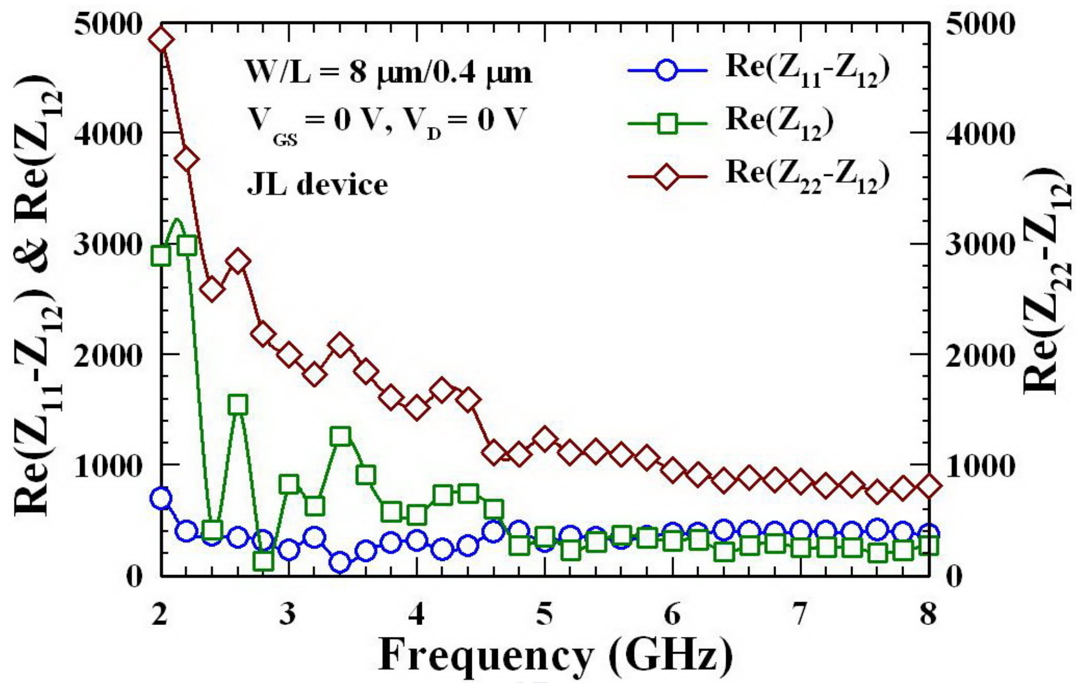


Fig. 5-54 The extraction results of extrinsic resistances.

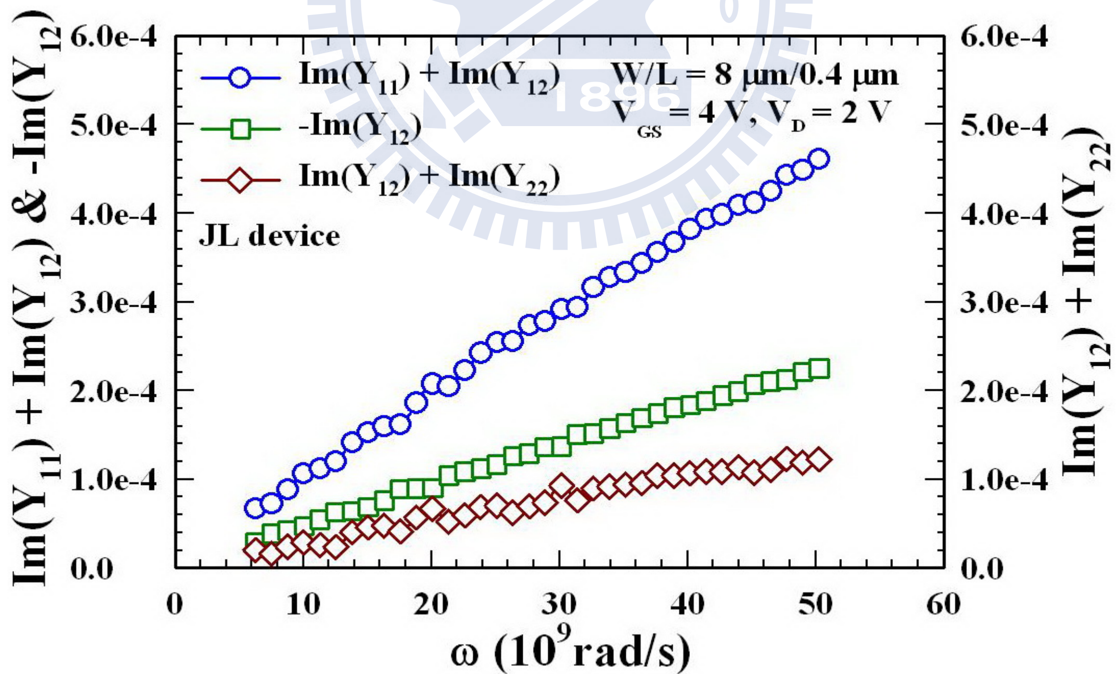


Fig. 5-55 The extraction results of $Im(Y_{11})+Im(Y_{12})$, $-Im(Y_{12})$, and $Im(Y_{12})+Im(Y_{22})$ as a function of the angular frequency.

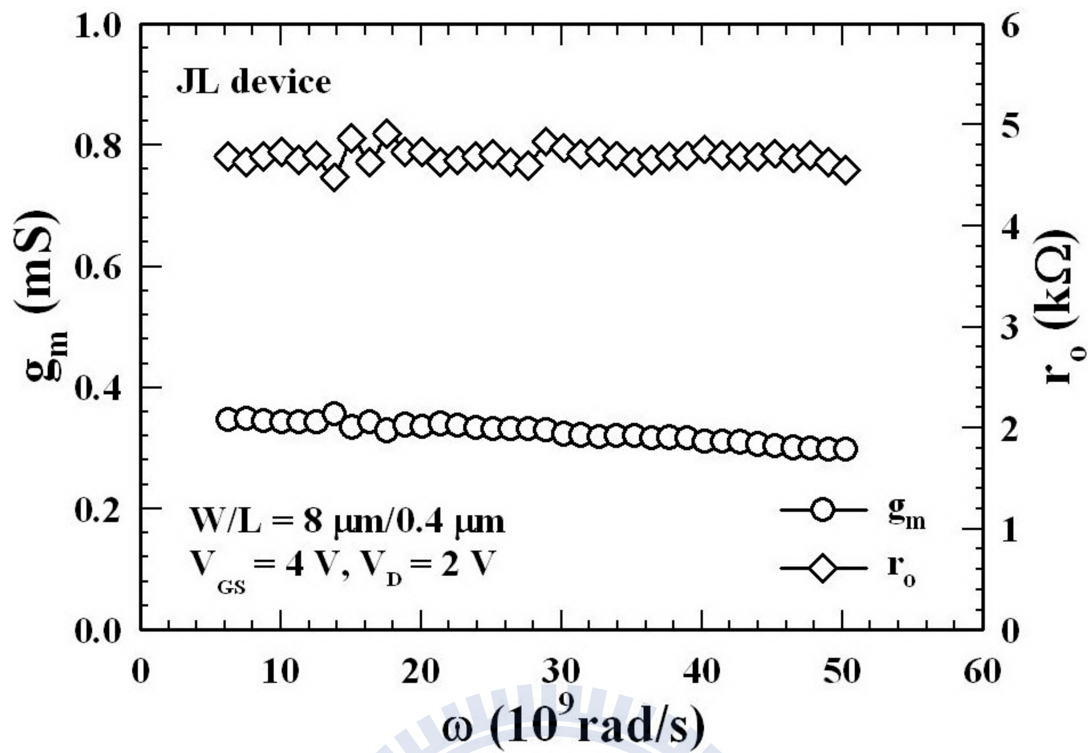


Fig. 5-56 The extraction results of g_m and r_o as a function of the angular frequency.

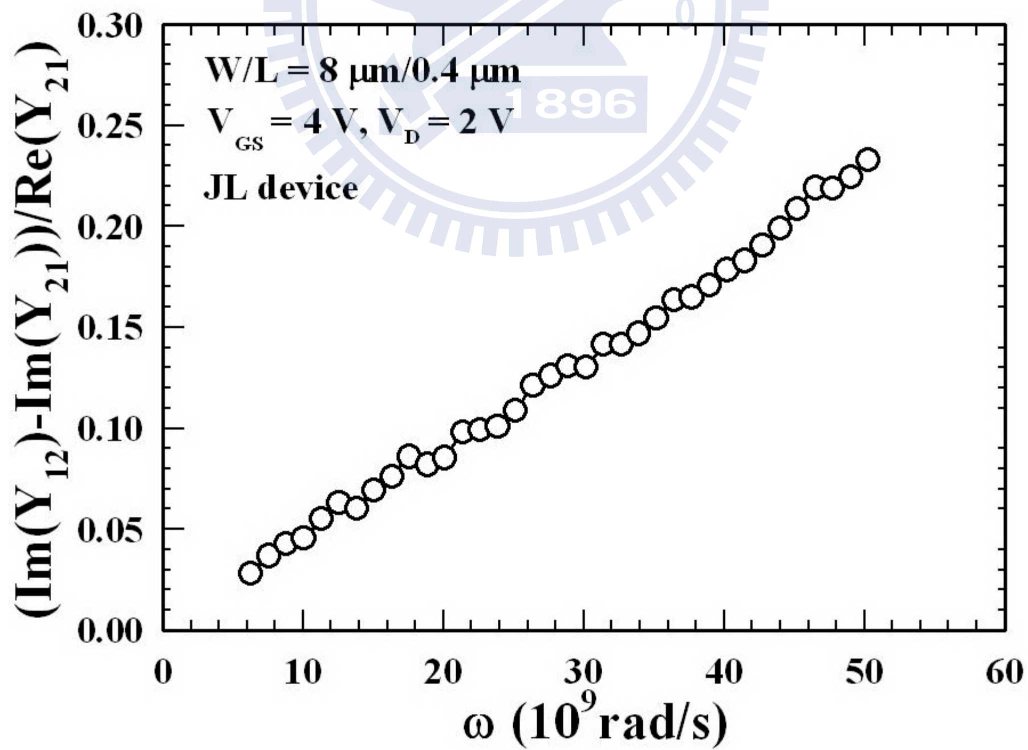


Fig. 5-57 The extraction results of τ as a function of the angular frequency.

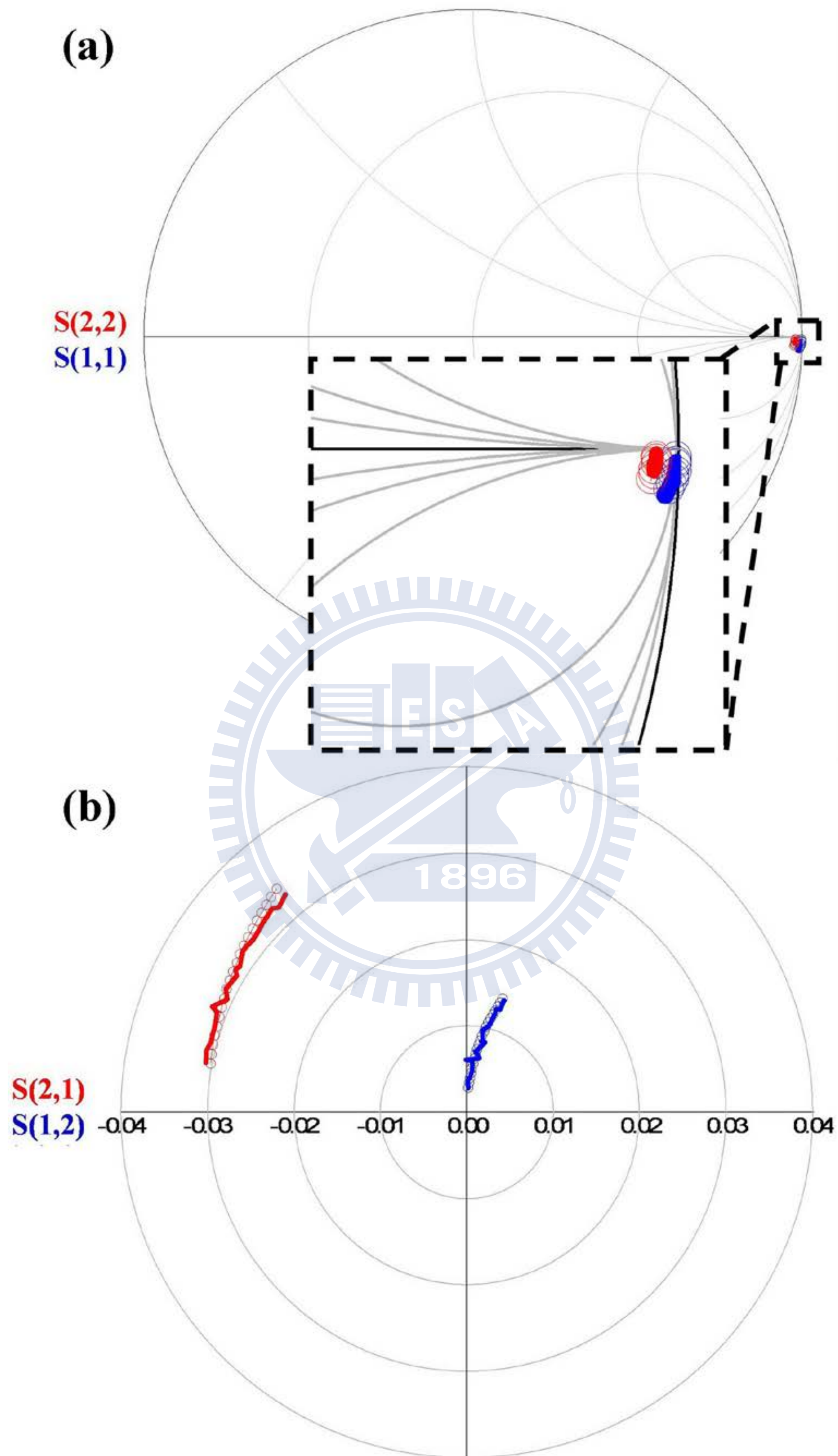


Fig. 5-58 The modeling results of the fabricated TFT (a) S_{11} and S_{22} and (b) S_{12} and S_{21} (lines for measurements, symbols for models).

Chapter 6

Conclusion and Suggested Future Work

6.1 Conclusion

In this dissertation, we have developed a novel double-patterning (DP) technique for generation of gate patterns with gate length down to 80 nm using a conventional I-line stepper. Some alternative methods, such as electron beam direct writing and photoresist-ashing scheme adopted in the university-based laboratories for studying the nano-scale devices, are quantitatively compared with the proposed DP method in terms of variation in critical dimension control and throughput. With the aid of this I-line DP technique, several kinds of devices with symmetrical or asymmetrical S/D were fabricated and characterized to investigate the device physics and trade-off between device performance and reliability. On the other hand, the junctionless (JL) poly-Si-based devices were successfully demonstrated, for the first time, with an implant-free process. Various device structures and configurations, including multiple-gated (MG) nanowires (NW) field-effect transistors (FETs), silicon-oxide-nitride-oxide-silicon (SONOS) flash memory cells, and radio-frequency devices, were fabricated and characterized using an *in situ* doped poly-Si layer as the channel and S/D to accomplish the implant-free process. Several important results were observed and summarized as follows:

In Chapter 2, the I-line-based DP lithographic process is presented and its availability has been verified by the successful fabrication of 120 nm n-/p-MOSFETs. In comparison with the conventional single-patterning method through both in-line and cross-sectional SEM analyses, the DP technique is capable of achieving much shorter line patterns, good critical dimension (CD) control, and acceptable throughput. The impacts of S/D halo on device performance, including short-channel effect, current drivability and V_{th} roll-off, are also discussed. The results indicate that it is very important to optimize the halo implant for nano-scale device manufacturing.

In Chapter 3, using a refined technique, we have extended the lithography limit of the DP technique to sub-60 nm regimes and fabricated 45nm-nMOSFETs with symmetric or asymmetric S/D doping. Moreover, several lithographic processes are quantitatively compared from the perspectives of the uniformity of CD, throughput,

LER, and minimum line width. Our results indicate that the proposed method not only shows remarkable progress in shorting the line patterns, but also is promising for the research works carried out at the university-based laboratories. In addition, the fabricated devices are conducive to the optimization of the S/D engineering as far as the device performance is concerned. The asymmetric S/D doping device shows higher current drivability, which could be beneficial for RF IC application.

In Chapter 4, we have fabricated and characterized two types of asymmetrical devices, including TFETs and nMOSFETs with asymmetrical halo, to investigate the operation mechanisms. For the fabricated TFETs, the failure of forming abrupt junction profile and the reduction of BTBT are the main culprits to poor SS behavior. For the fabricated nMOSFETs, we have discovered the symmetrical halo-doping structure helps reduce the subthreshold leakage and improves the SCEs at the cost of degraded current drivability. Asymmetrical halo structure relieves such a dilemma. In hot-carrier (HC) reliability test, we found that the drain-side halo doping is the primary culprit of hot-carrier degradation due to the increased peak lateral electric field. We have also evaluated the impact of halo on device performance by investigating the flicker noise (1/f) characteristics before and after the hot-carrier stress. In short, that drain-side halo doping aggravates the HC degradation and deteriorates low-frequency noise further.

In Chapter 5, we have fabricated and characterized various JL devices by employing only one *in situ* doped poly-Si layer to act as the channel and S/D regions. From the SEM, TEM and electrical characterizations, we have confirmed the feasibility of JL poly-Si TFT technique in terms of accomplishing NWs, 3-D NWs, flash memories, and ultrathin-body architectures for future 3-D electronics and system-on-panel applications.

6.2 Suggested Future Work

Notwithstanding that several phenomena and topics of both asymmetrical devices and JL devices have been studied in this dissertation, there are still some aspects worthy of investigating to further improve device performance for practical applications.

For tunneling field-effect transistor (TFET) technique, the adoptions of green transistor (gFET) architecture [1], Si/Ge/Si heterostructure channel [2], III-V heterojunction engineering [3], thinner electrical oxide thickness, high source doping and so on are beneficial to steepening SS and boosting drive current, attributing to

larger tunneling area, source-to-channel tunnel barrier height, and greater gate controllability. These aforementioned schemes are suggested for future work to improve TFET performance.

For asymmetrical S/D MOSFETs, not only halo doping but also S/D extension and even deep S/D region could be asymmetrical through the proposed I-line DP technique. Besides, such asymmetrical MOSFETs are quite suitable for high-voltage and radio-frequency (RF) applications as the structures are properly designed. For instance, laterally diffused metal-oxide-semiconductor (LDMOS) transistor is inherently asymmetrical and easily integrated with the DP method. Therefore, it is suggested that the optimization of S/D doping engineering and diversification in asymmetrical structure are the targets deserving future efforts.

For JL devices, we could replace the stacked multilayer dummy patterns with n^+-doped poly-Si layer to fulfill double-gated operation and multilevel applications. In addition, JL SONOS devices could be replaced by high-κ dielectrics to boost memory properties such as faster programming/erasing speed and improved data retention [4]. Accordingly, the adoption of high-κ dielectrics in our JL memory devices would benefit the erasing behavior and worthy of further study. On the other hand, performance of the JL RF devices could be further improved by virtue of downscaling and adopting new materials in the device structure such as high-κ gate dielectrics, metal gate electrode, and lower-resistance silicided S/D.

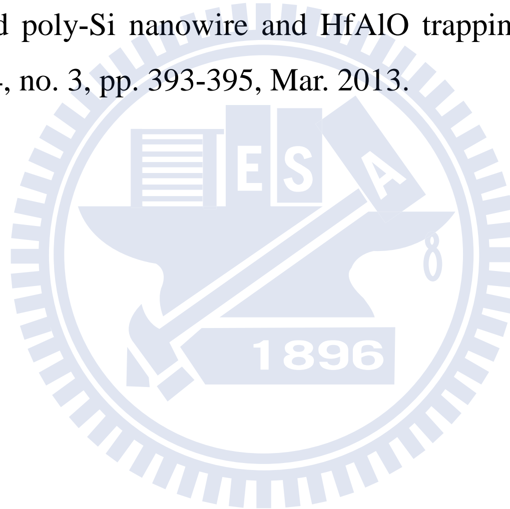
References

[1] C. Hu, D. Chou, P. Patel, and A. Bowonder, “Green transistor - a V_{DD} scaling path for future low power ICs,” in *IEEE Int’l Symp. VLSI-TSA*, 2008, pp. 14-15.

[2] A. Bowonder, P. Patel, K. Jeon, J. Oh, P. Majhi, H. H. Tseng, and C. Hu, “Low-voltage green transistor using ultra shallow junction and hetero-tunneling,” in *Junction Technology, 2008. IWJT '08*, 2008, pp. 93-96.

[3] G. Dewey, B. C. Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, “Fabrication, characterization, and physics of III–V heterojunction tunneling Field Effect Transistors (H-TFET) for steep sub-threshold swing,” in *IEDM Tech. Dig*., 2011, pp. 785-788.

[4] K. H. Lee, H. C. Lin, and T. Y. Huang, “A novel charge-trapping-type memory with gate-all-around poly-Si nanowire and HfAlO trapping layer,” *IEEE Electron Device Lett*., vol. 34, no. 3, pp. 393-395, Mar. 2013.



Vita

姓名：蔡子儀　　　　　　Tzu-I Tsai

性別：　男

生日：　民國 72 年 5 月 1 日

籍貫：　台灣省　台南市

住址：　台南市西門路四段 210 號

學歷：　國立中興大學電機工程學系 (90 年 9 月~94 年 6 月)

　　　　國立交通大學電子研究所碩士班 (94 年 9 月~96 年 7 月)

　　　　國立交通大學電子物理所博士班 (96 年 7 月~103 年 1 月)

博士論文題目：

非對稱金氧半場效電晶體及無接面多晶矽薄膜電晶體的研究

A Study on Asymmetrical MOSFETs and Junctionless Polycrystalline Silicon Thin-Film Transistors

Publication List

A. International Journal：

[1] **T. I. Tsai**, H. C. Lin, Y. J. Lee, K. S. Chen, J. Wang, F. K. Hsueh, T. S. Chao, and T. Y. Huang, “Impacts of a buffer layer and hydrogen-annealed wafers on the performance of strained-channel nMOSFETs with SiN-capping layer,” ***Solid State Electronics***, vol. 52, no. 10, pp.1518-1524, Oct. 2008.

[2] **T. I. Tsai**, H. C. Lin, M. F. Jian, T. Y. Huang, and T. S. Chao, “A Simple Method for Sub-100 nm Pattern Generation with I-line Double Patterning Technique,” ***Microelectronics Reliability***, vol. 50, pp. 584-588, Jan. 2010.

[3] H. C. Lin, **T. I. Tsai**, T. S. Chao, M. F. Jian, and T. Y. Huang, “Fabrication of sub-100-nm metal-oxide-semiconductor field-effect transistors with asymmetrical source/drain using I-line double patterning technique,” ***J. Vac. Sci. Technol. B***, vol. 29, no. 2, pp. 021007-1－021007-7, Mar. 2011.

[4] **T. I. Tsai**, H. C. Lin, T. Y. Lin, K. M. Chen, T. S. Chao, and T. Y. Huang, “RF characteristics of poly-Si thin-film transistors,” ***Transactions of the Materials Research Society of Japan***, vol. 38, no. 1, pp. 37-40, Mar. 2013.

B. International Letter：

[1] C. J. Su, **T. I. Tsai**, Y. L. Liou, Z. M. Lin, H. C. Lin, and T. S. Chao, “Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels,” ***IEEE Electron Device Lett.***, vol. 32, no. 4, pp. 521-523, Apr. 2011.

[2] C. J. Su, T. K. Su, **T. I. Tsai**, H. C. Lin, and T. Y. Huang, “A junctionless SONOS nonvolatile memory device constructed with in situ-doped polycrystalline silicon nanowires,” ***Nanoscale Research Lett.***, vol. 7, no. 1, pp. 162-162-6, Feb. 2012.

[3] C. J. Su, **T. I. Tsai**, H. C. Lin, T. Y. Huang, and T. S. Chao, “Low-Temperature Poly-Si Nanowire Junctionless Devices with Gate-All-Around TiN/Al_2O_3 Stack Structure Using an Implant-Free Technique,” ***Nanoscale Research Lett.***, vol. 7, no. 1, pp. 339-339-6, Jun. 2012.

[4] **T. I. Tsai**, K. M. Chen, H. C. Lin, T. Y. Lin, C. J. Su, T. S. Chao and T. Y. Huang, “Low-Operating-Voltage Ultra-Thin Junctionless Poly-Si Thin-Film Transistor Technology for RF Applications,” ***IEEE Electron Device Lett.***, vol. 33, no. 11, pp. 1565-1567, Nov. 2012.

C. International Conference：

[1] **T. I. Tsai**, Y. J. Lee, K. S. Chen, J. Wang, C. C. Wan, F. K. Hsueh, H. C. Lin, T. S. Chao, and T. Y. Huang, “Impacts of a buffer Layer and Hi-wafers on the performance of strained-channel nMOSFETs with SiN capping layer,” in *Proc. International Semiconductor Device Research Symposium (IRDRS)*, MD, USA, Dec. 2007.

[2] **T. I. Tsai**, Y. J. Lee, K. S. Chen, J. Wang, C. C. Wan, F. K. Hsueh, H. C. Lin, T. S. Chao, and T. Y. Huang, “Reliability of strained-channel nMOSFETs with SiN capping layer on Hi-wafers with a thin LPCVD-TEOS buffer layer,” in *Proc. International Semiconductor Device Research Symposium (IRDRS)*, MD, USA, Dec. 2007.

[3] **T. I. Tsai**, Y. J. Lee, K. S. Chen, J. Wang, F. K. Hsueh, H. C. Lin, and T. Y. Huang, "Comparisons on performance improvement by nitride capping layer among different channel directions nMOSFETs," in *Proc. International Semiconductor Device Research Symposium (IRDRS)*, MD, USA, Dec. 2007.

[4] **T. I. Tsai**, R. J. Hsieh, T. S. Chao, H. C. Lin, L. Chan and T. Y. Huang, "Generation of sub-100nm patterns with I-line double patterning technique," in ***Int. Electron Devices and Materials Symp.*** **(*IEDMS*)**, Taoyuan, Taiwan, Nov. 2009. (**Best Student Paper Award**)

[5] **T. I. Tsai**, M. F. Jian, T. S. Chao, H. C. Lin, and T. Y. Huang, "Characteristics and flicker noise performance of nano-scale nMOSFETs with asymmetrical source/drain," in ***Int. Electron Devices and Materials Symp.*** **(*IEDMS*)**, Chungli, Taiwan, Nov. 2010.

[6] T. K. Su, **T. I. Tsai**, C. J. Su, H. C. Lin, and T. Y. Huang, "Fabrication and characterization of a junctionless SONOS transistor with poly-Si nanowire channels," in *4th IEEE International Nanoelectronics Conference (INEC)*, Taoyuan, Taiwan, Jun. 2011.

[7] **T. I. Tsai**, T. S. Chao, C. J. Su, H. C. Lin, T. Y. Huang, and Y. J. Wei, "Low temperature polycrystalline Si nanowire devices with gate-all-around Al_2O_3/TiN structure using an implant-free technique," in *4th IEEE International Nanoelectronics Conference (INEC)*, Taoyuan, Taiwan, Jun. 2011.

[8] **T. I. Tsai**, T. S. Chao, H. C. Lin, T. Y. Huang, and Y. J. Wei, "A simple method for forming sub-30 nm gate patterns with modified I-line double patterning technique," in *4th IEEE International Nanoelectronics Conference (INEC)*, Taoyuan, Taiwan, Jun. 2011.

[9] Z. M. Lin, **T. I. Tsai**, T. Y. Huang, and H. C. Lin, "Fabrication and characterization of gate-all-around polycrystalline silicon nanowire thin-film transistors with sub-60 mV/decade subthreshold swing," in ***Int. Electron Devices and Materials Symp.*** **(*IEDMS*)**, Taipei, Taiwan, Nov. 2011. (**Best Student Paper Award**)

[10] **T. I. Tsai**, T. Y. Lin, H. C. Lin, K. M. Chen, T. S. Chao, and T. Y. Huang, "Low-operating-voltage poly-Si thin-film transistor technology for RF applications," in *Int. Union of Materials Research Societies-Int. Conference on Electronic Materials* (*IUMRS-ICEM 2012*), Yokohama, Japan, Sep. 2012. **(Award for Encouragement of Research)**

[11] **T. I. Tsai**, C. J. Su, H. C. Lin, T. S. Chao, and T. Y. Huang, "Junctionless transistors with three dimensional stacks of heavily doped polysilicon nanowire channels," in ***Int. Electron Devices and Materials Symp.*** **(*IEDMS*)**, Kaohsiung, Taiwan, Nov. 2012.

[12] C. J. Su, T. K. Su, **T. I. Tsai**, B. S. Shie, H. C. Lin, and T. Y. Huang, "The effects of doping concentration and gate configuration on junctionless poly-Si nanowire SONOS memory devices," in ***Int. Electron Devices and Materials Symp.*** **(*IEDMS*)**, Kaohsiung, Taiwan, Nov. 2012. (**Best Student Paper Award**)

D. Local Conference：

[1] **T. I. Tsai**, M. F. Jian, P. H. Chang, T. S. Chao, H. C. Lin, and T. Y. Huang, "Impacts of pocket implant on the performance of 120 nm-gate-length MOSFETs with I-line

double patterning technique," in ***Symp. on Nano Device Technology (SNDT)***, Hsinchu, Taiwan, Apr. 2010.

[2] T. Y. Lin, **T. I. Tsai**, T. S. Chao, K. M. Chen, H. C. Lin, and T. Y. Huang, "The development of polysilicon thin-film transistor technology for RF applications," in ***Symp. on Nano Device Technology (SNDT)***, Hsinchu, Taiwan, Apr. 2012.

[3] **T. I. Tsai**, H. C. Lin, T. S. Chao, and T. Y. Huang, "A comparison of lithographic techniques," in *Taiwan ESD and Reliability Conference*, Hsinchu, Taiwan, Nov. 2012.