The Design of a 3-V 900-MHz CMOS Bandpass Amplifier

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***Abstract*— A new bandpass amplifier which performs both functions of low-noise amplifier (LNA) and bandpass filter (BPF) is proposed for the application of 900-MHz RF front-end in wireless receivers. In the proposed amplifier, the positive-feedback Q-enhancement technique is used to overcome the low-gain low-Q characteristics of the CMOS tuned amplifier. The Miller-capacitance tuning scheme is used to compensate for the process variations of center frequency. Using the high-Q bandpass amplifier in the receivers, the conventional bulky off-chip filter is not required. An experimental chip fabricated by 0.8-μm N-well double-poly-double-metal CMOS technology occupies 2.6 $\times$ 2.0 mm^2 chip area. Under a 3 V supply voltage, the measured quality factor is tunable between 2.2 and 44. When the quality factor is tuned at $Q = 30$, the measured center frequency of the amplifier is tunable between 869–893 MHz with power gain 17 dB, noise figure 6.0 dB, output 1 dB compression point at -30 dBm, third-order input intercept point at -14 dBm, and power dissipation 78 mW.**

***Index Terms*— Bandpass amplifier, bandpass filter, CMOS technology, integrated inductor, low-noise amplifier, mobile communication, radio frequency, wireless receiver.**

I. Introduction

In recent years, the rapid growth of mobile radio systems has led to an increasing demand of low-cost high-performance communication IC's. The operational frequency bands of the modern mobile systems such as advanced mobile phone service (AMPS) and Pan European Group special mobile (GSM) are 900 MHz, and 1.9 GHz for the personal communication network (PCN) and digital European cordless telephone (DECT) [1]. In such a high-frequency band, the complete systems often contain many IC's and discrete elements to obtain the maximum performance/cost ratio. Typical implementation of the systems uses silicon bipolar or BiCMOS IC's as the RF/IF sections [2]–[7] and CMOS IC's as the baseband section [8]–[10]. In order to obtain a small-size low-weight handheld system, a single-technology scheme is preferred for the maximum integration level. To realize this scheme, low-cost high-integration all-CMOS implementation is one of the most attractive solutions [11].

The key factor to obtain an all-CMOS system is the availability of high-performance CMOS RF components, which include low noise amplifiers (LNA's), bandpass filters (BPF's), mixers, voltage control oscillators (VCO's), and power amplifiers (PA's). Recent progress in IC technology has brought the cut-off frequencies of CMOS devices beyond the GHz range, but implementing the GHz-range CMOS components is still a great challenge due to the existence of inherent limiting factors in CMOS technology. The limiting factors encountered in the CMOS RF design include:

- low device transconductance;
- large device terminal capacitances;
- not available high-precision high-quality on-chip passive components;
- not available precise high-frequency CAD model.

Recently, much effort has been devoted to the integration of RF components in CMOS technology. With the special techniques developed to overcome some of the limiting factors, the proposed CMOS LNA [12], [13], mixer [14], [15], synthesizer [16], and PA [17] have good high-frequency performance. However, the CMOS BPF has not been reported. Thus, the external passive filters such as ceramic filters or surface acoustic wave (SAW) filters are still required [18]. In order to obtain the maximum integration level, the BPF's have to be on-chip integrated with other CMOS RF components.

In this paper, a new 900 MHz CMOS bandpass amplifier is proposed, which performs the functions of LNA and BPF simultaneously. As compared with the design of separate LNA and BPF, the proposed bandpass amplifier can retain the same features of low noise, high gain, and high Q. Moreover, it has the advantages of low cost, low power consumption due to the high integration level, and the reduction of extra matching elements between LNA and BPF.

The typical system requirements of RF front-end circuits in mobile systems are given in Section II. The design methodology of the proposed bandpass amplifier is given in Section III. In Section IV, design considerations and simulation techniques are presented. In Section V, experimental results are described. Finally, the conclusion is given in Section VI.

II. System Requirements

The RF front-end circuit is an important building block in the wireless receivers because it determines the RF sensitivity and intermodulation immunity of the overall receivers. A typical block diagram of the RF front-end circuit is shown in Fig. 1, which consists of a band filter, an LNA, an image filter (required in a dual-conversion receiver), and a downconversion mixer with the associated local oscillator (LO). The object of this design is a bandpass amplifier providing the functions of band filter and LNA, therefore, the specifications of band

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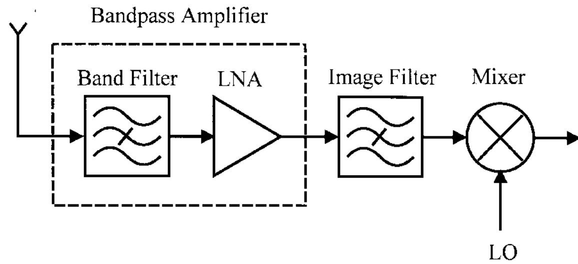


Fig. 1. Typical block diagram of the RF front-end in wireless receivers.

filter and LNA must be met simultaneously. The essential features are center frequency, quality factor, power gain, noise figure, linearity, impedance matching, stability, and power consumption.

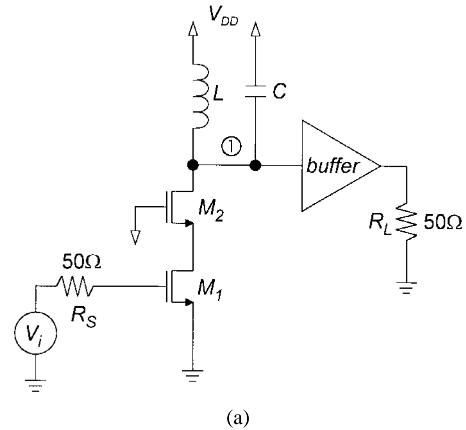
The major function of the band filter is to remove the out-of-band noise, which also contributes to the rejection of image signals. In the modern 900 MHz mobile systems, the signal bandwidth is 25 MHz (AMPS, GSM) or 35 MHz (E-GSM). Thus, a band filter of $Q = 30$ is required.

The power gain of the front-end pre-amplifier is an important parameter in the receivers. Its value should be high enough to reduce the noise contribution of the subsequent stages, but not so high to overdrive the subsequent mixer. The power gain is featured by S_{21} (transducer power gain) of the amplifier. Its typical value is about 10–20 dB.

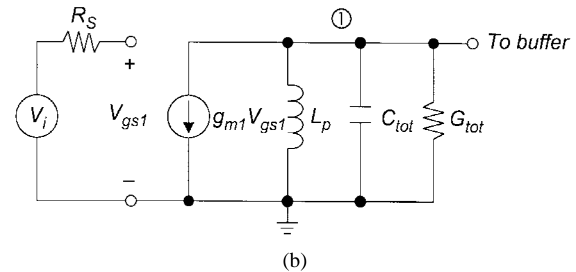
Both noise figure (NF) and third-order input intercept point (IIP_3) are also important features. They determine the minimum detectable signal and the RF sensitivity of the receivers. For a GSM receiver, the GMSK modulation scheme requires the minimum signal-to-noise ratio of 12 dB when a -102 dBm signal is received [19], which is equivalent to the maximum NF of 7 dB in the front-end circuits. Assume the total NF of the stages subsequent to the bandpass amplifier is less than the gain of bandpass amplifier. Then the required NF of the bandpass amplifier is about 6 dB. However, the NF of the bandpass amplifier should be kept as low as possible to ease the NF requirements of other stages in the receiver.

The linearity of a receiver is characterized by the IIP_3 because the intermodulation of two signals in the adjacent channels may appear in the desired channel to degrade the signal-to-noise ratio. For a better intermodulation rejection, the value of IIP_3 should be as high as possible. Typical specification of the IIP_3 is about -18 dBm [20]. Moreover, large-level signals may also occur at the input terminal of the receivers, thus the 1 dB compression point ($P_{1\,\mathrm{dB}}$) used to measure the power handling capability of the amplifier is also an important factor. The value of $P_{1\,\mathrm{dB}}$ should be as large as possible.

The impedance matching at input and output terminals are also important features. The matching characteristics are characterized by S_{11} and S_{22}, whose values should be as low as possible to avoid the use of external matching elements. In addition, the amplifier should also be a stable two-port network. Its stability factor K used to measure the tendency of oscillation must be considered. Finally, the power dissipation of the circuits should be kept low to extend the available service time of the battery-operated portable systems.



(a)



(b)

Fig. 2. (a) Circuit diagram and (b) simplified small-signal equivalent circuit of the RF tuned amplifier.

III. Design Methodology

A. RF Tuned Amplifier

The design of the bandpass amplifier is originated from the RF tuned amplifier shown in Fig. 2(a), which consists of a cascode stage driving an LC resonator and an output buffer driving a low-resistance load. Generally, the tuned amplifier is a popular structure for high-frequency amplifiers. In the RF tuned amplifier of Fig. 2(a), the LC resonator acts as a high-impedance load for the cascode stage at the resonant frequency. Thus, the circuit gain at resonant frequency can be boosted. A simplified small-signal equivalent circuit of the amplifier is shown in Fig. 2(b), where g_{m1} is the transconductance of the MOSFET M_1, L_p is the equivalent parallel inductance of the inductor L, C_{tot} is total capacitance at the node ① including the capacitor C and the terminal capacitances of the MOSFET M_2, and G_{tot} is the total conductance at the node ① including the output conductance of the cascode stage and the equivalent parallel conductance of the inductor L. From Fig. 2(b), the voltage gain at the resonant frequency can be derived as

$$A_v = -\frac{g_{m1}}{G_{\mathrm{tot}}} A_{\mathrm{buffer}} \tag{1}$$

where A_{buffer} is the voltage gain of the buffer. As seen in (1), the key factor to obtain high circuit gain is to decrease the value of G_{tot}, or equivalently increase the Q value of the inductor L.

Unlike the integrated inductors in the GaAs monolithic microwave integrated circuit (MMIC) technology with gold

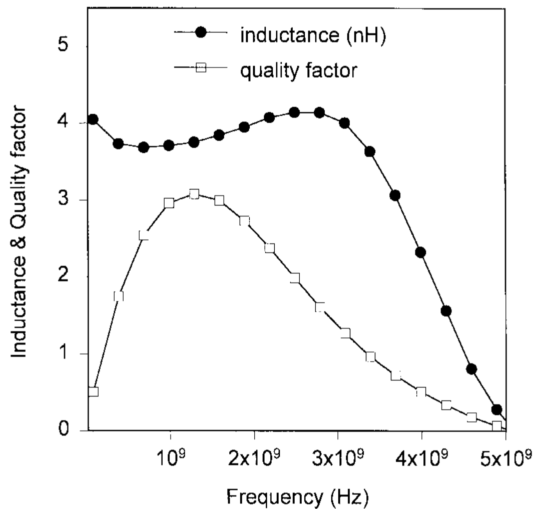


Fig. 3. Measured inductance and quality factor versus frequency of a four-turn spiral inductor with optimum performance around 1 GHz.

metallization layer on thick dielectric substrate, the inductors in CMOS technology suffer from the resistive losses of metallization layer and substrate resistance. Thus, the inductors' quality factor and self-resonant frequency are limited [21], [22]. Investigations show that a four-turn square spiral inductor with 24-μm line-width, 8-μm line-space, and 314-μm outer-dimension has the maximum quality factor around 1 GHz. The measured inductance and quality factor of this inductor are shown in Fig. 3. As may be seen from Fig. 3, the inductance and quality factor at 900 MHz are 3.7 nH and 2.9, respectively. This low-quality-factor inductor prevents the direct realization of CMOS tuned amplifier in Fig. 2(a).

The required power gain described in the previous section is 10–20 dB. Assume the design goal is $S_{21} = 16$ dB. Then the required voltage gain A_v is 10 dB in 50 Ω systems. Since the driving capability of the CMOS buffer is limited and its loss is about 6 dB, the required $g_{m1}/G_{\rm tot}$ is 16 dB = 6.3. The value of $G_{\rm tot}$ depends on the resistive loading of the node ①. Because the output resistance of the cascode stage is often very high, the value of $G_{\rm tot}$ is dominated by the parallel conductance of the integrated inductor. The parallel conductance of the optimized CMOS integrated inductor is about 1/78 ℧ at 900 MHz. Thus the required g_{m1} is 6.3 $G_{\rm tot} = 6.3(1/78) = 8 \times 10^{-2}$ ℧. Such a high transconductance requires a large W/L ratio device operated at high dc current. Simulation shows that an NMOSFET with $W/L = 1250/0.8$ operated at $I_D = 52$ mA is required. At $V_{DD} = 3$ V, the dc power dissipation would be 156 mW. Such a high power dissipation would prevent its applications in modern portable systems.

Since the intrinsic characteristics of CMOS devices can not easily be modified, improving techniques on integrated inductors must be developed to realize the RF tuned amplifier. Recently, large suspended inductors on silicon substrate have been proposed [12] which use an extra mask to etch substrate material under the inductors. The Q-enhancement techniques are also proposed to enhance the quality factors of the integrated inductors [23]–[25]. In this design, the Q-enhancement technique is employed.

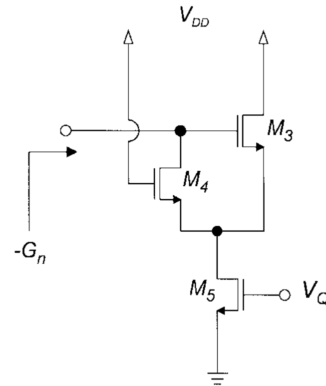


Fig. 4. Circuit used to generate negative conductance.

B. Q-Enhancement Circuit

The basic principle of the Q-enhancement technique is to add a negative conductance to the LC resonator so that the inductor resistive losses can be compensated. With the negative conductance $-G_n$ connected in parallel with the resonator, the total conductance $G_{\rm tot}$ in Fig. 2(b) becomes

$$G_{\rm tot} = G_L - G_n \tag{2}$$

where G_L is the parallel conductance of the inductor which is equal to 1/78 ℧ at 900 MHz in this design. As in (2), $G_{\rm tot}$ is decreased by the presence of negative conductance $-G_n$. As $G_{\rm tot}$ is decreased, the Q value of the circuit can be increased and the required circuit gain can be obtained with a lower value of g_{m1}.

The negative conductance $-G_n$ can be generated from a positive feedback network. In this design, the negative conductance is generated by a source follower with a common-gate stage as the positive feedback element as depicted in Fig. 4. In Fig. 4, the transistor M_3 acts as the source follower whereas the transistor M_4 as the common-gate stage. The effective negative conductance of this combination can be derived as

$$-G_n = -\frac{g_{m3}g_{m4}}{g_{m3} + g_{m4}} \tag{3}$$

where the transconductances g_{m3} and g_{m4} of M_3 and M_4, respectively, are determined by the bias current of the transistor M_5. Thus, the negative conductance $-G_n$ can be tuned through the tuning of V_{gs5}. Since $-G_n$ is tunable, $G_{\rm tot}$ is also tunable. Thus, the circuit gain and quality factor become tunable.

C. Center-Frequency Tuning Circuit

Since the center frequency of the tuned amplifier is determined by the integrated LC resonator which has inevitable variations in the IC fabrication process, the value of center frequency may suffer from a deviation from the desired one. A method to overcome this drawback is to post-tune the values of L or C after the chip has been fabricated. Thus, the variation of center frequency can be compensated through the post-tuning process.

In this design, a Miller-capacitance tuning scheme is used to post-tune the C value. The scheme is illustrated in Fig. 5

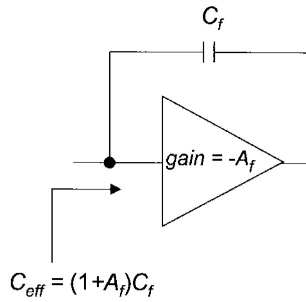


Fig. 5. Miller-capacitance tuning scheme.

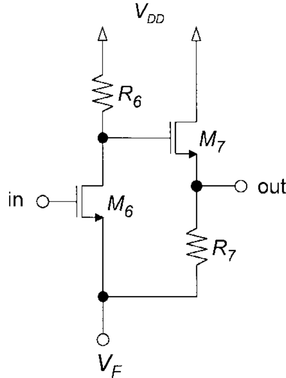


Fig. 6. Circuit diagram of the voltage amplifier in the center-frequency control circuit.

where C_f is the feedback capacitor of the voltage amplifier with the voltage gain $-A_f$. Due to the Miller effect, the effective capacitance C_{eff} at the input terminal of the voltage amplifier becomes $(1+A_f)C_f$. By tuning the value of $-A_f$, the effective capacitance C_{eff} can be tuned to compensate for the deviations of the center frequency.

In the design of the voltage amplifier, tuning range of $-A_f$ should be large enough to obtain the desired tuning range of center frequency. In addition, the output impedance of the voltage amplifier should be kept low to minimize its resistive loading to other stages. The voltage amplifier in this design is shown in Fig. 6 where a resistor-load common-source stage is connected to a resistor-load source follower. The voltage gain of the amplifier is

$$-A_f = -g_{m6}R_6K_7 \tag{4}$$

where K_7 is the gain of the source follower and R_6 and g_{m6} are the load resistance and transconductance of the common-source stage, respectively. The voltage gain $-A_f$ can be tuned through the tuning of g_{m6}, which is accomplished by changing the source control voltage V_F of the transistor M_6. It is noted that both the source of M_6 and the resistor R_7 are connected to V_F to realize the g_m tuning and reduce the power dissipation.

IV. Design Considerations

A. Design Equations

The block diagram of the proposed bandpass amplifier is illustrated in Fig. 7 where the Q-enhancement circuit and center frequency control circuit are connected in parallel between tuned amplifier and output buffer. The corresponding circuit diagram is shown in Fig. 8 where the circuits introduced in Section III are used. In Fig. 8, the bias transistors M_{10} and M_{11} are used to bias the tuned amplifier. The transconductance g_{m10} of M_{10} and the output resistance r_{o11} of M_{11} determine the input resistance of the circuit. Since $r_{o11} \gg 1/g_{m10}$, the contribution of r_{o11} to both input resistance and noise figure can be neglected. R_S and C_B are antenna termination resistance and dc blocking capacitor, respectively. The output buffer formed by two cascaded resistor-load source followers has a voltage gain of A_{buffer}. The tuning of center frequency and quality factor are realized through the tuning of bias voltages V_F and V_Q, respectively.

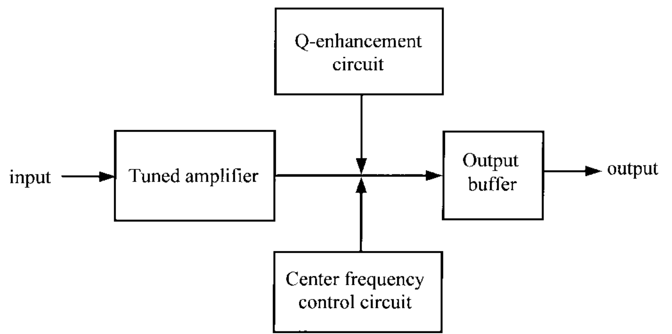


Fig. 7. Block diagram of the proposed bandpass amplifier.

The center frequency f_0, quality factor Q, input resistance R_i, voltage gain A_v at f_0, and noise factor F at f_0 can be derived under the first-order approximation as

$$f_0 = \frac{1}{2\pi\sqrt{L_pC_{\text{tot}}}} \tag{5}$$

$$Q = \frac{1}{G_{\text{tot}}}\sqrt{\frac{C_{\text{tot}}}{L_p}} \tag{6}$$

$$R_i = \frac{1}{g_{m10}} \tag{7}$$

$$A_v = -\frac{R_i}{R_S+R_i}\frac{g_{m1}}{G_{\text{tot}}}A_{\text{buffer}} \tag{8}$$

$$F = 1 + \frac{2}{3}(g_{m10}+g_{m11})R_S + \frac{2}{3}\frac{(1+g_{m10}R_S)^2}{R_Sg_{m1}} \cdot \left\{1 + \frac{g_{m4}}{g_{m1}^2(g_{m3}+g_{m4})}[g_{m3}+g_{m4}g_{m5}]\right\} \tag{9}$$

where g_{mi} is the transconductance of the transistor M_i, and L_p is 4.1 nH at 900 MHz. Note that (5)–(9) give sufficient accuracy for hand calculation and can be used as the design guidelines to determine or adjust the parameters in the circuit simulations.

In the above design equations, C_{tot} consists of the tunable capacitance $(1+A_f)C_f$ and the parasitic capacitance C_1, and the terminal capacitance C' of the MOS devices. Thus

$$C_{\text{tot}} = (1+A_f)C_f + C_1 + C'. \tag{10}$$

Due to the strong dependence of f_0 on the parasitic capacitance C_1, more precise simulation with the parasitic capacitances extracted from the circuit layout is necessary.

The advantage of incorporating the Q-enhancement circuit with the bandpass amplifier can be seen by evaluating the value

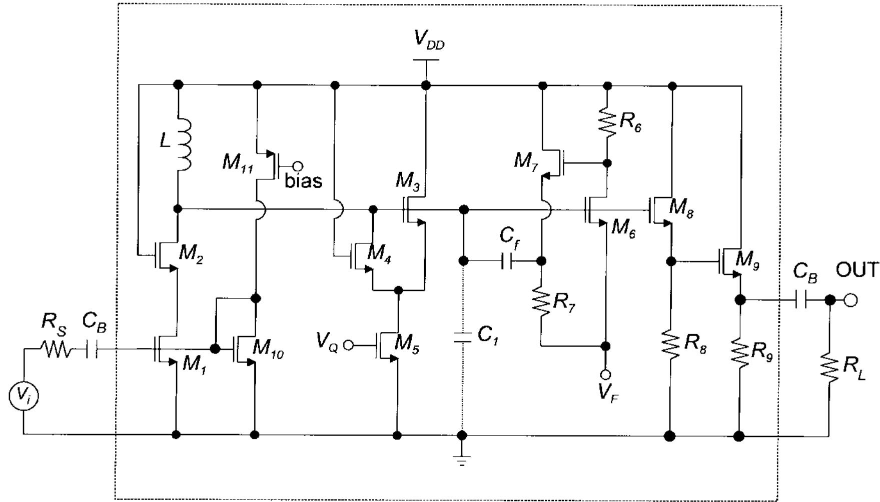


Fig. 8. Overall circuit diagram of the bandpass amplifier.

of g_{m1} from (5)–(8). At the center frequency of 900 MHz, the required value of $C_{\rm tot}$ is 7.62 pF from (5). Under the specifications $A_v = 16$ dB at $Q = 30$ and $L_p = 4.1$ nH in this design, the resultant $G_{\rm tot}$ is 1.43×10^{-3} ℧ in (6). Then substituting $A_v = 3.16$, $R_S = R_i = 50\,\Omega$, $A_{\rm buffer} = 0.5$, and $G_{\rm tot} = 1.43 \times 10^{-3}$ ℧ into (8), the resultant g_{m1} is 1.8×10^{-2} ℧. This value of g_{m1} is 4.4 times lower than that required in the amplifier without Q-enhancement circuit as calculated in Section III. Thus, high Q and high gain can be obtained with a lower value of g_{m1}. Although the Q-enhancement circuit consumes power too, the total power dissipation is still lower than that without Q-enhancement circuit.

B. Simulation Techniques

The circuit simulations based on the conventional device model have been found to have limited accuracy in the 900 MHz frequency band. In order to obtain more accurate simulation results, an extended wide-channel MOS model is employed [26] which replaces each large MOS device by ten smaller MOS devices connected by the gate polysilicon resistances of MOS devices. The major difference between wide-channel model and conventional model is that the wide-channel model takes into account the effect of gate poly resistances of MOS devices, which produce considerable thermal noise and are important in the noise performance simulations. Thus, the noise simulations with the conventional model could lead to inflated results.

The simulation model of the inductor is based on an extended multisection equivalent circuit model developed by the authors [22], which has been proved to have high accuracy in modeling the high frequency behavior of the inductors on silicon substrate. In the whole circuit simulations, the parasitic capacitances extracted from the circuit layout are considered. To determine the component values and transistor dimensions of the circuit, many trade-offs among f_0, A_v, R_i, F, and power dissipation should be encountered. Therefore, iterative tuning and simulation of each circuit component is necessary to obtain the optimal performance. After the optimization, the component values and device dimensions are summarized in Table I. From the simulation results, it is shown that the proposed bandpass amplifier has tunable center frequency between 933–966 MHz, 10 dB power gain, and 5.8 dB noise figure when tuned at $Q = 30$.

TABLE I
COMPONENT VALUES AND DEVICE DIMENSIONS OF THE BANDPASS AMPLIFIER

PARAMETERS	VALUE
$(W/L)_1$	1560/0.8
$(W/L)_2$	780/0.8
$(W/L)_3$	2400/0.8
$(W/L)_4$	800/0.8
$(W/L)_5$	400/0.8
$(W/L)_6$	300/0.8
$(W/L)_7$	300/0.8
$(W/L)_8$	200/0.8
$(W/L)_9$	200/0.8
$(W/L)_{10}$	200/0.8
$(W/L)_{11}$	80/0.8
C_f	1 pF
R_6	300 Ω
R_7	20 Ω
R_8	1.2 kΩ
R_9	180 Ω

C. Q-Tuning Limit

The Q-tuning limit encountered in this circuit is caused by the instability of the positive feedback network for negative conductance generation. As in (2), the total conductance $G_{\rm tot}$ is the sum of the negative conductance $-G_n$ and the parallel conductance G_L of the inductor. If $|-G_n|$ is tuned to be equal to G_L, $G_{\rm tot}$ is zero and Q is infinite as in (6). Thus, the amplifier starts to enter the unstable region. If $|-G_n| > G_L$, the value of $G_{\rm tot}$ becomes negative and the transfer function of the amplifier has right-half-plane (RHP) poles s_1 and s_2 expressed as

$$s_1, s_2 = \frac{|G_{\rm tot}|}{2C_{\rm tot}} \pm \sqrt{\frac{1}{L_pC_{\rm tot}} - \left(\frac{|G_{\rm tot}|}{2C_{\rm tot}}\right)^2}. \qquad (11)$$

In this case, the amplifier is unstable.

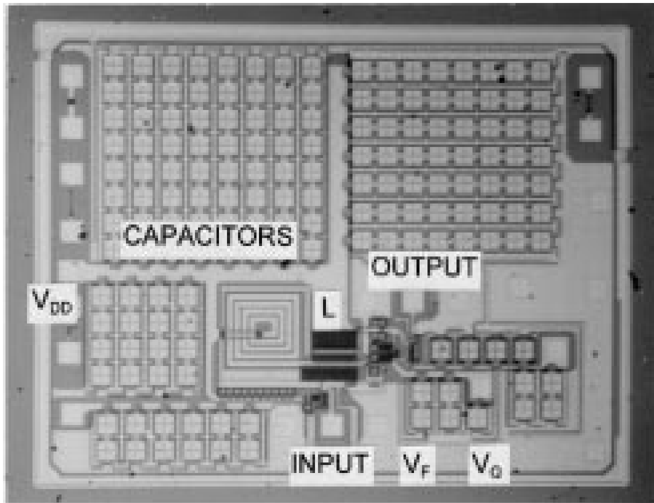


Fig. 9. The microphotograph of the fabricated bandpass amplifier.

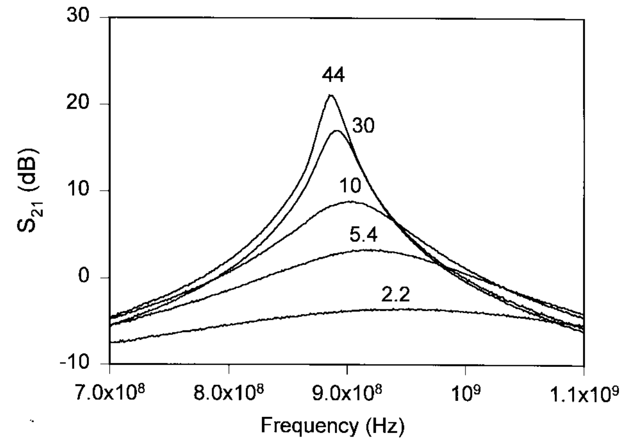
Since the values of G_L and G_n are frequency dependent, so is $G_{\rm tot}$. When the amplifier is tuned to the high Q condition, $|-G_n(jw_0)| \approx G_L(jw_0)$ at the center frequency f_0. Under this condition, the amplifier is stable at f_0. But at some frequency w around $f_0, |-G_n(jw)| > G_L(jw)$ could occur and the total conductance $G_{\rm tot}$ becomes negative. In this case, the input impedance of the amplifier is also negative and S_{11} is higher than 0 dB. Since a stable circuit requires both S_{11} and S_{22} below 0 dB at all frequencies, the maximum stable quality factor of the amplifier is the value of Q when $S_{11} > 0$ dB occurs. Note that the high-frequency spurious signals in the circuit may have positive feedback and become unstable. This may further degrade the maximum stable quality factor.

D. Layout Consideration

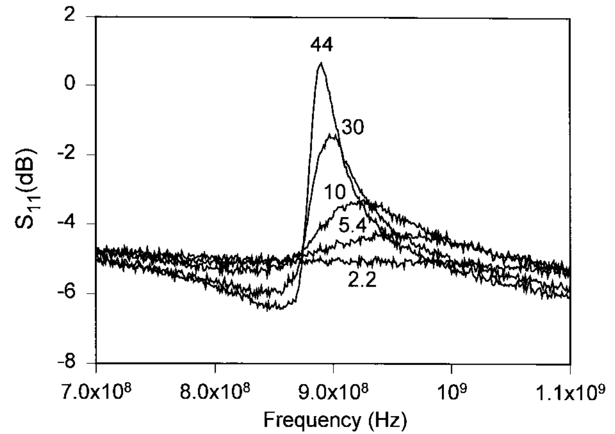
The chip layout plays an important role in the high-frequency circuits design. The unsuitable circuit layout may drastically degrade the circuit performance due to the increasing induced or coupled noise. To obtain the desired performance, the following guidelines are followed in the layout design.

- All active devices are surrounded by grounded p^+ guard rings to minimize the substrate noise and reduce the coupling among the devices.
- All interconnections are made by metal layer to minimize parasitic resistance.
- All MOS devices have minimum gate length of 0.8 μm to reduce the terminal capacitances.
- Ground connections are carefully routed to prevent the ground loop.

Furthermore, in order to reduce inductive parasitics of the power lines, all voltage bias or power supply nodes are connected with large on-chip bypass capacitors which are made by connecting many unit interpoly capacitors in parallel to reduce terminal series resistances. Since the capacitors may occupy large chip area, the value of each bypass capacitor is optimized through simulations to obtain the maximum performance/area ratio. The bypass capacitances at the nodes V_{DD}, V_F, V_Q, and the gate bias of M_{11} are 796, 46.4, 29, and 69.6 pF, respectively.



(a)



(b)

Fig. 10. The measured (a) S_{21} magnitude and (b) S_{11} magnitude of the fabricated amplifier tuned at different Q values.

V. Experimental Results

The bandpass amplifier was fabricated by 0.8-μm N-well double-poly-double-metal CMOS technology. The resistors R_6–R_9 in the circuit are implemented by poly resistors. The microphotograph of the experimental chip is shown in Fig. 9. The measurements were performed by wafer probing systems with on-chip calibration technique. The nominal supply voltage of the fabricated amplifier is 3 V. As the supply voltage is below 3 V, both circuit gain and linearity are degraded.

The measured S_{21} and S_{11} of the fabricated amplifier tuned at different Q values are given in Fig. 10(a) and (b), respectively. In these measurements, the center frequency control circuit is disabled and the Q-enhancement circuit is tuned by increasing the Q-tuning bias voltage V_Q from 0.7–1.08 V. When $V_Q = 0.7$ V, the Q-enhancement circuit is disabled and the inherent Q is 2.2, which is lower than the Q value (2.9) of the integrated inductor because of the resistive parasitics in the circuit. As V_Q increases, both quality factor and amplifier gain S_{21} are increased due to the increased positive feedback. However, the peak of S_{11} is also increased at the same time. In Fig. 10(b), the S_{11} peak crosses 0 dB

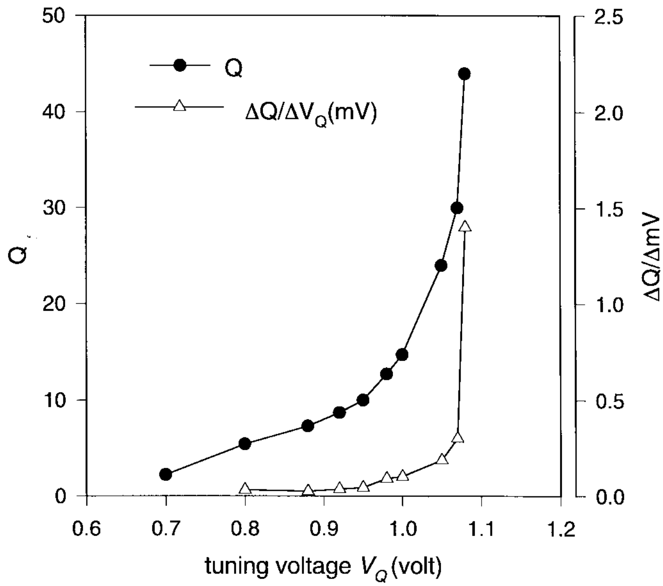


Fig. 11. The measured Q and Q-tuning sensitivity $\Delta Q/\Delta V_Q$ (mV) versus tuning voltage V_Q of the fabricated bandpass amplifier.

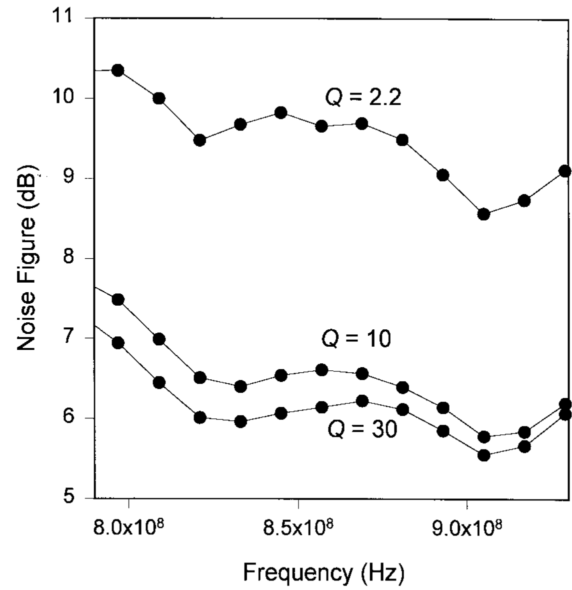


Fig. 12. The measured noise figures of the fabricated amplifier tuned at $Q = 30$ and $Q = 10$.

when the quality factor is 44 with $V_Q = 1.08$ V. This means the circuit is unstable if $Q > 44$ and the maximum stable Q is 44.

A plot of the measured Q and Q-tuning sensitivity $\Delta Q/\Delta V_Q$ (mV) versus V_Q is shown in Fig. 11. As seen in Fig. 11, Q is more sensitive to the variation of V_Q when the Q is tuned higher. In the measurement of $Q = 30 \pm 3$, the required accuracy of V_Q is ± 10 mV. Both threshold voltage and resistance variations in the circuit affect the accuracy of tuning voltage. The measurement results have shown that, under a fixed tuning voltage $V_Q = 1.06$ V, the variation of $Q = 30$ among 40% chips is $\pm 15\%$. The chip-to-chip Q variations can be reduced by proper layout technique. Moreover, both Q-tuning sensitivity and Q variations can be reduced by using the current tuning through a current mirror to adjust the voltage V_{gs5}.

Since the bandpass filtering function of the proposed amplifier has second-order characteristics, the out-of-passband attenuation is not so high as that in high-order filters. As can be seen from Fig. 10(a), the amplifier gain at the frequencies smaller than 800 MHz or greater than 1 GHz is below 0 dB, and it changes slightly as Q is varied. Thus, when the bandpass amplifier is applied to a dual-conversion receiver with 70–100 MHz IF, the image filter is still required.

As Q is tuned from 2.2–30, the peak gain increases from -3.4 to 17 dB, the center frequency decreases from 951 MHz to 893 MHz, and the total dc current increases from 13.9 to 24.1 mA. Because the amplifier characteristics strongly depend on Q, the following measurement results are obtained with Q fixed at 30. In some cases, the measured results with Q tuned at ten are also given for comparison.

The measured noise figures of the fabricated amplifier with $Q = 30$ and $Q = 10$ are shown in Fig. 12. As seen from Fig. 12, NF is about 6.0 dB around the center frequency. As Q decreases, NF increases. This is because the decreased Q leads to the decreased amplifier gain. Thus, the noise

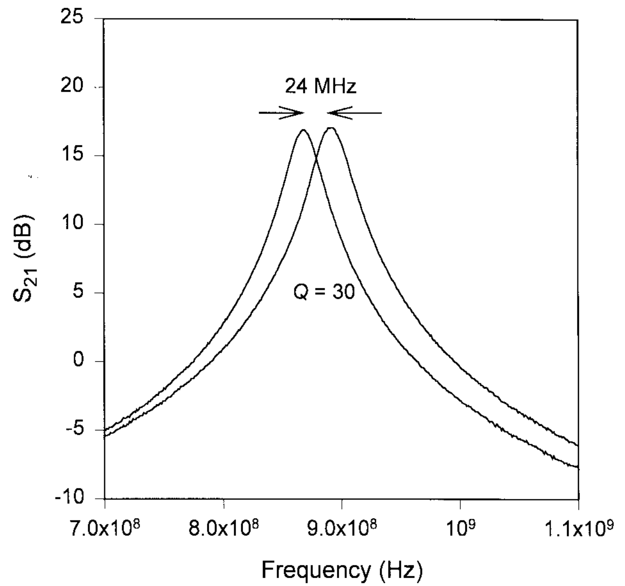
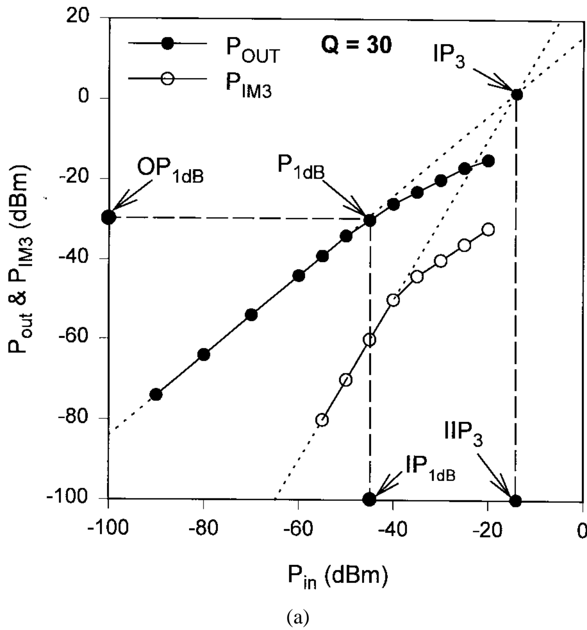


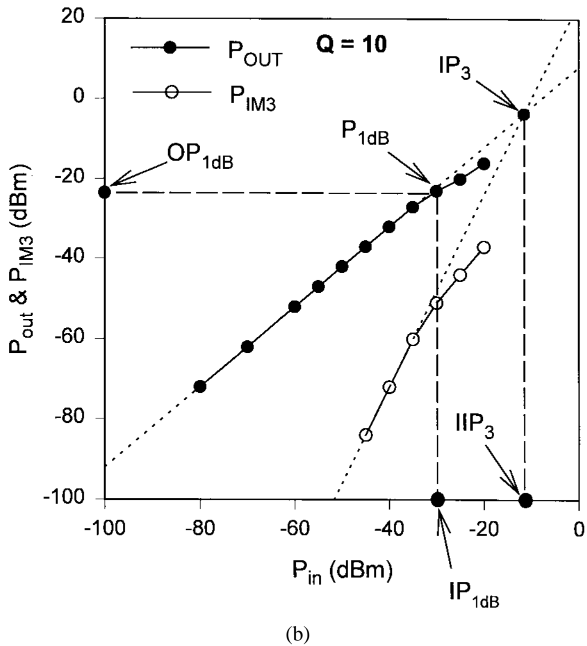
Fig. 13. The measured frequency response of the fabricated amplifier tuned at maximum and minimum center frequencies with the same Q of 30.

contributed by the devices after the gain stage is increased and NF is increased. Comparing the measured NF (6.1 dB) to the simulated value (5.8 dB) under the same gain of 10 dB, the deviation is 4.8%.

The center-frequency tuning range of the fabricated amplifier is illustrated in Fig. 13 where the measured S_{21} at maximum and minimum f_0 with the same Q of 30 are given. As seen from Fig. 13, the tunable range is 24 MHz from 869–893 MHz. If Q is decreased to ten, f_0 can be increased to 905 MHz and the tunable range of f_0 remains almost the same. Comparing the measured maximum frequency (893 MHz) to the simulated value (966 MHz) at $Q = 30$, the deviation is 8.2%. Note that the tuning of f_0 is dependent upon that of Q. Therefore, iterative tunings of V_Q and V_F are required to obtain a specified set of f_0 and Q.



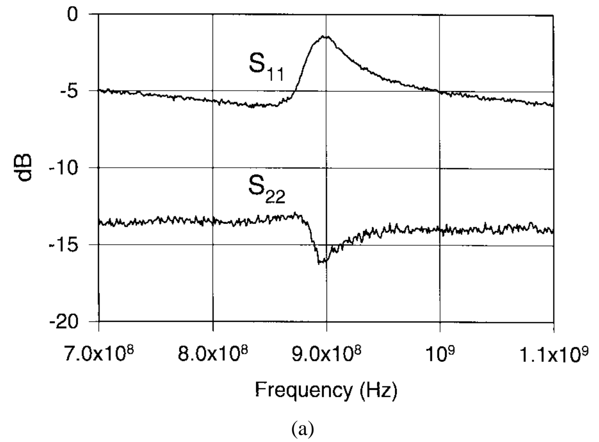
(a)



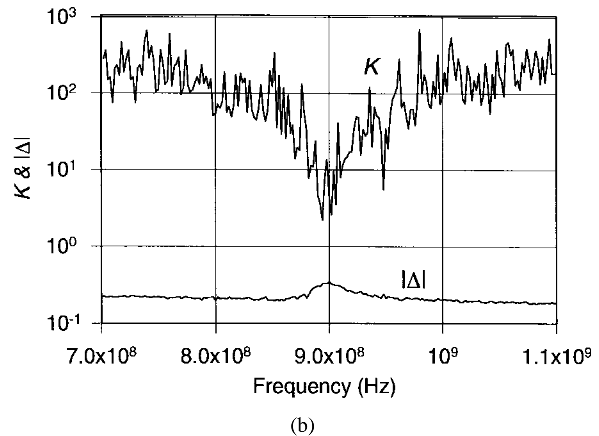
(b)

Fig. 14. The measured $P_{\rm OUT}$ and P_{IM3} versus $P_{\rm in}$ of the fabricated amplifier tuned at (a) $Q = 30$ and (b) $Q = 10$.

The linearity measurement results of the circuit tuned at $Q = 30$ and $Q = 10$ are given in Fig. 14(a) and (b), respectively. These plots are obtained by applying two sinusoidal signals of equal power $P_{\rm in}$ and different frequencies f_1 and f_2 to the amplifier and measuring the output power spectra $P_{\rm OUT}$ at frequencies f_1 and P_{IM3} at $2f_2 - f_1$ versus input power $P_{\rm in}$. In the measurement of $Q = 30$ (10), the two-tone frequencies f_1 and f_2 are 893 (905) MHz and 897 (909) MHz, respectively, and the third-order intermodulation frequency $2f_2 - f_1$ is 901 (913) MHz. Note that all the frequencies f_1, f_2, and $2f_2 - f_1$ fall in the passband of the amplifier. In Fig. 14(a) and (b), the corresponding 1 dB compression points $P_{1\,\rm dB}$ and third-order intercept points $\rm IP_3$ are indicated. As can be seen from the figures, the measured output 1 dB compression point



(a)



(b)

Fig. 15. The measured (a) S_{11} and S_{22} and (b) K and $|\Delta|$ of the fabricated amplifier tuned at $Q = 30$.

$OP_{1\,\rm dB}$ and third-order input intercept point $\rm IIP_3$ at $Q = 30$ (10) are -30 (-23) dBm and -14 (-12) dBm, respectively. The linearity is degraded with the increased Q because of the increased positive feedback.

The dynamic range of the circuit is measured by the input 1 dB compression point ($IP_{1\,\rm dB}$). In Fig. 14(a) and (b), the values of $IP_{1\,\rm dB}$ at $Q = 30$ and $Q = 10$ are -47 and -31 dBm, respectively. The dynamic range of the active Q-enhancement circuit is limited by the inherent Q of the circuit [24], which is 2.2 as in Fig. 10(a). Higher dynamic range can be obtained by increasing the inherent Q, which can be done by using a high-Q inductor or reducing the resistive loading of the circuit. In most cases, the Q of integrated inductors cannot be increased without modifying the fabrication process. Thus, the only way to improve the dynamic range is to reduce the resistive loading. In the circuit of Fig. 8, reducing the value of R_7 decreases the resistive loading. However, the tuning range of f_0 is also decreased. Thus, one should trade off between dynamic range and tuning range of f_0. In this case, $IP_{1\,\rm dB} = -47$ dBm is obtained with the f_0 tuning range of 24 MHz.

The measured matching characteristics S_{11} and S_{22} and stability factor K and $|\Delta|$ of the circuit tuned at $Q = 30$ are given in Fig. 15(a) and (b), respectively. As seen in Fig. 15(a), S_{22} is below -13 dB at all frequencies. This means the output impedance is well matched to 50 Ω. As

TABLE II
MEASUREMENT RESULTS OF THE BANDPASS AMPLIFIER

PARAMETER		VALUE
Supply Voltage		3 V
Quality Factor		2.2 – 44
Q = 30	Power Gain	17 dB
	Center Frequency	869 MHz - 893 MHz
	Noise Figure	6.0 dB
	OP_{1dB}	-30 dBm
	IIP_3	-14 dBm
	S_{11}	< -1.8 dB
	S_{22}	< -13 dB
	DC Power	78 mW

Q is tuned, S_{22} is only slightly changed due to the good output isolation offered by the double-buffer output stage. On the other hand, the input terminal is not well matched due to the trade-off between S_{11} and NF. As in (7), good input matching requires the transconductance $g_{m10} \cong 1/50$ ℧. This value of g_{m10} would produce considerable noise and degrade the overall noise figure as in (9). In order to keep the NF within the specification, the value of g_{m10} is set to a lower value to reduce the noise effect. Therefore, the external input matching circuit is required to obtain the minimum input return loss. An LC network contains a series inductor of 11 nH and a parallel capacitor of 6 pF at the source end can be used as the external matching circuit to match the input impedance. The simulation results have shown that with the LC input matching circuit, S_{11} is lower than -12 dB in the passband. The other parameters such as f_0, Q, gain, and NF change slightly after adding the matching network because the response of the amplifier is mainly determined by the internal circuit and the lossless LC elements do not contribute thermal noise. As shown in Fig. 15(b), the required conditions for an unconditional stable system, $K > 1$ and $|\Delta| < 1$, are met in this design. The measurement results of the fabricated CMOS bandpass amplifier are summarized in Table II.

VI. CONCLUSION

A bandpass amplifier has been successfully designed and fabricated by using 0.8-μm CMOS technology. Incorporating both Q-enhancement circuit and center-frequency control circuit with the tuned bandpass amplifier, the limiting factors in CMOS RF design can be overcome and the amplifier performance can be improved. In performing high-frequency circuit simulation for the proposed amplifier, wide-channel MOS model and multisection inductor model are used to minimize the simulation errors. The performance of the experimental chip has been verified, which can meet the requirement of 900 MHz wireless receivers. Thus, the proposed bandpass amplifier can perform the functions of LNA and band filter in conventional 900 MHz front-end circuits. Moreover, it is quite feasible to use the amplifier in the high-integration all-CMOS receivers.

In the future, high-order bandpass amplifier design and the integration of other RF components in CMOS will be conducted.

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