Innovative Voltage Driving Pixel Circuit Using Organic Thin-Film Transistor for AMOLEDs

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***Abstract*—In this work, we propose a novel active-matrix organic light-emitting diode displays (AMOLED) pixel circuit based on organic thin-film transistor (OTFT) architecture, which consisted of four switches, one driving transistor, and a capacitor. The pentacene-based OTFT device possesses a field-effect mobility of 0.1 $cm^2/V \cdot s$, a threshold voltage of −1.5 V, subthreshold slope of 1.8 V/decade and an on/off current ratio 10^6. The resultant voltage-driving pixel circuit, named "Complementary Voltage-Induced Coupling Driving" (CVICD), is different from the current-driving scheme and can appropriately operate at low gray level for the low-mobility OTFT circuitry. The current non-uniformity less than 2.9% is achieved for data voltage ranging from 1 to 17 V by SPICE simulation work. In addition, the new external driving method can effectively reduce the complexity of OLED pixel circuitry.**

***Index Terms*—Active-matrix organic light-emitting diode displays (AMOLEDs), organic thin-film transistor (OTFT), SPICE simulation.**

I. Introduction

ORGANIC thin-film transistors (OTFTs) have attracted much attentions and been widely studied because they have many potential applications, such as liquid crystal display panels, sensors, postage stamps, RFID, and flexible electronics [1]–[3]. Most research reports related to the performance of OTFTs have focused on the field-effect mobility, low operating voltage, low subthreshold swing, and a threshold voltage close to 0 V [4]–[7]. Among many disclosed organic semiconductor materials, the pentacene-based OTFT has attracted lots of interest to be used for active-matrix organic light-emitting diode displays (AMOLEDs) [8]–[10]. However, it also has been reported that the OTFT device is subjected to environmental and bias stress instability [11], [12]. The threshold voltage variations of the OTFT device originated from manufacture processes and electrical bias operation are critical issues for the image quality of AMOLED panels over the operation time. Besides, the OTFT devices fabricated in low-temperature processes generally exhibits a low mobility less than 0.5 $cm^2/V \cdot s$, thus leading to the limit in the design of pixel circuitry [13], [14]. The development of compensation circuits suitable for the low-mobility OTFT architecture is, thereby, important to gain a proper electrical operation scheme and maintain a constant driving current for the AMOLED applications. Nevertheless, few appropriate pixel circuits have been presented for the OTFT-driving OLEDs in recent years, and most of proposed circuits employed the current driving schemes. The settling time issues lead the current-driving scheme to set a current ranging from 2 μA to 8 μA [15]–[17], which are not realizable values for the AMOLED to define the gray scales. Therefore, we propose a voltage-driving compensation circuit in this study to well solve both issues of low field-effect mobility and threshold voltage variations for the OTFT-driving OLEDs.

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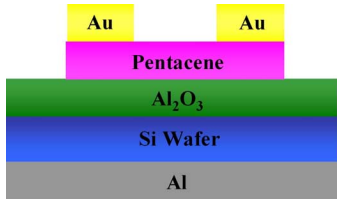

Fig. 1. Cross-sectional diagram of the proposed pentacene-based OTFT device with top contacts and bottom gate structure.

II. OTFT Fabrication Processes and Electrical Parameter Extraction

Fig. 1 shows the schematic cross section of the pentacene-based OTFT device with top contacts and a bottom gate. The fabrication processes of the pentacene-based OTFT were described subsequently. A layer of 240-nm-thick Al_2O_3 film was electron-gun deposited on p-type silicon wafers. Then, a 70-nm-thick pentacene layer was thermally evaporated and patterned through a shallow mask at a rate of 0.5 Å/s. It was followed a 100-nm-thick gold (Au) layer was thermally evaporated onto the pentacene film through a shallow mask to form the source and drain electrodes with normal channel width/length $(W/L) = 800\ \mu m/200\ \mu m$. Finally, 300-nm-thick Al gate electrodes were thermally evaporated on the backside of silicon wafers for the enhancement of gate voltage coupling.

These methods for the extraction of the field-effect mobility, threshold voltage, sun-threshold swing, and the on/off current ratio were characterized, respectively, as described in Section II-A–D.

A. Mobility

The field-effect mobility can be extracted from the transconductance g_m in the linear region [18]

$$g_m = \left[\frac{\partial I_D}{\partial V_G}\right]_{V_D=\text{CONSTANT}} = \frac{WC_{OX}}{L}\mu V_D \qquad (1)$$

where $C_{\rm OX}$ is the oxide capacitance per unit area and μ is the field effect mobility.

B. Threshold Voltage

The threshold voltage ($V_{\rm t}$) is related to the operation voltage and the power consumptions of an AMOLED display pixel circuit. We extracted the threshold voltage from (2), the intersection point of the square root of drain current versus gate voltage when the device operated in the saturation mode [18]. For $-V_{\rm D} > -(V_{\rm G} - V_{\rm t})$

$$\sqrt{I_{\rm D}} = \sqrt{\frac{W}{2L}\mu C_{ox}(V_{\rm G} - V_{\rm t})}. \quad (2)$$

C. Sub-Threshold Slope

The sub-threshold slope is also one of important electrical characteristics for device application. It is a measure of how rapidly the device switches from the off-state to the on-state. Besides, the sub-threshold swing also represents the interface quality and the defect density[18].

$$S = \left[\frac{\partial V_{\rm G}}{\partial(\log I_{\rm D})}\right]_{V_{\rm D}={\rm CONSTANT}}, \text{ when } |V_{\rm G}| < |V_{\rm t}|. \quad (3)$$

D. On/Off Current Ratio

OTFT devices with high on/off current ratio can represent high turn-on current and low off-state current. It determines the gray-level switching of the displays. High on/off current ratio means the TFT device can provide enough turn-on current to drive the pixel and sufficiently low off current to reduce power consumption.

III. Measurement and Spice Model of OTFT

Fig. 2(a) and (b) shows the transfer and output characteristics of the OTFT devices, respectively. The mobility of pentacene-based OTFT device was about 0.1 $\rm cm^2/V\cdot s$, subthreshold slope 1.8 V/decade, threshold voltage -1.5 V and on/off ratio 10^6. We use Level 62 TFT RPI model to fit the curve for HSPICE simulation. Fig. 3 shows the measured and simulated characteristics of the OTFT devices. These modeling results were employed for further circuit simulation. Comparisons show that the maximum rms error of extracted electrical parameters is less than a 4% of accuracy. Compared with the $I_{\rm D}$ while $V_{\rm G} = -20$ V, however, there is a mismatch occurred in the deep saturation region due to the intrinsic limitation of the RPI TFT model. One of reason is that the RPI mobility function fails at the high gate bias conditions [19]. Therefore the mobility function loses the accuracy at the high gate biased condition. The error is increased when the gate bias is increased. In this work, however, it is not matter because we just use the well matched linear region for the switch operation at the high gate bias conditions.

IV. Pixel Circuit Schematic and Operation

Fig. 4 depicts a schematic diagram of the proposed pixel circuitry. The inner of the dash square indicates a pixel region with a p-channel driving OTFT device TD, and four switch OTFT

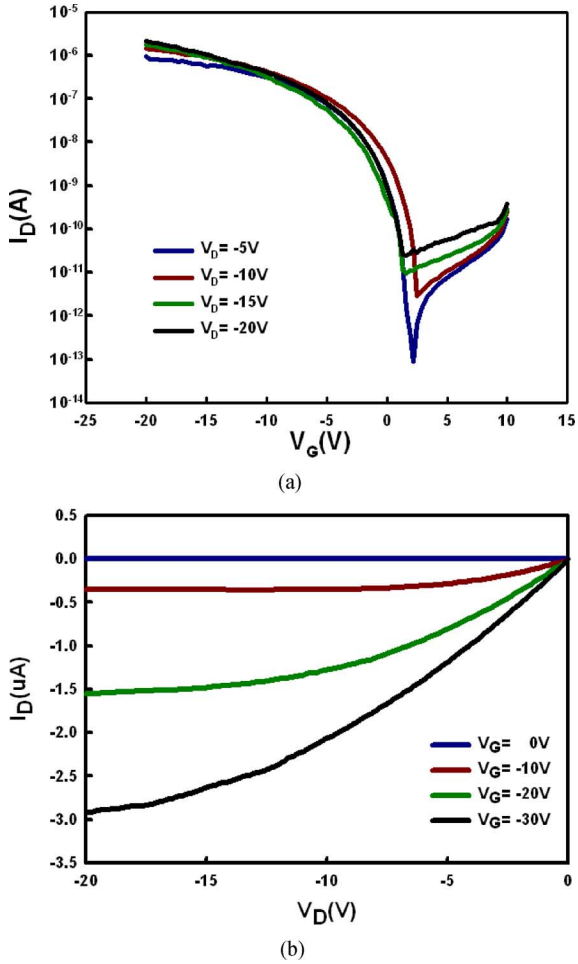

Fig. 2. (a) $I_{\rm D} - V_{\rm G}$ transfer and (b) $I_{\rm D} - V_{\rm D}$ output characteristics of the pentacene-based TFT devices.

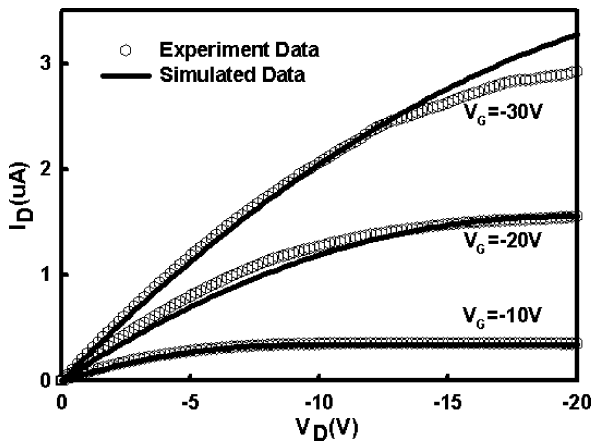

Fig. 3. Measured and simulated characteristics of the pentacene-based OTFT devices.

transistors T1, T2, T3, and T4. The switch OTFT transistor T5 is designed to be outside the pixel area. The operation principle can be divided into three periods, including releasing charge, threshold voltage generation and emission. In the first period, SCAN1 and SCAN2 are set to low to turn on the p-channel OTFTs T1, T2, and T3. T4 is in the powered off state and T5 is controlled at on state, respectively. In this period, the data

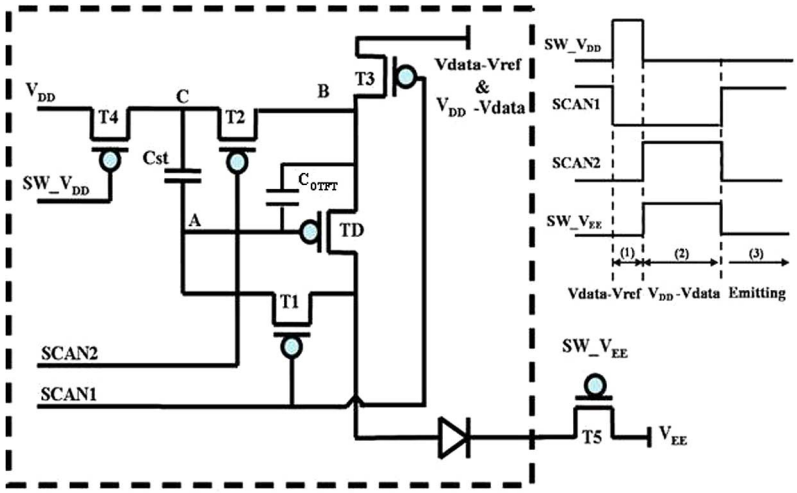

Fig. 4. Schematic of the proposed pixel circuit and controlling signals. The inner of the dash square indicates a pixel region with a p-channel driving OTFT device TD and four switch OTFT transistors T1, T2, T3, and T4. $V_{\rm DD}$ and $V_{\rm EE}$ were 0 V and -35 V, respectively. $\rm SW\_V_{DD}$, $\rm SW\_V_{EE}$, SCAN1, and SCAN2 were ranging between -45 V and 5 V.

voltage ($= V_{\rm data} - V_{\rm ref}$) is applied to node B ($V_{\rm B}$), and node A ($V_{\rm A}$) goes to $V_{\rm EE} + V_{\rm OLED}$. The layout of switch T5 was outside each pixel area and connected separately to each patterned cathode [20]. Therefore, the actual device layout in a pixel region consists of five transistors, especially suitable for the top-emission OLED pixel architecture. Such an arrangement of external driving circuit can decrease the manufacture complexity for each display pixel.

In the $V_{\rm t}$ generation period, SCAN1 is still kept low, T1 and T3 are kept in the turn-on state. SCAN2 goes high to turn T2 off, and T4 and T5 are changed to the on and off state, respectively. The data line is given $V_{\rm DD} - V_{\rm data}$. Because T4 is turned on and the voltage of data line changes, the voltage of node A ($V_{\rm A}$) is suffered feed through [21] in the meanwhile and is boosted to a higher voltage level.

$$V_{\rm A} = V_{\rm EE} + V_{\rm OLED} + (V_{\rm DD} - (V_{\rm data} - V_{\rm ref})) \times \frac{\rm C_{st}}{\rm C_{st} + C_{OTFT}} + ((V_{\rm DD} - V_{\rm data}) - (V_{\rm data} - V_{\rm ref})) \times \frac{C_{\rm OTFT}}{\rm C_{st} + C_{OTFT}} \quad (4)$$

where $\rm C_{st} \gg C_{OTFT}$, and $\rm C_{OTFT}$ is the parasitic capacitance of TD. For different input data, the corresponding threshold voltage generation period can be effectively decreased due to the voltage boost effect. It means a high level of data voltage in the first period, for example $V_{\rm DD} = 0$ V, $V_{\rm data} = 15$ V, and $V_{\rm ref} = 17$ V, then $V_{\rm DD} - (V_{\rm data} - V_{\rm ref}) = 2$ V. The voltage of node A ($V_{\rm A}$) has small boost effect. On the other hand, if a low level of data voltage is given, it will produce relatively high boost effect. In this case, $V_{\rm DD} = 0$ V, $V_{\rm data} = 2$ V, and $V_{\rm ref} = 17$ V, then $V_{\rm DD} - (V_{\rm data} - V_{\rm ref}) = 15$ V. The driving scheme is referred to as "Complementary Voltage-Induced Coupling Driving" (CVICD). We also designed a single RC series circuit to verify the concept of the proposed CVICD. In this condition, $\rm R = 10\ \Omega$, $C = 10\ \mu$F and $Vs = 10 \times \rm u(t)V$, where $\rm u(t)$ is a unit function. It takes 230 μs and 160 μs from capacitor voltage 0–9 V and 5–9 V (9 V is 90% of Vs), respectively. The time difference between the two initial conditions is 70 μs.

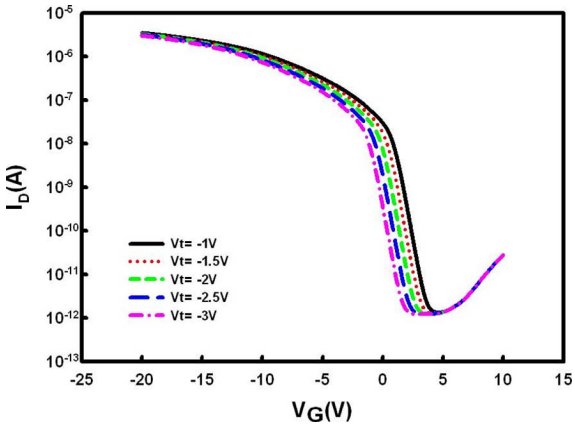

Fig. 5. The simulated $\rm I_D - V_G$ characteristics of OTFT devices with the $V_{\rm t}$ shift between ¡Ó1 V, while $V_{\rm D}$ was set to -10 V.

Thus, the CVICD method can decrease the charging time effectively. At the end of the $V_{\rm t}$ generation duration, $V_{\rm A}$ will settle to $V_{\rm DD} - V_{\rm data} - |V_{\rm t}|$.

In the driving period, SCAN1 is set to high to turn off T1 and T3. At the same time, SCAN2 is set to low to turn T2 on. Both T4 and T5 are at the on-state. At this moment, the source voltage of TD is $V_{\rm DD}$, then the voltage of storage capacitor is shown as

$$\begin{aligned} V_{\rm SC} &= V_{\rm DD} - (V_{\rm DD} - V_{\rm data} - |V_{\rm t}|) = V_{\rm data} + |V_{\rm t}| \\ \rm I_{OLED} &= K(V_{SC} - |V_t|)^2 = K(V_{data} + |V_t| - |V_t|)^2 \\ &= K(V_{\rm data})^2. \end{aligned} \quad (5)$$

The above formula clearly indicates that the proposed compensation circuit includes higher immunity to the threshold voltage variation [22] and especially suitable for OTFT derived top-emission OLED pixel circuits.

V. Results and Discussion

The HSPICE software with the RPI model (Level = 62) were used to verify the proposed OTFT pixel circuit. Based on our transistor model, the simulated $I_{\rm D}$–$V_{\rm G}$ characteristics of OTFT devices with a threshold voltage shift of ± 1 V are shown in Fig. 5. In this simulation work, the ratio of channel width (W)

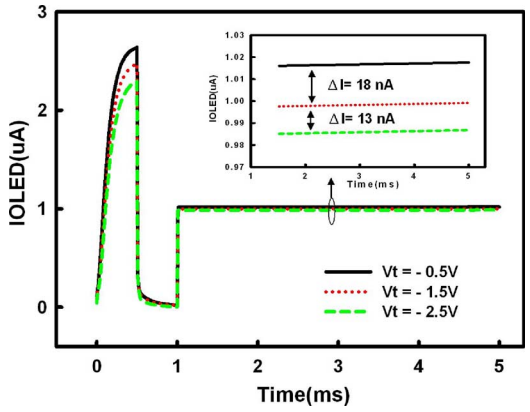

Fig. 6. Change of driving current (IOLED) versus operation time for the OTFTs with variant threshold voltages. IOLED is 1.016 μA, 0.998 μA, and 0.9852 μA for $V_{\rm t} = -0.5, -1.5,$ and -2.5 V, respectively.

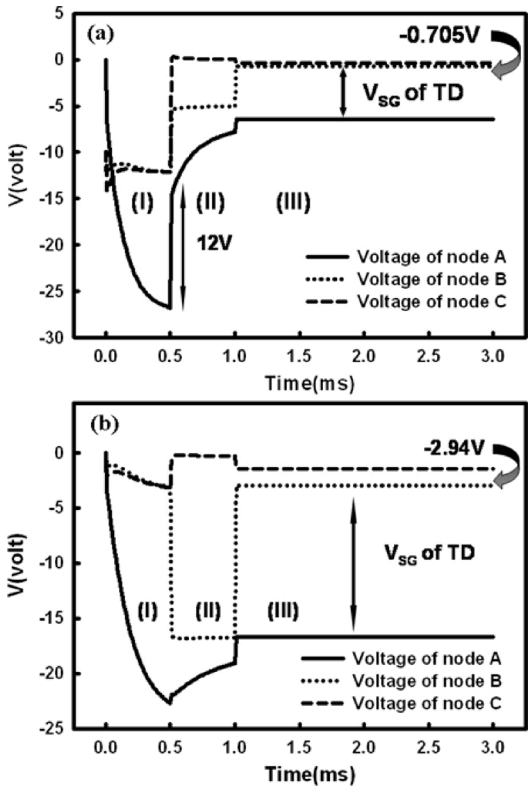

Fig. 7. Transient waveforms at specific nodes in the proposed pixel circuit while the input data was set to (a) $V_{\rm data} = 5$ V for generating 262 nA of driving current, and (b) $V_{\rm data} = 17$ V for generating 1 μA of driving current.

to channel length (L) for TD was 300 μm/50 μm, and switch T1 was 20 μm/40 μm designed to decrease the leakage current during the driving period, as well as other switch transistors were all set to 80 μm/10 μm. The storage capacitor was 5 pF. Fig. 6 shows the transition of driving current versus operation duration for the OTFTs with variant threshold voltages in the proposed pixel circuit architecture. The variation of driving current (ΔI) can be calculated to be less than 1.8%. This result shows the proposed pixel circuit can produce the extremely similar driving current of OTFTs, independent of the variation in threshold voltages.

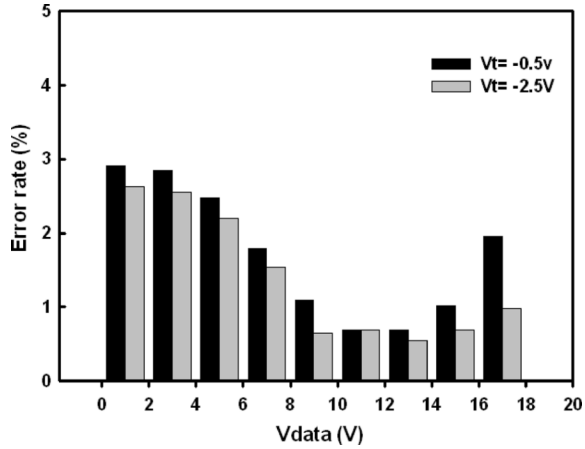

Fig. 8. Error rate of TD output current in our proposed pixel circuit due to the threshold voltage variation. The output current error is below 2.9% in our proposed pixel circuit when input data voltage is ranging from 1 to 17 V.

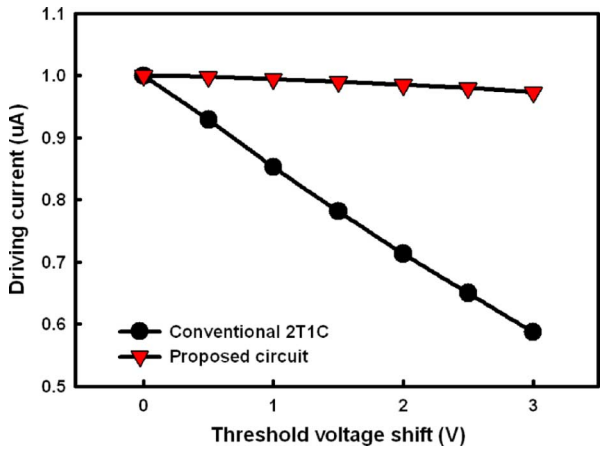

Fig. 9. Comparison of output driving current between the proposed pixel architecture and the conventional 2T1C circuit with different threshold voltage shifts.

Fig. 7(a) depicts the transient waveforms at specific nodes in the proposed pixel circuit while the input data voltage was set to 5 V for generating 262 nA of driving current. It is clearly observed an obvious voltage coupling effect, approximately 12 V coupling voltage produced in a short time period. It indicates the charging period is shortened and effectively reduce the $V_{\rm t}$ generation time, which is especially suitable for the OTFT devices with the low field-effect mobility. Also, a less coupling effect was demonstrated while input data voltage was set to 17 V for generating 1 μA of driving current, as shown in Fig. 7(b). The evolution of coupling effect corresponding to the different input data voltages (e.g., 17 and 5 V) is completely consistent with the proposed CVICD operation scheme. However, during the driving period (Regime III), Fig. 7(a) and (b) show the value of TD source voltage ($V_{\rm B}$) was -0.705 V and -2.94 V, separately, indicating $V_{\rm B}$ and $V_{\rm C}$ are deviated from the desirable $V_{\rm DD}$ level ($V_{\rm DD} = 0$ V). It is inferred the OTFT devices did not exhibit good current swing in the linear operation region due to the presence of high turn-on resistance. These undesirable effects are mainly originated from the characteristics of OTFT devices. Therefore, it gives us a future work to improve the electrical performance of the OTFT device. Fig. 8 presents the output current error of device TD while the data voltage ranges 1–17 V. The

output current error rate is below 2.9% in our proposed pixel circuit. The further comparison of output current between the proposed pixel circuit and the conventional one with 2T1C architecture is represented for threshold voltage shifts, shown in Fig. 9. This simulation result shows that the driving current in our proposed pixel architecture slightly degraded from 1 μA to 0.973 μA, while the one with a typical 2T1C scheme degraded severely to a value lower than 0.584 μA. These results surely indicate the excellent compensation ability can be effectively obtained to reduce the current non-uniformity via the application of the proposed CVICD pixel circuit.

VI. Conclusion

In this work, we have demonstrated the functionality of the proposed CVICD compensation circuit for OTFT-driving OLED technology. The CVICD scheme is especially suitable for the OTFT-based circuitry with low field-effect mobility, by means of lowering the voltage drop between the source and drain terminals of OTFT device to narrow down the charging time. The current nonuniformity for driving OLED can be effectively reduced. Also, the adoption of the external driving can decrease one transistor in a pixel region and reduce the circuit complexity.

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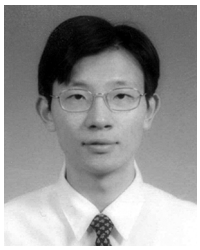

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