High-Voltage nLDMOS in Waffle-Layout Style With Body-Injected Technique for ESD Protection

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***Abstract*—Electrostatic-discharge robustness of n-channel lateral DMOS (nLDMOS) has been significantly increased in this letter through the waffle-layout style with body-current injection. This body-injected technique on high-voltage nLDMOS has been successfully verified in a 0.5-μm 16-V bipolar CMOS DMOS process without additional process or mask modification. The TLP-measured results confirmed that the secondary breakdown current (I_{t2}) of nLDMOS has a more than 2$\times$ increase by the body-current injection.**

***Index Terms*—Bipolar CMOS DMOS (BCD) process, body-current injection, electrostatic discharge (ESD), lateral DMOS (LDMOS).**

I. Introduction

RECENTLY, the high-voltage (HV) technology is prospering due to its extensive applications in the integrated-circuit (IC) industry [1]. To sustain high operating voltage in HV environments, device structures of lateral DMOS (LDMOS) are often more complex than those of advanced logic CMOS devices. As a result, not only the process complexity is increased but also the difficulty to guarantee the reliability of HV devices.

Electrostatic discharge (ESD) is an inevitable event of ICs during fabrication, packaging, conveyance, and assembly processes. In HV technologies, the n-channel LDMOS (nLDMOS) is known to have poor ESD robustness under ESD stresses [2], [3]. The method of inserting N+ buried layer has been reported to effectively enhance the ESD robustness of nLDMOS [2]. However, additional process steps and mask layer are needed. In this letter, a body-injected technique without process or mask modification is proposed to effectively improve the ESD robustness of nLDMOS.

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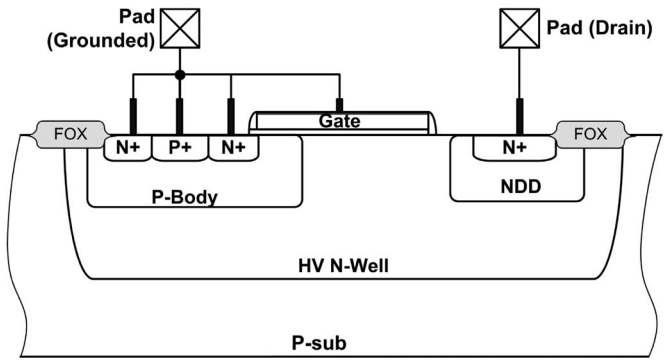

Fig. 1. Device cross-sectional view of the nLDMOS in a 0.5-μm 16-V BCD process.

II. Device Structure

Fig. 1 shows the device cross-sectional view of the nLDMOS in a 0.5-μm 16-V bipolar CMOS DMOS (BCD) process. To fulfill the concept of reduced surface field [4], the nLDMOS is surrounded by an HV N-well. As a result, the p-body is fully separated from the common p-type substrate (P-sub), and the channel length is decided by the overlapped distance of p-body with the polygate. Because the body of the nLDMOS is separated from the P-sub, additional P+ body pick up at every source region is required.

Fig. 2(a) shows the traditional layout of nLDMOS in stripe style. In low-voltage (LV) CMOS technologies, one of the most effective methods to increase ESD robustness of ESD protection devices is the substrate-triggered technique [5]. To inject the substrate-triggered current into the base of parasitic n-p-n bipolar junction transistor (BJT) inherent in LV NMOS, a P+ trigger node was placed at drain and connected to the trigger circuit [6]. However, in HV nLDMOS, the base of its parasitic n-p-n BJT is the p-body region, which is surrounded by the HV N-well. As a result, the traditional layout method in LV technologies to inject the substrate-triggered current by placing the P+ trigger node at drain side cannot be implemented in such an HV BCD process.

In order to effectively inject the trigger current into the p-body of nLDMOS (base of n-p-n BJT), nLDMOS realized in waffle-layout style is proposed in this letter. As shown in Fig. 2(b), the drain of nLDMOS in waffle style is drawn in a square. Source and body of the waffle nLDMOS is laid out at four sides of the drain square. Such a waffle-layout style leads to four squares (trigger nodes) at the diagonal corner of drain region. In the given 0.5-μm 16-V BCD process, the p-body is

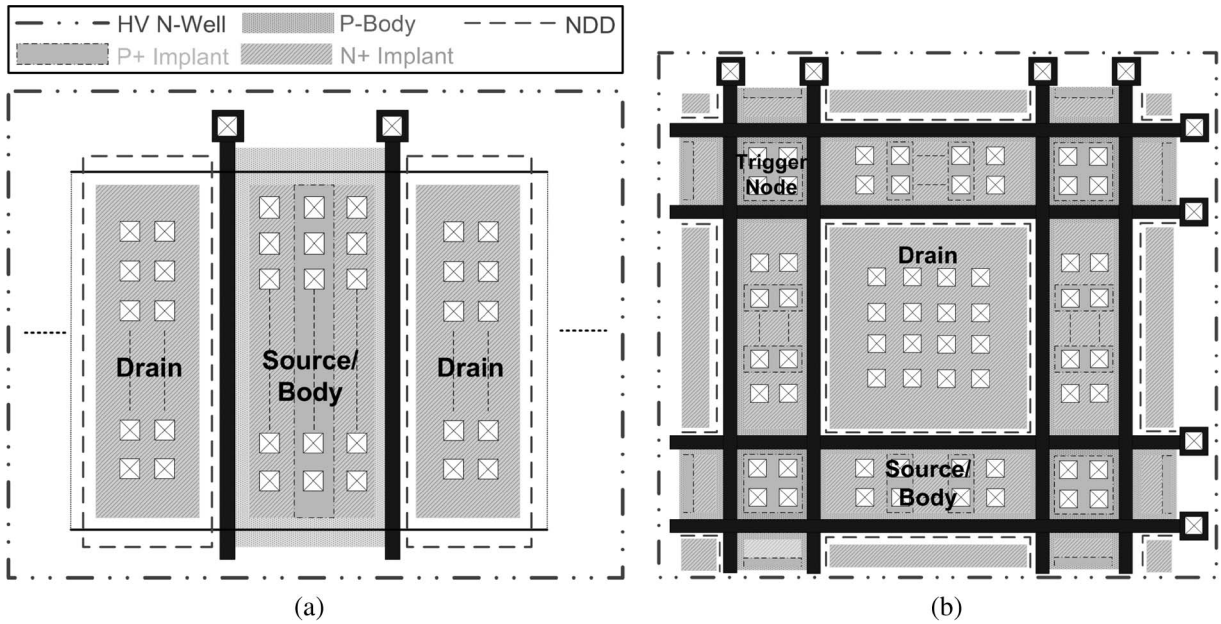

Fig. 2. Layout top view of the 16-V nLDMOS in (a) stripe and (b) waffle-layout style.

implanted before the formation of gate oxide; therefore, the four squares at the diagonal corner of drain are shorted to the body pick up at source/body region. The body current can therefore be injected from these trigger nodes, which will be collected by the grounded P+ pick up at the source/body. The injected body current at the trigger node acts as the base current to turn on the parasitic n-p-n BJT inherent in nLDMOS.

III. Experimental Results

To verify the turn-on ability of the parasitic n-p-n BJT in nLDMOS through the body-current injection, a stand-alone waffle-style nLDMOS with its trigger node connected to a bonding pad was fabricated on chip. Different levels of body current (I_B) were injected into a stand-alone waffle nLDMOS through the trigger node. Measurement setup is shown in the inset of Fig. 3, where the R_{Body} denotes the equivalent resistance of p-body from the trigger node to the P+ body pick up. With the larger injected I_B current, the nLDMOS exhibits higher collector current I_C. This result has verified that the parasitic n-p-n BJT inherent in waffle-style nLDMOS can be successfully triggered on through the body-current injection.

The 100-ns TLP-measured I–V curves and multiple-zapping reliability of three 16-V nLDMOS devices are shown in Fig. 4(a) and (b), respectively. The stripe nLDMOS in Fig. 4 has the traditional layout style as shown in Fig. 2(a). The waffle nLDMOS in Fig. 4 has layout style as shown in Fig. 2(b), where the trigger node of the waffle nLDMOS is grounded internally. The body-injected waffle nLDMOS in Fig. 4 has layout style as shown in Fig. 2(b), and the trigger node in the body-injected waffle nLDMOS is connected internally to the trigger circuit through metal directly wiring in the chip. Every test device is surrounded by a P-sub ring which is connected to the grounded-source node internally. The trigger circuit for the body-injected waffle nLDMOS is composed of an N-well

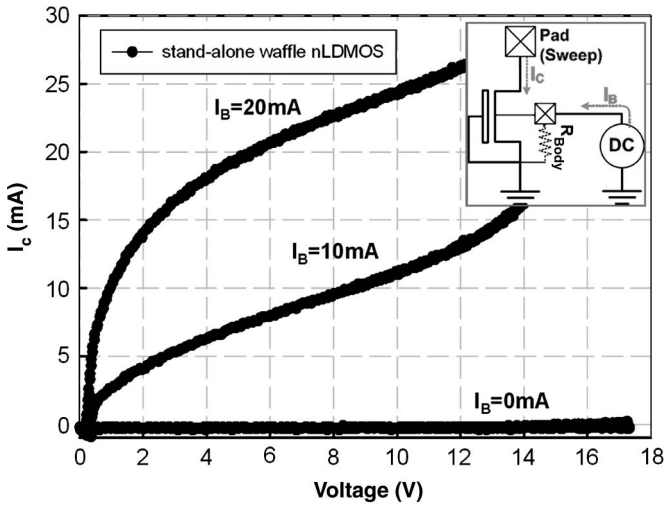

Fig. 3. Turn-on verification of the stand-alone nLDMOS drawn in waffle style with the additional body-current (I_B) injection.

resistor, a poly-insulator–poly capacitor, and an HV inverter [7]. The resistor and the capacitor are used to distinguish between ESD transition and normal-circuit power-on transition. The HV PMOS in the HV inverter provides trigger current to the trigger node of nLDMOS in waffle style under ESD stresses. In an experimental setup where the output of the stand-alone trigger circuit was connected to the trigger node of a stand-alone waffle nLDMOS through external metal wiring, the HV PMOS can provide a peak trigger current of 25 mA into the p-body of waffle nLDMOS when a 20-V voltage pulse with 10-ns rise time was given to the trigger circuit. The three nLDMOS shown in Fig. 4 have the same effective channel width (363.6 μm) and the same channel length (0.35 μm) in layout. For waffle nLDMOS, channel width for one side of a drain square is 10.1 μm, and there are 3 $\times$ 3 drain squares

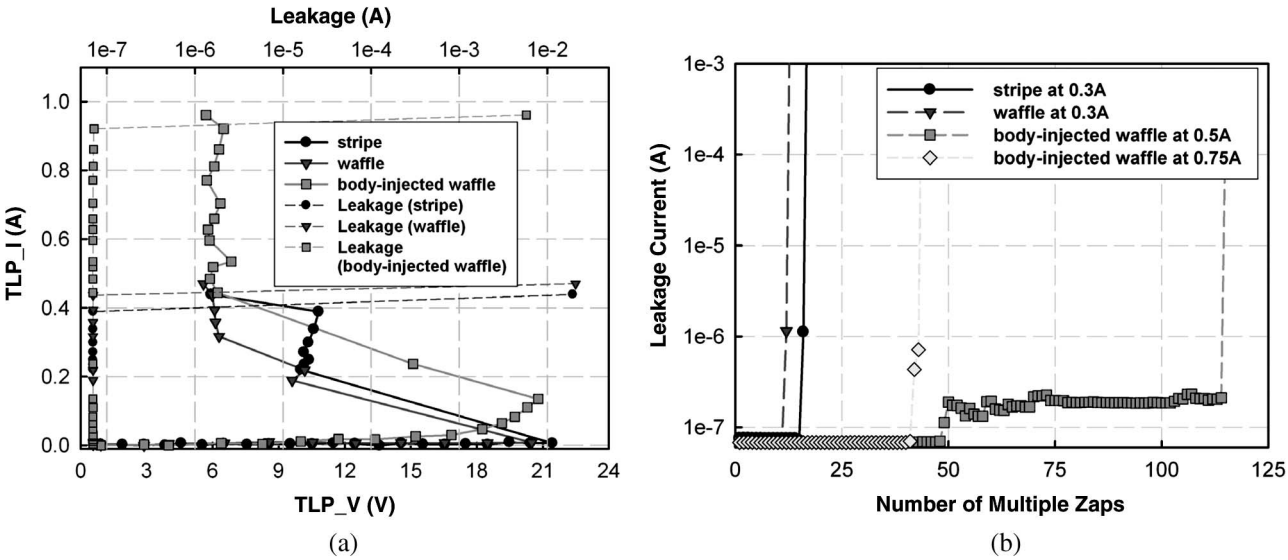

Fig. 4. 100-ns TLP-measured (a) I–V curves and (b) multiple-zapping reliability of stripe, waffle, and body-injected waffle nLDMOS.

in the waffle nLDMOS. The total effective channel width of the waffle nLDMOS is therefore $(4 \times 10.1 \times 9) = 363.6$ μm. For stripe nLDMOS, channel width of each finger is 45.45 μm, and there are eight fingers to form the same effective channel width of 363.6 μm. Failure criteria (1-μA leakage current under 16-V drain-bias voltage) of all devices are kept the same to judge their ESD robustness. As shown in Fig. 4(a), the stripe nLDMOS and waffle nLDMOS have roughly the same secondary breakdown current (I_{t2}) of 0.39 and 0.41 A, respectively, if the body-current injection was not applied. In Fig. 4(a), the waffle nLDMOS is found to have lower second snapback current than that of the stripe nLDMOS (200 mA versus 400 mA). This phenomenon can possibly come from the higher electric-field distribution near the sharp drain corners and the overlapped space-charge distribution near the corners of drain squares. By applying the body-current injection, I_{t2} of the waffle nLDMOS can be significantly increased from 0.41 to 0.95 A. Moreover, the multiple-zapping issue of nLDMOS [3] has also been found to be substantially alleviated by the body-current injection, as shown in Fig. 4(b). Under the fixed TLP current stress of 0.3 A, the stripe and waffle nLDMOS without body injection failed after 17 and 13 zaps, respectively. For the body-injected waffle nLDMOS under the fixed TLP current stress of 0.5 A, the number of zaps to the failure criteria of 1 μA is substantially increased to 116 zaps. Even at the higher fixed TLP current stress of 0.75 A, the body-injected waffle nLDMOS still shows higher reliability to sustain the number of zaps up to 44 before failure. From the 100-ns TLP measurement, a more than $2\times$ increase on I_{t2} and reliability improvement on multiple-zapping issue have been achieved through the waffle-layout style with the body-current injection.

IV. Conclusion

The nLDMOS in HV technologies is known to have poor ESD robustness under ESD stresses. With the proposed waffle-layout style in this letter, the body-injected technique in HV nLDMOS has been successfully verified in a 0.5-μm 16-V BCD process. The 100-ns TLP measurement has successfully verified that, with the body-current injection, I_{t2} of the waffle nLDMOS can be increased from 0.41 to 0.95 A. Experimental results have demonstrated that the body-injected technique is an effective method for increasing the ESD robustness of nLDMOS in HV ICs without modifying process steps nor increasing mask layer.

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