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Investigation of electrostatic integrity for ultra-thin-body GeOI MOSFET using analytical solution of Poisson's equation

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Abstract

The electrostatic integrity for UTB GeOI MOSFETs is examined comprehensively by using an analytical solution of Poisson's equation verified with TCAD simulation. Our results indicate that UTB GeOI MOSFETs with the ratio of channel length (L_g) to channel thickness (T_{ch}) around 5 can show comparable subthreshold swing to that of the SOI counterparts. The impact of the buried oxide thickness (T_{BOX}) and back-gate bias ($V_{back\text{-}gate}$) on the electrostatic integrity of GeOI devices is also examined.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Germanium as a pFET channel material has been recently proposed [1–6] to enable mobility scaling. However, its higher permittivity makes it very susceptible to short channel effects (SCEs). The ultra-thin body (UTB) MOSFETs with thin buried oxide (BOX) have emerged as an important candidate for CMOS scaling [7–9]. Germanium-on-insulator (GeOI) devices are expected to offer better electrostatic control over bulk Ge devices [10].

Several studies [10–12] have compared the electrostatic integrity of Ge and Si devices in the past. An *et al* [11] showed that the off-state leakage current of UTB GeOI devices is comparable to or even a little lower than that of SOI devices. Pethe *et al* [12] showed that the Ge double gate suffers worse SCEs and therefore has higher subthreshold swing than the Si device. Batail *et al* [10] showed that UTB GeOI devices present equivalent threshold voltage control as SOI devices. These studies, either employing numerical simulation or using a semi-empirical model with fitting parameters, have not shown consistent results. Moreover, analytical analysis of the UTB GeOI MOSFET has rarely been seen. In this work, we assess the electrostatic integrity for nanoscale UTB GeOI MOSFETs by using analytical solution of Poisson's equations and provide more scalable and predictive results for UTB GeOI MOSFET analysis. Following the 2007 edition of the International Technology Roadmap for Semiconductors [13], UTB MOSFETs for various generations are investigated. Through our theoretical model, a comprehensive analysis including the impact of T_{BOX}, T_{ch} and $V_{back\text{-}gate}$ on the electrostatic integrity of the UTB GeOI MOSFET is presented.

2. Analytical model and methodology

Our theoretical subthreshold swing for UTB GeOI is derived from analytical potential solution in the subthreshold region. Figure 1 shows a schematic sketch of a UTB MOSFET with thin BOX structure. In the subthreshold regime, the channel is fully depleted with negligible mobile carriers. Therefore, the channel potential distribution, $\phi_{ch}(x, y)$, satisfies Poisson's equation:

$$\frac{\partial^2 \phi_{ch}(x, y)}{\partial x^2} + \frac{\partial^2 \phi_{ch}(x, y)}{\partial y^2} = -\frac{qN_{ch}}{\varepsilon_{ch}}. \quad (1)$$

Since there is no charge in the BOX region, the BOX potential distribution, $\phi_{box}(x, y)$, satisfies the Laplace equation:

$$\frac{\partial^2 \phi_{box}(x, y)}{\partial x^2} + \frac{\partial^2 \phi_{box}(x, y)}{\partial y^2} = 0. \quad (2)$$

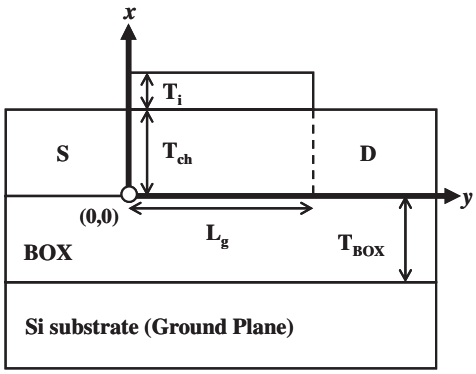

Figure 1. Schematic sketch of a UTB MOSFET with thin BOX structure investigated in this study.

Above, N_{ch} is the channel doping concentration and ε_{ch} is the permittivity of the channel. The required boundary conditions can be described as

$$\phi_{ch}(T_{ch}, y) + T_i \frac{\varepsilon_{ch}}{\varepsilon_i} \cdot \left.\frac{\partial \phi_{ch}(x, y)}{\partial x}\right|_{x=T_{ch}} = V_g - V_{fb}, \tag{3a}$$

$$\phi_{ch}(x, 0) = -\phi_{ms} + V_s, \tag{3b}$$

$$\phi_{ch}(x, L_g) = -\phi_{ms} + V_d, \tag{3c}$$

$$\phi_{box}(-T_{BOX}, y) = V_{back\text{-}gate} - V_{fb,back\text{-}gate} + (E_{i,ch} - E_{i,sub}), \tag{3d}$$

$$\phi_{box}(x, 0) = [V_{back\text{-}gate} - V_{fb,back\text{-}gate} + (E_{i,ch} - E_{i,sub})] + \frac{(-\phi_{ms} + V_s) - [V_{back\text{-}gate} - V_{fb,back\text{-}gate} + (E_{i,ch} - E_{i,sub})]}{T_{BOX}} x, \tag{3e}$$

$$\phi_{box}(x, L_g) = [V_{back\text{-}gate} - V_{fb,back\text{-}gate} + (E_{i,ch} - E_{i,sub})] + \frac{(-\phi_{ms} + V_d) - [V_{back\text{-}gate} - V_{fb,back\text{-}gate} + (E_{i,ch} - E_{i,sub})]}{T_{BOX}} x, \tag{3f}$$

$$\varepsilon_{ch} \cdot \left.\frac{\partial \phi_{ch}(x, y)}{\partial x}\right|_{x=0} = \varepsilon_{ox} \cdot \left.\frac{\partial \phi_{box}(x, y)}{\partial x}\right|_{x=0}, \tag{3g}$$

$$\left.\frac{\partial \phi_{ch}(x, y)}{\partial y}\right|_{x=0} = \left.\frac{\partial \phi_{box}(x, y)}{\partial y}\right|_{x=0}, \tag{3h}$$

where T_{ch}, T_i and T_{BOX} are the thicknesses of the channel, gate insulator and buried oxide, respectively; L_g is the gate length; ε_i and ε_{ox} are the permittivities of the gate insulator and BOX, respectively; V_g, $V_{back\text{-}gate}$, V_d and V_s are the voltage biases of the gate, back-gate, drain and source, respectively; V_{fb} and $V_{fb,back\text{-}gate}$ are the flat-band voltages of the gate and back-gate, respectively; ϕ_{ms} is the built-in potential of the source/drain to the channel; $E_{i,ch}$ and $E_{i,sub}$ are the intrinsic Fermi levels of the channel and substrate (back-gate), respectively.

The corresponding 2D boundary value problem can be divided into two sub-problems, a 1D Poisson's equation and a 2D Laplace equation. Using the superposition principle, the complete channel potential solution is $\phi_{ch}(x, y) = \phi_{ch,1}(x) + \phi_{ch,2}(x, y)$, where $\phi_{ch,1}(x)$ and $\phi_{ch,2}(x, y)$ are solutions of 1D and 2D sub-problems in the channel, respectively. The 1D solution $\phi_{ch,1}(x)$ can be expressed as

$$\phi_{ch,1}(x) = -\frac{qN_{ch}}{2\varepsilon_{ch}} x^2 + A \cdot x + B, \tag{4a}$$

$$A = \left\{ (V_g - V_{fb}) - [V_{back\text{-}gate} - V_{fb,back\text{-}gate} + (E_{i,ch} - E_{i,sub})] + \frac{qN_{ch}}{2\varepsilon_{ch}} \left(T_{ch}^2 + 2\frac{\varepsilon_{ch}}{\varepsilon_i} T_i T_{ch} \right) \right\} \Big/ \left\{ T_{ch} + \frac{\varepsilon_{ch}}{\varepsilon_i} T_i + \frac{\varepsilon_{ch}}{\varepsilon_{ox}} T_{BOX} \right\}, \tag{4b}$$

$$B = \frac{\varepsilon_{ch}}{\varepsilon_{ox}} T_{BOX} \cdot A + [V_{back\text{-}gate} - V_{fb,back\text{-}gate} + (E_{i,ch} - E_{i,sub})]. \tag{4c}$$

In solving the 2D sub-problem, the boundary condition of the gate dielectric/channel interface (3*a*) is simplified by converting the gate dielectric thickness to $(\varepsilon_{ch}/\varepsilon_i)$ times and replacing the gate dielectric region with an equivalent channel-material region. The electric field discontinuity across the gate dielectric and channel interface can thus be eliminated. For the channel/BOX interface, both potential distribution in the channel ($\phi_{ch,2}(x, y)$) and that in the BOX ($\phi_{box,2}(x, y)$) have to be considered to satisfy the boundary conditions (3*g*) and (3*h*).

The 2D solution $\phi_{ch,2}(x, y)$ can be obtained using the method of separation of variables:

$$\phi_{ch,2}(x, y) = \sum_n \{[c_n \cdot \sinh(\gamma_n y) + c'_n \cdot \sinh(\gamma_n (L_g - y))] \cdot \sin(\gamma_n x) + e_n \cdot \sinh(\lambda_n (T_{ch} + (\varepsilon_{ch}/\varepsilon_i) T_i - x)) \cdot \sin(\lambda_n y)\}, \tag{5a}$$

where

$$\lambda_n = (n\pi)/L_g, \tag{5b}$$

$$\gamma_n = (n\pi)/(T_{ch} + (\varepsilon_{ch}/\varepsilon_i) T_i). \tag{5c}$$

The coefficients c_n, c'_n and e_n in (5*a*) can be expressed as

$$c_n = \frac{1}{\sinh(\lambda_n L_g)} \left[2(-\phi_{ms} + V_d - B) \cdot \frac{1 - (-1)^n}{n\pi} + 2A \cdot \left(T_{ch} + \frac{\varepsilon_{ch}}{\varepsilon_i} T_i \right) \frac{(-1)^n}{n\pi} + 2 \left(T_{ch} + \frac{\varepsilon_{ch}}{\varepsilon_i} T_i \right)^2 \cdot \frac{(-1)^n - 1}{(n\pi)^3} \right], \tag{5d}$$

$$c'_n = \frac{1}{\sinh(\lambda_n L_g)} \left[2(-\phi_{ms} - B) \frac{1 - (-1)^n}{n\pi} + 2A \cdot \left(T_{ch} + \frac{\varepsilon_{ch}}{\varepsilon_i} T_i \right) \frac{(-1)^n}{n\pi} + 2 \left(T_{ch} + \frac{\varepsilon_{ch}}{\varepsilon_i} T_i \right)^2 \cdot \frac{(-1)^n - 1}{(n\pi)^3} \right], \tag{5e}$$

$$e_n = \frac{(\mathrm{RHS}_n/\mathrm{LHS}_n)}{\sinh\left(\frac{n\pi}{L_g}(T_{ch} + (\varepsilon_{ch}/\varepsilon_i) T_i)\right)}, \tag{5f}$$

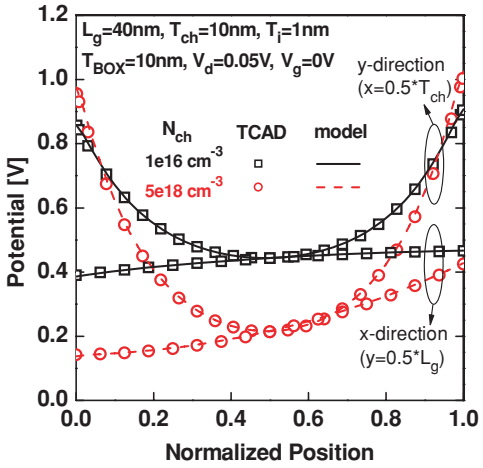

Figure 2. Analytical potential distribution compared with the result of TCAD simulation. A midgap work function (4.5 eV) is used.

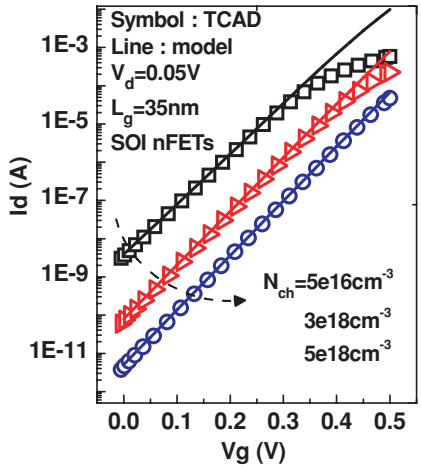

Figure 3. UTB SOI subthreshold current with heavily doped and lightly doped channels. Constant mobility model is used in both the analytical model and the TCAD simulation.

where

$$\mathrm{LHS}_n = \lambda_n \cdot \coth(\lambda_n T_{\mathrm{BOX}}) + \frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_{\mathrm{ox}}}\lambda_n \cdot \coth(\lambda_n((\varepsilon_{\mathrm{ch}}/\varepsilon_i)T_i + T_{\mathrm{ch}})), \tag{5g}$$

$$\mathrm{RHS}_n = 2\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_{\mathrm{ox}}}A \cdot \frac{1-(-1)^n}{n\pi} + \sum_m \left\{ \left[c_n \cdot \frac{\frac{(2\varepsilon_{\mathrm{ch}}/\varepsilon_{\mathrm{ox}})(-1)^{n+1}}{n\pi}\sinh(\lambda_m L_g)}{1+(\gamma_m/\lambda_n)^2} + c_n' \cdot \frac{\frac{(2\varepsilon_{\mathrm{ch}}/\varepsilon_{\mathrm{ox}})}{n\pi}\sinh(\lambda_m L_g)}{1+(\gamma_m/\lambda_n)^2} \right] \cdot \lambda_m - d_n \frac{m\pi}{T_{\mathrm{BOX}}}\frac{(-1)^{m+n+1}}{n\pi}\frac{2\sinh\left(\frac{m\pi}{T_{\mathrm{BOX}}}L_g\right)}{1+(\gamma_m/\lambda_n)^2} - d_n' \frac{m\pi}{T_{\mathrm{BOX}}}\frac{(-1)^m}{n\pi}\frac{2\sinh\left(\frac{m\pi}{T_{\mathrm{BOX}}}L_g\right)}{1+(\gamma_m/\lambda_n)^2} \right\}, \tag{5h}$$

$$d_n = \frac{2}{\sinh(\gamma_n L_g)}\left\{ [V_{\text{back-gate}} - V_{\text{fb,back-gate}} + (E_{i,\mathrm{ch}} - E_{i,\mathrm{sub}})] \cdot \frac{1-(-1)^n}{n\pi} + [(-\phi_{\mathrm{ms}} + V_d - B)] \cdot \frac{(-1)^{n+1}}{n\pi} \right\}, \tag{5i}$$

$$d_n' = \frac{2}{\sinh(\gamma_n L_g)}\left\{ [V_{\text{back-gate}} - V_{\text{fb,back-gate}} + (E_{i,\mathrm{ch}} - E_{i,\mathrm{sub}})] \cdot \frac{1-(-1)^n}{n\pi} + [(-\phi_{\mathrm{ms}} - B)] \cdot \frac{(-1)^{n+1}}{n\pi} \right\}. \tag{5j}$$

Our analytical potential solution has been verified with TCAD simulation [14]. Figure 2 shows that our model is fairly accurate for various channel doping (N_{ch}). Based on the potential solution, the subthreshold current can be derived by

$$I_d = \frac{q\mu_n W(kT/q)\left(n_i^2/N_{\mathrm{ch}}\right)[1-\exp(-V_d/(kT/q))]}{\int_0^{L_g}\mathrm{d}y \Big/ \int_0^{T_{\mathrm{ch}}}\exp[q\phi_{\mathrm{ch}}(x,y)/(kT)]\,\mathrm{d}x}. \tag{6}$$

Figures 3–6 demonstrate that our UTB subthreshold current model is quite scalable with important device design

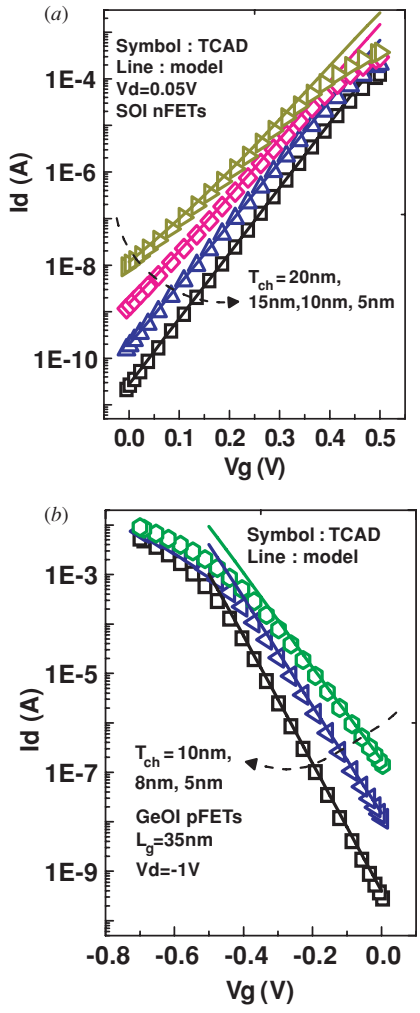

Figure 4. UTB subthreshold current with various T_{ch} for (*a*) nFET SOI devices and (*b*) pFET GeOI devices. Constant mobility model is used in both the analytical model and the TCAD simulation.

parameters such as N_{ch}, T_{ch}, L_g and $V_{\text{back-gate}}$. The UTB subthreshold current model shows good agreement with TCAD simulation for both N/P FET UTB SOI and GeOI

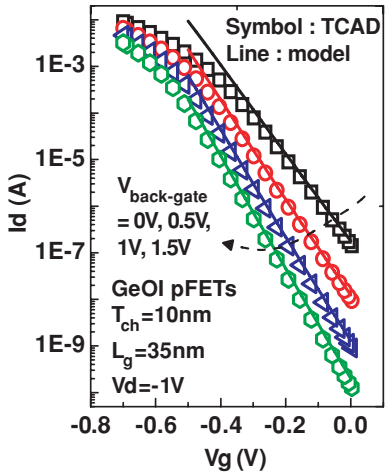

Figure 5. UTB subthreshold current with various back-gate biases for GeOI devices. Constant mobility model is used in both the analytical model and the TCAD simulation.

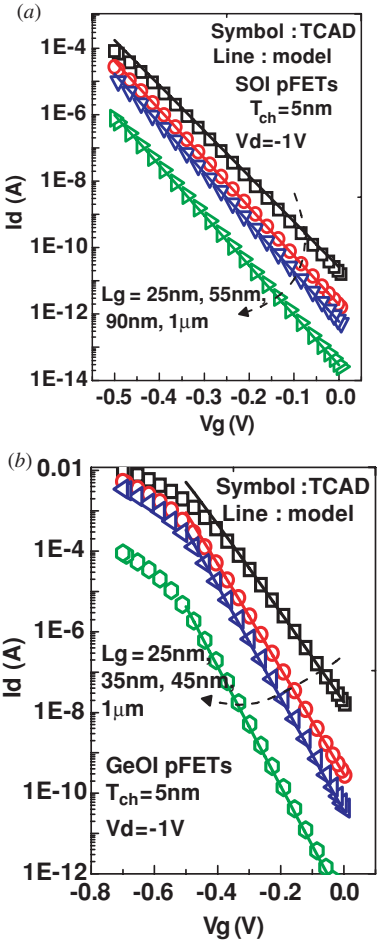

Figure 6. UTB subthreshold current with a wide range of gate lengths for (*a*) pFET SOI devices and (*b*) pFET GeOI devices. Constant mobility model is used in both the analytical model and the TCAD simulation.

devices. With the subthreshold current model, subthreshold swing can be obtained. Several papers recently published indicated that an accurate investigation of electrostatic integrity for bulk [15] and FDSOI [16] MOSFETs must

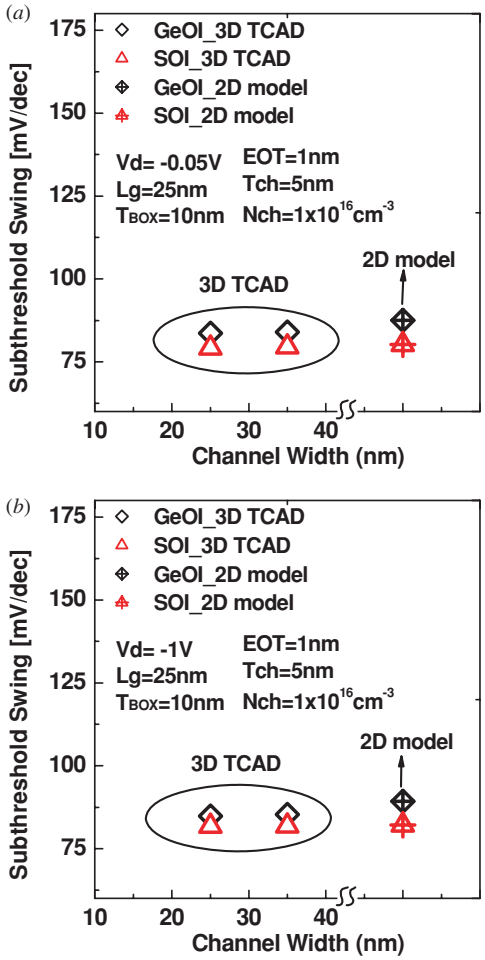

Figure 7. The impact of INWE on the subthreshold swing for the UTB thin BOX GeOI MOSFET with (*a*) $V_d = -0.05$ V and (*b*) $V_d = -1$ V.

be carried out by 3D Poisson analysis to consider the inverse narrow width effect (INWE). However, as shown in figure 7, for UTB thin BOX MOSFETs with a lightly doped channel, the impact of INWE on the subthreshold swing is insignificant. Therefore, our analytical subthreshold current model is sufficient for examining the electrostatic integrity of the UTB MOSFETs.

Compared with the TCAD device simulation, our methodology shows higher efficiency in determining the subthreshold current of a UTB MOSFET. For TCAD simulation, the CPU time needed for a single subthreshold current is about several minutes, while in our calculation several seconds only is needed.

In this work, important device parameters used for investigating the electrostatic integrity of the lightly doped ($N_{ch} = 1 \times 10^{16}$ cm^{-3}) pFET UTB MOSFET such as L_g and EOT for each generation are determined based on the ITRS roadmap [13].

3. Electrostatic integrity for UTB GeOI MOSFET

Figure 8 shows that due to higher permittivity, the hole conduction path of GeOI devices is closer to the back-gate

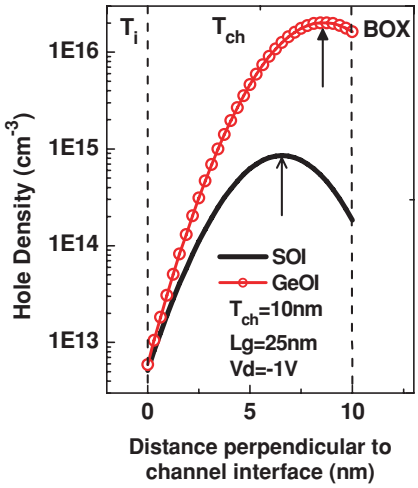

Figure 8. Hole density distribution for SOI and GeOI in the subthreshold region. The arrow tip indicates the hole conduction path.

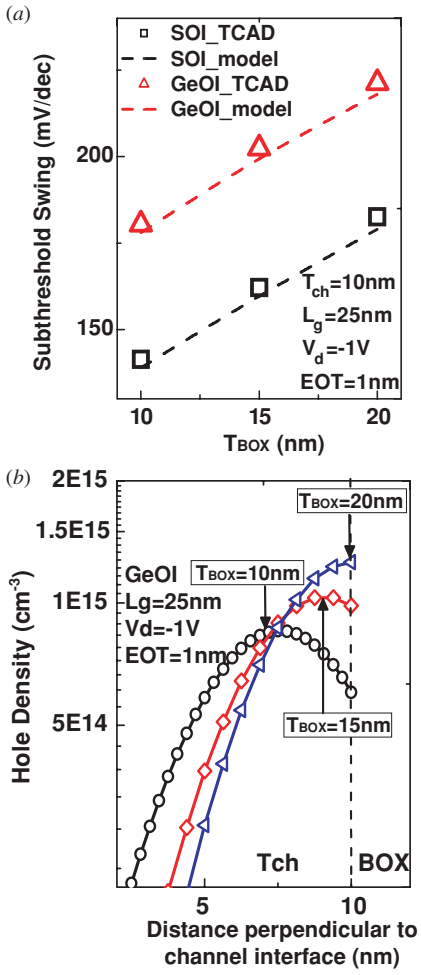

Figure 9. Impact of the buried oxide thickness (T_{BOX}) on (*a*) the subthreshold swing and (*b*) the hole density distribution in the subthreshold region.

interface (T_{ch}/BOX interface) than SOI devices. Thus, the GeOI device has worse electrostatic integrity than the SOI device generally. Figure 9 illustrates the impact of T_{BOX} on the subthreshold swing (figure 9(*a*)) and hole density distribution in the subthreshold region (figure 9(*b*)). At $V_d = -1$ V, the SCEs of UTB devices result from the electric field coupling between the source and drain through BOX. As T_{BOX} is scaled, the SCEs of UTB SOI and GeOI devices can be improved, and the UTB devices show lower subthreshold swing (figure 9(*a*)). Figure 9(*b*) shows that as T_{BOX} is scaled, the hole conduction path becomes closer to the front-gate surface (T_i/T_{ch} interface). Therefore, thin BOX with stronger front-gate controllability is needed for GeOI devices.

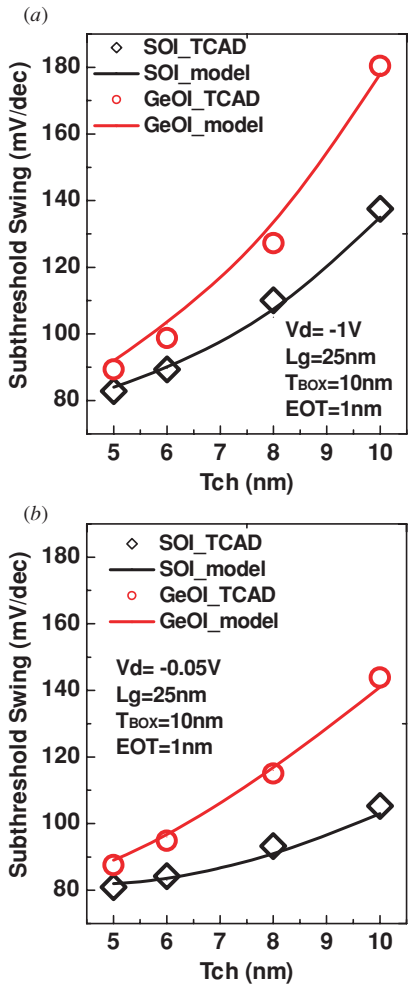

Figure 10. Impact of the channel thickness (T_{ch}) on the subthreshold swing for (*a*) $V_d = -1$ V and (*b*) $V_d = -0.05$ V with $L_g = 25$ nm.

Figure 10 shows the impact of T_{ch} on the subthreshold swing of SOI and GeOI devices for $V_d = -1$ V and $V_d = -0.05$ V with $L_g = 25$ nm. As T_{ch} is scaled, the subthreshold swing of the UTB device is reduced. When $T_{ch} = 10$ nm, the GeOI device with worse electrostatic integrity shows larger subthreshold swing than that of the SOI device. When T_{ch} is scaled to 5 nm, the subthreshold swing of the GeOI device becomes comparable to that of the SOI device because the GeOI device with thin T_{ch} shows well-controlled electrostatic integrity. Moreover, the UTB devices with $V_d = -1$ V and $V_d = -0.05$ V show comparable subthreshold swing as $T_{ch} = 5$ nm. In other words, the impact of drain-induced barrier lowering (DIBL) on subthreshold swing can be suppressed

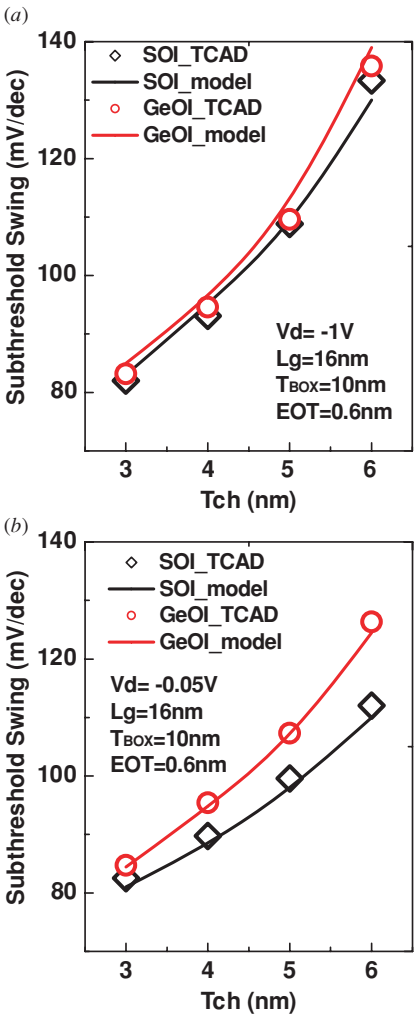

Figure 11. Impact of the channel thickness (T_{ch}) on the subthreshold swing for (*a*) $V_d = -1$ V and (*b*) $V_d = -0.05$ V with $L_g = 16$ nm.

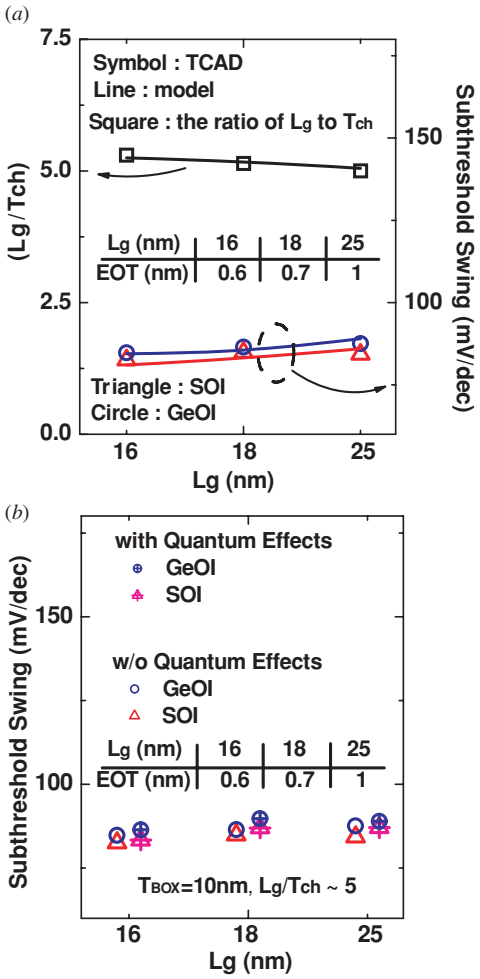

Figure 12. (*a*) GeOI devices with $L_g/T_{ch} \sim 5$ show comparable subthreshold swing to that of SOI devices at $V_d = -0.05$ V. (*b*) The subthreshold swing comparison between the GeOI and SOI MOSFETs as quantum effects are considered by using the density gradient model in TCAD simulation [14].

when T_{ch} is scaled. Figure 11 shows the impact of T_{ch} on the subthreshold swing of UTB devices with $L_g = 16$ nm. When T_{ch} is reduced to 3 nm, the GeOI device shows comparable subthreshold swing to that of SOI devices.

More generations of UTB devices are investigated for the device design of GeOI devices (figure 12(*a*)). As for the ITRS roadmap [13], the device design for SOI devices with a Si channel, the ratio of L_g to T_{ch} is around 3. Figure 12(*a*) shows that the GeOI devices with the ratio of L_g to T_{ch} around 5 can show well-controlled electrostatic integrity and comparable subthreshold swing to that of the SOI devices. Figure 12(*b*) shows that even considering quantum effects, the UTB GeOI and SOI MOSFETs still show comparable subthreshold swing as L_g/T_{ch} around 5. The comparison between UTB GeOI and SOI MOSFETs in figure 12 is based on the same off-current (2×10^{-8} A μm^{-1}) by adjusting the gate work function for both GeOI and SOI MOSFETs, respectively.

Besides T_{BOX} and T_{ch} scaling, $V_{back\text{-}gate}$ is also beneficial for suppressing the SCEs of GeOI devices. Figure 13 shows the impact of $V_{back\text{-}gate}$ on the subthreshold swing for $L_g = 25$ nm. As $V_{back\text{-}gate}$ is increased, the subthreshold swing

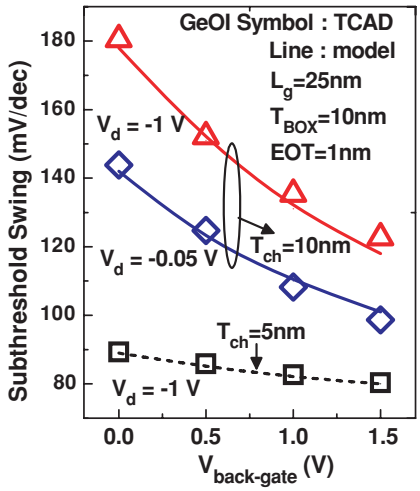

Figure 13. Impact of the back-gate bias ($V_{back\text{-}gate}$) on the subthreshold swing with $L_g = 25$ nm.

of UTB devices is reduced. In figure 13, the subthreshold swing of the GeOI device with larger T_{ch} (= 10 nm) shows

higher sensitivity to $V_{\text{back-gate}}$ as compared to that of the GeOI device with smaller T_{ch} (= 5 nm). The GeOI device shows better front-gate controllability and electrostatic integrity with increasing $V_{\text{back-gate}}$ because the hole conduction path for the GeOI device becomes closer to the front-gate surface.

Besides UTB MOSFETs, silicon-on-nothing (SON) MOSFETs have also been proposed as a possible alternative scalable solution to satisfy the ITRS roadmap requirements [17, 18]. Therefore, the comparison of the electrostatic integrity among GeOI, SOI and SON is an important issue and merits investigation in the future.

4. Conclusion

We have investigated the electrostatic integrity for UTB GeOI devices using analytical solution of Poisson's equation verified with TCAD simulation. Especially, the impacts of T_{BOX}, T_{ch} and $V_{\text{back-gate}}$ on the electrostatic integrity for the UTB GeOI MOSFET have been carefully examined. Our results indicate that the UTB GeOI MOSFETs with the device design of $L_g/T_{\text{ch}} \sim 5$ show acceptable and comparable subthreshold swing to that of SOI devices. The electrostatic integrity for the UTB GeOI MOSFET is very sensitive to the T_{ch} scaling. T_{BOX} reduction and positive $V_{\text{back-gate}}$ are also beneficial for suppressing the SCEs of pFET UTB GeOI MOSFETs. This study may provide insights for the UTB GeOI device design.

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