國 立 交 通 大 學

平面顯示技術碩士學位學程

碩士論文

大尺寸之脈衝重疊偵測

主動觸控面板的實作研究

Study & Implementation on Large Size Active Touch Panel

Using Pulse Overlapping Detection

研 究 生：簡君達

指導教授：戴亞翔 教授

中華民國一百零三年六月

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碩 士 論 文

A Thesis

Submitted to Degree Program of Flat Panel Display Technology

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of Master of Science

in

Flat Panel Display Technology

June 2014

Hsinchu, Taiwan, Republic of China

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摘　要

在本篇論文當中，我們運用之前所提出的新型主動式觸控電路，其架構為兩個 TFT（一個為開關用，一個為電阻用)以及一個電容，並藉由兩個閘極脈波輸入此觸控電路。當手指觸碰面板之感應區塊時，造成觸控電路之 RC 延遲時間增加，使開關 TFT 得以短暫地開啟。此開關 TFT 於開啟期間會有電流訊號通過，藉著外部之偵測電路，來加以判別手指是否已觸碰到面板之感應區塊。

此外，以該主動式觸控電路為基礎，分別加以探討實際應用之時，小尺寸面板以及大尺寸面板之負載效應，對於近端感應區塊以及遠端感應區塊之偵測影響程度為何。依據該主動式觸控電路之設計理念，面板當中感應區塊之 RC 延遲時間必須小於面板之掃描線 RC 延遲時間，也必須小於手指觸碰面板之感應區塊的 RC 延遲時間，面板未觸碰、面板延遲、及面板觸碰三者之時間關係為遞增。因此，當面板尺寸越大時，掃描線之負載也隨著增加，進而導致近端輸入之閘極脈波，到達遠端感應區塊時，已是失真之波形。在手指未觸碰面板之情況下，此失真波形也使得遠端感應區塊之 RC 延遲時間隨之增加，亦造成開關 TFT 進行了不必要之開啟動作，而讓外部之偵測電路誤判。

最後，進一步探討，若是將所有閘極脈波之高頻成份予以濾除，而得到失真波形。利用此失真波形輸入至觸控面板之中，理論上遠端之感應區塊的 RC 延遲時間，即不會受到掃描線之負載影響，不僅可避免遠端誤動作之情事，甚至可更精簡面板設計之準則。

Study & Implementation on Large Size Active Touch Panel Using Pulse Overlapping Detection

Student : Chun-Ta Chien Advisor : Prof. Ya-Hsiang Tai

National Chiao Tung University
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Abstract

In this thesis, we use the previous theory that the new active touch circuit is proposed. Its structure is composed of two TFTs (one is switch, another is resistor), one capacitor and then the two scan pulses transmit to this touch circuit. When the touch pad is touched by finger, there will be a rise in the RC delay time of touch circuit. The TFT will be opened in a transient time and pass through current. We can check whether the touch pad is touched by detection circuit during the period.

Besides, we have based on the new active touch circuit and discussed the influence between the loading effects of touch panel and the touch pad at near-end and far-end. According to the concept of design, we defined that the RC delay time is $t1_{untouched}$ when the touch pad is untouched, the RC delay time is $t3_{touched}$ when the touch pad is touched, and the RC delay time is $t2_{loading}$ for scan loading. Their relationships are shown as $t1_{untouched} < t2_{loading} < t3_{touched}$. Therefore, when the touch panel size is increased, the scan loading is also increased. The scan loading will cause the scan pulse is a distorted waveform at far-end. When the touch pad is untouched, the RC delay time of far-end ($t1_{untouched}$) is increased by the distorted scan pulse. It isn't necessary to open the TFT and will cause the mal-operation for the external detection circuit.

Finally, to be more precisely, if we filter out the high frequency harmonics of all scan pulse and then feed the distorted scan pulses in touch panel. Theoretically, the scan loadings can't influence the RC delay time of touch pad at far-end. It did not only avoid the mal-operation at far-end but also make the design rule of touch panel very simple.

誌　謝

謹以此論文獻給我敬愛的父母，簡榮森先生與林素鳳女士，感謝他們辛苦地培育我，且無後顧之憂地讀上大學、當兵、工作，也鼓勵我更上一層樓。於元太工作了五年後，決定與大學好友謝正揮先生一同努力讀書，也終於讓我們都考上在職專班。修完學分後，一度因為工作關係想要放棄，但在太太藍雅萍與岳父藍柳協先生和岳母朱鶯隨女士之鼓勵與支持下，使得我終於完成碩士論文。在此由衷地謝謝他們。

感謝我的論文指導教授 戴亞翔博士不遺餘力地教導以及指導生活上的待人處事，使我獲益良多，帶我一步步地完成學業，獲得碩士學位。亦感謝我的論文口試委員，有了他們的熱心建議與指導，使我的論文更趨完整。

感謝實驗室的學長和同學及學弟們，有了你們的支持與協助，讓我的論文可順利完成。在此也特別感謝畢業學長周祿盛先生、邱皓麟先生、林寬達先生，於論文遇到困難之時，不吝給予指導與糾正。

最後感謝支持與幫助我的親朋好友們，謝謝你們一路上給我的關心，使我今天得以完成碩士論文，謝謝大家。

簡君達 謹誌

2014 年 6 月

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Chapter 2

Chapter 1 Introduction

1.1 Background

Touch Panel (TP) has attracted much attention in various applications because it makes user interface more convenient and various. It can provide extra functionalities such as drawing, writing, and multi-touch. For this reason, TP has been widely used as an input device for mobile system such as PDA, digital camera, smart phone, and tablet-PC.

TP can be divided into two main categories. One is passive matrix TP, and the other is active matrix TP. For passive matrix TP, the earliest type is resistive type, which uses two ITO films biased and dot spacers holding the structure between them. Fig. 1-1 [1] shows the structure of resistive touch panel. When touching, the pressure of the external force makes the upper ITO layer contact with the lower ITO and the voltage drop at that touching point becomes zero. Consequently, the touching input function can be realized by recognize the site of the short circuit. Although the resistive touch panel operation is simple, the physical abrasion can lower its reliability.

Recently, Projective Capacitive Touch Panel (PCT) is adapted. Almost all of the smart phone and tablet-PC use PCT because of its high sensitivity. The sketch map of its operation principle is shown in Fig. 1-2 and Fig. 1-3 [2]. Not like the resistive type, it does not need any external force. The PCT function is carried out by using IC to detect the change of capacitive value when human's hands touch on the panel. There are two disadvantages in PCT. First, because the change of capacitive value is small, the IC must be very sensitive, that makes the PCT expensive. Another weak point in PCT is that, when panel size becomes large, touch signal is hardly to be read by IC. Active matrix is an effective solution to achieve a large size TP.

There are two major technologies to achieve active matrix TP; one of them is optical sensor, which is shown in Fig. 1-4 and Fig. 1-5 [3]. The optical sensor is widely studied since hydrogenated amorphous silicon has a sufficiently large photosensitivity for use as an optical sensor. It detects light reflected from screens or shadows made by external illumination when the screen is touched. However these properties make it difficult to use such device as a touch sensor since the sensor is apt to respond to unintended light noise.

Another way to achieve active TP is Liquid-Crystal Capacitance Detector. It uses a capacitive touch sensor which is composed of a liquid crystal capacitor and sensing transistors. Fig. 1-6 and Fig. 1-7 show the cross-sectional view of a capacitive sensor and the sensing circuit [4]. The sensing capacitor C_{ss} is formed by the electrodes on a TFT and a color filter substrate. When one pushes the upper CF substrate, there is a slight reduction in cell gap and the capacitance of C_{ss} increases, therefore voltage of point A decreases. For this reason, the drain current I_{ds} can become smaller when sensor is touched. The output signal is judged by the difference when sensor is touched or untouched.

Liquid-Crystal Capacitance Detector has two disadvantages. Because of the transistor T_{ss} is always on, it always consumes power whether pixel is touched or not. The other disadvantage is even more serious. In a sensing array, different sensing pixels on the vertical line share the same readout circuit. Because of the threshold voltage variation of the TFTs in different sensing pixels, touch signal and untouched signal in different pixels are difficultly distinguished by the same readout circuit. The simulation circuit and result are shown in Fig. 1-8 and Fig. 1-9, respectively [5]. In Fig. 1-9, we can see that, touch signal and untouched signal are almost the same when threshold voltage shifts 2V in one pixel but -2V in another pixel. When this case happens, the readout circuit cannot distinguish whether the pixel is touched or not.

1.2 The New Active Touch Panel

Recently, a new active touch panel was proposed in previous thesis [6]. Fig. 1-10(a) shows the operation of new active touch panel by one pixel circuit. We feed two consecutive scan pulses at node G_n and G_{n+1}. Depending on the touch circuit is touched and untouched, the node V_{out} will distinguish between signal and no signal. The verified result is okay when the new active touch panel is small size.

In Fig. 1-11(a) and Fig. 1-11(b) and Fig. 1-11(c), the principals are introduced. The new active pixel circuit is composed of two TFTs (T1, T2), one capacitor (C1). About the two TFTs, one is switch for T1, another is resistor for T2. In addition, we feed two scan pulses at node A and B that is shown in Fig. 1-11(a). In Fig. 1-11(a), when the touch pad is untouched, the pulse of node A passed through T2 and some parasitical resistances and capacitances (C_p), it is like as a first order RC circuit. The node C is a slightly distorted waveform. However, the signal voltage of node C is not high enough to turn on T1 when the scan pulse is in the on-state at node B. In this case, the node D (data line) detects no signal. Fig. 1-11(b) shows the touch pad is touched by the finger. At the moment, the capacitance of pixel circuit which is composed of some parasitical capacitances (C_p), the capacitance of finger (C_f), the capacitance of touch circuit (C1). When the pulse of node A passed through T2 and the capacitances ($C1 + C_p + C_f$), the delay time becomes large at node C. Therefore, when the scan pulse is still in the on-state at node B, the T1 is turned on by the signal of node C, and the node D receives the current signal of node B. Fig. 1-11(c) shows the scan pulse is generated once every frame time (60Hz, 16.67ms). If the finger continuously touches the touch pad, the current signal of node D is generated once every frame time (60Hz, 16.67ms). The current signal is converted to voltage signal by resistor (R1) and comparator.

1.3 Motivation

When the pixel circuit is applied to the large size panel, a critical issue occurs. In real application, the scan loading can affect the operation of far-end on touch panel because the driving pulse is deformed. The influence of scan line is especially serious when the panel is large. The large size panel means that the scan pulses are different at near-end and far-end when the scan loading is increased from small to large. Thus, we simulate the pixel at the far-end in the matrix of touch panel with the large scan loading by adding resistors (100KΩ) and capacitors (2nF) to the pixel. As shown in Fig. 1-10(b), spikes appear in the output signal at the node V_{out} when the scan loading becomes large even the touch panel is untouched. These spikes can lead to a false reading, which must be avoided.

For this false-spike issue, we propose a method that deforms the original scan pulse to be put onto the bus by filtering out the high frequency components in the pulse waveform. Therefore, the pixel circuit of far-end shares the same driving waveform as that of near-end. Thus, the operation is not affected by the loading of scan line, and the output level of data line is unified for both near-end and far-end.

1.4 The Organization of Thesis

In this thesis, there are two major key points that have to discuss. One is to solve the mal-operation issue for large size touch panel. Another is to verify the proposed method with system demonstration.

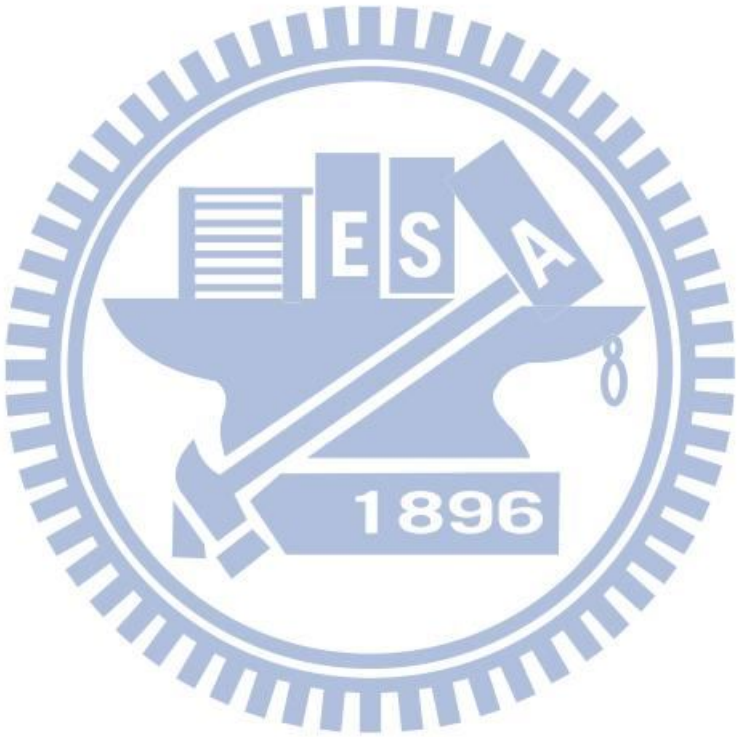
In chapter 1, the history of touch panel is reviewed briefly. In addition, the newly proposed active touch panel is introduced. The issue of the new active touch panel is discussed.

In chapter 2, first of all, the operation of new active touch circuit in the large size panel with significant signal delay is simulated. The mal-operation issue in large size touch panel is

discussed. Then the method proposed to improve the mal-operation issue is discussed with simulation results.

In chapter 3, the proposed method is verified by a system demonstration. The structure of system board is introduced in block diagrams. The results show that the proposed method is effective for the large size touch panel.

Finally, conclusions are given in chapter 4.



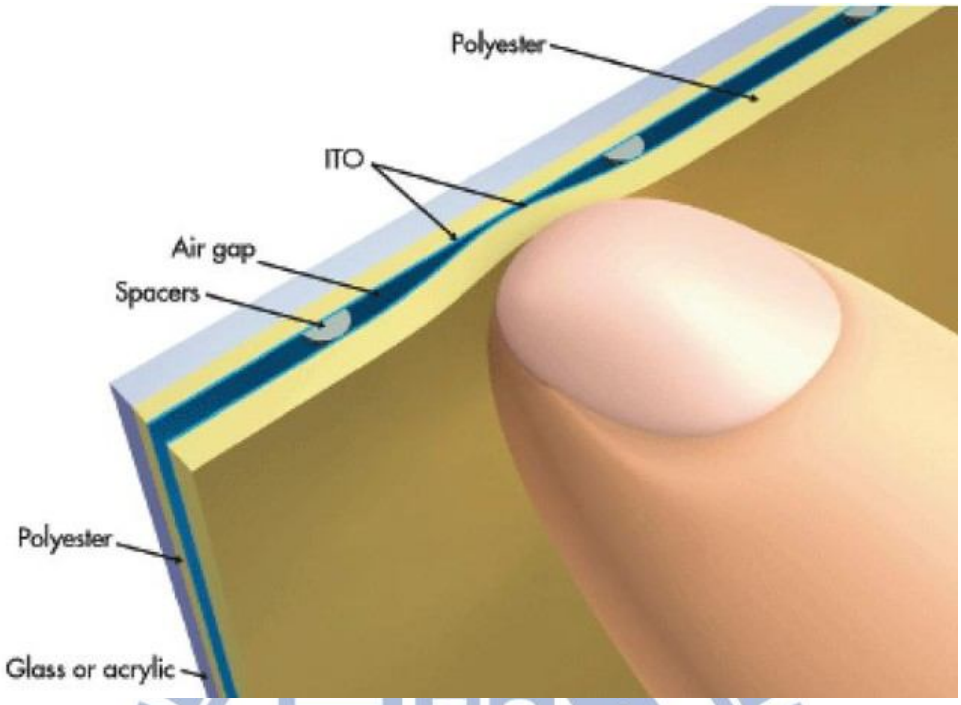


Fig. 1-1 The cross-section view of the resistive touch panel

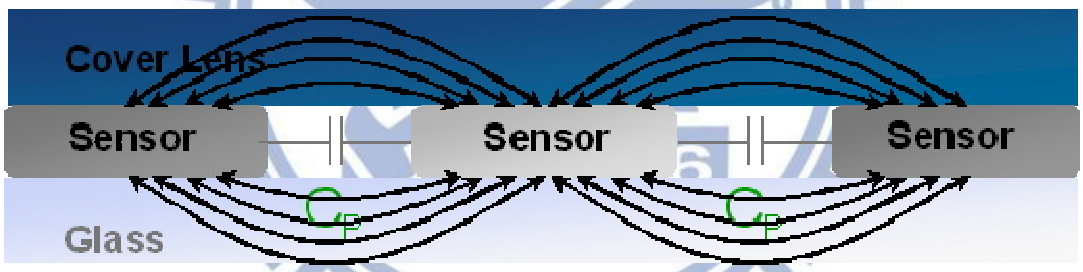


Fig. 1-2 The sketch map of PCT operation principle with panel is untouched

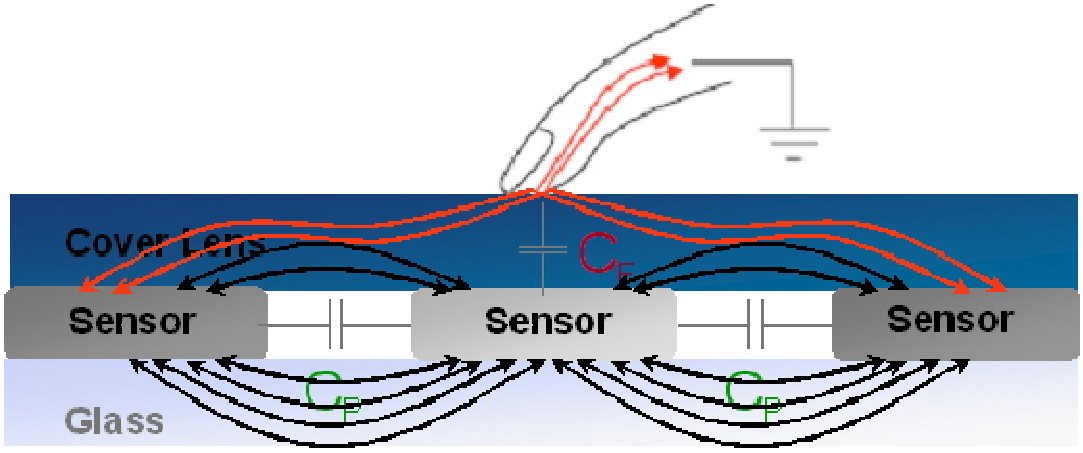


Fig. 1-3 The sketch map of PCT operation principle with panel is touched

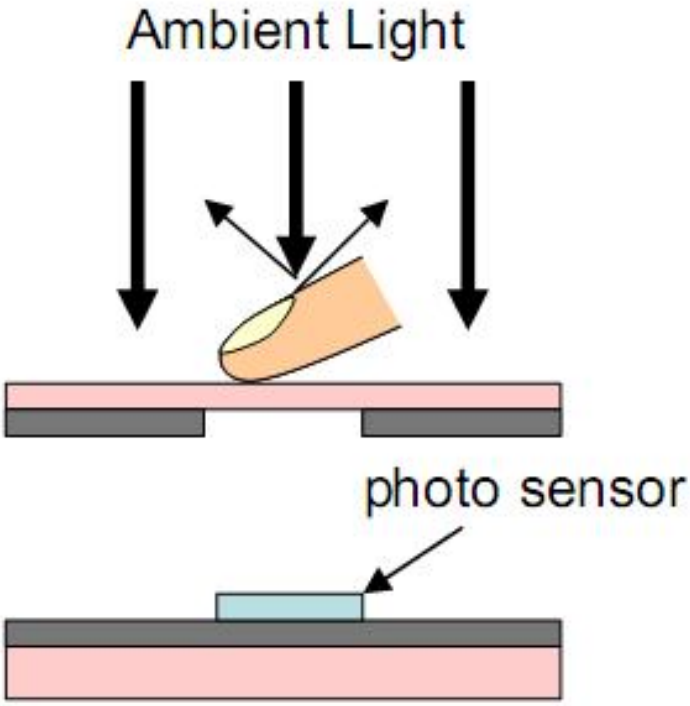


Fig. 1-4 Optical photo sensor

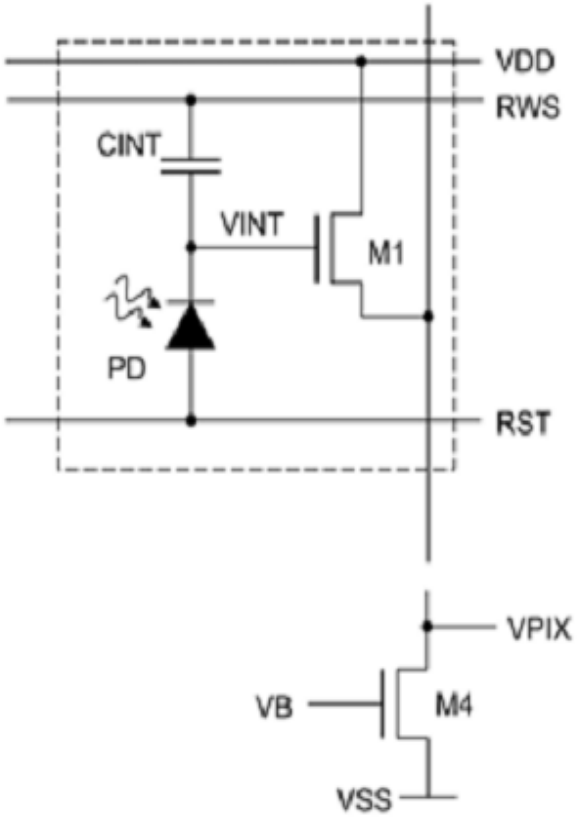


Fig. 1-5 Sensing circuit of optical photo sensor

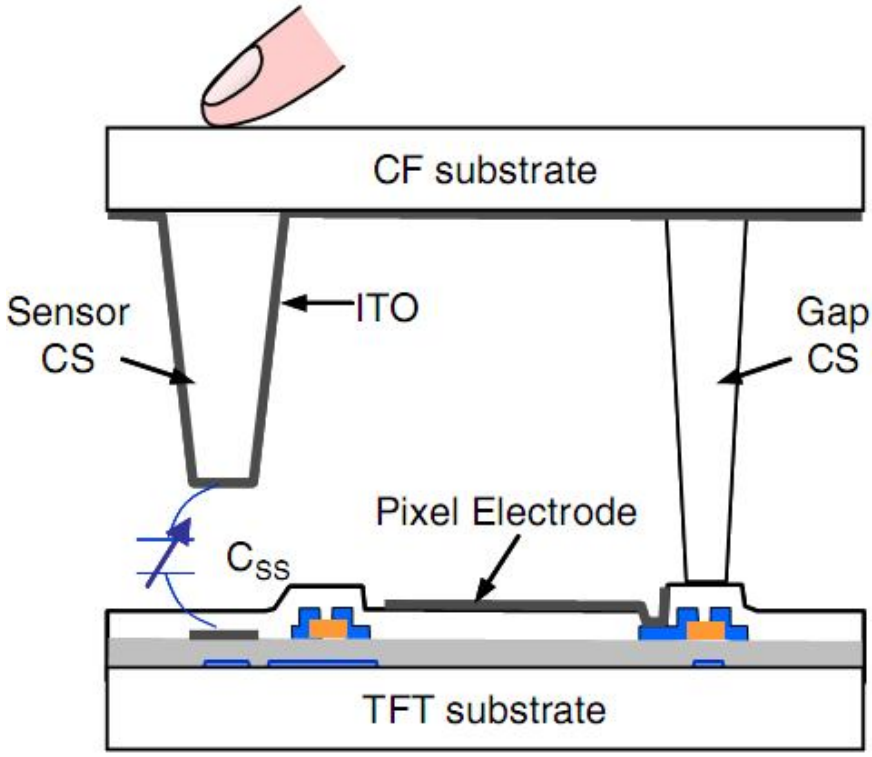


Fig. 1-6 Cross-sectional view of a capacitive sensor

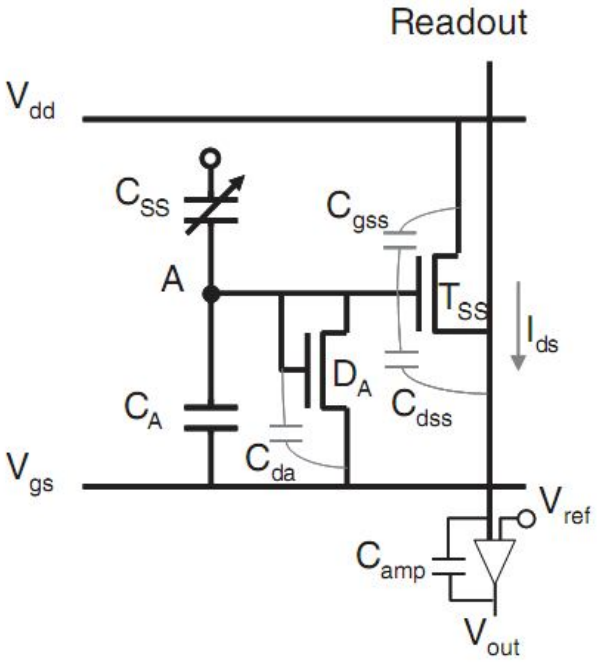


Fig. 1-7 Sensing circuit of Liquid-Crystal Capacitance Detector

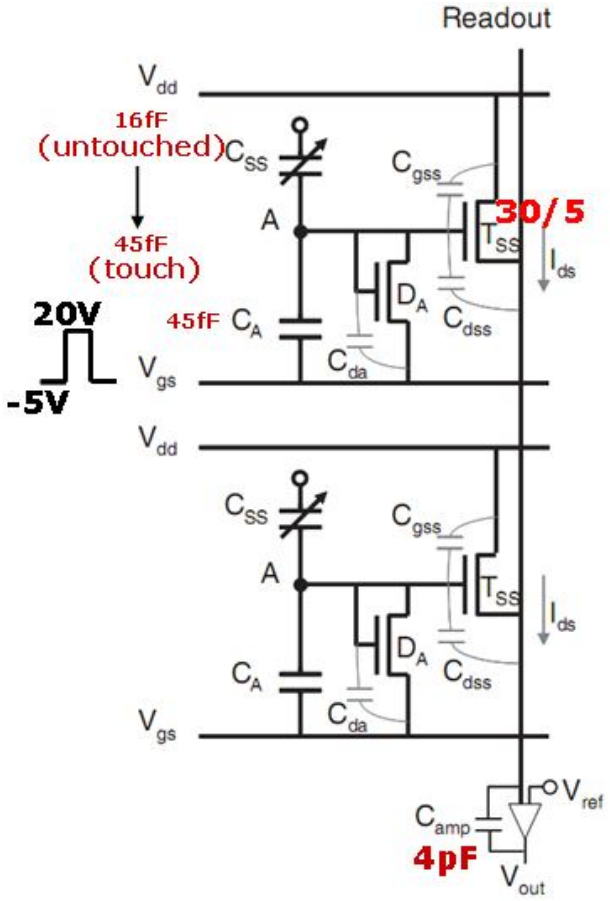


Fig. 1-8 Simulation circuit of Liquid-Crystal Capacitance Detector

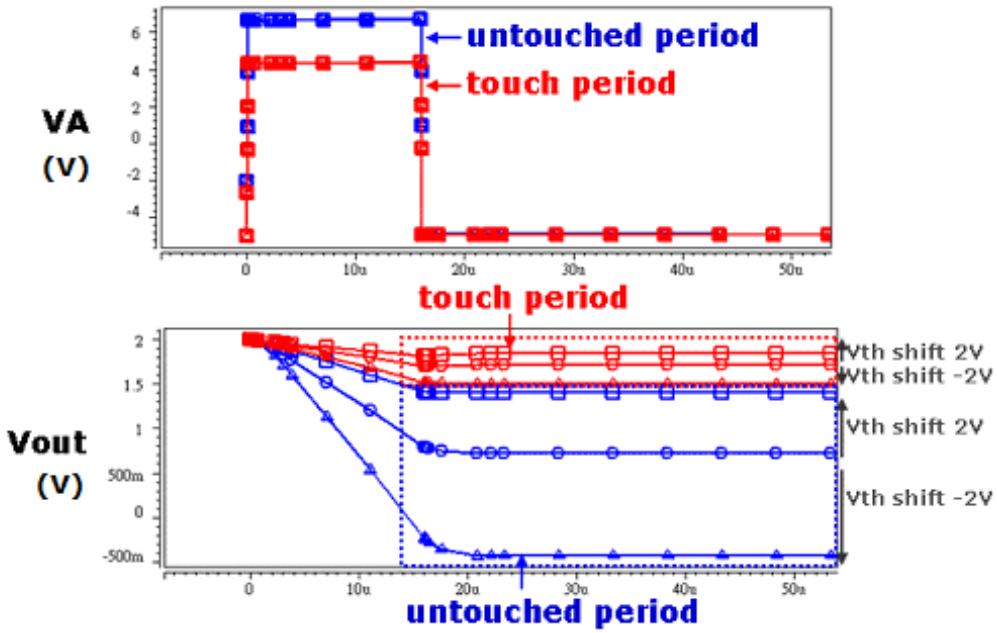


Fig. 1-9 Simulation result of Liquid-Crystal Capacitance Detector

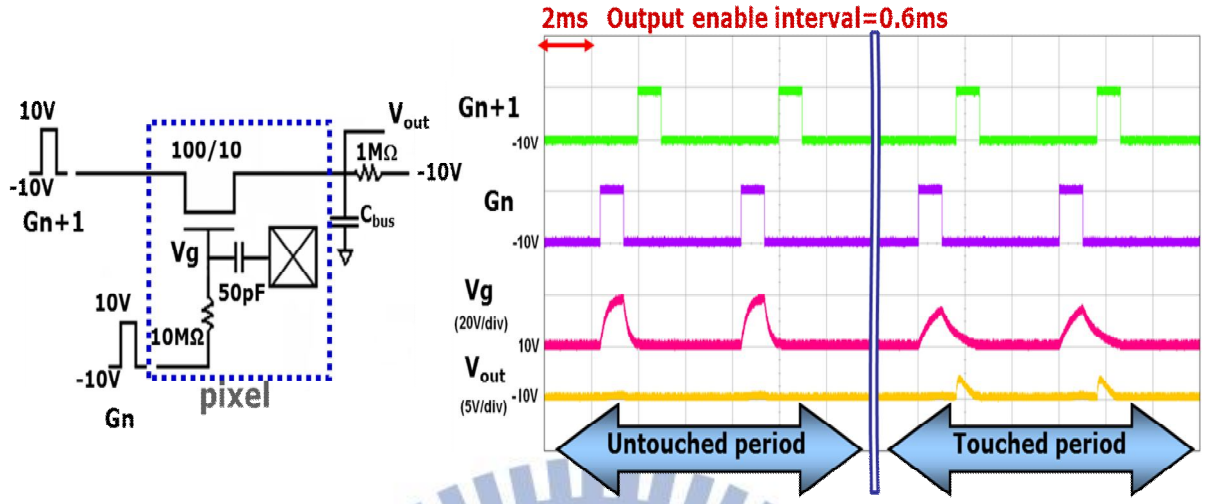


Fig. 1-10(a) 2T1C pixel circuit at near-end

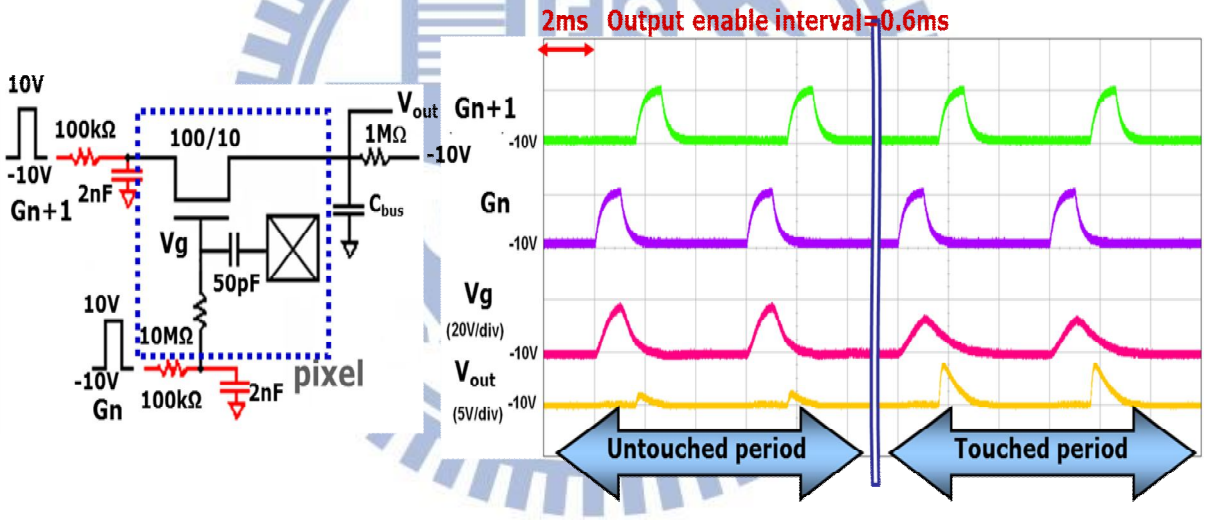


Fig. 1-10(b) 2T1C pixel circuit at far-end

Fig. 1-10 Experimental result for 2T1C pixel circuit

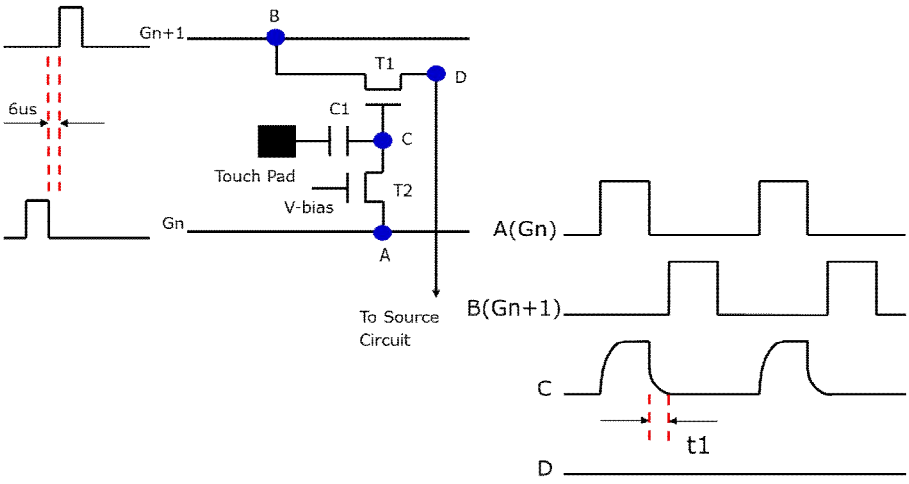


Fig. 1-11(a) The operation of 2T1C pixel circuit (Untouched)

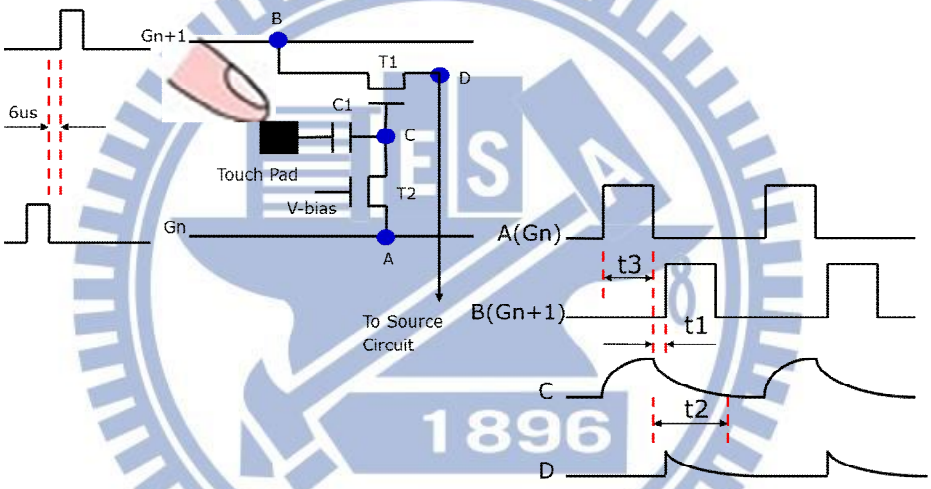


Fig. 1-11(b) The operation of 2T1C pixel circuit (Touched)

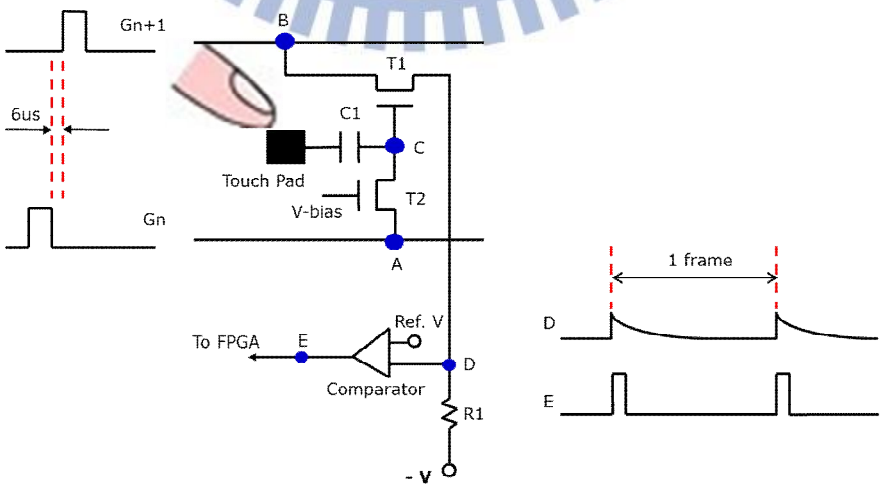


Fig. 1-11(c) The operation of 2T1C pixel circuit with comparator (Touched)

Fig. 1-11 Schematic for 2T1C pixel circuit

Chapter 2 Development of the Large Size Active Touch Panel

2.1 The Analysis of Mal-operation Issue

2.1.1 The Far-End of Scan Bus

As shown in Fig. 2-1, when the touch panel becomes large in size, the RC loadings on the scan lines (dashed line) are increased. The waveforms are distorted at the nodes D and E. Even when the touch pad is untouched, the signal of node D passes through T2 owing to the parasitical resistances and capacitances, which cause the waveform to be distorted more serious at node F. The tail of the distorted waveform can turn on T1. Therefore, the signal of node E passed to data line (S_n) by T1 to be read out.

2.1.2 The Principle of Square Wave

Ideally, the square wave has only two statuses of high and low levels. Between the two statuses are instantaneous transitions. However, this is impossible to achieve practically because of the physical limitations of the system that generates the waveform. When zoom in, we can see that the signal needs time to rise from the low level to the high level and back again, which are called the rising time and the falling time respectively. As shown in Fig. 2-2 [7], the square wave is expressed by the Fourier series which is composed of a fundamental harmonic, namely, N_{th} odd harmonic. For example, for the ideal square wave of 10KHz in frequency, the fundamental harmonic is 10KHz, the third harmonic is 30KHz (3 x 10KHz), the fifth harmonic is 50KHz (5 x 10KHz), the seventh harmonic is 70KHz (7 x 10KHz), …, the N_{th} harmonic is N x 10KHz. Since the odd harmonics are 30KHz, 50KHz, 70KHz, …, and limited in N x 10KHz in practical situation, we can only get a waveform that is similar square wave. If we want to make

the waveform close to ideal square wave, then the amounts of odd harmonics must be increased. The more amounts of odd harmonics are enough, the waveform is closer to the ideal square wave. Fig. 2-3 shows the ideal square wave in the red line, the fundamental harmonic in light blue line, and the other odd harmonics as the third harmonic, the fifth harmonic, the seventh harmonic, the ninth harmonic, the eleventh harmonic. Generally, the wave which is composed of a fundamental harmonic and the N_{th} odd harmonic to the eleventh is good enough to represent a square wave, as shown in Fig. 2-4 [7].

2.1.3 The Principle of First-Order RC Circuit

Next we start to talk about the relationship between square wave and RC circuit. Fig. 2-5 shows the first-order RC circuit which is composed of a resistor, a capacitor. In Fig. 2-5(b), the orange line is the square wave of node V_{in}, the others are exponential waveforms with different time constants at node V_{out}. First of all, we talk about the state of charge (rising). When t=0, the node V_{in} is still 0V, the capacitor C has no electric charge. Due to the time is continuous, the capacitor is charged continuously by the V1 of square wave until the voltage of capacitor is equal to V1. Accordingly, we can find a function that the course of charge is described as below.

$$V_{out}(t) = V_{in} * e^{-\frac{t}{RC}} \quad (2\text{-}1)$$

In function (2-1), the t is time, the RC(τ) is time constant, the node V_{in} is the high level (V1) of square wave, and the node V_{out} is the voltage of capacitor. When the time is increased, the node V_{out} gets higher and higher, but the speed of charge decreases because V_{in} and V_{out} gets closer and closer. If the RC value is small, the speed of charge is fast as shown by the red curve (left side) in 2-5(b). While the RC value is large, the speed of charge is as slow as the light green curve (left side). On the other hand, we can see the similar behavior of discharge (falling) in the RC circuit. When $t = t_n$, the voltage

of node V_{in} is still V1, the capacitor is full of electric charge. Because of the charge continuity in time, the capacitor is discharged by resistor until the electric charge is empty. According to the inferences, we can find a function that the course of discharge is described as below.

$$V_{out}(t) = -V_{in} * e^{-\frac{t}{RC}} \quad (2\text{-}2)$$

The notations in function (2-2) are the same as those in function (2-1).

The time constant RC(τ) in the RC circuit plays an important role. Fig. 2-5(c) shows the detailed waveform of the voltage across a capacitor that is charged with square wave in the RC circuit. During the expense of time is 1 τ , the capacitor is charged t 63.2% of the full swing V1. The capacitor is charged to 99% of the full swing when the expense of time is 5 τ . Similarly, when the capacitor is discharged by resistor, the expense of time 1 τ only approaches 36.8% of the full swing and there is still 1% left to be discharged when the expense of time is 5 τ . Even though the higher approaches of charging and discharging can be achieved by more time, because the speed of charge become even slower, the 5 τ is taken as the charging or discharging time in general application.

2.1.4 The Concept of Fifth-Order RC Circuit

Instead of using real large-size touch panel, we use fifth-order RC circuit to imitate the scan loading on a separate circuit board. Theoretically, the fifth-order RC circuit and upward, its delay waveform is almost the same as that of the scan loading. The way to calculate the delay time (1 τ) for the N_{th} order RC circuit, which is shown in Fig. 2-6 [8]. We will use the calculation result to build the RC circuit to emulate the scan bus delay.

2.1.5 Summary

In large size touch panel, the pixel circuit is generally driven by a square wave at

the near-end. When the touch pad of near-end is touched, it causes the square wave is distorted and the data line of near-end outputs signal. When the touch pad of near-end is untouched, the data line of near-end has no output signal. There is no problem for the operation at the near end. However, for the pixel circuit at the far-end, the square wave passes through scan loading that filters out the high frequency components. In this case, the square wave gets distorted. Thus, the pixel circuit at the far-end can output signal even if the touch pad of far-end is untouched. This mal-operation issue must be solved for the large size active touch panel.

2.2 The Approaches to Solve the Issue

Since the distortion of the waveform results from the filtering out of the high harmonic frequency components, we offer a new driving method to solve this issue. In Fig. 2-7, the basic concept of new driving method is illustrated. to show that the high frequency components of scan pulses are filtered by the first-order RC circuits (R_O and C_O), and how they transmit to two scan lines with G1 and G2 afterward. Theoretically, after the high frequency components of scan pulse are filtered, the waveform is no more affected by the scan loading (fifth-order RC circuit). Therefore, the scan pulses are similar at both near-end and far-end. In other words, the waveform at node A is similar to that at node D, and the one at node B is similar to that at node E. As to be discussed below, this new driving method is to be primitively verified by software simulation.

2.2.1 The Simulating Scheme

As shown in Fig. 2-8(a) and Fig. 2-8(b) and Fig. 2-8(c), the simulation of the pixel circuit for large size touch panel is composed of two scan-pulse generators, two first-order RC circuits, two pixel circuits at near-end and far-end, two scan loadings, which are indicated with orange, red, blue and green boxes, respectively. The scan pulse

generator provides a square wave with levels of +10V and -10V. The first-order RC circuit is composed of one resistor, one capacitor. The values of resistance and capacitance are yet to be decided according to the scan loading. The near-end and far-end pixel circuits each comprise a NMOS (Mx_xx), two parasitical capacitances (Cgdx_xx, Cgsx_xx), a resistance (Rbiasx), a capacitance of finger (Csensing_xx), an external resistance (Routx), and an external bias (Vbiasx). The scan loading is composed of five series first-order RC circuits.

2.2.2 The Simulated Results without Filtering Out the High Frequency Components

In the driving waveform, the gap between scan pulses G_n and G_{n+1} is defined as GT_OE. The scan pulse width in the on-state is 92us and the GT_OE is 6us in this simulation, as shown in Fig. 2-9. In Fig. 2-10(a) and Fig. 2-10(b), the cases when the touch pad is untouched and touched are illustrated respectively. The "$\tau_{untouched}$" and "$\tau_{touched}$" are the delay times in incorporation of C1 and some parasitical capacitances (C_{gd}, C_{gs}), as well as the corresponding capacitance of finger (C_f). In Fig. 2-10(c), the "τ_{delay}" indicates the delay time of scan loading. In order to design the new active touch circuit, the below equation of delay time must be satisfied:

$$\tau_{untouched} < \tau_{delay} < \tau_{touched}$$

In our simulation, $\tau_{untouched}$ is 1us and $\tau_{touched}$ is 9.2us, while two conditions of the τ_{delay} are set as below:

Condition 1: $\tau_{delay} = 1.036us$

Condition 2: $\tau_{delay} = 8.82us$

Then we define two experimental conditions. One is invariant duty cycle for scan pulse (gate on-state is 92us, GT_OE is 6us). The other is variant duty cycle for scan

pulse which is decided by the delay time of scan loading. According to the two experimental conditions, we can check the relationship between the pixel circuit of far-end and the scan loading when the touch pad is untouched or touched.

In Fig. 2-11, the node A denotes the scan pulse G_n of near-end, the node B represents the scan pulse G_{n+1} of near-end, the node D indicates the scan pulse G_n of far-end, the node E signifies the scan pulse G_{n+1} of far-end, the node S1 means the data line of near-end, and the node S_n marks the data line of far-end.

If the scan loading (τ_{delay}) of touch panel is 1.036us, there are no signals at data line of near-end (S1) and far-end (S_n) when the touch pads are untouched, as shown in Fig. 2-11(a). If the scan loading (τ_{delay}) of touch panel increases to 8.82us, the "S1" is still no output signal, but there is output signal at data line of far-end (S_n) even when the touch pads are untouched, as shown in Fig. 2-11(b).

As shown in this experiment, we know that if the scan loading becomes large and the duty cycle of GT_OE keeps invariant, the pixel circuit of far-end has false signal. This makes us to think more about this issue. Considering that the scan loading is increased when the touch panel size becomes large, if the duty cycle of GT_OE can be accordingly adjusted, the data line of far-end might not output false signal when the scan pulse G_{n+1} is on-state. It seems to be a way to solve the false signal issue at far-end, which is to be check hereafter.

First of all, we calculate the quintuple RC delay time of scan loading, which decides the duty cycle for T1 turning on. Once the duty cycle of GT_OE is defined, we can then determine the quintuple RC delay time. As mentioned in section 2.1.3, the quintuple RC delay time (5τ) is 44.1us for τ_{delay} = 8.82us, correspondingly. Here, we accordingly decide the GT_OE to be 50us.

In Fig. 2-12, the node A denotes the scan pulse G_n of near-end, the node B

represents the scan pulse G_{n+1} of near-end, the node D indicates the scan pulse G_n of far-end, the node E signifies the scan pulse G_{n+1} of far-end, the node F means the scan pulse G_n of far-end that passes through RC filter (T2 & C1), and the node S_n marks the data line of far-end.

If the GT_OE is 50us and the touch pad is untouched, there is no signal on data line (S_n) at far-end as we expected. It seems that the mal-operation issue of far-end is solved, as shown in Fig. 2-12(a). However, when the GT_OE is 50us, even the touch pad is touched, there is no signal on data line (S_n) at far-end as shown in Fig. 2-12(b). It becomes mal-functional in the other way.

As shown in the experiments above, we find that if the duty cycle of GT_OE is adjusted to be small, the data line of far-end cannot output signal whether the touch pad is untouched or touched or not. When the duty cycle is set large, the false signal of far-end as the touched is untouched seems to be solved. However, when the touch pad is touched, the signal of node F is not high enough to turn on the T1 when the next scan pulse G_{n+1} (node B, red curve) is "Hi" state. The problem on the other hand prohibits the data line of far-end to output correct signal. Thus, it is difficult to properly adjust the duty cycle of GT_OE for both near and far ends.

In the next section, by filtering out high frequency components, it is verified that the issue of false signals can be solved by the idea mentioned in section 1.3.

2.2.3 The Simulated Results with Filtering Out the High Frequency Components

In Table 2-1, the "R_L * C_L($=\tau_{delay}$)" is the time constant of scan loading, and the "R_O * C_O($=\tau_{external}$)" is the time constant for external first-order RC filter. We define three conditions of $\tau_{external}$ that confirm the data line signals are correct at near-end and far-end whether the scan loading is small or large. The three conditions of $\tau_{external}$ are

$\tau_{external} < \tau_{delay}$, $\tau_{external} = \tau_{delay}$, and $\tau_{external} > \tau_{delay}$ respectively. We start from simulating the case of filtering out the high frequency components and confirm the indifference of scan pulses at near-end and far-end in section 2.2.3.

In Fig. 2-13, we show the scan pulses of near-end and far-end when scan for the three conditions of high frequency filtering RC with scan loading (R_L * C_L = 8.82us). The node V1 means scan pulse G_n, the node V2 marks scan pulse G_{n+1}, the node A and node B denote the signals of first-order RC filter at near-end (G_n and G_{n+1}), the node D and node E represent scan pulses at far-end (G_n and G_{n+1}). As the simulation results, external first-order RC filter with the larger time constant , the waveform difference on the scan bus is between near-end (node A) and far-end (node D) can be reduced. The time differences respectively indicated by t4, t5, and t6 in Fig. 2-13(a), (b), and (c) get from large to small.

According to above mentioned, we infer that if the waveforms of scan pulses at near-end and far-end get more similar, their data line signals become less different in both untouched or touched cases, since the driving waveforms for the pixels are not much variant.

In Fig. 2-14, we further show the data line signals of near-end and far-end. the node V1 means scan pulse G_n, the node V2 marks scan pulse G_{n+1}, the node A and node B denote output signals of first-order RC filter at near-end (G_n and G_{n+1}), the node D and node E represent scan pulses at far-end (G_n and G_{n+1}), the node S1 indicates the signal of data line at near-end, the node S_n signifies the signal of data line at far-end.

In Fig. 2-14(a), the $\tau_{external}$ of 4us is less than the τ_{delay} (8.82us). When the touch pads of near-end and far-end are both untouched, at near-end, the signal of node B in the on-state overlaps the signal of node A in the off-state and the data line has a pulse which is -9.47V. At far-end, the signal of node E in the on-state overlaps the signal of

node D in the off-state and the data line has a pulse which is -8.65V. On the other hand, when the touch pads of near-end and far-end are both touched, at near-end, the signal of node B in the on-state overlaps the signal of node A in the off-state and the data line has a pulse which is -7.17V. At far-end, the signal of node E in the on-state overlaps the signal of node D in the off-state and the data line has a pulse which is -6.92V.

In Fig. 2-14(b), the $\tau_{external}$ is equal to the τ_{delay} (8.82us). When the touch pads of near-end and far-end are both untouched, at near-end, the signal of node B in the on-state overlaps the signal of node A in the off-state and the data line has a pulse which is -8.61V. At far-end, the signal of node E in the on-state overlaps the signal of node D in the off-state and the data line has a pulse which is -8.22V. On the other hand, when the touch pads of near-end and far-end are both touched, at near-end, the signal of node B in the on-state overlaps the signal of node A in the off-state and the data line has a pulse which is -6.65V. At far-end, the signal of node E in the on-state overlaps the signal of node D in the off-state and the data line has a pulse which is -6.80V.

In Fig. 2-14(c), the $\tau_{external}$ of 17.64us, is greater than the τ_{delay} (8.82us), which is 17.64us. When the touch pads of near-end and far-end are both untouched, at near-end, the signal of node B in the on-state overlaps the signal of node A in the off-state and the data line has a pulse which is -8.05V. At far-end, the signal of node E in the on-state overlaps the signal of node D in the off-state and the data line has a pulse which is -7.90V. On the other hand, when the touch pads of near-end and far-end are both touched, at near-end, the signal of node B in the on-state overlaps the signal of node A in the off-state and the data line has a pulse which is -6.60V. At far-end, the signal of node E in the on-state overlaps the signal of node D in the off-state and the data line has a pulse which is -6.76V.

Table 2-2 is generalized from the collection of simulation results. Basically it is better to drive the touch pads with less difference between near-end and far-end no

matter they are untouched or touched. In Table 2-2, we show that if the $\tau_{external}$ is less than the τ_{delay}, the differences of near-end and far-end are too obvious to sort out the difference. With the $\tau_{external}$ is increased, the differences of near-end and far-end are lessen. Even more, the differences of near-end and far-end can be further reduced in case that the $\tau_{external}$ is greater than the τ_{delay}.

2.2.4 Summary

In this chapter, we verify the fixed timing of scan pulse first. Gradually a false signal appeared on the data line for the untouched pad of far-end, when the scan loading is increased from small to large. Therefore, we try to increase the duty cycle of GT_OE to improve the false signal issue of far-end and it seemed to work. However, it results in another kind of failure that the touched pad of far-end has no more signal. Then, we propose the method of filtering out the high frequency components of scan pulse before input to scan line, so that the data line signals of near-end and far-end are similar. Thus, by properly designing the external source circuit, we can make the data line signals at near-end and far-end are almost the same no matter the touch pads are untouched or touched. This concept of filtering out the high frequency components is to be verified by implementation in chapter 3.

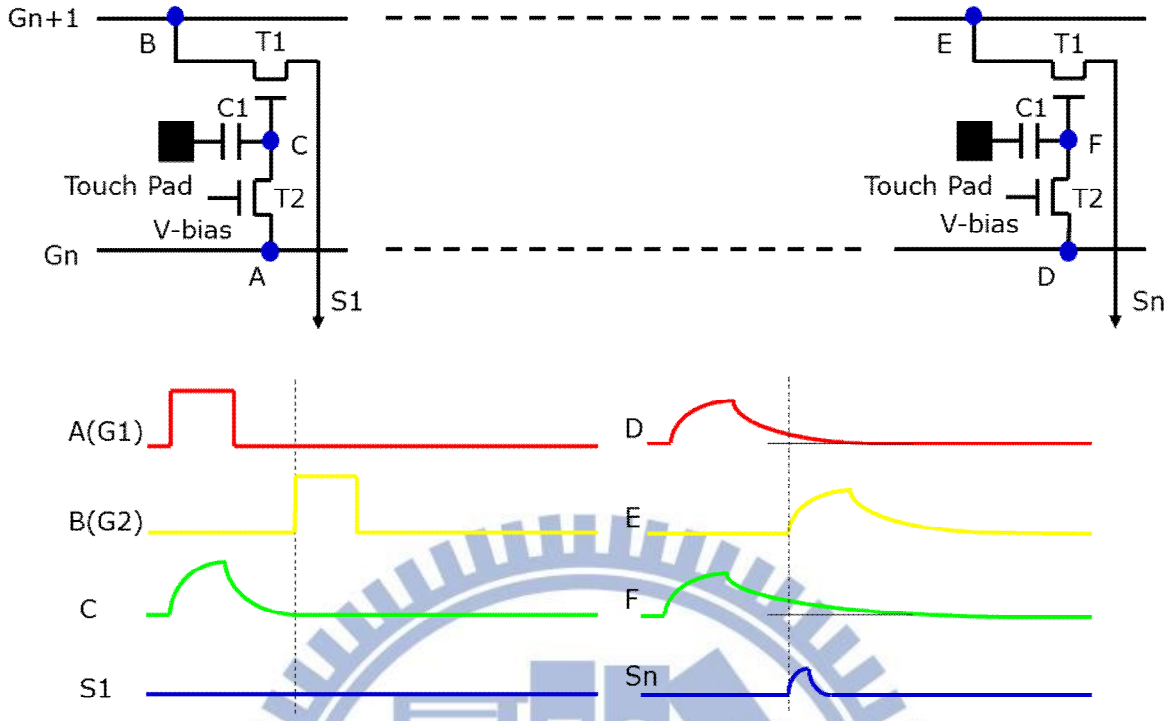
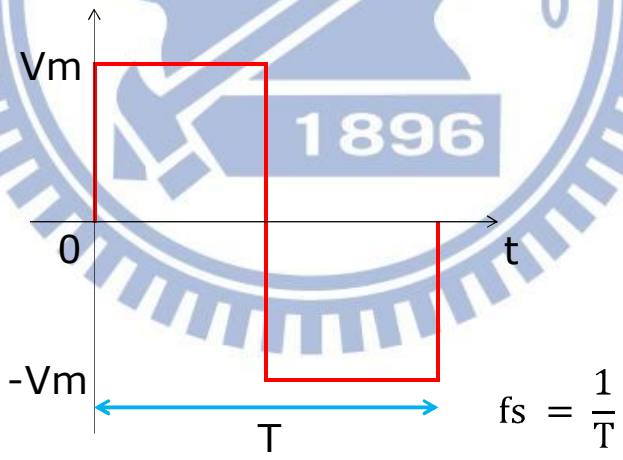


Fig. 2-1 The loading issue of scan line for large size touch panel



Fourier Series

$$V(t) = \frac{4}{\pi} Vm \left[\underbrace{sin2\pi fst}_{\text{Fundamental harmonic}} + \underbrace{\frac{1}{3} sin2\pi(3fs)t}_{\text{3'rd harmonic}} + \underbrace{\frac{1}{5} sin2\pi(5fs)t}_{\text{5'th harmonic}} + \cdots + \underbrace{\frac{1}{N} sin2\pi(Nfs)t}_{\text{N'th harmonic}} \right]$$

Fig. 2-2 The Fourier series of square wave

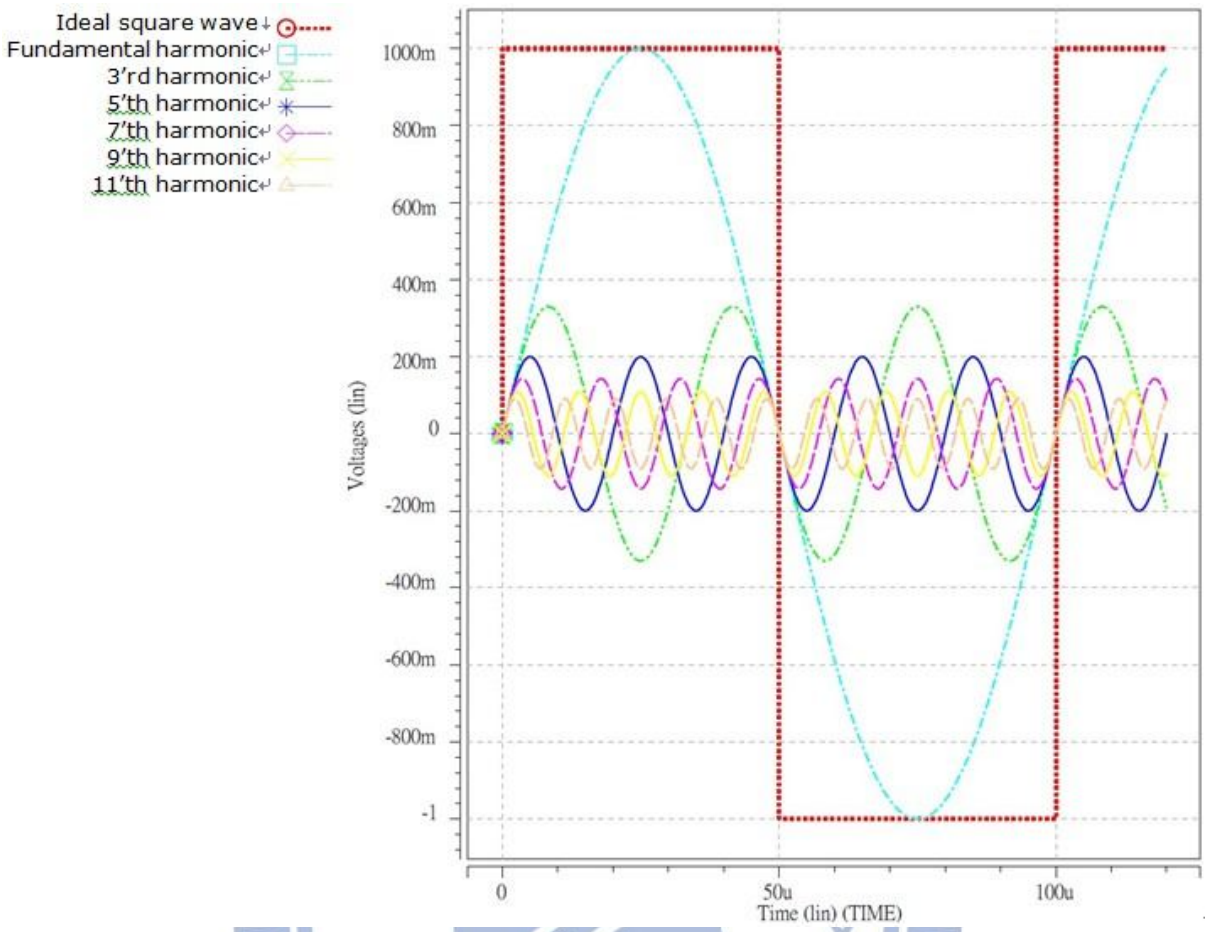


Fig. 2-3 Composition of square wave in fundamental harmonic and odd harmonics

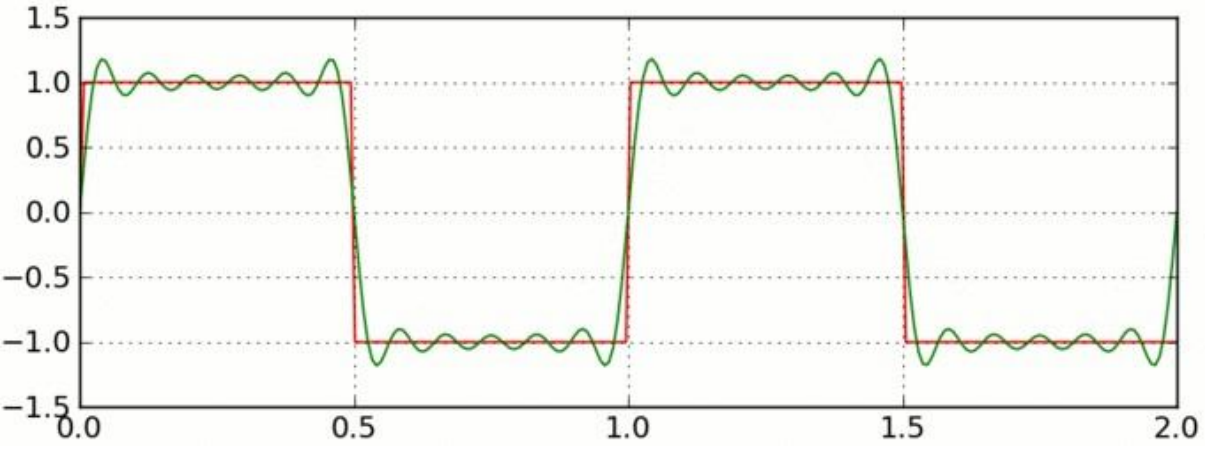


Fig. 2-4 Ideal and actual square waves

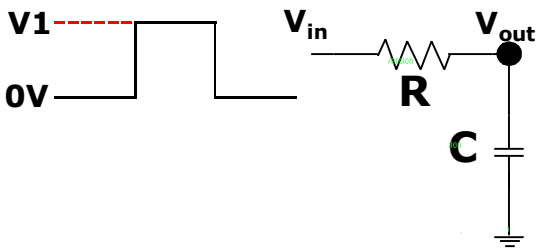


Fig. 2-5(a) First-order RC circuit

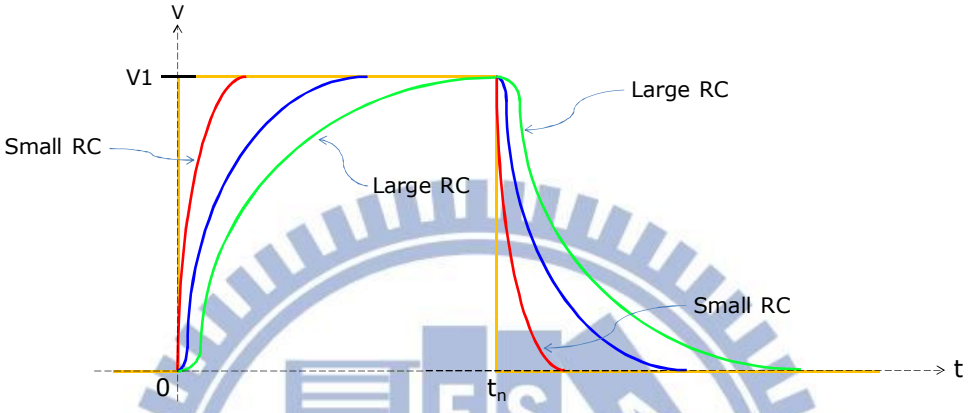


Fig. 2-5(b) The difference between small RC and large RC

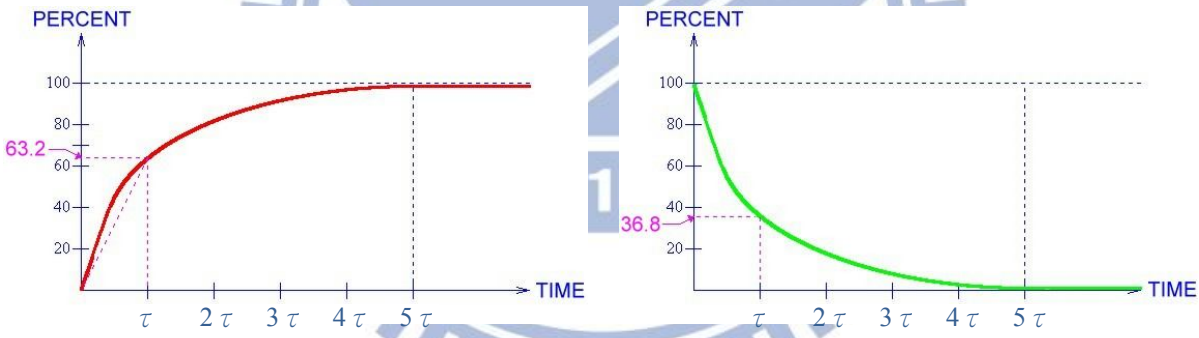
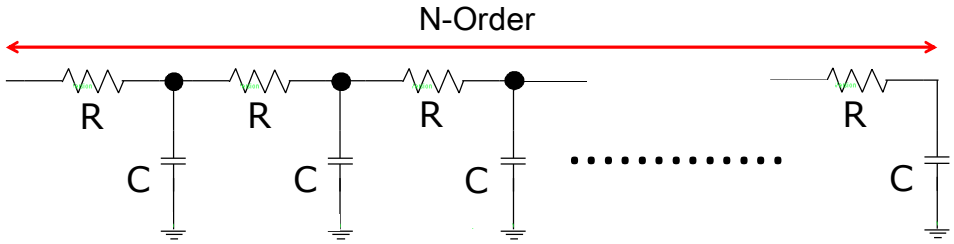


Fig. 2-5(c) The curves of charge (rising) and discharge (falling)

Fig. 2-5 The principle of square wave



$$1\tau = \frac{N(N+1)RC}{2}$$

Fig. 2-6 The delay time for N-Order RC circuit

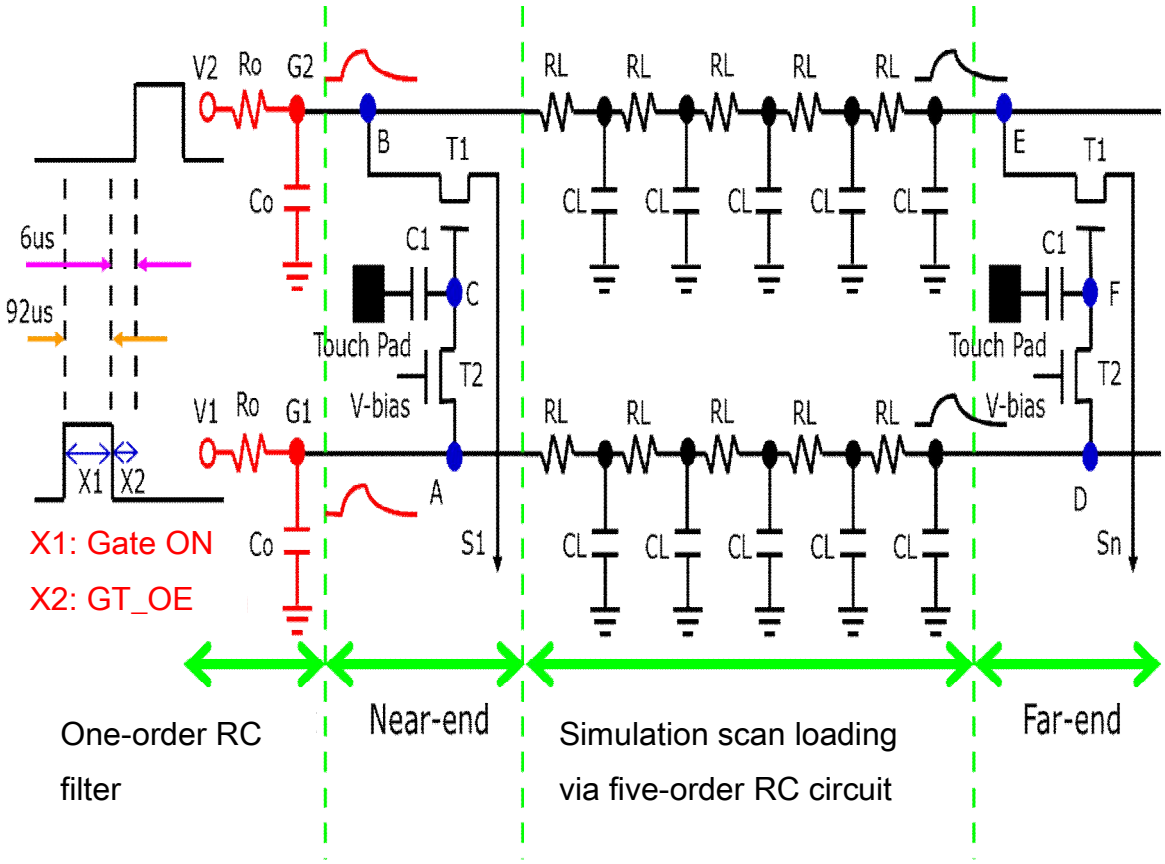


Fig. 2-7 Improvement method for the loading issue in large panel

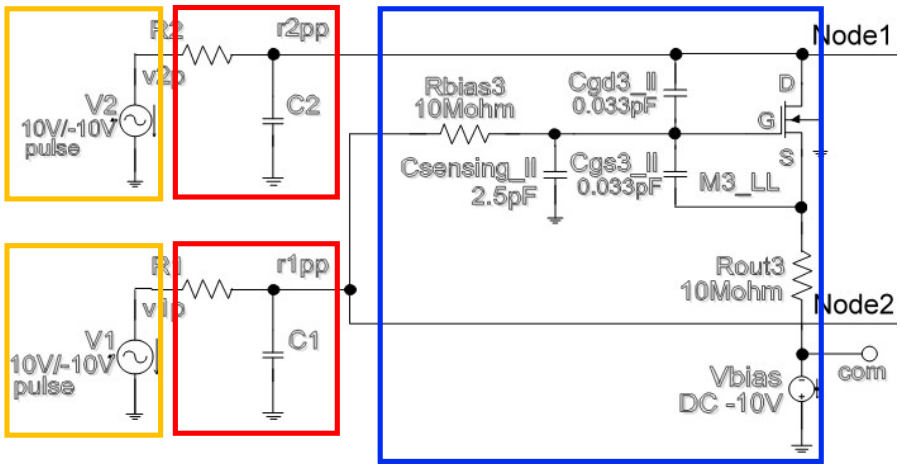


Fig. 2-8(a) 2T1C pixel circuit with RC circuit at near-end

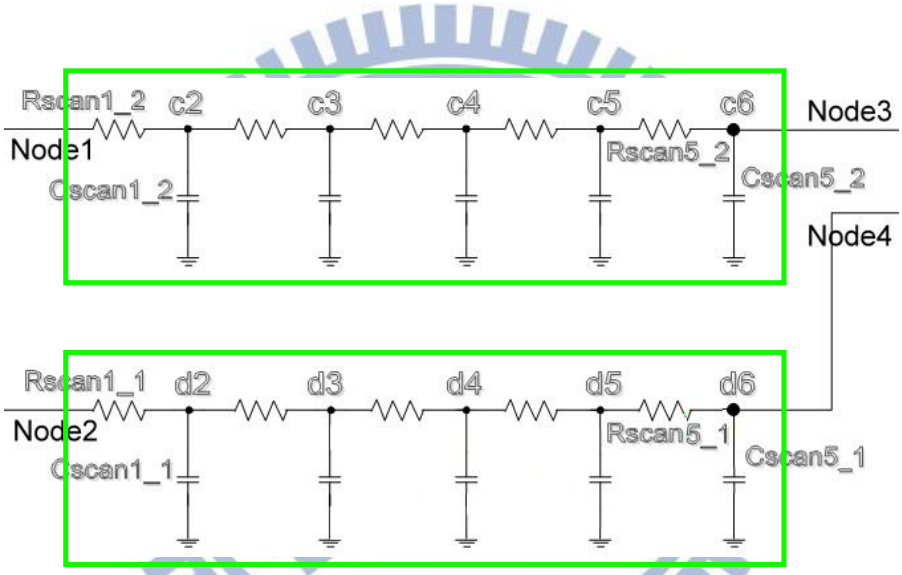


Fig. 2-8(b) Scan loading

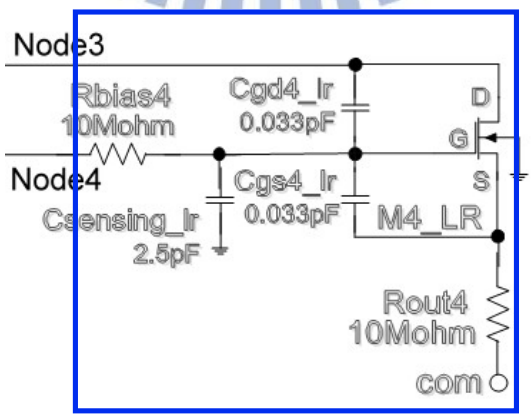


Fig. 2-8(c) 2T1C pixel circuit at far-end

Fig. 2-8 Schematic for simulating the large size touch panel

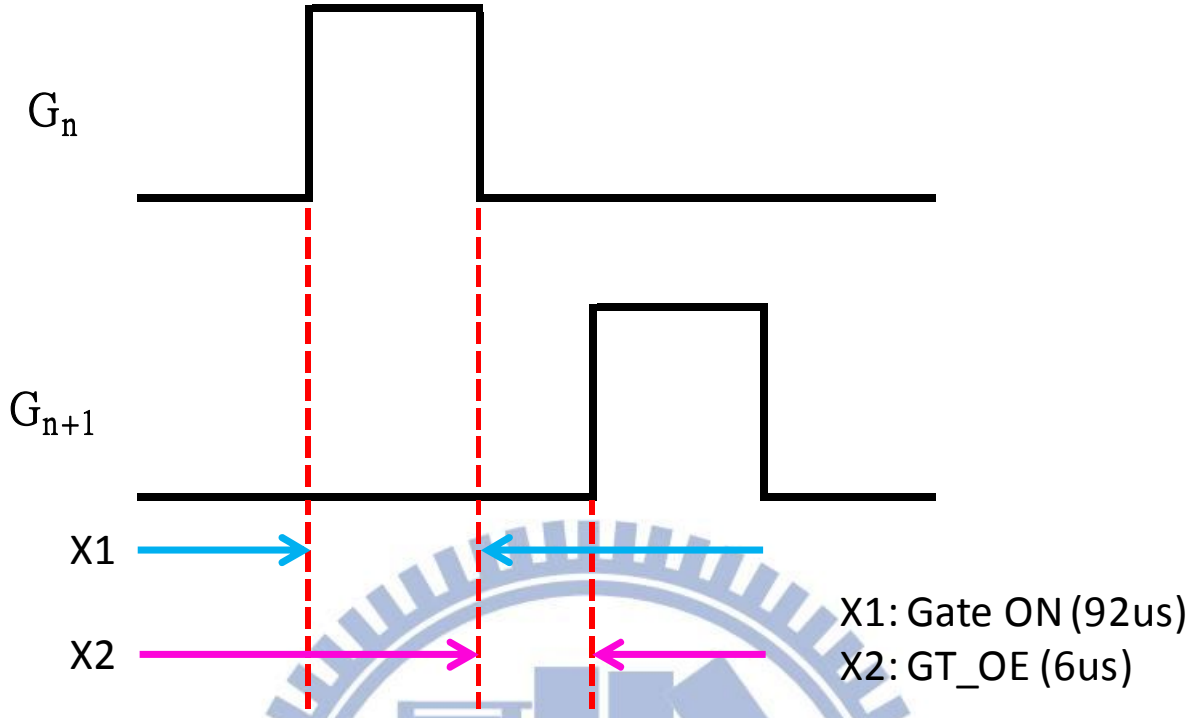


Fig. 2-9 The definition of scan pulse

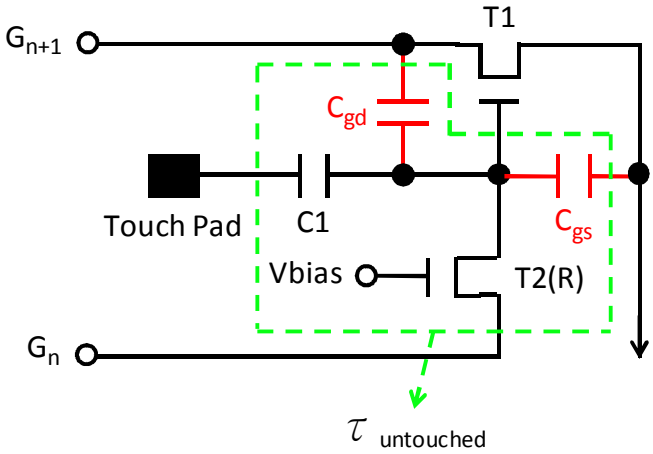


Fig. 2-10(a) When the touch pad is untouched, $\tau_{untouched} = T2(R) \times (C1 + C_{gd} + C_{gs})$

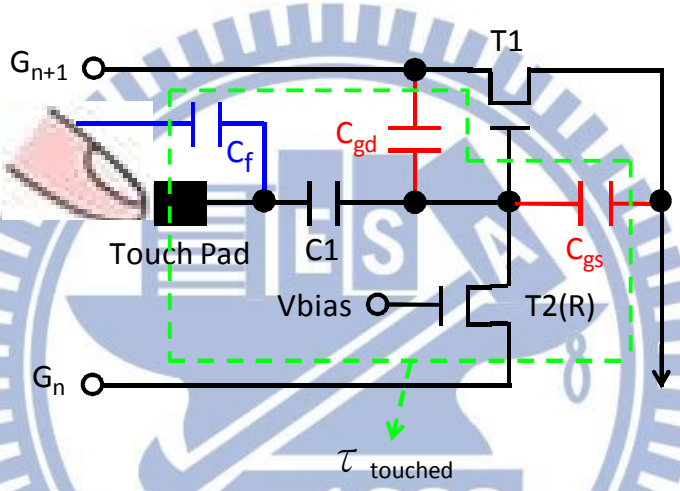


Fig. 2-10(b) When the touch pad is touched, $\tau_{touched} = T2(R) \times (C1 + C_f + C_{gd} + C_{gs})$

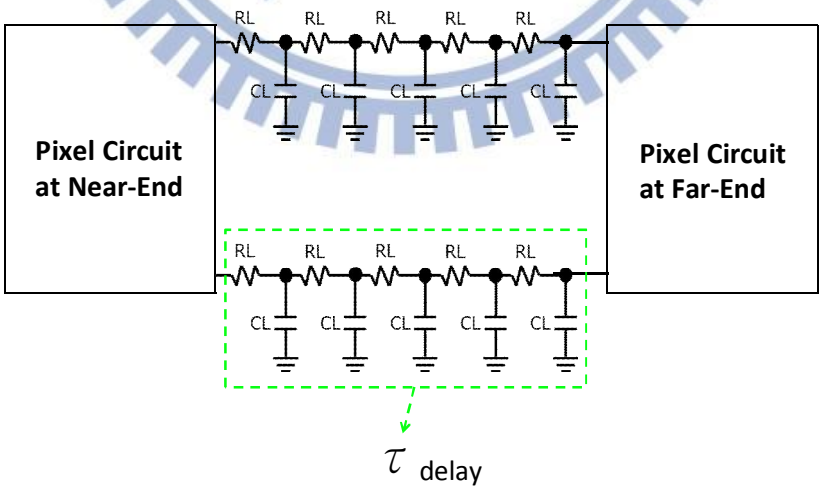


Fig. 2-10(c) The loading of scan line, $\tau_{delay} = 5 \times 3 \times R_L \times C_L$

Fig. 2-10 The cases of RC delay time

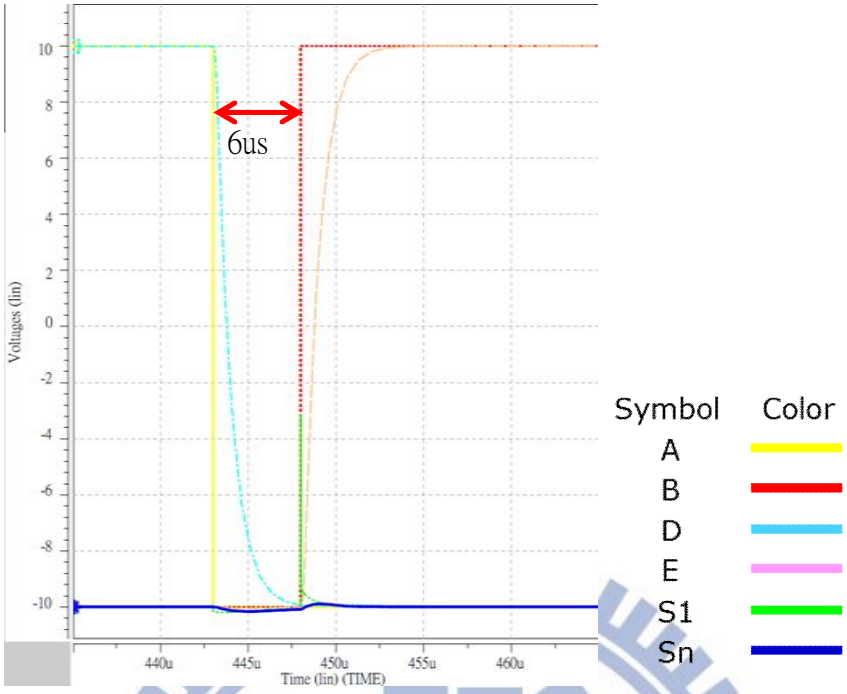


Fig. 2-11(a) τ_{delay} = 1.036us

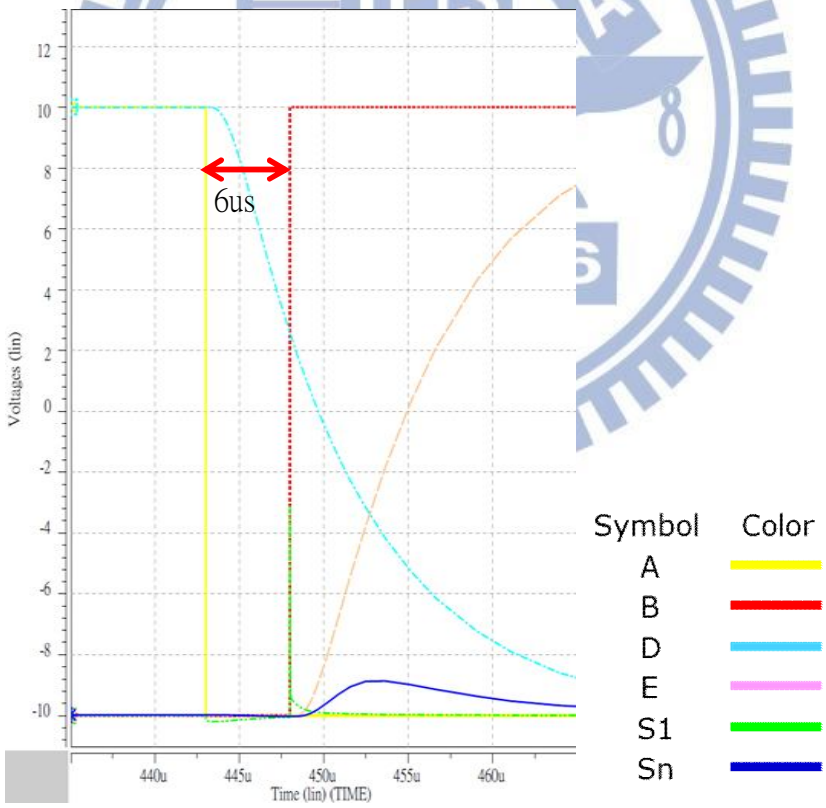


Fig. 2-11(b) τ_{delay} = 8.82us

Fig. 2-11 The simulation results of the untouched pixel at far end for the two conditions of scan delay time with fixed GT_OE

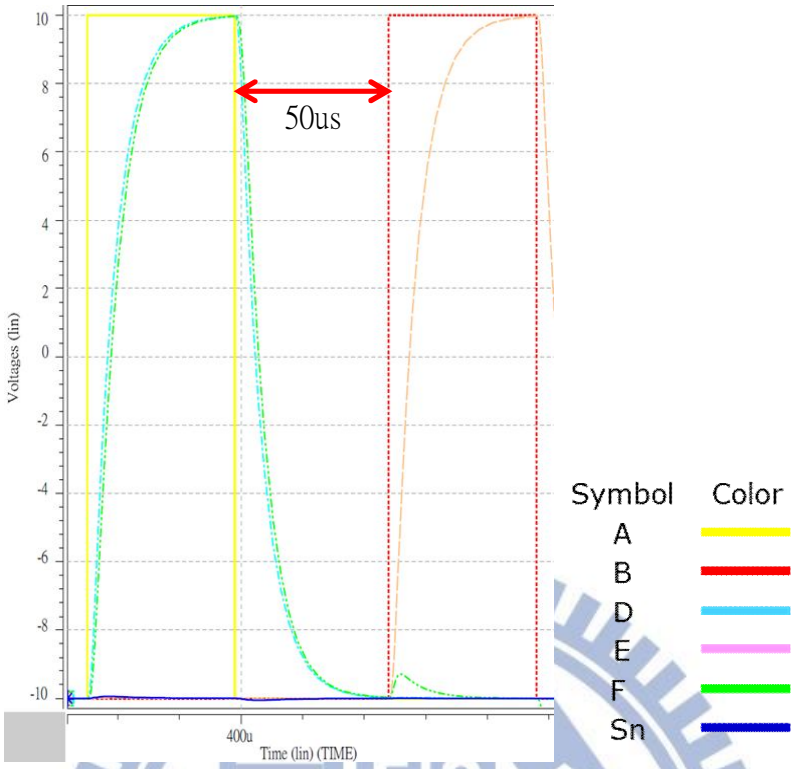


Fig. 2-12(a) τ_{delay} = 8.82us, untouched

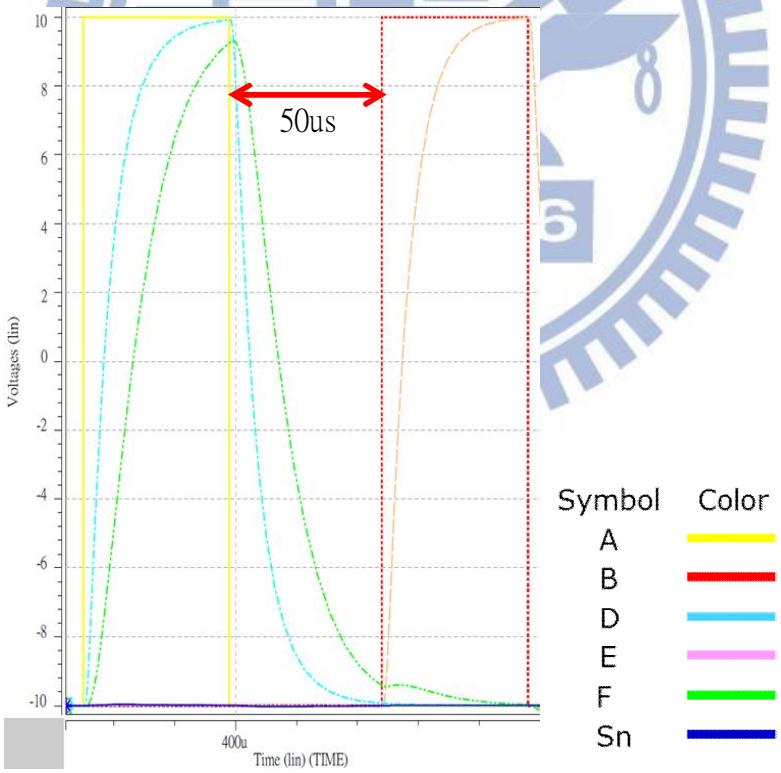


Fig. 2-12(b) τ_{delay} = 8.82us, touched

Fig. 2-12 The simulation result of the untouched and touched pixels at far-end for the condition of scan delay time with increased GT_OE

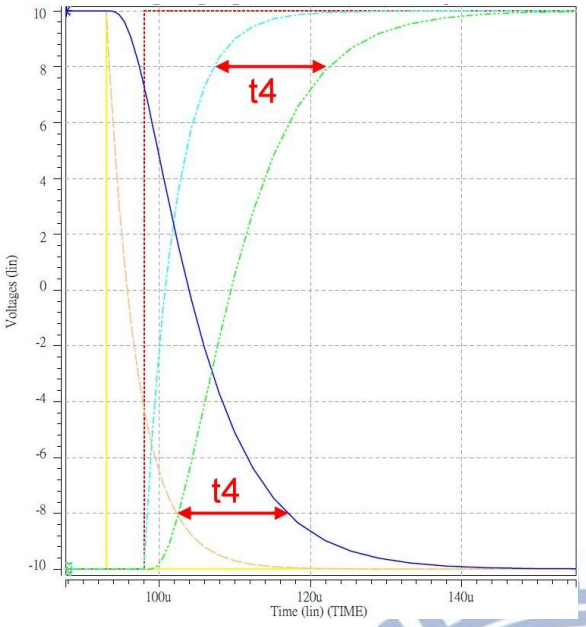


Fig. 2-13(a) The time constant of externa first-order RC filter is 4us

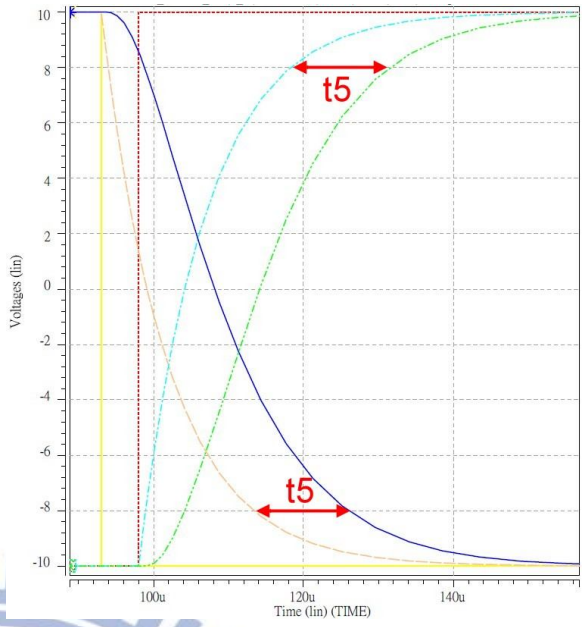


Fig. 2-13(b) The time constant of external first-order RC filter is 8.82us

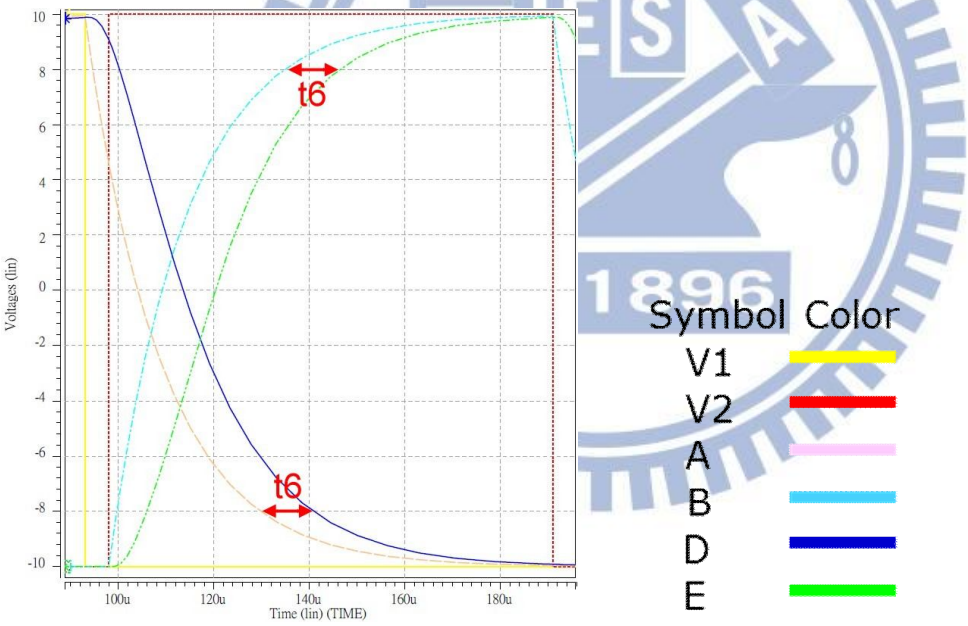


Fig. 2-13(c) The time constant of external first-order RC filter is 17.64us

Fig. 2-13 The scan pulses of near-end and far-end when scan loading is 8.82us

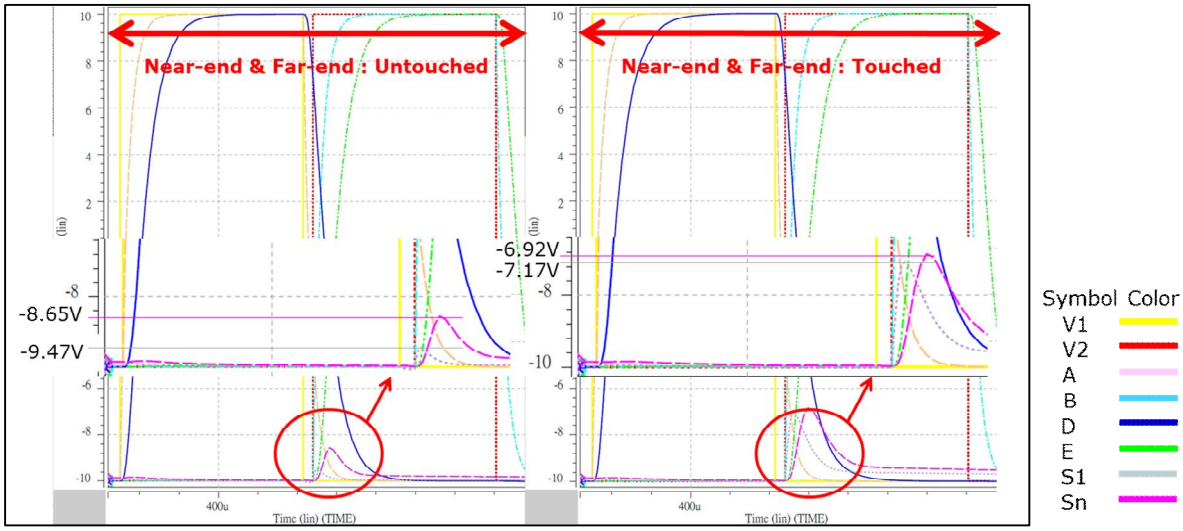


Fig. 2-14(a) Experiment1_1, R_O x C_O = 4us

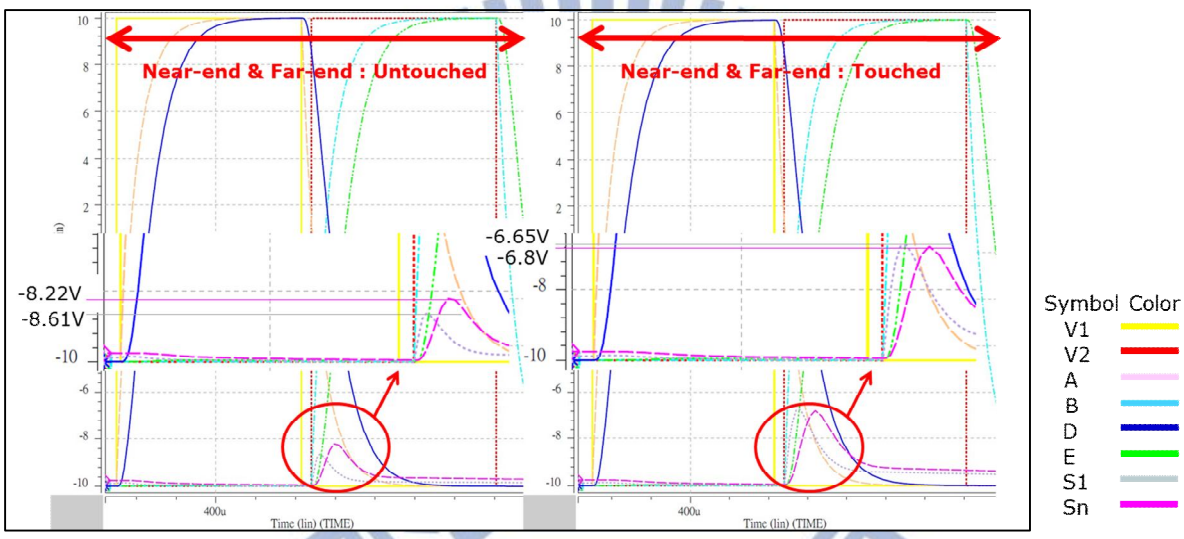


Fig. 2-14(b) Experiment1_2, R_O x C_O = 8.82us

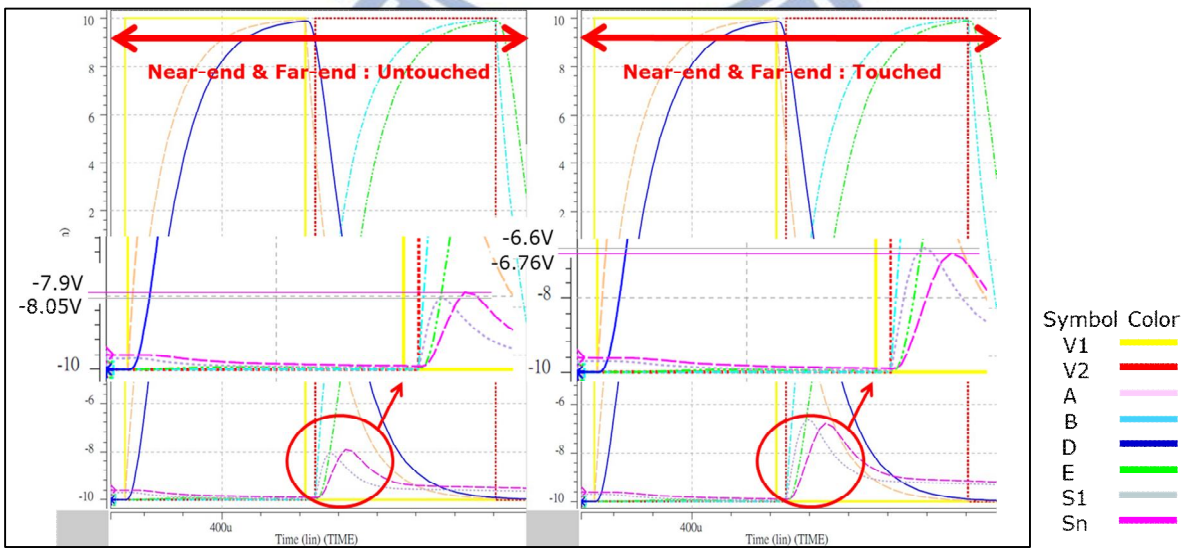


Fig. 2-14(c) Experiment1_3, R_O x C_O = 17.64us

Fig. 2-14 The data line signals of near-end and far-end when scan loading is 8.82us

Experiment No.	Gate ON	GT_OE	R_L	C_L	R_L*C_L	R_o*C_o
1_1	92us	6us	84KΩ	7000fF	8.82us	4us
1_2						8.82us
1_3						17.64us

Table 2-1 The different time constant of external RC filter with scan loading is 8.82us

R_L*C_L	Ro*Co (External RC Filter)	Untouched			Touched		
		Near-end (V1)	Far-end (V2)	| V2-V1 |	Near-end (V3)	Far-end (V4)	| V4-V3 |
8.82us	4us	-9.47V	-8.65V	0.82V	-7.17V	-6.92V	0.25V
	8.82us	-8.61V	-8.22V	0.39V	-6.65V	-6.8V	0.15V
	17.64us	-8.05V	-7.9V	0.15V	-6.6V	-6.76V	0.16V

Table 2-2 The data line signal levels at near-end and far-end with different time constant of external RC filter when scan loading is 8.82us

Chapter 3 Demonstration of the Large Size Active Touch Panel

3.1 System Overview

In addition to the simulation, we also prepare a system board and four pieces of touch panel (9 x 9 touch panel) to verify the functionality of the large size touch panel. The system is composed of the graphical user interface (GUI) and the printed circuit board assembly (PCBA). The GUI sets parameters for controlling PCBA. It controls the operation of PCBA with start and stop, and it also displays the location of touching. The four pieces of touch panel put on PCBA for simulating the four corners of large size touch panel.

After the FPGA receives the control parameter of GUI, it begins to generate the driving signals for touch panel. The driving signals are transferred to high voltage level and input to the scan line of touch panel. When the touch pad is touched, the data line outputs current signal and a comparator transfers the current signal to the logic signal of the FPGA. The FPGA confirms the location of finger and replies the coordinate information to GUI. Finally, the GUI shows the location of finger by dot.

3.1.1 Graphical User Interface (GUI)

In Fig. 3-1, we show that the GUI includes three blocks. The first part is display area (red square), which displays the location of touching. The second part is setting parameters area (blue square), which sets the frame rate for touch panel and the duty cycle of scan signals namely, HSY Hi, HSY Lo, VSY Hi, and VSY Lo, as well as others set parameters (system clock, scan line). The third part is control system area (green square), which controls the PCBA to start or stop.

3.1.2 Printed Circuit Board Assembly (PCBA)

In Fig. 3-2, we show the block diagram of PCBA, which includes six parts. The first part is power. It includes the main power for whole system, the power of the FPGA (light blue block), and the generator of high voltage (dark blue block). The second part is the control chip (FPGA). It is the core of the control system (bright green block). The third part is the serial interface. It commutes the signal levels between PC and the FPGA (olive green block). The fourth part is the scan circuit. It transfers the signal levels of the FPGA first (yellow block) and then the transformative signals input to logic shift register (sky blue block) that generate scan pulses. Finally, the level shifters transform the scan pulses into high voltage (orange block). The fifth part is the comparator circuit. The reference voltage generator generates a precision voltage and inputs to the comparators. The comparators transform the current signals of the data line into logic signals (pink block). Then these logic signals transmit to the FPGA. The final part is RC circuit. It includes RC1 and RC2. The RC1 is a first-order RC circuit (white block) and it filters out the odd harmonic of scan pulse. The RC2 is a fifth-order RC circuit (red block). It simulates the loading of the scan line and the data line for large size touch panel.

3.1.2.1 Power Circuit

In Fig. 3-3, we show the block diagrams and pictures of the power circuits. The outside power is DC 12V. The two PWM ICs generate DC 3.3V and 5V. The 3.3V provides the serial interface, the comparators, and six pieces of PWM IC. The 5V provides logic circuits for scan circuits, level shifter from 3.3V to 5V, and main control chip (XC6SLX4) for PCBA.

3.1.2.2 UART Interface Circuit

In Fig. 3-4, we show the block diagrams and pictures of the interface circuits. The MX3232 is voltage level shifter for serial interface (UART). It transforms the voltage level of serial port ('0' → +15V, '1' → -15V) into logic level ('0' → 0V, '1' →

3.3V). When the GUI transmits the control parameters to the FPGA, it transfers the voltage level from the serial port of PC to CMOS logic by RIN2 (From UART) pin, and the CMOS logic signal transmits to the FPGA by ROUT2 (UART Data to FPGA) pin. Before the FPGA replies the coordinate information to GUI, it outputs the coordinate information to DIN2 (FPGA Data to UART) pin. In the meantime, the MAX3232 chip transfers the signal level from CMOS logic to serial port with PC, and these signals transmit to PC side by DOUT2 (To UART) pin.

3.1.2.3 Core Chip (FPGA)

In Fig. 3-5, we show the block diagrams and pictures of the core chip. The FPGA receives the command of the GUI by ROUT2 (UART Data to FPGA) pin. When the FPGA starts, it generates the logic signals (GT_CLK, GT_SP1, GT_SP2) and receives the signals of data line from touch panel. After the FPGA received the signals of data line, it checks the location of finger and calculates the coordinate data. Then, the coordinate information is transmitted to PC by DIN2 (FPGA Data to UART) pin. The GUI shows the location of finger on display window.

3.1.2.4 Scan (Gate) Circuit

In Fig. 3-6, we show the block diagrams of the scan circuit. The scan circuit includes three parts. The first is level shifter1. It converts the FPGA signals (DC 3.3V) to DC 5V signals. The second is logic shift register. The GT_CLK of 5V is used to be the clock of logic shift register. When the GT_SP1 of 5V starts, the bus1 generates pulses from G1 to G10, which are shown in Fig. 3-7(a). Then the GT_SP2 with 5V starts, and the bus1 generates pulses from G123 to G132, which are shown in Fig. 3-7(b). The third is level shifter2. It transforms the 5V pulses of logic shift register into the plus voltage (VGH) and minus voltage (VGL). The plus voltage and minus voltage are provided for touch panel.

In Fig. 3-8, we show the block diagrams and pictures of the level shifter1. The level shifter1 transfers the signal level from FPGA signal (3.3V) to 5V signal. It is composed of three resistors, one capacitor, and one transistor. The circuits of GT_CLK and GT_SP1 and GT_SP2 are the same structure. In Fig. 3-9, we show the circuit of the level shifter1. The transistor (MMBT3904) is a switch. When the node D_{in} is 0V, the transistor is in the on-state, and thus the node D_{out} outputs 0V, which is shown in Fig. 3-9(a). When the node D_{in} is 3.3V, the transistor is in off-state, and thus the node D_{out} becomes 5V, which is shown in Fig. 3-9(b). Due to the electric charge remains on the transistor of pole B and E with on-state and off-state, it causes the speed slower for on-state and off-state. Therefore, we add a capacitor (221) to avoid the residual electric charge and fasten the speed for on-state and off-state.

Fig. 3-10(a) and Fig. 3-10(b) show the upper and lower sides of the logic shift register, respectively. They are composed of a D type flip-flop (74AS174), a "AND" gate (74AS08). The D type flip-flop and "AND" gate both are dependent on GT_CLK (A2). When we feed the GT_SP1 (B2) into D type flip-flop, the flip-flop outputs a pulse (1Q) in the next clock. In this way, the flip-flop follows the clock (GT_CLK) to work and outputs pulses one by one (1Q, 2Q, 3Q, …) through to the final channel. In Fig. 3-10(c), we show that every pulse is subject to "AND" operation with GT_CLK (A2) by logic IC ("AND" gate) and then these signals (1Y, 2Y, 3Y, …) are output to level shifter2.

Fig. 3-11 shows the block diagrams and pictures of the level shifter2. The logical signals with 5V swing are transferred to large swing signals with plus voltage (VGH) and minus voltage (VGL) in level. The input levels of 0V and 5V correspond to VGL and VGH, respectively.

3.1.2.5 Comparator (Source) Circuit

Fig. 3-12 shows the eighteen sets of comparator in block diagram and their picture. It transforms the signals of data line into logical signals for FPGA. Fig. 3-13 shows the reference voltage generator for comparators. It is composed of a variable resistor, two fixative resistors, a capacitor, and an operational amplifier (OPA). The voltage is adjusted by variable resistor to that we need. The voltage of variable resistor is stabilized by the capacitor (1uF). The OPA can avoid the impedance matching issue between the variable resistor and the loading. Fig. 3-14 shows the single circuit of comparator. The current of data line transfers to voltage by the resistor (10MΩ) and then the voltage is input to the node V_{in} of comparator. If $V_{in} > V_{ref}$, the V_{out} outputs 3.3V, else the V_{out} outputs 0V. Because the internal structure of node V_{out} is open collector, the node V_{out} must connect a resistor (2KΩ) to 3.3V. The resistor (1KΩ) is used for current limitation between the comparator and the FPGA.

3.1.2.6 RC Circuit

In Fig. 3-15, we show the RC circuits with their pictures. The RC circuit includes two types. The first type is a first order RC circuit. It filters out the odd harmonics of scan pulse, as shown in Fig. 3-15(a). The second type is a fifth order RC circuit, which is shown in Fig. 3-15(b). It simulates the loadings of scan line and data line. In this application, the delay time of first order RC circuit must be greater than the delay time of fifth order RC circuit for the right operation of the touch panel, as mentioned in 2.2.3.

3.1.2.7 Pixel Circuit

In Fig. 3-16(a), we show the pixel circuits with their pictures. The basic pixel circuit is composed of one MOSFET (2N7000), two registers (1Mohm), one

capacitor (0.2nF). As shown in Fig. 3-16(b), the circuit simulating pixel array is composed of two pixel circuits, two fifth order RC circuits (blue line). The fifth order RC circuit is same as scan loading. In Fig. 3-16(c), we show the structure simulating the whole touch panel by adding two RC filters (red line) to the circuit of Fig. 3-16(b).

According to the design conditions of pixel circuit, the delay time of node V_g is set to be 90 us when the touch pad is untouched, while the delay time of node V_g is set to be 250us when the touch pad is touched. In the implemented structure, because the touch pad is composed via jump wire, its parasitic capacitances are large and the couple effect of T1 becomes large, too. Thus, when T1 turns off, the small signal flows through it and the signal level is around 2.6V. In general application, it is taken as logic '0'.

3.2 Experimental Results

3.2.1 The Results without Filtering Out the High Frequency Components

We first verify the data lines at the near-end and far-end whether they have signals or not when the touch pad is untouched. In Fig. 3-17, the duty cycle of scan pulse is fixed, where the gate on time is 876.69us and GT_OE is 600us.

When the scan loading is small, which is corresponding to the delay time τ_{delay} of 100us, its quintuple time constant is less than GT_OE. As shown in Fig. 3-17(a), the data line signal is 2.6V in level when the touch pad of far-end is untouched. As mentioned in section 3.1.2.7, the signal of 2.6V is judged to be logic '0' in the normal operation. In this case, the data line has no false signal at far-end. On the other hand, when the scan

loading is large, which is corresponding to the delay time τ_{delay} of 300us, its quintuple time constant is greater than GT_OE. As shown in Fig. 3-17(b), its data line has the false signal with 6.4V when the touch pad of far-end is untouched.

Furthermore, we want to check the data line status at far-end if the GT_OE is increased to be greater than 5 x τ_{delay}. As shown in Fig. 3-18, when GT_OE is set at 1600us and the touch pad of far-end is untouched, its data line outputs a 2.6V signal. It seems to solve the false signal issue. However, the data line also outputs 2.6V signal even when the touch pad is touched. As discussed in 2.2.2, this is not what we want.

In the next section, we will test if this issue can be solved by filtering out the high frequency components of scan pulse before it is input to scan lines of touch panel.

3.2.2 The Results with Filtering Out the High Frequency Components

First of all, we test how the time constant ($\tau_{external}$) of external RC filter relates to the scan loading (τ_{delay}) in the operation of the touch panel. We set τ_{delay} to be 300us, and $\tau_{external}$ of external RC filter is set at 150us, 300us and 620us respectively. As shown in Fig. 3-19(a), when the $\tau_{external}$ is 150us, the external RC circuit does not have enough ability to filter out the high frequency components, so the scan loading can still influence the output signal (CH1) of external RC circuit obviously. It is also observed that the scan pulse (CH2) at far-end is distorted seriously. As shown in Fig. 3-19(c), if $\tau_{external}$ is greater than τ_{delay}, the scan pulse at near-end (CH1) is similar to far-end (CH2). Thus, the data line signals of near-end and far-end are very close, no matter the touch pads are untouched or touched.

Then, we continue to verify the data line signals of near-end and far-end for the cases of $\tau_{external}$ to be 150us, 300us, 620us. In Fig. 3-20 to 3-22, the CH1 probes the data line signal at the near-end, while the CH2 probes at the far-end.

With $\tau_{external}$ of 150us, as shown in Fig. 3-20(a), the difference between CH1 and CH2 at the both ends when the touch pads are untouched is only 200mV. On the other hand, when the touch pads are touched, because of the obvious influences from the scan loading, the difference increases to 640mV, as shown in Fig. 3-20(b).

For the external RC filter $\tau_{external}$ of 300us screens out more high frequency components, when the touch pads are untouched, the difference reduces to 120mV, as shown in Fig. 3-21(a). As for the case that the touch pads are touched, the difference also reduces to 120mV, as shown in Fig. 3-21(b).

With even larger external RC filter $\tau_{external}$ of 600us, most of high frequency components are filtered out, and thus the scan pulses are very similar between near-end and far-end. For both cases that the touch pads are untouched or touched, the difference between CH1 and CH2 is around 40mV, as shown in Fig. 3-22.

3.3 Summary

According to the result of implementation, we know that if the duty cycle of scan pulse is fixed and the scan loading is increased, the data line of far-end outputs false signal indeed. For this issue, if we increase the duty cycle of GT_OE, it seems to solve the false signal at far-end, but it prohibits the data line signal at the far-end even when the touch pad is touched. Ultimately, by filtering out the high frequency components for scan pulse before it is inputs to touch panel, we make the scan pulse waveforms at near-end and far-end similar. Thus, the data line signals at near-end and far-end are similar and both correct. It is proven by the implementation of the test board that the mal-operation issue can be solved by the appropriate design of the driving circuit.

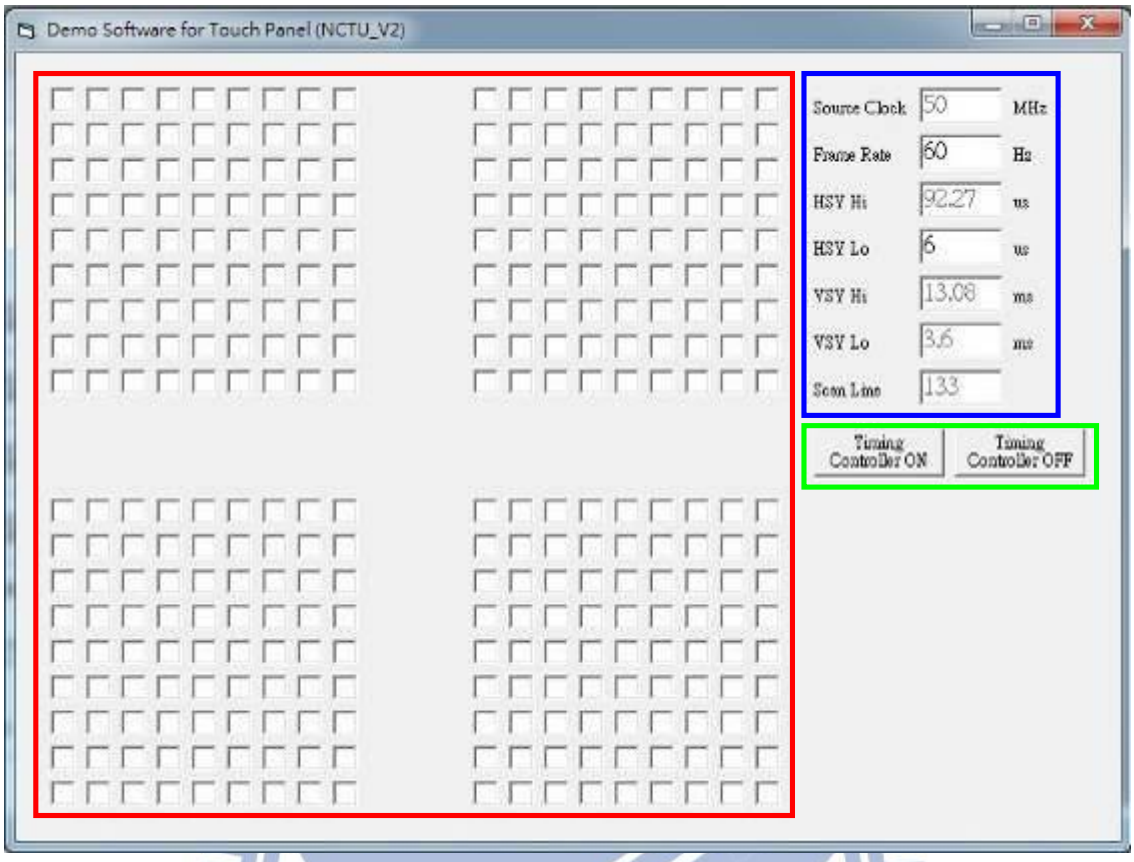


Fig. 3-1 Graphical User Interface

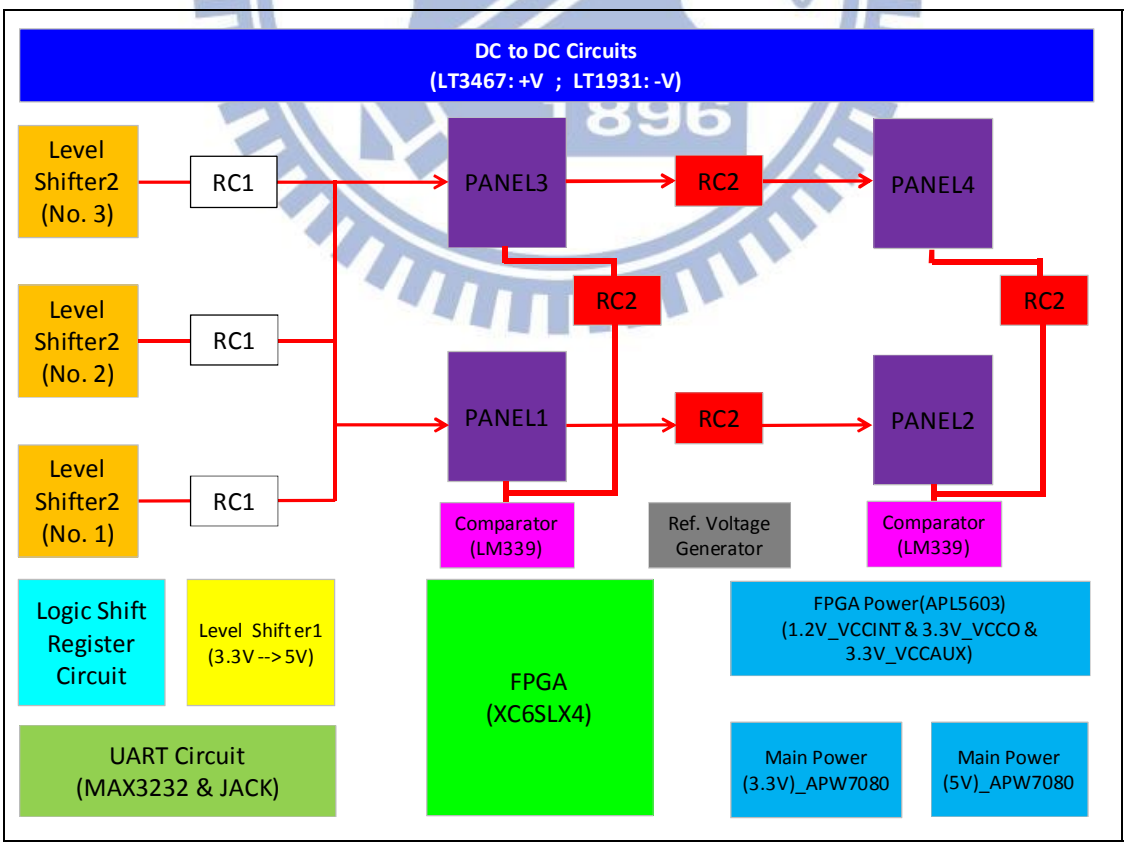


Fig. 3-2 Block diagrams for new system

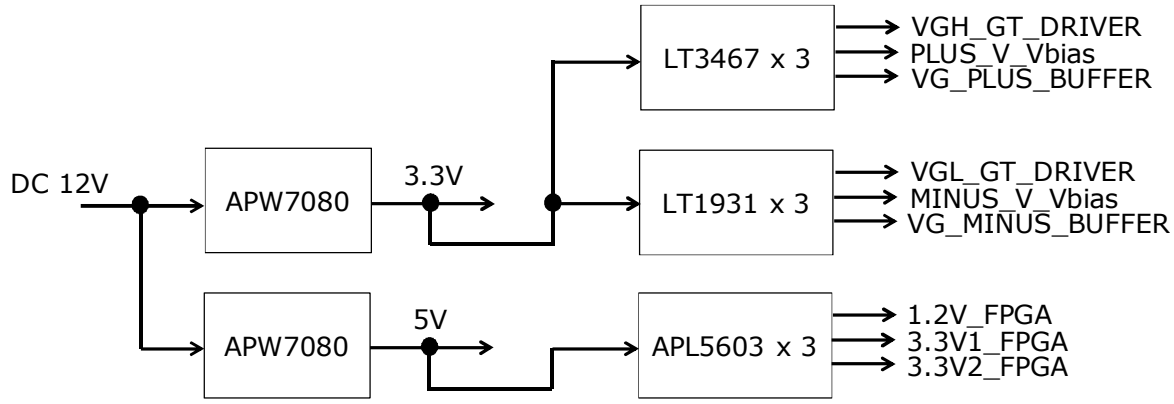


Fig. 3-3(a) Block diagram

APW7080 LT3467

LT1931 APL5603

Fig. 3-3(b) The real circuit

Fig. 3-3 Power circuit

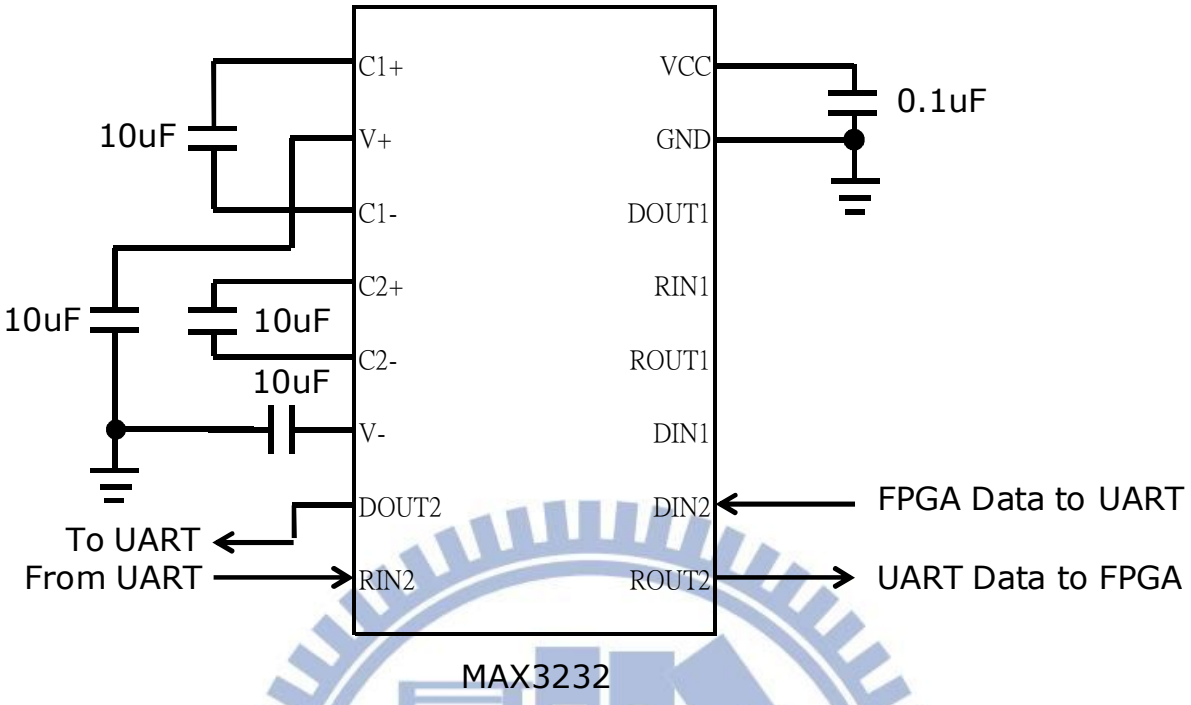


Fig. 3-4(a) Schematic

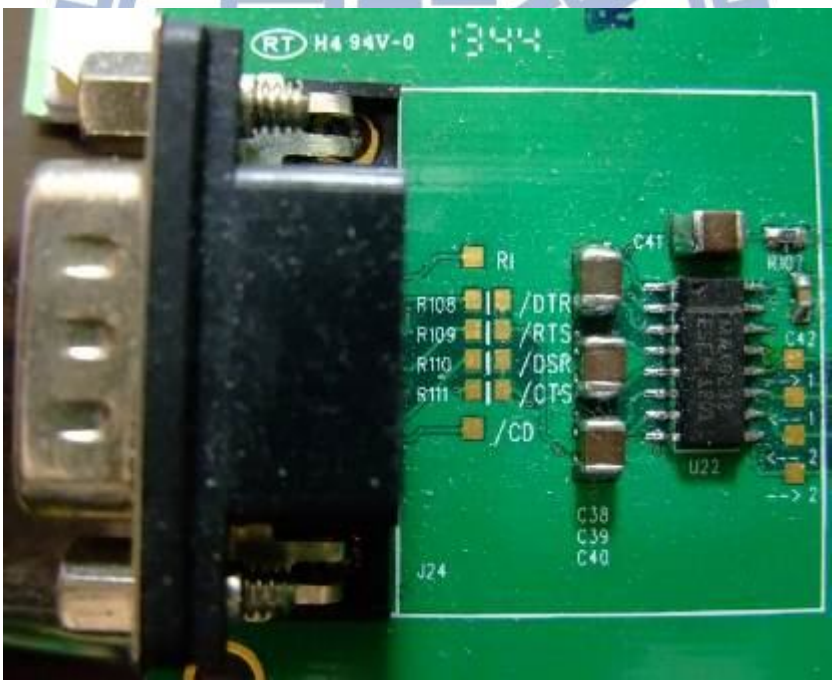


Fig. 3-4(b) The real circuit

Fig. 3-4 UART interface circuit

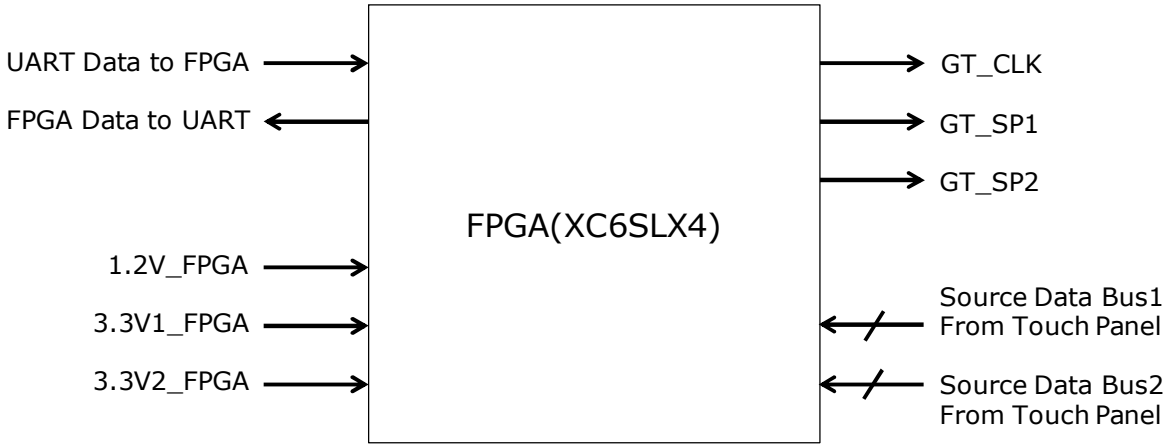


Fig. 3-5(a) Block diagram

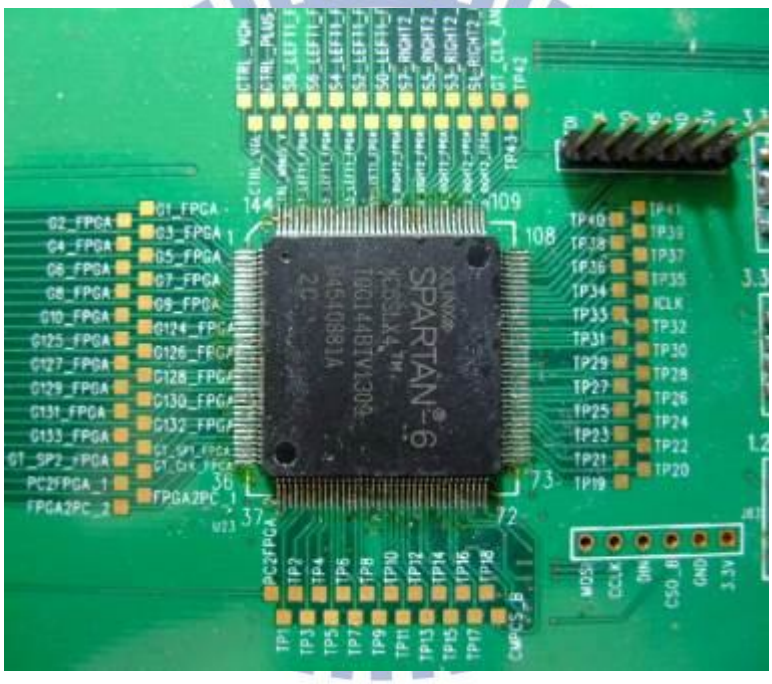
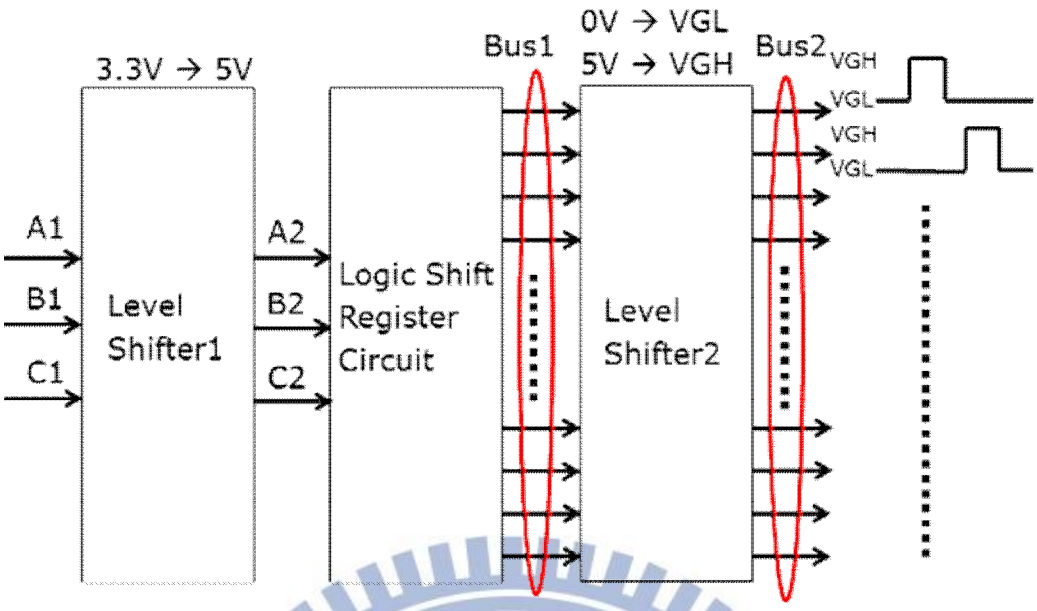


Fig. 3-5(b) The real circuit

Fig. 3-5 The core chip (FPGA)



A1: GT_CLK from FPGA
A2: GT_CLK to Logic Shift Register Circuit
B1: GT_SP1 from FPGA
B2: GT_SP1 to Logic Shift Register Circuit
C1: GT_SP2 from FPGA
C2: GT_SP2 to Logic Shift Register Circuit
Bus1: 5V control signals for gate line of touch panel
Bus2: Scan signals for gate line of touch panel

Fig. 3-6 Block diagrams for scan (gate) circuit

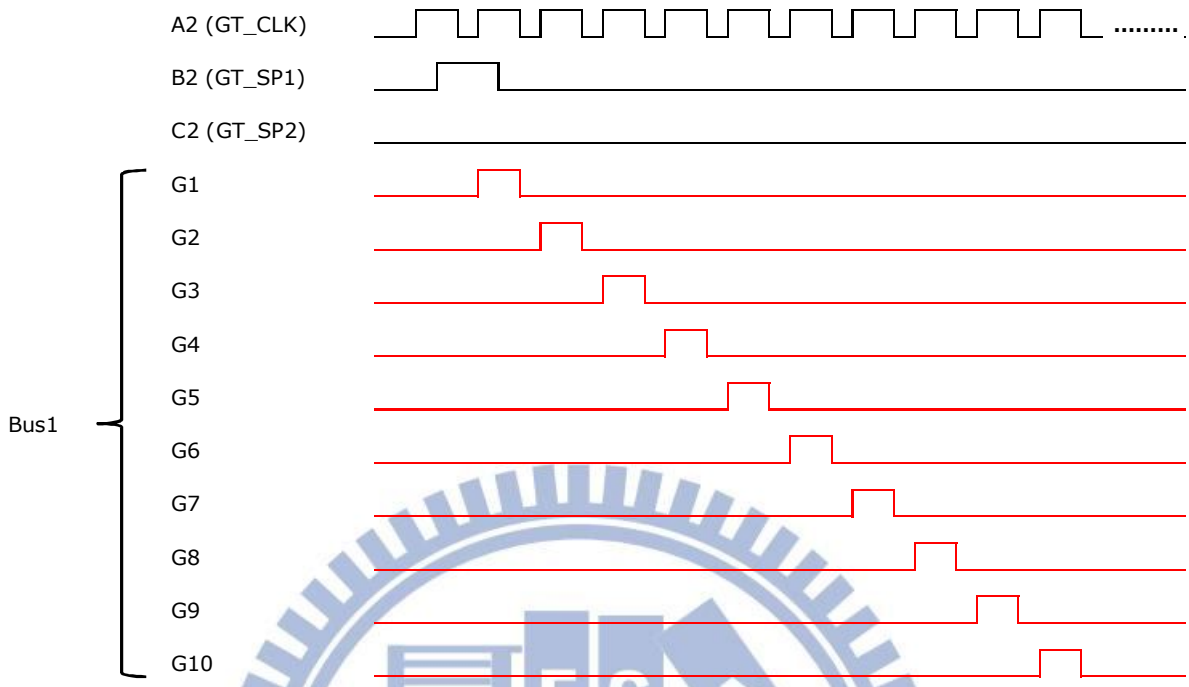


Fig. 3-7(a)

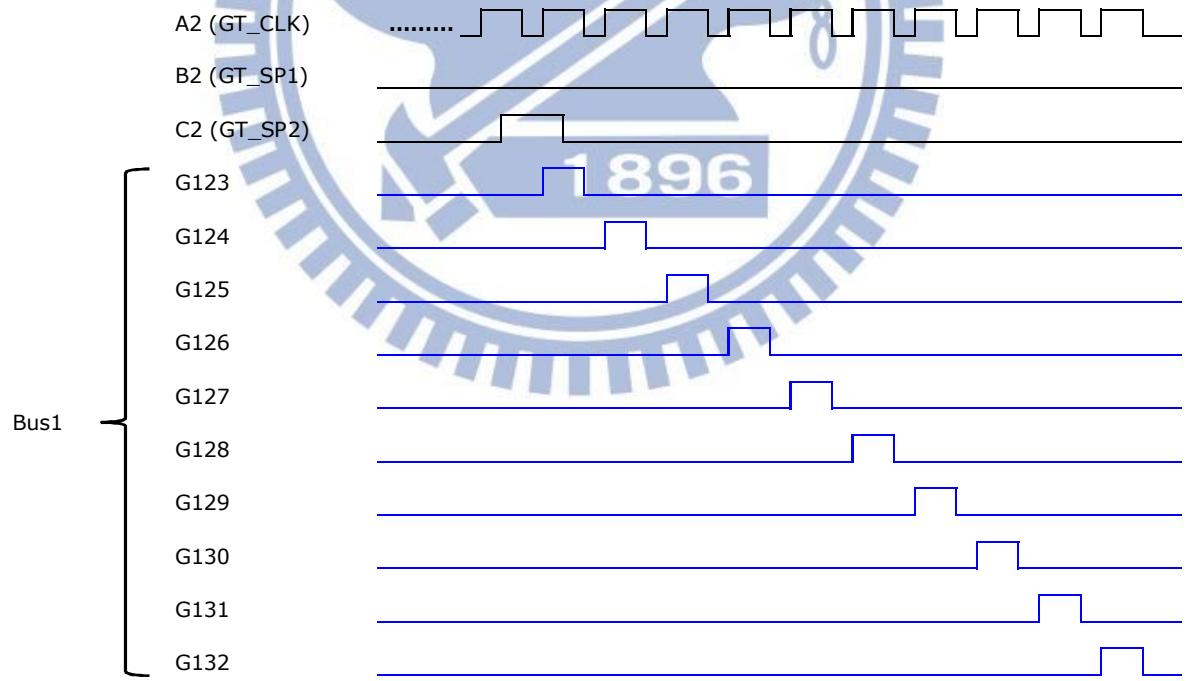


Fig. 3-7(b)

Fig. 3-7 Timing chart for scan (gate) circuit

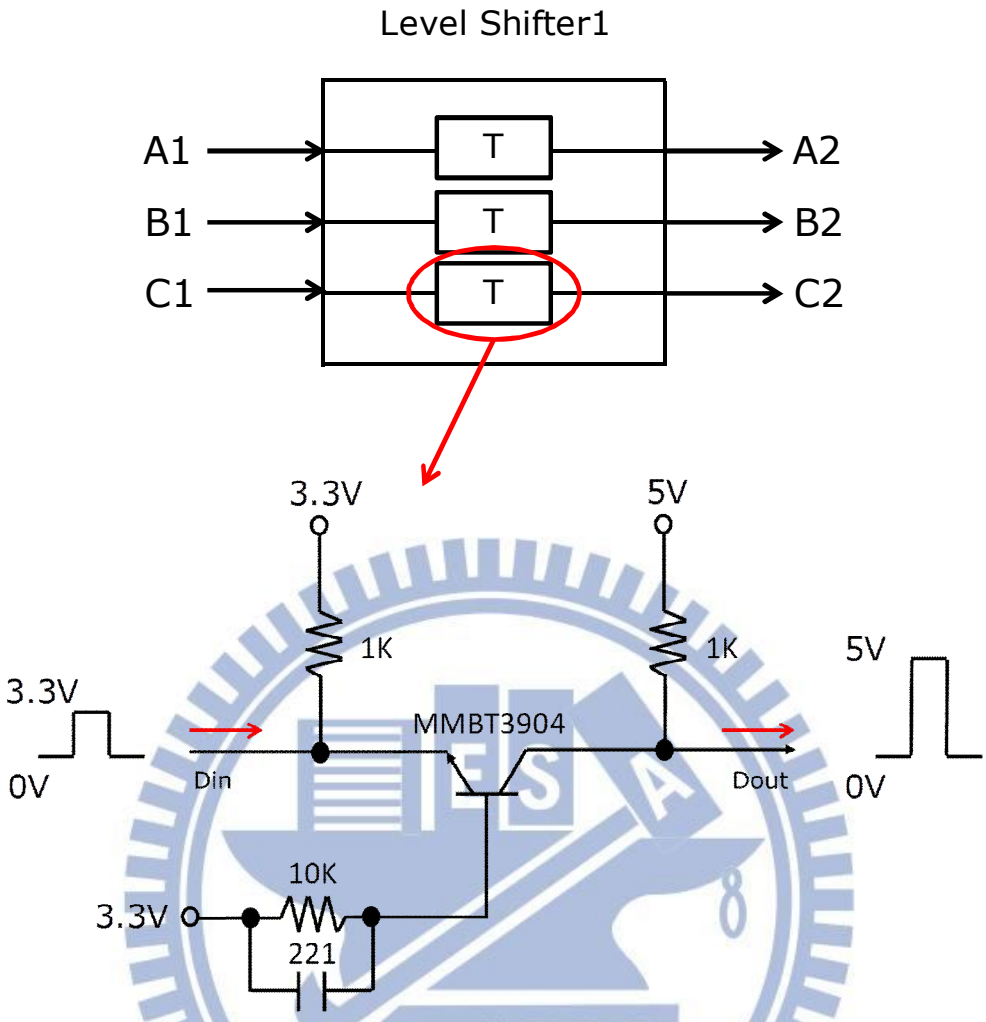


Fig. 3-8(a) Block diagram & schematic

Fig. 3-8(b) The real circuit

Fig. 3-8 Level shifter1 (FPGA signal to logic signal)

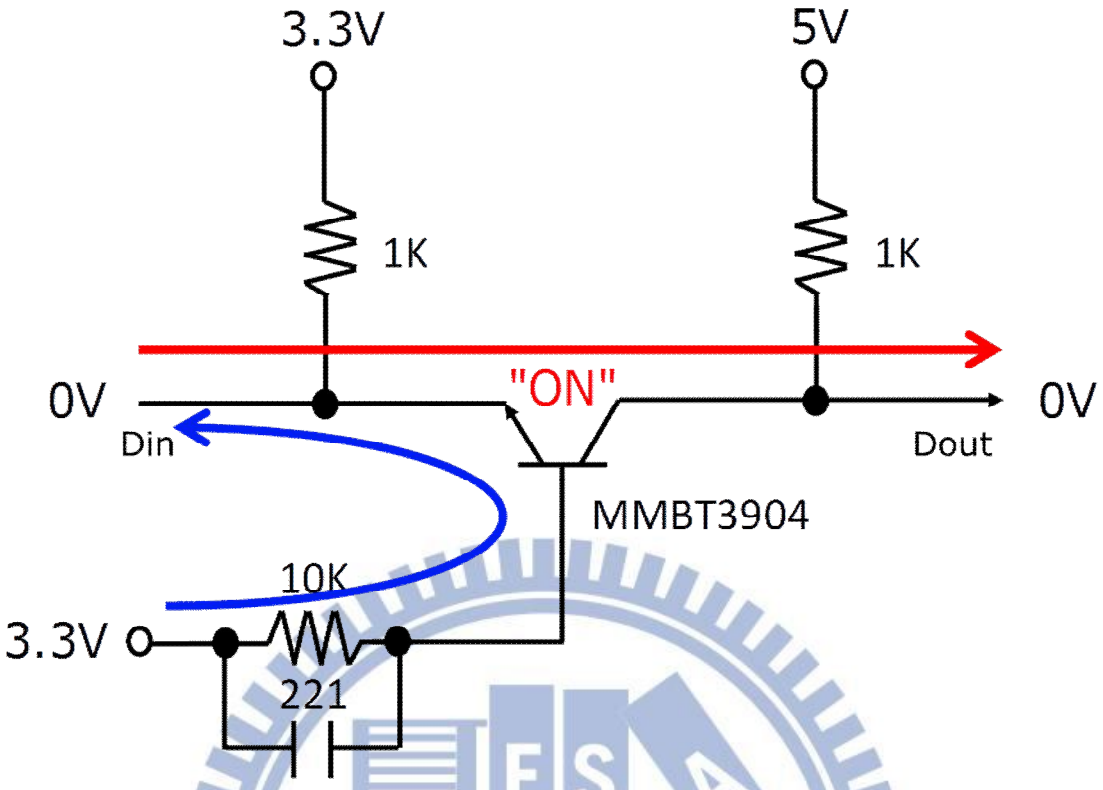


Fig. 3-9(a) ON state

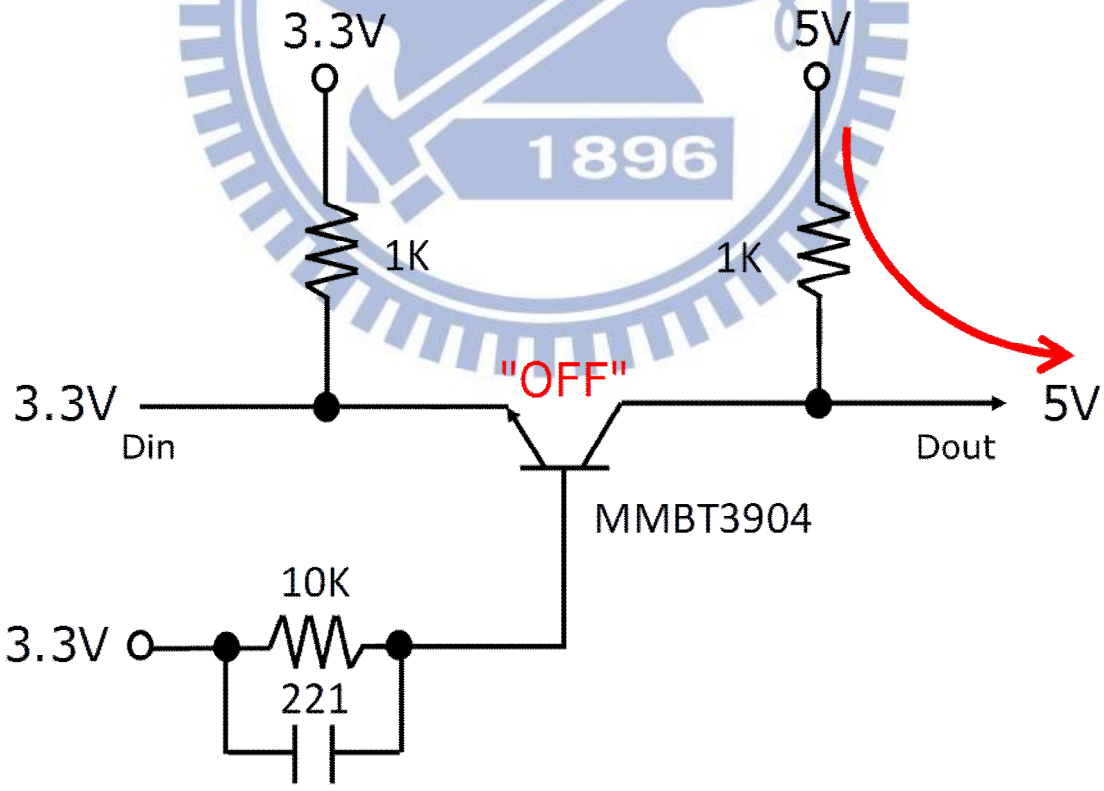


Fig. 3-9(b) OFF state

Fig. 3-9 The circuit of level shifter1

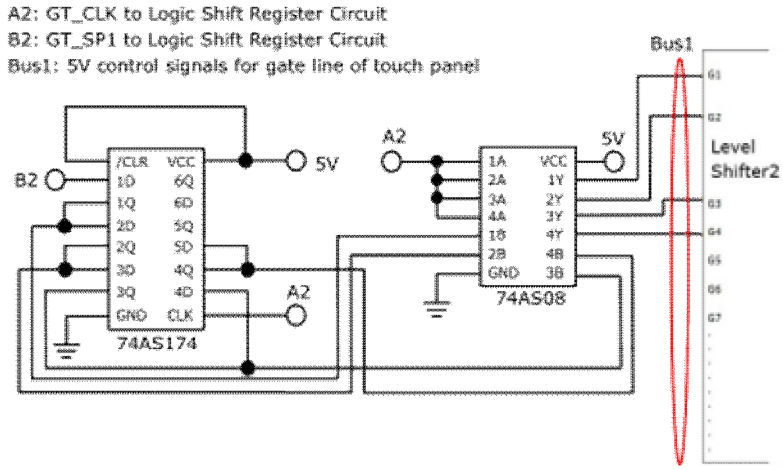


Fig. 3-10(a) The logic shift register circuit of upper side for scan circuit

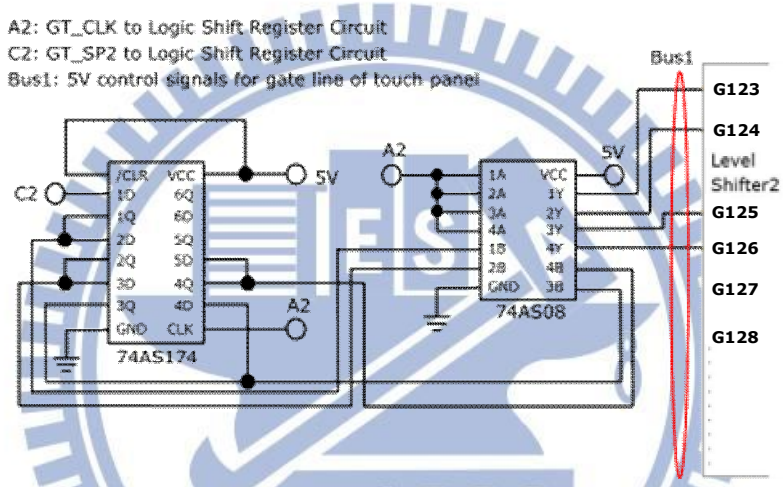


Fig. 3-10(b) The logic shift register circuit of lower side for scan circuit

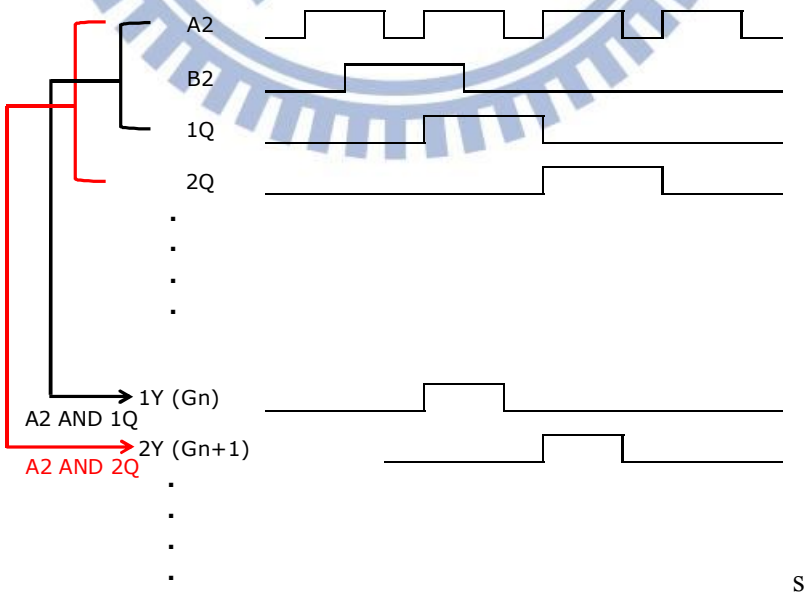


Fig. 3-10(c) Timing chart for logic shift register circuit

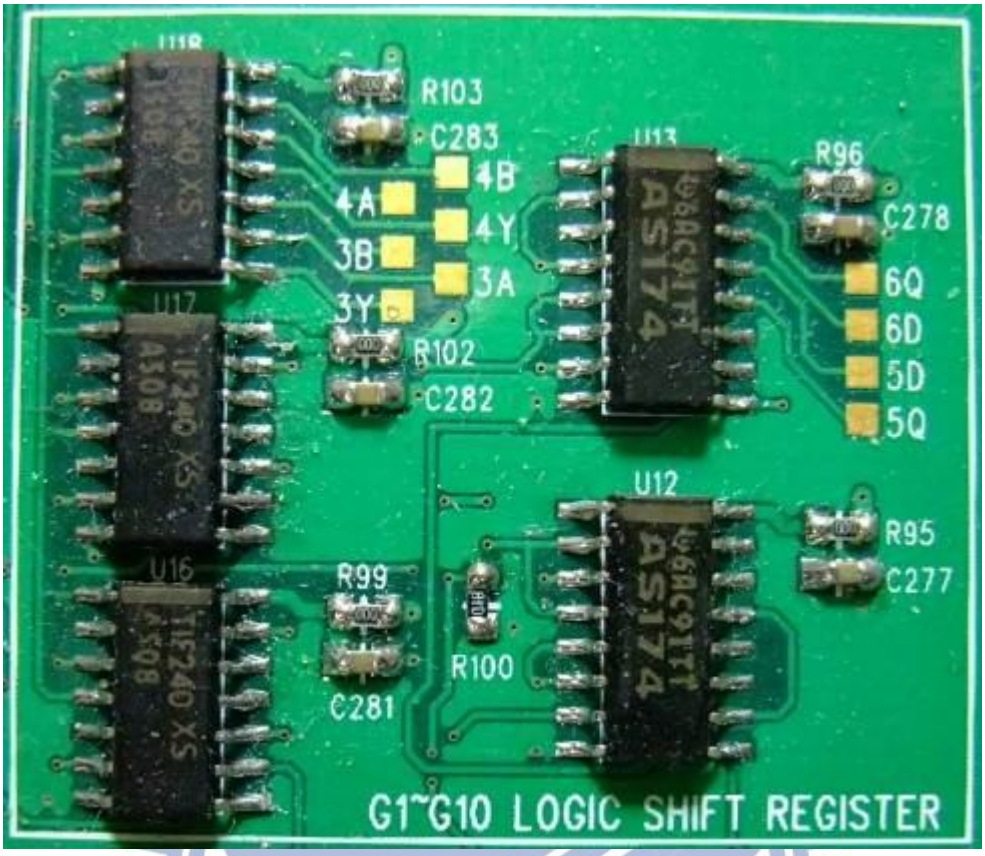


Fig. 3-10(d) The real circuit

Fig. 3-10 Logic shift register circuit

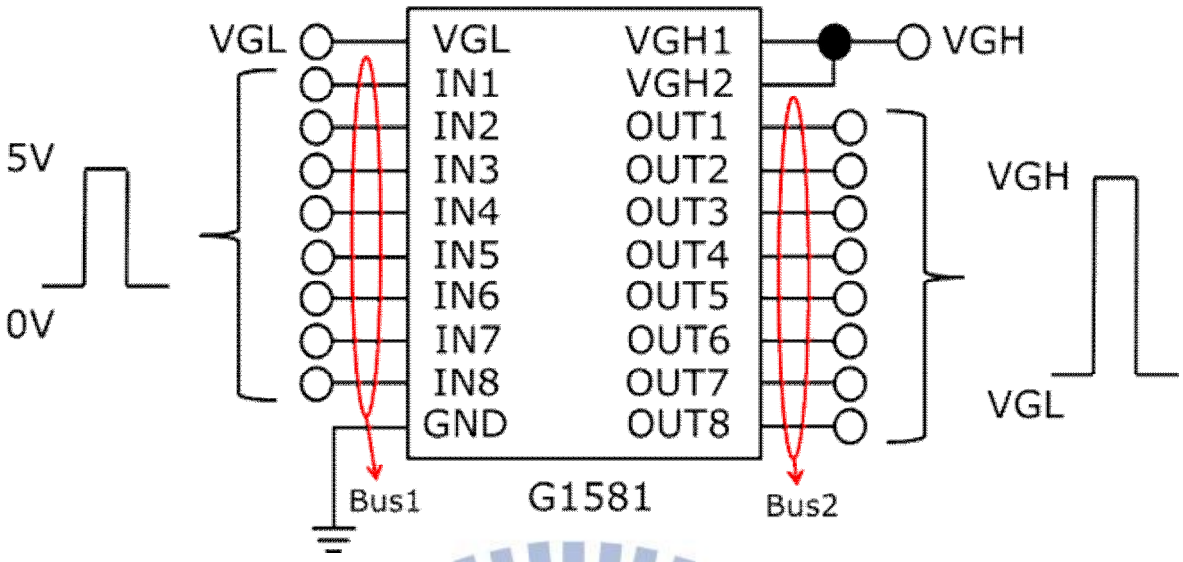


Fig. 3-11(a) Block diagram

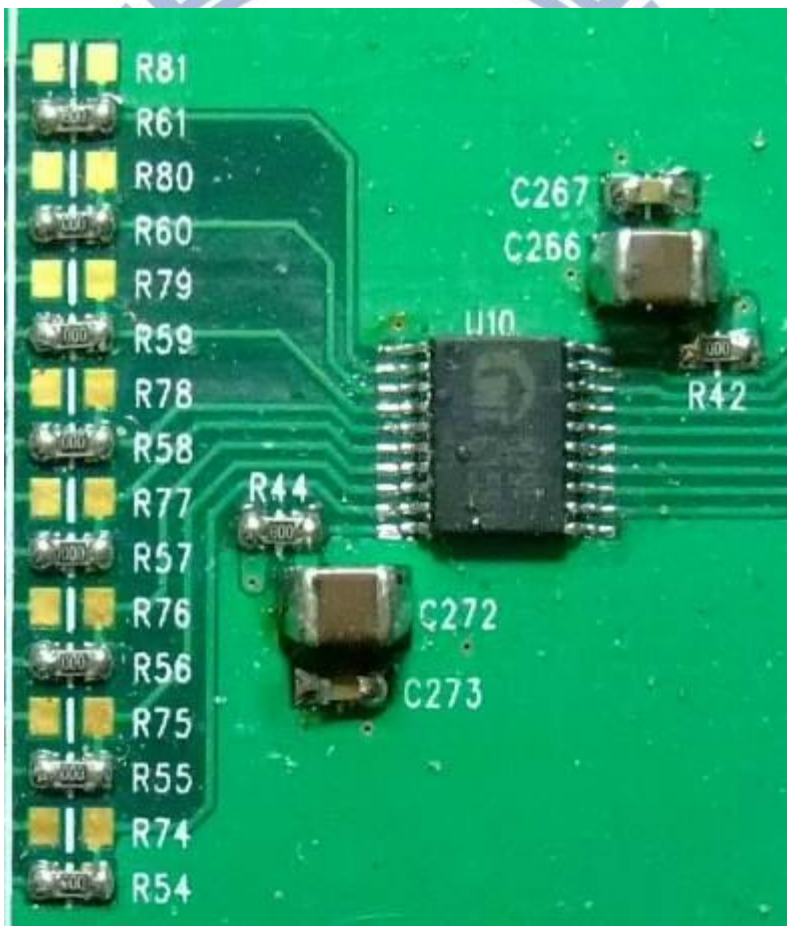


Fig. 3-11(b) The real circuit

Fig. 3-11 Level shifter2 (Logic signal to high voltage signal)

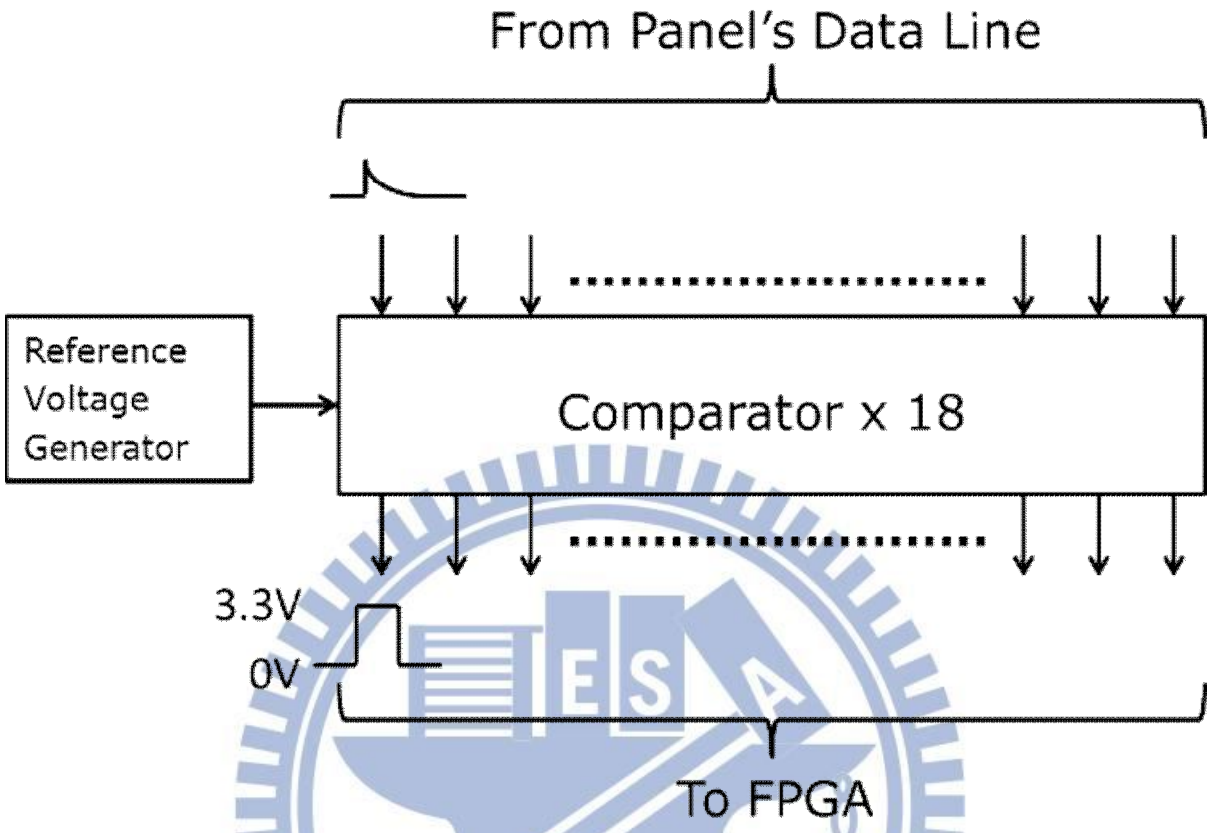


Fig. 3-12(a) Block diagram

Fig. 3-12(b) The real circuit

Fig. 3-12 Comparator (source) circuit

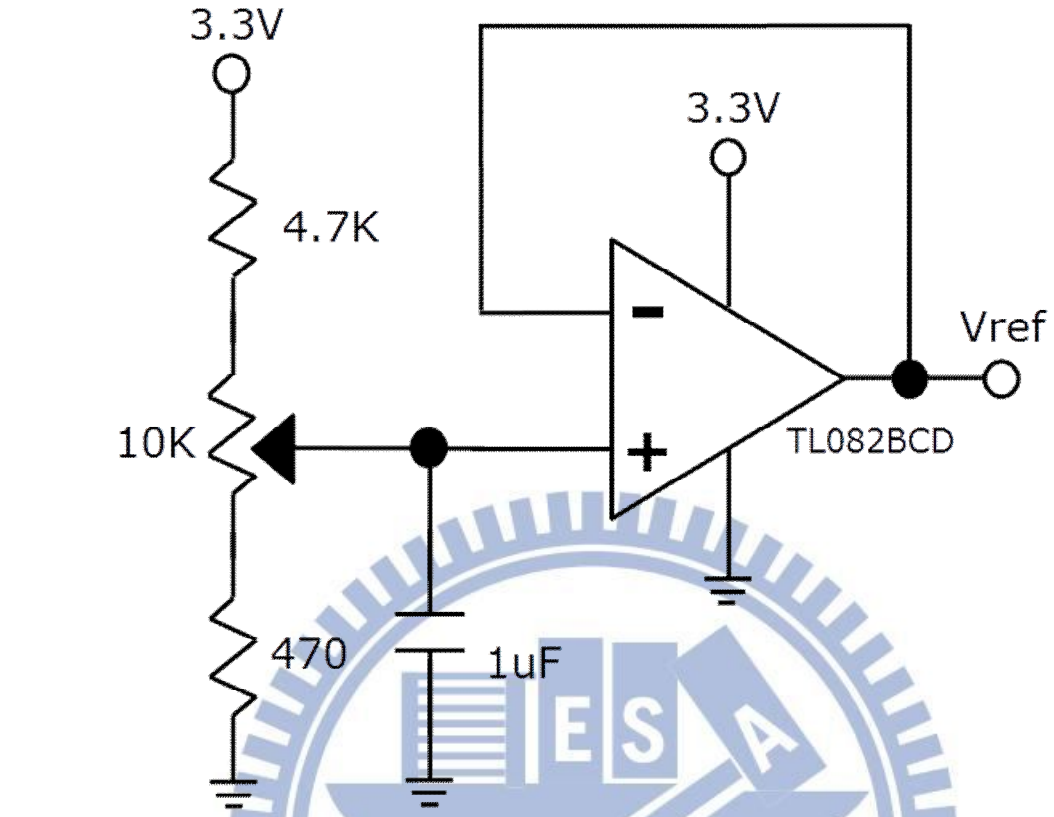


Fig. 3-13 Reference voltage (V_{ref}) circuit

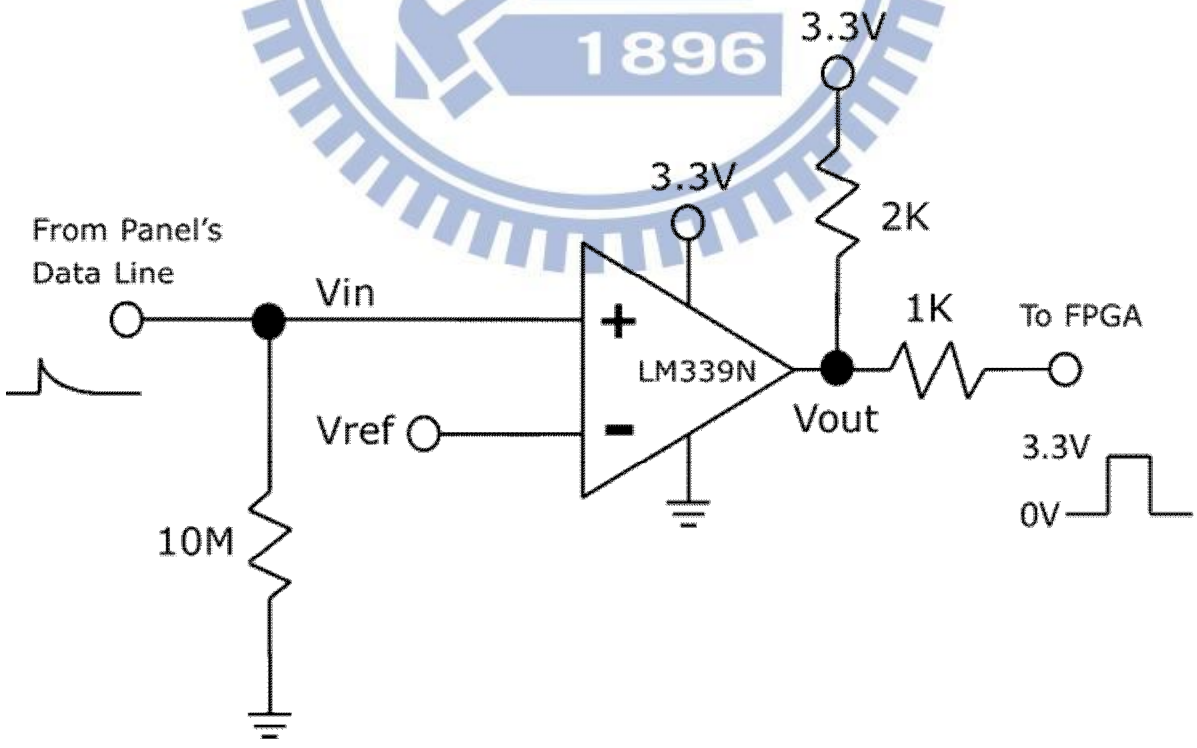


Fig. 3-14 Comparator circuit

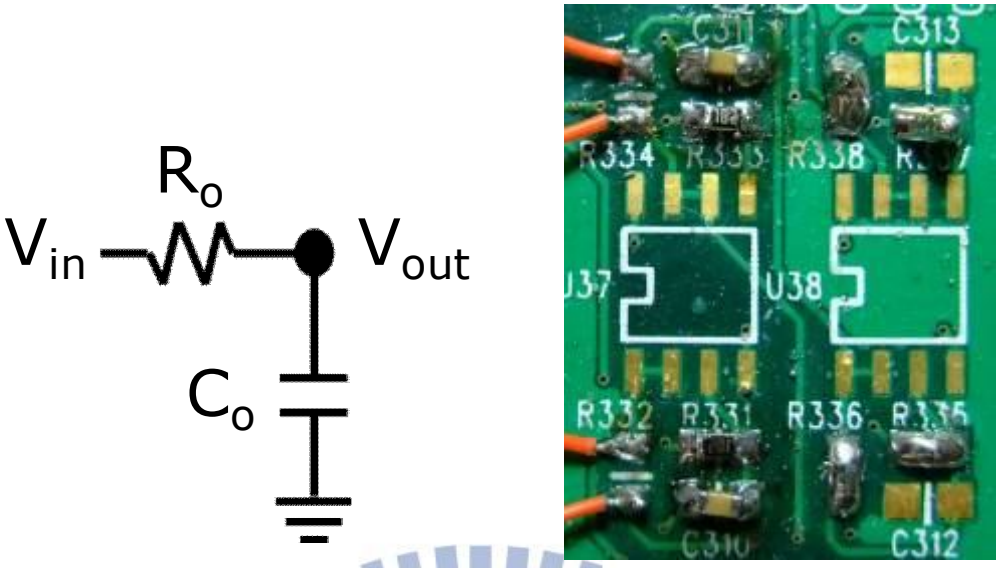


Fig. 3-15(a) First-order RC circuit & real circuit

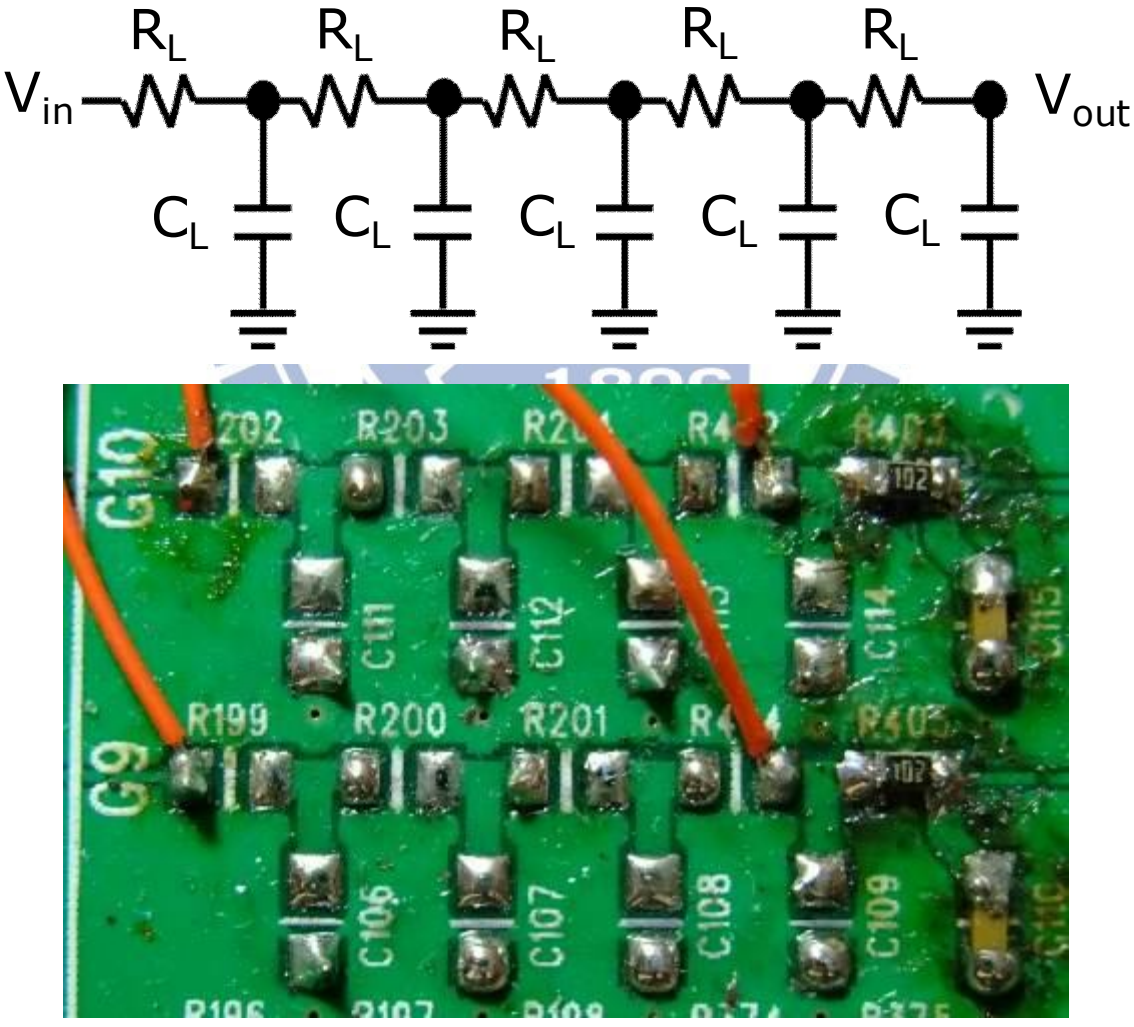


Fig. 3-15(b) Fifth-order RC circuit & real circuit

Fig. 3-15 RC circuit

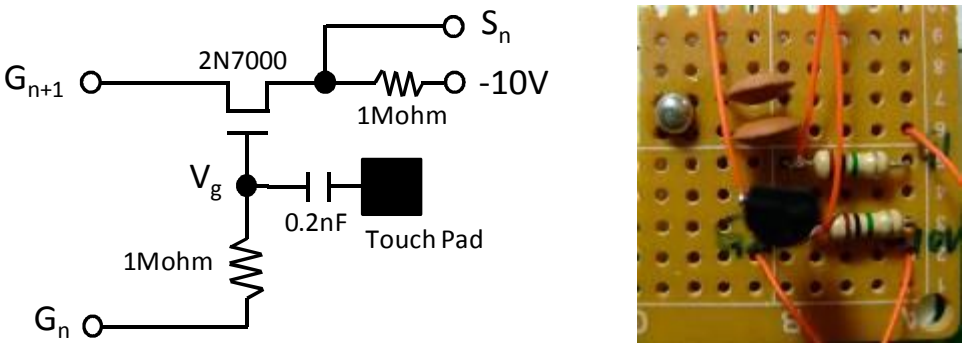


Fig. 3-16(a) Pixel circuit without delay circuit for scan line G_n and G_{n+1}

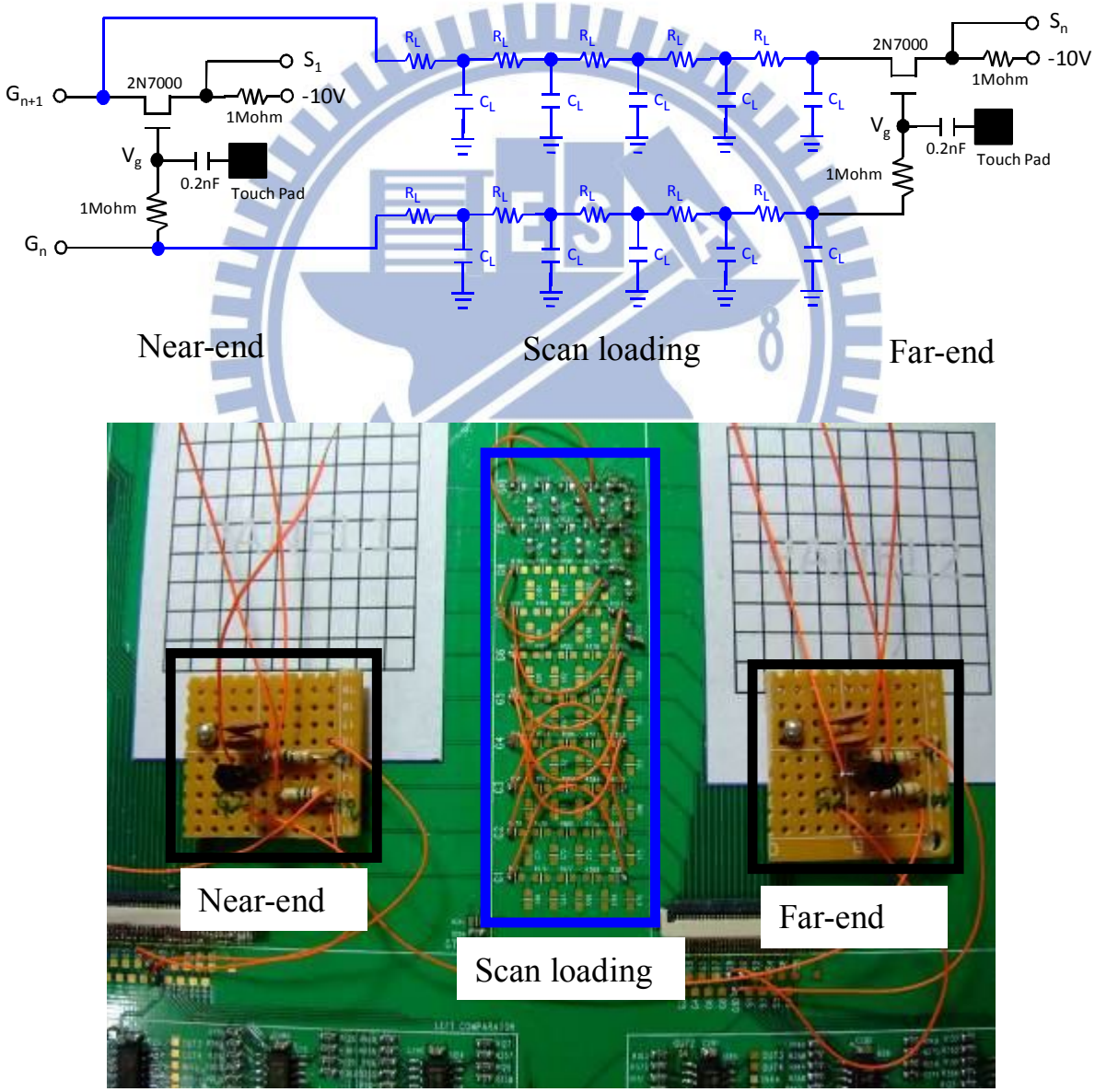
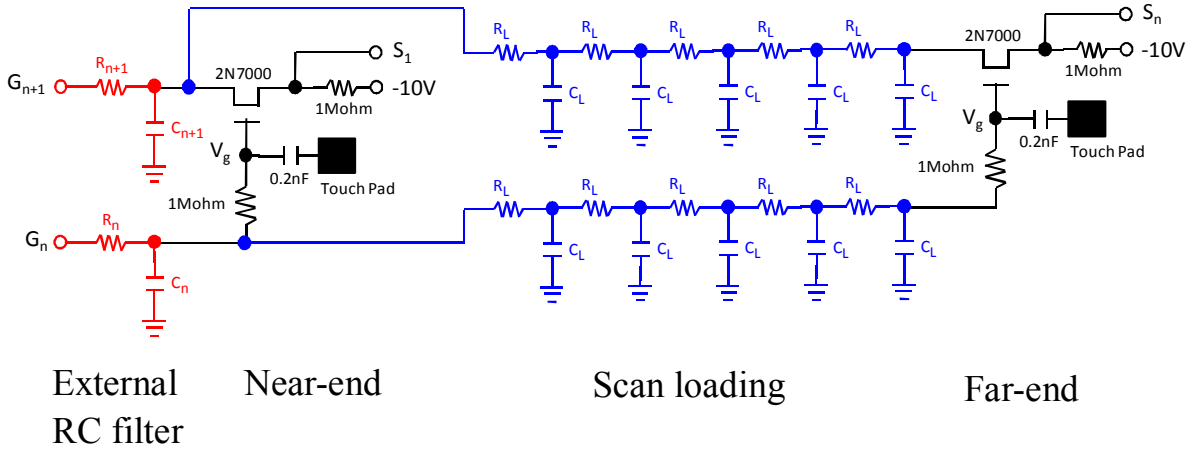


Fig. 3-16(b) Pixel circuit with delay circuit for scan line G_n and G_{n+1}



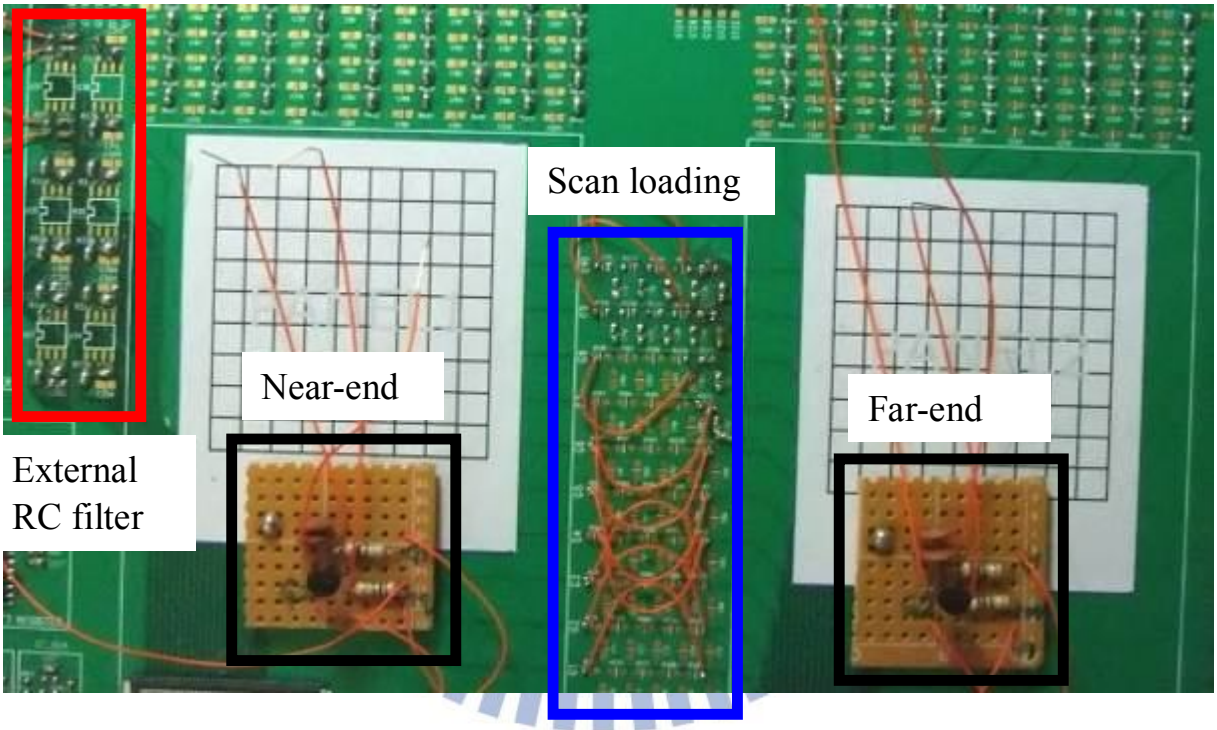


Fig. 3-16(c) Pixel circuit with delay circuit and external RC filter for scan line G_n and G_{n+1}

Fig. 3-16 The structure of pixel circuit for simulating touch panel

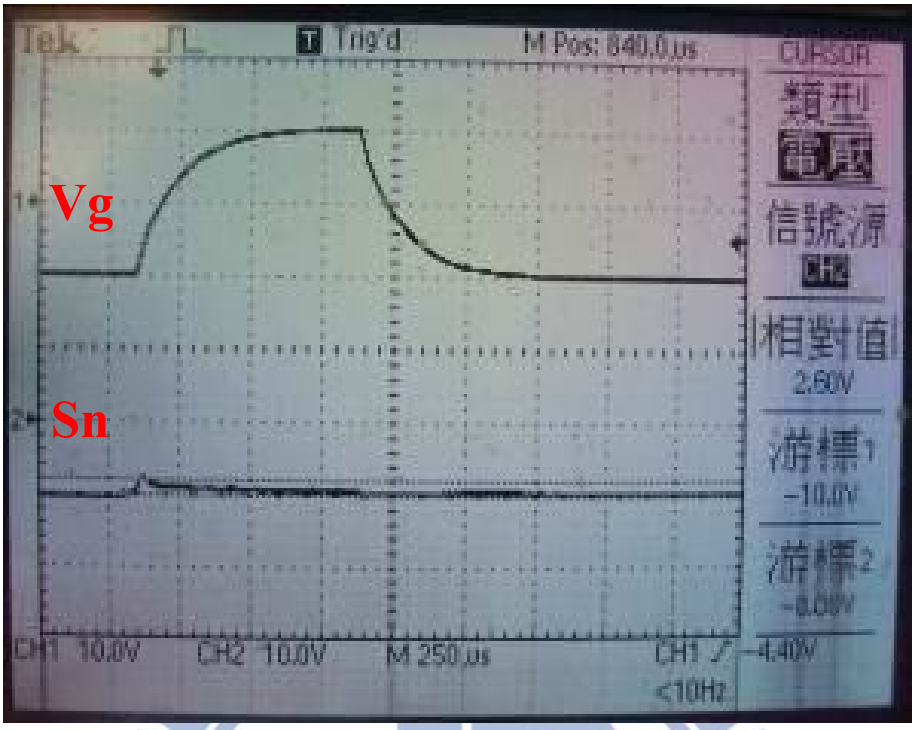


Fig. 3-17(a) τ_{delay} is 100us

Fig. 3-17(b) τ_{delay} is 300us

Fig. 3-17 The comparison of data line (S_n) with different τ_{delay} when far-end untouched and GT_OE is 600us

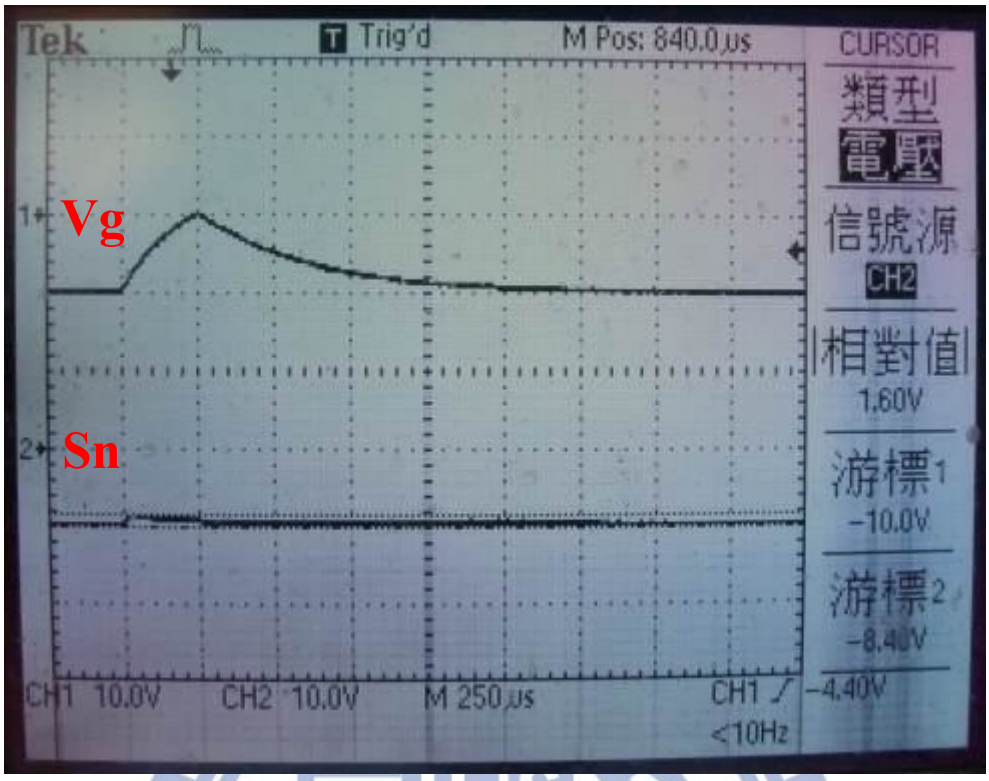


Fig. 3-18(a) When far-end untouched

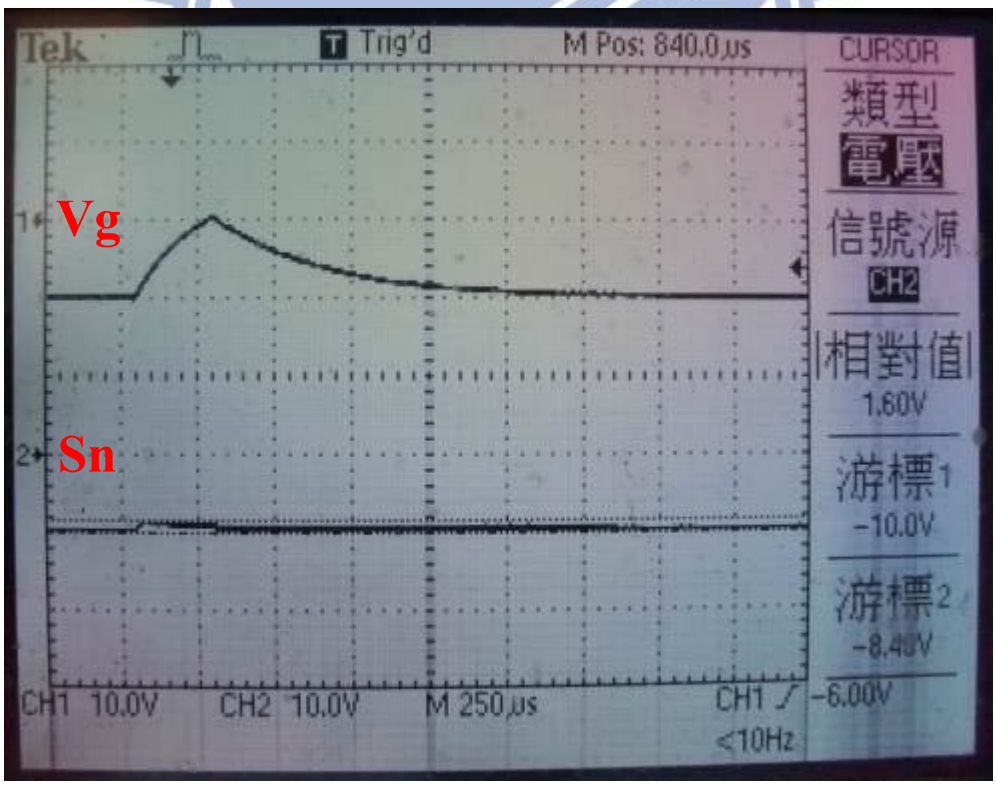


Fig. 3-18(b) When far-end touched

Fig. 3-18 The comparison of data line (S_n) when τ_{delay} is 300us and GT_OE is 1600us

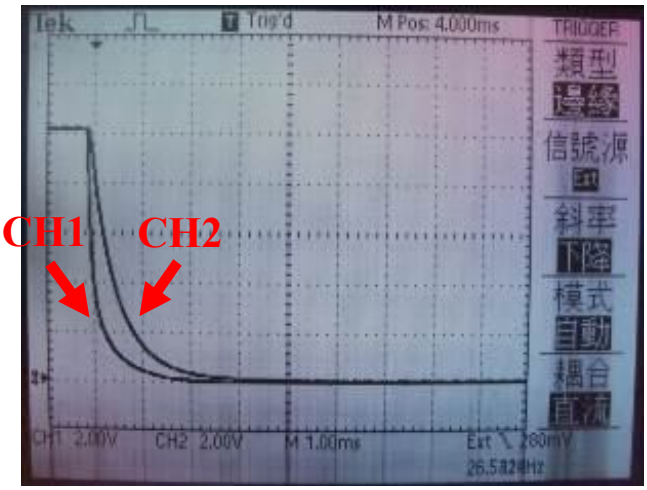


Fig. 3-19(a) $\tau_{external}$ is 150us

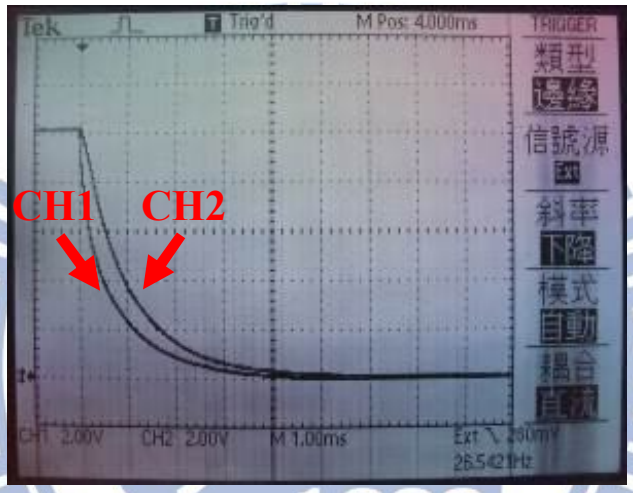


Fig. 3-19(b) $\tau_{external}$ is 300us

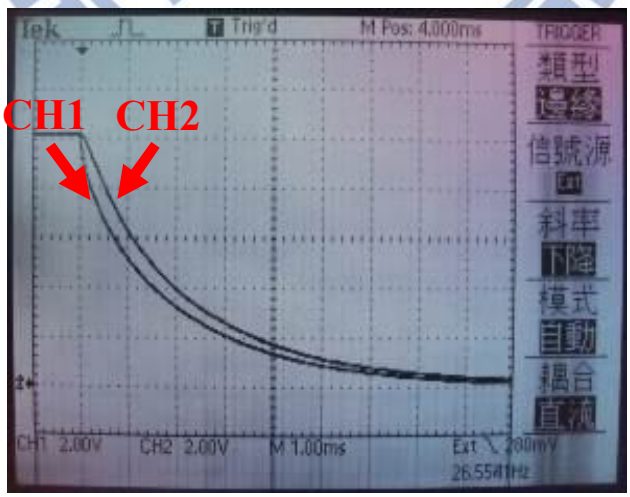


Fig. 3-19(c) $\tau_{external}$ is 620us

Fig. 3-19 The comparison of scan pulses with different $\tau_{external}$ at near-end and far-end

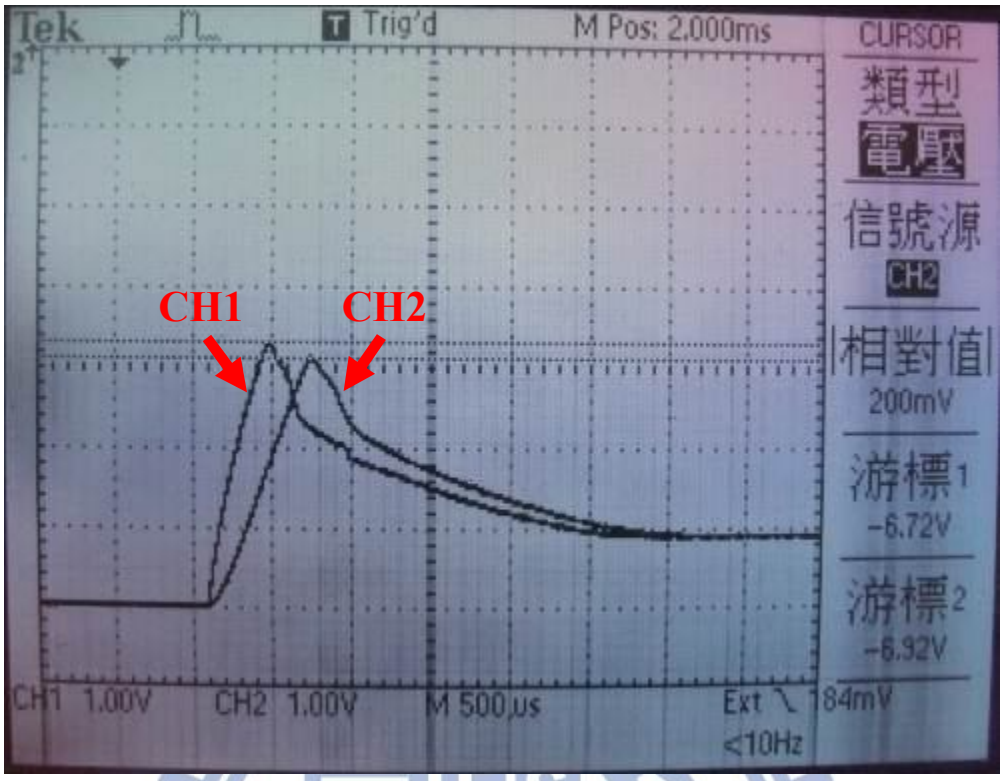


Fig. 3-20(a) The touch pads are untouched

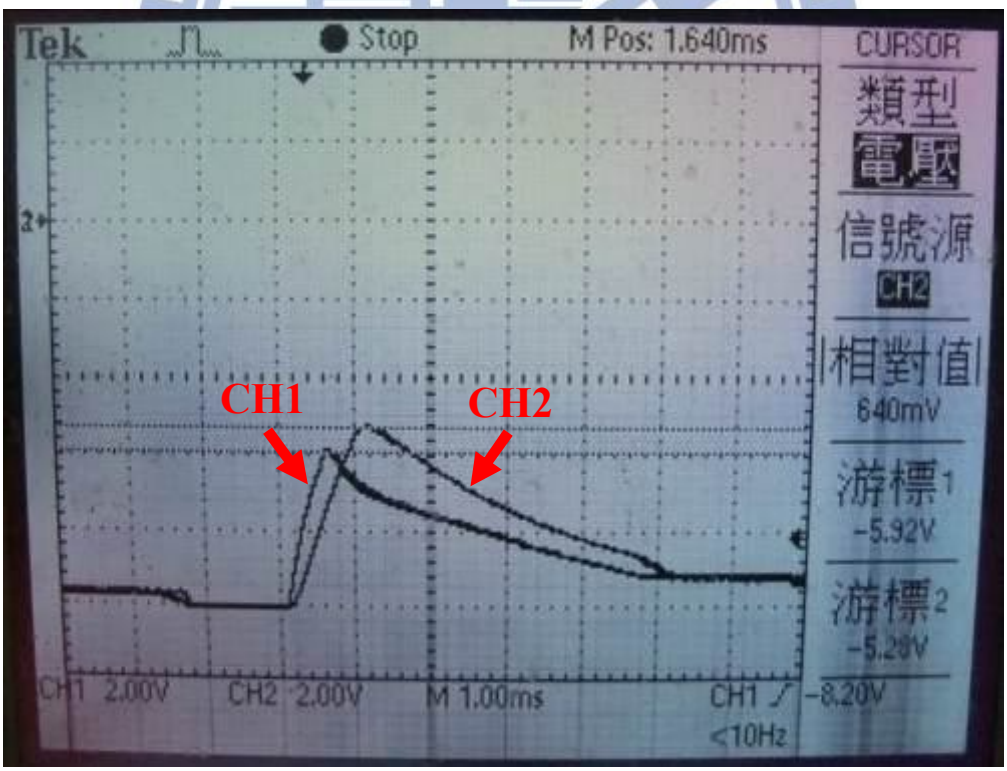


Fig. 3-20(b) The touch pads are touched

Fig. 3-20 The data line signals with τ_{delay} is 300us and $\tau_{external}$ is 150us for near-end (CH1) and far-end (CH2)

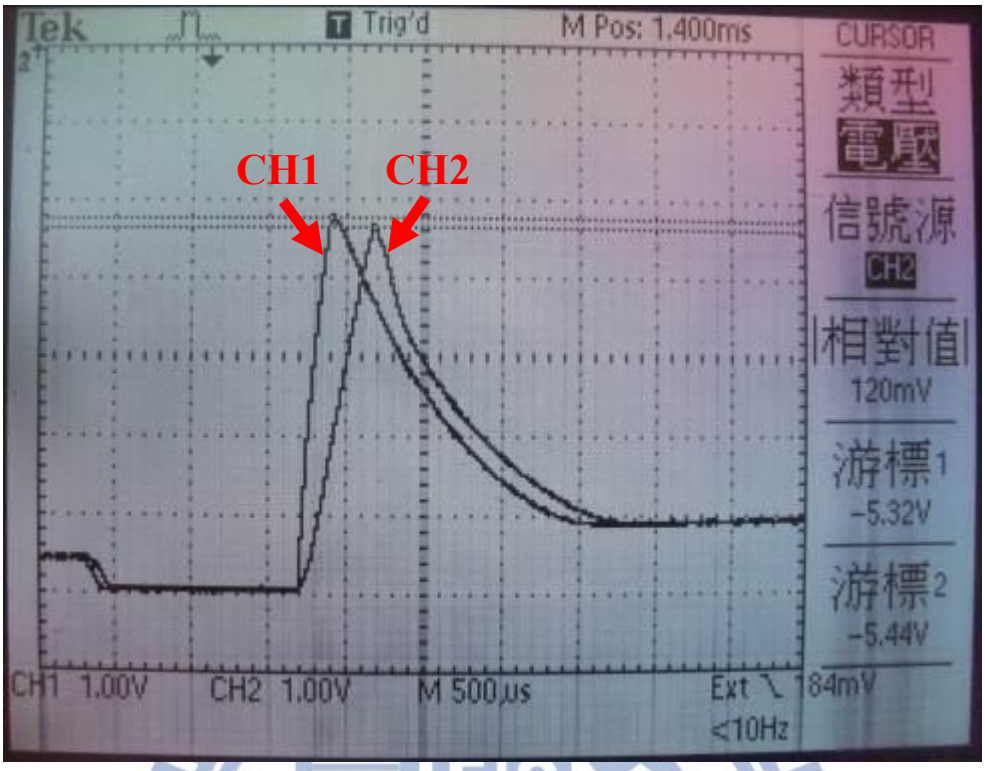


Fig. 3-21(a) The touch pads are untouched

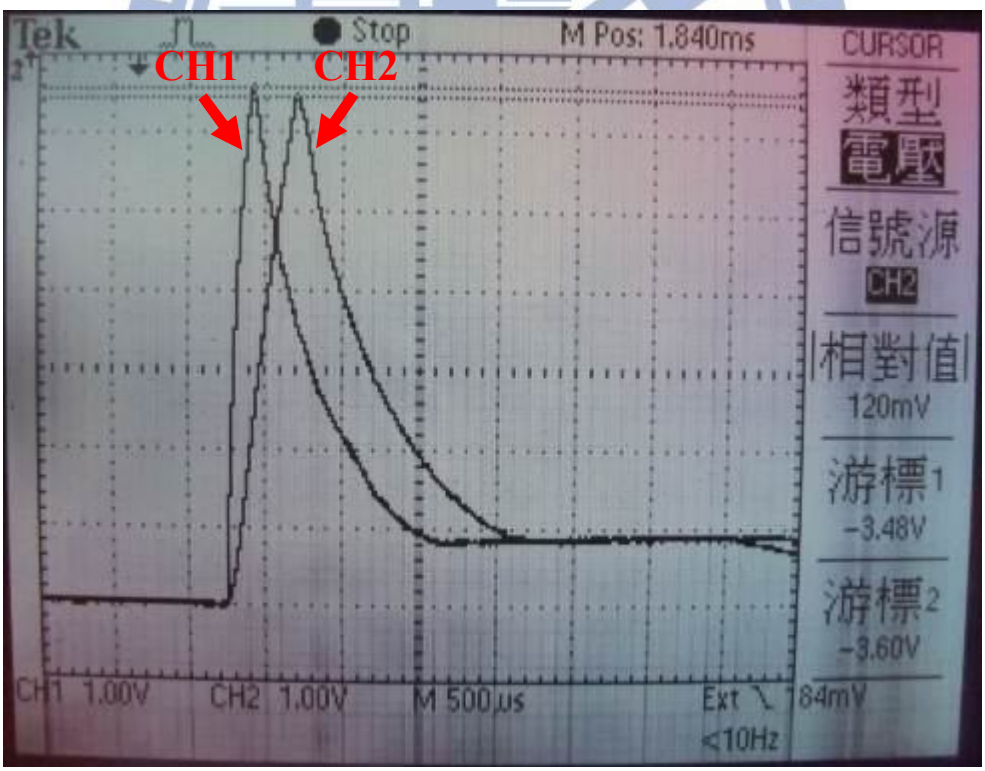


Fig. 3-21(b) The touch pads are touched

Fig. 3-21 The data line signals with τ_{delay} is 300us and $\tau_{external}$ is 300us for near-end (CH1) and far-end (CH2)

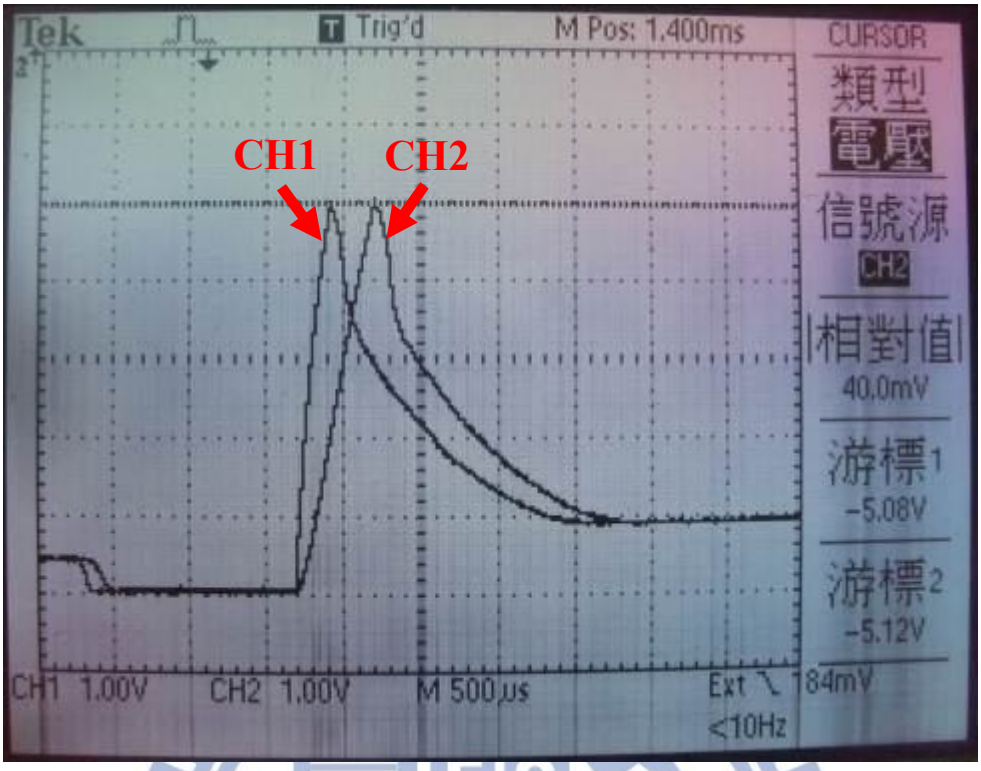


Fig. 3-22(a) The touch pads are untouched

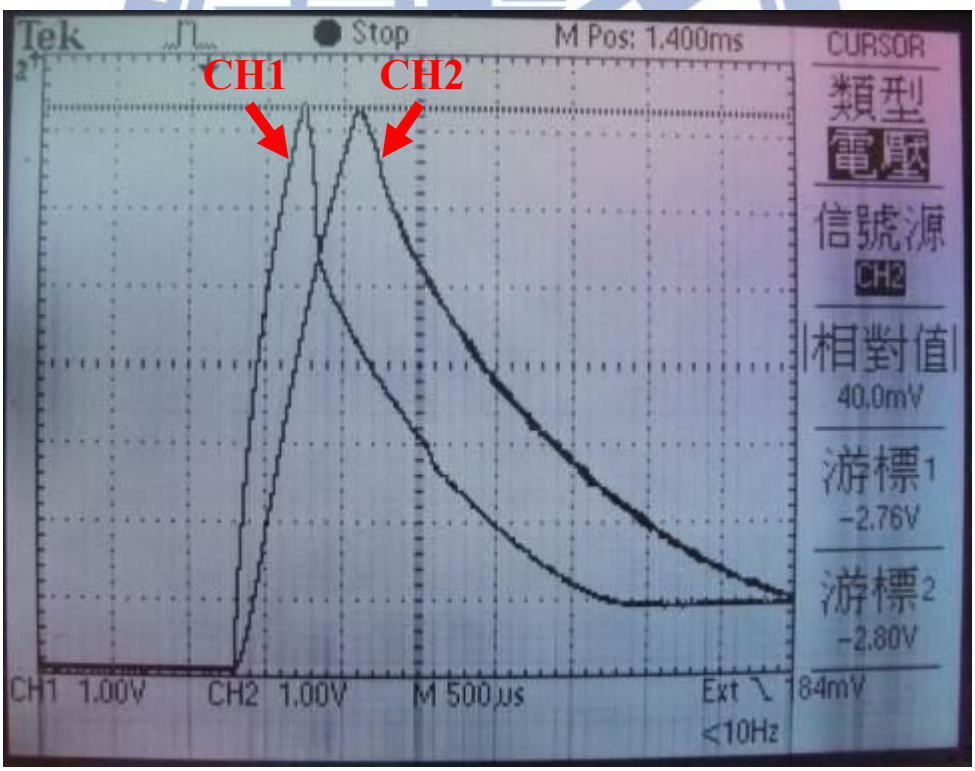


Fig. 3-22(b) The touch pads are touched

Fig. 3-22 The data line signals with τ_{delay} is 300us and $\tau_{external}$ is 620us for near-end (CH1) and far-end (CH2)

Chapter 4 Conclusions

In this thesis, the original concept of the active touch circuit that senses the change in the RC delay to detect the touch event is reviewed for the application in large panels. In such application, the increased touch panel leads to the intrinsic RC delay on the signal buses and thus might cause the mal-operation for the pixels in the far-end. By both simulation and implementation, we verified the newly proposed method to solve the issue. The harmonic components in high frequencies of scan pulse are filtered before being fed to the scan bus. Therefore, the far-end of the touch panel can be driven by the approximately same waveform as the near-end. The criteria of designing the loading of scan line is to make sure $\tau_{untouched} < \tau_{delay} < \tau_{touched}$. With this design rule, the voltage levels of output signals on the data lines in the touched or untouched cases can be accurately simulated. By setting the reference voltage of comparators between these two voltage levels, the large size active touch panel can be successfully designed and implemented.

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