

# Pulse-*IV* Characterization of Charge-Transient Behavior of SONOS-Type Devices With or Without a Thin Tunnel Oxide

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**Abstract**—The transient behavior of SONOS-type devices was investigated for the first time using pulse-*IV* technique. Three kinds of SONOS devices are studied: SONS (without top oxide), SONoS (with a thin top oxide), and SoNOS (with a thin bottom oxide). Devices with or without a thin tunnel oxide were able to provide very fast charge injection/detrapping, but their charge-transient behavior cannot be accurately monitored by conventional DC-*IV* method. By using specific pulse-*IV* setup for memory, we can measure the drain current response immediately after programming and erasing, as well as the fast charge relaxation under various reliability tests. The program and erase transient behavior shows that all devices are easily programmed and erased within 1  $\mu$ s at low gate voltages ( $< 6$  V). Moreover, SONS shows the fastest program and erase speeds because of the absence of tunnel oxide, and silicon nitride has very low barrier height that offers fast injection. We have also examined the charge relaxation under various field and temperature conditions and found that the charge loss mainly came from external charge injection during retention, not from detrapping through thermionic emission.

**Index Terms**—Gate injection, pulse-*IV* method, SONOS, SONS, transient behavior.

## I. INTRODUCTION

CHARGE-TRAPPING devices have gained great attention in non-volatile memory applications [1]. However, it is hard to monitor the “real” trapped charge behavior using conventional DC-*IV* measurement, particularly for the memory with serious hysteresis. Recently, pulse-*IV* techniques have been developed to characterize traps in high-*k* gate dielectrics of CMOS logic devices [2]–[5]. However, few studies talked about the applications on SONOS-type memory. In this letter, we utilize a specific pulse-*IV* setup for memory to investigate the instant charge transient behavior of SONOS-type devices.

Manuscript received December 2, 2008. First published February 6, 2009; current version published March 25, 2009. The review of this letter was arranged by Editor X. Zhou.

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Digital Object Identifier 10.1109/LED.2009.2012730

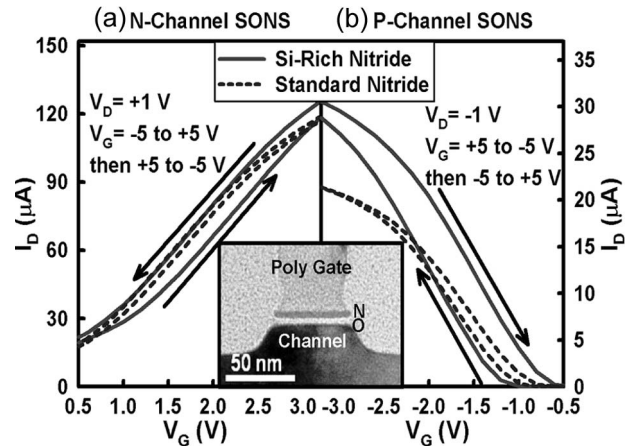


Fig. 1. Comparison of dual-sweep DC-*IV* characteristics of SONS with standard and silicon-rich nitride trapping layers. (a) N-channel devices. (b) P-channel devices. Gate voltage sweeps from  $-5$  to  $+5$  V and then  $+5$  to  $-5$  V for n-channel, and it sweeps reversely for p-channel. The hysteresis direction is also indicated. The inset is the typical cross-sectional view of SONS device.

We intentionally designed SONOS-type devices with or without a thin tunnel oxide to enhance the transient signal. In addition, silicon-rich nitride is used to provide even higher trap density.

## II. SAMPLE DESCRIPTIONS

Three kinds of SONOS devices are prepared:

- 1) “SONS:” SONOS without top oxide, where O/N = 30/50 Å;
- 2) “SONoS:” SONOS with a thin top oxide, where O/N/o = 30/50/8 Å;
- 3) “SoNOS:” SONOS with a thin bottom oxide, where o/N/O = 13/50/43 Å.

In addition to the conventional stoichiometric nitride, we have also prepared silicon-rich nitride samples that greatly enlarge the memory window. The channel length and width measured in our devices are nominally about 50 nm and 0.15  $\mu$ m, respectively (see inset of Fig. 1).

The SONS and SONoS are designed for the gate-injection operation [6], where tunneling mainly happens through the top dielectric instead of the bottom oxide. This avoids the stressing of gate oxide during programming and erasing of the device and, therefore, higher endurance [6].

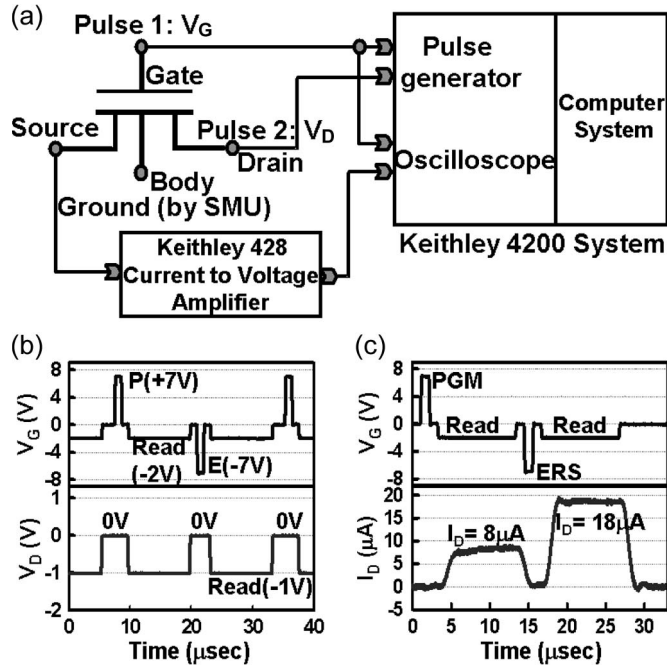


Fig. 2. (a) Pulse-IV setup. Pulses are applied to the gate and drain, while source is connected to a high-speed current-to-voltage amplifier.  $V_G$  and  $I_D$  signals are collected to the oscilloscope. (b) Designed gate and drain voltage pulses during P/E cycling test. Reading is performed immediately after programming and erasing. A  $-1$  V drain voltage pulse is applied during reading phase. (c) Typical measured drain current response during a P/E test. Large current difference ( $\sim 10 \mu\text{A}$ ) is obtained after programming/erasing.

### III. RESULTS AND DISCUSSIONS

#### A. DC-IV Characteristics

The conventional DC-IV measurements are carried out by dual-voltage sweeps. The results in Fig. 1 show that all devices have very significant hysteresis. This indicates that the devices are easily programmed/erased under low voltages. Moreover, silicon-rich nitride shows much larger hysteresis than the standard nitride. This suggests that silicon-rich nitride is more efficient in trapping charges at low voltage [7]. Furthermore, p-channel device shows slightly larger memory window than n-channel device. Therefore, we focus on p-channel devices in this letter.

The large hysteresis also suggests that the conventional DC-IV measurement to define threshold voltage [8] is not appropriate since these devices are easily disturbed during DC measurements. As we shall see later, pulse-IV is needed to accurately characterize these devices.

#### B. Pulse-IV Characteristics

The pulse-IV setup is shown in Fig. 2(a). The pulses are applied to the gate ( $V_G$ ) and drain ( $V_D$ ), while current is measured at the source. The source current, which is almost equal to drain current ( $I_D$ ), is converted to a voltage signal by using a fast current-to-voltage amplifier. Arbitrary waveforms can be generated to design any specific program/erase/read sequence. The oscilloscope can simultaneously collect  $V_G$  and  $I_D$ . Fig. 2(b) shows the  $V_G$  and  $V_D$  pulses during P/E cycling stressing. We measure  $I_D$  immediately (within  $1 \mu\text{s}$ ) after pro-

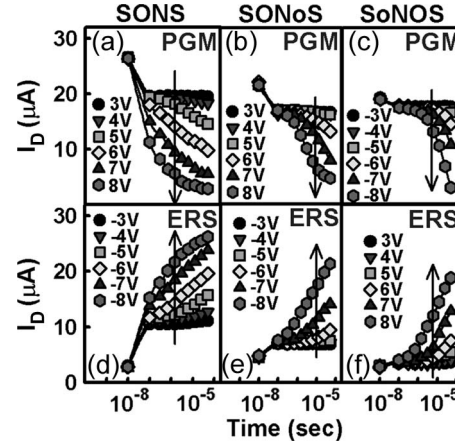


Fig. 3. Program and erase transient behavior of [(a) and (d)] SONS, [(b) and (e)] SONoS, and [(c) and (f)] SoNOS p-channel devices. All the devices use silicon-rich nitride. The programming injects holes and decreases the drain current; the erasing injects electrons and increases the drain current. SONS shows the fastest program and erase speeds. SONoS uses inverse polarity ( $-V_G$  for the program, and  $+V_G$  for the erase) because it is channel-injection mode.

gramming and erasing to monitor the instant current response. The typical drain current response for the p-channel SONS is shown in Fig. 2(c). A programmed state has smaller drain current, while an erased state has larger current.

#### C. Program/Erase Transient Characteristics

Instead of the conventional  $V_T$  versus time measurements, we measure  $I_D$  immediately after program/erase pulse because this is what is actually measured by the sense amplifier.

The program and erase transient behavior of SONS, SONoS, and SoNOS is shown in Fig. 3. Fig. 3(a)–(c) shows that the devices are easily programmed within  $1 \mu\text{s}$  at low  $V_G$  bias. Moreover, SONS shows much faster program speed than SONoS or SoNOS. The reason is because SONS does not have tunnel oxide, thus providing very fast speed injection (nitride has much lower barrier height than oxide). After programming,  $I_D$  decreases because of the hole injection in the p-channel device. At longer programming time,  $I_D$  approaches zero. Fig. 3(d)–(f) shows that SONS has much faster erase speed, and its erase speed is comparable with the programming speed. This is because nitride has similar tunneling barrier ( $\sim 2$  eV) for both electron and hole.

In Fig. 3, SoNOS needs reverse polarity for program/erase because SoNOS is programmed and erased by channel injection, while SONS and SONoS operate through gate injection.

#### D. Endurance Characteristics

The endurance characteristics of various devices are compared in Fig. 4(a). SONS shows the best memory window. This is caused by more efficient injection when the tunnel oxide is removed. Moreover, the introduction of silicon-rich nitride also enhances the charge-trapping characteristics. Fig. 4(b) shows that the memory window increases with larger operation voltages. However, the endurance is degraded because higher field causes more channel injection through the bottom oxide that degrades the read current.

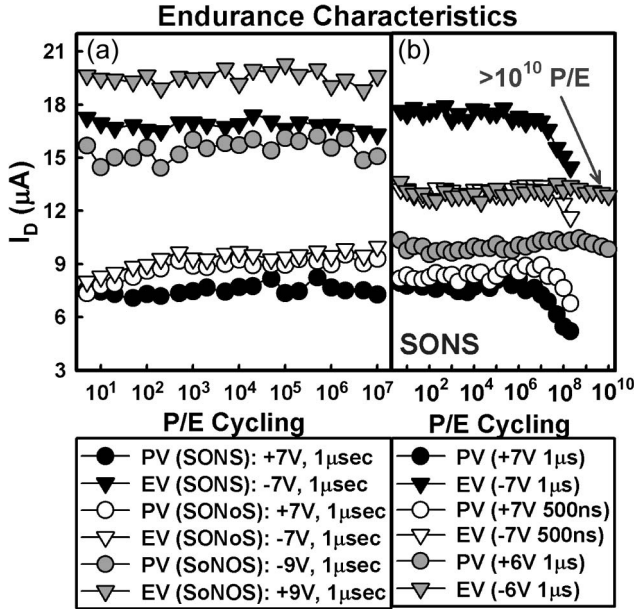


Fig. 4. (a) Endurance characteristics of SONS, SONoS, and SoNOS. SONS shows the best memory window. (b) Endurance characteristics for different bias voltages and P/E time for the SONS device. At  $\pm 6$  V operation, more than  $10^{10}$  P/E cycling is achieved.

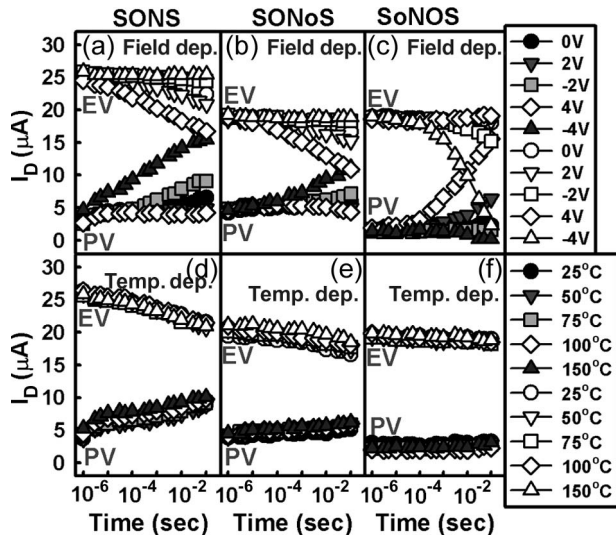


Fig. 5. (a)–(c) Field dependence and (d)–(f) temperature dependence of retention characteristics of SONS, SONoS, and SoNOS. SONS and SONoS are P/E by  $\pm 8$  V at 50  $\mu\text{s}$ , while SoNOS is P/E by  $\mp 8$  V at 50  $\mu\text{s}$  before retention test. Different external gate voltages (waiting voltage) are applied for field-dependence retention test, while different *in situ* baking temperatures are applied for temperature-dependence retention test. The retention characteristics of all devices are sensitive to the waiting voltages, but not on the storage temperatures.

Therefore, reducing the operation voltage is necessary to improve the endurance. At  $V_G < 6$  V, endurance can be greater than  $10^{10}$  cycles, suitable for high-endurance quasi-non-volatile memory applications.

#### E. Retention Characteristics

We measured the field and temperature dependence of the retention characteristics of SONS, SONoS, and SoNOS within a very short time (from 1  $\mu\text{s}$  to 0.1 s), as shown in Fig. 5,

to further investigate the transient charge relaxation (retention) behavior.

To monitor the field dependence of charge loss, in Fig. 5(a)–(c), we applied different external gate voltages (waiting voltage) during retention. We found that the retention characteristics of all devices were strongly dependent on external electric field since the external charges could easily inject into nitride by direct tunneling at low voltages. The larger waiting voltage resulted in larger electric field and larger injected current. The field dependence of SONS was more significant than that of SONoS because SONS did not have tunnel oxide to block the tunneling current.

We also studied the retention by *in situ* high-temperature pulse-IV measurement, as shown in Fig. 5(d)–(f). Surprisingly, the results show that the retention characteristics of all devices are very insensitive to the measuring temperature. Since the thermionic emission processes such as Frenkel–Poole emission should be very sensitive to temperature, we suggest that for SONS, SONoS, and SoNOS devices, the retention charge loss mainly comes from external charge injection (direct tunneling) to recombine the trapped charges, but not from the charge detrapping through thermionic emission processes. This result also suggests that the nitride traps are indeed very “deep” such that no fast detrapping occurs within seconds even at high temperatures.

#### IV. CONCLUSION

Pulse-IV measurement has been successfully applied to study the fast charge injection and relaxation of various SONS, SONoS, and SoNOS devices. We also prove that the major retention mechanism comes from direct tunneling leakage but not from thermionic emission of traps.

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