摘要

半導體元件微縮化是微處理器效能進化的原動力,元件的速度以每代增快百分之三十的速度挺進，如此微處理的效能方能以每兩年倍增的速度進步。為了維持如此的進步速度，積極的引進先進的淺接面技術勢在必行。淺接面技術中，選擇合適的金屬矽化物以提供低電阻電極及淺汲極接面試其中非常重要的一環。

金屬矽化物/多晶矽雙層結構可同時提供低電阻及低接觸電阻，因此吸引了許多研究者的注意，更進一步應用自我對準法將矽化物廣泛地應用於超大型積體電路元件上。然而由於淺接面的需要，對金屬矽化物厚度控制的要求日益嚴格，如此才能兼顧低電阻及低漏電，所以對金屬矽化物材料及製程的要求亦相形重要。

矽化鈷符合多項超大型積體電路元件使用的要求,可同時用於電極及汲極。相較於矽化鈦，矽化鈷不但具有低電阻及高熱穩定性，此外對於微小線寬上的金屬矽化物生成亦有較佳的能力。然而，若製程控制不良而形成不平整矽化鈷/矽介面或矽化鈷穿刺，則會使漏電流惡化。由於元件的微縮化，矽化鈷及接面邊界之間的距離越加接近，所以如何改善矽化鈷製程以兼顧速度與省電的需求對深次微米/奈米級元件是不可或缺。

在本文中我們將矽化鈷製程應用於奈米級元件,並研究其使用於金氧互

補半導體元件及電阻上引發的各種問題。我們發現覆蓋層材料的選擇對於微細線寬之電阻及淺接面漏電的控制非常重要。鈦覆蓋層及氮化鈦覆蓋層對微細線寬之電阻及淺接面漏電有非常不同的表現。在氮化鈦覆蓋層的製程中，矽化鈷會深入淺溝渠與主動區的介面，結果不但造成微細線寬上異常的電阻變化，並且惡化淺接面之漏電流表現。除了覆蓋層材料的選擇外，我們亦嘗試使用氧化層中介磊晶技術於奈米級超大型積體電路元件上，以提供平整的矽化鈷/矽介面，經由最佳化的氧化層及熱製程條件調整，得以達成低電阻及低漏電的要求。

最後，我們亦針對矽化鈷在微細線寬之多晶矽電阻上的熱穩定性進行研究。我們觀察到在微細線寬上矽化鈷的熱穩定性會產生異常的變化，而此種異常的變化和矽化鈷的粒徑分布與實際線寬有關。聚結現象之活化能亦在本文中被討論。藉由實驗我們推導出不同微細線寬上矽化鈷聚結現象的活化能，我們亦利用矽化鈷的聚結現象推導出一熱穩定性的量化指標，此熱穩定性的量化指標與矽化鈷的厚度、微細多晶矽電阻之線寬及矽化鈷的臨界粒徑有關，並且此熱穩定性的量化指標與微細線寬上矽化鈷聚結現象的活化能間亦呈現良好的一致性。

ABSTRACT

The scaling of the CMOS transistor has been the primary factor driving improvements in microprocessor performance. Transistor delay times have decreased by more than 30% per technology generation resulting in a doubling of microprocessor performance every two years. In order to maintain this rapid rate of improvement, aggressive engineering of the source/drain and well regions is required. One of the key factor for improving device performance is to select silicide for low resistance and shallow source/drain junction.

A compromising scheme, which uses silicide(metal)/polysilicon bi-layer structure as gate electrode and low contact-resistance interface, was investigated by many researchers. The incorporation of silicides in the devices structure is often implemented by using the self-aligned technique. The metals can react with silicon on both poly gate and source/drain area to form silicide. However, for the shallow junction requirements, the thickness of the silicide has to be controlled. The trade-off between low leakage at source-drain area and low resistance for gate stack needs to pay more attention on silicide material and process selection.

Cobalt silicide($CoSi_2$) meets many the criteria and has become one of the most promising candidates for silicide technology application. $CoSi_2$ is used for source, drain, and gate in the submicron CMOS device is an attractive material because its potential for low resistance. The resistivity and thermal stability of $CoSi_2$, are better than those of $TiSi_2$. In

addition, the sheet resistance of $CoSi_2$, is relatively insensitive to decreasing line-width.

However, $CoSi_2$ junctions can suffer high diode leakage because of non-uniform $CoSi_2$/Si interfaces or $CoSi_2$ spikes. The margin between the silicide thickness and junction depth lower range is getting smaller along device shrinkage, therefore good uniformity and smooth silicide/Si interface are necessary to serve deep sub micron process need in order to take care the needs from two ends - speed and power consumption.

In this thesis, cobalt silicide was applied on nano-scale CMOS process. Source/drain area, activation area resistors and poly resistors were formed with cobalt silicide and the behavior of silicide on CMOS devices and resistors were studied. According these studies, the capping material selection is very important for the cobalt silicide formation. The TiN capping and Ti capping processes demonstrated very different behaviors on resistivity for narrow line and junction leakage. Penetrated silicide profile in TiN capping process induced the anomalous width-dependent sheet resistance change. This penetrated silicide profile in TiN capping process also resulted in the anomalous junction leakage as compared to the junction leakage performance of Ti capping process. Besides the optimized capping material selection, the smooth $CoSi_2$/Si interface can be achieved by implementing oxide-mediated epitaxy (OME) process. Low sheet resistance and junction leakage current can be obtained by optimal process.

Finally, the thermal stability for silicided poly resistors was studied. Anomalous thermal stability for narrow lines was concluded to related to the grain size distribution and the actual poly line width. The thermal stability for silicided poly resistors was also studied by extracting the activation energy for agglomeration. A quantitative equation for thermal stability was derived by the combination of thickness, line width and critical grain size. This equation shows good correlation with the activation energy of silicide thermal stability degradation and the material thermal stability index can also be derived

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