Chapter 1

Introduction

1-1 Motivation

The complementary metal oxide semiconductor (CMOS) field effect transistor (FET) has formed the basis of the silicon integrated circuit industry for decades. This extremely small unit is used to construct various sophisticated electronic products. Figure 1-1 presents a cross section of a typical MOSFET. The central region is called the gate. In this region, the substrate silicon is isolated from the gate electrode (typically a polysilicon layer) by an insulating layer, so-called spacer (typically a thermally grown SiO_2 and Si_3N_4 layer). The two adjacent regions, called the source and the drain, are interchangeable and formed by the controlled diffusion of the dopant in these areas. The MOSFET is the building block of various complex circuits designed and manufactured today. For more than 3 decades, MOS device technologies have been shrunk to a very small scale dramatically. [1] A large part of the success of the MOS transistor follows from its scalability to smaller dimensions, which increase the density and improves the performance of devices. Since the early 1970s, technical progress has propelled the integrated circuit industry from small-scale integration (SSI), at fewer than 30 devices per chip, through medium-scale integration (MSI), at 30 to

10^3 devices per chip, through large-scaled integration (LSI), involving 10^3 to 10^5 devices per chip, to very-large-scaled integration (VLSI), at 10^5 to 10^7 devices per chip. Currently, ultra-large-scaled integration (ULSI) involves 10^7 to 10^9 devices per chip. Table1-1 lists the device dimensions and density changes that have accompanied technical advances. The capability to improve performance consistently while reducing power consumption has made CMOS architecture the dominant technology for integrated circuits. The scaling of the CMOS transistor has been the primary factor that has driven improvements in microprocessor performance. Transistor delay times have decreased by over 30% per technological generation, double microprocessor performance every two years. Aggressive engineering of the source/drain and well regions is required to maintain this rapid speed of improvement. Key methods for improving device performance are (1) to create shallow source/drain extension (SDE) profiles for improved short channel effects; (2) to explore new materials that fulfill low resistance (R) and low capacitance (C) requirements; (3) to use retrograde and halo well profiles to improve leakage characteristics, and (4) to scale the thickness of gate oxide. The scaling rate of the last decade will be extremely difficult to continue if no new method is available for improving devices found. The ability to overcome current physical and material limitations, such as gate oxide thickness, the use of low-RC materials and the formation of shallow junctions, as well as tradeoffs in circuit design, will determine whether MOS transistors can be scaled into the next century.

The characteristics of a MOS device are determined by several parameters, of which the RC time constant is the most important. R and C represent, respectively, the effective total resistance and capacitance at the gate and interconnection levels. A higher the RC value corresponds to a slower operating devices. Early MOSFET circuits used aluminum as the gate electrode and the contact metal, neither of which was self-aligned with the source/drain, so the layout dimensions were limited. The introduction of polysilicon for the gate electrode and the interconnection has enabled the self-alignment and high-temperature processes. Thus, issues associated with the poly-gate electrode and the interconnection have quickly come to represent current mainstream of MOSFET technology, notwithstanding the latent disadvantage of the high resistivity of polysilicon. This disadvantage of polysilicon was not seriously considered in the early 1970's because polysilicon met the requirement of circuit speed. As the minimum feature size of devices continues to shrink, the latent disadvantage of polysilicon is gradually becoming evident, and has been regarded as a primary constraint on the speed performance of devices. [2,3] Many approaches have been proposed to alleviate this problem. One of them is to replace polysilicon with refractory metals [4-7] or metal silicide. [8-10] However, using refractory metals as gate electrodes will change the work function of the gate. Moreover, refractory metals cannot withstand most of the extensively used chemicals and so impose many limitations on the fabrication process, the reliability of refractory metals as gate electrodes also remains questionable. Therefore, refractory metals

are rarely used as gate electrodes in practical MOSFET circuits.

Many researches have investigated a compromise, which involves using the silicide(metal)/polysilicon bi-layer as the gate electrode and a low contact-resistance interface. [11-16] Silicides are commonly incorporated into devices by self-aligned process. [17-23] The metals can react with silicon on both the poly gate and the source/drain area to produce silicide. The resistivity of silicides is normally one order of magnitude lower than that of the heavily doped polysilicon, [24] so the bi-layer structure experiences a smaller RC time delay. Besides the resistivity improvement, self-aligned silicidation (so-called salicide) provides large-area contacts and substantially reducing parasitic series resistance. [25,26] However, , the thickness of the silicide has to be controlled to fulfill the shallow junction requirements. The trade-off between low leakage in the source-drain area and the low resistance of the gate stack requires that more attention be paid to silicide material and process selection.

1.2 Selection of Silicide for ULSI Devices

Many metals, including most refractory and near-noble metals, have been proposed to form silicide. Various important characteristics must be considered when a silicide selected for IC applications.

(1) Low resistivity

(2) Ease of formation of the silicide

(3) Lack of reactivity with SiO_2 and Si_3N_4

(4) Low contact resistance, and minimal junction penetration

(5) Smooth salicide surface and silicon/salicide interface, and providing low junction leakage current

(6) Ability to be removed by selective etching, and compatibility with self-aligned silicide process

(7) Minimum Si consumption for silicide formation

(8) Adequate thermal stability

(9) Mechanical stability with low film stress and good adhesion to Si

(10) Excellent resistance of silicide to post-silicidation dry/wet etching process

Table 1.2 presents basic properties of several silicides, of which $TiSi_2$ has been widely used in silicide processes since 0.25um node, because it has low resistivity and high thermal stability. In the formation of $TiSi_2$, initially, Ti silicide is formed in the meta-stable C49 phase (60-90μΩ-cm), which must then be converted through additional thermal treatment to the desired low resistivity C54 phase (13-20μΩ-cm). However, the line width, the film thickness, the surface energy and the formation temperature influence this phase transformation. [27-29] The observation of the dependence on line width of the

transformation of $TiSi_2$ to its low-resistance phase, has motivated the study of the alternatives. [30,31] Cobalt silicide($CoSi_2$) meets many important criteria and has become one of the most promising candidates for silicide technology applications. It is an attractive material because it has for low resistance, compatibility with self-aligned silicide process. [32-34] The resistivity and thermal stability of $CoSi_2$, are also better than those of $TiSi_2$. Furthermore, the sheet resistance of $CoSi_2$, is relatively insensitive to narrow line-width. The Co silicide process can successfully reduce the resistance for a gate of length 0.075μm. [35-37] $CoSi_2$ is generally formed in using a two-step annealing process. The first step of annealing is at low temperature (450-550℃) and yields Co-rich silicide (such as Co_2Si or CoSi), while minimizing lateral silicide formation. After wet etching to remove the un-reacted Co, high-temperature annealing (750-850℃) is applied to convert the silicide to the low resistivity phase, $CoSi_2$. [38]

However, $CoSi_2$ junctions suffer high diode leakage because the $CoSi_2$/Si interfaces are non-uniform or $CoSi_2$ spikes occur. According to the SIA roadmap (Fig. 1-2), the required silicide thickness is only about 30nm for the 0.1um node, the margin between the thickness of silicide and depth of shallow junction shrinking, so a uniform and smooth silicide/Si interface is required to support deep sub micron processes to needs of speed and power consumption. Additionally, controlling the source/drain parasitic series resistance (Rsd) is becoming important to drive the scaling down of devices. As in earlier generations, the total Rsd should

be less than 10% of the total series resistance for a MOS, to ensure acceptable device performance. The Rsd of the current path from the contact to the edge of the channel can be modeled by the sum of four components, (Fig.1-3)

$$Rsd = Rco + Rsh + Rsp + Rac \quad (1)$$

Where Rco is the contact resistance between metal and the source/drain region, Rsh is the sheet resistance of the bulk region of the source and drain, Rsp describes the resistance of the current crowding near the channel end of the source, and Rac is the accumulation –layer resistance.[39] The impact of contact resistance (Rco) is growing as the device scaled down. The factor that dominates the control of Rco is the formation of silicide.

The following chapters focus on the $CoSi_2$ process with topics to junction leakage, the sheet resistance of silicide, device performance and thermal stability. Studies of these issues reveal a new path to nano-scaled ULSI processes.

1-3 Thesis Outline

In this thesis, cobalt silicide was applied to a nano-scale CMOS process. The source/drain area, activation-area resistors and poly resistors were formed with cobalt silicide. The behaviors of silicide on CMOS devices and resistors were investigated. Chapter 2

discusses the theory of silicide formation, including the epitaxial silicide growth. The thermal stability theory for silicide is also discussed in this chapter. Chapter 3 describes the test structures used in work, and also addresses theories for the measurements used in this study.

In Chapter 4, cobalt-silicide samples with the different capping material, exhibit the different changes in the sheet resistance change with the width of the active region; the effect on junction leakage were also studied. Chapter 5 then discusses the epitaxial silicide growth, which provides a smooth interface between silicon and silicide, thus reducing junction leakage.

Chapter 6 addresses the thermal stability of silicide formed on nano-scale poly resistors. Anomalous thermal stability was identified and is discussed in relation to grain size distribution. Chapter 7 presents a quantitative equation, which explains the thermal stability behavior for thin and narrow silicided ploy resistor. This chapter also develops an index for predicting the effect of substrate properties on silicide formation. Finally, chapter 8 draws conclusions and offers suggestions for future studies.

Chapter 2

Basic Theories for Silicides

2.1 Formation of Silicide

Many previous studies have addressed the reaction of cobalt (Co) and silicon (Si). [1-5] Figure 2-1 shows the sheet resistance after deposition Co on Si and rapid thermal annealing (RTA) at various temperatures. The sheet resistance increases from 300 °C to 500 °C, and decreases as the temperature rises further. The change in sheet resistance is directly correlated with the phase formation. Figure 2-2 presents the X ray diffraction spectra of cobalt silicide formed at different RTA temperatures. In this figure, Co_2Si and CoSi are present at low temperatures. The CoSi phase grows until 500 °C and the Co layer is completely converted to CoSi. Treatments at higher temperatures lead to the formation of $CoSi_2$. The phase sequence obtained from X-ray diffraction (XRD) agrees closely with the sheet resistance data. Table 1-2 reveals the sheet resistance is 70 $\mu\Omega$-cm for Co_2Si, 100-150 $\mu\Omega$-cm for CoSi and 14-17 $\mu\Omega$-cm for $CoSi_2$.

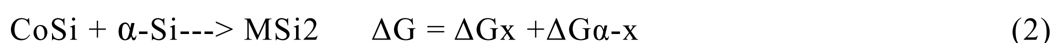
Figure 2-3 presents the phase sequence Co-CO_2Si-COSi-$COSi_2$ at various RTA temperatures, and thus elucidate the phase transformation. In this phase transformation sequence, the growth of Co_2Si and CoSi are controlled by the

diffusion of Co and Si, respectively. [6,7] The kinetics activation energies for the growth of Co_2Si and CoSi are 1.5 eV and 1.9 eV, respectively. [4,7] The growth of $CoSi_2$ is controlled by mixed kinetics of nucleation and diffusion via Co motion. [8] The nucleation of the $CoSi_2$ phase occurs at triple point between two CoSi grains and Si. Then, lateral growth takes place until a continuous $COSi_2$-Si interface is formed. The reaction then proceeds layer by layer. [8-9] Therefore, following an initial fast transformation, the interaction slows down. The diffusion of Co through $CoSi_2$ is slow and has high activation energy. [10] This fact is indicated by the slow $CoSi_2$ growth at low temperatures, according diffusion-controlled kinetics.

2.2 Substrate Effect on Silicide Formation

The substrate is important in thermodynamically that determining the formation of silicide, especially in the final stage of the reaction, in which the $CoSi_2$ grows at the expense of the CoSi. [8] For most silicides, the di-silicide on Si is more stable than the mono-silicide. Therefore, the following reaction schemes and their associated free energy changes, ΔG, must be considered.

$$CoSi + x\text{-}Si \rightarrow CoSi2 \qquad \Delta G = \Delta Gx \qquad (1)$$



$$CoSi + \alpha\text{-}Si \text{---}> MSi2 \qquad \Delta G = \Delta Gx + \Delta G\alpha\text{-}x \qquad (2)$$

where M stands for the metal; x is for crystalline; α represents amorphous Si, and ΔGα-x is the Gibbs free energy of crystallization of α-Si. ΔGx is of the order of kT.[11] The heat of crystallization of α-Si, of the order of 15 kJ mol^{-1}, is much higher than the free energy change from the mono-silicide to the di-silicide. [12,13] This fact explains why a nucleation-controlled process occurs during the growth of the di-silicide from the mono-silicide on x-Si and a diffusion-controlled growth process occurs on α-Si. [14] The formation of cobalt silicide on top of amorphous silicon is faster and provides a better surface morphology. Pre-amorphization by Ge [15] and implantation of N_2 [16] has been proposed to inhibit poly Si grain growth, and thus to provide smaller grain size. Dopants in the substrate also play a role in formation of silicide. Chou et al. reported on the enhanced grain growth of phosphorous-doped poly-Si during silicidation, attributes this to the redistribution of phosphorus.

2.3 Formation of Epitaxial Cobalt Silicide

$CoSi_2$ grows epitaxially on Si because it has a similar lattice structure to that of Si (CaF_2) and a small lattice mismatch (~1.2%) with Si at room temperature. However, single-crystal epitaxial $CoSi_2$ cannot be formed by simple deposition and annealing on most Si surfaces, although it can be formed on Si (111). Bulle-Lieuwma et al. reported the effect of substrate orientation on $CoSi_2$ growth.

[18]. They proposed that, in addition to the good in-plane lattice match between Si (100) and $CoSi_2$ (100) planes, Si (100) planes also match $CoSi_2$ $(01\bar{1})$, $(12\bar{2})$ and $(53\bar{3})$ planes closely. The multiple available ways of lattice matching make the epitaxy (with a single orientation) of $CoSi_2$ on Si (100) difficult. Therefore, many methods of improving the epitaxy of $CoSi_2$ on Si surfaces have been proposed. Many works have presented for epitaxial silicide growth, such as titanium-interlayer-mediated epitaxy (TIME), [19] oxide-mediated epitaxy (OME) [20] and high-temperature sputtering (HTS) [21]. Bypassing the formation of the intermediated phases, Co_2Si and CoSi, is very important in growing epitaxial $CoSi_2$. [22-24] The growth of intermediated phases, Co_2Si and CoSi, is controlled by diffusion, so reducing the supply rate of Co is key to the growth of epitaxial $CoSi_2$. The oxide-mediated epitaxy demonstrates the $CoSi_2$ epitaxy through a deliberately grown line layer of “chemical” oxide.[20] This thin SiOx acts as a barrier that reduces the diffusion of Co towards Si. This thin amorphous layer presumably contains Ti,Co,Si and O. The rate of flux has thus been suggested to be the most crucial factor in the alignment of CoSi2 with the Si substrate.

2.4 Thermal Stability of Cobalt Silicide

Given sufficiently high mobility, all samples evolve to minimize their total

energy. This means that, if no chemical transformation occurs, then the surface energy is minimized. Therefore, liquid drops are spherical, as by thermodynamics: a higher surface energy more strongly drives agglomeration. However, things look differently when kinetics is considered. A plane thin film exhibits contrary behavior: any fluctuation increases the size of the surface and the surface energy, and is therefore unstable; the instability increases with the specific surface energy. This seems paradoxical between thermodynamics and kinetics: thermodynamics dictate that the driving force for agglomeration increases with the specific surface energy; the kinetics states that in contrast, higher surface energy reduces the likelihood of agglomeration. In the real world, the $CoSi_2$ layers can be prepared in solid-state reactions by rapid thermal annealing and subsequent annealing at high temperatures to trigger agglomeration. However, the high activation energy for agglomeration (3.5 – 5.2 eV) [25] explains why samples with initially small grains are the most morphologically stable at low temperatures and short period annealing. This fact is in agreement with proposed models of the agglomeration of thin film.

When the temperature is high enough or annealing time sufficiently long to overcome the activation energy, agglomeration occurs via thermal grooving. The grooving process proceeds until local equilibrium at the grain boundary and the film surface/interface is reached. [26,27] Local equilibrium is reached when the force of surface/interface energy (γ_S/γ_i) is balanced by the grain boundary energy(γ_b), as shown in Fig. 2-4. The relationships among surface, interface and grain boundary energies are,

$$\gamma_b = 2\gamma_S \sin\theta s \quad (3)$$

$$\gamma_b = 2\gamma_i \sin\theta i \quad (4)$$

where θs and θi are the equilibrium angles at surface and interface, respectively. The thermal grooving concept has been proposed [28,29] to determine the critical grain size Lc, below which no islanding occurs. According to these models, L increases for thicker films, lower grain boundary energies and higher surface energies. The point is to limit grain growth during thermal treatment, such that Lc is not surpassed. Typical L values are about ten times of the silicide film thickness, for example, a grain size of 500 nm for a 50 nm silicide film.

The literatures offer widely different data on thermal stability of $CoSi_2$ and $TiSi_2$. [30-34] Studies of grain size control and related thermal stability have not been conducted systematically. In general, impurities at the interface or at the surface improve the thermal stability of $TiSi_2$. For $CoSi_2$ smaller grains increase thermal stability. The use of a capping layer generally limits thermal degradation, because it increases the silicide/SiO_2 interfacial energy and inhibits the material transport. Furthermore, the thermal stabilities of both $CoSi_2$ and $TiSi_2$ on polycrystalline Si have been reported to be worse than those on mono-crystalline Si. Notably, minor changes in the processing conditions during silicidation significantly affect thermal stability. [35,36]

Chapter 3

Test Structures and Measurements

3.1 Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

This section presents the process flow of the metal-oxide-semiconductor field-effect transistor (MOSFET). Figure 3.1 schematically depicts the cross section of the nano-scaled USLI circuit. Boron-doped, p-type Si with resistivity of 10 Ω cm and 001 orientation were used as substrates; after the growth of pad oxide and the deposition of silicone nitride, the active region was defined by deep ultraviolet (DUV) lithograph; a shallow trench was then etched. After the photo resist was removed, the silicon trench was filled by oxide to complete isolation of the shallow trench process.

Following the shallow-trench isolation (STI) formation, the P-well and N-well were produced by implanting boron and phosphorus, respectively, into the regions defined by the photo resist. Wafers were sent for wet cleaning before gate oxide was grown in a furnace. After the growth of gate oxide, poly silicon was deposited on the gate oxide by low-pressure chemical vapor deposition (LP-CVD). DUV lithograph was applied to define the gate conductor, local connection and poly resistors.

Thinner gate oxide and channel with high dosage of implant are needed in shrinking short channel devices. However, both approaches drastically increase the electric field near

drain regions where charge carriers, accelerated by this field and becoming hot, can overcome the oxide barrier and be injected into the gate. Hot carriers damage gate oxide and may be trapped there, degrading the performance of device. The lightly doped drain (LDD) alleviates this problem by reducing the drain field. [1] Moreover, in nano-scaled devices, the spacer interface degradation from the hot carrier injection is not subjected to gate control. A better approach is to implement the LDD at a large-tilting angle. [2] Furthermore, a "halo" implant must be applied to the drain of the device to improve the punch-through voltage of a MOSFET. [3] Both large-tilting angle LDD implant and halo implant are self-aligned to gate electrode.

After LDD engineering, the spacer is form by the deposition of SiO_2 and Si_3N_4, followed by anisotropic etching. The N+ source / drain and P+ source / drain were formed by self-aligned of implanted As/P and BF_2/B, respectively, to the spacer. Rapid thermal annealing (RTA) was then applied to activate the implant doses.

After S/D engineering, self-aligned silicide (salicide) is applied. In this thesis, several approaches were used, including Ti capping/TiN capping and oxide mediated epitaxy (OME) cobalt silicide processes. The following chapters detail the silicide process.

After silicide formation, the inter-layer dielectric film was formed by CVD. DUV lithography is used to define the contact, and then the contact holes are created by applying anisotropic etch. Tungsten (W) plug is filled into contact hole, then followed by chemical

mechanical polish (CMP) for planarization. Finally, copper metallization was performed. The structure used in the thesis, including the MOS, two-terminal resistors (see section 3.2), perimeter-intensive diodes (see section 3.3) and the bridge-cross Kelvin resistor (see section 3.4), were made according to the complex steps described above.

3.2 Two-terminals Active-Region Resistor and Poly Resistor

As plotted in Fig.3-2, the resistance of a rectangular section of a film with length (L), width (W) and thickness (t), is given by

$$R=\frac{\rho L}{Wt} \tag{1}$$

where R is the resistance of the film, and ρ is the resistivity. Introducing sheet resistance, changes Eq. 1 to

$$R= Rs\frac{L}{W} \tag{2}$$

where Rs is the sheet resistance in Ω/sq, and is independent of the size of the square, but depends only on the resistivity and thickness of the film. The sheet resistance can be obtained directly from the voltage drop across the length of the two-terminals resistors.

In this thesis, two types of two-terminals silicided resistors were used, one was on the active-region the other is on the poly-Si (Fig. 3-3). Resistors for both the active region and the poly-Si were fabricated with different widths from 90nm to 2000nm. The resistance was measured by applying 0.1mA of current and then measuring the voltage drop between the two terminals.

3.3 Perimeter-intensive diodes for Junction Leakage Measurement

A high electric field across a reverse-biased p-n junction causes significant current to flow through the junction by the tunneling of electrons from the valence band of the p-region to the conduction band of the n-region (This is called band-to-band-tunneling (BTBT)). [4] In an MOSFET, when the drain-substrate and/or the source-substrate junction is reverse-biased at a potential higher than that of the substrate, a significant BTBT current flows through the junctions. In nano-scale devices, higher doping at the junctions makes this current significant and considerably increases the total leakage current. The cobalt silicide spikes, [5] and the mechanical stress which induced by the silicide and STI, [6] can weaken the control of junction leakage. In this study, the worse pattern for junction leakage – perimeter-intensive diodes, were used to measure junction leakage because such pattern is with larger perimeter than bulk pattern, when the total area for these patterns are the same.

Both N+/P-well and P+/N-well junctions were studied in this thesis. Figure 3-4

schematically depicts N+/P-well perimeter-intensive diodes. This combo-type diode is composed of 600 active region branches, each of which is 0.1μm wide and 65μm long. The total perimeter is about 80,000μm.

For a PN junction under reverse bias, the total reverse current can be given by the sum of the ideal reverse saturation current and the generation current in the depletion region [7] :

$$\boldsymbol{I_R = I_{gen} + I_s \approx I_{gen}} \quad (3)$$

$$I_{gen} = A * \int_0^w eQdx = \frac{en_i W}{2\tau_0} \quad (4)$$

where W is the width of the depletion-layer and τ_0 is the effective lifetime. At a given temperature, the ideal reverse saturation current is independent of the reverse-bias. However, I_{gen} is proportional to the width of the depletion-layer, and depends on the applied reverse-bias. Thus, the diode reverse leakage current is expressed as follows;

$$I_{gen} \propto T^{\frac{3}{2}} * V^{\frac{1}{2}} * \exp(-\frac{Ea}{kT}) \quad (5)$$

where T is the temperature and V the applied bias. Ea represents the activation energy close to the energy level of the generation-recombination centers (Eg/2). In this study, the

junction leakage was measured under different reverse-biases to understand the voltage dependency of the junction leakage on silicided perimeter-intensive diodes.

3.4 Bridge Cross Kelvin Resistor (CBKR) and Specific Contact Resistance

The shrinking of devices requires the development of self-aligned silicides, such as $CoSi_2$ and $TiSi_2$, to improve the specific contact resistivity ρ_c. It is important for process development to monitor the specific contact resistance between the silicide and silicon. In the standard Kelvin test structure for measuring metal to source/drain contact resistivity, three contacts are required over the same diffusion region (Fig. 3-6). But by the nature of self-aligned silicide, the entire diffusion region is silicided and thus there is only one silicide-to-Si contact within each diffusion region. Therefore, only the metal-to-silicide contact resistance can be measured, but not the silicide-to-Si contact. Lynch et al reported a test structure called the Bridge Cross Kelvin Resistor (CBKR). [8] This test structure is equivalent to a Kelvin test structure that can be produced by the standard silicide process, so the actual silicide-to-Si ρ_c can be accurately monitored. The new tester mainly consists of three silicided source/drain areas separated by two gates (Fig. 3-5). These three contacts although physically separated by the gates, can be electrically connected if a gate bias (Vg >> Vt) is applied, thus providing connectivity and satisfying the requirements of a Kelvin test structure. Notably, the structure, basically two MOSFETs back-to-back, is fully

compatible with standard device processing. This factor is important because the tester can be incorporated into the wafer as a monitor and processed simultaneously. The results can thus exactly duplicate those of the real devices.

The main difference between this test structure and a conventional Kelvin test structure is the current flow pattern in the Si region, as shown in Fig. 3-6 and 3-7. Specifically, current patterns between the contacts differ in two major ways. First, in the new structure, the connection is the MOSFET channel whose sheet resistance per square differs from that of the diffusion region underneath the silicided contact. Second, the current pattern in that region is physically confined to the surface with channel thickness of less than 100 A. This could potentially affect the validity of the transmission-line model (TLM) of the center contact [9] since the TLM assumes the diffusion layer under the silicide (ground plane). Is a homogeneous planar sheet. When there is current crowding at the edge of the channel, the validity of the planar sheet approximation should be determined by the current uniformity (as a function of depth) directly underneath the leading edge of the contact. Since the spacing between the channel edge and the contact edge, i.e. the lateral extent of the junction, is a considerable fraction (50-75%) of the junction depth, this distance is much larger than the channel thickness itself and is believed to be adequate for the current to recover to a reasonable depth. The TLM is thus believed to be accurate. It is concluded that since both of these factors occur only in the regions connecting the contacts, they should not affect the

validity of the TLM at the contacts. Also since the test structure directly models the actual current flow in the MOS device, the results obtained should be directly applicable to MOS device modeling.

As the plane view of CBKR structures is shown in Fig. 3-5, the common principle of this structure is that current is forced between two adjacent contacts, and the voltage is measured between the third contact and the center contact. Since there is no current flowing through the third contact, its potential follows the potential of the Si beneath the center contact and it incorporates the parameters such as the specific contact resistivity, ρ_c and the sheet resistance of the diffusion region Rd underneath. This voltage measured is also a function of the layout geometry. According to the TLM of a contact, if the contact metallization is held at ground potential and a current I is forced through the contact (see Fig. 3-7), the localized potential of the Si diffusion underneath the contact is given by [9]

$$V(x) = J(x)\,\rho_c$$

$$= \frac{I\sqrt{Rd\rho_c}}{W}\frac{\cosh[(\sqrt{\frac{Rd}{\rho_c}}\,(L-x)]}{\sinh(\sqrt{\frac{Rd}{\rho_c}}\,L)} \qquad (6)$$

where J(x) is the current density across the interface, W is the width (into the paper) of the device, L is the length of the contact (in this case silicide) and x is the distance from the

leading edge along the length direction. Equation (1) is an interesting general equation for any contact, and it includes the effects due to current crowding. In the CBKR, the voltage tap contact is situated at the side of the center contact (perpendicular to the current direction), and thus the measured voltage is a linear average of the Si potential over the entire length L. This measured voltage is given by

$$\text{Vside} = \frac{\int_0^L V(x)dx}{L} = I\frac{\rho_c}{LW} \tag{7}$$

from substituting Eq. (1), or general by

$$\text{Vside} = \frac{\int_0^L J(x)\rho_c\, dx}{L} = I\frac{\rho_c}{LW} \tag{8}$$

In this measurement ρ_c can be obtained without knowing Rd, and is independent of current crowding [10]. It should be noted that the structure is symmetrical such that current can be supplied via either one of the end contacts.

Chapter 4

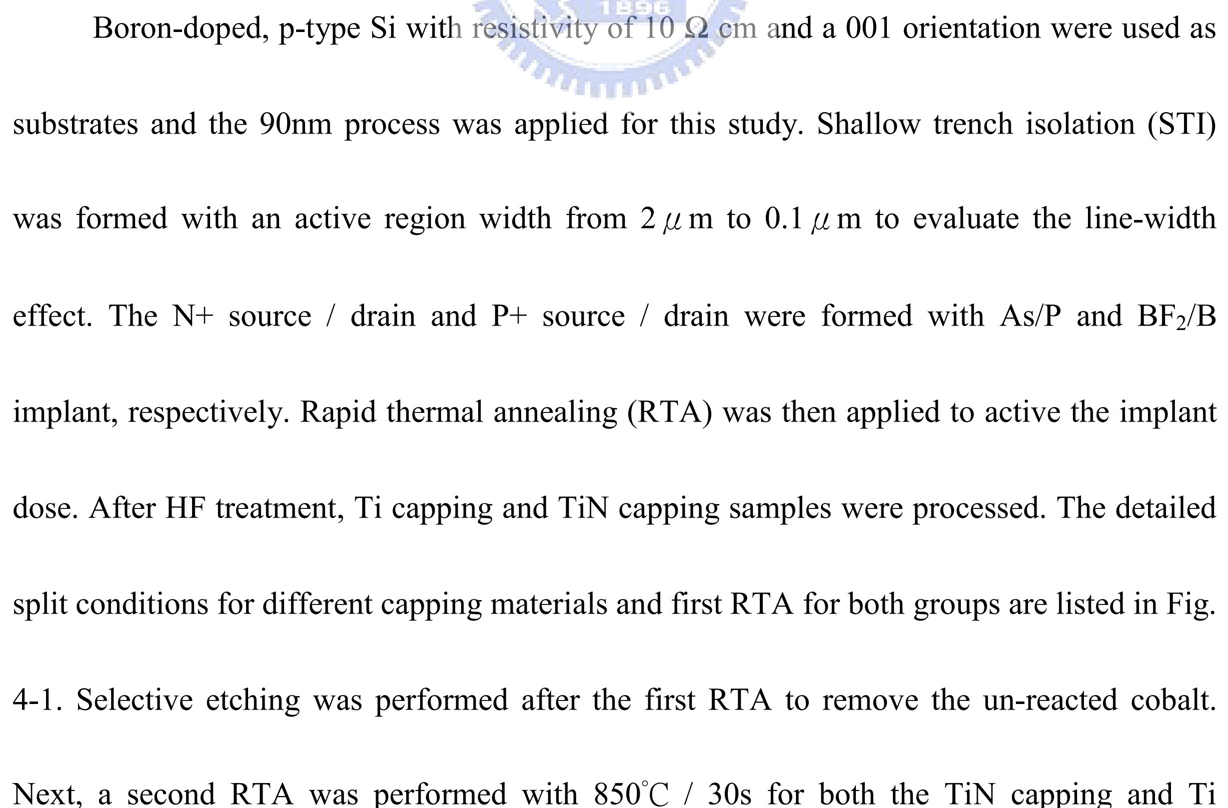
Width-dependent Anomalous CoSix Sheet Resistance Change by Ti and TiN Capping Process

4.1 Introduction

In order to minimize the RC propagation delay along the device shrinkage, self-aligned silicide (Salicide) technology has been widely used to reduce source/drain/gate spreading resistance and contact resistance. Among all silicides, Cobalt silicide ($CoSi_2$) is the most popular material beyond 0.25μm node due to less line width dependence than titanium silicide ($TiSi_2$).[1] The single layer of cobalt on silicon has been replaced by other processes, like TiN capping and Ti capping, because of the difficulties in manufacturing.[2] The TiN capping (TiN/Co/Si) process has been reported to have a large process window with respect to the control of lateral growth.[3-4] The Ti capping (Ti/Co/Si) process has been shown to be a very promising process and its scalability toward 0.1μm and below has been demonstrated.[5-6] The reaction mechanisms are different in TiN capping and Ti capping processes. Ti diffuses through the Co layer and accumulates at Co/SiO_2 interface in the Ti capping process, but only less Ti does in TiN capping case.[7] It is a common belief that Ti serves as an oxygen scavenger. It consumes the native oxide present because of insufficient cleaning or re-oxidation prior to Co sputter. The in-situ Ar sputter applied to remove native

oxide before Co deposition is usually used for the TiN capping process, but not necessary for Ti capping process.[8-9] Recently, many researches have been evaluating the performance differences between different capping materials from the perspective of sheet resistance and junction leakage.[10-13] However, no report has yet to study the impact of capping materials to the silicide formation on narrow-width active region. In this report, the Ti and TiN capping materials were investigated on 90 nm process. The difference of sheet resistance between Ti and TiN capping processes were studied by applying electrical measurement and transmission electronic microscopy (TEM).

4.2 Experimental Procedures



Boron-doped, p-type Si with resistivity of 10 Ω cm and a 001 orientation were used as substrates and the 90nm process was applied for this study. Shallow trench isolation (STI) was formed with an active region width from 2 μm to 0.1 μm to evaluate the line-width effect. The N+ source / drain and P+ source / drain were formed with As/P and BF_2/B implant, respectively. Rapid thermal annealing (RTA) was then applied to active the implant dose. After HF treatment, Ti capping and TiN capping samples were processed. The detailed split conditions for different capping materials and first RTA for both groups are listed in Fig. 4-1. Selective etching was performed after the first RTA to remove the un-reacted cobalt. Next, a second RTA was performed with 850°C / 30s for both the TiN capping and Ti

capping samples. The 193nm lithography was performed for contact layer after the inter-layer dielectric layer was formed through chemical vapor deposition. Finally, copper metallization was performed. The sheet resistance of silicided N+ active region was measured from two terminal Rs bars with the width from 2μm to 0.1μm. Junction leakage measurements were taken from finger type active region patterns. In this study, the stress effect on silicide formation was also studied. The samples were prepared on blanket wafers and the stress was measured by stress gauge which extracting stress by measuring the changes on radius of curvature. The X-ray diffraction (XRD) was performed on silicided blanket wafers for the prefer orientation study.

4.3 The Anomalous Sheet Resistance Change

Fig. 4-2 showed the anomalous sheet resistance behavior for both TiN capping and Ti capping cobalt silicide. The behaviors of these two processes were very different. The sheet resistance of the TiN capping silicided active region increased as active region width decreased, while the sheet resistance of the Ti capping silicided active region decreased as active region width decreased.

The 0.1μm active region for both TiN capping and Ti capping silicide were compared by applying TEM cross-section check. As shown in Fig. 4-3, the silicide formations of various capping layers were very different. The profile of silicide for the TiN capping samples

showed silicide penetration at the active region edge. This anomalous "crying face" silicide growth at STI edge makes the effective active region width became larger than the design of layout drawing. The width of active region was narrower, the lower sheet resistance of active region. In opposite to the TiN capping samples, the Ti capping samples showed active region edge silicide thinning, so called "smiling face" profile. The narrower active region width resulted in higher sheet resistance.

Fig. 4-4(a) showed that the anomalous sheet resistance roll-off became more significant for the TiN capping samples when the first RTA process temperature was higher, which indicated that the anomalous silicide growth at active region edge was accelerated. Also of note was that the sheet resistance for wide active region (10μm) became saturated when process temperature of RTA1 was over 500°C. This result showed the threshold RTA1 temperature for completely consumed cobalt was about 500°C. Compared to the TiN capping samples, the higher first RTA temperature slowed the anomalous sheet resistance roll-off for Ti capping one, as shown in Fig. 4-4(b). The threshold RTA1 temperature for completely consumed cobalt was about 520℃.

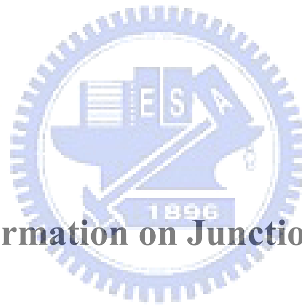
4.4 The Stress Impact on Silicide Formation

Figures 4-5 showed the cross section of the silicide profiles after first RTA for TiN capping and Ti capping samples, respectively. There is no obvious difference between the

profiles of these two samples, it's not like the results obtained after the second RTA. Similar profiles after the first RTA between two samples mean that the silicide profile difference at the active region edge occurred during the second RTA. When anneal temperature was around 500°C, the forming phase was primarily CoSi, and the moving species when forming was Si. However, when process temperature was higher than 700°C[14], the CoSi transferred to $CoSi_2$ and the moving species was Co.

Steegen et al. reported that compressive mechanical stress is induced by STI.[15] The narrower an active region becomes, the higher stress levels are that build at the active region's edges. Blanket Si substrates were prepared with silicon nitride deposited at backside of the substrate to produce compressive stress on the front side of substrate. The stress effect on silicide formation was studied. To produce different levels of compressive stress, the silicon nitride deposition conditions were evaluated by adjusting the gas ratio of NH_3/SiH_4 on CVD reactor (Fig. 4-6). After silicide formed on substrate front side by both Ti and TiN capping processes, the XRD check was performed. As shown in Fig. 4-7, the orientation preference of silicide changed as the compressive stress increased for the TiN capping process, but the orientation preference of silicide did not change for the Ti capping process. The intensity of (111) orientation (I_{111}) became higher than the intensity of (220) orientation (I_{220}) under compressive stress for TiN capping process. That means the compressive stress can enhance the formation for (111) $CoSi_2$. Since the profile difference between Ti capping

and TiN capping processes happened during second RTA, it was believed that compressive stress enhances the CoSi to $CoSi_2$ transformation. Bulle-Lieuwma et al. reported the (111) of $CoSi_2$ has the lower activation energy for nucleation than that of (200). [16] Compressive stress is believed to increase the initial surface energy of CoSi/Si, thus further decreases the activation energy of nucleation for (111). Ti was reported to exist at CoSi/CoSi/Si triple-point, decreases the surface energy, and increase the activation energy for nucleation. [17] In Ti capping process, the compressive stress may not able to overcome the surface energy increased by the existing of Ti atom at triple-point, thus, no penetrated profile was seen as in TiN capping process.



4.5 The Effect of Silicide Formation on Junction Leakage Current Control

In deep submicron process, the leakage current requires careful control to ensure that the integrated circuit operates with minimal power consumption. Therefore, junction current leakage between the silicide and silicon interface also requires effective control In this work, the active region intensive junction leakage pattern with active region width equal to 0.1μm was measured. As Fig. 4-8(a) shows, the junction leakage of the TiN capping sample was increasing while applied voltage increased. Unlike the TiN capping process, the junction leakage for the Ti capping sample increased only slightly when the applied voltage increased (see Fig. 4-8(b)). The high junction leakage of TiN capping sample resulted from the

anomalous active region edge silicide growth. Furthermore, the STI edge doping anomalous re-distribution reported by Lee[18], showed that the upward doping distribution makes the junction shallower at the STI edge, and thus, enhanced the junction leakage in the TiN capping process (see Fig. 4-9). For the selection of the silicide, both low sheet resistance and low junction leakage are important. Figure 4-10 shows the index for silicide selection. The multiple of sheet resistance and junction leakage current by 3.3 volts test was used as the index. Low sheet resistance and junction leakage current are both important factors for nano-scaled devices fabrication. According to this index, the Ti capping process showed superior performance to the TiN capping process for future deep sub-micron device need.

4.6 Conclusions

The anomalous silicide growth at the active region edges was reported. The TiN capping and Ti capping processes demonstrated very different behavior. High compressive stress at the STI and active region interface enhanced the silicide formation for the TiN capping process. Penetrated silicide profile in TiN capping process induced the anomalous width-dependent sheet resistance change. This penetrated silicide profile in TiN capping process also resulted in the anomalous junction leakage as compared to the junction leakage performance of Ti capping process. The Ti capping process proved better junction leakage performance than the TiN capping process.

Chapter 5

Oxide-Mediated Formation of Epitaxy Silicide on Heavily Doped Si Surfaces and Narrow Width Active Region

5.1 Introduction

The formation of a reliable, low-resistance and shallow silicide contact on complementary metal-oxide-semiconductor (CMOS) devices is a challenge in the manufacture of deep sub-micron ultra-large scale integrated (ULSI) circuits. As the depth of the junction is reduced to less than 0.1μm, the thickness of the silicide layer must be kept under 30nm. Good silicide uniformity and a smooth silicide/Si interface are required to ensure that the junction leakage current is low. Cobalt silicide ($CoSi_2$) has attracted much attention in the field of sub-micron CMOS technology, because it has better characteristics than other silicides such as $TiSi_2$.[1] Beyond having a low resistivity of ~10–18 μΩcm and the excellent chemical stability, [2] $CoSi_2$ grows epitaxially on Si because its has a similar lattice structure to Si (CaF_2) and a small lattice mismatch (~1.2%) with Si at room temperature. However, single-crystal epitaxial $CoSi_2$ can not be formed with simple deposition and annealing on most of Si surfaces, except on (111) Si surface.[3] Therefore, many methods of improving the epitaxy of $CoSi_2$ on Si surfaces have been developed. Titanium-interlayer-mediated epitaxy (TIME)[3] oxide-mediated epitaxy (OME)[4] and high-temperature sputtering (HTS)[5] can improve epitaxy. Among these techniques, OME is

compatible with general semiconductor processes because of the simple process requirement.

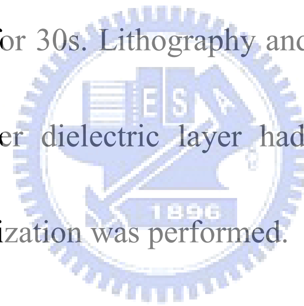
Epitaxial cobalt silicide has a smoother interface than silicon and a much higher thermal stability.[6-7] However, the dopants implanted in the Si layer seem to influence strongly the properties of silicide.[8-9] In this work, the effects of the dopant species and the various chemical oxides on the electrical characteristics of cobalt silicides are investigated.

5.2 Experimental Procedures

A boron-doped, p-type Si blanket wafer with a resistivity of 10 Ω-cm with an (001) orientation was used as the substrate in this work. Heavy N-type and P-type dopants were implanted into the Si substrate and then high-temperature rapid thermal annealing was performed (RTA). Three different chemical species - ozone, APM (NH_4OH:H_2O_2:H_2O=1:5:25) and HPM (HCl:H_2O_2:H_2O=1:1:4) were used to form chemical oxide layers before cobalt sputtering to study the effect of quality of the chemical oxide on the OME. The titanium (Ti) cap was sputtered after cobalt (Co) was deposited without breaking a vacuum. Various annealing temperatures were applied after Co and Ti were deposited; then, selective etching was applied to remove any un-reacted Co or Ti. The sheet resistance of the silicide was measured using a 4-point probe. Figure 5-1 presents the detail process flow.

Another experiment was done on ultra-high density integrated circuit wafers according

to the observation from above blanket wafers experiment. Ozone 1 minute and APM 3 minutes chemical treatments were selected to applied on 90nm CMOS devices. Shallow trench isolation (STI) was used with an active region width from 2000nm to 100nm, to evaluate the line width effect. N+ source/drain and P+ source/drain were fabricated by implanting arsenic/phosphorus and boron, respectively. Rapid thermal annealing (RTA) was then performed to activate the implanted species. After treatment with various chemicals, Ti /Co were sputtered, and RTA was conducted at a temperature of 500, 520 or 540°C. Subsequently, selective etching was used to remove un-reacted Ti; the samples were then annealed by 2nd RTA at 850°C for 30s. Lithography and etching were applied to define the contact layer after the inter-layer dielectric layer had been formed by chemical vapor deposition. Finally, copper metallization was performed.



5.3 Oxide Mediated Expitaxy Growth of Cobalt Silicide

The sheet resistance of silicided N+ and P+ blanket wafers was measured after the second RTA. Figure 5-2 plots the changes of the sheet resistance when different chemicals and the process time the process time for heavily doped N+ wafers. The sheet resistance changed significantly with the process time in ozone, but not in APM or HPM. When the process time was short (1min.) in ozone, the sheet resistance even exceeded that associated with a longer treatment time in APM/HPM. Ozone treatment is believed to generate a thicker

oxide film on N+ heavily doped wafers than on wafers treated with HPM/APM. Notably, the sheet resistance was not uniform after HPM treatment. Bardwell et al. also found that the uniformity of the oxide on the Si wafer was poor when the process time in HPM was short.[10] The poor oxide uniformity on the HPM-treated wafer resulted in the large variation for the sheet resistance. APM offered the lowest sheet resistance and best uniformity. Figure 5-3 shows the relationship between the sheet resistance and the chemicals used, and with the process time for the heavily doped P+ wafer. After chemical treatment, the sheet resistances differed less on the P+ wafer than on the heavily doped N+ one, that indicated the thickness of oxide produced on P+ are similar among different chemicals. This phenomena is consistent with the observation in previous study.[10] The X-xay diffraction patterns in Fig. 5-4 reveals the difference between the orientations of the samples that had and had not been treated with chemical oxide. Unlike the untreated sample, the wafer treated for 3minutes with APM exhibited only the $CoSi_2$ (111) orientation. This finding is consistent with that of a previous investigation.[11] The single orientation demonstrates the success of epitaxial $CoSi_2$ formation, also the smoothness of the $CoSi_2$ /Si interface.

5.4 Silicide Process Impact on Devices Performance

APM and ozone treatment were applied to the CMOS process to check their effects on the sheet resistance in the narrow active region, the specific contact resistance and the

junction leakage. The first RTA temperature for forming silicide was also studied to optimize OME process and to obtain uniform sheet resistance and low junction leakage. Figures 5-5(a) and 5-5(b) show the effect of 1 minute of ozone treatment on the sheet resistance of heavily doped N+ and P+ active regions, respectively. The sheet resistance is much higher on the N+ active region than on the P+ active region. This result is consistent with the observation of the blanket wafers. The thick chemical oxide on the N+ active region suppresses the formation of silicide, even at the first RTA temperature of 540°C. The lower sheet resistance on the narrower active region reveals that the oxide thickness is thinner at narrow active region. The retarded oxidation by compressive stress was reported by D. B. Kao.[12] The oxide thickness on active region around STI corner is thinner than planar area because of the compressive stress produced by STI. The oxide thinning at active region corner makes the oxide thickness thinner for small active region than large active region.

After APM treatment, the sheet resistance on the N+ active region is comparable with that of the P+ active region, as presented in Fig. 5-6(a) and Fig. 5-6(b). The saturation (Isat) and off (Ioff) current of the NMOS devices with a gate length of 0.1μm were measured to understand the impact of the formation of silicide on the electrical properties. Figure 5-7 shows that the Isat-Ioff curve was degraded by 4% when ozone-treated chemical oxide was applied. As the MOS shrinks to the sub-micron scale, the intrinsic parasitic series resistance substantially affects the speed of the device.[13] An important part of the parasitic series

resistance is the specific contact resistance. The specific contact resistance was measured on the modified Kelvin structure, as reported by Lynch, to confirm that the poor formation of silicide on the ozone-treated surface contributed to the degradation of the device.[14] Figure 5-8 clearly indicates that the poor specific contact resistance induced by the poor formation of silicide degrades the device.

Junction leakage control is also crucial for deep sub-micron CMOS devices, especially those used in low power applications. Figure 5-8 plots the junction leakage measured on the N-type STI edge intensive test pattern (periphery is about 6mm) with different applied voltage. Under 3.3 volts stress, the leakage current for APM 3min./540˚C RTA wafer is lower than that of ozone 1min./500˚C RTA wafer. The higher sheet resistance and the higher junction leakage of the 1 minute ozone-treated wafer indicate that the silicide/Si interface obtained by ozone treatment is rougher than that obtained by APM treatment. Figure 5-9 displays the TEM cross-sections of the N+ active regions on both APM and ozone treated wafers. The Si/silicide interface associated with the APM treatment process is clearly smoother than that of the ozone treatment process. The smooth interface provides better junction leakage performance and is very important to the manufacture of nano-scaled devices. Figure 11 shows the index for silicide selection. The multiple of sheet resistance and junction leakage current by 3.3 volts test was used as the index. Low sheet resistance and junction leakage current are both important factors for nano-scaled devices fabrication.

According to this index, the APM treatment process showed superior performance to the ozone treatment process for future deep sub-micron device need.

5.5 Conclusions

The effect of chemically treating the wafers on OME cobalt silicide was investigated. Different heavily doped Si surfaces were also considered. APM treatment provides the best control of the sheet resistance and junction leakage than other chemical treatments. Low sheet resistance and junction leakage current can be obtained by optimal chemical treatment and the use of an optimal RTA temperature.

Chapter 6

$CoSi_x$ Thermal Stability on Narrow Width Poly Silicon Resistors

6.1 Introduction

Cobalt silicide is widely used on polycrystalline Si (poly-Si) as low-resistance gate electrodes and local interconnects because 0.18-μm node cobalt silicide has low bulk resistivity (~18 μohm-cm), excellent chemical stability, and less line-width dependence compared to titanium silicide.[1-2] However, thermal stability is a concern for the application of cobalt silicide in actual devices. The thermal stability of silicide on poly-Si and its effect on device performance has been studied extensively.[3] In previous studies, the thermal stability of silicide via long-time or high-temperature thermal testing has been investigated[4-6] and some groups have used force-balance model to explain silicide agglomeration.[7-9] This study focuses on the effect of different line widths and dopant types on the thermal stability of poly-Si lines in 90-nm processes. It is found that the narrow poly-Si lines defined in 90-nm processes induce poor thermal stability and high sheet resistance. Both the line width and the doping type determine the thermal stability of narrow ploy-Si lines.

6.2 Experimental Procedures

Boron-doped, p-type Si wafers with resistivity of 10 Ω-cm and with an (001) orientation were used as substrates and 90-nm process was applied for this study. 100-μm-long poly-Si lines with line widths ranging from 2000 nm to 90 nm were fabricated to evaluate the thermal stability. N+ source/drain and P+ source/drain were formed by As/P and BF_2/B implant, respectively. Then spike rapid thermal annealing (RTA) was used to active the implant dose. After HF treatment, Ti capping (Co/Ti) materials were sputtered on silicon wafer followed by first RTA. Selective etching was performed after first RTA to remove un-reacted Ti and Co. Next, second RTA was performed with 850^{0}C/30s to form low-resistivity silicide. Lithography and dry etching were performed for contact layer definition after the inter-layer dielectric layer was deposited by chemical vapor deposition. Finally, copper metallization was performed. The sheet resistance of silicided N+ and P+ poly resistors with various line widths (see Chapter. 3) was measured by HP4071 semiconductor electrical parameters analyzer. Emission microscope (EMMI) was used for failure sites positioning and transmission electron microscope (TEM) was used to examine silicide thickness, poly-Si physical line width and agglomeration phenomenon.

6.3 Anomalous Sheet Resistance Change on Silicided Narrow Poly Resistors

In previous study, the thermal stability of silicide has usually been examined by

long-term thermal stress and analyzed by resistance variation.[5,10-12] These researches concluded that narrow line and large silicide grain degraded the thermal stability. Figure 1 shows the sheet-resistance variation of N+ and P+ poly-Si lines with different widths. These lines were fabricated by the Ti capping process. The larger sheet-resistance variation indicates poor thermal stability. It is usually thought that the narrower poly-Si line, the worse the thermal stability. In this study, the thermal behavior of all N+ poly resistors is consistent with the common result, as shown in Figure 1. However, the P+ poly resistors have anomalous behavior that contradicts common belief. P+ poly-Si lines fabricated by the Ti capping process and poly resistors with a line width of 130 nm have the largest variation in the sheet resistance, rather than the narrowest line. In order to verify the thermal behavior of P+ poly resistors, the second RTA with various temperatures and process times was investigated. Figure 2 displays the cumulative plots for the sheet resistance of P+ poly-Si lines. The spread of the sheet-resistance increases as the RTA temperature and process time increases. In particular, the sheet resistance increases by 4.5 ohm/sq for each jump for the P+ poly resistor processed by 850° C/120 s. EMMI images in the inset of Figure 2 show that one hot spot is found on the 4.6-ohm/sq-increased sample and two hot spots are found on the 8.9-ohm/sq-increased sample, indicating that the increase in the sheet resistance is determined by the number of disconnections that occurred on the narrow poly resistors. As the agglomeration mechanism studied in previous studies, the silicide agglomeration

happened during silicidation and left a vacancy behind. [6, 12] In Fig. 3, TEM plane view for the EMMI hot spot site shows a void formed across the whole poly line and the void size is about 75nm in longitude direction, so that results in the high sheet resistance. Figure 4 plots a schematic to explain the increase in the sheet resistance. The total sheet resistance increase by void (R) is the sum of 2 times of Rco and Rb, where Rco is the contact resistance between silicide and non-silicide poly-Si, and Rb is the resistance of non-silicided poly where the length is equivalent with the void.

$$R\frac{L}{w} = 2R_{co} + R_b \qquad (1)$$

where L is the length of the poly resistor (=100μm), w is the drawn width the poly resistor (=130nm). Due to crowding effect, the transfer length, l_t, can be calculated by following equation. [13]

$$l_t = \sqrt{\frac{\rho_c}{\rho_{sh}}} \qquad (2)$$

where ρ_c is the specific contact resistivity and ρ_{sh} is the sheet resistance for the non-silicided poly. The specific contact resistance (ρ_c) is 21 ohm-μm^2 and sheet resistance of non-silicide poly line drawn with 130nm (ρ_{sh}) is 820 ohm/sq, which can be obtained by

measuring on CBKR and non-silicided poly resistor, respectively. Transfer length(l_t) is 0.16 μm according to equation (2). Rco can be obtained as Rc can be obtained as

$$R_{co} = \frac{\rho_c}{l_t w_t} \quad (3)$$

where w_t is the actual width of poly line, which is 88nm obtained from Fig. 3. R_b can be obtained as,

$$R_b = \rho_{sh} \frac{S_v}{w} \quad (4)$$

By equation (1) –(4), the sheet resistance increased by the single void was obtained as 4.5 ohm/sq which is consistent with the observation in Figure 2. As shown in Figure 2, the void on 130-nm P+ poly resistors are almost as large as the line width and these voids have a similar size. These voids may lead to the stepped increase in the sheet resistance. The result is very different from that of the narrow N+ poly resistors. Figure 5 shows the cumulative plot for the sheet resistance of N+ poly resistors with different drawn widths. When the poly-Si line width shrinks to 90 nm, the spread of the sheet-resistance distribution for N+ poly resistors becomes worse. The TEM plane view of the 90-nm sample with high sheet

resistance is shown in Figure 6. Unlike the case in 130-nm P+ poly lines, the voids randomly distributed on the 90-nm N+ poly line are much smaller than the line width, resulting in a gradual increase in the sheet resistance, rather than a stepped increase as in the P+ poly lines.

6.4 The Relationship between Thermal Stability and Silicide Grain Size

The different void size that occurred on N+ and P+ poly resistors results in the different thermal behaviors that are related to the grain size on poly-Si lines. The TEM plane views of Figures 7(a)-(c) show the grain size distribution on N+ poly resistors with different widths. As shown in Figure 7(a), a large spread in the grain-size distribution is clearly observed on the 2000-nm drawn poly-Si line. The grain dimension ranges from 30 nm to 170 nm, with an average value of 100 nm. For the 130-nm drawn poly-Si line, the actual line width is about 83 nm. The grain distribution on this line is not a normal distribution like that on the 2000-nm-width poly line. The maximum grain size is constrained by the actual line width. The TEM plane view also shows that the grain size is as large as the line width and also shows the quasi-bamboo like microstructure, as can be seen in Figure 8. As the line width shrinks, the maximum grain size on narrow poly lines is limited by the line width and forms the quasi-bamboo microstructure where either a single grain or two grains coexist in the line width.[14] For the 90-nm drawn poly line, the maximum grain size is only about 50 nm, which is consistent with the actual line width. Figures 7(b) and 7(c) show that there are still

small portions of grains that smaller than the actual line width distributed around the line edge. The disappearing of these grains results in an increase in the sheet resistance, as can be seen in Fig. 6. The grain size of P-type poly resistors is shown in Figures 9(a)-(c). The grain-size distribution in 2000-nm drawn poly lines is similar to that in N-type poly lines. Broadening grain-size distribution is found and it ranges from 40 nm to 130 nm, with an average value of 80 nm. For the 130-nm drawn poly line, the actual width is about 88 nm. This is close to the mean grain size in the 2000-nm drawn poly line, where grain growth has no constraint. The grain-size distribution in the 130-nm drawn poly line ranges from 40 nm to about 80 nm. The majority is around 60 nm. As shown in Figure 3, the grain size similar to the line width is believed to leave a void behind while grains merge with each other during the thermal cycle. The grain size in the narrower poly line is further constrained when the line width is narrower than the unconstrained grain size. The 90-nm drawn P+ poly resistor thus results in similar thermal stability to the N-type poly line and does not show the similar thermal stability to the 130-nm drawn P type poly line because the less the grain boundary exists, the less the probability for Co/Si diffusion. The degradation of silicide is strongly affected by the silicide thickness and, for the same thickness, the microstructure of the silicide impacts thermal stability significantly. The underlying silicon substrate has the greatest influence on the microstructure of the silicide. Consequently, it influences the thermal stability of the silicide. The poly grain size for non-silicide N+ and P+ poly were

measured on blanket wafers. The grain sizes for N+ poly and P+ poly were about 120 nm and 78 nm, respectively. These sizes are similar to those of the formed silicide. A similar observation for the under-layer morphology was also made in previous research.[15] The dopants implanted in the poly-Si layer have a great influence on thermal stability property.[16,17]

6.5 Conclusions

The thermal stability of poly silicide formed on poly-Si lines with different widths and dopant types was investigated in this study. As was concluded in previous studies.[5,10-12] large silicide grain size and narrow poly width degrade the resistance to agglomeration and lead to poor thermal stability. In this study, the thermal behavior of silicide formed on N+ poly resistor agrees with that previous observation. However, a special digitalized sheet-resistance increase is observed on P+ poly resistors. The voids on the specific line width of P+ poly resistors result in this digitalized sheet-resistance increase. This anomalous thermal-stability change in the P+ poly resistors with different line widths is related to the grain size distribution and the actual poly line width. The substrate plays a significant role in the silicide grain size, which then impacts the thermal stability in the cobalt-silicide process.

Chapter 7

Quantitative Thermal Stability Study on Nano-scale Poly Silicide Resistors

7.1 Introduction

Silicides on polycrystalline Si (poly-Si) are widely used as low resistance gate electrode and local interconnections. Among all silicides, cobalt silicide ($CoSi_2$) is the most popular material beyond 0.25μm node because of less line-width-dependence effect than titanium silicide ($TiSi_2$). [1] However, the potential problem of $CoSi_2$ is the inferior thermal stability of silicided poly resistors compared to the resistor those use $TiSi_2$ and WSi_2. [2] Therefore, the thermal stability are extensively studied in previous researches.[3-9] Process related studies have proposed several theoretical models for the thermal stability of the silicided thin poly film. [10-13] These models are based on the assumption that agglomeration is caused by thermal grooving at grain boundaries. This reaction involves several steps, these are, the breaking of the $CoSi_2$ molecules close to the grain boundary, the migration of cobalt and silicon atoms, the reaction of the cobalt with the silicon atom and the epitaxial growth of silicon at the intersection of grain boundaries. These reaction steps indicate the importance of several factors in determining thermal stability, including thickness of the film, composition of the silicide and dimension of grains. In fact, the models predict that thicker films are more resistant to agglomeration and that films with smaller grains should agglomerate after long

thermal processes. However, all these models are more qualitative than quantitative. This study develops an equation for the thermal stability of silicide. This thermal stability equation predicted the weak points of the line width with a particular silicide thickness and material used. Through this thermal stability equation, an optimized silicide process can be designed to achieve the thermal stability requirement for different silicide processes.

7.2 Anomalous Thermal Stability for Silicided P+ Poly Resistors

The thermal stability of silicide has been commonly examined by long-term thermal stress and analyzed by resistance variation in previous studies.[14-16] Figure 7-1 shows the variation in sheet resistance of N+ and P+ poly-Si resistors with different drawn widths. A larger sheet resistance variation indicates worse thermal stability. A narrower silicided poly-Si line is generally corresponds to worse thermal stability. In this study, the thermal behavior of all N+ silicided poly-Si resistors is consistent with the commonly recognized result plotted in Fig. 7-1. However, the P+ silicided poly-Si resistors exhibit anomalous behavior that is not the same as common believes. The P+ silicided poly-Si resistor with a drawn line width of 130 nm, and not the one with the narrowest line, exhibited the largest variation in sheet resistance.. The activation energy of silicided poly-Si resistors with different widths was studied afterward to verify this anomalous thermal stability behavior.

7.3 Activation Energy Extraction

Extra thermal cycles at different temperatures and various times were applied to silicided poly-Si resistors after the silicide was formed (2nd RTA) to investigate the activation energy. The sheet resistance of silicided poly-Si resistor for different doping types and different line width were measured after the extra thermal cycles. Figure 7.2 plots the increase in sheet resistance of the 2000nm silicided P+ poly-Si resistors and reported the percentage increase with temperature of the extra thermal cycles. The slopes of the linear fits increased with the anneal temperature and the incubation time. The agglomeration time was extracted from Fig. 7-2 based on a definition that sheet resistance increased by 500% (5X). Different definitions for agglomeration were as also checked, for example, 700% of sheet resistance increase, the results were kept the same. The agglomeration time, which is the time to increase the sheet resistance 500%, obtained from a plot of 1/kT, (Fig. 7-3) the activation energy of the agglomeration process could be obtained. The activation energy was 5.235 eV for 2000nm wide silicided P+ poly-Si resistor. This number is similar to that obtained for the blanket film in the previous research. [17] Figure 7.4 plots the activation energy for silicided poly-Si resistors, with different doping types and drawn widths, extracted by the same method. The activation energy for the 2000nm N+ poly resistor was 3.49 eV, which is also similar to that obtained in previous study. [17] The activation for silicided N+ poly-Si resistors was lower than that of P+ poly. The previous study explained this behavior by the

presence of a high concentration of As at the grain boundary. [18] The high concentration of As at grain boundary can reduce the energy needed to break the cobalt silicide molecule and the energy necessary for the reaction at the interface. Besides, for the silicided P+ poly-Si resistor, the presence of fluorine at the $CoSi_2$/Si interface increases the energy required for the reaction at the silicide/silicon interface, and thus increases the thermal stability. [19-20] The activation energy determines the thermal stability. Figure 7.4 plots the thermal stability for narrow silicided poly-Si resistors. Intuitively, a wider line should correspond to easier silicide formation, and therefore, better thermal stability. However, it was not the observation in this study. In Fig. 7-4, neither the activation energy for N+ and P+ silicided poly resistors was reduced as the line width decreased. To the author's knowledge, this anomalous activation degradation behavior has never been reported. The reverse points for silicided N+ poly-si resistor and silicided P+ poly-Si resistor were around 180nm and 130nm, respectively.

7.4 The Physical Dimensions Effect on Thermal Stability

The relationship between the thickness of silicide and width of the poly line width was studied by TEM to understand the thermal stability of the silicide formed on a narrow poly-Si line. Figure 7-5 presents the definition of dimensions related to silicide formation, where w is the width of silicided line; t is the thickness of the silicide and the poly-Si exposed above spacer, and s is the spacer top-loss. The thickness of cobalt sputtered on the poly-Si line and

the rapid thermal process temperature for formation of silicide are key factors to determine the silicide thickness on poly-Si line. However, the top loss is also important for determining the silicide thickness on poly-Si resistors. Silicide was formed on poly-Si resistors with different top losses (s = 30nm–60nm) by adjusting the spacer etching. After the formation of silicide, contact definition and metallization, the sheet resistance of samples which with different top-loss were measured on different width of poly resistors. As the sheet resistance changes shown in Fig. 7-6, the sheet resistance significant increased for narrow poly line when the top loss was small. The TEM cross-section shown in Fig. 7-7 reveals the small top loss on the narrow poly line induced the formation of thin silicide, resulting in a high sheet resistance. The silicide formed on the center of poly line was thicker than that on the edge of poly line (at the interface between the spacer and the poly line), revealing that the smaller top-loss confined the formation of silicide especially when the poly line was narrow. Other than the thickness sputtered cobalt, the rapid thermal process temperature and the spacer top loss, the morphology of the under layer [3] and the dopant implanted in the polysilicon layer[4,5] also importantly determine for the thickness of silicide.

7.5 Derivation of the Thermal Stability Equation

However, the combination of the poly line width, the silicide thickness and the substrate effect make the predicting the thermal stability difficult because the thermal stability is not

simply proportional to the width of the poly line. The above study of the degradation of activation energy indicates that thermal stability of silicided P+ poly-Si resistor was worst when the drawn line was 130nm wide, and the actual width was 83nm, according to the cross section obtained by TEM. This number was consistent with the critical grain size for the worst thermal stability in Fig. 7-1. Nolan et al. also investigated the critical grain size (Lc) for thermal stability. [11] Considered the possibility of voids on a silicided narrow poly line, the index was set to w/ Lc. This number is not smaller than one because there was at least one grain on the narrow poly line, and it is also not larger than three because of the probability that a void presents around one grain is the same when the line width is three times larger than the critical grain size. Table 7-1 and 7-2 list w,t values for silicided P+ and N+ poly-Si resistors, respectively. The silicided line-width is proportional to and less than the drawn line width because of the etching bias of poly dry etching. The thickness of silicide increases as the line-width decreases, however it is not a proportional increase. All above qualitative statements have been quantified by the relationship between thermal stability and factors studied in this work (silicide thickness, line width and critical grain size). During agglomeration, vacancies migrate and accumulate at the interface, separating two silicide grains, leaving vacancies behind. [21-24] The vacancies remain in silicide block the electrical current and significantly increase the sheet resistance of silicided poly line. The thermal stability (Q) is proportional to the activation energy (Ea), and so is inversely proportional to

the ratio that the cross section occupied by vacancies (V/A), where V is the number of vacancies accumulated at the interface and A is the cross section of the grain boundary. The number of vacancies that can migrate and accumulate at the interface is proportional to the diffusion rate through the grain boundary, which is inversely proportional to the thickness of silicide. [25] The thermal stability equation can thus be written as

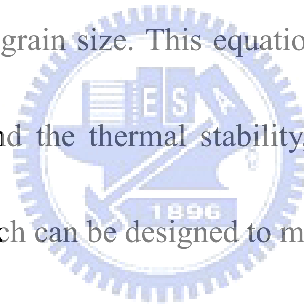
$$Q \propto Ea \propto \left(\frac{V}{A}\right)^{-1} \propto \left[\left(\frac{1}{t}\right) / \left(\frac{w}{Lc} \times t\right)\right]^{-1} = C \times \frac{w}{Lc} \times t^2 \quad (1)$$

where w and t are as shown in Fig. 7-5, and C is a constant that is related to the substrate underneath the silicide. By substituting the line width, critical grain size and silicide thickness of the P+ poly-Si resistors into the thermal stability equation yields the weakest point at which the thermal stability is the worst when w=130 nm. This point is at about 180nm for N+ poly-Si resistors, as presented in Fig. 7-8. Thermal stability index is strongly correlated with the activation energy (Fig. 7-9). The slope in Fig.7-9 represented the substrate factors, as mentioned in Eq.1. The index of the thermal stability of the silicide can be extracted and the silicide process can be designed to maximize the thermal stability.

7.6 Conclusions

The thermal stability of both silicided N+ and P+ poly-Si resistors was studied by

extracting the activation energy for agglomeration. Anomalous degradation behavior was investigated and the factors that govern this phenomenon were also reported. The silicide thickness and the line width of the silicided narrow poly-Si resistors critically influence the thermal stability of the silicide. The sputter thickness of cobalt, the rapid thermal process temperature, the spacer top loss, the morphology of the under-layer and the dopant implanted in the polysilicon layer also importantly determine the silicide thickness. Other than thickness of silicide, the size distribution of the silicide grains also greatly affects the thermal stability of silicided narrow poly-Si resistors. An equation for thermal stability was derived in terms of thickness, line width and critical grain size. This equation demonstrates a strong correlation between the activation energy and the thermal stability, also extracts the thermal stability index for the silicide process, which can be designed to maximize the thermal stability.



Chapter 8

Conclusions and Suggestions for Future Studies

8.1 Conclusions for This Thesis

Cobalt silicide($CoSi_2$) has become one of the most promising candidates for silicide technology application. $CoSi_2$ is used for source/drain and gate in nano-scaled CMOS devices, because of its low sheet resistance, low contact resistance and high compatibility with the ULSI process. However, as the devices are shrunk to the nano-scale, issue of process control and its effect on silicide profile, the roughness of $CoSi_x$/Si interface and the thermal stability have been raised from sheet resistance, junction leakage and device reliability view points.

In this thesis, cobalt silicide was applied to a nano-scale CMOS process. The source/drain area, activation area resistors and poly-Si resistors were formed with cobalt silicide. The behaviors of silicide on CMOS devices and resistors were studied. The formation of $CoSi_2$ can fulfill the 90nm process requirements if the optimized capping material and oxide-mediated epitaxy are applied. Furthermore, the thermal stability of the nano-scaled silicided poly-Si resistors was quantified. The following important conclusions are drawn.

(1) The selection of the capping material is very important in determining the formation of cobalt silicide. The TiN capping and Ti capping processes were responsible for

the very different resistivity on narrow active region resistors. A high compressive stress at the STI and active region interface enhanced the formation of silicide in the TiN capping process. The deep-penetrated silicide profile at active region in TiN capping process induced the anomalous width-dependent change in sheet resistance. This penetration profile of silicide in TiN capping process also resulted in the anomalous junction leakage, as compared to the junction leakage performance in Ti capping process. The Ti capping process yielded a better junction leakage performance than the TiN capping process.

(2) Chapter 5 presented the benefits of the OME cobalt silicide. A smooth $CoSi_2$/Si interface can be obtained by implementing this OME process. The chemical oxide layer formed on Si surfaces heavily doped with N+ was thicker than that on surfaces heavily doped P+. Balancing the formation of silicide in both N+ and P+ area is very important. Chemical oxide growth using different chemicals was also studied. Of all tested treatment, APM treatment provided the best control of the sheet resistance and junction leakage. A low sheet resistance and low junction leakage current can be obtained by using optimal chemical treatment and optimal RTA temperature.

(3) Resistors with various dopants exhibited different behaviors on thermal stability. The anomalous thermal stability change of the narrow silicided P+ poly-Si resistors is related to the distribution of grain sizes and the actual width of the poly line. The substrate significantly influences the size of silicide grain, and so influences the thermal stability of

cobalt silicide. In this study, the thermal behavior of the silicide formed on N+ poly resistor is consistent with the observation of previous works that large silicide grain size and narrow poly lines degrade the resistance to agglomeration and thus result in poor thermal stability. However, a special digitalized step increase in sheet resistance was observed on P+ poly resistors. The voids in silicided P+ poly-Si resistor with a particular width resulted in this digitalized step increase in sheet resistance. This anomalous variation reflected to the thermal stability, and can be explained by the correlation between the line width of poly-Si resistors and the distribution of grain sizes. The substrate also significantly affects the size of silicide grains, thus influences impact the thermal stability of cobalt silicide.

(4) The thermal stability for both silicided N+ and P+ poly resistors was studied by extracting the activation energy for agglomeration. The thickness of silicide and the line width of the narrow poly resistors critically influenced the thermal stability of the silicide. The thickness of the sputtered cobalt, the temperature of rapid thermal process, the spacer top loss, the morphology of the under layer and the dopant implanted in the polysilicon layer also importantly affected the thickness of the silicide. The distribution of the silicide grain sizes significantly determined the thermal stability of the silicide. An equation for thermal stability was derived in terms of thickness, line width and critical grain size. This equation demonstrates a strong correlation between the activation energy and the thermal stability, also extracts the thermal stability index for the silicide process, which can be designed to

maximize the thermal stability.

8.2 Suggestions for Future Studies

As 65 nm technology nodes and smaller are developed, cobalt silicide is increasingly replaced with nickel mono-silicide (NiSi). The NiSi has several technological advantages, including low sheet resistivity, line-width independent, low Si consumption, potential to provide less junction leakage, low thermal budget for formation, and compatibility with silicon germanium ($Si_{1-x}Ge_x$) substrate technology.[1-4] Orthorhombic NiSi is an attractive alternative to the silicides, $TiSi_2$ and $COSi_2$, currently utilized in Si device fabrication. However, NiSi has been reported to agglomerate at temperatures as low as 600° C [5,6] and phase transformation to the high resistivity CaF_2 structure $NiSi_2$ occurs at temperatures of 750 ^{o} C and above.[7] Moreover, the abnormal oxidation of the NiSi on the As-doped source/drain has also been reported,[8] and this degrades the silicide and causes the anomalous junction leakage current.[9]

Recent studies have suggested preliminary approaches to solving the problems mentioned above. Additional impurities, such as Ti, Co, Pt and Pd have been proven to increase the thermal stability of NiSi. [10-14] Some works has tried to use TiN capping and N2 gas during the deposition of Ni to retard abnormal oxidation. [15] Further investigations of process-integration must be conducted NiSi can be applied on sub-50nm ULSI devices.

Therefore, the projected future works for silicide application on ULSI process can be listed as follows.

(1) Adding impurities can increase the thermal stability of NiSi. However, the impacts of impurities on the integrity of the NiSi shallow junctions and the thin gate electrode need to be investigated by different layout of ULSI devices. The optimal temperature for silicide formation and the un-reacted metal removal must be investigated.

(2) The impact of STI stress on the formation of NiSi and the silicide profile must be examined. The junction leakage performance should be also studied.

(3) The selection of capping material for the formation of NiSi should be studied. The thermal stability and oxidation behaviors must be verified.

(4) The thermal stability on narrow poly lines, which silicided with NiSi, should be checked. A quantitative study of the thermal stability and the effects of thickness, line width and critical grain size on NiSi narrow lines. Derive the thermal stability index for NiSi.

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