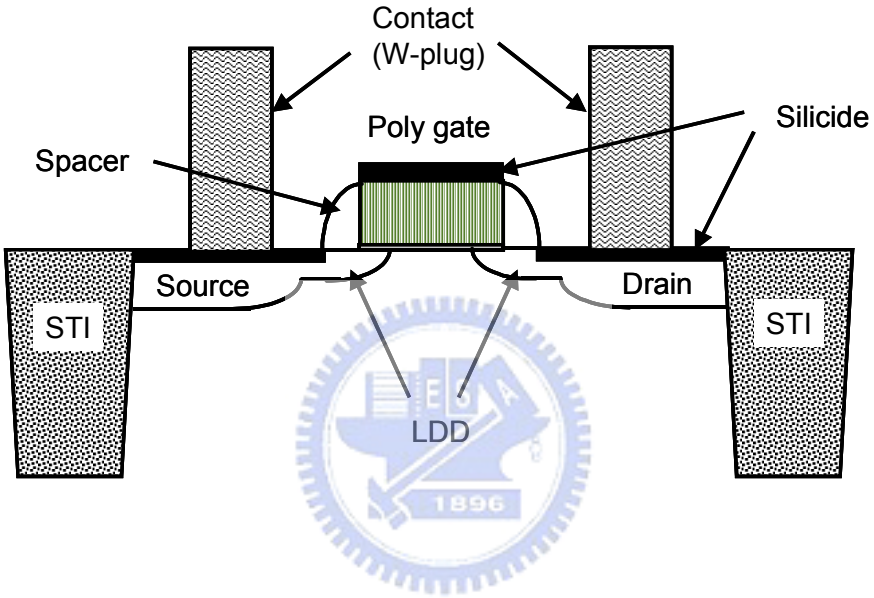

Fig. 1-1 : Schematic cross section for nano-scaled metal-oxide-filed-effect-transistor (MOSFET)

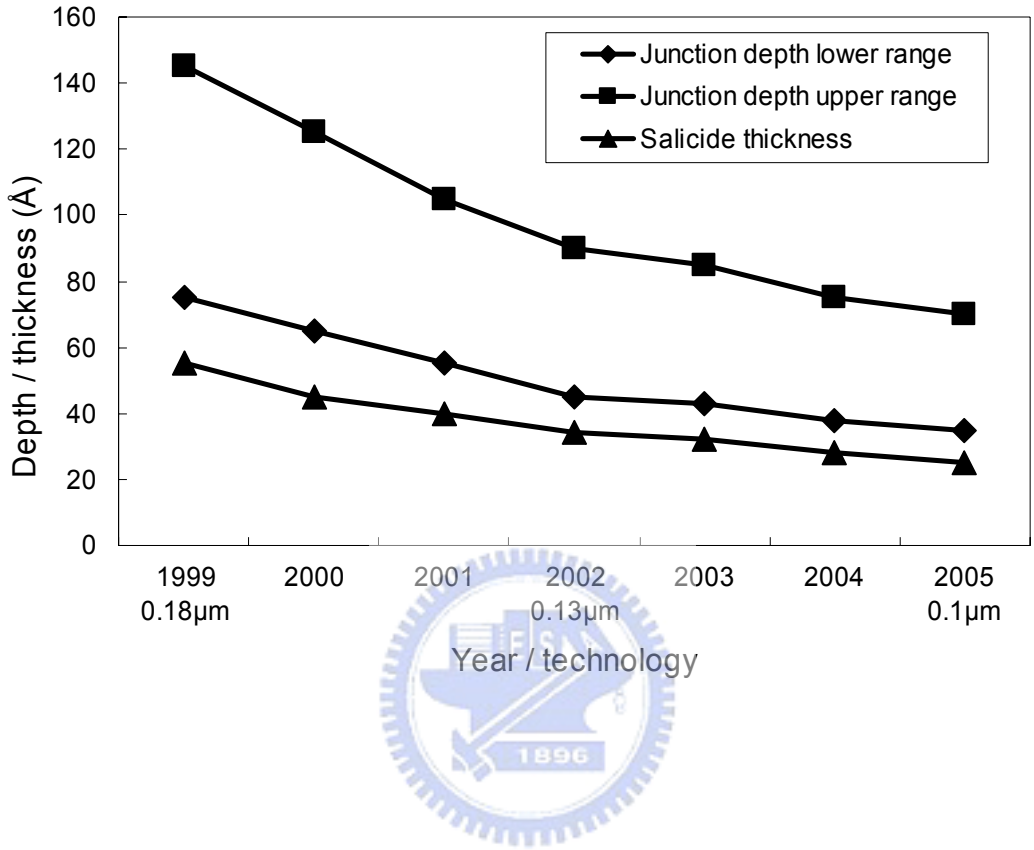

Fig. 1-2 : Silicide thickness requirement for different ULSI generations

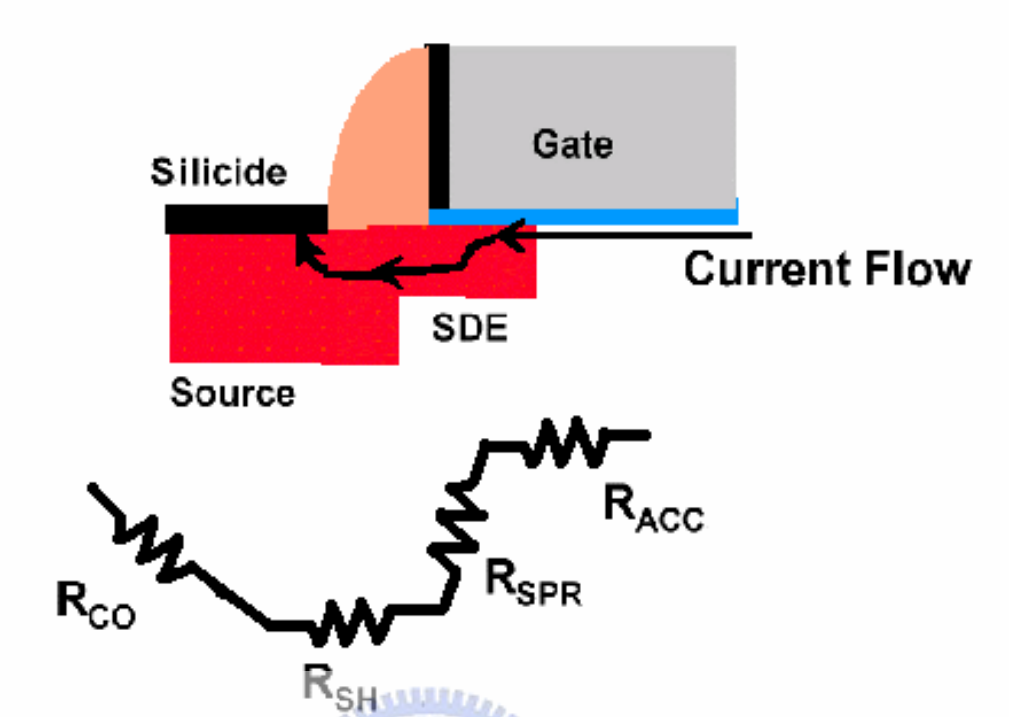

Fig. 1-3 : Major contributors for series resistance of CMOS device

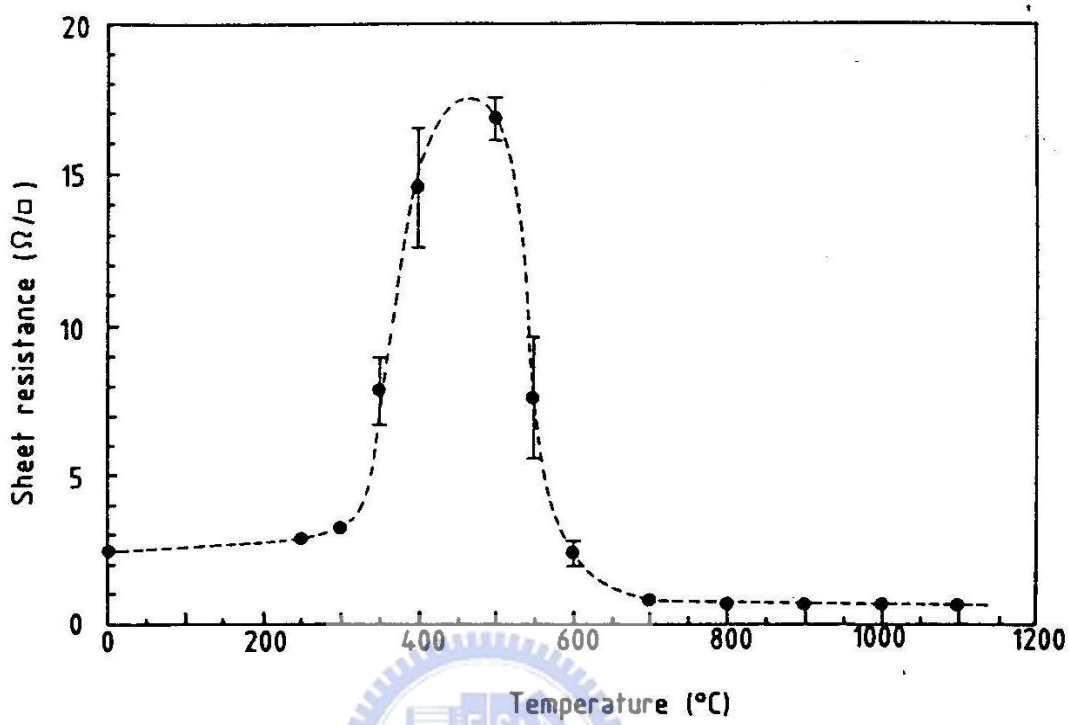

Fig. 2-1 : Sheet resistance as a function of reaction temperature during RTA

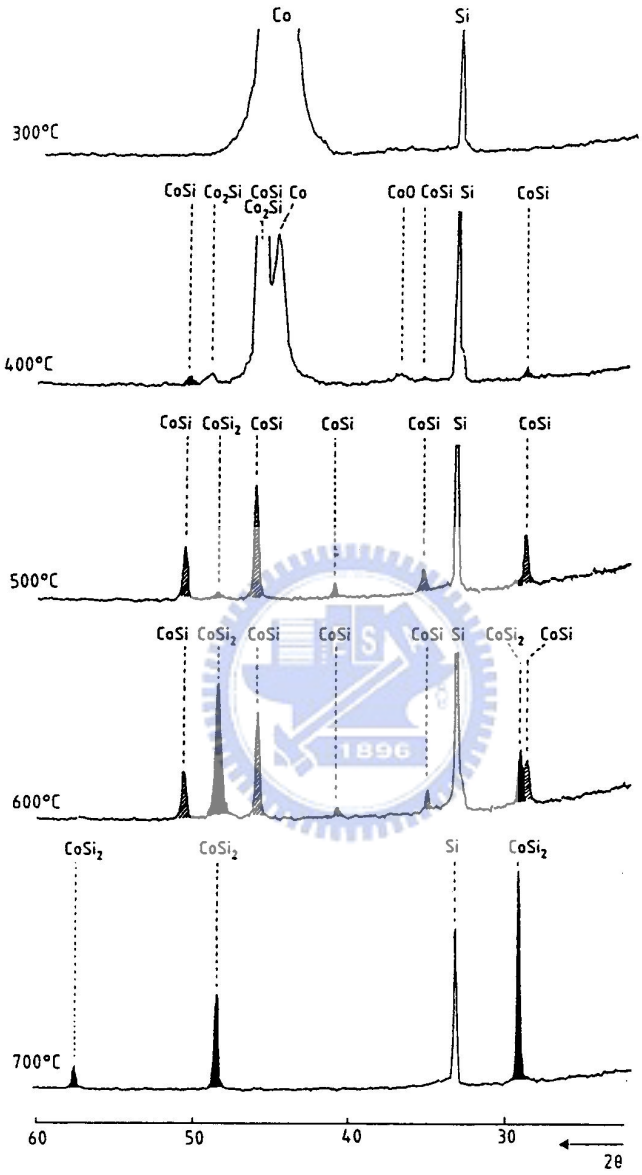

Fig. 2-2 : X-ray diffraction spectra for Co on Si after RTA at various temperature

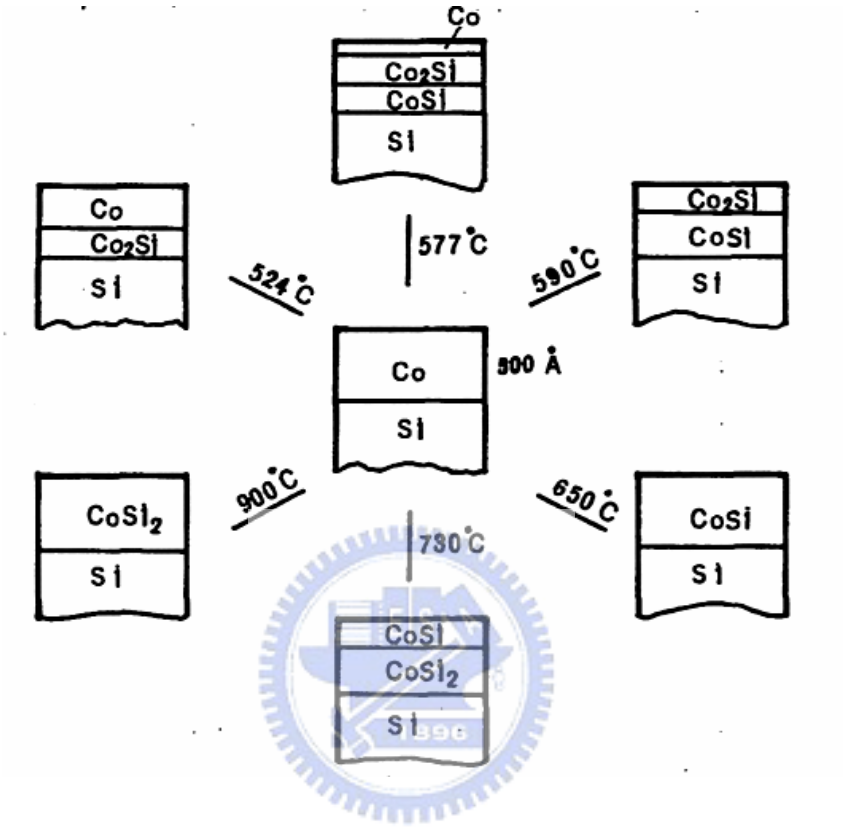

Fig. 2-3 : Schematic of the silicides formed after annealing at various temperatures during RTA

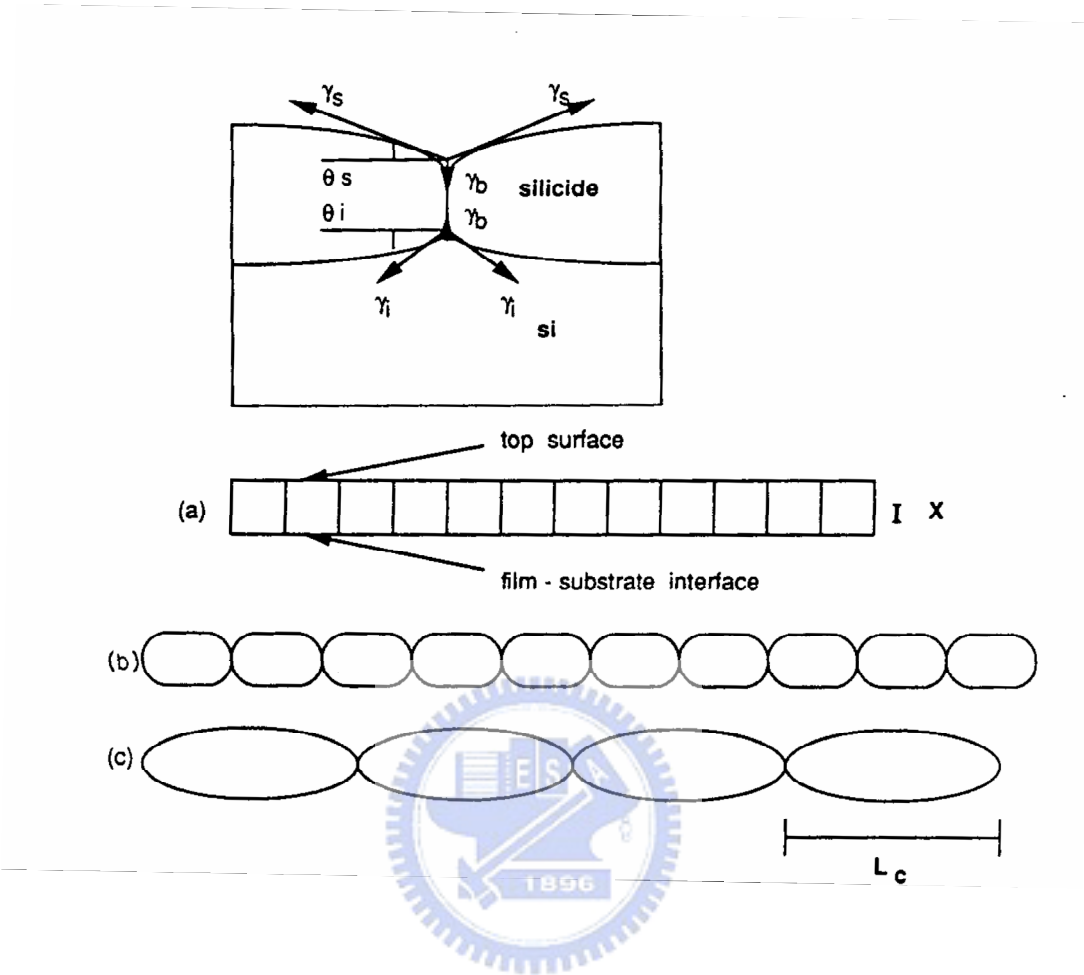

Fig. 2-4 : Mechanism for thermal grooving (a) Energy balances at the grain boundary grooves and (b) schematic cross-sectional view of the evolution thermal grooving of a thin silicide layer (c) the critical size (Lc) for agglomeration

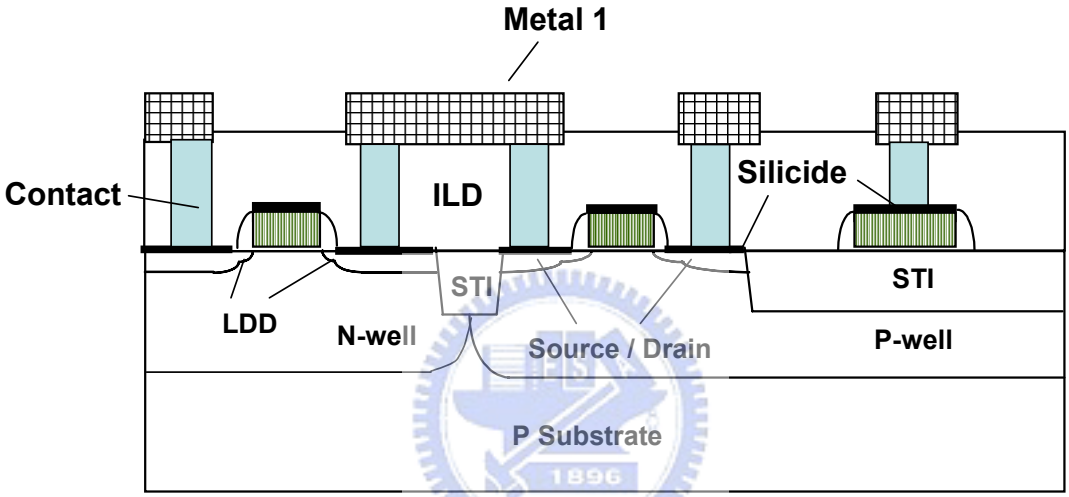

Fig. 3-1 : Cross section for advanced nano-scaled ULSI circuit

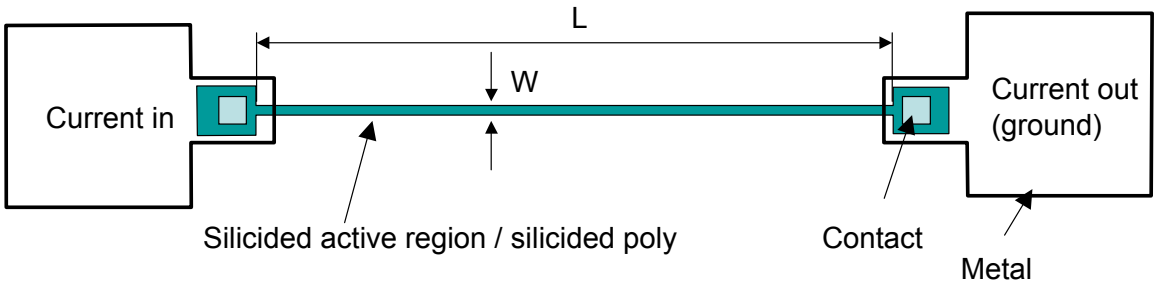

Fig. 3-2 : Schematic plan view for two-terminals resistor

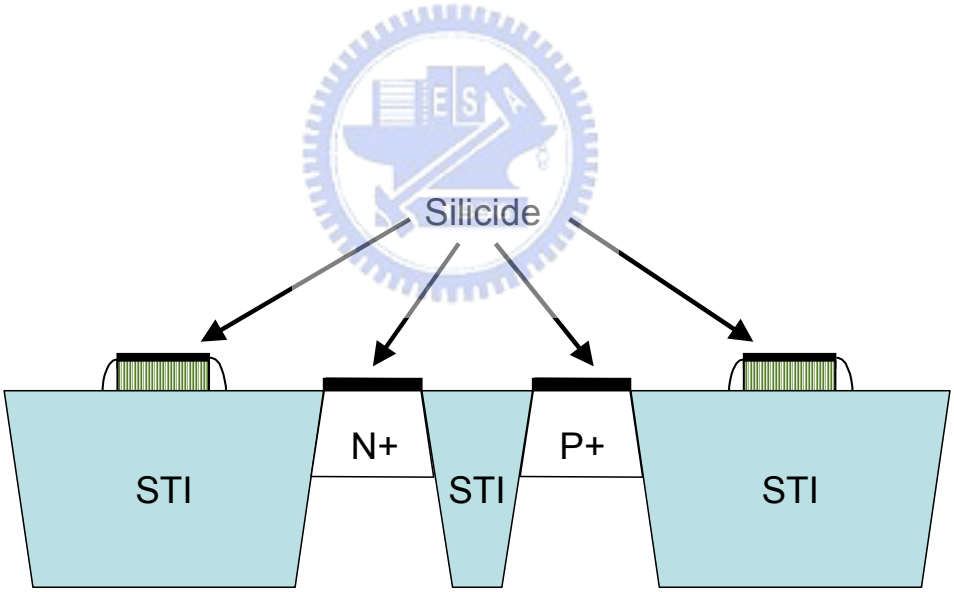

Fig. 3-3 : Schematic cross-section for the 2-terminals resistors, from left to right are N+ poly, N+ active region, P+ active region and P+ poly

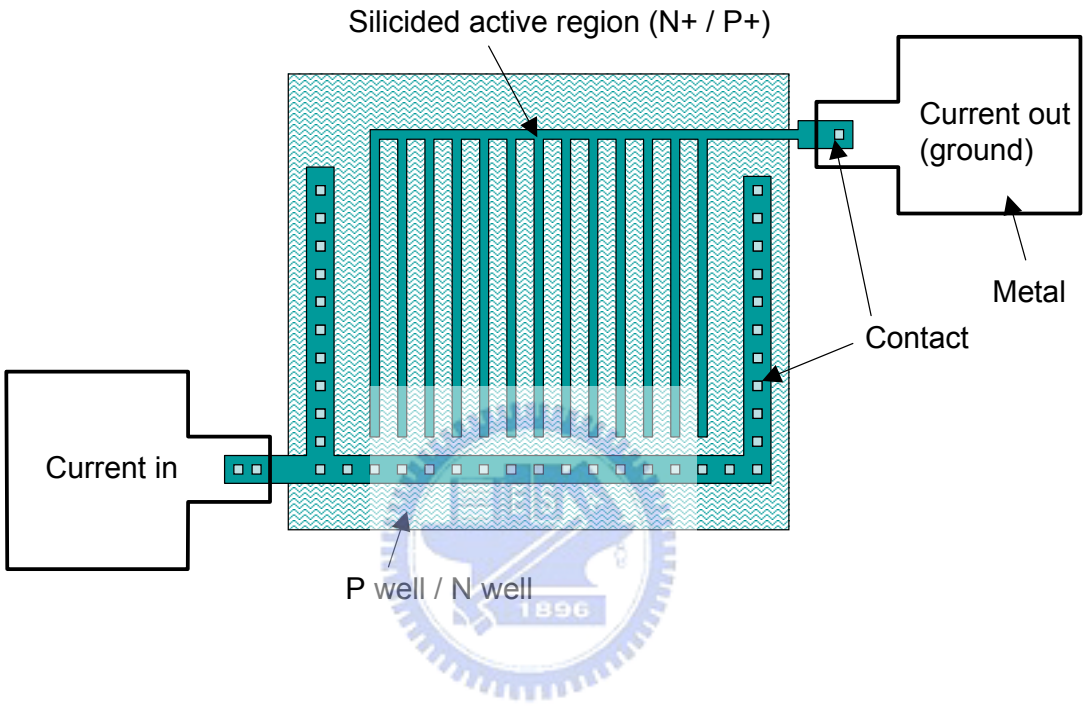

Fig. 3-4 : Schematic plan view for the perimeter-intensive diodes

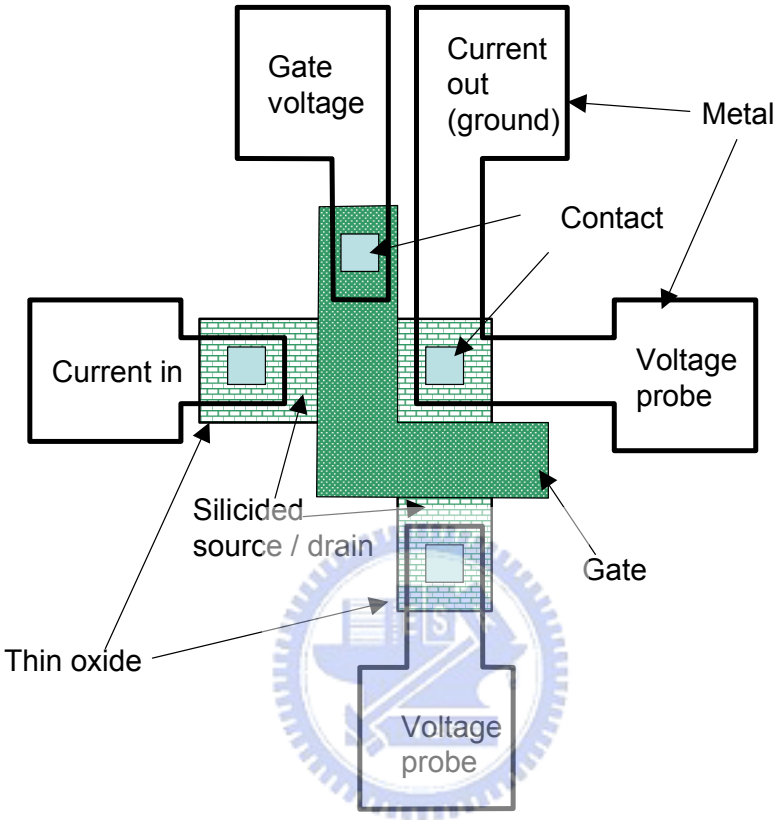

Fig. 3-5 : Schematic plan view for the cross-bridge Kelvin resistor (CBKR)

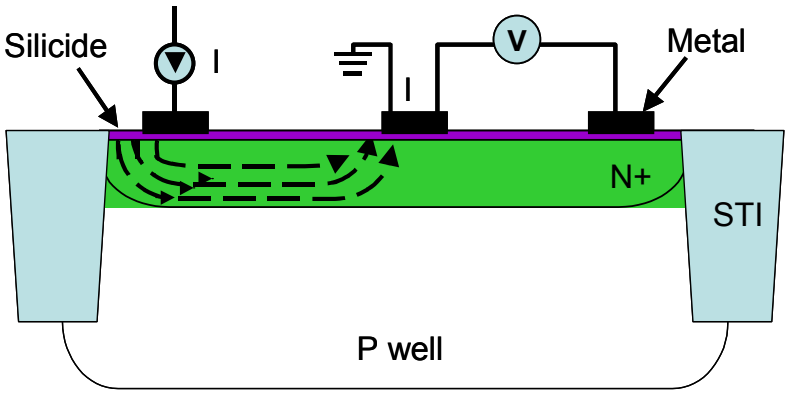

Fig. 3-6 : Schematic cross section for conventional Kelvin resistor

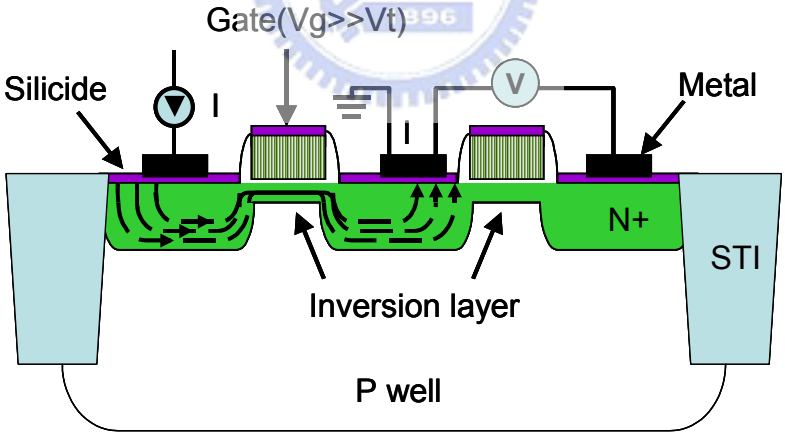

Fig. 3-7 : Schematic cross section for cross bridge Kelvin resistor

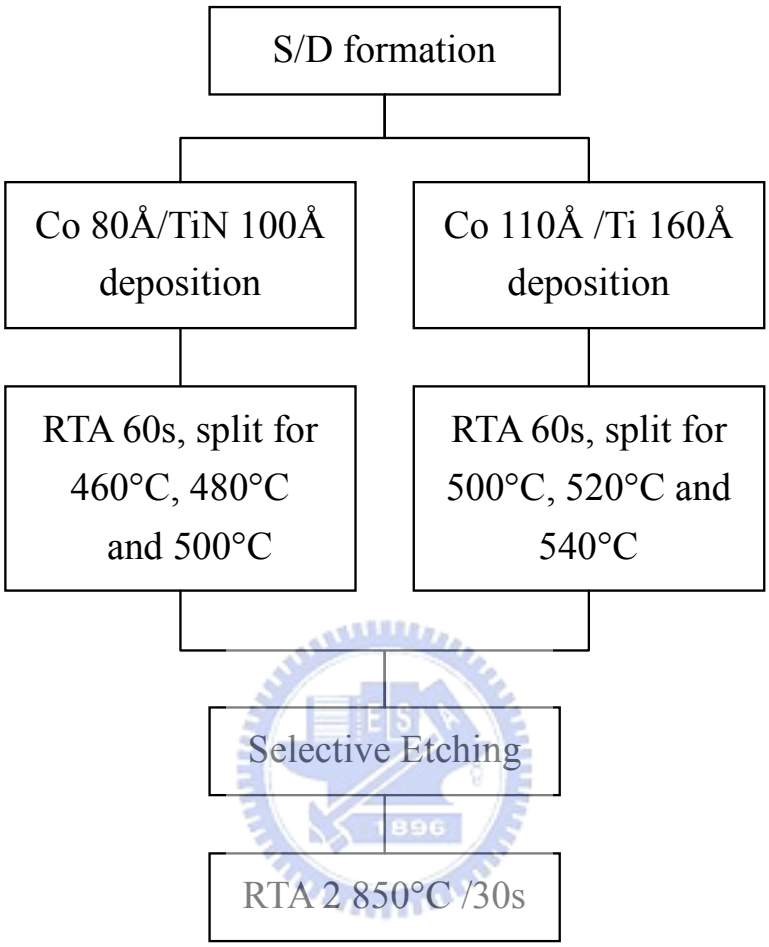

Fig. 4-1 : Experimental procedure detail

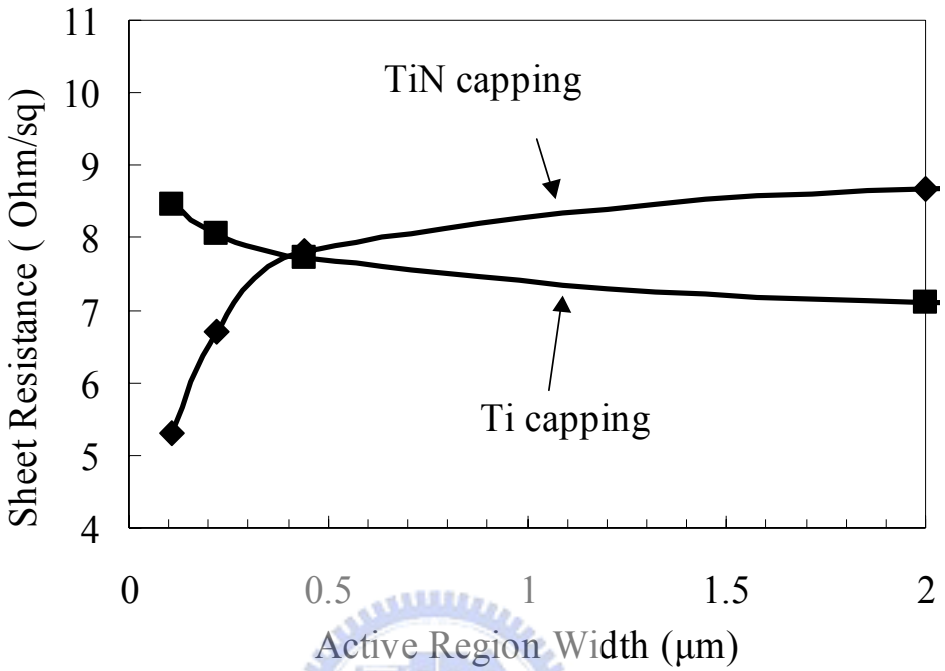

Fig. 4-2 : Sheet resistance change comparison between Ti capping and TiN capping cobalt silicide process along different active width

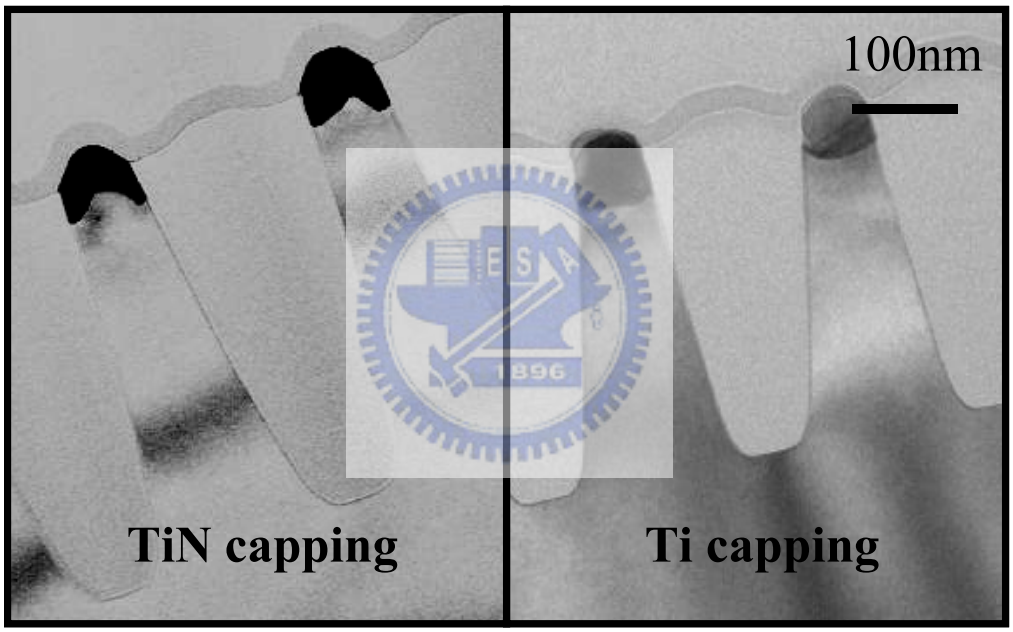

Fig .4-3 : The TEM cross section for TiN capping and Ti capping cobalt silicide

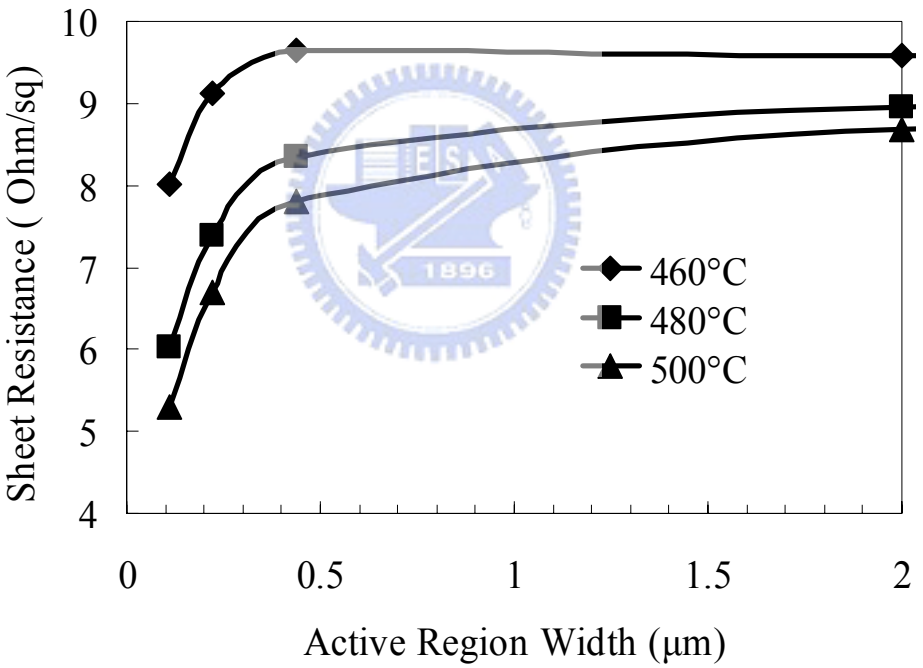

Fig. 4-4(a) : First RTA temperature effect on TiN capping process

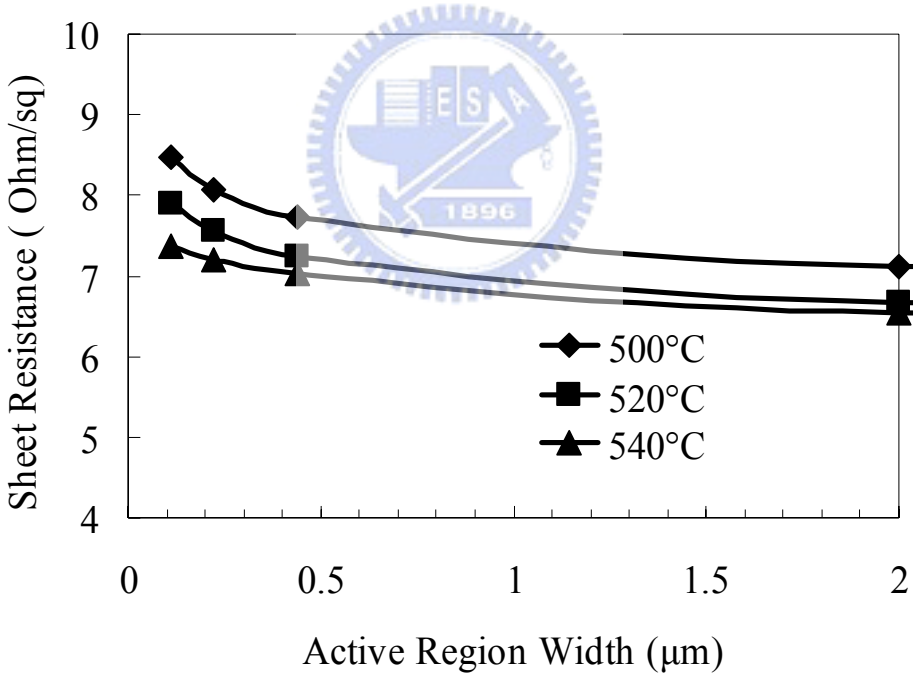

Fig. 4-4(b) : First RTA temperature effect on Ti capping process

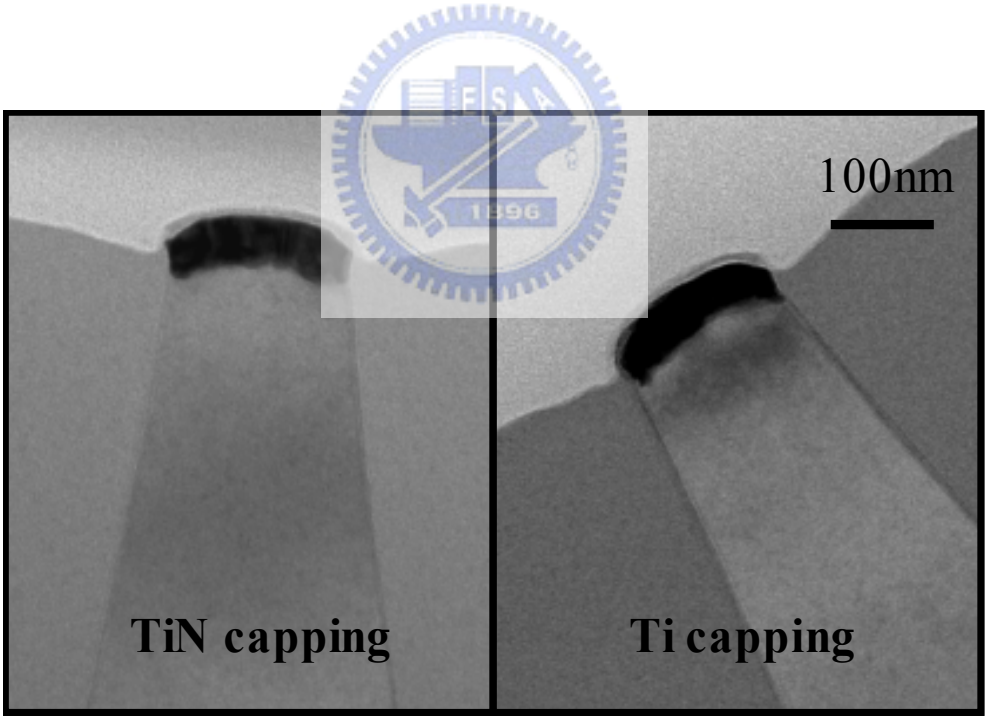

Fig. 4-5 : TEM cross section for TiN capping and Ti capping cobalt silicide after first RTA

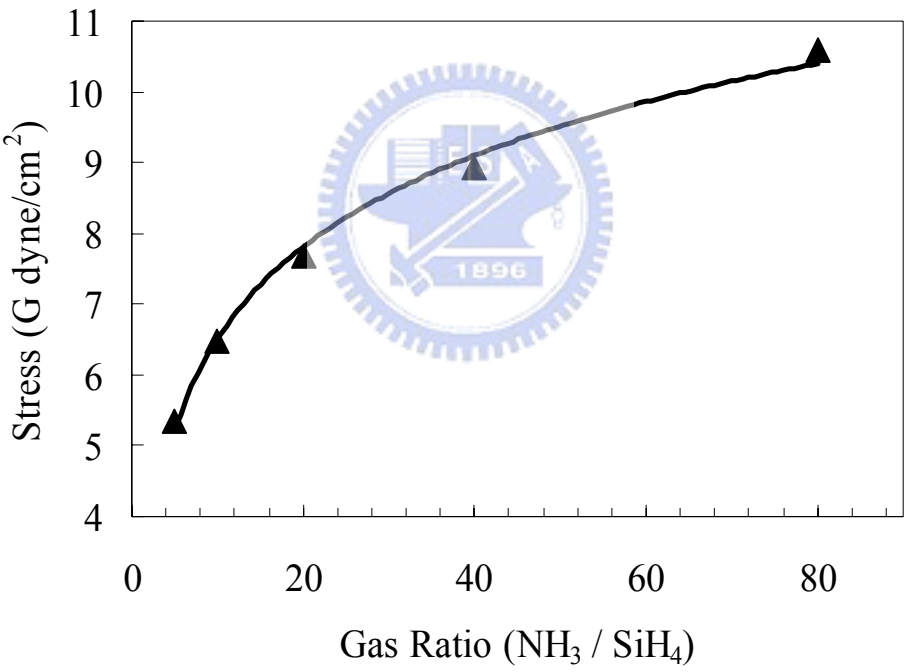

Fig. 4-6 : Si_3N_4 film stress adjustment

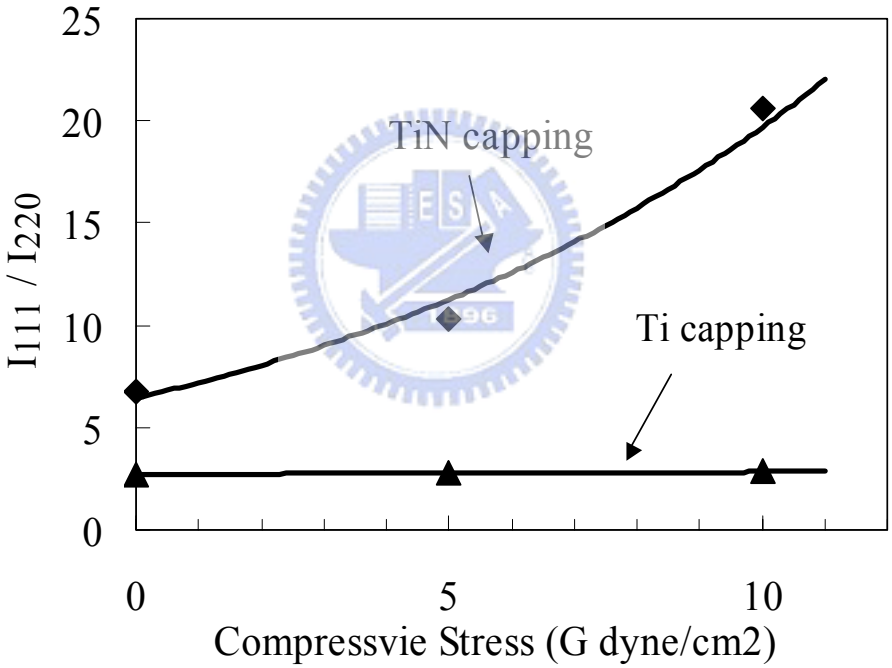

Fig. 4-7 : Orientation intensity change by backside film stress

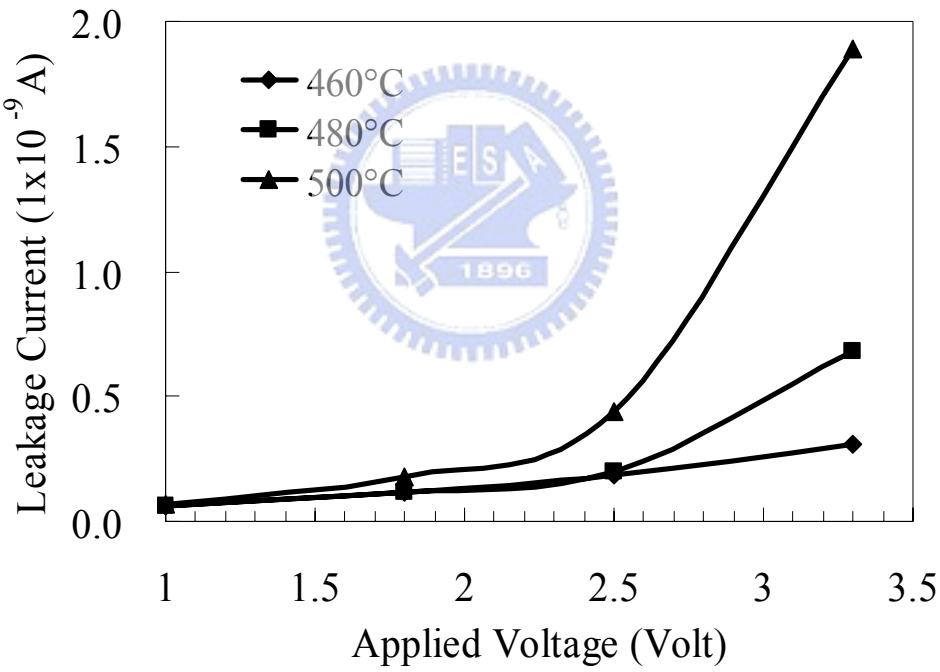

Fig. 4-8(a) : The junction leakage current for TiN capping process

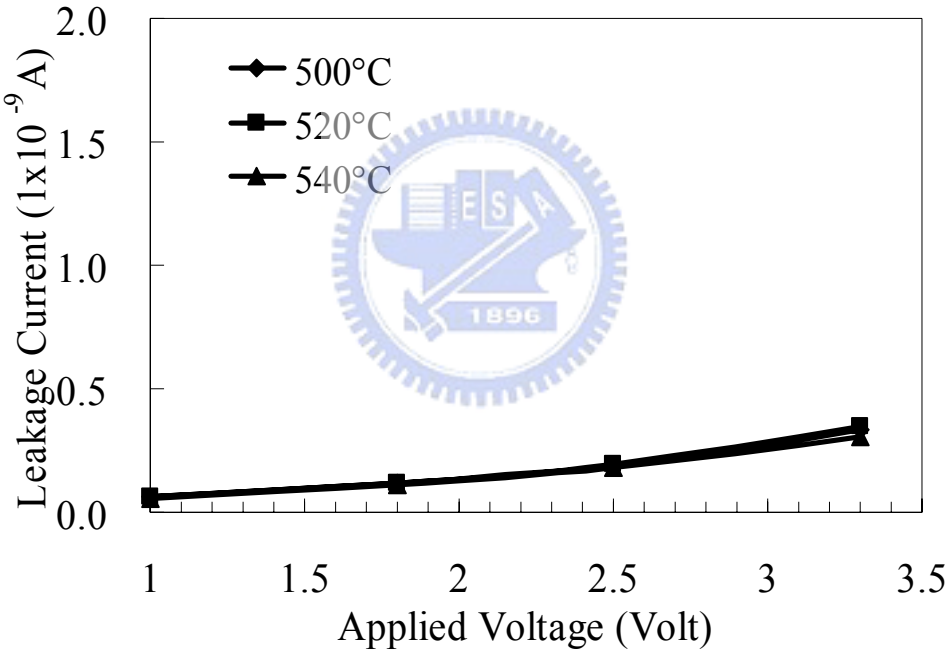

Fig. 4-8(b) : The junction leakage current for Ti capping process

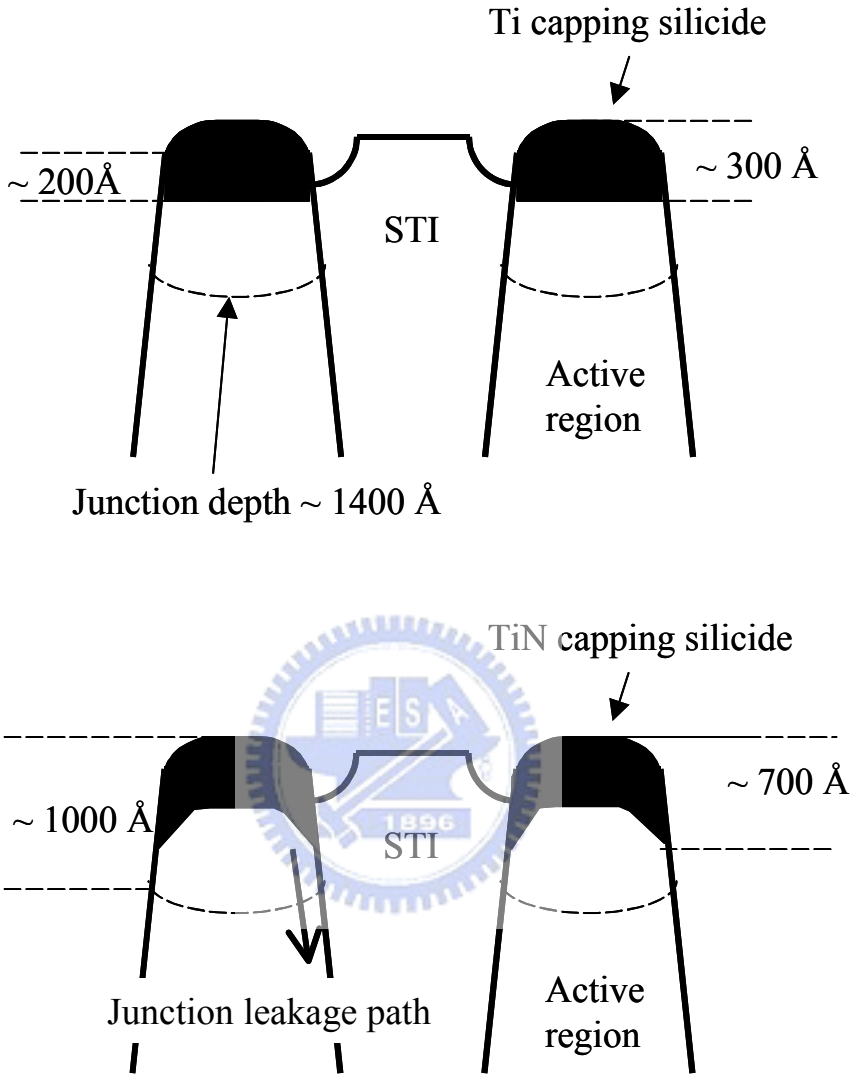

Fig. 4-9 : Illustration for the junction leakage current path comparison between TiN and Ti capping cobalt silicide

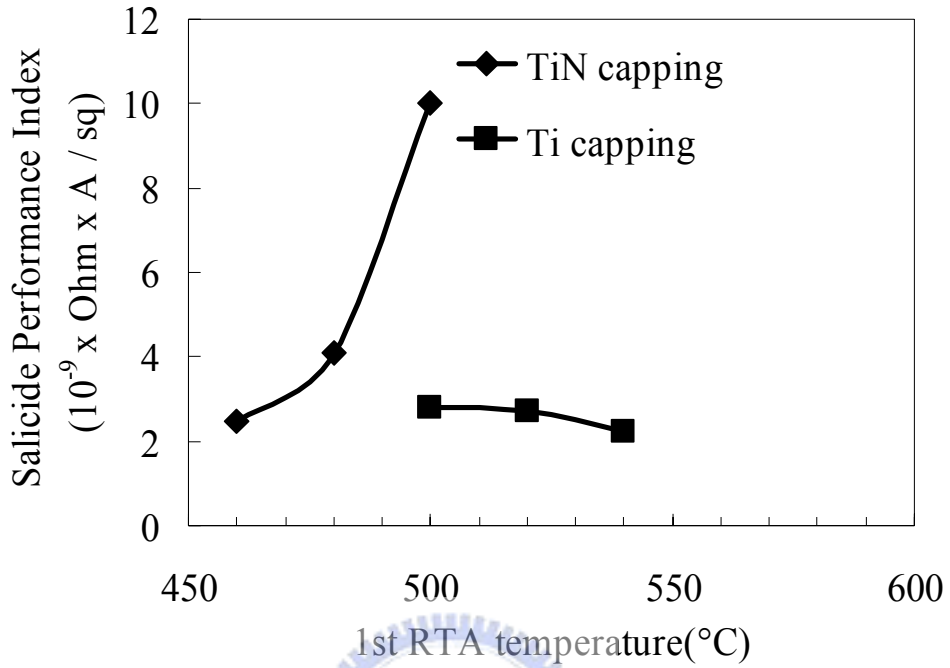

Fig. 4-10 : Silicide performance index comparison between TiN capping and Ti capping processes

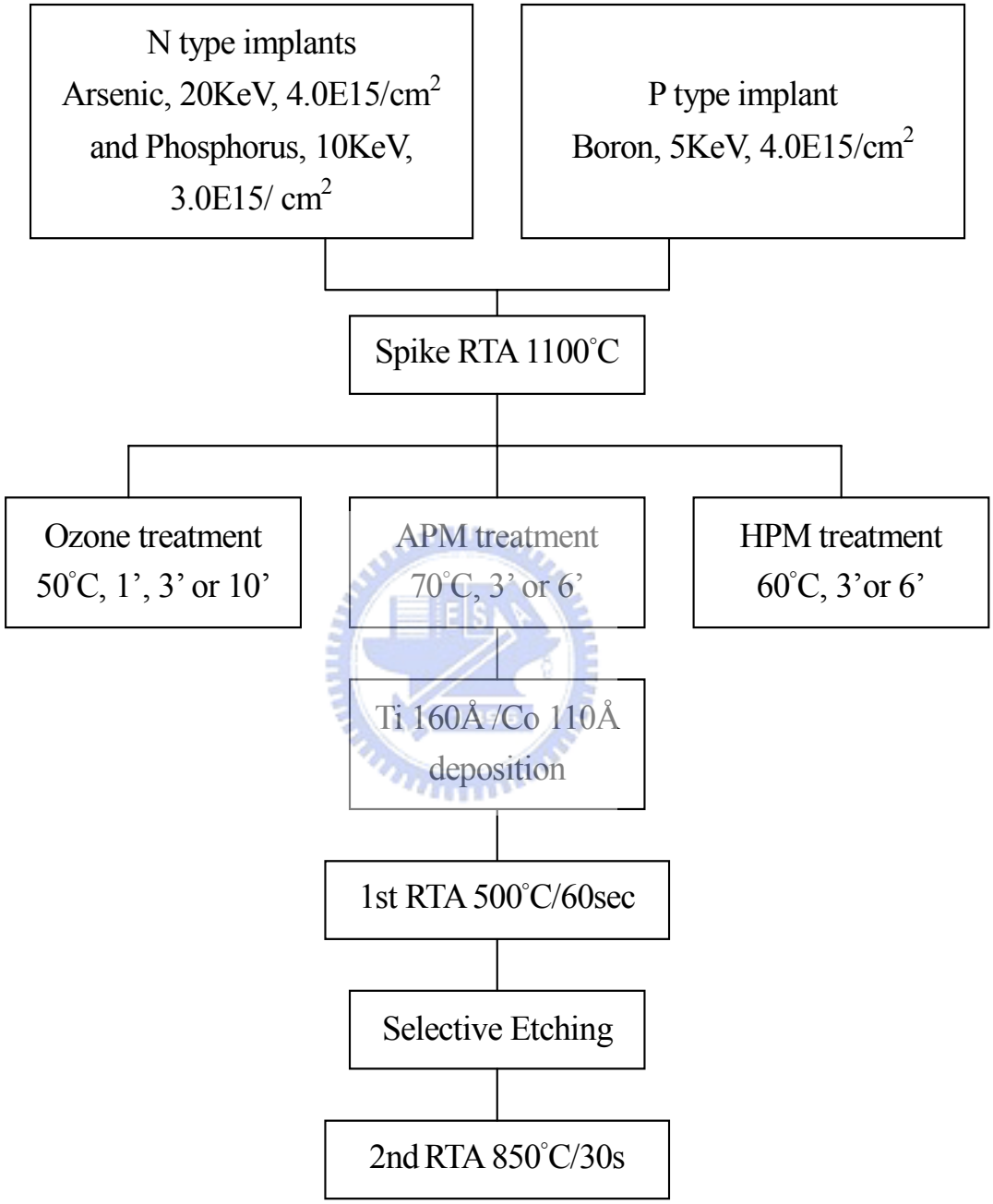

Fig. 5-1 : Process flow of blanket substrate study

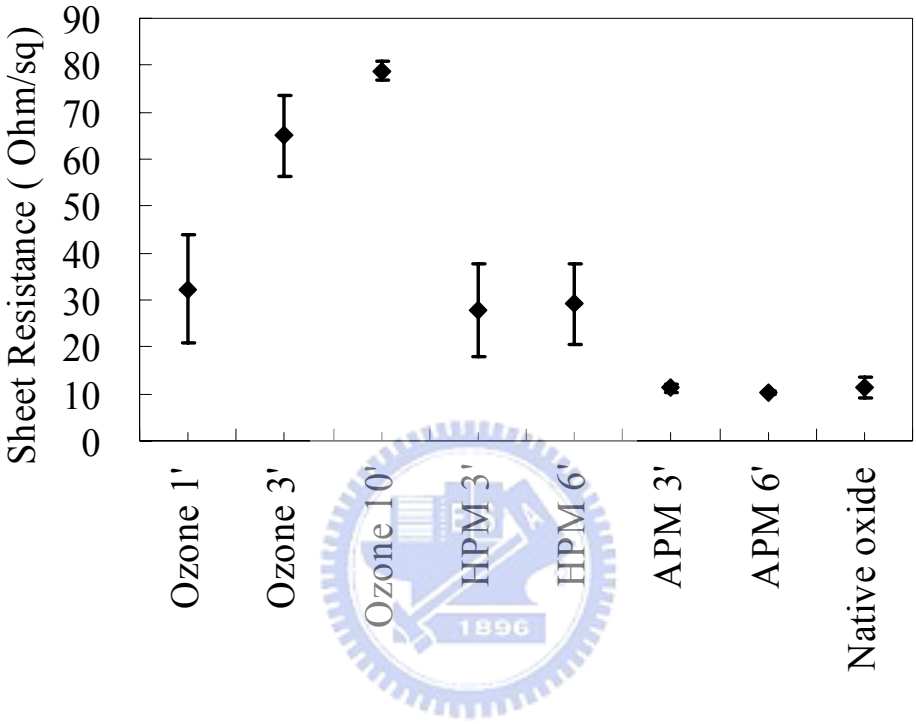

Fig .5-2 : The sheet resistance with different chemical treatments and process time on heavy doped N+ substrate.

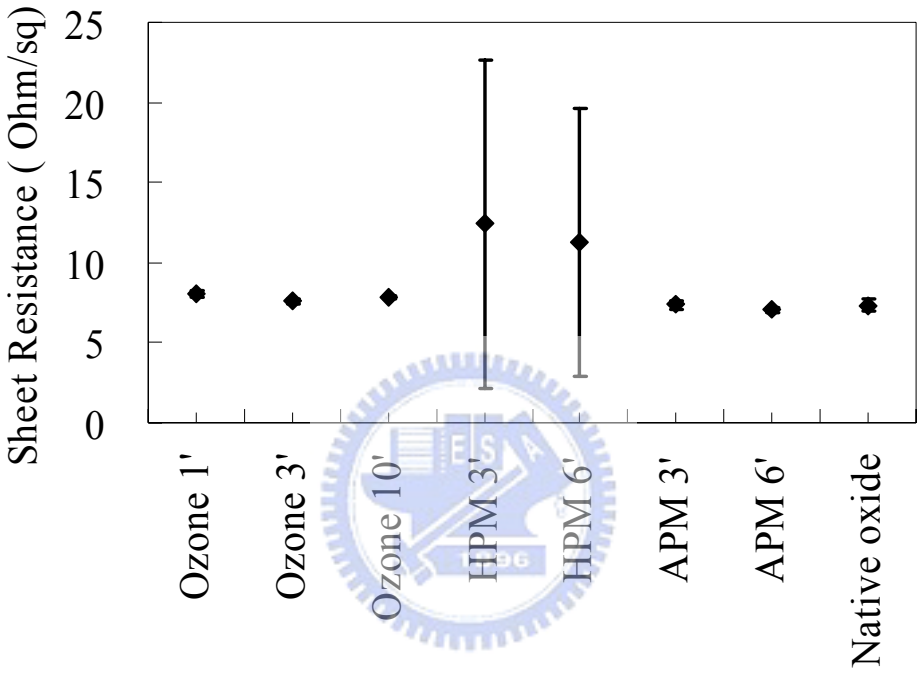

Fig.5-3 : The sheet resistance with different chemical treatments and process time on heavy doped P+ substrate.

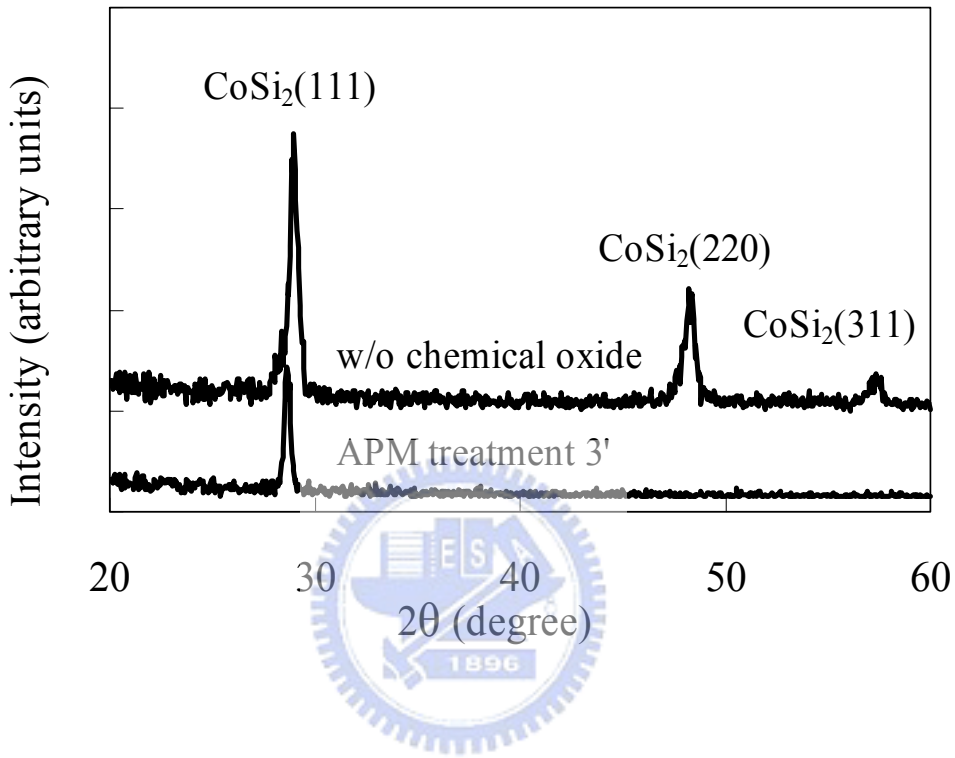

Fig. 5-4 : X-ray diffraction patterns for without chemical oxide (native oxide) and with APM treatment 3 minute

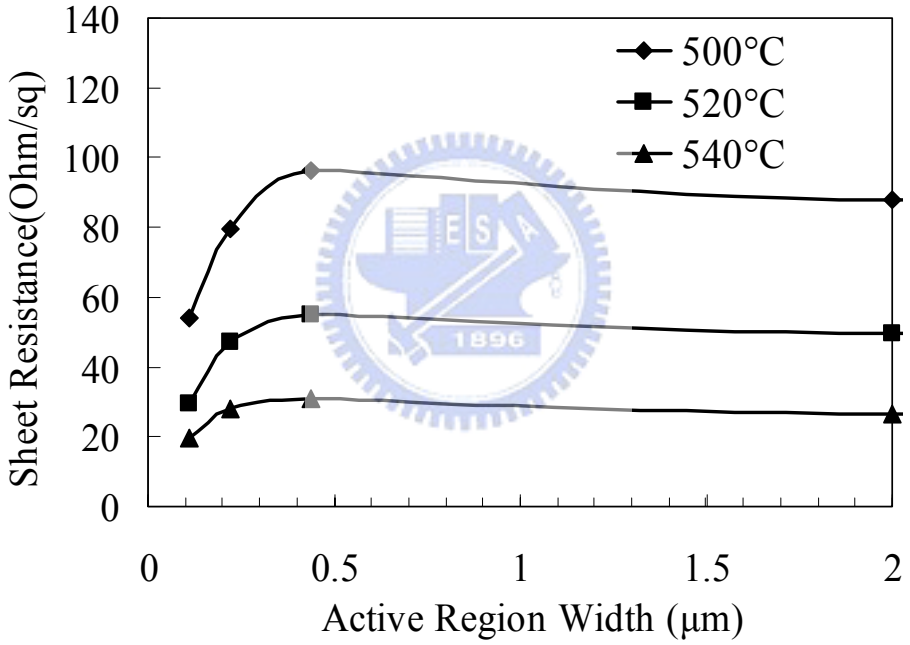

Fig. 5-5(a) : Sheet resistance of N+ active region treated by 1 minute of ozone.

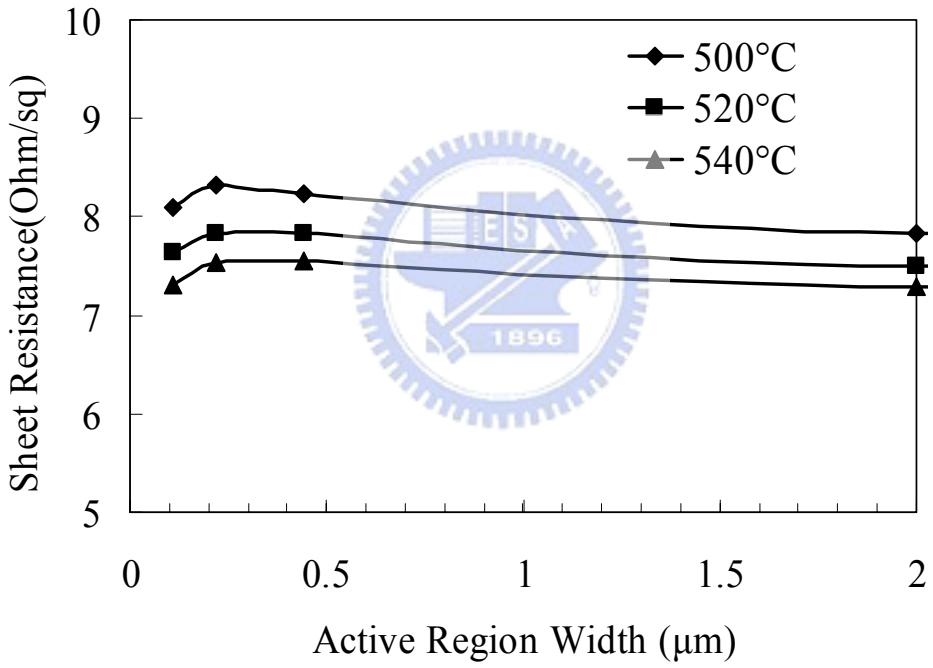

Fig. 5-5(b) : Sheet resistance of P+ active region treated by 1 minute of ozone.

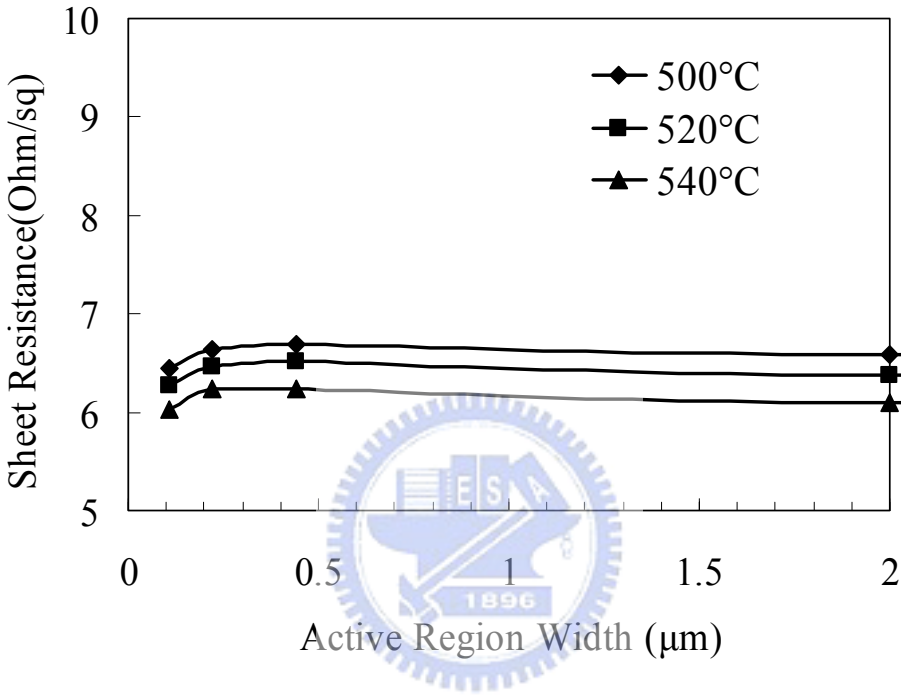

Fig. 5-6(a) : Sheet resistance of N+ active region treated by 3 minute of APM.

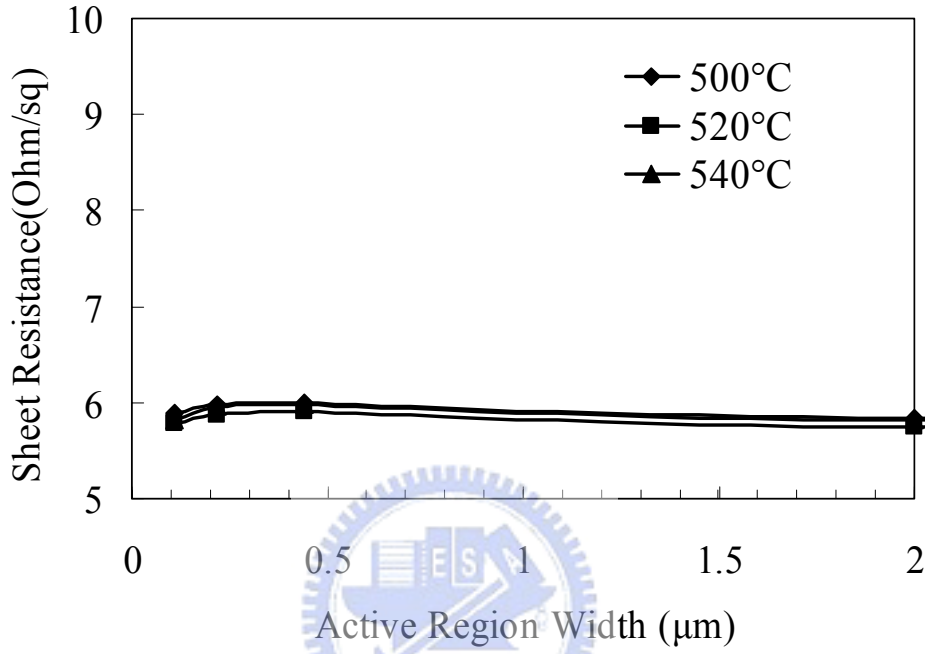

Fig. 5-6(b) : Sheet resistance of P+ active region treated by 3 minute of APM.

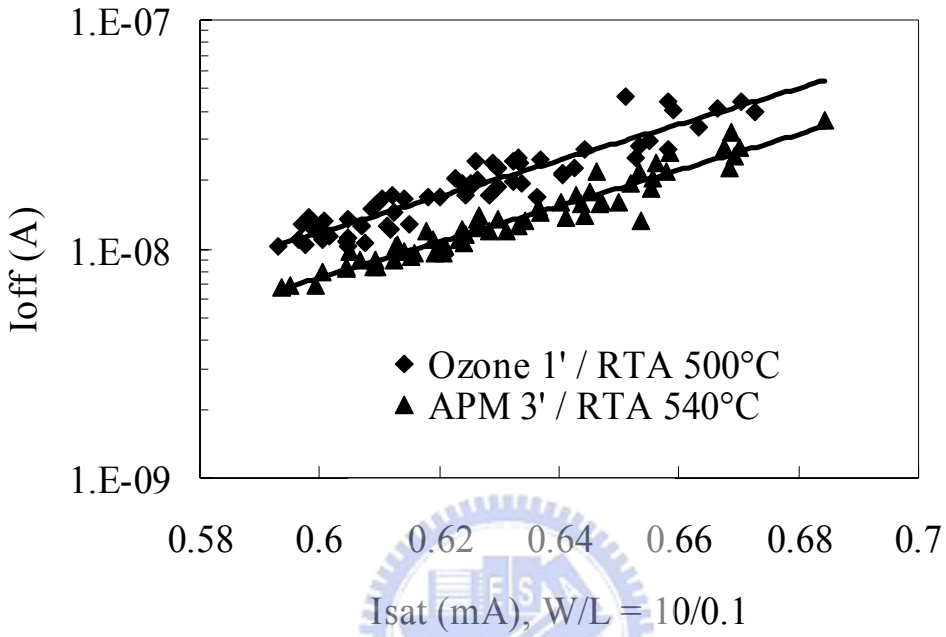

Fig. 5-7 : The Isat-Ioff measurement on NMOS processed by different chemical oxide

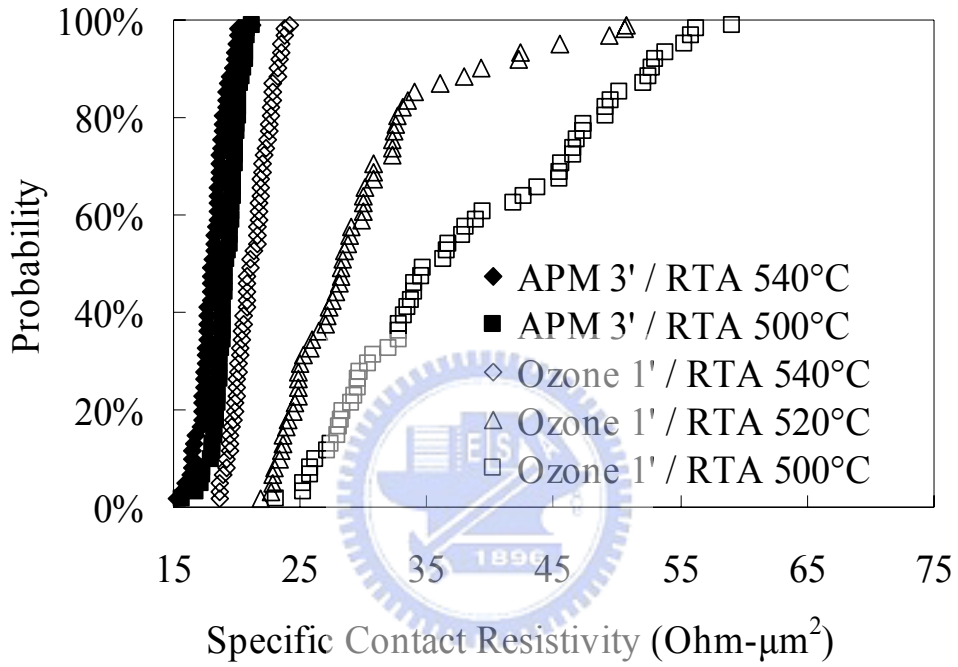

Fig. 5-8: Specific contact resistance for different chemical treatment substrate

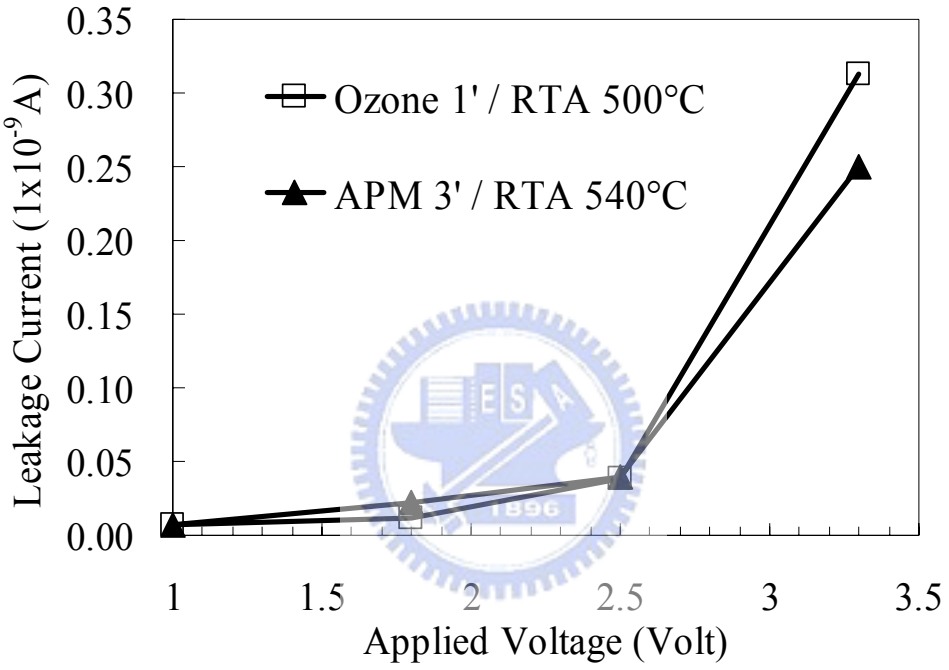

Fig. 5-9: Junction leakage on N type finger type active region

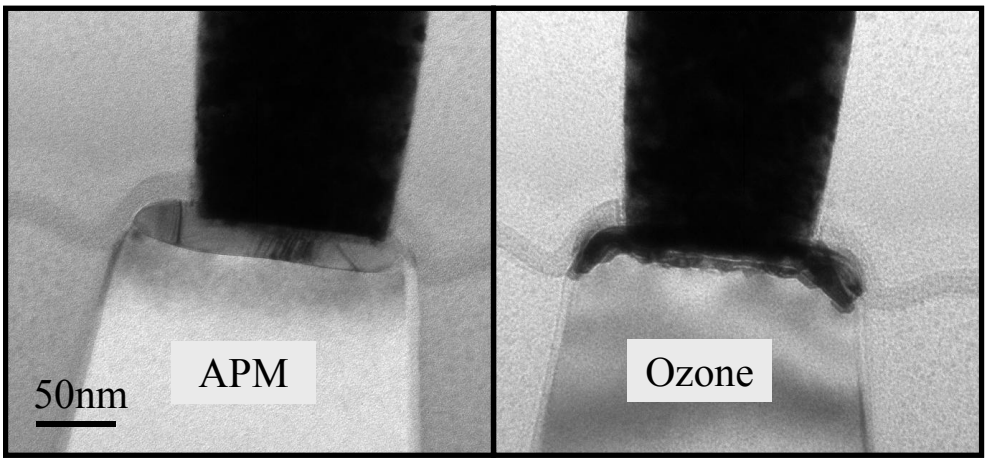

Fig. 5-10: TEM cross section for APM and ozone treatment process on N+ active region

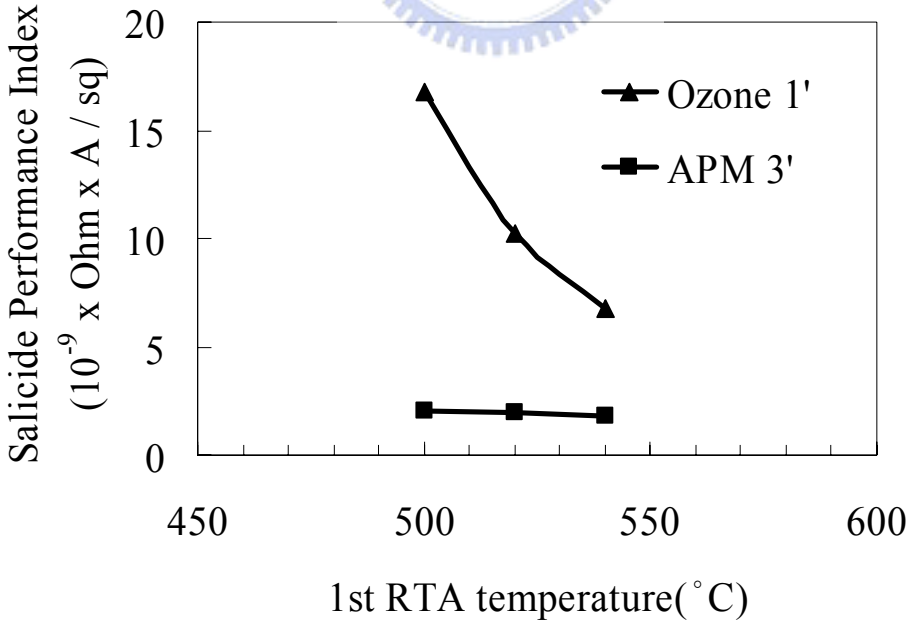

Fig. 5-11: The silicide selection index

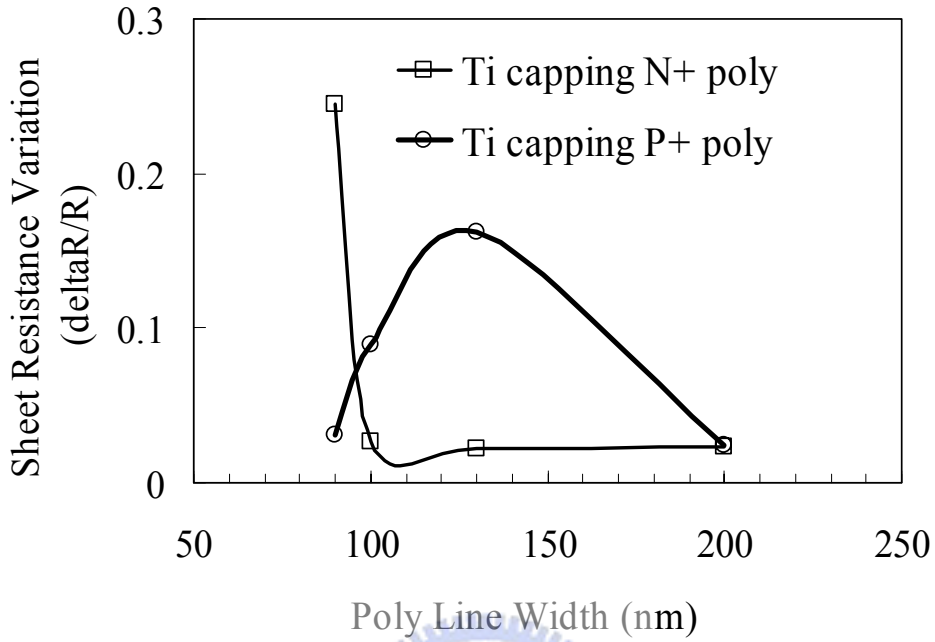

Fig. 6-1 : Sheet resistance variation of poly resistors with different widths.

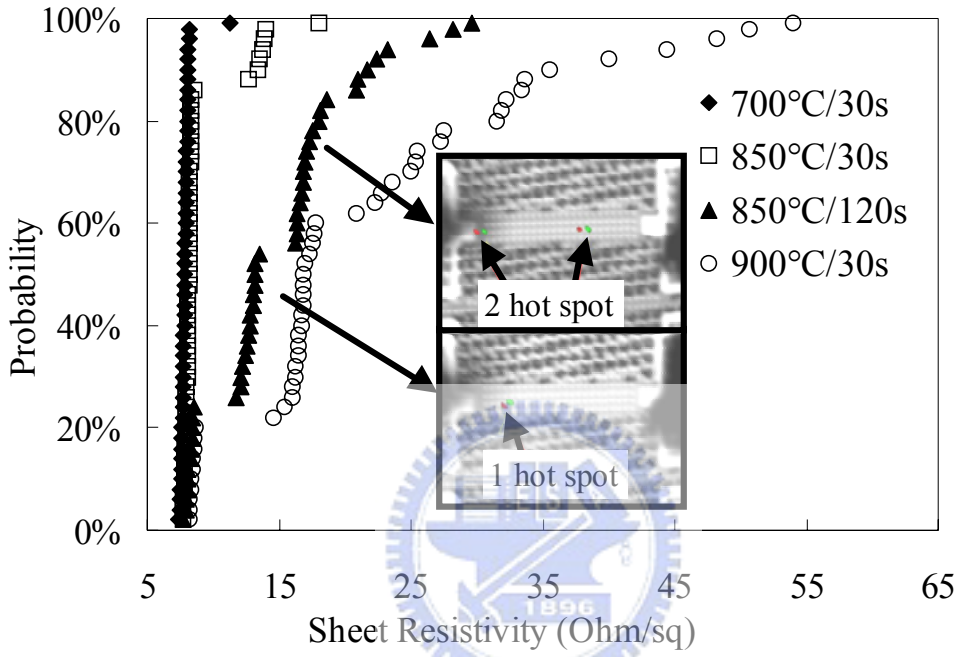

Fig. 6-2 : Sheet resistance distribution for P+ poly resistor (drawn width = 130 nm). The insets are the EMMI images of high resistance sites.

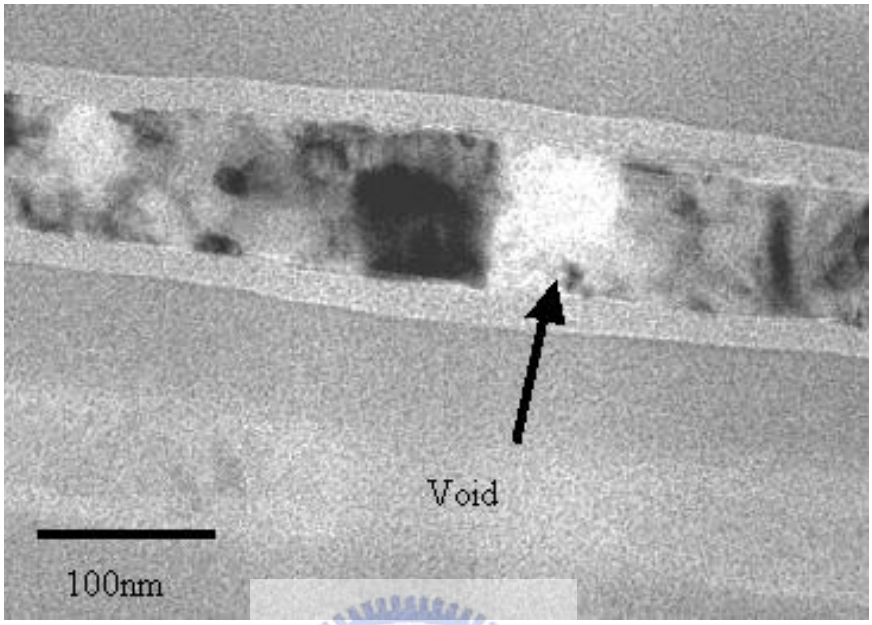

Fig. 6-3 : TEM plan view for the high resistance site on P+ poly resistor (drawn width = 130 nm, the "1 hot spot" sample in Fig. 6-2).

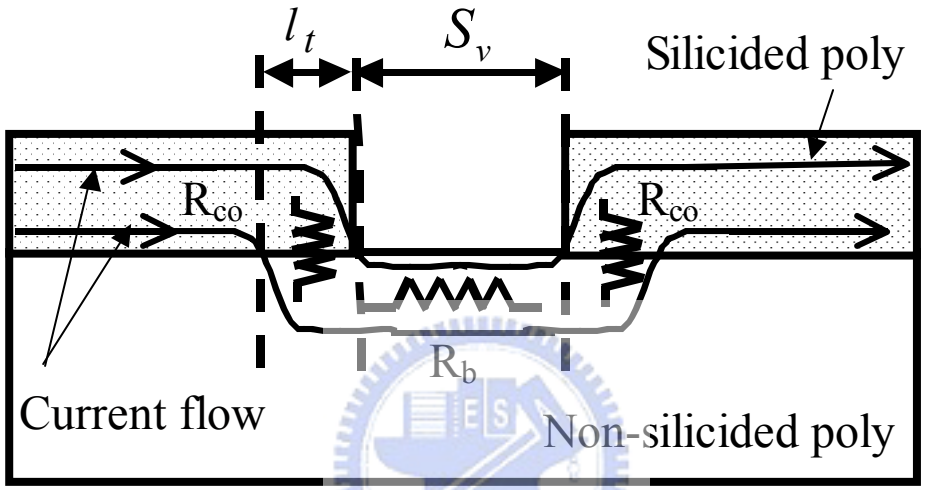

Fig. 6-4 : Illustration for the current flow through the poly resistor. (Not to the scae)

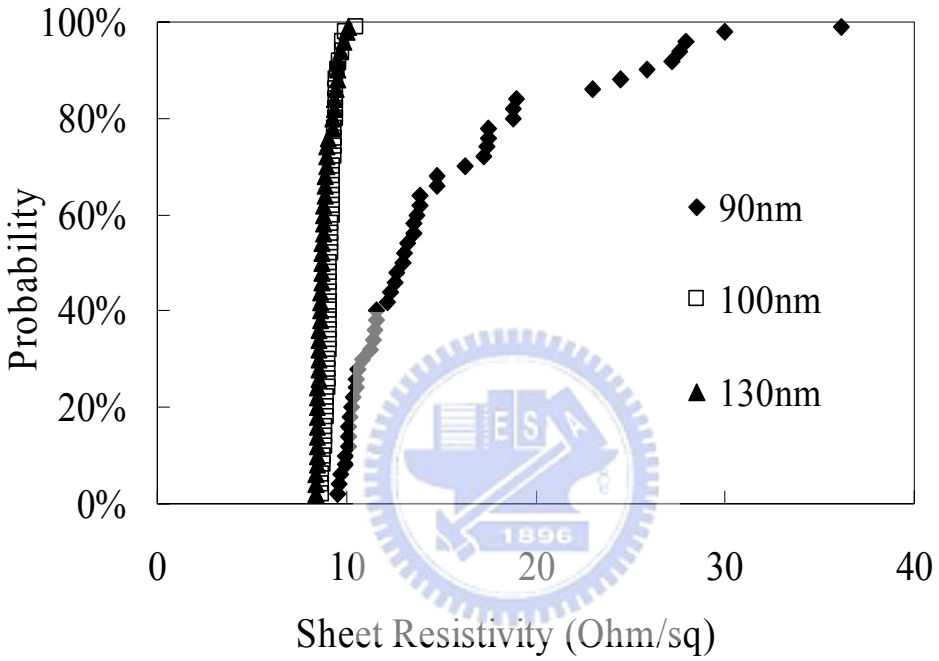

Fig. 6-5 : Sheet resistance distribution for different drawn width of N+ poly resistors

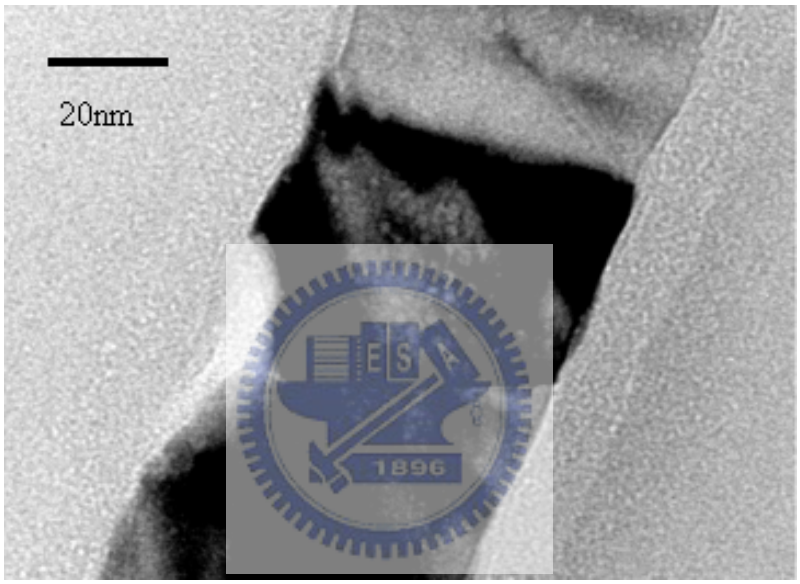

Fig. 6-6 : TEM plan view for the high resistance site on N+ poly resistor (drawn width = 90nm).

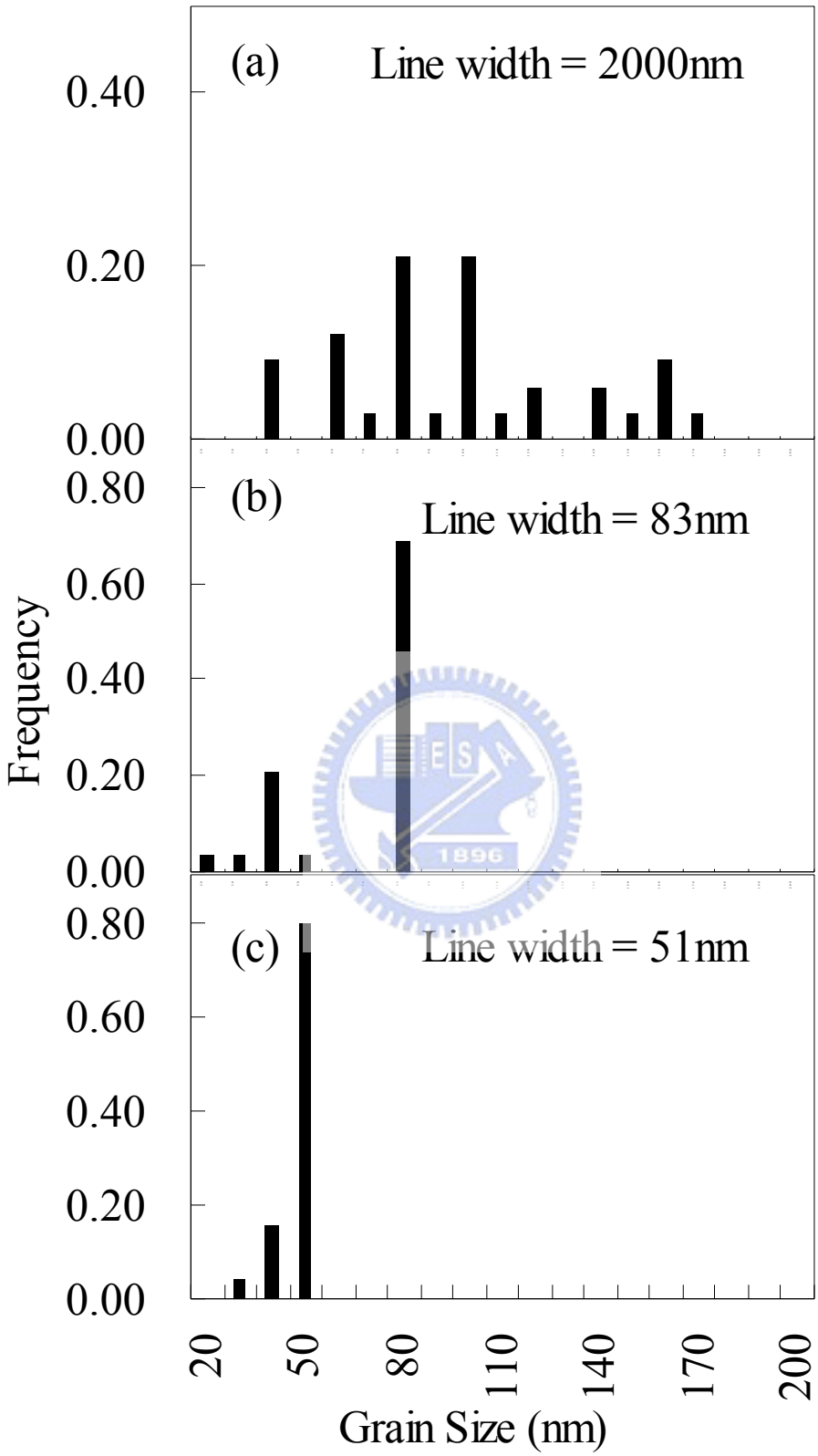

Fig. 6-7 : Grain size distribution for N+ poly resistors.

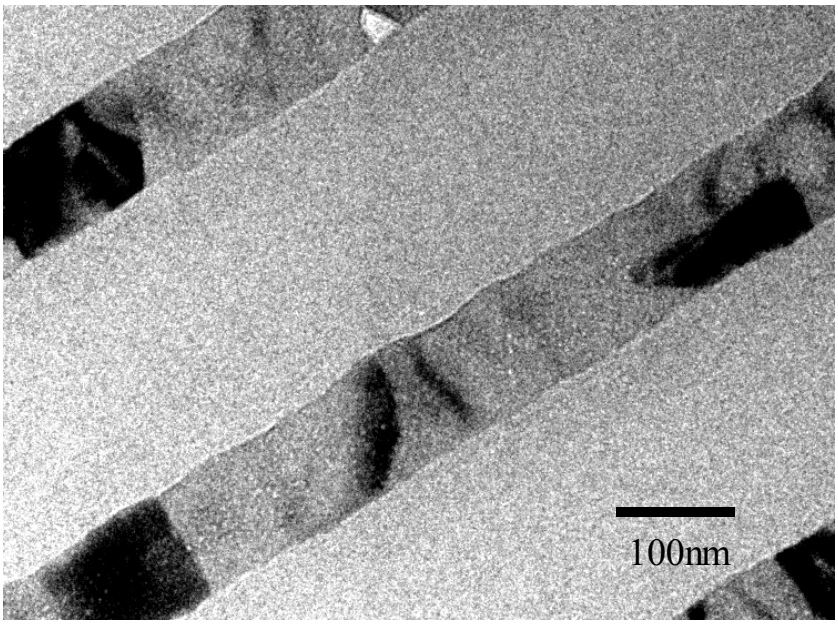

Fig. 6-8: TEM plane view for the quasi-bamboo microstructure on narrow N+ poly resistor

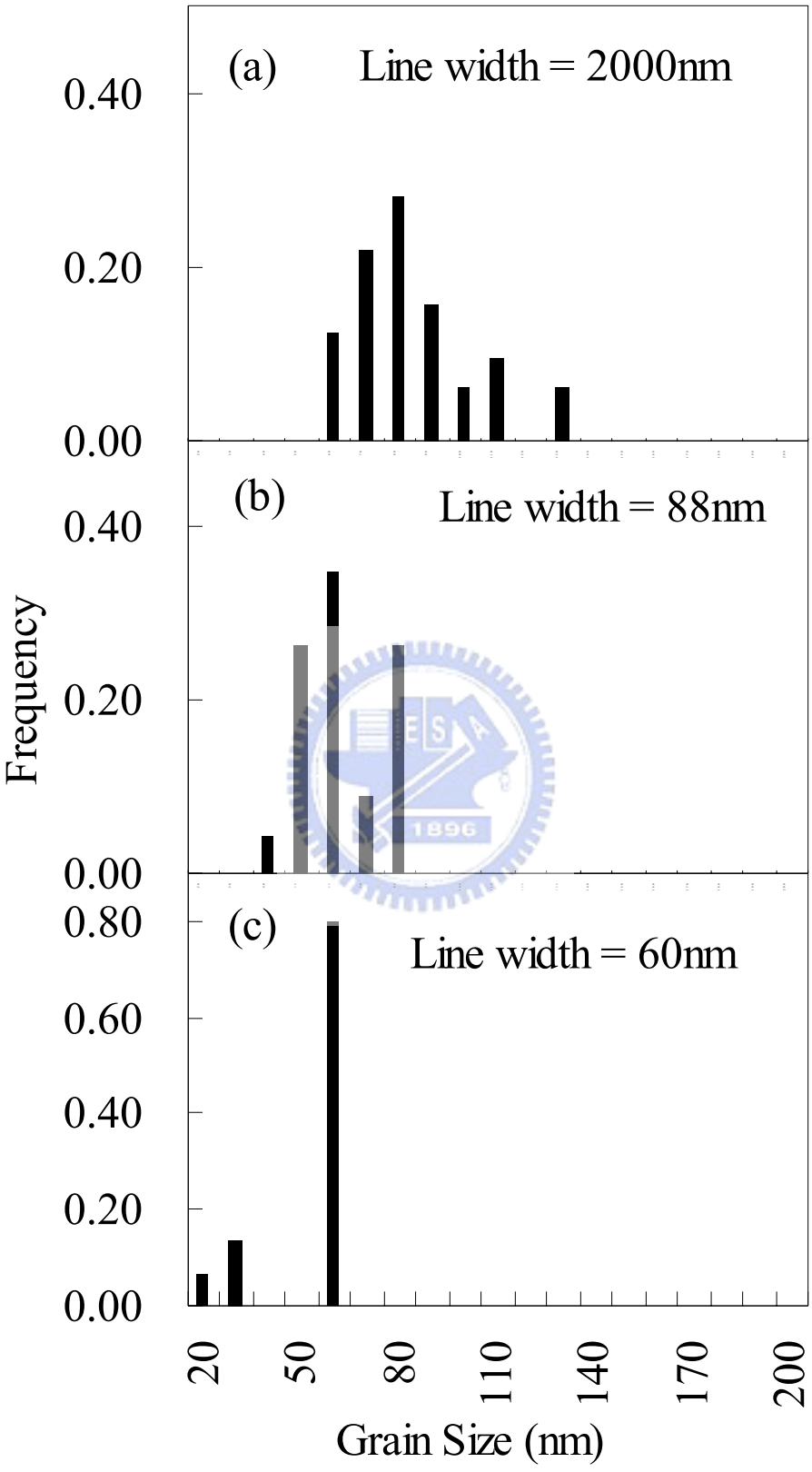

Fig. 6-9 : Grain size distribution for P+ poly resistors.

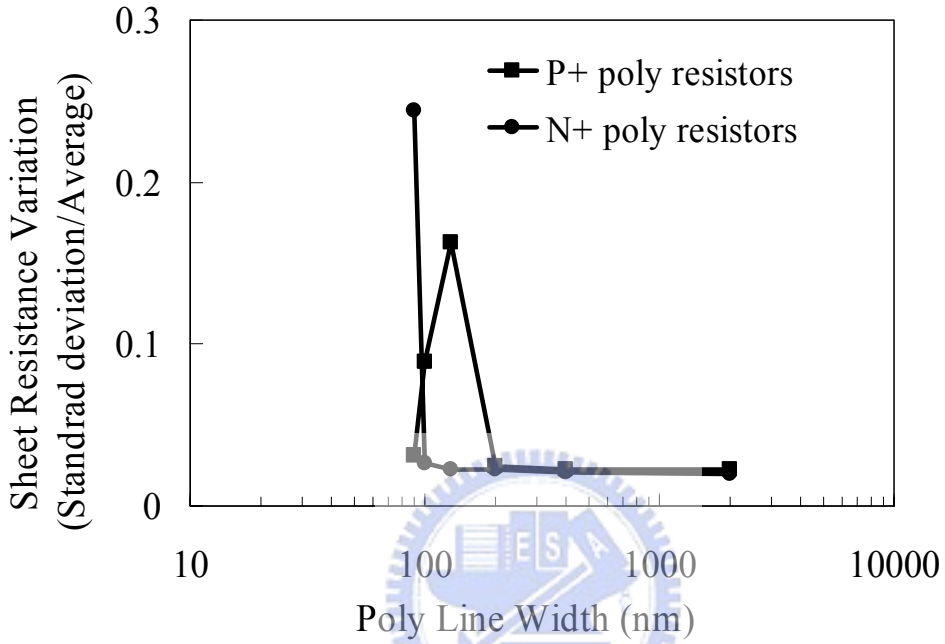

Fig. 7-1 : Sheet resistance variation of N+ and P+ poly-Si resistors with different drawn widths

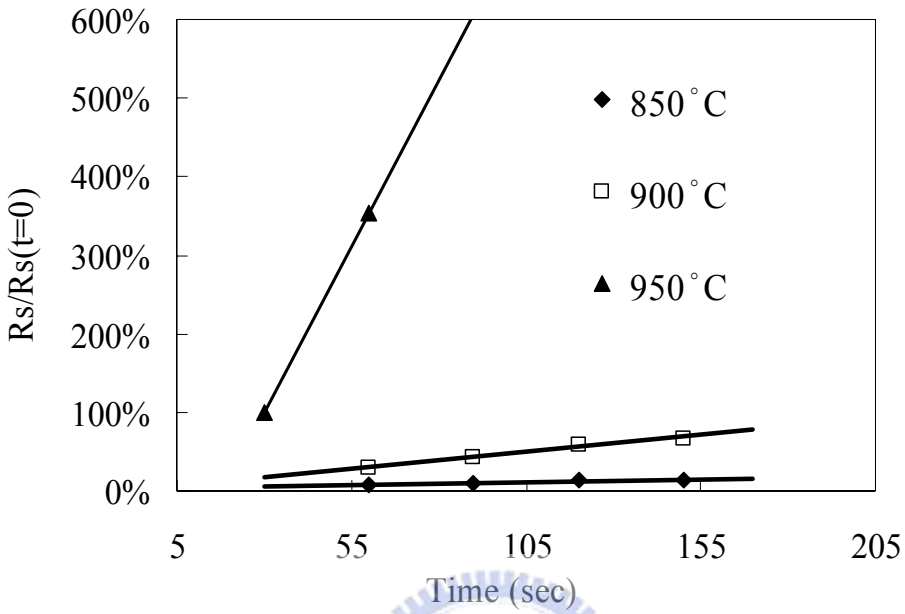

Fig. 7-2 : Sheet resistance measurement vs extra anneal time and temperature for P+ poly resistor (w=2000 nm)

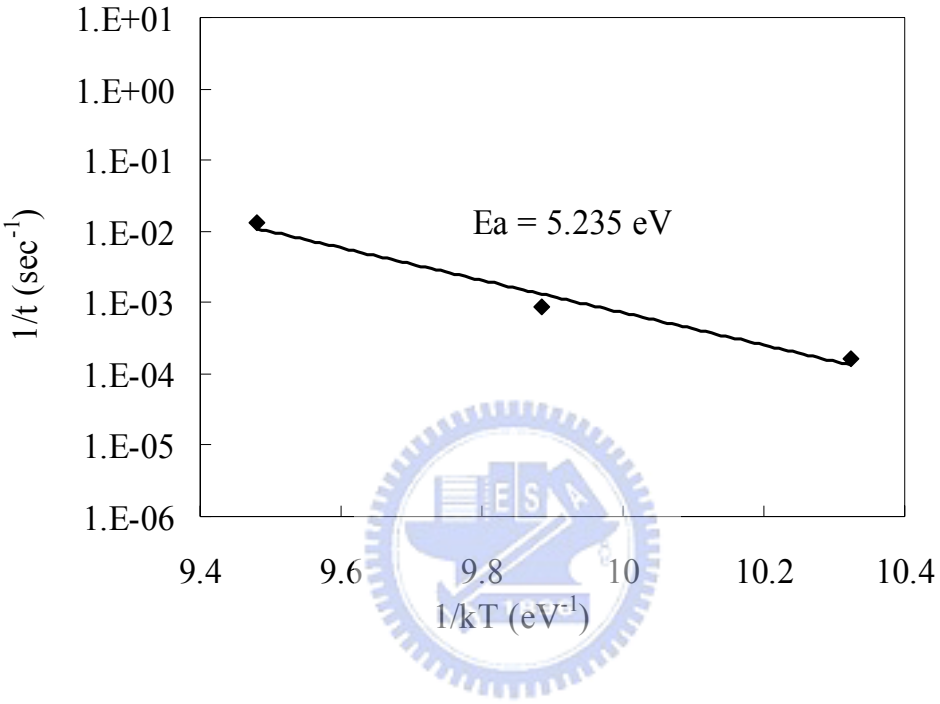

Fig. 7-3 : Activation energy extraction P+ poly resistor (w=2000 nm)

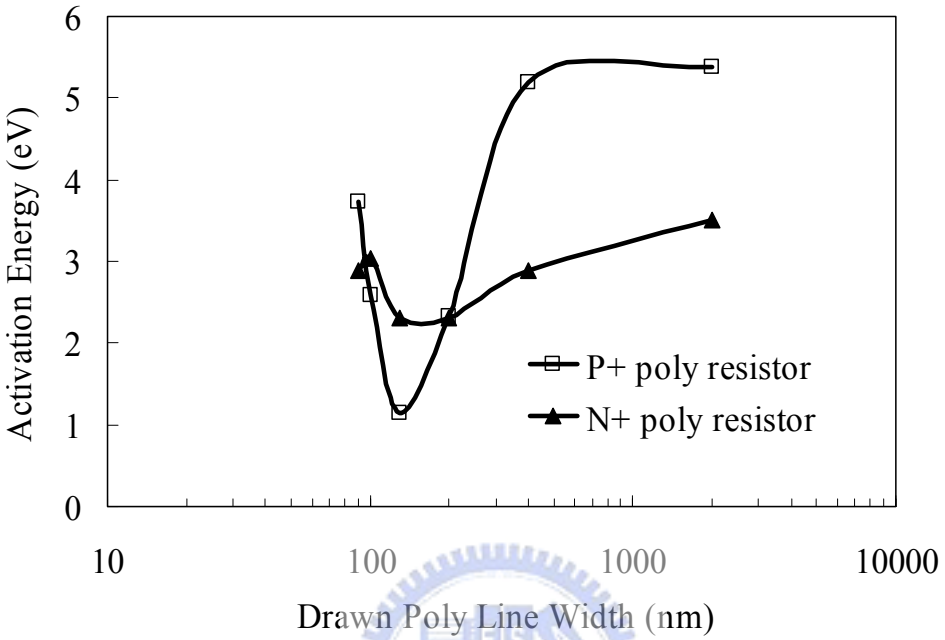

Fig. 7-4 : Activation energy vs different drawn width for both N+ and P+ poly resistors

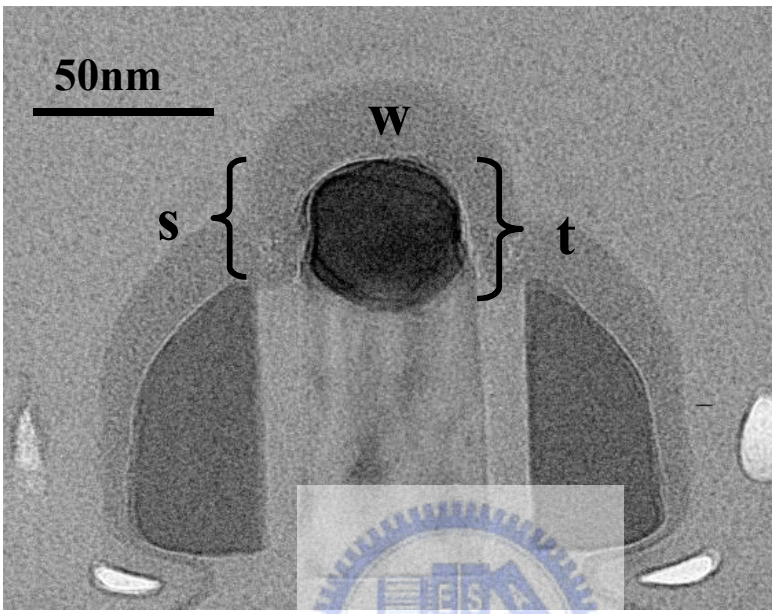

Fig. 7-5 : The definition for the actual poly width (w), silicide thickness (t) and spacer top –loss (s)

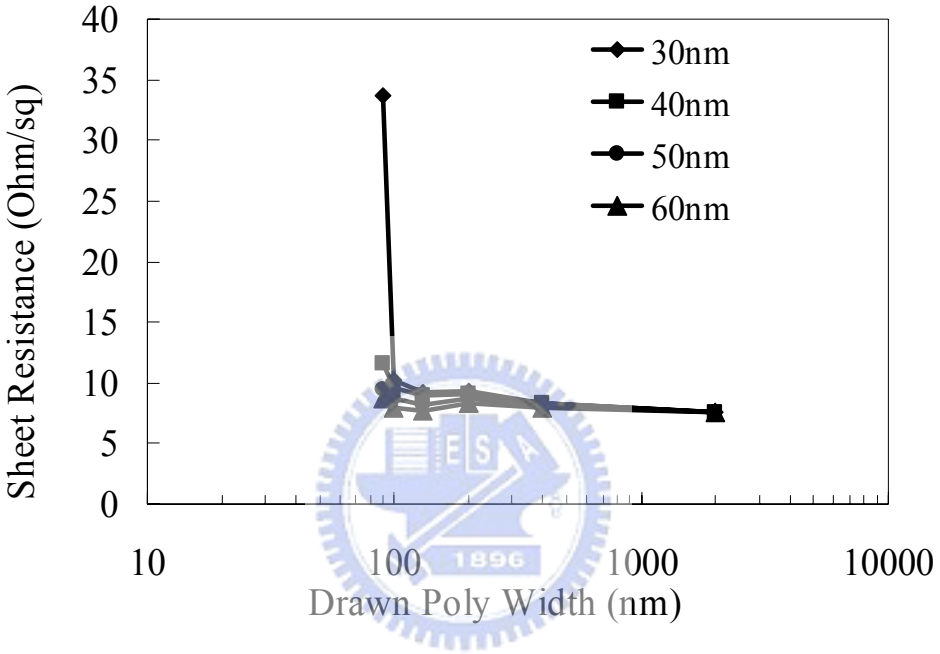

Fig.7-6 : Sheet resistance measurement vs spacer top loss for different drawn poly width

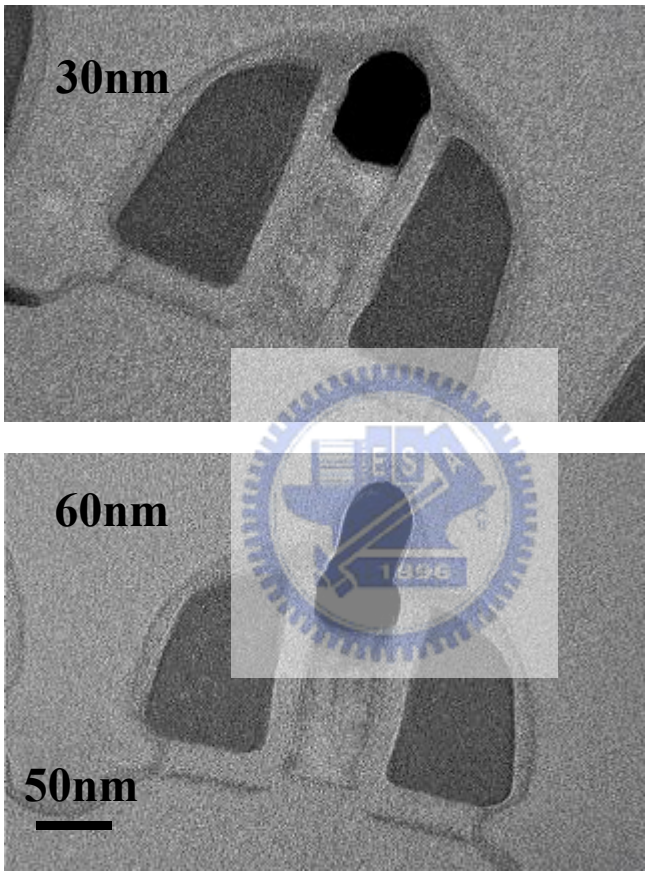

Fig. 7-7 : TEM cross section for different spacer top-loss samples

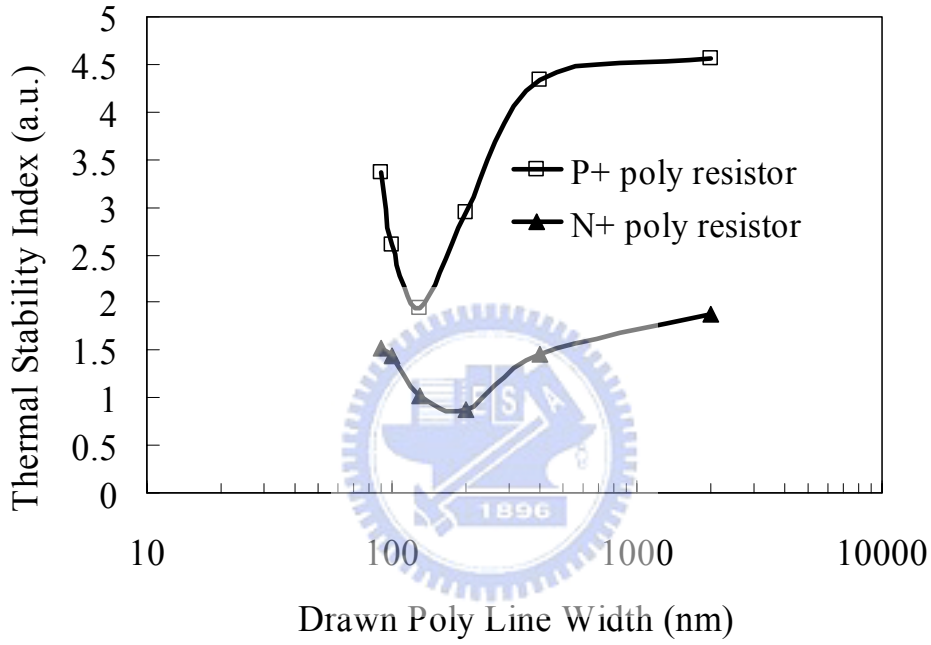

Fig. 7-8 : Thermal stability index vs different drawn poly width

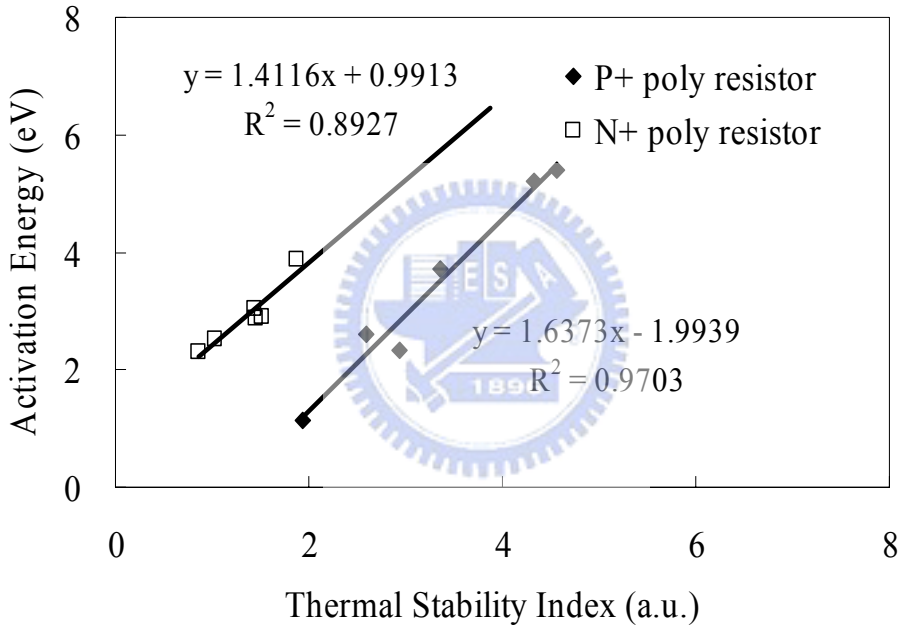

Fig. 7-9 : The correlation between thermal stability index and activation energy

Year	1993	1995	1997	1999	2001
Technology node	0.5μm	0.35μm	0.25μm	0.18μm	0.13μm
Physical gate length (nm)	500	350	200	130	70
Transistors in per cm^2	300K	800K	2M	5M	89M
DRAM product	16M	64M	256M	256M	512M

Year	2003	2005	2007	2009
Technology node	90nm	65nm	45nm	32nm
Physical gate length (nm)	50	30	20	15
Transistors in per cm^2	307M	487M	773M	1227M
DRAM product	1G	2G	2G	4G

Table 1-1 : The device dimension and density change along the technology rolling

Silicide	Thin film resistivity	Sintering temperature	Stability	Si consumed/ nm of metal	nm of resulting silicide / nm of metal	Barrier height to n-Si
	(μΩ-cm)	℃	℃	nm	nm	eV
PtSi	28-35	250-400	~750	1.12	1.97	0.84
$TiSi_2$ (C54)	13-16	700-900	~900	2.27	2.51	0.58
$TiSi_2$ (C49)	60-70	500-700		2.27	2.51	
WSi_2	30-70	1000	~1000	2.53	2.58	0.67
Co2Si	~70	300-500		0.91	1.47	
CoSi	100-150	400-600		1.82	2.02	
$CoSi_2$	14-20	600-800	~950	3.64	3.52	0.65
NiSi	14-20	400-600	~650	1.83	2.34	
$NiSi_2$	40-50	600-800		3.65	3.63	0.66
$MoSi_2$	40-100	800-1000	~1000	2.56	2.59	0.64
$TaSi_2$	35-55	800-100	~1000	2.21	2.41	0.59

Table 1-2 : Basic properties for metal silicides

Drawn poly width (nm)	90	100	130	200	400	2000
Silicide thickness,t (nm)	58	51	42	40	38	39
Actual line width,w (nm)	52	60	88	147	309	2000
Grain boundary index,w/Lc	1	1	1.1	1.84	3.00	3
Thermal stability index,wt^2/Lc	3364	2601	1940.4	2940.00	4332.00	4563

Table 7-1 : The actual poly width, silicide thickness, void data for P+ poly resistors

Drawn poly width (nm)	90	100	130	200	400	2000
Silicide thickness,t (nm)	39	38	32	29	25	25
Actual line width,w (nm)	45	51	83	134	303	2000
Grain boundary index,w/Lc	1	1	1	1.03	2.33	3
Thermal stability index,wt^2/Lc	1521	1444	1024	866.88	1456.73	1875

Table 7-2 : The actual poly width, silicide thickness, void data for N+ poly resistors