

Chapter 6

Conclusions

In this dissertation, structure and characteristics of the dry film photo-resist were introduced. Reaction mechanism and process flow were discussed. Several experiments were conducted to find the optimized process parameters for the dry film photo-resist. A Laminator was adopted to laminate the dry film. The lamination temperature was 110°C and the pressure was 45Psi. Lamination Speed was about 52cm/min. For patterns with 30μm and 50μm in diameter, optimized exposure dose and developing time were 50mJ/cm² and 3 minutes respectively. For the gold plating process, hard baking is necessary to improve the adhesion of the dry film. The optimized hard baking process parameters were 90°C for 6 minutes. Surface roughness increases from 0.272nm to 1.44nm after the hard baking.

For gold bump electroplating, 1 hour and 1.5 hours plating resulted in 31.8μm and 53.8μm bump height respectively for the patterns with 60μm diameter. For copper bump electroplating, 1.5 hours and 2 hours plating resulted in 30.3μm and 45.5μm bump height respectively for the patterns with 60μm diameter.

In this dissertation, the dry film photo-resist is used for high frequency flip-chip packaging as thick film photo-resist for masking in order to reduce the

production cost. Both GaAs chips and alumina substrates with bumps were fabricated. SEM micrography of Au, Cu, SnCu, and SnAg bumps are shown. Shear strength of the electroplated bumps were tested. The average shear force of Au, Cu, SnCu, and SnAg bumps after eight tests were 42.84gm, 31.22gm, 12.46gm, and 12.80gm respectively. Novel cladding metal layer fabrication approach is proposed and compared to the process in literature.

Several circuit patterns and bumps layout were designed to find the best electrical performance. Coplanar waveguides with impedance ranging from 47-52 Ω were designed. After bonding, S-parameter was measured. Good agreement of simulation and measurement was observed. The performances of the copper bumps and the gold bump are the same. For the bumps with optimized circuit design, S_{11} is below -20dB and S_{21} is above -0.3dB in the range from DC to 40GHz.

