乾膜光阻應用在高頻覆晶凸塊製程之研究

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摘　要

本論文研究的方向是將乾膜光阻應用於高頻覆晶封裝上。乾膜光阻比起一般厚膜光阻有許多的優點，諸如：快速的製程時間、良好的表面均勻性、低曝光能量與低廉的成本等。在本論文中，針對乾膜製程中每一道製程，本論文皆提出最佳的製程參數，並使用多種不同材料的凸塊，以乾膜光阻作為模具加以電鍍，並以推球應力測試探討不同材料凸塊的剪應力分佈。 新的抗氧化層製作方法亦被提出以解決銅凸塊容易氧化的問題。

此外，本論文並詳述覆晶封裝製程，分別討論以氧化鋁基版端與砷化鎵晶片端製作凸塊的作法，以及覆晶結合的過程。 本實驗嘗試以不同尺寸大小的共平面波導傳輸線，配合凸塊位置的分佈，研究其在高頻下的 S 參數表現。結果顯示，對於最佳化的覆晶結構而言，在 0～40GHZ 的範圍內，S11 參數低於-20dB，而 S21 參數高於-0.3dB。

總結來說，本文證實乾膜光阻適用於晶圓級高頻覆晶封裝製程。本實驗顯示經過最佳化的傳輸線路設計與凸塊分佈，低成本高效能的覆晶封裝結構目標可以達成。

The study of dry film photo-resist for high frequency flip chip bump application

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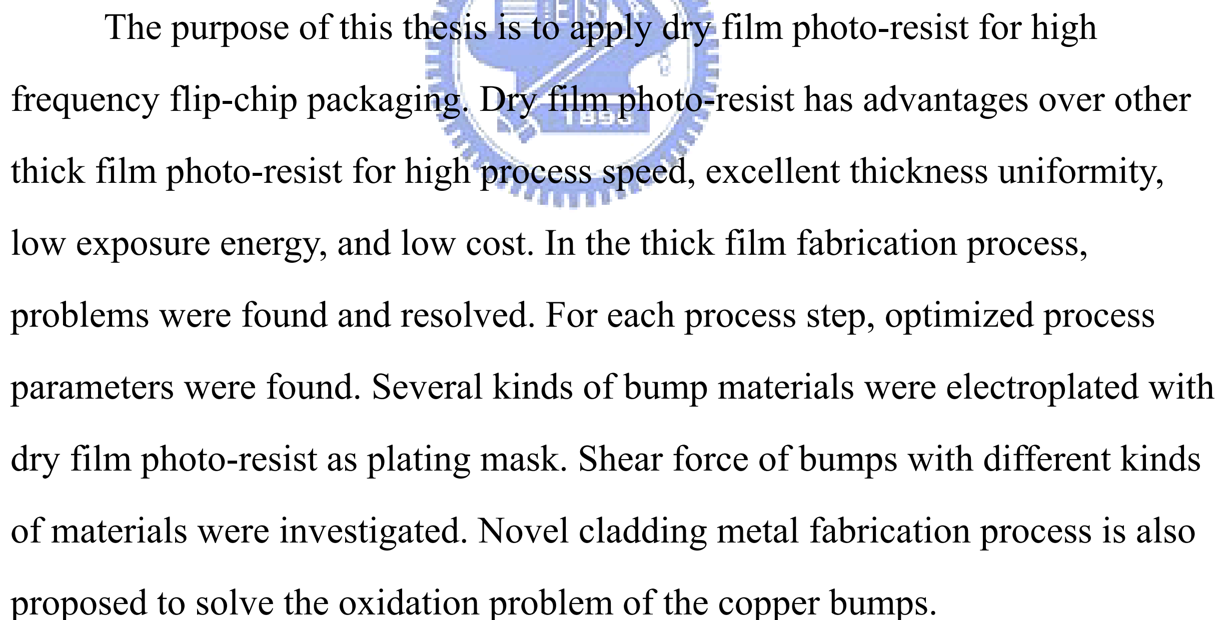
Abstract



The purpose of this thesis is to apply dry film photo-resist for high frequency flip-chip packaging. Dry film photo-resist has advantages over other thick film photo-resist for high process speed, excellent thickness uniformity, low exposure energy, and low cost. In the thick film fabrication process, problems were found and resolved. For each process step, optimized process parameters were found. Several kinds of bump materials were electroplated with dry film photo-resist as plating mask. Shear force of bumps with different kinds of materials were investigated. Novel cladding metal fabrication process is also proposed to solve the oxidation problem of the copper bumps.

In addition, detailed flip-chip process flow was described and implemented. Bumps growth on alumina substrate side and gallium arsenide chip side were processed and discussed as well as the flip-chip bonding process. CPW lines with different sizes in conjunction with optimum bumps layout was designed to investigate the s parameter of the transmission lines. The results

show that S_{11} is below -20dB and S_{21} is above -0.3dB as measured from DC to 40GHz.

In summary, dry film photo-resist was applied to the wafer level high frequency flip-chip packaging process. With optimized circuit design and bump layout, high performance transmission lines for flip chip packages can be achieved using dry film as the masking material for the bump plating.