

Content

Abstract (Chinese)	I
Abstract (English)	III
Acknowledgment	V
Content	VI
Table Captions	VIII
Figure Captions	IX
Chapter 1 Introduction	1
1.1 Research Motivation	1
1.2 Chapter Outlines	2
Chapter 2 Literature Review	4
2.1 Development of Electronic Packaging	4
2.2 Millimeter Wave Packaging	6
Chapter 3 Dry Film Photo-resist	20
3.1 Development and Characteristics of the Dry Film	20
3.2 Structure and Composition	21
3.3 Reaction Mechanism	22
3.3.1 Reaction Mechanism of Exposure	22
3.3.2 Reaction Mechanism of Developing and Stripping	23
3.4 Process Procedure	24
3.5 Experiments and Results	27
Chapter 4 High Frequency Flip-Chip Experiments	45
4.1 Basic Theory and Structure of Coplanar Wave Guide	45
4.2 Theory and Process Procedure of Electroplating	52
4.3 Flip-Chip Bonding Process	57
4.4 Experiments	60
4.4.1 Chip Fabrication	60
4.4.2 Substrate Fabrication	64
4.4.3 Flip-Chip Bonding	66
4.4.4 S-Parameter Simulation and Measurement	66
Chapter 5 Results and Discussions	82
5.1 Process Results	82
5.1.1 Uniformity of Electroplating	82
5.1.2 Double Layer Dry Film Electroplating	83

5.1.3 Chip fabrication results	83
5.1.4 Substrate fabrication results	84
5.1.5 Flip chip bonding results	84
5.1.6 Cladding Layers Fabrication Results	85
5.1.7 Shear Strength Results	87
5.2 RF and Microwave Measurement Results	87
Chapter 6 Conclusions	114
Reference	116



Table Captions

Table 2.1	Comparison of the wire bonding, TAB, and flip-chip characteristics.	19
Table 2.2	Three approaches for obtaining S-parameter.	19
Table 3.1	Development history of the dry film photo-resist	43
Table 3.2	Various pattern sizes on a test mask.	44
Table 3.3	Hard baking conditions with various baking times and temperatures.	44
Table 4.1	Properties of gold.	78
Table 4.2	Properties of copper.	79
Table 4.3	Characteristics of the binary solders.	80
Table 4.4	Properties of various substrate materials	81
Table 5.1	Uniformity of the plated gold and copper bumps.	113



Figure Captions

Fig. 2.1	Five levels of electronic packaging.	12
Fig. 2.2	Several approaches of flip-chip assembly.	12
Fig. 2.3	Measured insertion loss S_{21} of the flip-chip and the wire bond test assemblies.	13
Fig. 2.4	Electric field distribution of microstrip line and coplanar waveguide.	13
Fig. 2.5	S-parameter comparison of the microstrip and CPW line with the same physical dimension.	14
Fig. 2.6	Flip-chip configuration in CPW technology.	14
Fig. 2.7	Schematic drawing of the flip-chip equivalent circuit model.	15
Fig. 2.8	Simplified version of the flip-chip equivalent circuit model.	15
Fig. 2.9	Measurement and FDTD simulation data for the cases with and without the metal lid.	16
Fig. 2.10	Equivalent circuit model of the flip-chip transition.	16
Fig. 2.11	Effect of the dielectric substrate and underfill material on the elements of the equivalent circuit model.	17
Fig. 2.12	Flip-chip CPW-CPW with staggered bumps (plan view of CPW-chip and CPW-substrate).	17
Fig. 2.13	Optimized interconnect design. (a) Without any compensation. (b) Staggered bumps. (c) High and high-low impedance compensation.	18
Fig. 3.1	Structure of the dry film photo-resist.	31
Fig. 3.2	Dry film reaction mechanism for exposure	32
Fig. 3.3	Dry film reaction mechanism for developing and stripping.	32
Fig. 3.4	Structure of a dry film laminator.	33
Fig. 3.5	1X and 50X optical microscopy of dry film surface laminated by a roller.	34
Fig. 3.6	1X and 50X optical microscopy of the dry film surface laminated by a laminator.	34
Fig. 3.7	AFM image of as laminated dry film photo-resist.	35
Fig. 3.8	50X optical microscopy results for the 50 μ m test pattern with various exposure doses and developing times.	36
Fig. 3.9	50X optical microscopy results for the 30 μ m test pattern with various exposure doses and developing times.	37
Fig. 3.10	Optimized developing time for various pattern diameters.	38
Fig. 3.11	SEM pictures of the as developed dry film with various pattern sizes	39
Fig. 3.12	Patterns with underplating for the dry film with hard bake condition of 190 $^{\circ}$ C, 2 minutes.	40

Fig. 3.13	Patterns without underplating for the dry film hard baked at the conditions of (a) 110°C, 6 minutes (b) 90°C, 6 minutes.	40
Fig. 3.14	AFM image of hard baked dry film photo-resist with optimized baking condition.	41
Fig. 3.15	Double layer dry film after developing.	42
Fig. 4.1	Concept figure of a transmission line.	68
Fig. 4.2	Equivalent circuit model of a transmission line.	68
Fig. 4.3	Cross section structures of the coplanar waveguide (a) CPW (b) GCPW.	69
Fig. 4.4	Coplanar waveguide with infinite substrate and zero conductor thickness	70
Fig. 4.5	Simplified coplanar waveguide for calculating impedance	70
Fig. 4.6	Coplanar waveguide with finite substrate and conductor thickness	71
Fig. 4.7	Main components for a plating facility.	72
Fig. 4.8	Photograph of the Flip chip bonder.	73
Fig. 4.9	Schematic drawing of a flip chip bonder alignment system.	74
Fig.4.10	The flip chip process flowchart.	75
Fig.4.11	Reference HEMT device.	76
Fig. 4.12	Different kinds of pattern layout.	77
Fig. 5.1	The pattern for plating uniformity test.	90
Fig. 5.2	SEM picture of a double layer plated copper bump.	91
Fig. 5.3	SEM pictures of the fabricated passive chips.	92
Fig. 5.4	SEM pictures of the fabricated substrates with bumps.	93
Fig. 5.5	Alpha stepper result of the metal thickness of the substrate circuit.	94
Fig. 5.6	SEM picture of the substrate with gold bumps.	95
Fig. 5.7	SEM picture of a single gold bump.	95
Fig. 5.8	SEM picture of the substrate with copper bumps.	96
Fig. 5.9	SEM picture of a single copper bump.	96
Fig. 5.10	SEM picture of the substrate with SnCu bumps.	97
Fig. 5.11	SEM picture of a single SnCu bump.	97
Fig. 5.12	SEM picture of the substrate with SnAg bumps.	98
Fig. 5.13	SEM picture of a single SnAg bump.	98
Fig. 5.14	SEM picture of the substrate with bumps after bonding.	99
Fig. 5.15	SEM picture of a single bump after bonding.	99
Fig. 5.16	Structure of a copper bump with cladding metals.	100
Fig. 5.17	Top view of the developed dry film with cladding metals.	101
Fig.5.28	Detailed top view of the developed dry film with cladding metals.	101
Fig. 5.19	Cross section of the developed dry film w/o cladding metals.	102
Fig. 5.20	SEM picture of a copper bump with cladding metals.	103
Fig. 5.21	EDX analysis of the cladding metals.	103
Fig. 5.22	The cross section of a 60µm copper bump with cladding metals.	104

Fig. 5.23	The cross section of a 50 μ m copper bump with cladding metals.	104
Fig. 5.24	Schematic diagram of the shear strength measurement	105
Fig. 5.25	Shear strength test results of eight gold bumps.	106
Fig. 5.26	Shear strength test results of eight copper bumps.	106
Fig. 5.27	Shear strength test results of eight SnCu bumps.	107
Fig. 5.28	Shear strength test results of eight SnAg bumps.	107
Fig. 5.29	Measured S-parameter of the bonding structure with gold bumps.	108
Fig. 5.30	Measured S-parameter of the bonding structure with copper bumps.	108
Fig. 5.31	Simulation S-parameter of the bonding structure.	109
Fig. 5.32	Simulation S-parameter of the first bonding structure.	110
Fig. 5.33	Measured S-parameter of the first bonding structure.	110
Fig. 5.34	Simulation S-parameter of the second bonding structure.	111
Fig. 5.35	Measured S-parameter of the second bonding structure.	111
Fig. 5.36	Simulation S-parameter of the third bonding structure.	112
Fig. 5.37	Measured S-parameter of the third bonding structure.	112

