Chapter 2

Literature Review

2.1 Development of Electronic Packaging

Electronic Packaging is to assemble an integrated circuit device with specific function and to connect with other electronic devices. It has to provide power transmission, signal communication, heat dissipation, and structure protection. Electronic packaging processes can be divided into five levels as shown in Fig. 2.1. The zeroth level is interconnection on IC chips. The first level is to put IC chip into a packaging frame and to achieve electrical connection and air-tight protection. The second level is to assemble the packaging frame onto a circuit card. The third level is to assemble the card onto a circuit board. The fourth level is to integrate circuit board and the devices altogether into an electronic product. With the integrated circuit function trend goes into high capacity, multi-functional, and high speed. The functional density of the electronic device increase more and more. IC chips need high I/O counts and fine pitch to meet the industry's demands. Therefore, Area Array packaging has gradually replaced traditional Peripheral Array technology. This can be confirmed from the transformation of SOP (small Outline Package), TSOP (Thin Small Outline Package), QFP (Quad Flat Package) technology into BGA (Ball Grid Array), CSP (Chip Scale packaging), and COB (Chip on Board) technology. For the same reason, chip packaging technology also transforms from wire

bonding, TAB into flip-chip bonding. Table 2.1 compares wire bonding, TAB, and flip-chip in many aspects. Flip-chip microelectronic assembly is the direct electrical connection of face-down electronic components onto substrates, circuit boards, or carriers, by means of conductive bumps on the chip bond pads. In contrast, wire bonding, the traditional technology which is being replaced by flip-chip, uses face-up chips with a wire connection to each pad. In 1960, IBM introduced flip-chip interconnection for their mainframe computers. It was called C4 (Controlled Collapse Chip Connection) at that time. Expected to reduce the labor cost of the wire bonding and to enhance the interconnect density and reliability. It is also called Direct Chip Attach (DCA), a more descriptive term, since the chip is directly attached to the substrate, board, or carrier.

Flip-chip has several advantages. First of all, it reduces the required board area by up to 95%, and requires far less height compared with wire bonding technology. Weight can be less than 5% of the packaged device weight. It is the simplest package with smallest size, even smaller than Chip Scale Packages (CSP's). Second, it offers the highest speed electrical performance of any assembly method. Eliminating bond wires reduces the delaying inductance and capacitance of the connection by a factor of 10, and shortens the path by a factor of 25 to 100. The result is high speed off-chip interconnection. Third, it gives the greatest input/output connection flexibility. Wire bond connections are limited to the peripheral of the die, driving the die sizes larger as the number of the connections increases. Flip-chip uses the whole area of the die, accommodating many more connections on a smaller die. Fourth, it provides the lowest cost interconnection for high volume automated production, with costs below $0.01

per connection.

With the development of the interconnection technology, the flip-chip technology has been broadly defined as: Technology which utilizes metal or other conductive material as a media to join substrate and the faced-down chip. There are many approaches such as Solder Bump, Plated Bump, Stud Bump, ICA (Isotropic Conductive Adhesives), ACA (Anisotropic Conductive Adhesives), Conductive Polymer Bump. Fig. 2.2 depicts some of these approaches. From all of the approaches mentioned above, Plated Bump is the mainstream and has been used in mass production for its batch process characteristics.

2.2 Millimeter Wave Packaging

The drive in industry towards more and more wireless communication for various purposes increases the need for packaging for ever higher frequencies. There are increasing applications in the millimeter wave range such as automotive radar systems [1] and high speed wireless communications [2]. To make these products more affordable for common people, the main concern is reducing the cost while maintaining a good enough performance.

Wire bond and flip-chip are two main approaches for high frequency packaging. Although wire bond is a traditional and mature technology, it has several disadvantages that make it hard to be applied to the millimeter wave devices [3]. Due to the long distance of the wire bond interconnection, the insertion loss decreases very fast at high frequency and the attenuation of the wire bond is large compared with flip-chip [4].

On the other hand, Flip-chip has several advantages such as shorter interconnection length and higher reliability [5]. Fig. 2.3 is a comparison of the measured insertion loss of the flip-chip and wire bond test assemblies [6]. Since the chip is flipped, high frequency performance may change significantly due to the electromagnetic field interaction between the flipped chip and the mounting substrate [7]. It is concluded that the key parameters of the flip-chip structure are “Transmission line type”, ”Spacing between chip and substrate” and “Transition into the chip” [8].

For the photolithography process in the semiconductor industry, microstrip line and coplanar waveguide are the most common approaches for high frequency transmission line. The main difference between them is the electric field distribution during wave propagation [9]. Fig. 2.4 shows the electric field distribution. From the figure, it can be seen that the interaction of the electromagnetic wave and the dielectric substrate is much more in the microstrip case. This interaction will suffer from additional loss and cross talk issue. Furthermore, the line width of the microstrip is in proportion to the wafer thickness, so it always need wafer thinning and backside processing [10]. Considering these factors, manufacturing costs will be high.

One the other hand, CPW (coplanar waveguide) has several advantages which may just overcome those problems. The line width is almost independent of the wafer thickness so it is much flexible for design [11]. Fig. 2.5 is an s-parameter comparison of the microsrip and the CPW line with same dimension [12]. It can be seen that the CPW type shows better performance over microstrip

type. From the cost and the performance point of view, the CPW type with flip-chip bonding is therefore selected for study in this dissertation.

To exam the CPW performance, three steps are needed to obtain the accurate s-parameter. Table 2.2 shows these steps. From the table, simulation is an efficient way but its accuracy still needs verification. Experiment is conducted in real world but need carefully process and measurement. Once data are observed from simulation or experiment, the equivalent circuit model can be derived.

Fig. 2.6 shows a common flip-chip CPW structure [13]. The chip is flipped and connected to the substrate through metal bump or post. Chip type can be either MIC or MMIC. The equivalent circuit model can be expressed in Fig. 2.7. Lb and Gb denote the bump inductance and the radiation conductance. C1 and C2 denote the discontinuity capacitance at the substrate and the chip. G1 and G2 denote the loss conductance of the substrate and the chip. In literature, the conductance's effect is believed to be relatively smaller as compared to the inductance and capacitance [14]. Fig. 2.8 is a simplified version of the equivalent circuit model [15]. The impedance of the bump can be derived as following.

$$Z_D = \sqrt{L/(C_1 + C_2)} \tag{2-1}$$

Also, it is believed that, in most cases, the capacitance is the dominating part of the transition so the interconnection can be further reduced to an effective

capacitance [16].

There are many variables which can affect the performance of the system. The first one is chip detuning. Chip detuning happens when the distance between the chip and the substrate is small [17]. Two cases exist based on whether a metal layer exits below the chip circuit or not [18]. With metal lid, it is recommended that the distance between the chip and the substrate be larger than the ground to ground spacing [18]. Otherwise, the impedance will change significantly. On the other hand, without metal lid, the recommended distance is about 30% of the ground to ground spacing [9]. Fig. 2.9 is an example with and without metal lid [16]. It can be seen that the difference of the performance is big, this is because the distance between the chip and the substrate is not big enough to eliminate the detuning effect. However, from the literature, some people said that the higher the bump the worse the s-parameter while other people have opposite data [16][18]. This explanation can be verified by the equivalent model. Fig. 2.10 shows that the inductance is in proportional to the height while the capacitance does not change very much.

From literature, smaller bump cross section results in better s-parameter, but the cross section is limited by the resolution and the aspect ratio of the photo-resist [19]. The bump shape also affects the performance. From one paper, the best result comes from concave bump but in reality it is difficult to fabricate [20]. The distance between signal and ground bump also affect the performance [21]. From two papers, it is concluded that larger pitch results in better performance. From transmission line's point of view, one paper says that smaller line width results in better performance, but there exists a trade off [22]. The

dielectric overlap is defined as distance between chip edge and circuit edge. One paper says that shorter dielectric overlap results in better performance but in reality chips have to leave some areas for dicing [23]. The conductor overlap is also called bump pad length. All of the papers agree that shorter bump pad length or bump pad area results in better performance [16] [21]. It is believed that the main reason for capacitance domination is due to the overlap of bump pad. Comparing overlap with another parameter, it can be found that the former is always dominant one [24].

In 2005, one paper uses statistic method to examine the overall effect and obtain the equivalent circuit model [25]. It also point out the importance of each parameter. As concluded before, the conductor overlap plays the most import role. Bump height and diameter also affect performance to some degree. Sensitivity analysis has also been done to identify the influence of the process variations. Conductor overlap is still first order parameter. The author also examines the mutual influence of the two parameters. From above, reducing bump pad area may be a good way to achieve better performance.

The glob top and underfill are another issue from reliability's point of view. Some papers exam the influence of glob top and underfill on performance [26]. The result shows that adding a glob top or underfill will make return loss degrades about 3 to 5db. It also shows the result is very sensitive to chip size and transmission line length. However, in the reliability test, the result shows that the reliability of underfilled chip is twice than the non-underfilled chip whether the substrate is ceramic or duroid. From the equivalent circuit's point of view, in Fig. 2.11 [27], the underfill material increases the capacitance of the

interconnect and changes the impedance of the circuit. It is recommended that underfill should be used with dielectric constant as low as possible.

To further improve performance, several approaches have been proposed. Fig. 2.12 depicts a way to stagger the signal bump. One paper claims that the best stagger distance is about two times of signal line width [28]. From equivalent model's point of view, staggering the bump increases inductance and decreases the capacitance. It is believed that this is due to electric field concentrates on the air. There is another way to increase the performance. Fig. 2.13 shows a way to use high impedance compensation to match the impedance near the bump [23]. Comparing these two methods, the stagger way can get local minima at particular frequency while the high impedance way can achieve broad band improvement. There are also some papers propose compensation on both side of chip and substrate [29]. The performance is better than one side compensation.

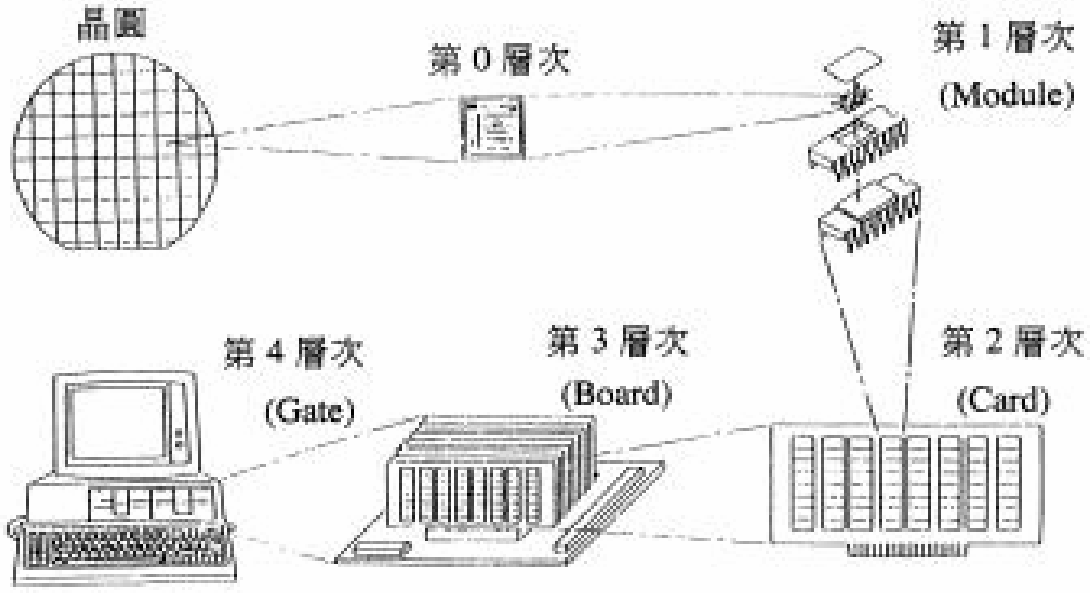


Fig. 2.1 Five levels of electronic packaging.

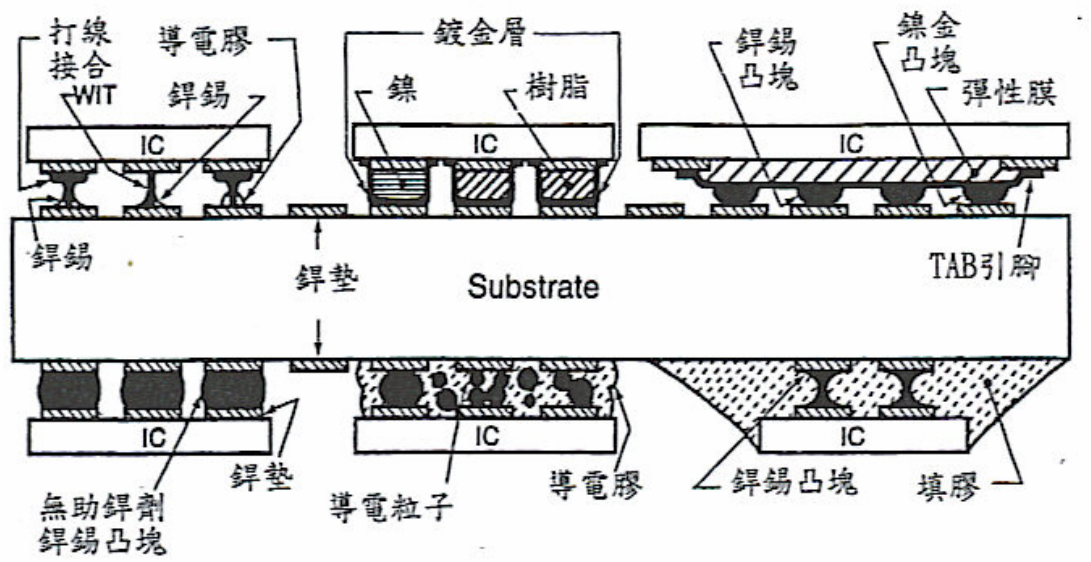


Fig. 2.2 Several approaches of flip-chip assembly.

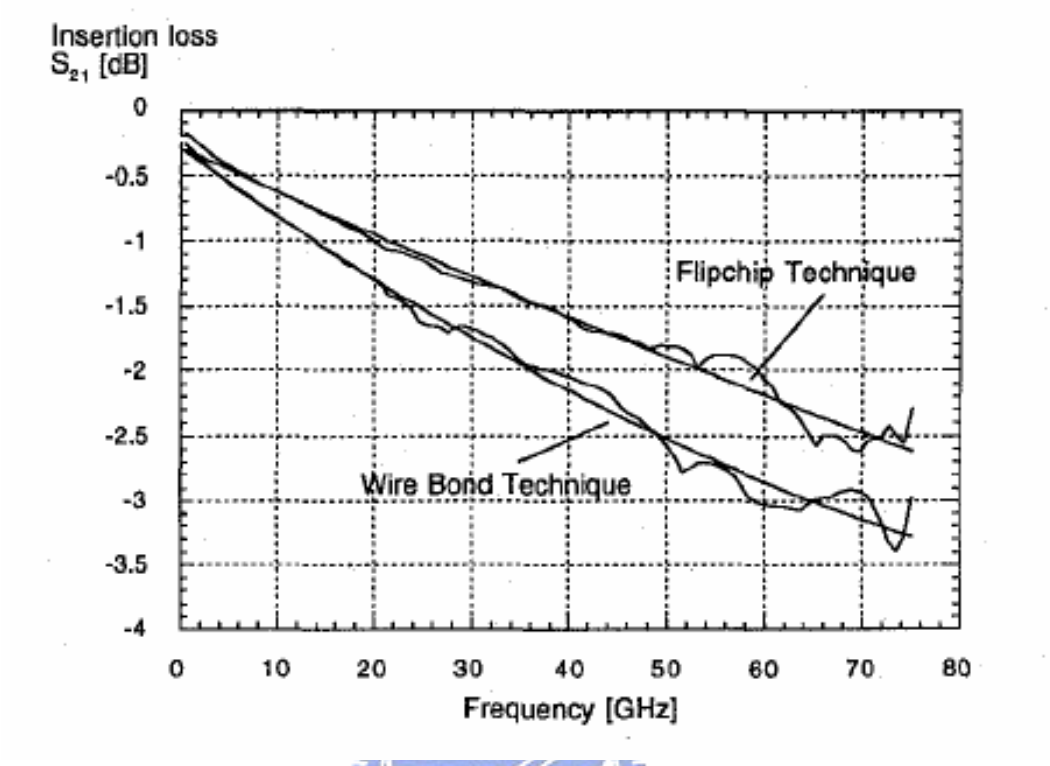
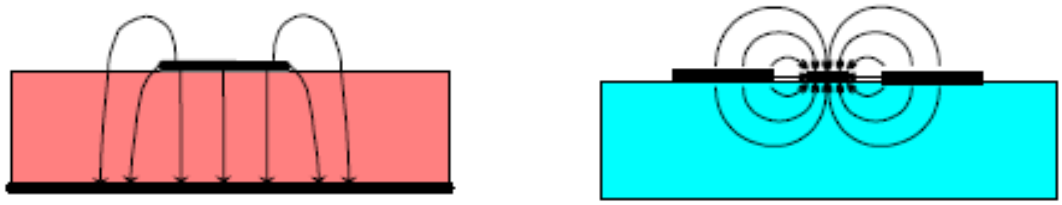


Fig 2.3 Measured insertion loss S_{21} of the flip-chip and the wire bond test assemblies.



Microstrip line on chip or substrate

Coplanar waveguide on chip or substrate

Fig. 2.4 Electric field distribution of microstrip line and coplanar waveguide.

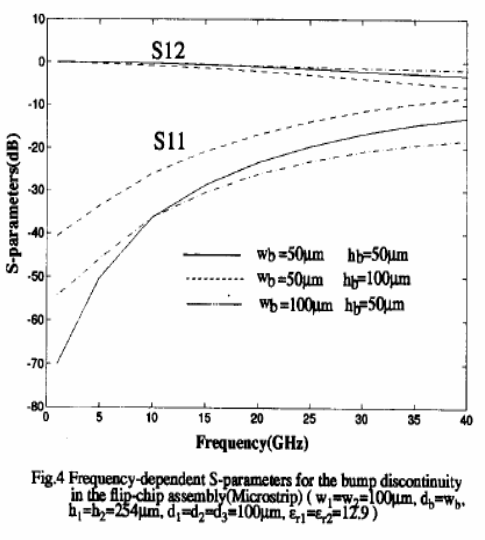


Fig.4 Frequency-dependent S-parameters for the bump discontinuity in the flip-chip assembly(Microstrip) ($w_1=w_2=100\mu m$, $d_b=w_b$, $h_1=h_2=254\mu m$, $d_1=d_2=d_3=100\mu m$, $\varepsilon_{r1}=\varepsilon_{r2}=12.9$)

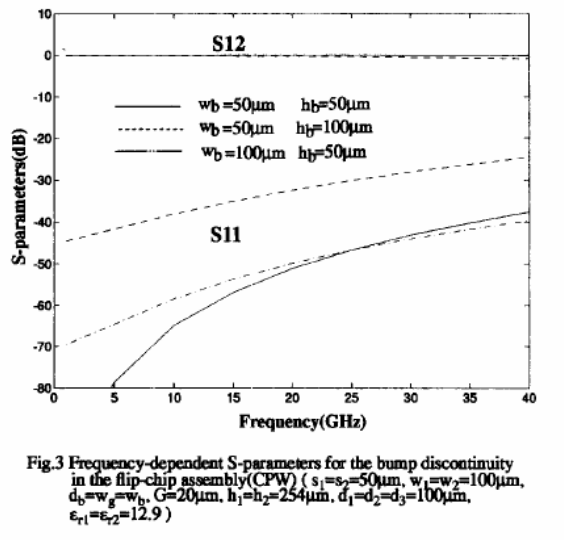


Fig.3 Frequency-dependent S-parameters for the bump discontinuity in the flip-chip assembly(CPW) ($s_1=s_2=50\mu m$, $w_1=w_2=100\mu m$, $d_b=w_g=w_b$, $G=20\mu m$, $h_1=h_2=254\mu m$, $d_1=d_2=d_3=100\mu m$, $\varepsilon_{r1}=\varepsilon_{r2}=12.9$)

MS - MS

CPW - CPW

Fig. 2.5 S-parameter comparison of the microsrip and CPW line with the same physical dimension.

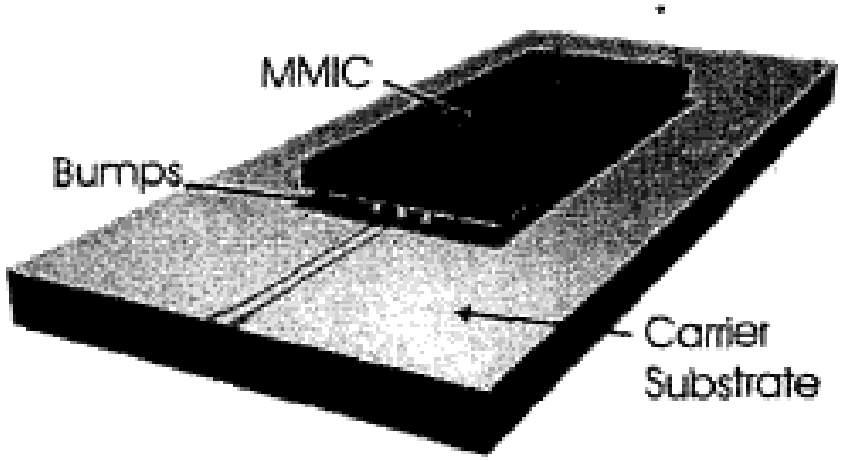


Fig. 2.6 Flip-chip configuration in CPW technology.

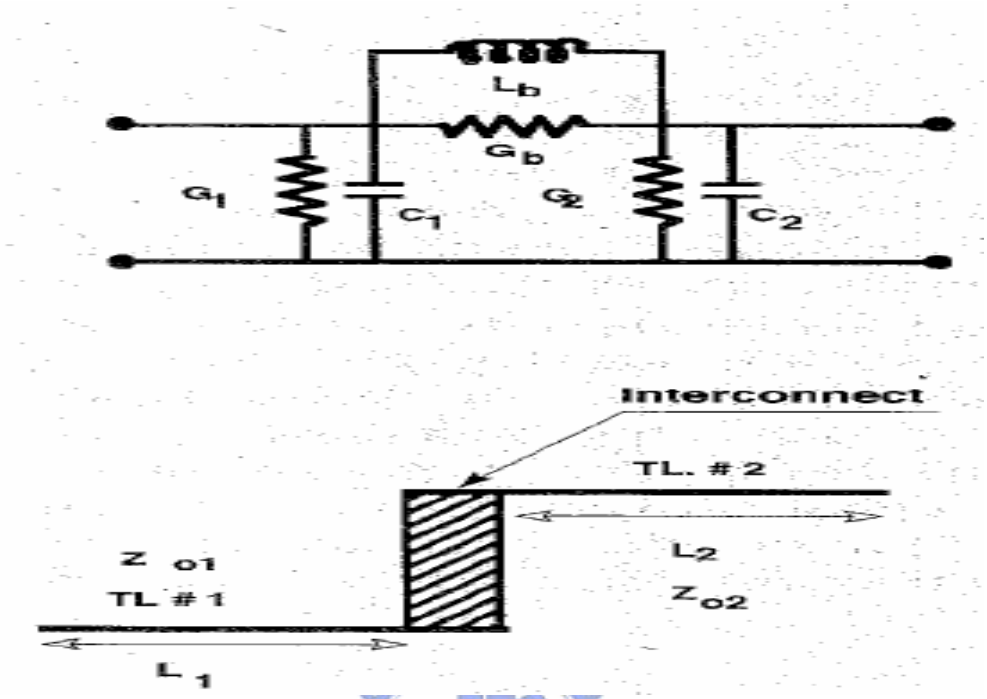


Fig. 2.7 Schematic drawing of the flip-chip equivalent circuit model.

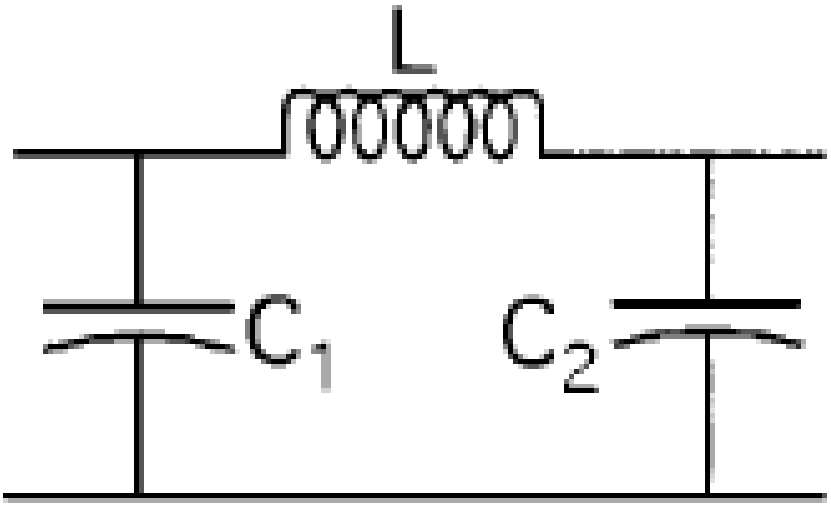


Fig. 2.8 Simplified version of the flip-chip equivalent circuit model.

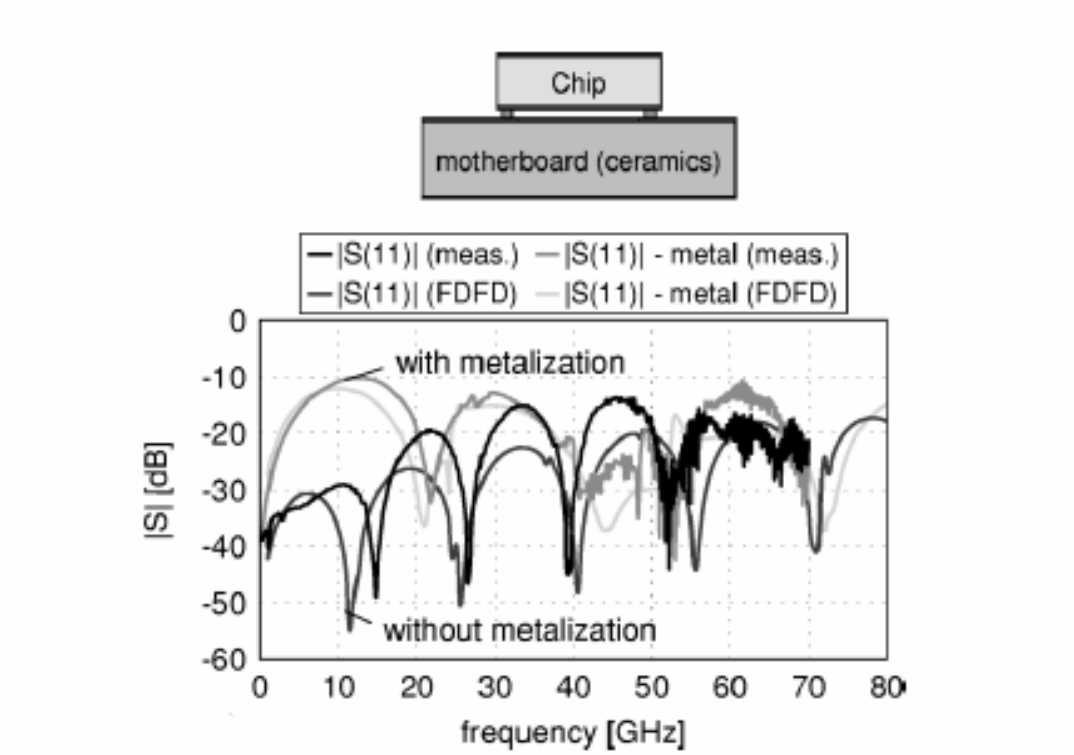


Fig. 2.9 Measurement and FDTD simulation data for the cases with and without the metal lid.

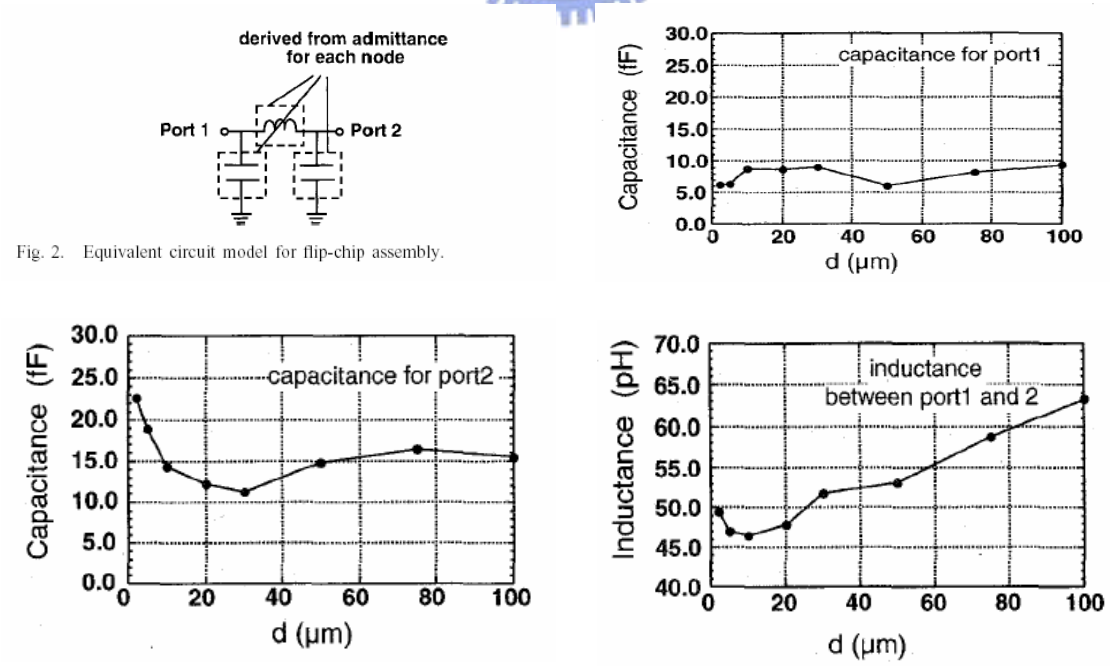


Fig. 2. Equivalent circuit model for flip-chip assembly.

Fig. 2.10 Equivalent circuit model of the flip-chip transition.

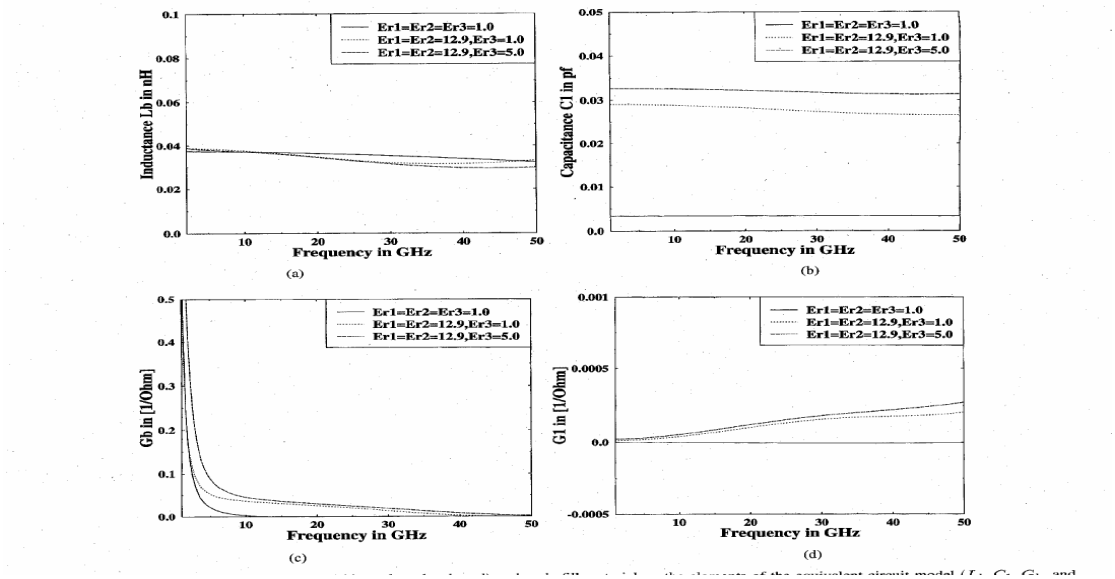


Fig. 2.11 Effect of the dielectric substrate and underfill material on the elements of the equivalent circuit model.

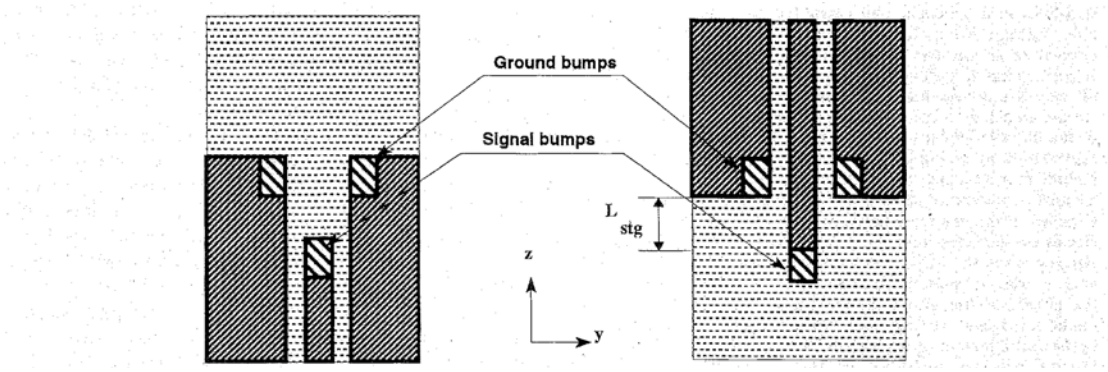


Fig. 2.12 Flip-chip CPW-CPW with staggered bumps (plan view of CPW-chip and CPW-substrate).

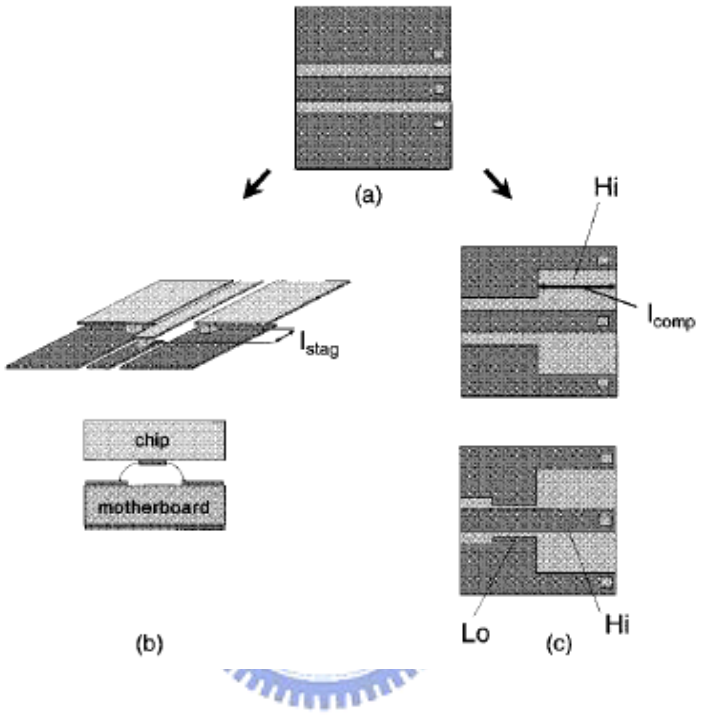


Fig. 2.13 Optimized interconnect design. (a) Without any compensation. (b) Staggered bumps. (c) High and high-low impedance compensation.

Characteristic	Wire Bond	TAB	Flip Chip
Maturity	◎	○	○
Pitch	4-7 mils	3-4 mils	8-10 mils
Max I/O counts	400-500	800-1000	>1000
Projection area	20-100 mils	80-800 mils	<20 mils
Assembly speed	△	◎	◎
Wafer testing	△	◎	○
Cost	$0.001	$0.003~0.01	$0.002

Table 2.1 Comparison of the wire bonding, TAB, and flip-chip characteristics.

Method	Speed	Characteristic	Accuracy
Simulation	Medium	Parameter setting	Need verification
Experiment	Slow	Higher cost	Process variation
Equivalent circuit model	Fast	Simple circuit for designer	Depend on Sim. or Exp.

Table 2.2 Three approaches for obtaining S-parameter.