Chapter 4

High Frequency Flip-Chip

Experiments

This chapter will go through high frequency flip-chip experiments related topics. Basic theory and structure of the coplanar wave guide will be described in section 4.1. After that, theory and process procedure of the electroplating will be described in section 4.2. In section 4.3, a method of bonding a substrate and a flipped chip will be described. RF characteristic is important as a benchmark and will be described in section 4.4. Finally, arming with the knowledge and facility, experiment process flow will be shown in section 4.5.

4.1 Basic Theory and Structure of Coplanar Wave Guide

Since World War II, in order to gather more intelligence from enemies, technology development for applications such as radar exploration and artificial satellite communication was progressing rapidly. These new applications have greatly contributed to the research and development of the microwave technology. At earlier time, metallic waveguide was adopted to transmit high power efficiency electromagnetic waves. In the area of microwave circuit design, it was achieved by the coaxial cable and stripline in the primary stage. Afterward, with the advance of planar circuit, microstrip line gradually became the main stream. However, for the millimeter wave or even higher frequency bands,

microstrip line had its limit in reducing the size and weight. Therefore, Dr. C. P. Wen firstly brought up the idea of CPW (Coplanar waveguide) in 1969.

For understand CPW structure, it has to consider transmission line theory first. The concept figure of a transmission line is illustrated in Fig. 4.1. The voltage, current and power efficiency can be viewed as a transmissive wave. Part of the insertion wave will be reflected back to the power source. The reflected wave is then reflected again and forms a standing wave on the transmission line. If the cross-section of a transmission line is uniform, the equivalent circuit model can be illustrated in Fig. 4.2. The characteristic impedance is defined as following.

$$Z_0 = \sqrt{\frac{L}{C}} \tag{4.1}$$

At high frequency band, 50Ω, 75Ω, 90Ω and 300Ω of the impedances are commonly adopted. However, a transmission line with 50Ω impedance is the most common one. The total voltage and current are the sum of insertion wave and reflected wave, therefore, can be represented as following.

$$V_r = E_{insertion} + E_{reflection} \tag{4.2}$$

$$I_t = \frac{E_{insertion} - E_{reflection}}{Z_0} \tag{4.3}$$

The dynamic characteristics of an electromagnetic wave in a waveguide can be derived from the Maxwell equation. Solutions of the equation can be divided into TEM mode, TE mode and TM mode. TEM mode can only exist in

the structure of multi metallic interconnection, called Multi-conductor Transmission line. Its characteristics are described as following.

(i) Electric field and magnetic field is perpendicular to each other and also perpendicular to the traveling direction.

(ii) Phase of electric field and magnetic field is identical.

If a dielectric material of any transmission line type is uniformly distributed, a single, well-defined electromagnetic wave mode of propagation can exist during transmission at certain frequency. For example, a coaxial cable transmits electromagnetic wave in a single TEM mode. If a dielectric component is not uniformly distributed, however, single TEM mode during wave propagation can not exit even the input signal is single TEM mode. Other modes of electromagnetic wave will be induced during transmission. Even though it is the case for coplanar waveguide, transmission energy which forms inside the substrate would be very close to the distribution of a single TEM mode. Therefore, it can be said that a CPW transmission line transmits energy in a quasi-TEM mode.

The structure of a coplanar waveguide (CPW) is depicted in Fig. 4.3. It is formed from a conductor separated from a pair of ground planes. All of the metal layers are on the same plane, atop a dielectric medium. A variant of coplanar waveguide is formed when a ground plane is provided on the opposite side of the dielectric, which is called finite ground-plane coplanar waveguide (FGCPW), or more simply, grounded coplanar waveguide (GCPW). Compared with microstrip line, CPW has several advantages. (1) It has higher electric

density. (2) It can provide extremely high frequency response (100 GHz or more) since connecting to CPW does not entail any parasitic discontinuities in the ground plane. (3) Insertion loss between active devices and passive devices can be reduced. (4) Backside processes such as wafer lapping and via hole etching can be eliminated, which can save about 30% of the cost. (5) Multilayer process is possible for future 3-D packaging, total volume can be minimized.

One disadvantage is potentially lousy heat dissipation (this depends on the thickness of the dielectric and whether it makes contact to a heat sink). However, the main reason that CPW is rarely used is that there is a general lack of understanding of how to employ it within the microwave design community. Nowadays, only few CAD programs support it. This will change in the years to come as more millimeter-wave work will demand the benefits of CPW. It is worth performing a complete advanced study and more experiments on it.

The characteristic dimensions of a CPW are the central strip width W and the width of the slots s shown in Fig. 4.4. The structure is symmetrical along a vertical plane running in the middle of the central strip. A CPW can be quasi-statically analyzed by the use of conformal mappings. Briefly speaking, it consists in transforming the geometry of the PCB into another conformation, whose properties make the computations straightforward. Considering the simplest case, a CPW of negligible thickness located on top of an infinitely deep substrate, as shown in Fig. 4.5, can be mapped into a parallel plate capacitor filled with dielectric ABCD using the conformal function:

$$w = \int_{z_0}^{z} \frac{dz}{\sqrt{(z - W/2)(z - W/2 - s)}} \qquad (4.4)$$

To further simplify the analysis, the original dielectric boundary is assumed to constitute a magnetic wall, so that BC and AD become magnetic walls too and there is no resulting fringing field in the resulting capacitor. With that assumption, the capacitance per unit length is merely the sum of the top (air filled) and bottom (dielectric filled) partial capacitances. The former is given by:

$$C_a = 2 \cdot \varepsilon_0 \cdot \frac{K(k_1)}{K'(k_1)} \qquad (4.5)$$

while the later is:

$$C_d = 2 \cdot \varepsilon_0 \cdot \varepsilon_r \cdot \frac{K(k_1)}{K'(k_1)} \qquad (4.6)$$

In both formulae K(k) and K/(k) represent the complete elliptic integral of the first kind and its complement, and $k_1 = \frac{W}{W + 2s}$. While K and K/ is difficult to be calculated, the answer of K/K/ ratio can be easily get through the following formulae:

$$\frac{K(k)}{K'(k)} = \frac{\pi}{\ln\left(2 \cdot \frac{1 + \sqrt{k'}}{1 - \sqrt{k'}}\right)} \qquad \text{for} \quad 0 \le k \le \frac{1}{\sqrt{2}} \qquad (4.7)$$

$$\frac{K(k)}{K'(k)} = \frac{\ln\left(2 \cdot \frac{1+\sqrt{k}}{1-\sqrt{k}}\right)}{\pi} \qquad \text{for} \quad \frac{1}{\sqrt{2}} \le k \le 1 \tag{4.8}$$

with k/ being the complementary modulus: $k' = \sqrt{1-k^2}$. The total line capacitance is thus the sum of Ca and Cd. The effective permittivity is therefore:

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} \tag{4.9}$$

It is merely the average of the dielectric constant of the substrate, and that of free space. In the case of GaAs, ε_{re} =12.9, the effective dielectric constant would be (12.9+1)/2=6.95. One way to think about this is that half of the electric field lines are in free space, and half are in the dielectric. The impedance can be expressed as:

$$Z = \frac{30\pi}{\sqrt{\varepsilon_{re}}} \cdot \frac{K'(k_1)}{K(k_1)} \tag{4.10}$$

In practical cases, the substrate has a finite thickness h. To carry out the analysis of this conformation, a preliminary conformal mapping transforms the finite thickness dielectric into an infinite thickness one. Only the effective permittivity is altered; it becomes:

$$\varepsilon_{re} = 1 + \frac{\varepsilon_r - 1}{2} \cdot \frac{K(k_2)}{K'(k_2)} \cdot \frac{K'(k_1)}{K(k_1)} \tag{4.11}$$

where k_1 is given above and

$$k_2 = \frac{\sinh\left(\dfrac{\pi W}{4h}\right)}{\sinh\left(\dfrac{\pi \cdot (W + 2s)}{4h}\right)} \tag{4.12}$$

In most practical cases, the strips are very thin, yet their thickness cannot be entirely neglected. The complete structure is shown in Fig. 4.6. A first order correction to take into account the non-zero thickness of the conductor is given by:

$$s_\varepsilon = s - \Delta \tag{4.13}$$

and

$$W_\varepsilon = W + \Delta \tag{4.14}$$

where

$$\Delta = \frac{1.25t}{\pi} \cdot \left(1 + \ln\left(\frac{4\pi W}{t}\right)\right) \tag{4.15}$$

In the computation of the impedance, both k_1 and the effective dielectric constant are affected. Therefore, k_1 must be substituted by an "effective" modulus k_e, with:

$$k_\varepsilon = \frac{W_\varepsilon}{W_\varepsilon + 2s_\varepsilon} \approx k_1 + (1 - k_1{}^2) \cdot \frac{\Delta}{2s} \qquad (4.16)$$

and

$$\varepsilon_{r\varepsilon}^t = \varepsilon_{r\varepsilon} - \frac{0.7 \cdot (\varepsilon_{r\varepsilon} - 1) \cdot \dfrac{t}{s}}{\dfrac{K(k_1)}{K'(k_1)} + 0.7 \cdot \dfrac{t}{s}} \qquad (4.17)$$

From the formulae derived above, 50Ω transmission line can be obtained by choosing the right signal line width, slot width, substrate material, substrate thickness, and conductor thickness.

4.2 Theory and Process Procedure of Electroplating

Electroplating is a procedure to coat an adherent metal layer on a metal or non-metal surface. Because the plated layer becomes a component of the whole system, this layer is expected to keep its adherence to achieve the purpose of protection, artistry and engineering applications. There are four main parts constructing an electroplating facility. The first part is an outer circuit which includes a DC power supply, a conducting wire, a variable resistor, a voltage meter and current meter. The second part is a cathode which includes a holder and a sample to be plated. The third part is a bath solution. The forth part is an anode which usually composed of the plating metal but sometimes composed of an inert or insoluble material. The whole structure is shown in Fig. 4.7.

The Procedure of an electroplating process in this thesis can be divided into several steps.

(1) Measure the area and calculate the opening areas ratio of a sample. Determine the current density and calculate total applied current by the following formula.

$$J = \rho \cdot A \cdot O.P \qquad (4.18)$$

where ρ is the current density which usually uses Amp/dm^2 as unit. Dm is 1/10 meter, A is the sample area in dm^2 and O.P is the opening ratio without unit. Although the well-known Faraday's law can be used for calculating the plating time, it is found, however, there is a discrepancy between the calculated time and the experiment time. Thus, the best way to find the relation between the plating height of a pattern and the plating time is to do some experiment and find the trend according to the results. Basically, the area and thus the opening ratio is fixed. Thus, total current is in proportional to the current density. Larger current density results in faster plating speed but if the speed is too fast, micro bubbles will appear in the plating structure which will reduce the mechanical strength at the resistance of the plated metal.

(2) The sample is mounted on the holder and connected to the power supply through a conducting wire.

(3) An anode board is set up in the plating bath and the conditions need to be checked before plating.

(4) The power supply is set up and the calculated current is applied.

(5) The mounted sample is rinsed with D.I. water and then immersed into the plating bath. The rinse step is very important because it let the ions flow in and out more fluently. Distance between the sample (cathode) and the anode should be kept a fixed amount of value.

(6) The final step is to check the connection between the power supply and the anode, and also the power supply and the cathode. Set a timer to the desired plating time and push the start bottom of the timer and power supply simultaneously.

In the following subsections, three kinds of materials will be introduced. All of them will be utilized as bump materials in this thesis. Property of the materials and the compositions of the plating bath will be briefly discussed.

Gold Electroplating

Gold is one of the soft metals on earth, it has excellent ductility. It has good electric conductivity and it is very stable under oxygen-rich atmosphere. It has strong resistance to acid and base solutions, only dissolve in a few solutions. Detailed characteristics are listed in Table 4.1. Nowadays, gold electroplating technology has many applications in the areas of microelectronics and micro systems. For instance, connections between FPD (flat panel display) and driver ICs, transmission line and air bridge in GaAs chips, X-ray mask fabrication in LIGA technology. Take the first case for example, driver IC/s and FPD are packaged by the way of TCP (tape carrier packages) or COG (chip-on-glass) technology. This technology is mainly accomplished by gold

bump electroplating. In the area of microwave device and packaging, plating gold is an everyday process in GaAs-wafer fabrication. Therefore, it is not surprising that the first bumps used for most wafer manufactures are gold-plated bumps. It is also compatible with the underlying gold circuits, thus, UBM is not necessary for gold bumps.

In the gold plating bath systems, cyanide bath is the most common one due to its stable and low cost characteristics. There is also non-cyanide bath which is developed for environment friendly purpose. In this thesis, an acid cyanide bath is adopted. Acid bath has the advantages of harmless to the underlying substrate and the purest plated gold can be obtained. The main component of this bath is $KAu(CN)_2$ which is used for supplying gold ions.

During the electroplating process, pre-electroplating is necessary. The electric potential of gold is the highest in all of the elements, thus gold ion is tend to reduce to gold atom in the presence of any element. However, this kind of gold reduction will suffer from poor adhesion. Thus, a pre-plate process is adopted to add a fine grain gold layer before the final plating process.

Copper Electroplating

Copper, a low cost and high conductivity material, is used for interconnection in semiconductor industry recently. Several characteristics are listed in Table 4.2. Compared to gold, copper also has good ductility. The low cost characteristic makes it attractive to be used as a bump material. However, copper has several issues need to be overcome before practical applications. The most common way to fabricate copper interconnection is electroplating. By the

reduction of the copper ions in the aqueous electrolyte, copper atoms can be deposited on the wafer surface. There are two types of electrolytes. One is the base solution and another is the acid solution. The main components of the base solution are copper cyanide and sodium cyanide. On the other hand, the main components of acid solution are copper sulfate, sulfuric acid and hydrochloric acid. In the acid electrolyte case, electroplating is conducted under room temperature. As the current is applied, copper is plated out at the cathode and goes into the solution at the anode as copper(II) ions, maintaining a constant concentration of copper(II) ions in the electrolytic solution. The reaction happens as follows.

$$\text{Cathode}：Cu^{2+}(aq) + 2\ e^- \longrightarrow Cu(s) \tag{4.19}$$

$$\text{Anode}：Cu(s) \longrightarrow Cu^{2+}(aq) + 2\ e^- \tag{4.20}$$

The amount of electroplated copper is proportional to the amount of the charges passed. The plating rate is found to be related to the cupric ion concentration, current density and surface preparation.

Lead Free Solder Electroplating

Solder has been utilized for a long time with the development of human history. However, in the area of electronics packaging, selection of the solder material and the bonding method have become the key research points until SMT (surface mount technology) became the mainstream. In packaging module system, the main function of the solder is to provide the electrical and heat conduction. As a key component of SMT, solder also needs to provide enough mechanical strength to support a device. From the reliability point of view,

solder also has to provide good fatigue resistance. Lead-tin (Pb-Sn) solder is currently the most popular material because of it is low cost and its weldable properties. However, the increasing awareness of the lead bumps pollution danger to the environment stimulated substantial research and development for the lead-free solders. The characteristics of several binary solders are listed in Table 4.3. In this thesis, 99.3Sn/0.7Cu and 96.5Sn/3.5Ag are adopted as the solder bump materials.

To plate alloys, the electric potentials of these two kinds of metals should be close to each other. If the difference of the electrical potential is too big, complexing agents must be utilized to reduce the potential gap. Generally speaking, co-deposit is possible when the potential difference is within 0.2V. Several factors responsible for the alloy qualities. (1) Current density (2) Agitation (3) Temperature (4) PH value (5) Composition of the plating bath. Ultrasonic is utilized in this thesis, the result will be shown in the next chapter.

4.3 Flip-Chip Bonding Process

As mentioned in Chapter 1, there are many methods to fabricate bumps such as electroplating, e-gum evaporating and conductive adhesives. Also, there are many materials which have been used for fabricating bumps such as lead-tin solder, lead-free solder, gold and copper. However, whatever methods and materials are chosen and whether the bumps are on the chip or the substrate, the last step is to join the chip and the substrate together. Bonding is conducted under controlled temperature and pressure. The bonding temperature and pressure depend on the substrate material, chip material, bump material and bump shape. For the low melting point bump materials, solder, for example,

bonding is performed around the melting point and the interface melt and solidify. For the non-reflow bump material such as gold, however, bonding temperature is usually below 1/3 of the melting point. Solid diffusion is the main mechanism in this kind of bonding. The melting points of various materials can be referenced in Table 4.1, Table 4.2 and Table 4.3. There is also an alternative way by adding ultrasonic energy on the interface during the bonding process. It is believed that adding this kind of energy is helpful to lower bonding temperature and bonding time.

In this thesis, a semi-automatic flip-chip/die bonder of M9 series from RD Automation Company is adopted. RD Automation (formerly Research Devices) was founded in 1969 with the purpose of manufacturing high quality production and inspection equipment for the semiconductor industry. RD Automation's systems are used to manufacture components for a diverse array of applications including optoelectronic telecommunications devices, focal plane arrays, high frequency (RF) devices, chip-scale packages, MEMS, liquid crystal displays, and others. The system of the flip-chip bonder is PC-based and running on Windows XP. This allows all functionality to be controlled via mouse or touch screen. An air-bearing stage ensures precision movement for the placement accuracy of ±0.5 μm (application-dependent). Flexibility enhancing features include the closed-loop force and the temperature maintenance, unlimited programmable bonding cycles, adjustable planarity, optional machine vision alignment, bonding by distance, and high force capability (up to 100 kg). The M9 Series are manual flip chip bonding systems used for the process development, prototyping, and low volume production. It is flexible, modular systems that can be setup to address most bonding processes and it is capable of

placing components with an accuracy of ±0.5 μm, and bonding force in excess of 125Kg or as little as 5 grams. The picture of the machine is shown in Fig. 4.8.

Bonding processes are described as follows.

Chip and substrate feeding

The first step is to place a substrate on a tray which lies inside the bonding chamber. After that, a chip will be picked up and placed on another tray which is movable for bonding purpose. After a chip is manually placed to a desired position, the chip will be held by vacuum. The tray with chip will then be flipped faced down to the substrate, complete the final step.

Chip and substrate alignment

To align chip and substrate precisely, two CCDs are placed between the chip and the substrate. One faces up monitoring the chip and another faced down monitoring the substrate. Image signal is transmitted to the computer monitor, thus, real time color images can be seen. Distance between CCD and chip can be adjusted to focus the chip image. Also, distance between the CCD and the substrate can be changed to focus on the substrate image. Schematic drawing of the alignment system is shown in Fig. 4.9. When two images are focused, images are overlapped in the same area. At this time, X axis, Y axis and rotation angle could be fine tuned. Bumps should be located on both sides of the bump pads. After few more checks, both sides of the CCDs are removed away.

Parameter setting

At this step, unlimited programmable bonding cycles are set up with different temperatures and pressures and bonding times according to the bonding

materials. In addition, different bonding temperatures and bonding forces could be applied to the chip side and the substrate side, separately. For example, bonding is divided into 3 steps. In the first step, both chip side and substrate side are heated up to 100℃ for 5 seconds. Applied force is 200 gram. The bonding interface is warming up for next step. In the second step, chip side is heated at 210℃ for 60 seconds while substrate side is heated at 200℃. Applied force is 250 gram. Finally, both chip and substrate are cooled to room temperature, say, 25℃.

Bonding

After the alignment and setting the desired parameters, bonding will be proceed automatically until the final step is done. If the bonding is successful, chip will be bonded on the substrate. The whole package structure will stay on the tray inside the chamber. The completed flip chip package will be shown in the next chapter.

4.4 Experiments

In this section, detailed experiment processes are discussed including chip and substrate fabrication as well as bonding process. The complete process flow is shown in Fig. 4.10.

4.4.1 Chip Fabrication

Circuit and mask design

Gallium arsenide is selected as chip material. Passive chip circuits are designed based on active HEMT device. The referenced HEMT chip is shown in

Fig. 4.11. Five different kinds of chip are designed to exam the high frequency performance.

Seed layer deposition

Seed layer is used to conduct electric current during electroplating process. To do so, a substrate is cleaned to remove particles and then baked on a hot plate at 120℃ in 10 minutes. The purpose of baking is to remove residual water molecular on the surface. After that, TiW and Au are evaporated sequentially by e-gun evaporator. Thickness of TiW and Au layer is about 1000 and 500 Å. TiW is used to enhance the adhesion between the substrate and the gold. Au is the seed layer used in electroplating.

PR Coating

After seed later deposition, the substrate is cleaned again before coating photo-resist. Photo-resist is coated by spin coater in the yellow room of National Nano Device laboratory. The resist is positive tone and its type is S1818. The thickness of the photo-resist is controlled by rotation speed. In this thesis, 3μm circuit is desired. According to the specification, the rotation speed is corresponding to 3000rpm. After some experiments, the parameters were optimized at 1000rpm for 10 seconds and 3000rpm for 45 seconds.

Soft bake

soft bake is conducted on a hot plate at 90℃ for 3 minutes. The purpose of soft bake is to drive out portion of the solvent and to reduce the fluidity.

Exposure

Broad band Karl-Suss MJB-3 Mask Aligner is used for the exposure. After some experiments, the optimal exposure time was set at 30 seconds, without filter.

Post exposure bake

There are two reasons for post exposure bake (PEB). First, it restructures the molecular arrangement of the photo-resist to alleviate standing wave effect. Second, it enhances the solubility of exposure area. Therefore, contrast ratio between the exposed and the un-exposed area is increased. Resolution of the transformed pattern is improved.

Developing

The type of developer is FHD-5. The substrate is immersed into the developer for 1 minute. In the process of developing, the exposure area of the photoresist gradually dissolves in the developer. It is worth mentioning that, in order to improve the quality of the development, slightly shaking is helpful to dissolve the photoresist with better uniformity and without the residual resist.

Hard bake

After developing and checked with the optical microscopy, hard bake is conducted on a hot plate for 1 minute. The purpose of the hard bake is to eliminate the solvent more completely, increase the physical and chemical strengths for further electroplating.

Electroplating

Now the substrate is ready for electroplating. The purpose of electroplating in this step is to thicken the metal on the circuit. The thick metal on the circuit is helpful to maintain the base layer metal during the seed layer etching process. Therefore, gold was electroplated on the evaporated seed layer. There are several things to notice before processing the plating. First, decide the magnitude of the plating current. As mentioned in section 4.2, the plating current is the product of the current density, the substrate area and the opening ratio. If the area and the opening ratio are fixed, the total current is in proportional to the current density. As we know, higher current results in higher plating rate. Thus, it is critical to find a current density and control the plating time to the desired thickness. In this thesis, the substrate is a square with 5cm in length. Convert to the unit used in the electroplating, the area is equal to $0.25dm^2$. Current density is set to 0.3ASD (ampere/ dm^2) and the opening ratio is 0.3 without unit. Total plating time is 9 minutes.

PR strip

Most of the photo-resists dissolve in acetone. Thus, acetone is used to strip the photo-resist. When the substrate is immersed into acetone, photo-resist would totally dissolve in a few minutes.

Seed layer etching

The next step is seed layer etching. Recalling that there are two seed metals. The upper one is Au and the lower one is TiW. KI/I_2 solution is used to etch Au. Etching time is about 10 seconds. TiW is etched by a solution composed of ammonia, hydrogen peroxide, and water (1:1:10). Etching time was about 20 seconds. After DI water cleaning, an GaAs substrate with thick

gold circuit is obtained.

Dicing

The last step is chip dicing. 4 inch GaAs wafer was first thinned to a desired thickness and then mounted. After that, wafer is sawed to individual dies or chips. The results are shown in next chapter.

4.4.2 Substrate Fabrication

Circuit and mask design

As mentioned in section 4.1, the impedance of a CPW transmission line is affected by the signal line width, gap distance between the signal line and the ground line and the substrate dielectric constant, circuit material and thickness. The main target of this thesis is to investigate the impact of S-parameter by different sizes of the CPW lines, the bump layout and also the bump material. Different kinds of layout patterns are shown in Fig. 4.12. Mask design is accomplished by L-edit.

Substrate selection

The main concerns of a substrate are dielectric constant, loss tangent and thermal expansion coefficient (CTE). Dielectric constant affects the impedance of a CPW line. Loss tangent affects the energy transmission in the form of S-parameter. Thermal expansion coefficient affects the robustness of the whole packaging structure. Too much mismatch in CTE between a chip and a substrate would degrade the reliability of the structure. Common choices are PTFE, FR-4, Getek, Alumina (Al_2O_3), Aluminum Nitride(AlN) and Silicon Carbide (SiC). Typical properties of these substrate materials are given on Table 4.4. From all

of them, alumina is the most popular selection for its similar CTE to GaAs chip. The dielectric constant and the loss tangent also make its electrical properties desirable. Therefore, alumina substrate is selected in this thesis.

Circuit fabrication

This step is the same as chip fabrication. After the seed layer deposition, photo-resist is coated and patterned. Then the electroplating was conducted and the photo-resist was stripped after the plating. In the next step, several types of bumps will be fabricated on top of the circuits.

4.4.2.1 Gold Bump Fabrication

The detailed dry film processes has been discussed in chapter 2. The only difference between chapter 2 and this chapter is underlying metal layer. In chapter 2, for testing purpose, dry film is directly laminated on the seed layer without thickened metal circuits. However, in this chapter, dry film is laminated on the seed layer with thickened metal circuits. As mentioned in chapter 2, one of the advantages of the dry film is good planarization effect. Therefore, there is minor influence on the lamination for the circuits with 3μm plated metal.

In the electroplating process, pre-plating is conducted in order to achieve better plating quality. Current density was 0.6ASD and the total plating time was 1.5hr. After the bump fabrication, the seed metal layers were etched.

4.4.2.2 Lead-Free Solder Bump Fabrication

$SnCu_{0.7}$ and $SnAg_{3.5}$ were used as the bump materials in this study. Current density was 5ASD and overall plating time was 2.5 hours. Ultrasonic

energy was adopted during plating process.

4.4.2.3 Copper Bump Fabrication

Three samples were fabricated in this study. One is monolayer dry film without anti-oxidation metal. Another is the monolayer dry film with anti-oxidation metal. The third is double layer dry film without anti-oxidation metal. The feasibility of the double layer dry film has been discussed in chapter 3. For the sample with anti-oxidation layers, metals are deposited by e-gun evaporator after dry film pattern development. Au and TiW were deposited sequentially on the surface and pattern of dry film. After deposition, the metals on the surface of the dry film were removed away. After that, electroplating is conducted just like other samples. After copper bump plating, SnCu solder was directly plated on the copper bumps. Thickness of the solders was about 1~2μm. The purpose of doing so is to provide a bonding layer between the copper bumps and the chip. The results will be shown in next chapter.

4.4.3 Flip-Chip Bonding

The Flip-Chip bonding started with chip and substrate feeding into the bonder. After that, chip and substrate were aligned by computer with images on the CCD screen. Then, bonding parameters were set according to the bump material. Finally, bonding was performed automatically. Detailed steps are described in section 4.3. Several types of substrate patterns were bonded with the matching chips.

4.4.4 S-Parameter Simulation and Measurement

In this thesis, software called "High Frequency Structure Simulator"

(HFSS) was utilized to simulate the bonding structure. It is a full-wave electromagnetic (EM) field simulator for arbitrary 3D volumetric passive device modeling. With proper structure configurations, S-parameter of the simulated structures were predicted. Measurement of S-parameter was conducted using vector network analyzer from 0.5GHz to 40GHz. LRRM calibration was conducted before device measurement. Comparison of the simulation and the measurement results will be discussed in the next chapter.
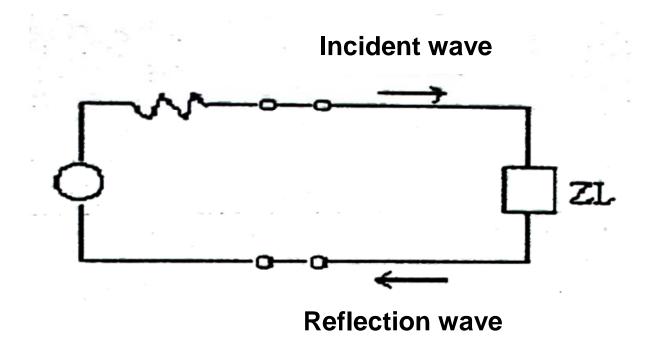
Incident wave

Reflection wave

Fig. 4.1   Concept figure of a transmission line.
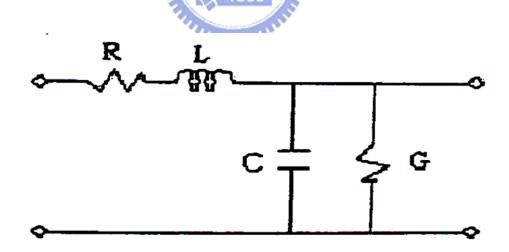
Fig. 4.2   Equivalent circuit model of a transmission line.
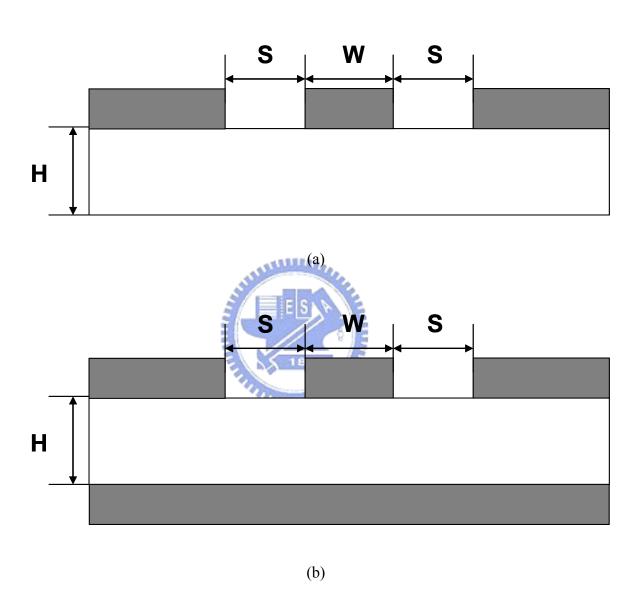
Fig. 4.3　Cross section structures of the coplanar waveguide (a) CPW (b) GCPW.
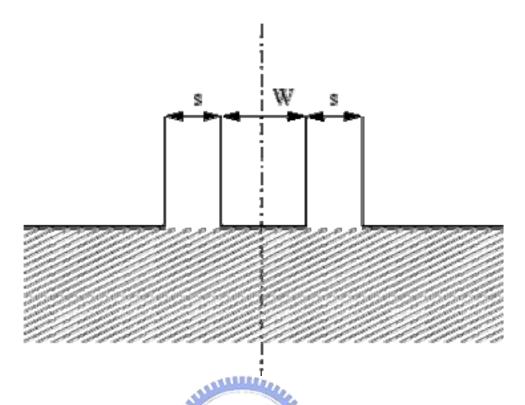
Fig. 4.4   Coplanar waveguide with infinite substrate and zero conductor thickness
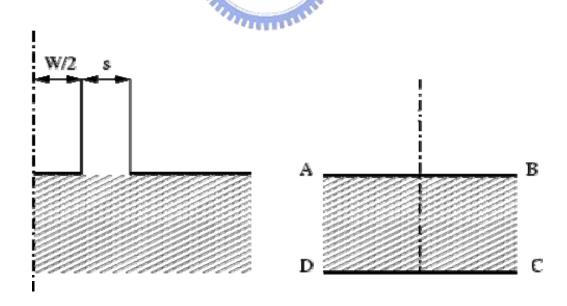
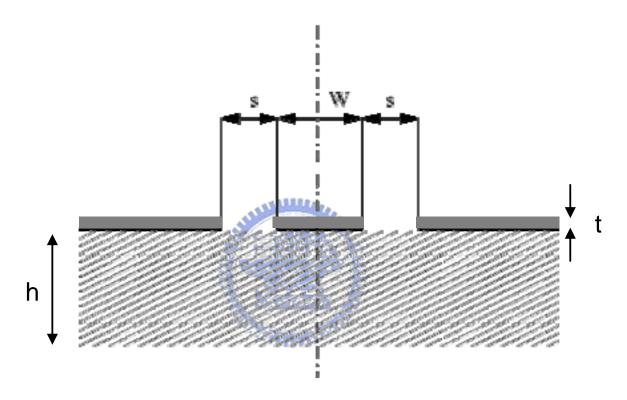Fig. 4.5   Simplified coplanar waveguide for calculating impedance

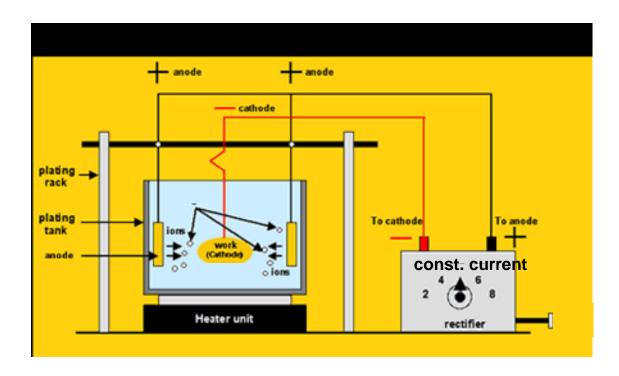Fig. 4.6 Coplanar waveguide with finite substrate and conductor thickness

Fig. 4.7   Main components for a plating facility.

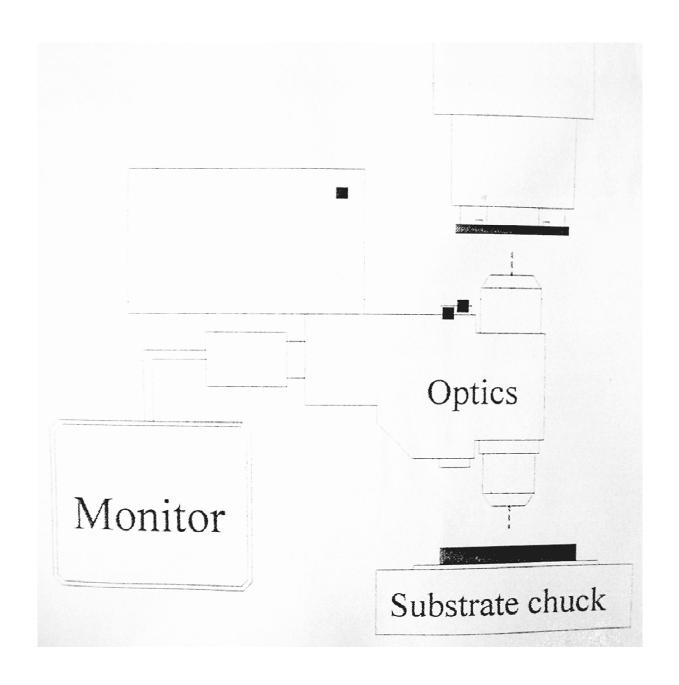Fig. 4.8   Photograph of the Flip chip bonder.

Fig. 4.9　Schematic drawing of a flip chip bonder alignment system.

Process Flowchart

Fig.4.10   The flip chip process flowchart.
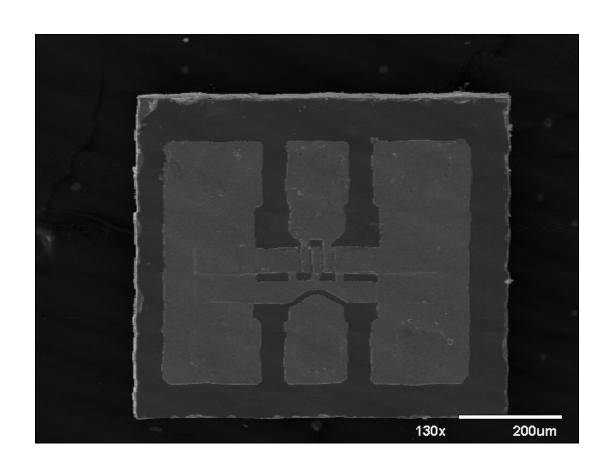
Fig.4.11   Reference HEMT device.
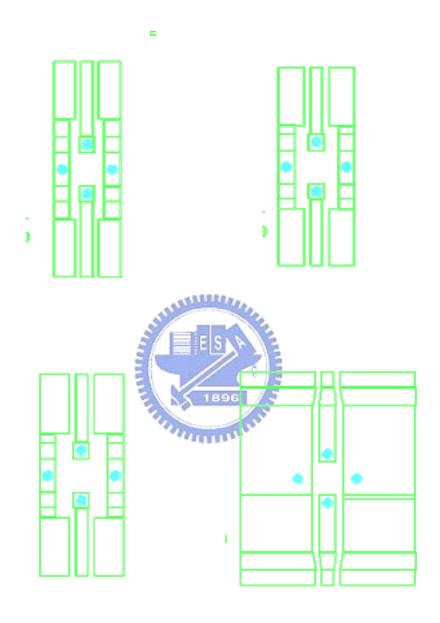
Fig. 4.12   Different kinds of pattern layout.

Atomic Number	79
Atomic Weight	196.9665
Crystal Structure	FCC
Melting Point	1063℃
Boiling Point:	2809℃
Density at 25℃	19.302g/cm
Electrical Resistivity	2.2μΩ-cm
Thermal Expansion Coefficient	14.2ppm/℃
Thermal Conductance	297W/m℃
Standard Electric Potential	$Au \Leftrightarrow Au^{+3}$ +1.50 $Au \Leftrightarrow Au^{+}$ +1.68
Valence	+1 and +3

Table 4.1　　Properties of gold.

Atomic Number	29
Atomic Weight	63.54
Crystal Structure	FCC
Melting Point	1083℃
Boiling Point:	2582℃
Density at 25℃	8.94g/cm
Electrical Resistivity	1.74μΩ-cm
Thermal Expansion Coefficient	17ppm/℃
Thermal Conductance	393W/m℃
Standard Electric Potential	$Cu \Leftrightarrow Cu^{+2}$ +0.34 $Cu \Leftrightarrow Cu^{+}$ +0.521
Valence	+1 and +2

Table 4.2   Properties of copper.

Solder Material	Melting Point	Characteristics	Toxicity
99.3Sn/0.7Cu	227	good thermal fatigue resistance low cost relative high melting point	No
96.5Sn/3.5Ag	221	high mechanical strength good thermal resistance relative high melting point	No
95Sn/5Sb	240	high mechanical strength good creep resistance relatively high melting point	No
91Sn/9Zn	198	good mechanical properties good oxidation resistance poor weld ability poor corrosion resistance	No
63Sn/37Pb	183	excellent in many aspects low cost poor creep resistance	Yes
48Sn/52In	118	good weld ability low melting point high cost	No
42Sn/58Bi	139	good floatability poor welding ability	No

Table 4.3   Characteristics of the binary solders.

Substrate type	Dielectric constant	Loss tangent	In-plane CTE, (ppm/℃)
Pure PTFE (60GHz)	2.1	0.0001	100-120
PTFE with woven glass (10GHz)	2.2	0.0009	12-16
FR-4	4.2-4.5	0.025	12-16
Getek	3.6-4.2	0.010-0.015	12-16
Aluminum, Al2O3, 96%	9.4	0.0006	7
Aluminum Nitride, AlN	8-10	0.0007-0.002	4.5
Silicon Carbide, SiC	40	0.05	3.7

Table 4.4   Properties of various substrate materials