Chapter 5

Results and Discussions

5.1 Process Results

5.1.1 Uniformity of Electroplating

The Gold and Copper plating uniformities were investigated. Fig. 5.1 shows the test patterns. Bumps are numbered from 1 to 4. Plating parameters are described in section 4.4.2. After plating, the bump heights were measured by SEM. Table 5.1 shows the measured results. For gold bumps, one hour plating resulted in 31.8μm average bump height. Good uniformity was observed. Further increase of the plating time to 1.5 hours, the average bump height was about 53.8μm. This height was taller than the dry film, so mushroom shape at the top of the bumps was observed. One way to overcome this problem is removing the overplated parts by sandpaper. For copper bumps, 1.5 hours plating results in 30.3μm average bump height. However, from the table, it can be seen that there is a large gap between minimum bump height and the maximum bump height, this can cause problems during bonding process. Increasing the plating time to 2 hours, average bump height was about 45.5μm and uniformity was good.

5.1.2 Double Layer Dry Film Electroplating

As described in section 3.5, double layer dry film were laminated and patterned sequentially. Plating parameter is described in section 4.4.2. Recalling from section 5.1, plating time for monolayer copper bump is about 1.5 hours. However, in the case of double layer copper bump, plating time is increased to 11 hours. The possible reason is higher aspect ratio and the larger bump size of upper layer. Fig. 5.2 shows the SEM picture of the electroplated bump. From the picture, 93μm bump height can be observed. Owing to the double laminating, the first layer of the dry film was heated under laminator twice, results in longer stripping time.

5.1.3 Chip fabrication results

Chip fabrication process is described in section 4.4.1. The results are shown in Fig. 5.3. After dicing, the chip length was 550μm and the chip width was 700μm. Chip thickness was thinned from 650μm to 250μm. The signal line width was 100μm and the ground line width was also 100μm. For upper left figure, gap between the signal line and the ground line is 100μm. Signal line and ground line length is 400μm. For upper right figure, gap between the signal line and the ground line is 100μm. The signal line length is 400μm and the ground line length is 300μm. For middle left figure, gap between the signal line and the ground line is 100μm. The signal line length is 400μm and the ground line length is 100μm. For middle right figure, the gap between the signal line and the ground line is 75μm. The signal line length is 400μm and the ground line length is 100μm. For lower left figure, the gap between the signal line and the ground line is 50μm. The signal line length is 400μm and the ground line length is

100μm.

5.1.4 Substrate fabrication results

Substrate fabrication process is described in section 4.4.2. The results are shown in Fig. 5.4. Patterns with stagger bumps are fabricated; each signal bump is lying in the middle of the circuit. Different pitches of bumps are shown. For upper left figure, the pitch between the ground bumps is 300μm. For upper right figure, the pitch between ground bumps is 360μm. For lower left figure, the pitch between the ground bumps is 400μm. For the lower right figure, the pitch is 350μm and ground line width is increased to 430μm. Fig. 5.5 shows the alpha stepper test result. It shows the thickness of the circuit is about 3.2μm. Subtracting thickness of the two seed layers to the metal thickness in the circuit, the resulting thickness of the metal is about 3μm. According to section 4.1, calculated impedance of the transmission line ranges from 47 to 54Ω. Same results are observed from the chip side.

For bump structure, electroplated gold bump is shown in Fig. 5.6 and Fig. 5.7. Copper bump is shown in Fig. 5.8 and Fig. 5.9. It is noticed that from Fig. 5.9, a thin SnCu layer of 2μm thickness is electroplated on top of the copper bump. This layer is used for bonding purpose. The SnCu bumps are shown in Fig. 5.10 and Fig. 5.11. The SnAg bumps are shown in Fig. 5.12 and Fig. 5.13. Compare these two materials, SnAg bumps has smoother surface.

5.1.5 Flip chip bonding results

Substrates with gold bumps and copper bumps were bonded to the

matching chips. The former (gold bump) was bonded at 300℃ for 90 seconds under a pressure of 200g. Bonding process was very smooth and successful. Small distortion of the bump height was observed. The later was bonded at 240 ℃ for 30 seconds in the pressure of 100g. However, large distortion of the bump height was observed. Fig. 5.14 shows the distorted bump after bonding. During heating and compression, bumps were flattened while total volume remained the same. Fig. 5.15 shows the flattened bump height is about 22μm and the diameter increases from 60μm to 80μm. From the literature, higher bump and smaller diameter are beneficial for S-parameters. Thus, the measurement results of the S-parameter would degrade to some degree.

5.1.6 Cladding Layers Fabrication Results

The high frequency performance of the alumina substrate with copper bump is confirmed. However, copper has oxidation issue which has to be overcome. Novel cladding metal fabrication process is proposed in this these and compared with US patent 20040166661A1 (Method for forming copper bump anti-oxidation surface). In the beginning, first Ti layer was deposed on the bond pad and passivation layer. After that, a polymer layer was coated and patterned on the first Ti layer. Thick film photo-resist was then coated and patterned following by the second Ti layer deposition. Copper bumps were electroplated and the photo-resist was stripped. Second Ti layer was etched away. Cladding metals were deposited by electroplating or electroless-plating nickel and gold sequentially on copper. Finally, polymer layer and the first Ti layer were etched away sequentially.

In this thesis, novel approach is proposed as following. First, dry film photo-resist is laminated and patterned directly on the evaporated Ti and Au layers. After that, cladding Au and Ti layers are evaporated sequentially. Notice that the sequences of the cladding layers are in reverse order of the seed layers. Then, cladding layers on top of the dry film are removed away. Copper bumps and SnCu solder are plated and after that, the dry film is stripped. Fig. 5.16 illustrates the final structure after completion. Compared with the approach of the patent described, the approach proposed has some advantages. For example, the polymer layer can be eliminated and there are less photolithography steps than the approach in the patent. Plating processes are also less than the approach in the patent, thus the overall processes become simpler and faster with the proposed approach. In addition, full coverage of the gold cladding layer is accomplished in our approach. It can be noticed that in the patent approach, Ti layer is exposed to the atmosphere. Fig. 5.17 shows the result after removing the surface metals. Magnified picture of a single pattern is shown in Fig. 5.18. From these pictures, a shining layer surrounded by dry film is observed. Fig. 5.19 shows the side view of the dry film with and without the cladding metals. Clearly, surface profiles are different.

One concern of the proposed process is the adhesion of the cladding metals when dry film is stripped. Fig. 5.20 shows the final structure of a copper bump with cladding metals. It can be seen that the cladding metals still surrounded the copper bumps. Further investigating of the layer by EDX confirms the assumption. The EDX result is shown in Fig. 5.21. Gold peak is observed and the copper peak is observed as well. Because the X-rays are generated in a region about 2μm in depth, appearance of the copper peak is

explained. Another concern of the proposed process is plating issue. Because the cladding metal layers are covered from bottom to side wall, copper would be plated from both bottom and side direction. Thus, large void may form after process. Fig. 5.22 shows the cross section of a 60μm bump. A large void is found in the center of the bump. However, for bumps smaller than 50μm as shown in Fig. 5.23, no void was found. It can be concluded that the proposed process is suitable for bumps with smaller diameters.

5.1.7 Shear Strength Results

The shear strength of the 60μm diameter electroplated bumps was investigated. Testing procedure is shown in Fig. 5.24. First, a metal probe is placed close to a bump. Second, the metal probe is slightly tapping the substrate surface to set a ground plane. Third, measurement height is set. Finally, the metal probe moves horizontally and measures the shear force. Results for gold bumps are shown in Fig. 5.25. Maximum shear strength was 44.91gm and minimum shear strength was 37.21gm. Mean shear strength was 37.21gm. Results for the copper bumps are shown in Fig. 5.26. Maximum shear strength was 40.01gm and the minimum shear strength was 30.05gm. Mean shear strength is 31.22gm. The difference between the shear strengths of the gold bump and the copper bump was 11.62gm. Results for SnCu bumps and SnAg bumps are shown in Fig. Results for SnCu and SnAg bumps are shown in Fig. 27 and Fig. 28. Weaker shear force was found.

5.2 RF and Microwave Measurement Results

As described in section 5.5, copper bump was flattened during bonding process. Simulation structure was designed to the changed size. First, meddle

right chip of Fig. 5.3 and lower right substrate of Fig. 5.4 are bonded. S-parameter of both substrates with gold and copper bumps are measured. Measured results are shown in Fig. 5.29 and Fig. 5.30. Simulation result is shown in Fig. 5.31. It can be seen that three of the figures are almost the same. From 0.5GHz, S_{11} increases with increasing frequency. The worst S_{11} is about -12dB at 24GHz. After 24GHz, S_{11} decreases gradually to -17dB at 40GHz. S_{21} is larger than -0.4dB in the range of the measurement. It can be concluded that the high frequency performance of the copper bump and the gold bump are almost the same and the simulation results match measurement results excellently well from 0.5GHz to 40GHz.

Next, different kinds of patterns were compared to find the optimized high frequency performance. For the lower left chip in Fig. 5.3 and upper left substrate in Fig. 5.4, simulation and measurement results are shown in Fig. 5.32 and Fig. 5.33 respectively. From the two figures, simulation and measurement agree well for S_{11} but have a little deviation for S_{21}. From 0.5GHz, S_{11} increases with increasing frequency. The worst S_{11} is about -17dB at 24GHz. After 24GHz, S_{11} decreases gradually to -28dB at 40GHz. S_{21} is larger than -0.3dB in the range of measurement. For the middle right chip in Fig. 5.3 and upper right substrate in Fig. 5.4, simulation and measurement results are shown in Fig. 5.34 and Fig. 5.35 respectively. From these figures, simulation results shows more optimistic prediction than the measurement. For Fig. 5.35, S_{11} increases with increasing frequency from 0.5GHz to 21GHz. However, it is different from other cases discussed before, there exits a dip at 35GHz. The S_{11} ends in -24dB at 40GHz. S_{21} is again larger than -0.3dB in the range of measurement. For the middle left chip in Fig. 5.3 and lower left substrate in Fig. 5.4, the simulation and

measurement results are shown in Fig. 5.36 and Fig. 5.37 respectively. From these figures, trend of simulation resembles the measurement result except some peak shift. For simulation, peak occurs at 14GHz. For measurement, peak occurs at 18GHz. 4GHz peak shift is observed. The S_{11} is below -20dB from 0.5GHz to 34GHz. After 34GHz, S_{11} rises again and ends in -15dB at 40GHz. S_{21} is again larger than -0.3dB in the range of the measurement. Comparing these three patterns, it can be seen that different staggered pitches resulted in different S-parameter results. As discussed in chapter 2, flip chip bump transition acts like effective capacitance. Increasing stagger distance acts like increasing inductance. Thus, when capacitance and inductance balanced well, the optimized results would be obtained. This is the case of Fig. 5.35. For Fig. 5.33, capacitance is dominated so the compensation for the inductance was not enough. For Fig. 5.35, capacitance and inductance balance well so the results were optimized. For Fig. 5.37, inductance seems dominate over 28GHz so the inductance compensation is a little more over. It is concluded that tuning the inductance part by controlling the distance of the staggered bumps with the aid of the simulation tool can find the optimized S-parameter results before the flip chip fabrication.

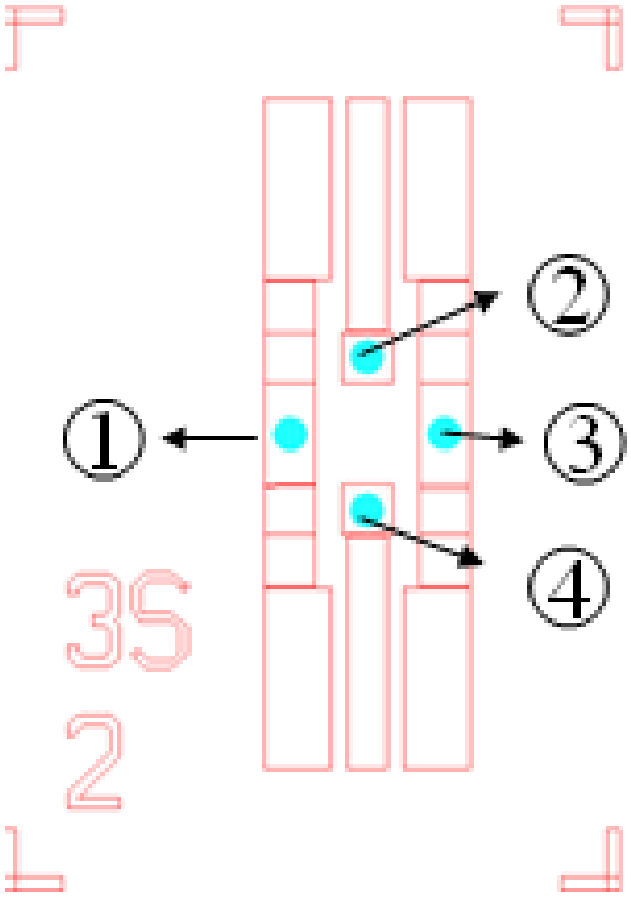

Fig. 5.1 The pattern for plating uniformity test.

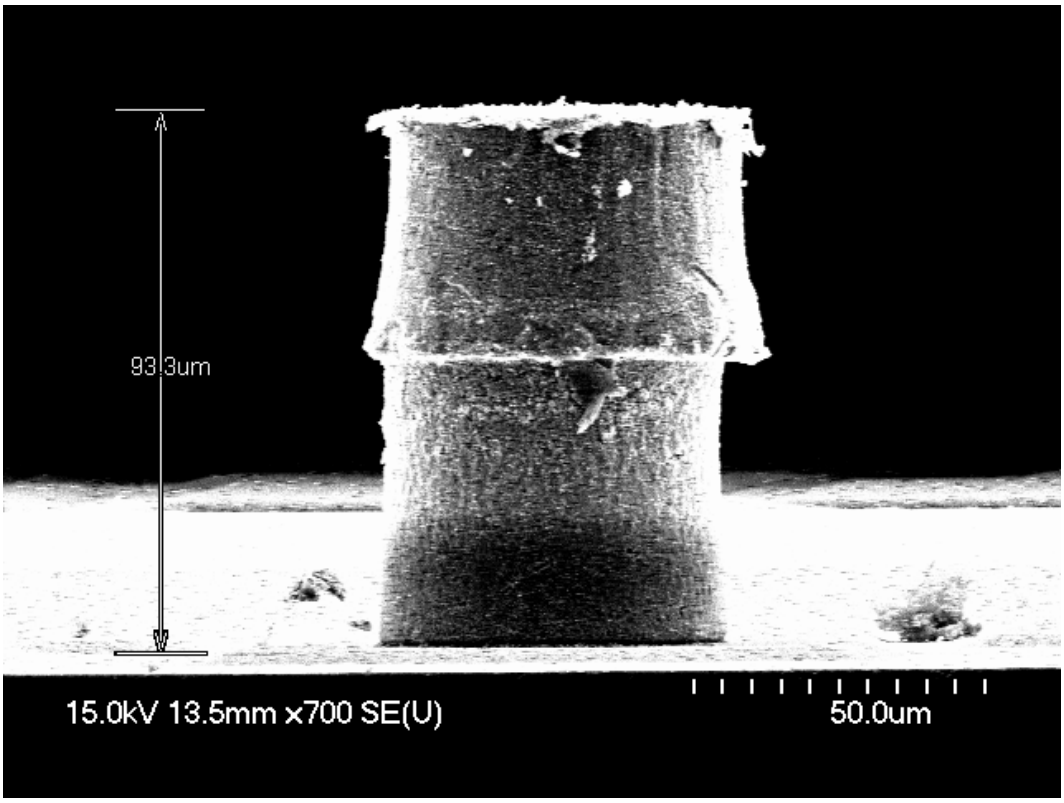

Fig. 5.2 SEM picture of a double layer plated copper bump.

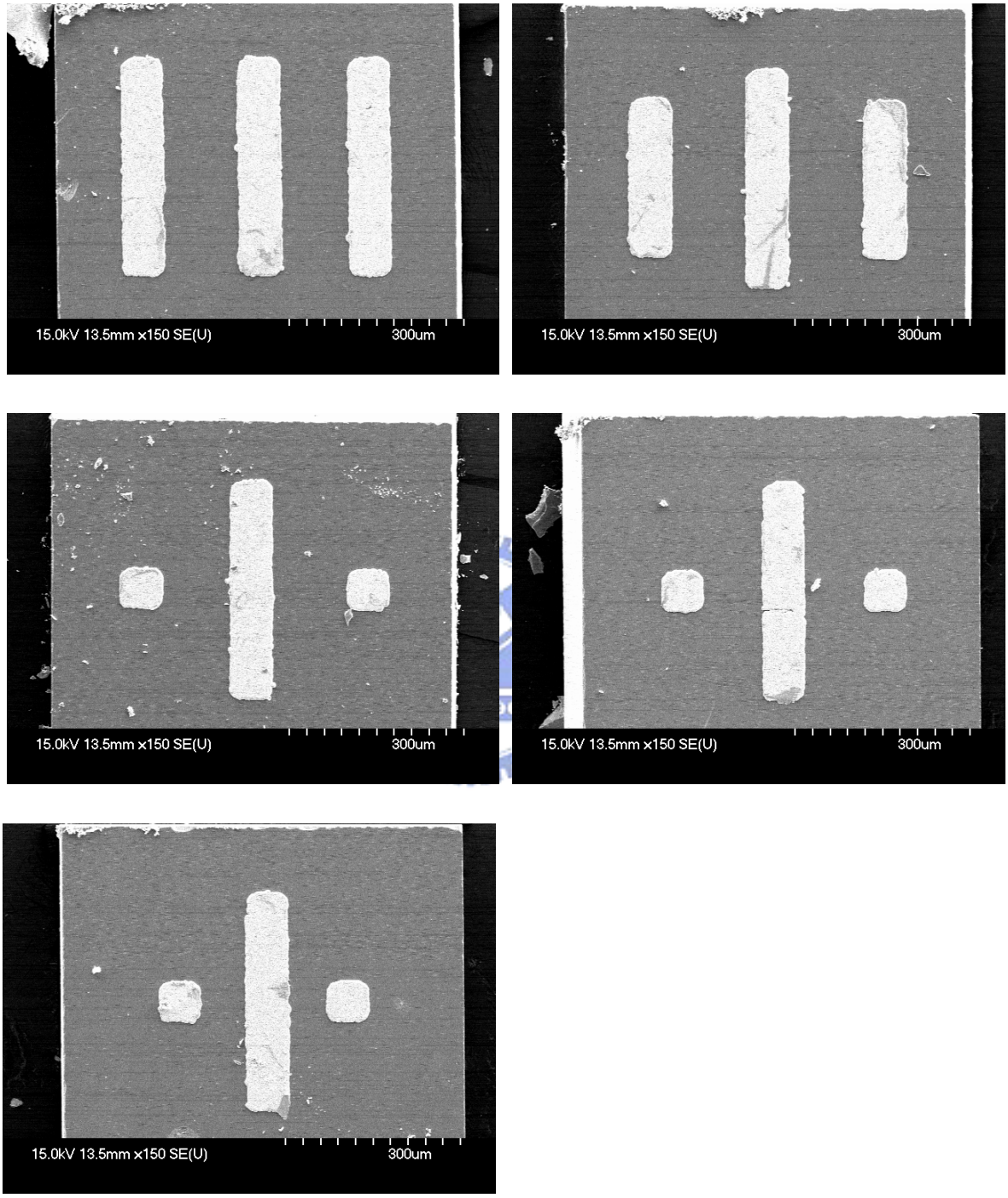

Fig. 5.3 SEM pictures of the fabricated passive chips.

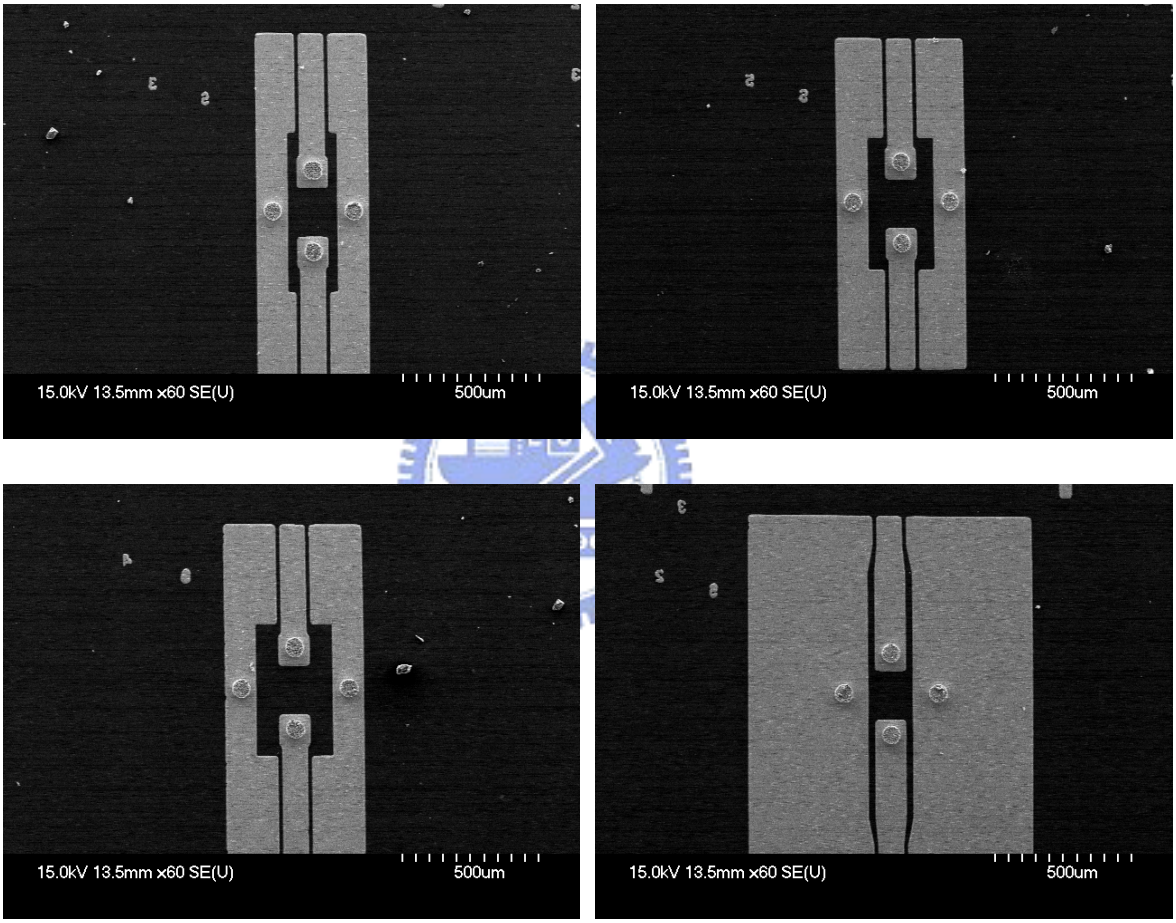

Fig. 5.4 SEM pictures of the fabricated substrates with bumps.

Fig. 5.5 Alpha stepper result of the metal thickness of the substrate circuit.

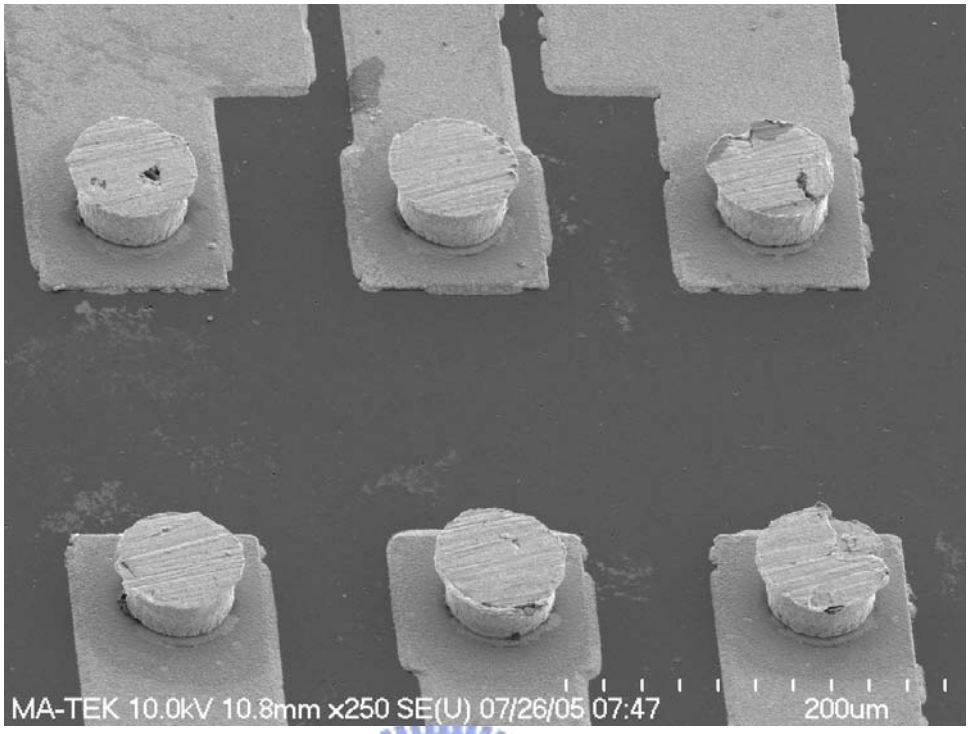

Fig. 5.6 SEM picture of the substrate with gold bumps.

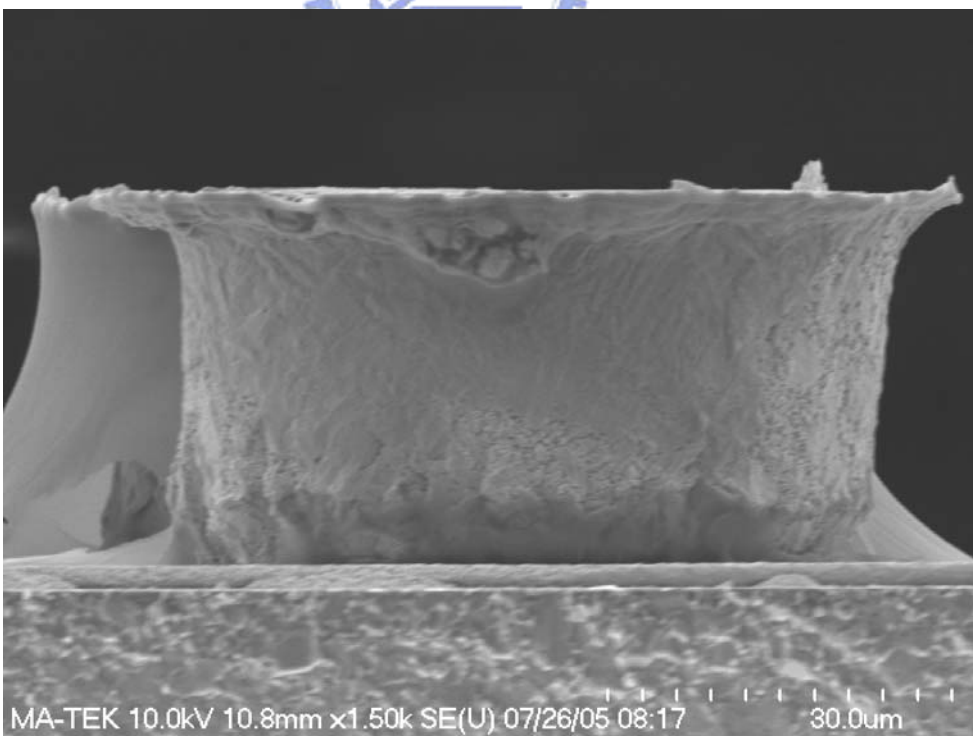

Fig. 5.7 SEM picture of a single gold bump.

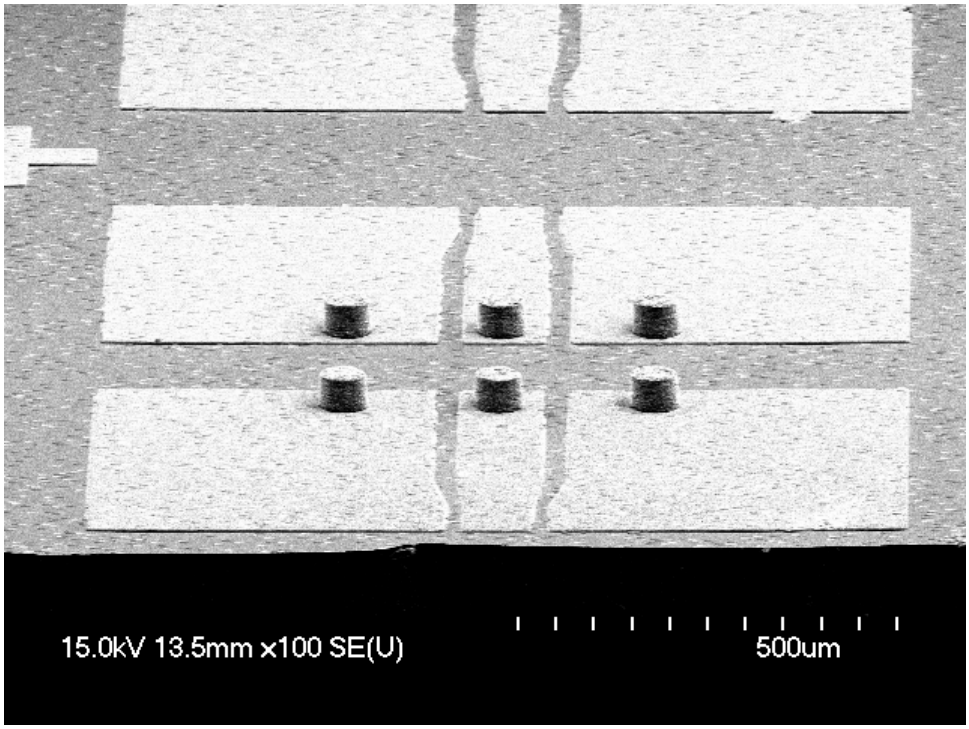

Fig. 5.8 SEM picture of the substrate with copper bumps.

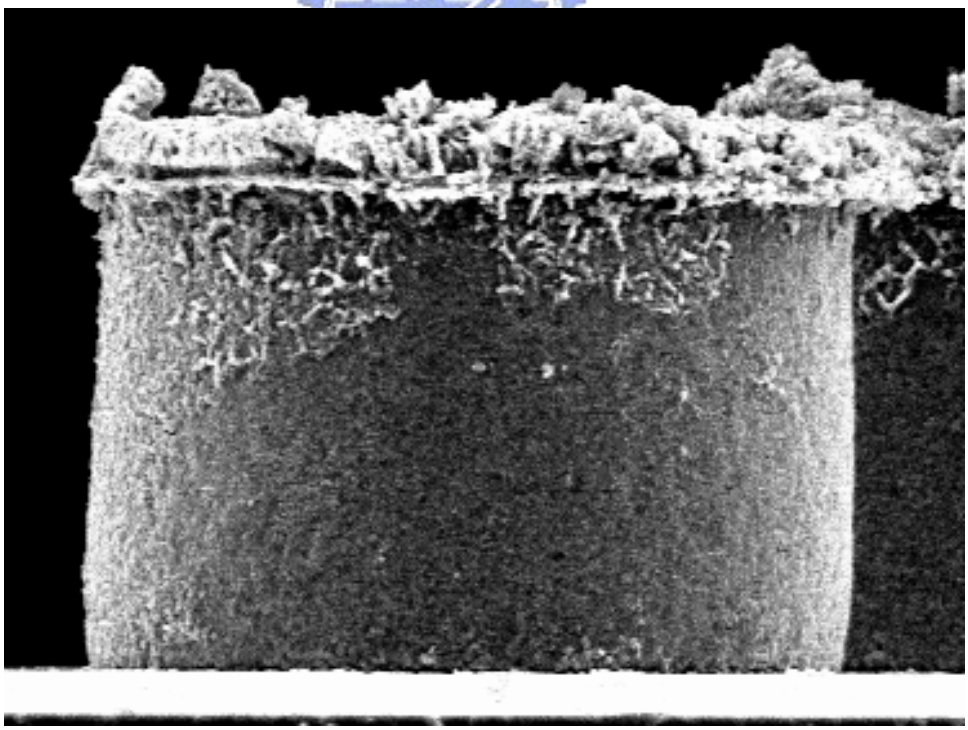

Fig. 5.9 SEM picture of a single copper bump.

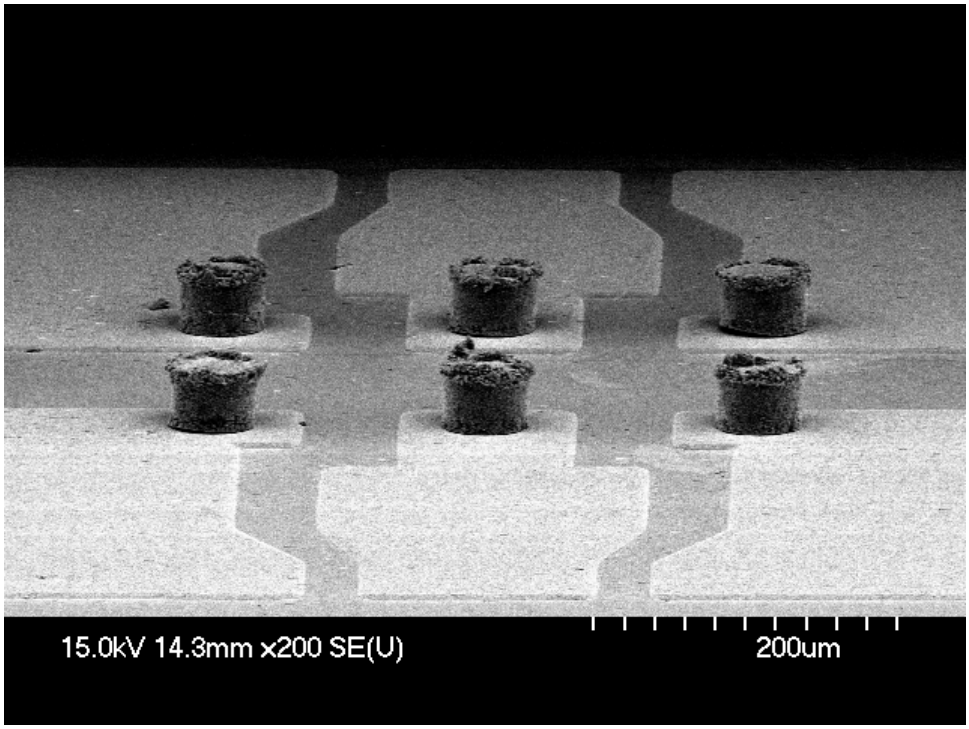

Fig. 5.10 SEM picture of the substrate with SnCu bumps.

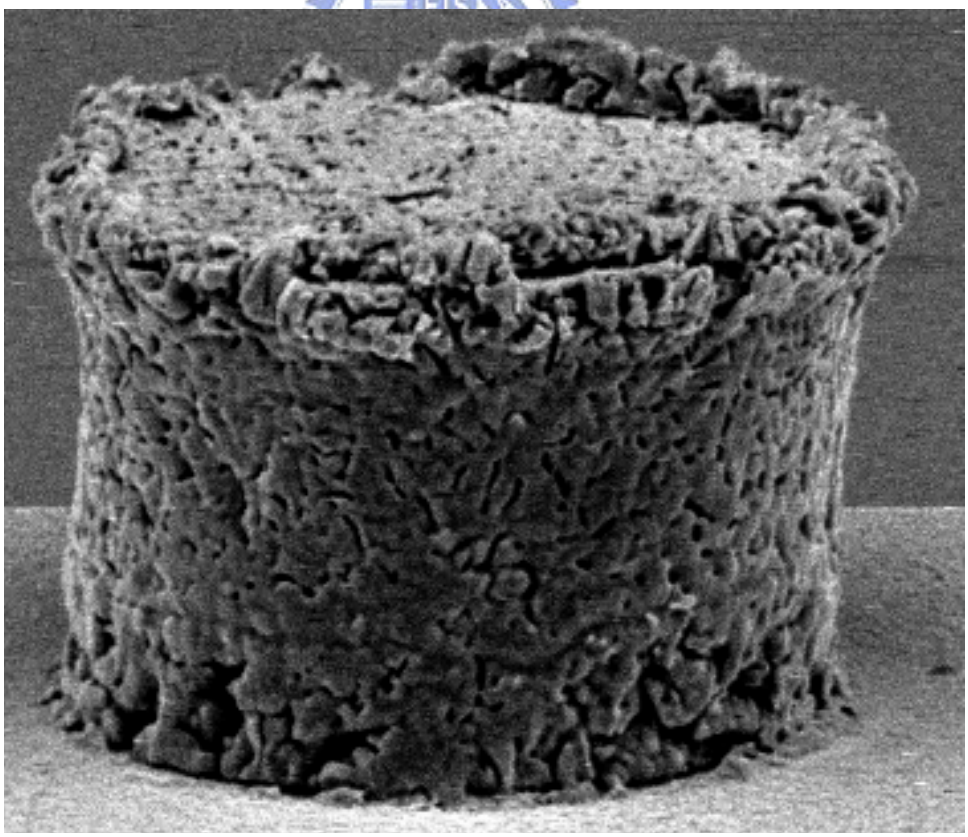

Fig. 5.11 SEM picture of a single SnCu bump.

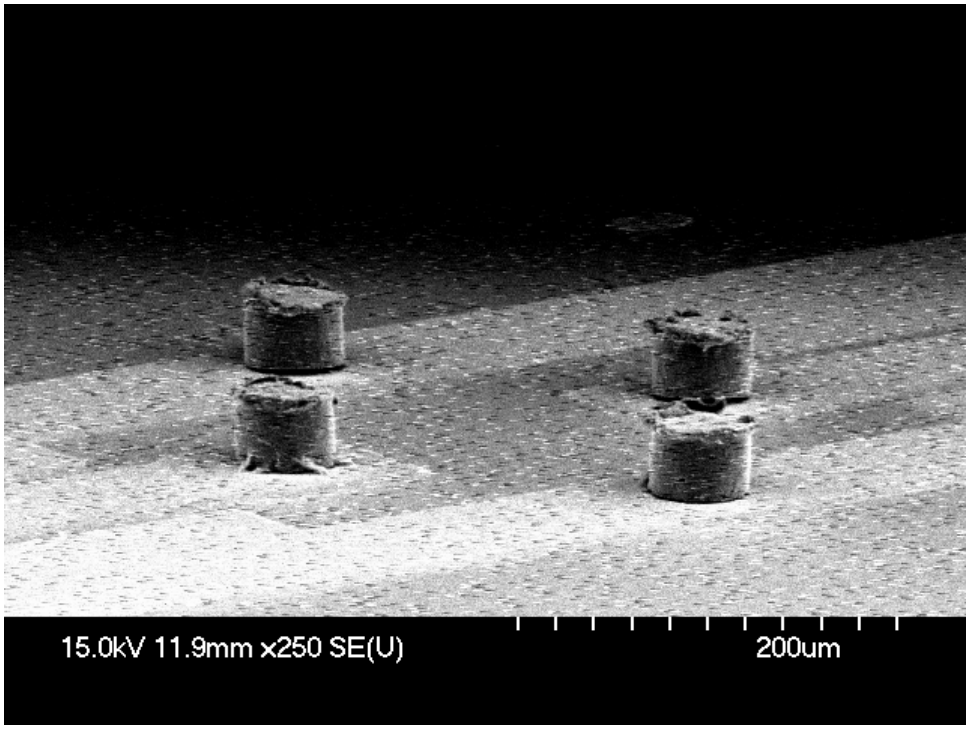

Fig. 5.12 SEM picture of the substrate with SnAg bumps.

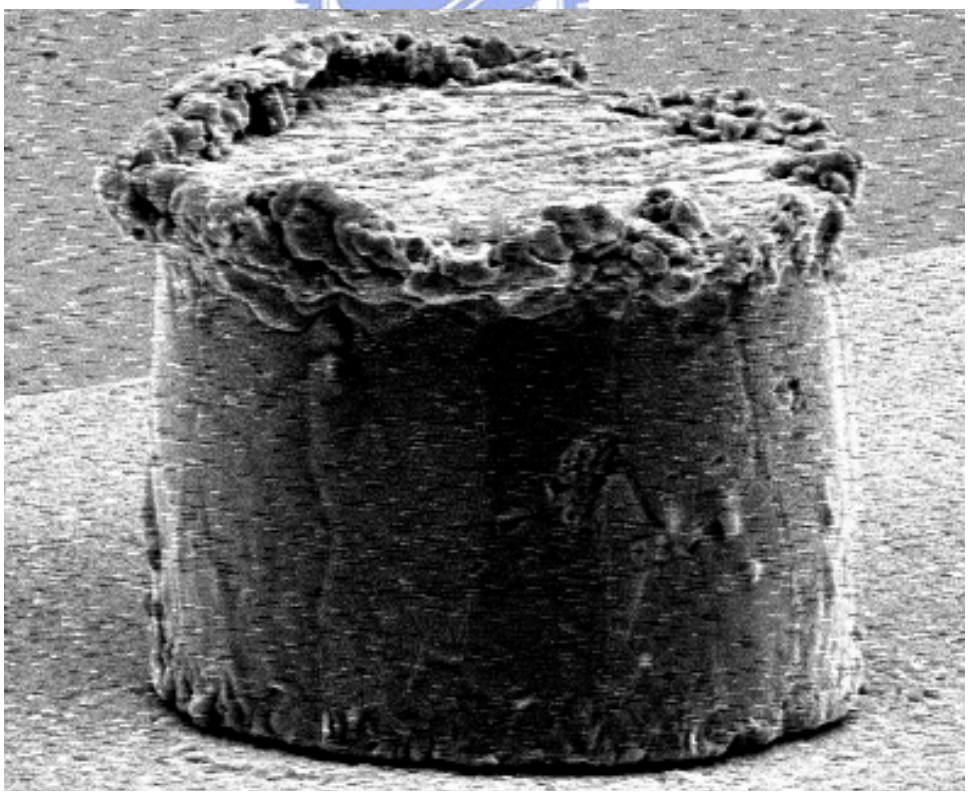

Fig. 5.13 SEM picture of a single SnAg bump.

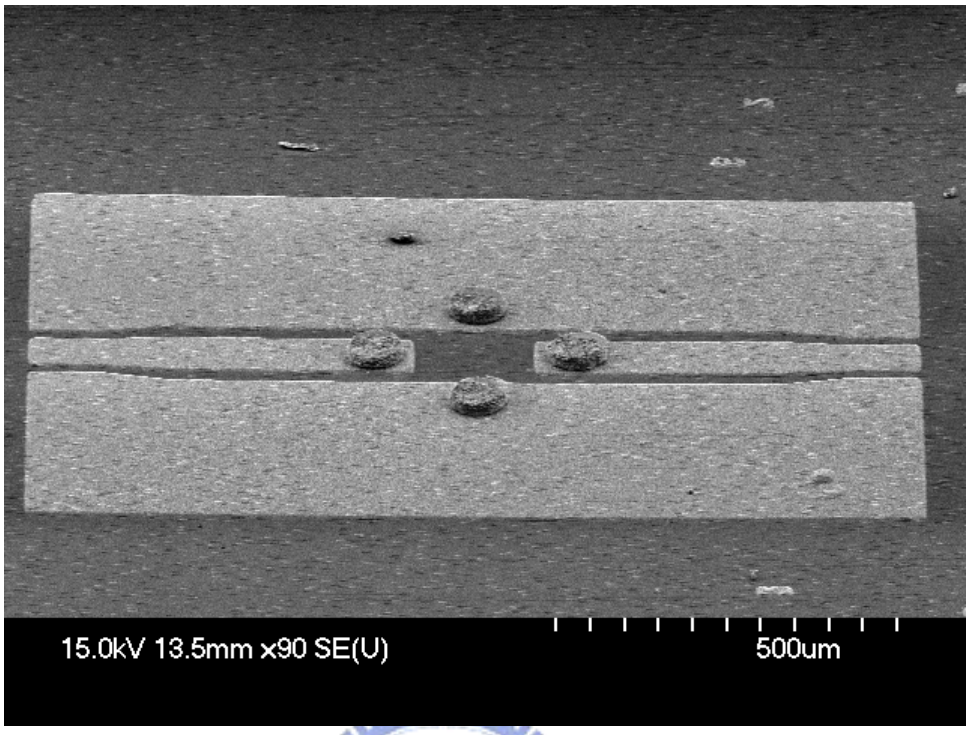

Fig. 5.14 SEM picture of the substrate with bumps after bonding.

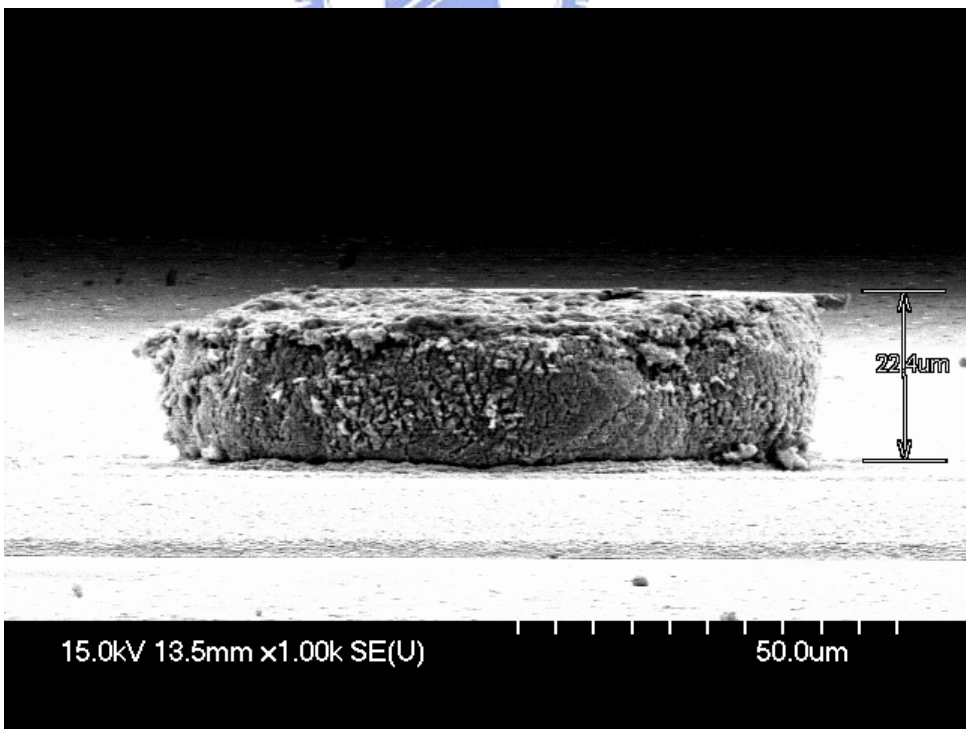

Fig. 5.15 SEM picture of a single bump after bonding.

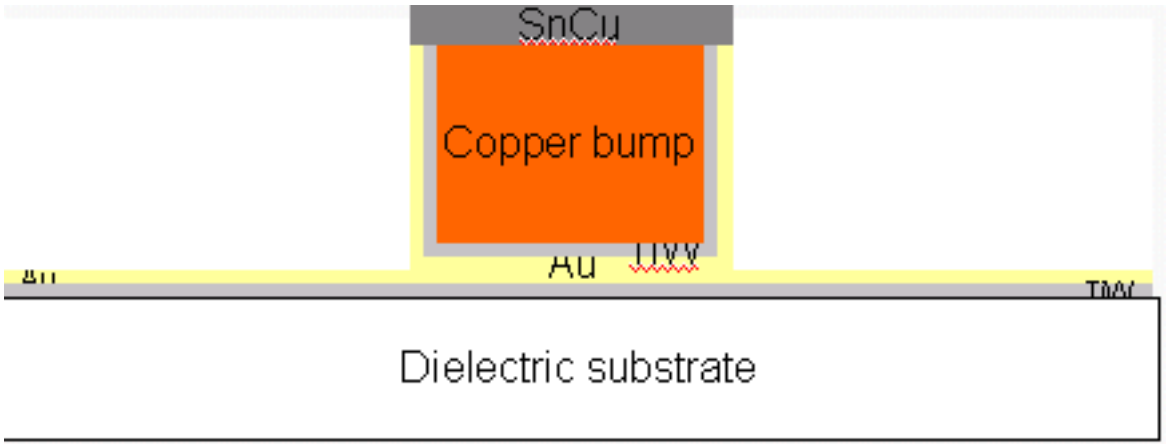

Fig. 5.16 Structure of a copper bump with cladding metals.

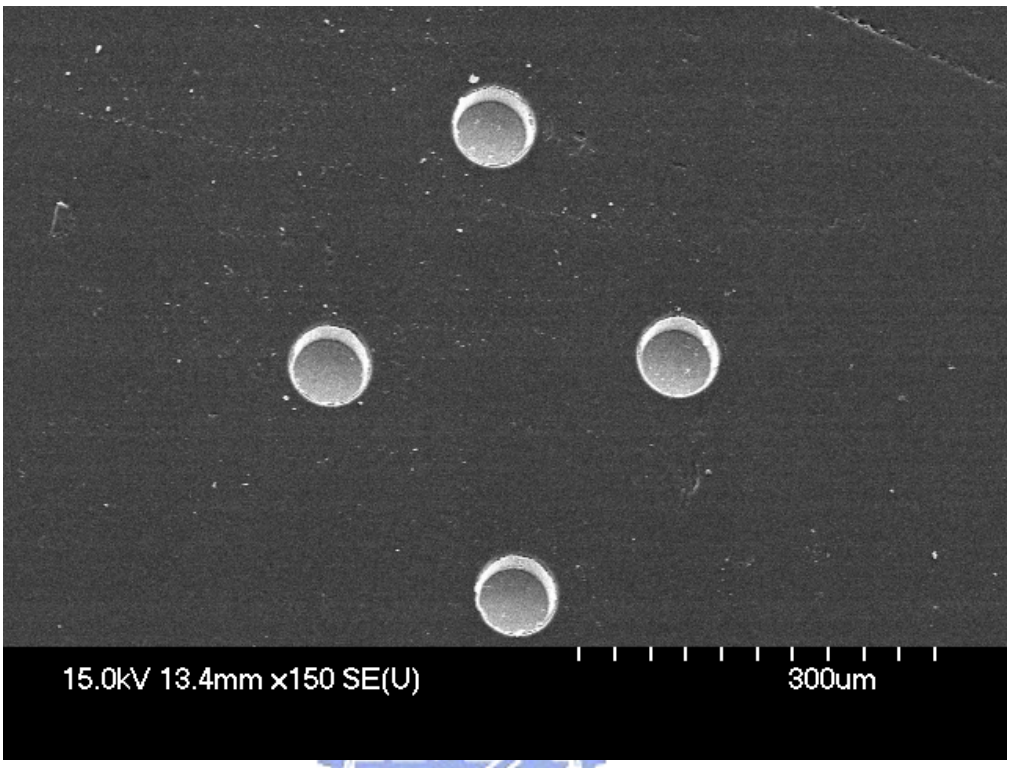

Fig. 5.17 Top view of the developed dry film with cladding metals.

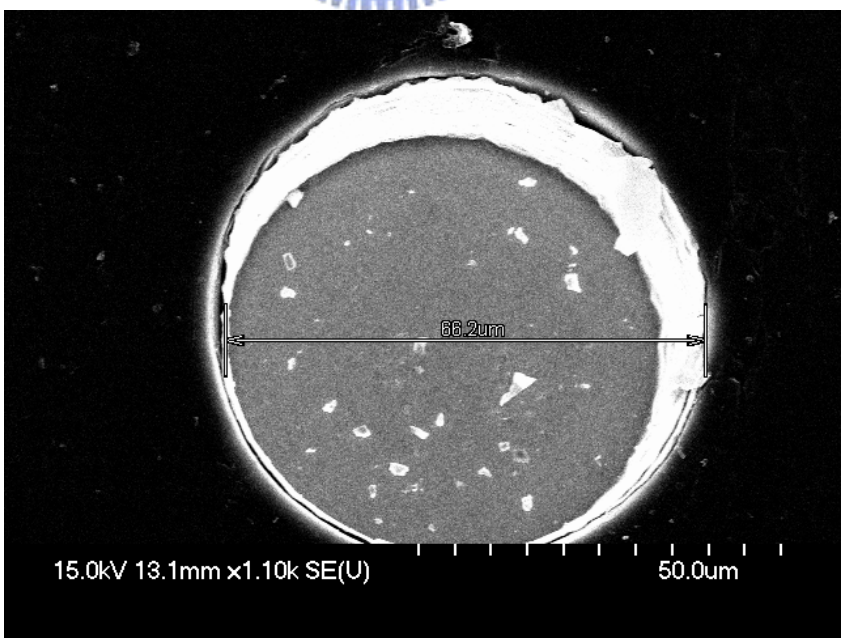

Fig.5.28 Detailed top view of the developed dry film with cladding metals.

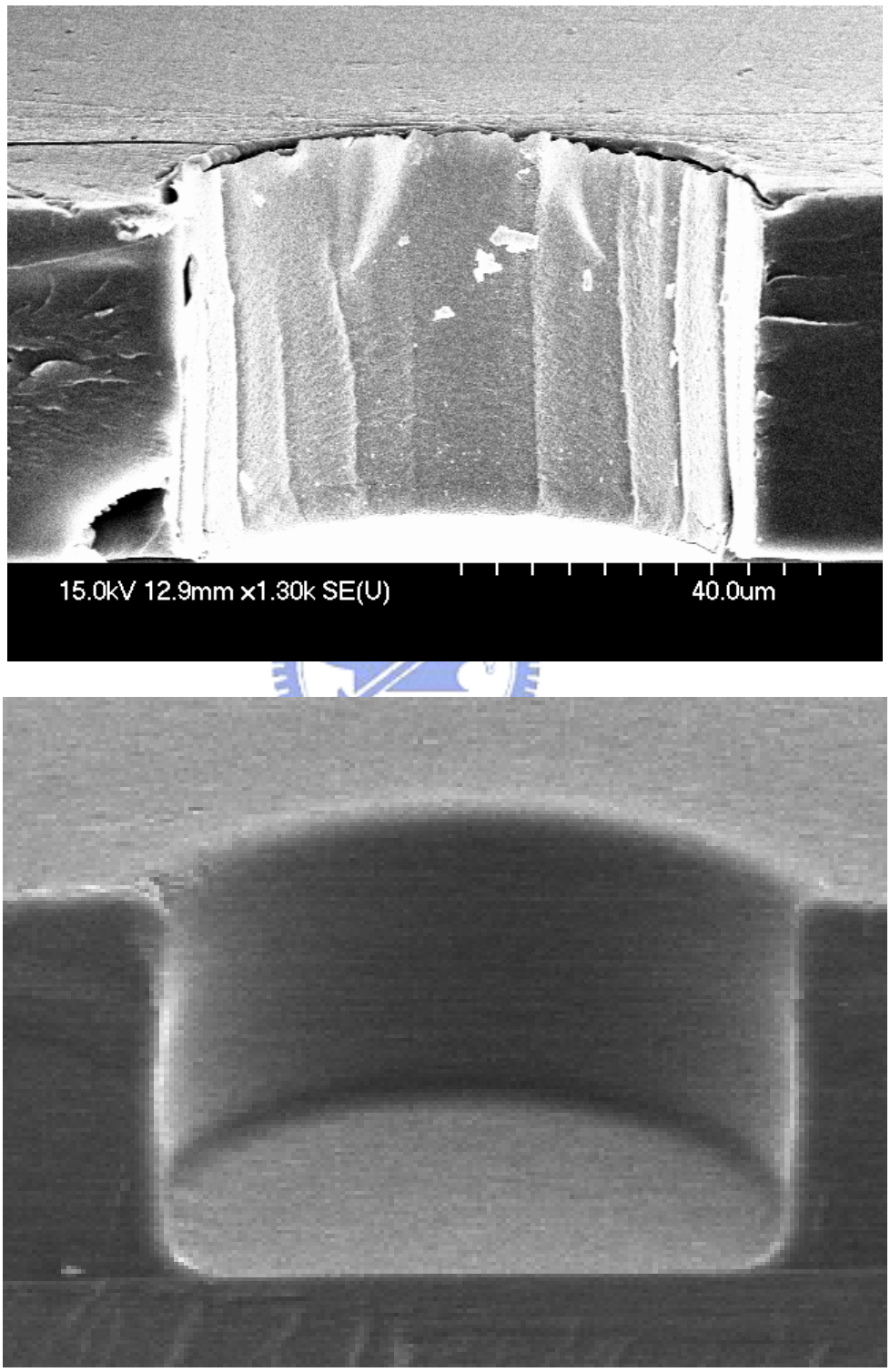

Fig. 5.19 Cross section of the developed dry film w/o cladding metals.

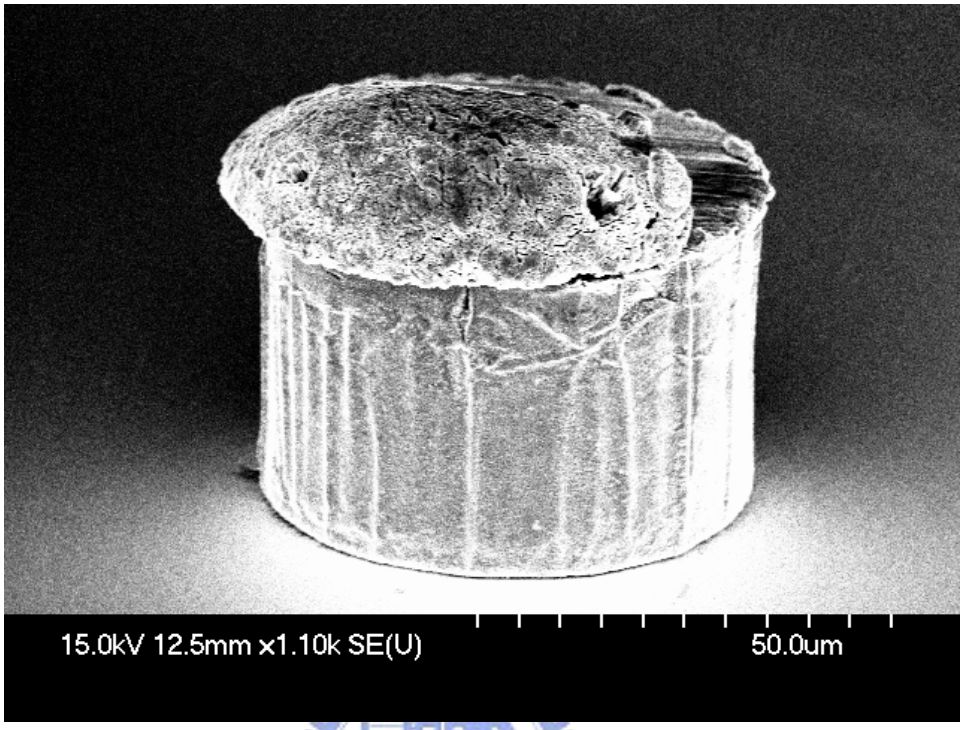

Fig. 5.20 SEM picture of a copper bump with cladding metals.

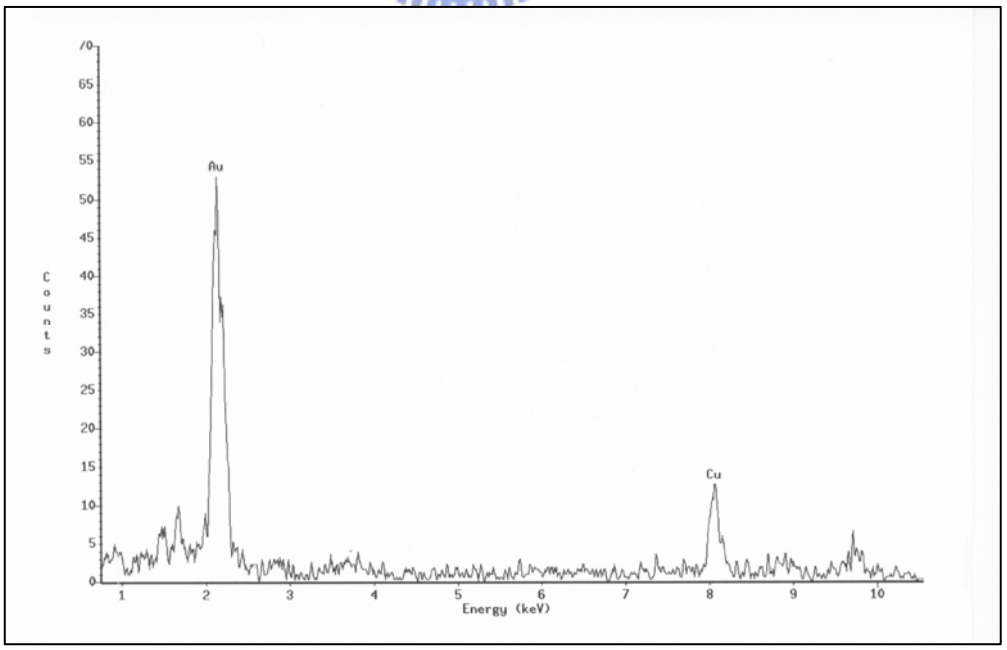

Fig. 5.21 EDX analysis of the cladding metals.

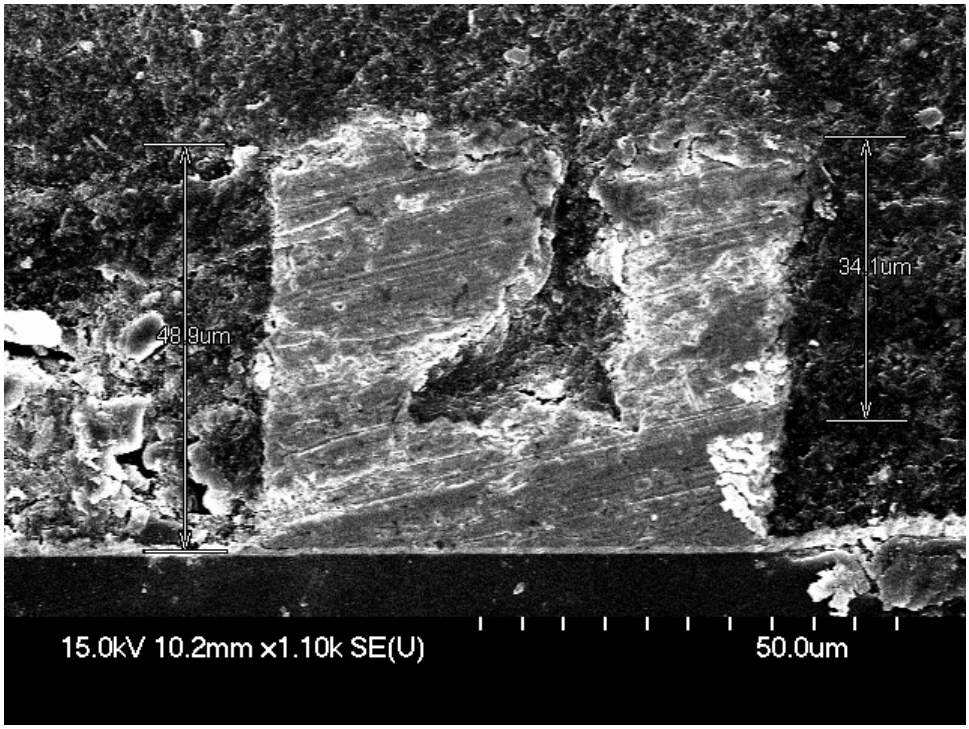

Fig. 5.22 The cross section of a 60μm copper bump with cladding metals.

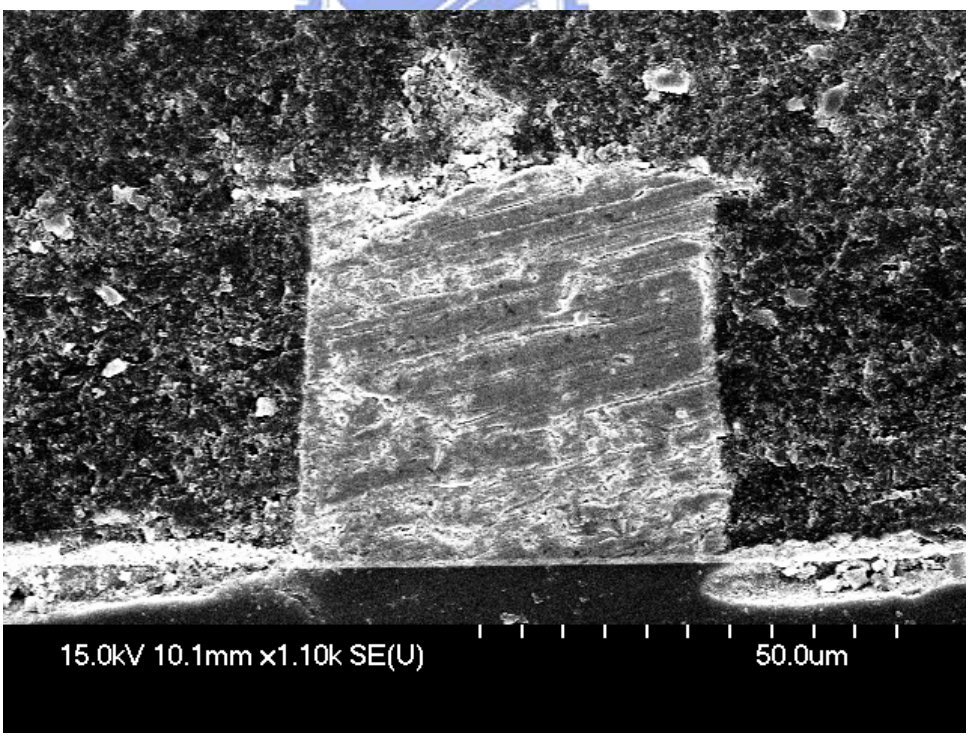

Fig. 5.23 The cross section of a 50μm copper bump with cladding metals.

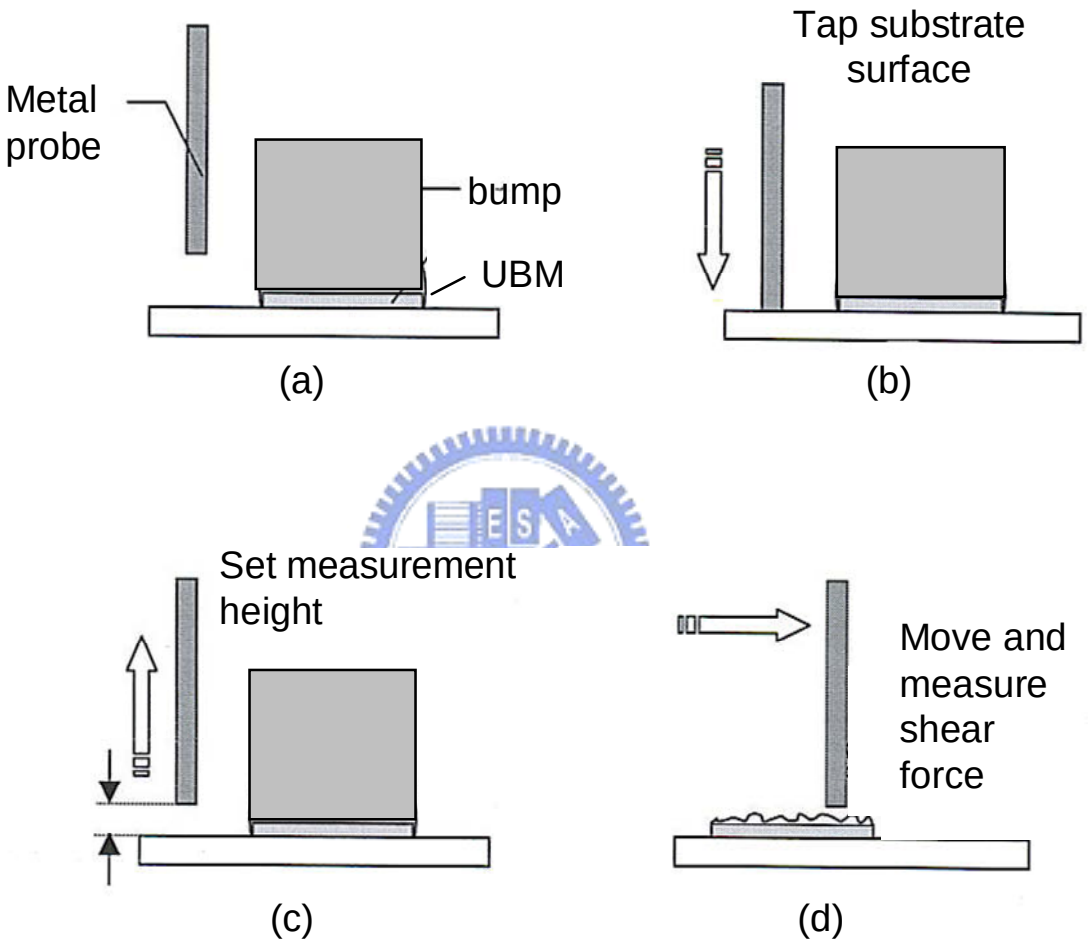

Fig. 5.24 Schematic diagram of the shear strength measurement

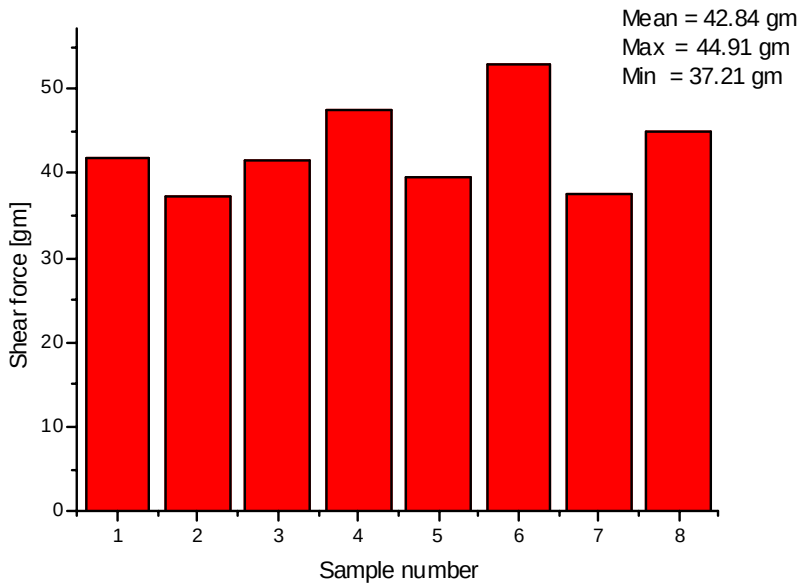

Fig. 5.25 Shear strength test results of eight gold bumps.

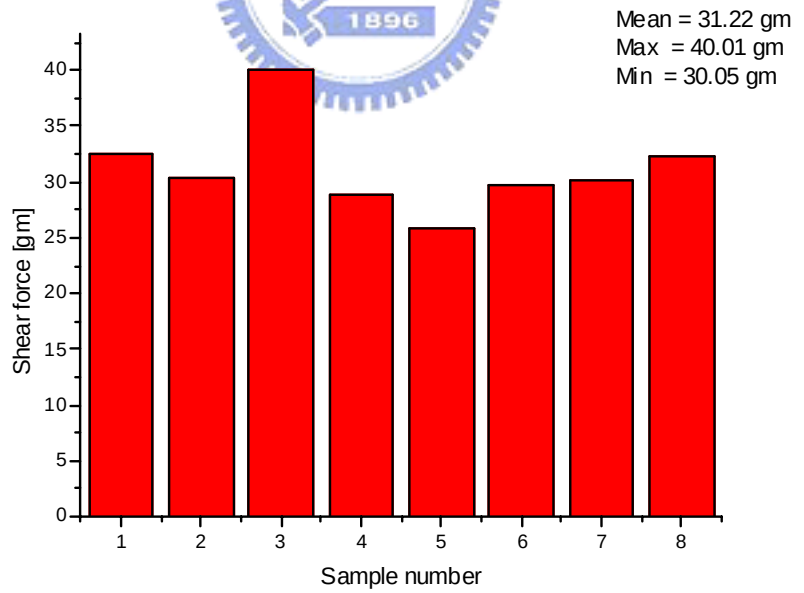

Fig. 5.26 Shear strength test results of eight copper bumps.

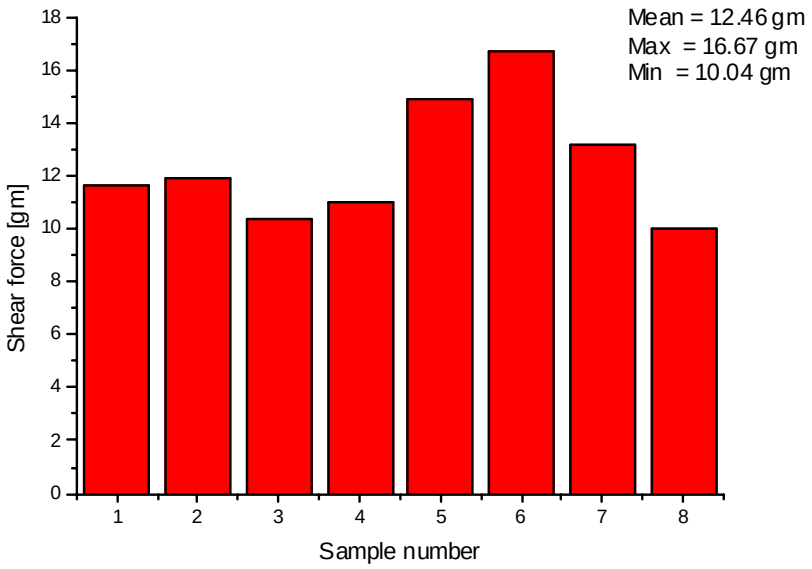

Fig. 5.27 Shear strength test results of eight SnCu bumps.

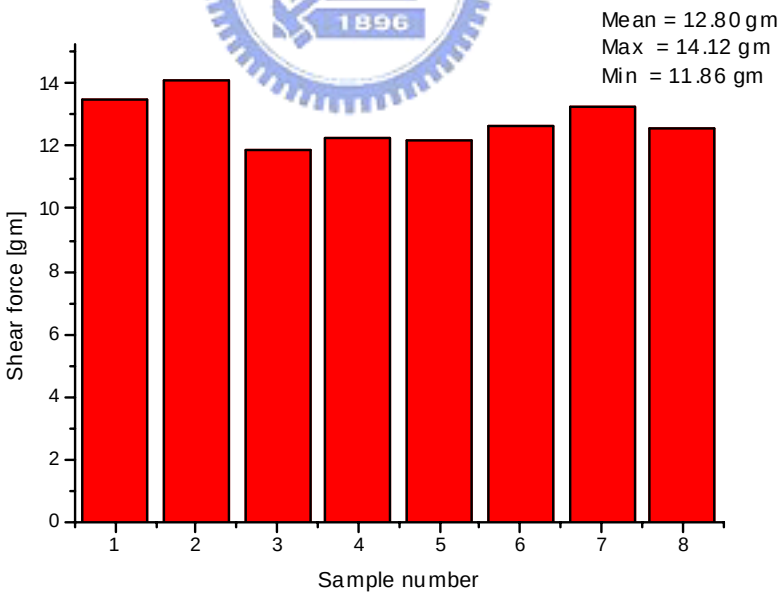

Fig. 5.28 Shear strength test results of eight SnAg bumps.

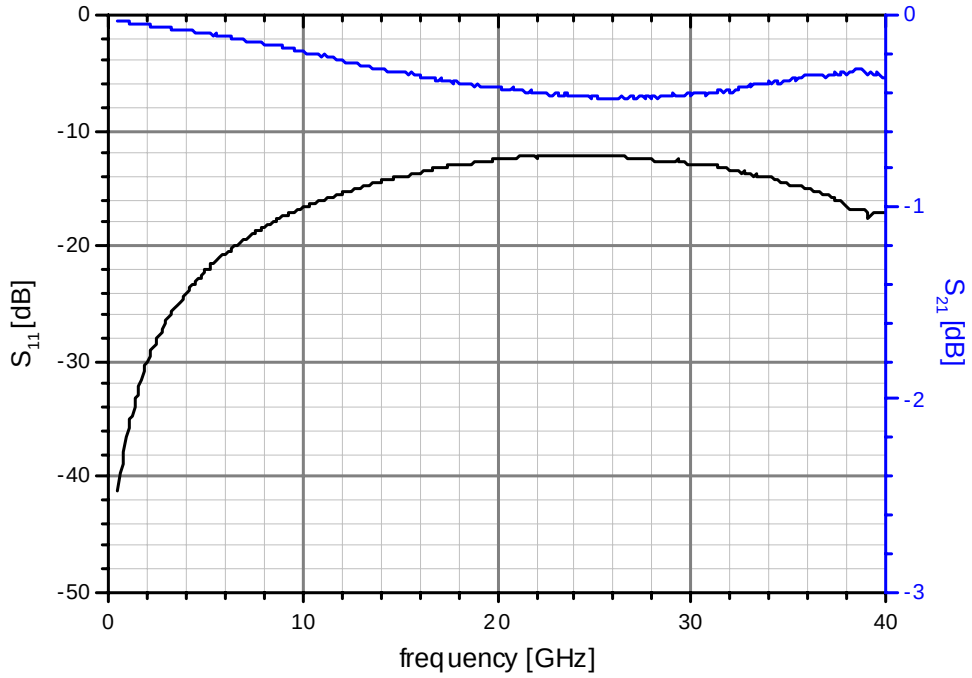

Fig. 5.29 Measured S-parameter of the bonding structure with gold bumps.

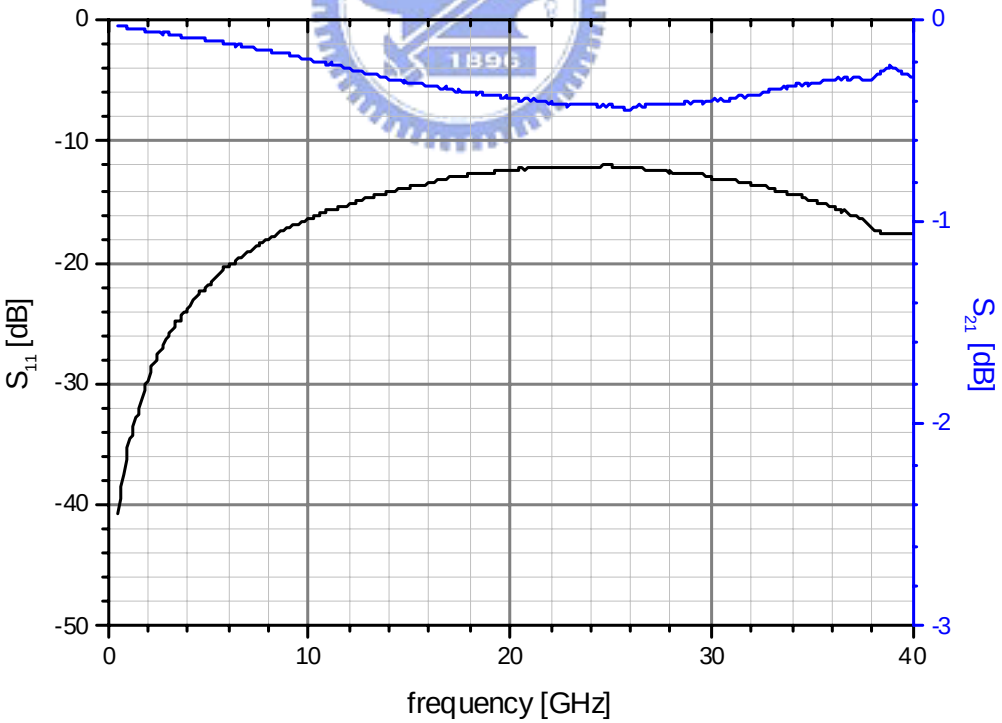

Fig. 5.30 Measured S-parameter of the bonding structure with copper bumps.

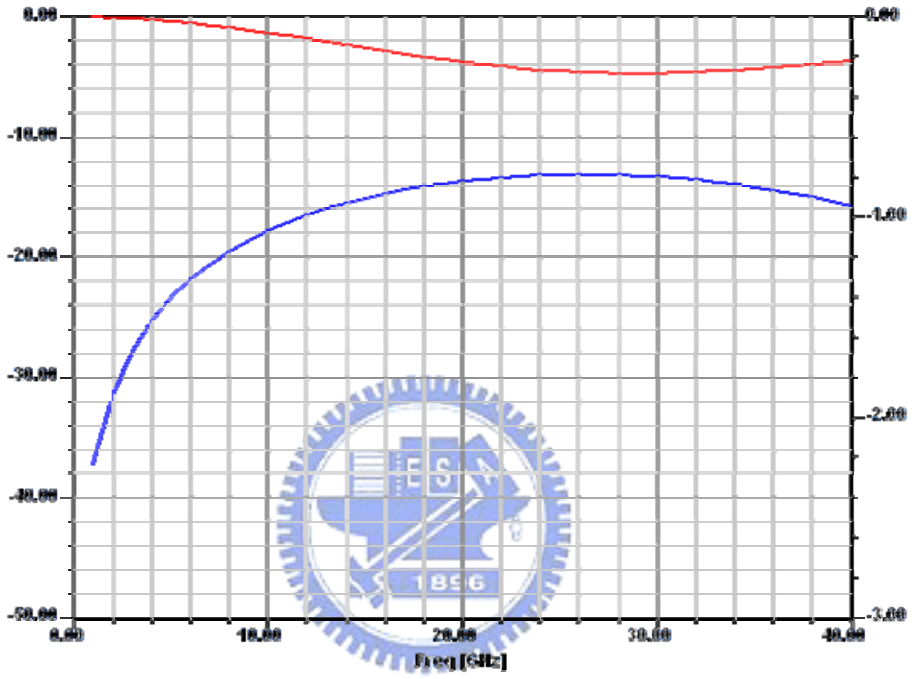

Fig. 5.31 Simulation S-parameter of the bonding structure.

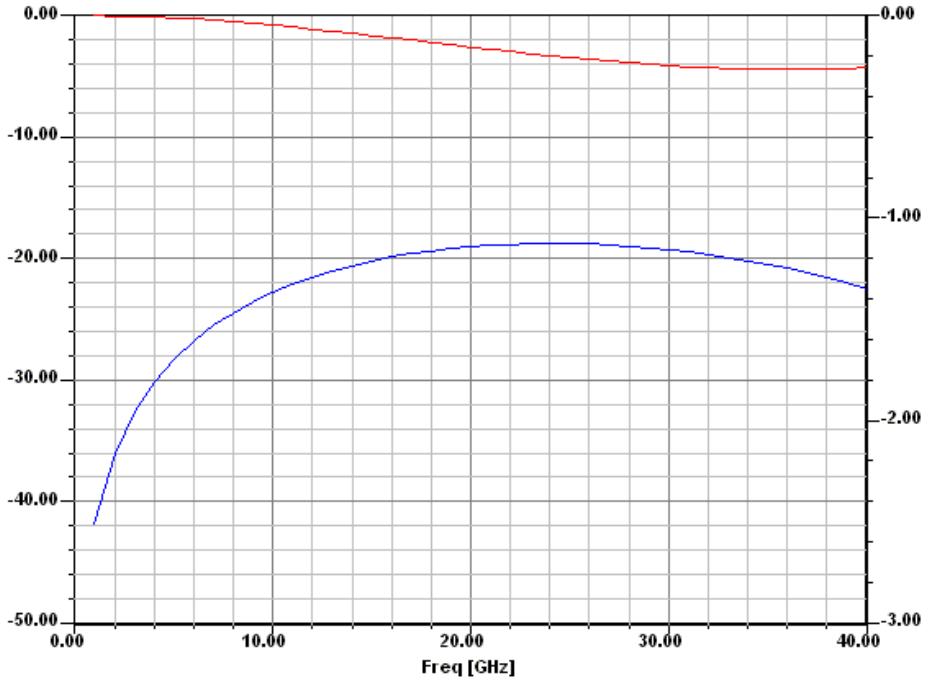

Fig. 5.32 Simulation S-parameter of the first bonding structure.

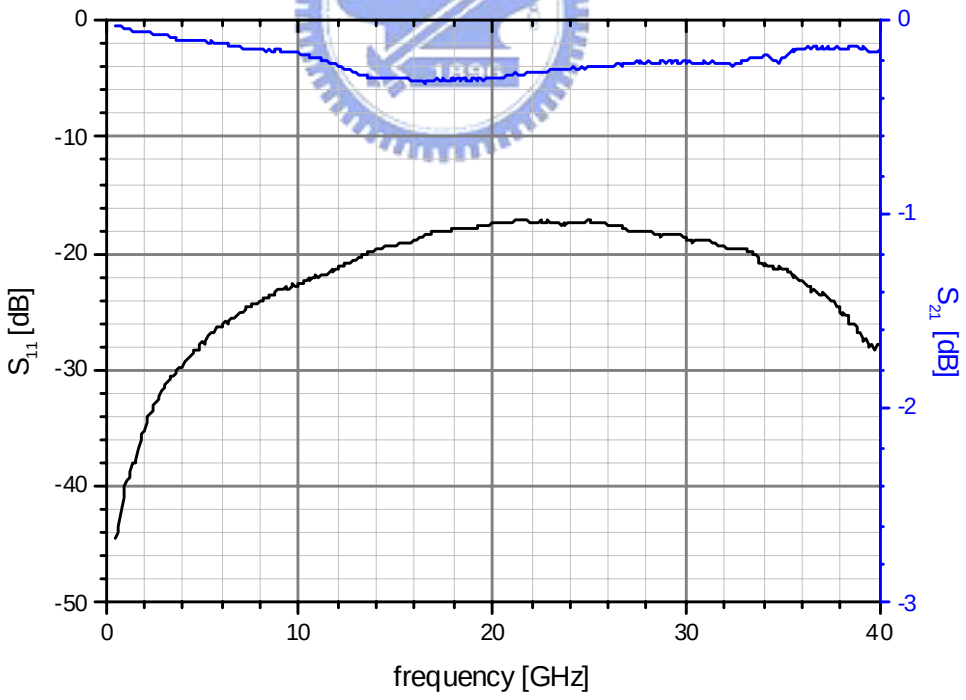

Fig. 5.33 Measured S-parameter of the first bonding structure.

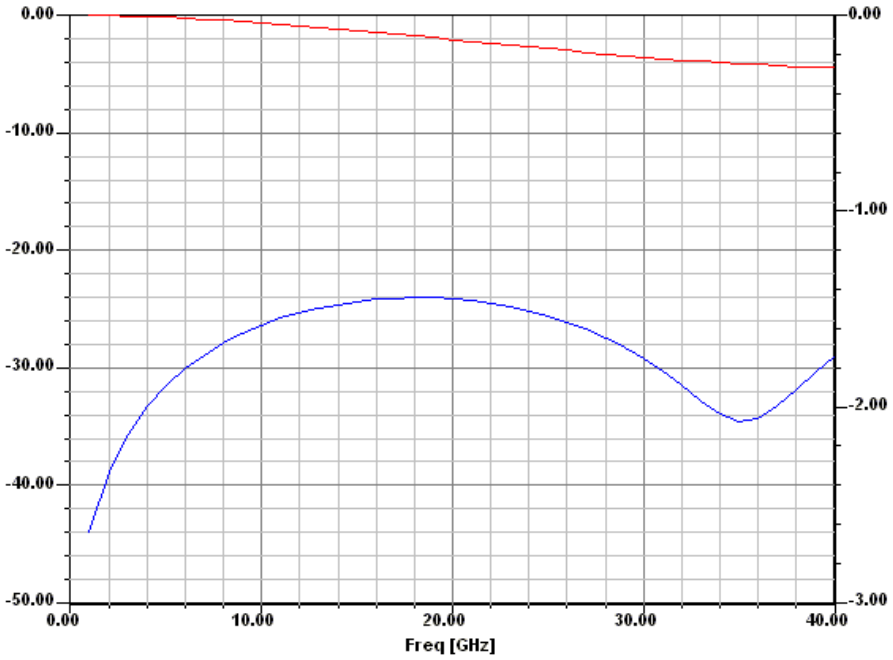

Fig. 5.34 Simulation S-parameter of the second bonding structure.

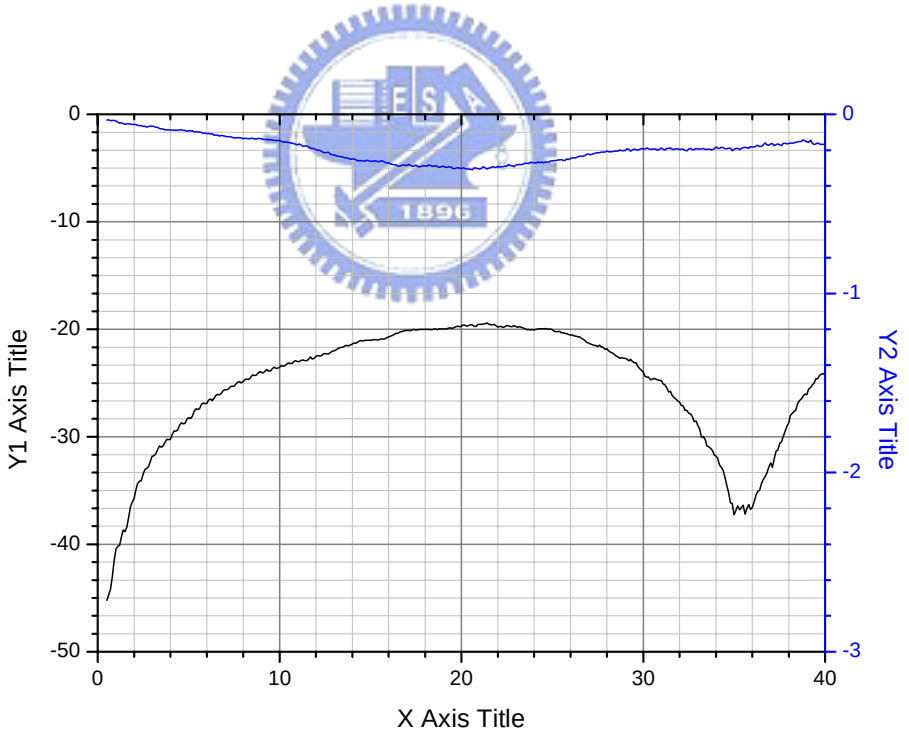

Fig. 5.35 Measured S-parameter of the second bonding structure.

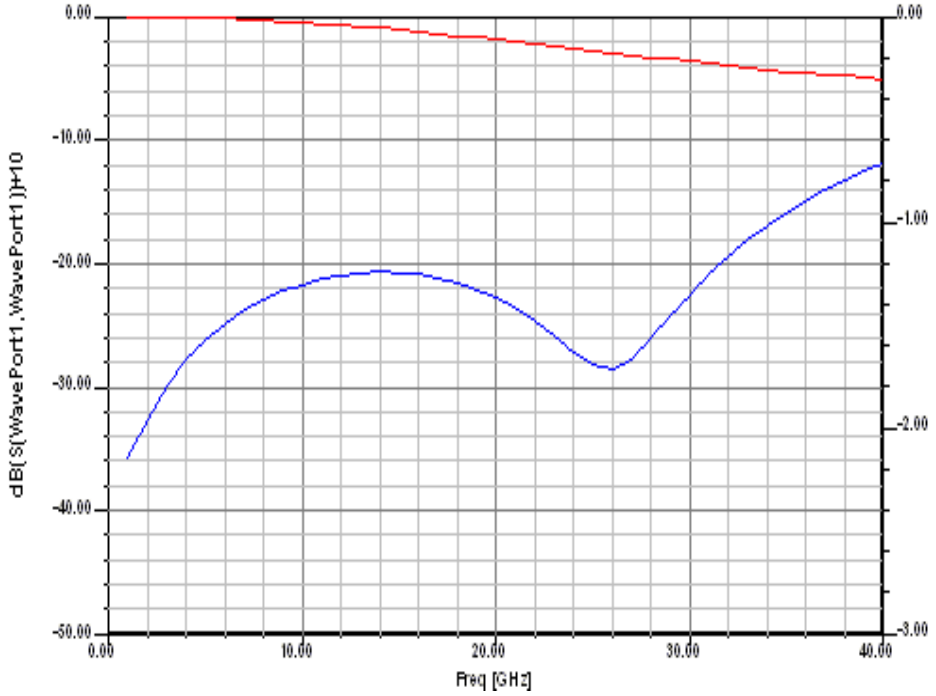

Fig. 5.36 Simulation S-parameter of the third bonding structure.

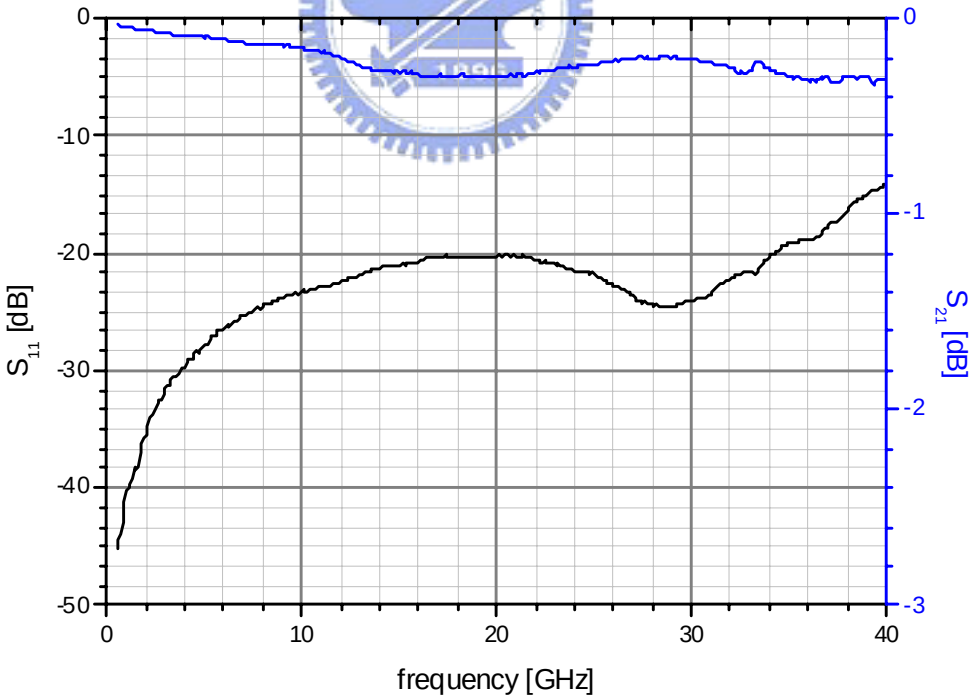

Fig. 5.37 Measured S-parameter of the third bonding structure.

Bump material	Plating time	Bump1 height	Bump2 height	Bump3 height	Bump4 height	Average height
Au	1hr	32 μm	31 μm	33 μm	31 μm	31.8 μm
Au	1.5hr	52 μm	58 μm	55 μm	50 μm	53.8 μm
Cu	1.5hr	33 μm	30 μm	45 μm	13 μm	30.3 μm
Cu	2hr	45 μm	48 μm	45 μm	44 μm	45.5 μm

Table 5.1 Uniformity of the plated gold and copper bumps.